```
#------------------------------
# innovus cmd list
#------------------------------
Puts
addAIORow
addAIoFiller
addBumpConnectTargetConstraint
addChannelDensityControl
addDeCap
addDeCapCellCandidates
addDummyBoundaryWires
addEndCap
addFiller
addFillerGap
addHaloToBlock
addHierInst
addInst
addInstToInstGroup
addIoFiller
addIoInstance
addIoRowFiller
addMimCap
addModulePort
addModuleToFPlan
addNet
addNetToNetGroup
addObjFPlanCutBox
addPGFTV
addPinToPinGroup
addPowerSwitch
addRepeaterByRule
addRing
addRoutingHalo
addSdpGroupMember
addSdpObject
```

addSizeBlockage
addSpareInstance
addSpecialRoute
addSplitPowerVia
addStripe
addTSV
addTieHiLo
addWellTap
add_cell_obs
add_clock_tree_source_group_roots
add_connection_to_neighbor_partition
add_decomp_filler
add_gate_array_filler
add_gui_marker
add_gui_shape
add_gui_text
add_interposer_route_block
add_line_end_track
add_ndr
add_oa_library_property
add_obj_on_bump
add_sai_boundary_flops
add_shape
add_tap_walls
add_target_pg
add_text
add_thru_substrate_insts
add_to_collection
add_tracks
add_via
add_via_definition
adjustFPlanChannel
alias
alignObject
alignPtnClone

all_analysis_views
all_clocks
all_connected
all_constraint_modes
all_delay_corners
all_fanin
all_fanout
all_hold_analysis_views
all_inputs
all_instances
all_library_sets
all_op_conds
all_outputs
all_rc_corners
all_registers
all_setup_analysis_views
analyze_esd_network
analyze_esd_voltage
analyze_ir_paths
analyze_joule_heat
analyze_package
analyze_paths_by_basic_path_group
analyze_paths_by_bottleneck
analyze_paths_by_clock_domain
analyze_paths_by_critical_false_path
analyze_paths_by_drv
analyze_paths_by_hier_port
analyze_paths_by_hierarchy
analyze_paths_by_view
analyze_rail
analyze_resistance
analyze_self_heat
analyze_signal_resistance
analyze_thermal
aocv_chip_size

aocv_core_size
append_to_collection
applyGlobalNets
assembleDesign
assemble_proto_model
assignBump
assignIoPins
assignPGBumps
assignPtnPin
assignSigToBump
assignTSV
assign_clock_tree_source_groups
attachDiode
attachIOBuffer
attachModulePort
attachTerm
auto_file_dir
auto_file_prefix
bindKey
bit_blasted_port_style
bitblast_ports
calNegSlack
calculate_ccopt_cannot_clone_reason
calculate_didt
calculate_differential_voltage
calculate_noise_margin
ccopt_add_exclusion_drivers
ccopt_design
ccopt_pro
changeBBoxMasterFromR0
changeBBoxMasterToR0
changeBumpMaster
changeCurrentDesign
changeFloorplan
changeIoConstraints

```
change_IB_cell_site_name
checkBondPadSpacing
checkBump
checkDesign
checkFPlan
checkFPlanSpace
checkFiller
checkFootPrint
checkHierRoute
checkMacroLLOnTrack
checkMultiCpuUsage
checkNetlist
checkPartitionSdc
checkPinAssignment
checkPlace
checkSdpGroup
checkTQuantusModelFile
checkTimingLibrary
checkUnique
checkWhatIfTiming
check_base_layer_density
check_bus_guides
check_ccopt_clock_tree_convergence
check_ccr
check_design
check_design_across_hierarchy
check_design_report_async_pins
check_design_report_scan_pins
check_design_threshold_fanout
check_instance_library_in_views
check_ldb_version
check_library
check_macro_place_constraint
check_module_model
check_noise
```

check_pg_library
check_power_intent
check_syntax
check_tcic
check_timing
check_tracks
check_ufc
ciopLoadBumpColorMapFile
cleanupExcludeNet
clearActiveLogicView
clearAllRulers
clearDeCapCellCandidates
clearDrc
clearGlobalNets
clearScanDisplay
clearSpareCellDisplay
clock_opt_design
cloneMSVGate
clonePlace
clonePtnObj
close_ctd_win
colorizePowerMesh
colorize_cell_library
commit_ccopt_clock_tree_route_attributes
commit_module_model
commit_power_intent
commit_pushdown_eco
comparePinAssignStatistics
compare_cellview
compare_collections
compare_instance_obs
compare_model_timing
compare_power_intent
compare_release
compress_special

congRepair
connectMacroFeedthrough
connect_clock_tree_mesh_drivers
convertBlackBoxToFence
convertFenceToBlackBox
convertFenceToLef
convert_gds_to_def
convert_lib_clock_tree_latencies
copyOaRestoreFiles
copyObject
copy_bump
copy_collection
createAbuttedFPlan
createActiveLogicView
createBasicPathGroups
createBusGuide
createBusNetGroup
createDensityArea
createExclusiveGroups
createFence
createGAFillerGroup
createGuide
createInstGroup
createInterfaceLogic
createIoRow
createLib
createLogicHierarchy
createMarker
createNetGroup
createPGPin
createPhysicalPin
createPinBlkg
createPinGroup
createPinGuide
createPipelineBusGuide

createPipelineNetGroup
createPlaceBlockage
createPtnCut
createPtnFeedthrough
createRegion
createRouteBlk
createRouteBlkAlongTrack
createRow
createRuler
createSdpGroup
createShield
createSignalPin
createSnapshot
createSoftGuide
createSpareModule
createSpecialDrcRegion
createSpecialMarkLayerShape
createStairwayBoundary
createTBOptFile
createTQuantusModelFile
createTSVNoLoadSPEF
createTrack
createUserBundleNet
createUserDisableForCombLoopBreak
createWhatIfInternalGeneratedClock
create_analysis_view
create_buffer_psPM_table
create_bump
create_bump_cluster
create_bump_grid
create_ccopt_clock_spine
create_ccopt_clock_tree
create_ccopt_clock_tree_source_group
create_ccopt_clock_tree_spec
create_ccopt_flexible_htree

create_ccopt_generated_clock_tree
create_ccopt_macro_model_spec
create_ccopt_preferred_cell_stripe
create_ccopt_skew_group
create_clock
create_constraint_mode
create_current_region
create_delay_corner
create_die_model
create_flexfiller_route_blockage
create_generated_clock
create_hier_view
create_histogram_png
create_inst_space_group
create_interposer_route_block
create_library_set
create_module_model
create_op_cond
create_parasitic_coordinate_transform
create_partition_wrapper
create_path_category
create_pg_model_for_macro_place
create_physical_partitions
create_power_pads
create_property_alias
create_proto_model
create_ps_per_micron_model
create_pushdown_eco
create_rc_corner
create_relative_floorplan
create_route_type
create_spice_deck
create_stress_rule
create_thermal_model
create_virtual_fin_bound_marker

create_virtual_shape_on_pg_wires
create_what_if_shape
ctd_save_histogram
ctd_save_view
ctd_show_skew_group
ctd_trace
ctd_win
cts_refine_clock_tree_placement
current_design
current_instance
cutBoxListFromPowerDomain
cutPowerDomainByOverlaps
cutRectilinearInst
cutRow
cvd
dbEdge
dbGet
dbQuery
dbSchema
dbSet
dbShape
dbTransform
db_browser
db_pt
db_rect
dbu2uu
dd_get
debugPtnBoundaryPorts
debug_irdrop
decompress_special
decrypt
defComp
defHierChar
defIn
defInCheckMaskShifts

defInShapeBasedDefFile
defOut
defOutBySection
defOutCompressVia
defOutLefNDR
defOutLefVia
defOutPolygonDieArea
defOverlapWireReportFileName
defStreamOutCheckUncolored
definePartition
define_add_on_module_model
define_bundled_bus
define_glitch_holding_resistance
define_proc_arguments
define_property
dehighlight
delaycal_default_net_delay
delaycal_default_net_load
delaycal_input_transition_delay
delaycal_rd_rnet_fraction_threshold
delaycal_support_min_max_pin_cap
delaycal_support_rise_fall_pin_cap
delaycal_support_wire_load_model
delaycal_use_default_delay_limit
deleteAIoFiller
deleteAllCellPad
deleteAllDensityAreas
deleteAllFPObjects
deleteAllInstGroups
deleteAllPowerPreroutes
deleteAllPtnCuts
deleteAllPtnFeedthroughs
deleteAllScanCells
deleteAllSignalPreroutes
deleteBNet

deleteBufferTree
deleteBumpConnectTargetConstraint
deleteBumps
deleteBusGuide
deleteCellEdgeSpacing
deleteCellEdgeType
deleteCellPad
deleteDangling1b1Or0s
deleteDanglingNet
deleteDanglingPort
deleteDeCap
deleteEmptyModule
deleteExclusiveGroups
deleteFPObject
deleteFiller
deleteGAFillerGroup
deleteHaloFromBlock
deleteInst
deleteInstFromInstGroup
deleteInstGroup
deleteInstPad
deleteIntegRouteConstraint
deleteIoFiller
deleteIoInstance
deleteIoRowFiller
deleteMimCap
deleteModule
deleteModulePort
deleteNet
deleteNetFromNetGroup
deleteNetGroup
deleteNetWeight
deleteNotchFill
deletePGPin
deletePartition

deletePinBlkg
deletePinFromPinGroup
deletePinGroup
deletePinGuide
deletePipelineNetGroup
deletePlaceBlockage
deletePowerSwitch
deletePtnCut
deleteRouteBlk
deleteRoutingHalo
deleteRow
deleteScanCell
deleteScanChain
deleteScanChainPartition
deleteSdpObject
deleteSecondaryPGNet
deleteSelectedFromFPlan
deleteShield
deleteSizeBlockage
deleteSpareModule
deleteTSV
deleteTieHiLo
deleteTrack
deleteUninstantiatedModules
deleteUserBundleNet
deleteWhatIfTimingAssertions
deleteWorkspace
delete_bump_grid
delete_ccopt_clock_spines
delete_ccopt_clock_tree_source_group
delete_ccopt_clock_tree_spec
delete_ccopt_clock_trees
delete_ccopt_flexible_htrees
delete_ccopt_preferred_cell_stripe
delete_ccopt_skew_groups

delete_cell_obs
delete_cell_stack_area
delete_cell_stack_group
delete_cell_virtual_align
delete_clock_tree_repeaters
delete_feedthru_buffer
delete_gui_object
delete_inst_space_group
delete_path_category
delete_pg_keepout
delete_relative_floorplan
delete_route_type
delete_thru_substrate_insts
deriveTimingBudget
deselectAll
deselectBusGuide
deselectGroup
deselectIOPin
deselectInst
deselectInstByCellName
deselectInstOnNet
deselectModule
deselectNet
deselectPin
deselectSecondaryPGNet
deselect_bump
deselect_obj
detachModulePort
detachSdpGroup
detachTerm
detailRoute
disconnectDanglingPort
displayBufTree
displayScanChain
displaySpareCell

displayUserBundleNet
display_obj_connectivity
display_temperature_result
display_timing_map
distributed_mmmc_disable_reports_auto_redirection
do_extract_model
dumpCongestArea
dumpMultiBitFlopMappingFile
dumpNanoCongestArea
dumpNetsInCongestedArea
dumpOutVias
dumpPictures
dumpToGIF
dump_histogram_view
dump_unannotated_nets
earlyGlobalRoute
ecoAddBacksideConstraint
ecoAddRepeater
ecoChangeCell
ecoClone
ecoCloneFlop
ecoCloneInstGroup
ecoCompareNetlist
ecoDefIn
ecoDeleteRepeater
ecoDesign
ecoDisableNetRenamingForFlatNetlist
ecoMergeCombinationalCell
ecoOaDesign
ecoPlace
ecoRemoveTiedInputs
ecoRoute
ecoSplitCombinationalCell
ecoSplitComplexFlop
ecoSplitFlop

ecoSwapSpareCell
eco_opt_ir_aggressor
editAddFillet
editAddPoly
editAddRoute
editAddTrimMetal
editAddVia
editAdjust
editBumpConnectTargetConstraint
editChangeLayer
editChangeMask
editChangeNet
editChangeRule
editChangeStatus
editChangeVia
editCommitPoly
editCommitRoute
editCopy
editCutWire
editDelete
editDeleteFillet
editDeselect
editDuplicate
editFixWideWires
editMerge
editMove
editPin
editPowerVia
editResize
editRotate
editSelect
editSplit
editTrim
edit_bump_name
enable_legacy_metric

encEnableMetric
encMessage
enc_partial_cmd_argument_matching
enc_print_full_message_summary
enc_save_binary_timing_constraints
enc_save_timing_constraints_always
enc_source_continue_on_error
enc_source_echo_filename
enc_source_verbose
enc_source_verbose_cmd_print_length_limit
enc_source_verbose_output
enc_tcl_error_info
enc_tcl_report_header_with_value
enc_tcl_return_display_limit
encrypt
encrypt_thermal_file
endECO
end_parallel_edit
end_sai
eval_common_ui
exportNdr
exportPowerSwitch
extractRC
extract_metal_density
extract_package
extract_shrink_factor
fcroute
fillNotch
fill_setting_save
filter_collection
findLefEquivalentCells
findPinPortNumber
find_global
finishFloorplan
fit

fixACLimitViolation
fixAllIos
fixBondPad
fixVia
fix_boundary_overlaps
fix_drc_with_patch
fix_feedthru_assign
fix_floorplan
fix_multi_drivers
fix_pg_antenna
flattenCoverCell
flattenIlm
flattenPartition
flipModule
flipOrRotateObject
flipSdpObject
flipchip_allow_routed_bump_edit
floorPlan
foreach_in_collection
fp_vertical_row
free_memory_of_compressed_objects
free_power_intent
genPinText
generateCapTbl
generateFFSetupFile
generateLef
generateRCFactor
generateVias
generate_esd_rlrp_report
generate_fence
generate_pg_library
generate_power_up_report
generate_tech_pg_lib
generate_vertical_cell_edge_constraint
generate_xpgv

getActiveLogicViewMode
getAddRingMode
getAddStripeMode
getAllLayers
getAnalysisMode
getAttribute
getBlackBoxArea
getBondPad
getBudgetingMode
getBuildArch
getCPFUserAttributes
getCheckMode
getClonePtnOrient
getCmdLogFileName
getCompressLevel
getDbGetMode
getDelayCalMode
getDensityMapMode
getDesignMode
getDistributeHost
getDrawView
getEcoMode
getEditMode
getEndCapMode
getExportMode
getExtractRCMode
getFPlanMode
getFillerMode
getFinishFPlanMode
getFlipChipMode
getGenerateViaMode
getHierMode
getIlmMode
getIlmType
getImportMode

getInstPowerDomain
getIntegRouteConstraint
getIoFlowFlag
getLatencyFile
getLayerPreference
getLogFileName
getModuleView
getMsvMode
getMultiCpuUsage
getNanoRouteMode
getNetWeight
getOaxMode
getObjFPlanBoxList
getObjFPlanPolygon
getOptMode
getPGNetResis
getPGPinUseSignalRoute
getPinAssignMode
getPinConstraint
getPinDensityMapMode
getPlaceMode
getPreference
getPtnPinStatus
getRailPrototypeMode
getResizeFPlanMode
getRouteMode
getSIMode
getScanReorderMode
getSchedulingFile
getSdpGroupAttribute
getSdpMode
getSignoffOptMode
getSpecialNetResis
getSrouteMode
getStreamOutMode

getTieHiLoMode
getTimeLibFile
getUPFPortAttr
getUsefulSkewMode
getValidPowerSwitchLocation
getVersion
getViaGenMode
getWhatIfTimingAssertions
getWhatIfTimingMode
get_abstract_mode
get_activity
get_add_target_pg_mode
get_analysis_view
get_arcs
get_capacitance_unit
get_ccopt_clock_spines
get_ccopt_clock_tree_capacitance
get_ccopt_clock_tree_cells
get_ccopt_clock_tree_nets
get_ccopt_clock_tree_sinks
get_ccopt_clock_tree_slew
get_ccopt_clock_tree_source_groups
get_ccopt_clock_trees
get_ccopt_dag_traversal
get_ccopt_delay_corner
get_ccopt_effective_max_capacitance
get_ccopt_flexible_htrees
get_ccopt_preferred_cell_stripe
get_ccopt_property
get_ccopt_skew_group_delay
get_ccopt_skew_group_path
get_ccopt_skew_groups
get_cells
get_clock_network_objects
get_clocks

get_constant_for_timing
get_constraint_mode
get_ctd_win_id
get_ctd_win_title
get_default_switching_activity
get_delay_corner
get_designs
get_dynamic_power_simulation
get_equivalent_cells
get_generated_clocks
get_glitch_threshold
get_global
get_interactive_constraint_modes
get_ir_insight
get_lib_arcs
get_lib_cell_leakage_power
get_lib_cells
get_lib_clock_tree_path_delay
get_lib_pg_pins
get_lib_pins
get_library_set
get_libs
get_macro_place_constraint
get_message
get_metric
get_multi_input_switching_mode
get_nets
get_oa_default_rule_lib
get_object_name
get_op_cond
get_path_groups
get_pba_mode
get_pg_nets
get_pg_pins
get_physical_info

get_pins
get_ports
get_power
get_power_analysis_mode
get_power_intent_restricted_hinsts
get_propagated_clock
get_property
get_proto_design_mode
get_proto_mode
get_proto_model
get_ptn_fplan_mode
get_rc_corner
get_reinforce_pg_mode
get_resistance_unit
get_sdc_mode
get_signal_em_analysis_mode
get_snap_grid_info
get_socv_rc_variation_factor
get_socv_reporting_nsigma_multiplier
get_time_unit
get_trace_obj_connectivity_mode
get_verify_drc_mode
get_via_pillars
get_visible_bumps
get_visible_netGroups
get_visible_nets
get_well_tap_mode
globalDetailRoute
globalNetConnect
globalRoute
group
group_instance_suffix
group_path
gui_attach_to_cursor
gui_clear_highlight_safety_mechanism

gui_clear_trace_flightline
gui_close_cell_view
gui_deselect
gui_dim_foreground
gui_dump_picture
gui_get_legend
gui_get_schematic
gui_group_hinst
gui_highlight_safety_mechanism
gui_open_cell_view
gui_report_trace_flightline
gui_save_flightline
gui_schematic_add_selected
gui_schematic_load_view
gui_schematic_save_view
gui_select
gui_set_legend
gui_show_edge_number
gui_trace_flightline
gui_ungroup_hinst
gui_verbose
gui_zoom_ctd
handlePtnAreaIo
help
highFreqInterposerFlow
highlight
highlightSyncObj
highlight_pin
highlight_pin_connection
highlight_timing_report
hiliteFeedthroughNets
hilite_proto_model
identify_proto_model
ignore_max_via_stack_rule
importPowerSwitch

```
import_ilm_data
import_module_model
index_collection
initCoreRow
initECO
init_abstract_view
init_check_output_pin_constant
init_cpf_file
init_design
init_design_netlisttype
init_design_settop
init_design_uniquify
init_enable_drc_region_layer
init_gnd_net
init_hier_cell
init_ignore_pgpin_polarity_check
init_import_mode
init_io_file
init_layout_view
init_lef_check_antenna
init_lef_check_mask_shifts
init_lef_file
init_ml
init_mmmc_file
init_mmmc_version
init_no_new_assigns
init_oa_default_rule
init_oa_design_cell
init_oa_design_lib
init_oa_design_view
init_oa_foundry_rule
init_oa_ref_lib
init_oa_search_lib
init_oa_special_rule
init_original_verilog_files
```

init_power_intent_file
init_pwr_net
init_top_cell
init_verilog
init_verilog_tolerate_port_mismatch
inn_save_lef_ignore_abstracts
innovus
insertPtnFeedthrough
insert_physical_cell
ioInstOverlapCheck
is_common_ui_mode
justifyBudget
justifyException
layerNameNoAbbreviation
lefDefOutVersion
lefExtend2DCellShapes
lefExtendCellObsShapeUnderTrim
lefIgnoreLayerNames
lefdefInputCheckColoredShape
legalizeFPlan
legalizePin
lib_build_asynch_de_assert_arc
lineSelect
list_gui_marker
list_libraries
list_property
lminus
loadBlackBoxNetlist
loadDefFile
loadDrc
loadECO
loadFPlan
loadFootPrint
loadIoFile
loadLefFile

loadPtnPin
loadSpecialRoute
loadViolationReport
loadWorkspace
load_netlist_ignore_undefined_cell
load_path_categories
load_timing_debug_report
man
map_activity_file
map_die_package
map_dies
mark_physical_power_domains
merge_clock_cells
merge_hierarchical_def
merge_model_timing
merge_multi_port_to_single_port
merge_pg_library
merge_vtm
metric_advanced_url_endpoint
metric_capture_3d_hotspots
metric_capture_depth
metric_capture_design_image
metric_capture_design_image_blockages
metric_capture_design_image_blockages_threshold
metric_capture_design_image_power_intent
metric_capture_design_image_route_drc
metric_capture_max_drc_markers
metric_capture_min_count
metric_capture_overwrite
metric_capture_pba_tns_histogram
metric_capture_per_view
metric_capture_reg2reg_metrics
metric_capture_timing_analysis_mode
metric_capture_timing_path_groups
metric_capture_timing_paths

metric_capture_tns_histogram
metric_capture_tns_histogram_buckets
metric_capture_tns_histogram_max_slack
metric_capture_tns_histogram_paths
metric_capture_vth_metrics
metric_capture_vth_per_power_domain
metric_category_default
metric_current_run_id
metric_enable
metric_summary_metrics
modifyBudget
modifyPipelineNetGroup
modifyPowerDomainAttr
modify_ccopt_skew_group
modify_ndr
monitor_hosts
moveGroupPins
moveMacroInsideModule
movePowerSwitch
moveSdpObject
move_obj
mustjoinallports_is_one_pin
oaIn
oaOut
open_gtd
open_schematic
optDesign
optPower
optVirtual
pack_align_macros
pack_module_model_libs
pan
panCenter
panPage
parse_proc_arguments

partition
partitionPushSpecialWires
pasteObject
pinAlignment
pinAnalysis
placeAIO
placeBondPad
placeCursor
placeInstance
placeJtag
placePIO
placePad
placePadIO
placePipeline
placeSdpGroup
placeSpareModule
place_cells_at_center_for_feedthrus
place_connected
place_design
place_opt_design
place_partition_clone
power_integrity_place
predict_floorplan
prepareForEcoRoute
print_message
propagate_activity
proto_design
pull_block_constraint
push_ptn_network
queryDensityInBox
queryFPlanObject
queryPinDensity
query_objects
query_power_data
range_collection

rcOut
readBumpLocation
readDieAbstract
readFlipChipProperty
readIoUpdate
readPackage
readSdpFile
readTSVConfig
readTransitionFile
readWriteLefCheckUncoloredShapes
read_activity_file
read_codesign_die_abstract
read_design_stack_config
read_ilm_eco_db
read_instance_obs
read_name_mapping
read_parallel_edit_files
read_parasitics
read_path_descriptions
read_physical_context_data
read_power_intent
read_power_rail_results
read_sai
read_sdf
read_spdf
read_stream
read_taf
read_temperature_map_file
read_twf
rechainPowerSwitch
reclaimArea
recreatePtnCellBlockage
redirect
redo
redraw

refineMacro
refinePlace
refine_macro_place
registerTrigger
register_gui_edit_callback
reinforce_pg
relink_db_files
remove_assigns
remove_from_collection
remove_gui_marker
rename_obj
rename_pg_library
replaceLefMacro
replacePowerSwitch
replace_proto_model
reportAlwaysOnBuffer
reportCapViolation
reportCellPad
reportCongestArea
reportCongestion
reportConnectivity
reportCritInstance
reportCritNet
reportCritTerm
reportDanglingNet
reportDanglingPort
reportDeCap
reportDeCapCellCandidates
reportDelayCalculation
reportDensityMap
reportFanoutViolation
reportFootPrint
reportFreqViolation
reportGateCount
reportIgnoredNets

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reportIlmStatus
reportInstPad
reportIsolation
reportJtagInst
reportLegalWireWidthForBump
reportLengthViolation
reportMultibit
reportNetGroup
reportNetStat
reportPathGroupOptions
reportPinAssignStatistics
reportPinDensityMap
reportPipeline
reportPowerDomain
reportPowerRoute
reportPowerSwitch
reportProbePins
reportRC
reportRoute
reportRouteTypeConstraints
reportScanCell
reportScanChainPartition
reportSeedConnection
reportSelect
reportShield
reportShifter
reportSpecialRoute
reportTimingLib
reportTranViolation
reportTwoPinChain
reportUnalignedNets
reportUnsnapBlocks
reportVoltage
reportVtInstCount
reportWire
```

reportWirePath
report_analysis_coverage
report_analysis_summary
report_analysis_views
report_annotated_assertions
report_annotated_check
report_annotated_delay
report_annotated_parasitics
report_annotations
report_aocv_derate
report_area
report_bundled_bus
report_case_analysis
report_ccopt_cell_filtering_reasons
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timing_report_drv_per_frequency_per_input_slew
timing_report_drv_use_worst_timing_slack
timing_report_enable_clock_to_for_unconstrained_paths
timing_report_enable_clock_unrolling
timing_report_enable_cppr_point
timing_report_enable_em_index_clipping_report
timing_report_enable_lead_trail_to_rise_fall_map
timing_report_enable_markers
timing_report_enable_max_capacitance_drv_for_constants
timing_report_enable_max_path_limit_crossed
timing_report_enable_report_clock_timing_across_clock_p
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timing_report_enable_si_debug
timing_report_enable_slack_summary_at_bottom
timing_report_enable_unique_pins_multiple_capture_clock
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timing_report_enable_use_valid_start_end_points
timing_report_generated_clock_info
timing_report_group_based_mode
timing_report_max_transition_check_using_nsigma_slew

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timing_report_pulse_width_matching_launch_capture_paths
timing_report_redirect_message_types
timing_report_retime_formatting_mode
timing_report_skip_constraint_loop_check
timing_report_socv_summary_mean_sigma
timing_report_timing_header_detail_info
timing_report_unconstrained_path_early_late_header
timing_report_unconstrained_paths
timing_report_use_receiver_model_capacitance
timing_report_use_worst_parallel_cell_arc
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timing_sdf_adjust_negative_setuphold
timing_sdf_enable_setuphold_scond_ccond
timing_self_loop_paths_no_skew
timing_self_loop_paths_no_skew_max_depth
timing_self_loop_paths_no_skew_max_slack
timing_set_clock_source_to_output_as_data
timing_set_nsigma_multiplier
timing_set_scaling_for_negative_checks
timing_set_scaling_for_negative_delays
timing_socv_preserve_variation_with_annotations
timing_socv_rc_variation_mode
timing_socv_statistical_min_max_mode
timing_socv_view_based_nsigma_multiplier_mode
timing_spatial_derate_chip_size
timing_spatial_derate_distance_mode
timing_suppress_escape_characters
timing_suppress_ilm_constraint_mismatches
timing_time_unit
timing_timing_window_pessimism_removal_include_si_delay
timing_use_clock_pin_attribute_for_clock_net_marking
timing_use_incremental_si_transition
timing_use_latch_early_launch_edge

timing_use_latch_time_borrow
timing_use_verilog_for_model_netlist
timing_waveform_aware_pulse_width_checks_high_voltage_level
timing_waveform_aware_pulse_width_checks_low_voltage_level
timing_write_sdf_no_escape_backslash_control
trPrintIgnoredPadNets
traceJtag
trace_obj_connectivity
translateSNDCSetupFile
trimDesign
trimMetalFillNearNet
trim_pg
trim_pg_library
uiAdd
uiDelete
uiFind
uiGet
uiGetRecordObjByInfo
uiSet
uiSetTool
ui_view_box
unassignBump
unassignTSV
undo
undo_uniquify_partition
unfixAllIos
unfixBondPad
unfixBump
unflattenIlm
ungroup
uniquify
uniquify_partition
unloadPtnPin

unlockOaDesign
unplaceAllBlocks
unplaceAllGuides
unplaceAllInsts
unplaceGuide
unplaceGuideConstraints
unplaceJtag
unregister_gui_edit_callback
unsetFixedBlockSize
unsetMessageLimit
unsetPinConstraint
unsetProbePin
unset_ccopt_property
unspecifyBlackBox
unspecifyIlm
unspecifyJtag
unspecifySelectiveBlkgGate
unsuppressMessage
update_analysis_view
update_bus_guide
update_ccopt_clock_tree
update_clock_latencies
update_clock_tree_source_latency
update_clock_tree_spec_annotations
update_constraint_mode
update_delay_corner
update_floorplan_for_macro_place
update_glitch
update_io_latency
update_library_set
update_module_model
update_names
update_oa_lib
update_partition
update_rc_corner

uu2dbu
vPuts
validate_pg_library
verifyACLimit
verifyConnectivity
verifyCutDensity
verifyEndCap
verifyFlipChipRoutingConstraints
verifyIO2BumpConnectivity
verifyIsolatedCut
verifyMetalDensity
verifyPowerDomain
verifyPowerSwitch
verifyPowerVia
verifyTieCell
verifyWellAntenna
verifyWellTap
verifyWireGap
verify_antenna
verify_drc
verify_stacked_die
viewBumpConnection
viewLast
viewLog
viewNext
viewSnapshot
view_dynamic_movie
view_dynamic_waveform
view_package_results
violationBrowser
violationBrowserDeleteByArea
violationBrowserReport
win
windowDeselect
windowSelect

windowToggleSelect
wireload
writeAnnotatedTransition
writeBumpLocation
writeDesignTiming
writeDieAbstract
writeFPlanScript
writeFlipChipProperty
writeFlowTemplate
writeHif
writeIntegRouteConstraint
writeLefAbstractCustomerHeader
writeMicroBumpMappingFile
writeSdpFile
writeSetLoad
writeTimingCon
writeVSMappingFile
write_category_summary
write_codesign_die_abstract
write_design_stack_config
write_do_lec
write_extraction_spec
write_generalized_feedthru_paths
write_global_slack_report
write_global_slack_worst_trigger_path_on_clocks
write_ilm_eco_db
write_instance_obs
write_ldb
write_lec_dft_constraints
write_lec_directory_naming_style
write_lec_files
write_lef_abstract
write_lef_library
write_macro_place_constraint
write_ml_design

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write_ml_library
write_ml_timing_graph
write_ml_timing_path
write_model_timing
write_module_model_context
write_name_mapping
write_net_groups_topo
write_oa_techfile
write_path_descriptions
write_path_list_summary
write_physical_context_data
write_power_constraints
write_power_intent
write_sdf
write_spd
write_tcf
write_text_timing_report
write_timing_windows
zoomBox
zoomIn
zoomOut
zoomSelected
zoomTo
```