```
#-----------------------------
# dc/pt/icc2 cmd list
#-----------------------------
acs_check_directories
acs_compile_design
acs_create_directories
acs_customize_directory_structure
acs_get_parent_partition
acs_get_path
acs_merge_design
acs_read_hdl
acs_recompile_design
acs_refine_design
acs_remove_dont_touch
acs_report_attribute
acs_report_directories
acs_report_user_messages
acs_reset_directory_structure
acs_set_attribute
acs_submit
acs_submit_large
acs_write_html
add_array_to_macro_group
add_attachment
add_buffer
add_buffer_on_route
add_command_hook
add_eco_repeater
add_feedthrough_buffers
add_group_repeaters
add_ldb_views
add_macro_to_group
add_module
add_parameter
add_pg_pin_to_db
```

```
add_pg_pin_to_lib
add_pins_to_virtual_connection
add_port_protection_diodes
add_port_state
add_power_state
add_pst_state
add_redundant_vias
add_shield_association
add_spare_cells
add_state_transition
add_supply_state
add_tie_cells
add_to_bound
add_to_bundle
add_to_collection
add_to_edit_group
add_to_group
add_to_io_guide
add_to_io_ring
add_to_matching_type
add_to_multisource_clock_sink_group
add_to_must_join_ports
add_to_net
add_to_net_bus
add_to_pin_blockage
add_to_pin_guide
add_to_placement_attraction
add_to_port_bus
add_to_routing_corridor
add_to_rp_group
add_to_scan_chain
add_via_mapping
after
alias
alib_analyze_libs
```

align_objects
align_pins
all_active_scenarios
all_clock_gates
all_clocks
all_cluster_cells
all_clusters
all_connected
all_corners
all_critical_cells
all_critical_pins
all_designs
all_dont_touch
all_drc_violated_nets
all_exceptions
all_fanin
all_fanout
all_high_fanout
all_high_transitive_fanout
all_ideal_nets
all_inputs
all_instances
all_isolation_cells
all_level_shifters
all_macro_cells
all_modes
all_outputs
all_registers
all_scenarios
all_test_modes
all_threestate
all_tieoff_cells
all_transitive_fanin
all_transitive_fanout
all_upf_repeater_cells

analyze
analyze_datapath
analyze_datapath_extraction
analyze_design_violations
analyze_dw_power
analyze_lib_cell_placement
analyze_library
analyze_minpwr_library
analyze_mv_design
analyze_power_plan
analyze_rail
analyze_rtl_congestion
analyze_subcircuit
analyze_timing_correlation
analyze_via_ladder
annotate_trace
append
append_to_collection
apply
apply_clock_gate_latency
apply_power_model
apropos
array
as_collection
assign_3d_interchip_nets
assign_feedthrough_supply
assign_tsv
associate_checkpoint_action
associate_checkpoint_report
associate_mv_cells
associate_performance_via_ladder
associate_supply_set
attach_drc_error_data
audit_scripts
balance_buffer

balance_clock_groups
balance_registers
binary
break
calc_lib_pin_cap
capture_app_var
capture_detailed_script_runtime
case
catch
cd
cell_of
chan
change_abstract
change_link
change_names
change_reference
change_selection
change_view
characterize
characterize_block_pg
characterize_context
characterize_topology_plans
check_3d_design
check_activity
check_bindings
check_block_abstraction
check_boundary_cells
check_bsd
check_budget
check_bufferability
check_bump_spacing
check_busplan_constraints
check_clock_gate_library_cell_availability
check_clock_trees
check_consistency_settings

check_constraints
check_design
check_design_for_clock_trunk_planning
check_design_states
check_duplicates
check_eco
check_equivalent_power_domains
check_error
check_feedthroughs
check_finfet_grid
check_floorplan_rules
check_freeze_silicon
check_hier_design
check_host_options
check_implementations
check_io_placement
check_legality
check_legalizer_sanity
check_level_shifters
check_library
check_license
check_lvs
check_mib_alignment
check_mib_for_pin_placement
check_multibit_library
check_mv_design
check_netlist
check_noise
check_objects_for_push_down
check_pg_connectivity
check_pg_drc
check_pg_missing_vias
check_physical_constraints
check_pin_placement
check_placement_constraints

check_power
check_pre_pin_placement
check_pre_place_io
check_pt_qor
check_routability
check_routes
check_routing_corridors
check_rp_constraints
check_sadp_tracks
check_safety_intent
check_scan_chain
check_scan_def
check_secondary_pg_placement_constraints
check_shapes
check_starrc_in_design
check_supply_equivalence
check_synlib
check_target_library_subset
check_targeted_boundary_cells
check_tcd_cells
check_timing
check_topology_plans
check_upf
check_vclp_design
clean_buffer_tree
clock_opt
clone_macro_group_packing
close
close_blocks
close_drc_error_data
close_ems_databases
close_lib
close_mw_lib
close_rail_result
collection_to_list

color_macro_pins
commit_blackbox_timing
commit_block
commit_secondary_pg_placement_constraints
commit_upf
compare_app_options
compare_checksum
compare_collections
compare_delay_calculation
compare_floorplans
compare_interface_timing
compare_lib
compare_qor_data
compare_supplies
compile
compile_boundary_cells
compile_mcl
compile_partitions
compile_pg
compile_prefer_runtime
compile_targeted_boundary_cells
compile_ultra
complete_net_parasitics
compute_area
compute_budget_constraints
compute_clock_latency
compute_dff_connections
compute_infeasible_path_overrides
compute_polygons
compute_topology_node_origins
concat
connect_freeze_silicon_tie_cells
connect_logic_net
connect_net
connect_pg_net

connect_pg_via_ladders
connect_pin
connect_pins
connect_power_switch
connect_rsfq_clock
connect_supply_net
connect_topology_nodes
continue
convert_aocv_pocv
convert_db
convert_from_polygon
convert_pg
convert_shape_patterns_to_shapes
convert_shapes_to_shape_pattern
convert_spef_to_gpd
convert_to_polygon
convert_via_matrixes_to_vias
convert_vias_to_via_matrix
copy_block
copy_busplan
copy_collection
copy_design
copy_floorplan
copy_lib
copy_module
copy_mw_lib
copy_objects
copy_relative_placement
copy_to_layer
coroutine
cputime
create_3d_mirror_bumps
create_3d_top_design
create_3d_virtual_blocks
create_abstract

create_abut_rules
create_auto_path_groups
create_backend_tcd_cells
create_blackbox
create_blackbox_clock_network_delay
create_blackbox_constraint
create_blackbox_delay
create_blackbox_drive_type
create_blackbox_generated_clock
create_blackbox_load_type
create_block
create_block_abstraction
create_bond_pad_array
create_bound
create_bound_shape
create_boundary_cells
create_bsd_patterns
create_budget_busplan
create_buffer_trees
create_bump_array
create_bump_block
create_bump_cluster
create_bump_pattern
create_bundle
create_bundles_from_patterns
create_bus
create_bus_routing_style
create_busplans
create_cache
create_cell
create_cell_array
create_cell_array_pattern
create_cell_bus
create_channel_congestion_map
create_check_design_strategy

create_checkpoint_action
create_checkpoint_report
create_clips
create_clock
create_clock_balance_group
create_clock_buffer
create_clock_drivers
create_clock_rp_groups
create_clock_skew_group
create_clock_straps
create_cluster
create_command_group
create_context_for_sub_block
create_corner
create_custom_shields
create_cut_metals
create_default_topology_plans
create_dense_tap_cells
create_density_rule
create_design
create_design_rule
create_dff_trace_filters
create_dft_netlist
create_die
create_die_block
create_differential_group
create_diodes
create_drc_error
create_drc_error_data
create_drc_error_shapes
create_drc_error_type
create_eco_bus_buffer_pattern
create_edit_group
create_ems_database
create_ems_message

create_ems_rule
create_exterior_tap_walls
create_fill_cell
create_frame
create_freeze_silicon_leq_change_list
create_frontend_tcd_cells
create_generated_clock
create_geo_mask
create_grid
create_group
create_group_repeaters_guidance
create_hdl2upf_vct
create_icovl_cells
create_ilm
create_interior_tap_walls
create_interposer_routeplan
create_io_break_cells
create_io_corner_cell
create_io_filler_cells
create_io_guide
create_io_ring
create_keepout_margin
create_layer
create_left_right_filler_cells
create_length_limit
create_lib
create_logic_net
create_logic_port
create_macro_array
create_macro_groups
create_macro_relative_location_placement
create_marker_layers
create_mask_constraint_routing_blockages
create_matching_type
create_mim_capacitor_array

create_mismatch_config
create_mode
create_module
create_multibit
create_multisource_clock_sink_group
create_mv_cells
create_mw_lib
create_net
create_net_bus
create_net_priority
create_net_shielding
create_operating_conditions
create_pad_rings
create_pass_directories
create_path_tag_set
create_pg_composite_pattern
create_pg_macro_conn_pattern
create_pg_mesh_pattern
create_pg_ml_data
create_pg_pattern_shapes
create_pg_region
create_pg_ring_pattern
create_pg_special_pattern
create_pg_stapling_vias
create_pg_std_cell_conn_pattern
create_pg_strap
create_pg_vias
create_pg_wire_pattern
create_pin
create_pin_blockage
create_pin_bus
create_pin_constraint
create_pin_guide
create_placement
create_placement_attraction

create_placement_blockage
create_poly_rect
create_port
create_port_bus
create_power_domain
create_power_group
create_power_rail_mapping
create_power_state_group
create_power_switch
create_power_switch_array
create_power_switch_ring
create_pr_rule
create_pst
create_purpose
create_qor_snapshot
create_qtm_clock
create_qtm_constraint_arc
create_qtm_delay_arc
create_qtm_drive_type
create_qtm_generated_clock
create_qtm_insertion_delay
create_qtm_load_type
create_qtm_model
create_qtm_path_type
create_qtm_port
create_rdl_power_extension
create_rdl_routing_guides
create_rdl_shields
create_repeater_groups
create_repelling_group_bound_shapes
create_routing_blockage
create_routing_corridor
create_routing_corridor_shape
create_routing_guide
create_routing_rule

create_rp_group
create_sadp_track_rule
create_safety_core_group
create_safety_core_rule
create_safety_register_group
create_safety_register_rule
create_scan_chain
create_scenario
create_secondary_pg_placement_constraints
create_shape
create_shape_pattern
create_shaping_blockage
create_shaping_channel
create_shaping_constraint
create_shields
create_si_context
create_site_array
create_site_def
create_site_row
create_starrc_files
create_stdcell_fillers
create_stub_chain
create_supernet
create_supply_net
create_supply_port
create_supply_set
create_tap_cells
create_tap_meshes
create_taps
create_targeted_boundary_cells
create_tech
create_terminal
create_terminals_for_pins
create_test_protocol
create_topological_constraint

create_topology_edge
create_topology_node
create_topology_plan
create_topology_repeater
create_track
create_trunk
create_trunk_pin_to_pin
create_trunk_pin_to_trunk
create_trunk_shared_track
create_trunk_topology
create_trunk_via_ladder
create_tsv_array
create_undo_marker
create_upf2hdl_vct
create_utilization_configuration
create_via
create_via_def
create_via_ladder
create_via_matrix
create_via_region
create_via_rule
create_virtual_connection
create_voltage_area
create_voltage_area_rule
create_voltage_area_shape
create_vtcell_fillers
create_wire_load
create_wire_matching
cross_probing_filter
current_block
current_corner
current_design
current_design_name
current_dft_partition
current_instance

current_lib
current_mode
current_mw_lib
current_power_rail
current_scenario
current_test_mode
current_topology_plan
cut_rows
date
dbatt
dbatt_dc
dc_allocate_budgets
decompose_shape_patterns
decompose_via_matrixes
decrypt_lib
define_antenna_accumulation_mode
define_antenna_area_rule
define_antenna_layer_ratio_scale
define_antenna_layer_rule
define_antenna_rule
define_cell_alternative_lib_mapping
define_design_lib
define_design_mode_group
define_dft_design
define_dft_partition
define_name_maps
define_name_rules
define_power_model
define_proc_attributes
define_process
define_qtm_attribute
define_scaling_lib_group
define_test_mode
define_user_attribute
delete_operating_conditions

derive_3d_interface
derive_cell_snap_data
derive_clock_balance_constraints
derive_clock_balance_points
derive_clock_cell_references
derive_clocks
derive_constraints
derive_hier_antenna_property
derive_macro_relative_location
derive_mask_constraint
derive_metal_cut_routing_guides
derive_perimeter_constraint_objects
derive_pg_mask_constraint
derive_pin_access_routing_guides
derive_placement_blockages
derive_preferred_macro_locations
derive_route_connection
derive_secondary_pg_placement_constraints
describe_state_transition
dft_drc
dict
disconnect_3d_bumps
disconnect_net
distribute_objects
drive_of
duplicate_logic
echo
eco_change_legal_reference
eco_netlist
eco_opt
eco_update_supply_net
edit_block
edit_ems_rule
edit_module
edit_via_matrix

elaborate
enable_primetime_icc_consistency_settings
enable_runtime_improvements
enable_via_ladder_insertion
enable_write_lib_mode
encoding
encrypt_lib
eof
error
error_info
estimate_clock_network_power
estimate_cts_drc
estimate_delay
estimate_eco
estimate_resistance
estimate_timing
estimate_topology_timing
eval
eval_checkpoint
eval_pg_ml_model
eval_with_undo
exec
exec_gds2rh
exit
expand_objects
expand_outline
explore_logic_hierarchy
export_advanced_technology_rules
expr
extend_mw_layers
extract_model
extract_svf
fblocked
fconfigure
fcopy

file
fileevent
filter
filter_collection
find
find_objects
fix_eco_drc
fix_eco_leakage
fix_eco_power
fix_eco_timing
fix_floorplan_rules
fix_mv_design
fix_pg_missing_vias
fix_placement_color_mask
fix_signal_em
fix_via_ladder_constraints
flip_objects
flush
for
foreach
foreach_in_collection
format
generate_hot_spots
generate_mv_constraints
generate_mv_feedback
generate_net_pattern
generate_pg_script
generate_rm
generate_sadp_tracks
generate_via_ladder_template
generate_via_rules_for_performance
get_abstract_type
get_alternative_lib_cell
get_alternative_lib_cells
get_always_on_logic

get_antenna_rule_names
get_app_option_value
get_app_options
get_app_var
get_attribute
get_blackbox_generated_clocks
get_block_objects
get_blocks
get_bound_shapes
get_bounds
get_budgets
get_buffers
get_bump_cluster_name
get_bump_cluster_objects
get_bundles
get_busplans
get_cell
get_cell_array_patterns
get_cell_buses
get_cells
get_cells_of_scan_chain
get_checkpoint_data
get_clock_balance_groups
get_clock_gate_pins
get_clock_gates
get_clock_group_groups
get_clock_groups
get_clock_network_objects
get_clock_relationship
get_clock_skew_groups
get_clock_toggle_rate
get_clock_tree_pins
get_clocks
get_clusters
get_command_hooks

get_command_option_values
get_connected_routing
get_constraint_groups
get_core_area
get_corners
get_coupling_capacitors
get_cputime
get_cross_probing_info
get_current_checkpoint
get_current_ems_database
get_current_hook_command
get_current_mismatch_config
get_current_power_domain
get_current_power_net
get_date
get_defined_attributes
get_defined_commands
get_density_rules
get_design
get_design_checks
get_design_lib_path
get_design_rules
get_designs
get_dff_connections
get_dft_hierarchical_pins
get_domain_elements
get_dont_touch_cells
get_dont_touch_nets
get_drc_error_data
get_drc_error_types
get_drc_errors
get_dvfs_scenarios
get_early_data_check_records
get_eco_bus_buffer_patterns
get_edit_groups

get_edit_setting
get_editability
get_edrc_setting
get_em_max_capacitance
get_em_max_toggle_rate
get_ems_databases
get_ems_rules
get_equivalent_power_domains
get_essential_points
get_estimated_wirelength
get_exception_groups
get_exceptions
get_fill_cells
get_flat_cells
get_flat_nets
get_flat_pins
get_generated_clock
get_generated_clocks
get_geometry_result
get_gpd_corners
get_gpd_layers
get_grids
get_ground_capacitors
get_groups
get_ilm_objects
get_input_delays
get_instance_result
get_io_guides
get_io_rings
get_keepout_margins
get_label_switch_list
get_latch_loop_groups
get_layers
get_lib
get_lib_attribute

get_lib_cell
get_lib_cells
get_lib_pin
get_lib_pins
get_lib_timing_arcs
get_libs
get_license
get_licenses
get_macro_group_packing_clone_candidates
get_matching_types
get_mem
get_message_ids
get_message_info
get_message_instances
get_mib_objects
get_mismatch_objects
get_mismatch_types
get_modes
get_modules
get_msg
get_multibits
get_multisource_clock_sink_groups
get_net
get_net_buses
get_net_estimation_rules
get_nets
get_noise_violation_sources
get_object_by_id
get_object_name
get_object_occurrences
get_objects_by_location
get_output_delays
get_overlap_blockages
get_parasitic_techs
get_path_count_for_tag

get_path_group
get_path_groups
get_pg_pins
get_pg_regions
get_pin
get_pin_blockages
get_pin_buses
get_pin_constraints
get_pin_guides
get_pins
get_placement_attractions
get_placement_blockages
get_placement_ir_drop_target
get_polygon_area
get_port
get_port_antenna_property
get_port_buses
get_ports
get_power_budget
get_power_clock_scaling
get_power_derate
get_power_domains
get_power_group
get_power_group_objects
get_power_per_pgpin
get_power_per_rail
get_power_strategies
get_power_switch_patterns
get_power_switches
get_pr_rules
get_purposes
get_qtm_ports
get_random_numbers
get_references
get_related_supply_net

get_related_supply_nets
get_repeater_group_info
get_repeater_paths_info
get_resistors
get_routes_between_objects
get_routing_blockages
get_routing_corridor_shapes
get_routing_corridors
get_routing_guides
get_routing_rules
get_rp_blockages
get_rp_group_objects
get_rp_groups
get_safety_core_groups
get_safety_core_rules
get_safety_register_groups
get_safety_register_rules
get_scan_cell_names
get_scan_cells_of_chain
get_scan_chain_collection
get_scan_chain_count
get_scan_chain_names
get_scan_chain_of_cell
get_scan_chains
get_scan_chains_by_name
get_scenarios
get_selection
get_shape_patterns
get_shapes
get_shaping_blockages
get_shaping_channels
get_shaping_constraints
get_shift_register_chains
get_si_bottleneck_nets
get_site_arrays

get_site_defs
get_site_rows
get_snap_setting
get_statements
get_stub_chains
get_supernets
get_supply_groups
get_supply_net_probability
get_supply_nets
get_supply_ports
get_supply_sets
get_svf
get_switching_activity
get_taps
get_techs
get_terminals
get_timing_arcs
get_timing_paths
get_topological_constraints
get_topology_edges
get_topology_nodes
get_topology_plans
get_topology_repeaters
get_trace_option
get_tracks
get_undo_info
get_unix_variable
get_user_units
get_utilization_configurations
get_via_defs
get_via_ladders
get_via_matrixes
get_via_regions
get_via_rules
get_vias

get_view_switch_list
get_virtual_connections
get_voltage_area_rules
get_voltage_area_shapes
get_voltage_areas
get_vsdc
get_working_design_stack
get_zero_interconnect_delay_mode
getenv
gets
glob
global
group
group_cells
group_path
group_variable
gui_add_missing_vias
gui_append_utable
gui_bin
gui_change_highlight
gui_change_layer
gui_change_via_def
gui_change_via_size
gui_check_drc_errors
gui_close_utable
gui_create_attrgroup
gui_create_pref_category
gui_create_pref_key
gui_create_task
gui_create_task_item
gui_create_task_page
gui_create_tk_palette_type
gui_create_utable
gui_create_vm
gui_create_vm_objects

gui_create_vmbucket
gui_delete_attrgroup
gui_edit_vmbucket_contents
gui_eval_command
gui_execute_menu_item
gui_exist_pref_category
gui_exist_pref_key
gui_explore_logic_hierarchy
gui_export_utable
gui_fill_utable
gui_get_bucket_option
gui_get_bucket_option_list
gui_get_current_task
gui_get_display_view
gui_get_hierview_data
gui_get_highlight
gui_get_highlight_options
gui_get_layer_widths
gui_get_map
gui_get_map_list
gui_get_map_option
gui_get_map_option_list
gui_get_mapbucket
gui_get_pref_keys
gui_get_pref_value
gui_get_presets
gui_get_setting
gui_get_task_list
gui_get_task_page
gui_get_utable
gui_get_vm
gui_get_vmbucket
gui_get_window_ids
gui_get_window_pref_categories
gui_get_window_pref_keys

gui_get_window_pref_value
gui_get_window_presets
gui_get_window_types
gui_highlight_nets_of_selected
gui_import_utable
gui_list_attrgroups
gui_load_cell_density_mm
gui_load_clock_trunk_planning
gui_load_path_analyzer_flylines
gui_load_pin_density_mm
gui_load_power_density_mm
gui_merge_utable
gui_open_utable
gui_read_timing_paths
gui_remove_pref_key
gui_remove_vm
gui_remove_vmbucket
gui_report_task
gui_select_bounds_of_selected
gui_select_bundles_of_selected
gui_select_by_name
gui_select_cells_of_selected
gui_select_connected_net_shapes
gui_select_connected_rdl_net_shapes
gui_select_connections_of_selected
gui_select_constraint_groups_of_selected
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report_si_bottleneck
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report_si_double_switching
report_si_noise_analysis
report_signal_em
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set_coupling_separation
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set_design_rule_attribute
set_design_top
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set_dft_signal
set_direct_power_rail_tie
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set_disable_tie_insert
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set_dp_smartgen_options
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set_driving_cell
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set_eco_placement_net_weight
set_eco_power_intention
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set_editability
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set_floorplan_composite_spacing_rules
set_floorplan_enclosure_rules
set_floorplan_exception_rules
set_floorplan_extension_rules
set_floorplan_forbidden_rules
set_floorplan_halo_rules
set_floorplan_length_rules
set_floorplan_location_rules
set_floorplan_reshape_rules
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set_ideal_transition
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set_individual_pin_constraints
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set_isolation_cell
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set_lc_options
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set_libcell_dimensions
set_libpin_location
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set_license_limit
set_link_library_subset
set_load
set_local_link_library
set_locked_objects
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set_logic_zero
set_logicbist_configuration
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set_macro_group_shape
set_macro_relative_location
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set_max_capacitance
set_max_delay
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set_max_fanout
set_max_leakage_power
set_max_lvth_percentage
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set_mw_technology_file
set_net_estimation_rule
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set_noise_immunity_curve
set_noise_lib_pin
set_noise_margin
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set_parasitic_parameters
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set_pg_pin_model
set_pg_strategy
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set_pg_via_master_rule
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set_pin_budget_constraints
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set_pipeline_scan_data_configuration
set_placement_ir_drop_target
set_placement_spacing_label
set_placement_spacing_rule
set_placement_status
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set_port_antenna_property
set_port_attributes
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set_preserve_clock_gate
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set_rtl_to_gate_name
set_safety_core_rule
set_safety_logic_port_map
set_safety_register_rule
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set_scan_group
set_scan_link
set_scan_path
set_scan_register_type
set_scan_replacement
set_scan_skew_group
set_scan_state
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set_shaping_options
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set_si_noise_analysis
set_si_noise_disable_statistical
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set_spacing_label_rule
set_spfm_target
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write_blackbox_timing_script
write_bsd_rtl
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write_compile_script
write_context
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write_default_pg_pattern
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write_design_lib_paths
write_dff_trace_filters
write_drc_error_data
write_early_data_check_config
write_eco_design
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write_floorplan
write_frame_options
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write_hier_data
write_icc2_files
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write_ilm_parasitics
write_ilm_script
write_ilm_sdf
write_interface_timing
write_io_constraints
write_ivm
write_layer_map
write_lef
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write_lib_specification_model
write_link_library
write_macro_relative_location
write_makefile
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write_milkyway
write_multibit_components
write_mw_lib_files
write_name_map
write_net_estimation_rules
write_oasis
write_parasitics
write_partition
write_partition_constraints
write_physical_annotations
write_physical_rules
write_pin_constraints
write_pt_checksum
write_push_down_eco
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write_qtm_model
write_rde
write_rh_file
write_rh_power_file
write_routes
write_routing_constraints
write_rp_groups
write_rtl_load
write_safety_register_script
write_saif
write_sanity_check_point
write_scan_def
write_script
write_sdc
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write_session_settings
write_shadow_eco
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write_taps
write_tech_file
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