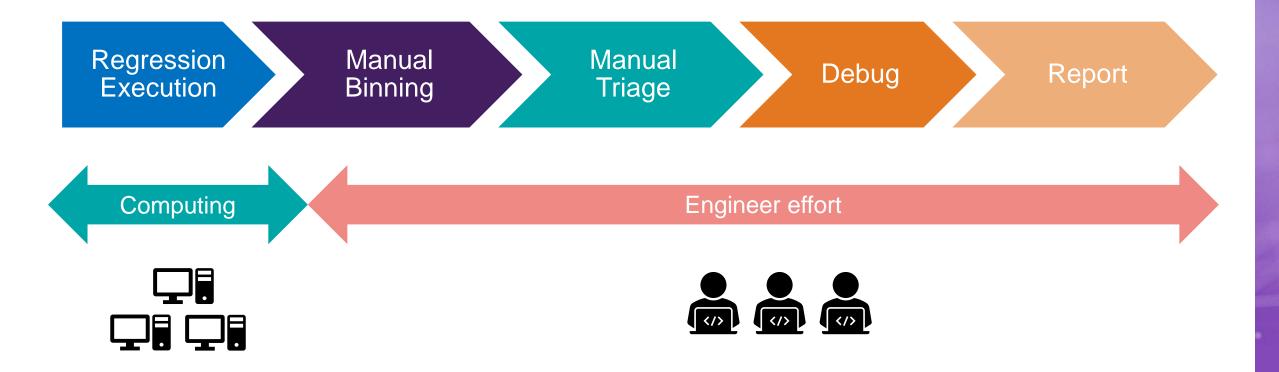


#### Verdi RDA: A flexible regression debug accelerator

ChienLin Huang, MediaTek Sherwin Lai, Stan Huang, Kai Yang, Alvin Chen, Synopsys

#### **Traditional Regression Flow**





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# Pain points 1: Analyze and Classify Issues

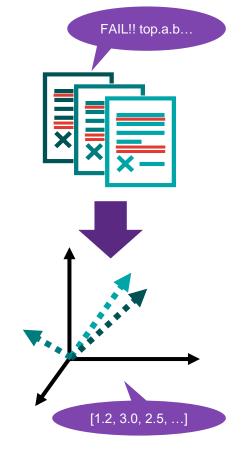
ML based auto binning feature: Error binning

- Extract all error messages in simulation logs – Customized error messages acceptable
- Calculate the error shapes of failed simulations
   Convert error messages to error shapes
- Conduct binning Into buckets
  - Group similar failures into the same bucket
  - Separate irrelevant failures into different buckets

Classify the result with the press of a single button by anyone. -> Save 4 hours 1 man per regression result -> Save 8 hours 1 man for result parser



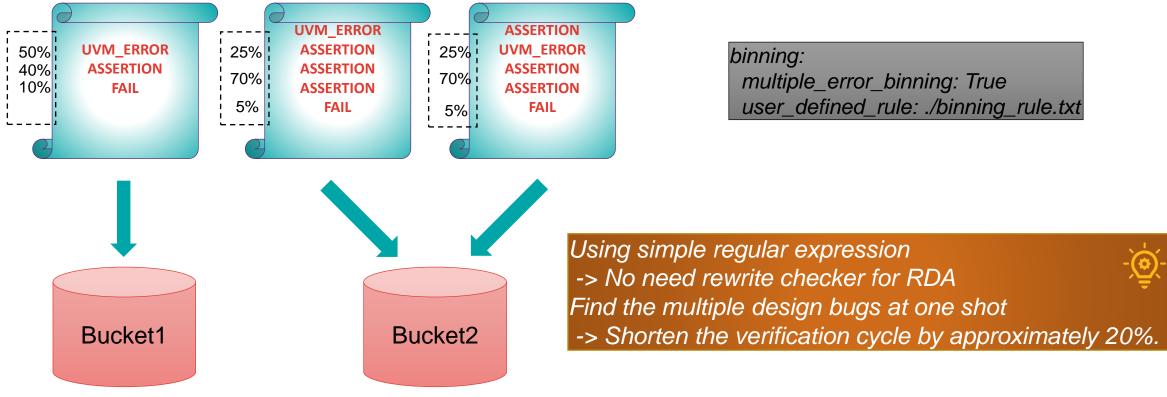




# Pain points 1: Analyze and Classify Issues

ML based auto binning feature: Multiple error binning + user defined error

- Turn on with binning.multiple\_error\_binning: True in config yaml
- Grouping by the distribution of all the error messages in each logs









Memo system in the auto binning feature: memo + bucket movement

	Bucket Movement (on odcgen-vcs-16cx240g-2640-010)	$\otimes$	
	Source Bucket: Bucket1		
<pre> <rcasmv:1> sqlite@/re</rcasmv:1></pre>	Fail Log: //remote/us01home57/shenhang/work/rda_database/change_bucket/regression_cases/case4/sim.log	1	x
<u>File View Tools Window H</u> elp		-	
🖹 🔛 🔜 🔍 🕞 🖄	Target Bucket: Bucket2	-	
	Owner: Test		
Latest 🗙	Root Cause:		
Bucket1 (5 Fail, Date: 20240229	top.a.b		- x- =
Buckett (5 rail, Date: 20240225 Image: provide the second seco			
[Memo]			
Test: [2024/03/01 00:14:41]			
- Memo for snug			
Error Message:			
100.0%: [UVM Error] C			
Remaining Cases			
Bucket2 (3 Fail, Date: 20240229	Memo:		
- /remote/us01home57/shenha			
···· (no memo)	[2024/03/01 00:14:41] - Memo for snug		
Error Message:			
33.3%: [Assertion Erro simTop.u riscv.u RISC]			
			×
33.3%: [UVM Error] cs			
Remaining Cases			
Bucket3 (3 Fail, Date: 20240229			Use the memo system instead of emai
The second se			-> more straightforward
	Cancel Ok		
			-> no more mail bomb

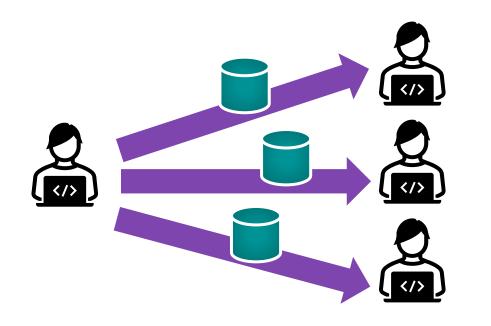
• Adjust binning results based on users' knowledge flexibly



## Pain points 2: Assign and tracking debug status

Memo system in the auto binning feature: assignment collaboration

- Collaboration with RDA instead of mailing
  - Assign buckets to the right assignee
  - Leave a memo
  - Review debugging status



ttest_ufe/autoRCA/reg	re	ssion_binning/case1	
		Р. М	enu
(S)			
	1	Working status	Action
		New (assignee: _NA_)	
ression_cases/case4/sim.lo			
			2
101 and dce_rx value is <*			
		Debugging (assignee: St)	
ression_cases/case10/sim.l			١
			2
			-

Analyze -> assign -> report in one tool -> no more issue tracking system, save lots of \$\$ -> reduce 20% effort for issue assign and tracking

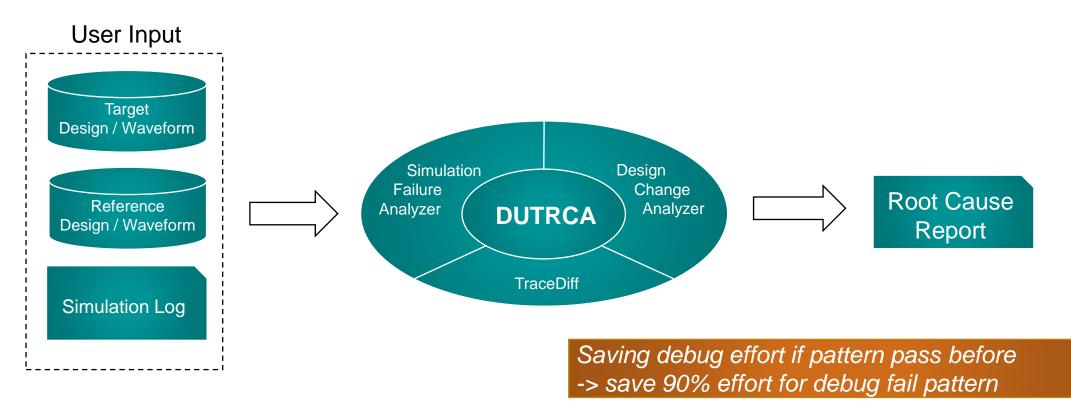


# Pain points 3: Testcase pass before

DUTRCA / TBRCA feature



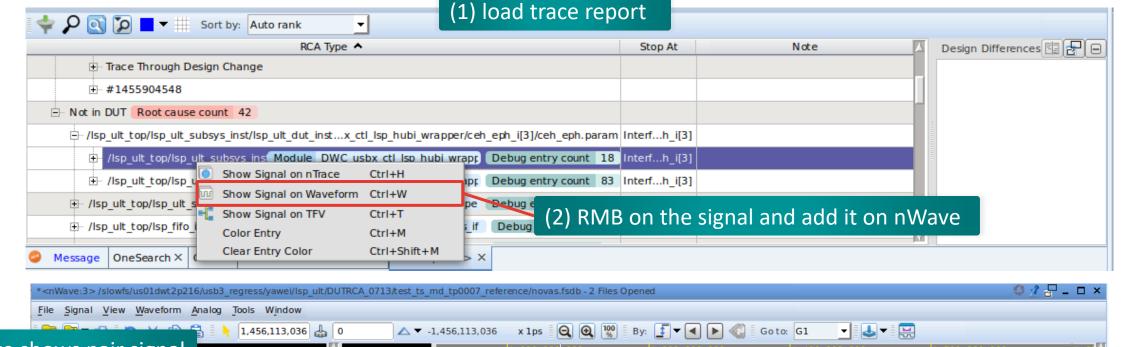
 Apply technology of "Log Analyzer", "TraceDiff" and "Design Change Detection" to find suspected fail case root cause automatically



## Pain points 3: Testcase pass before

DUTRCA / TBRCA feature: Add pair signals on Waveform

Message OneSearch × Console \*<nWave:3> novas.fsdb ×



(3) nWave shows pair signal

Image: file signal view waveform Analog Tools Window

(3) nWave shows pair signal

Image: file signal view waveform debug time

Image: file signal

Image: file signal view waveform debug time

Image: file signal

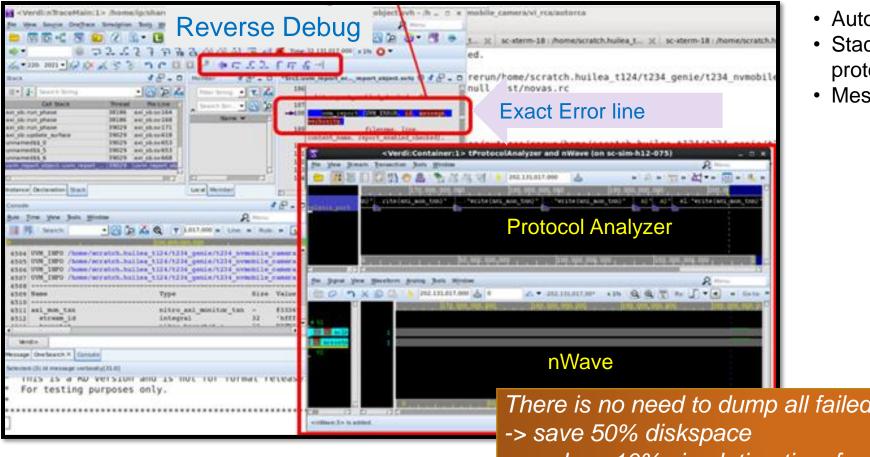
Image:

<rcaReport:4> ×



## Pain points 4: Rerun for dump waveform

Debug facilitator feature: Interactive reverse debug





- Automatically stop at the error point
- Stacked view of synchronize protocol analyzer & nWave
- Message Analyzer Report

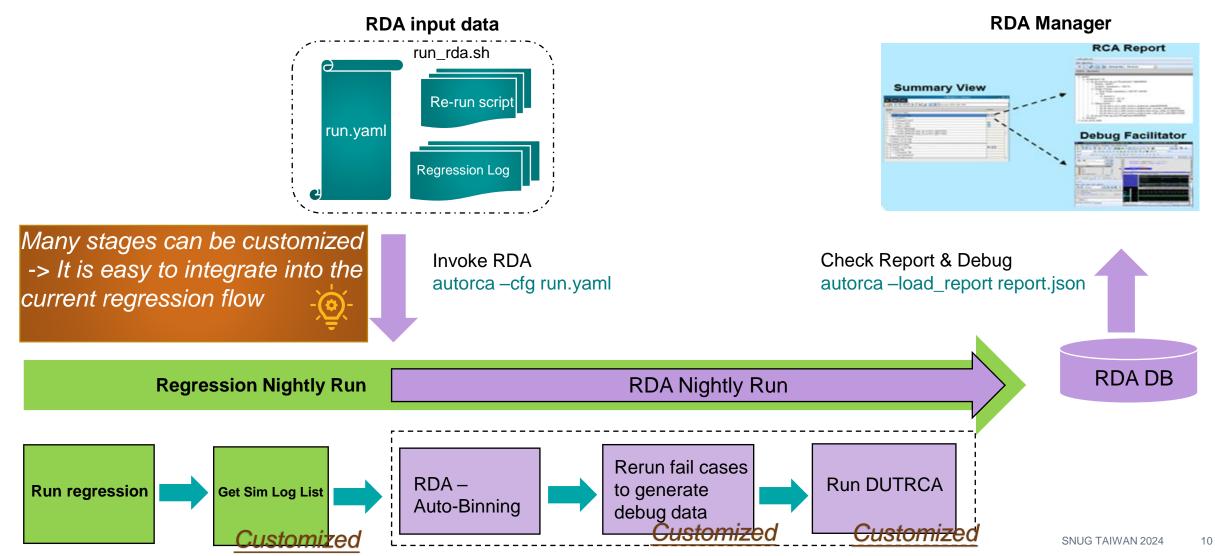
There is no need to dump all failed waveforms before debugging

-> reduce 10% simulation time for waveform dumping

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## Binning + DUTRCA + DF

= Flexible Regression Debug Automation System





#### Conclusions

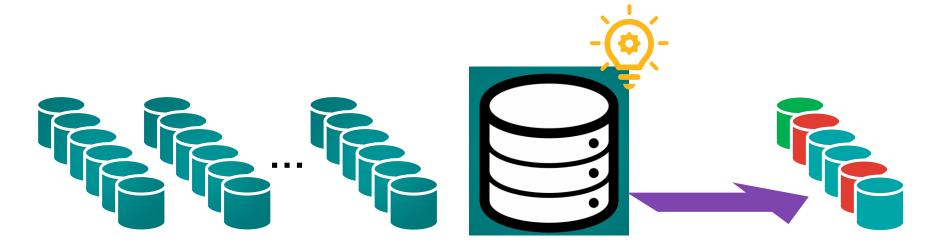


- RDA is a system that integrates log analysis, error binning, issue assignment and tracking, root cause analysis, and on-the-fly debugging within a single Verdi GUI. In our test cases, this system
  - Saved the effort of one person
  - Two in-house tools
  - Reduced designer debug effort by 50%
  - Shortened the cycle time for single regression issue debugging by 20%.
- The DUTRCA feature provides regression owners with a very powerful tool, saving 90% of the debug effort, although it is currently only applicable to fixed patterns.
- Since all tasks can be completed within the same interface, the feedback from team members has been very positive.
- The difficulty of implementation has been reduced by 50% due to the ability to customize in many places through options. Of course, some scripts will still be needed to interface with the original regression flow.

#### **Future Works**

Historical analysis with database

- Provide debugging recommendations and hints
  - Continuous failing bucket, new failing bucket...
- Detect similar bucket-fixed patterns before
  - Reduce redundant effort
- Critical debugging, effective debugging







# THANK YOU

Our Technology, Your Innovation<sup>™</sup>