Critical Path Level IR-aware STA

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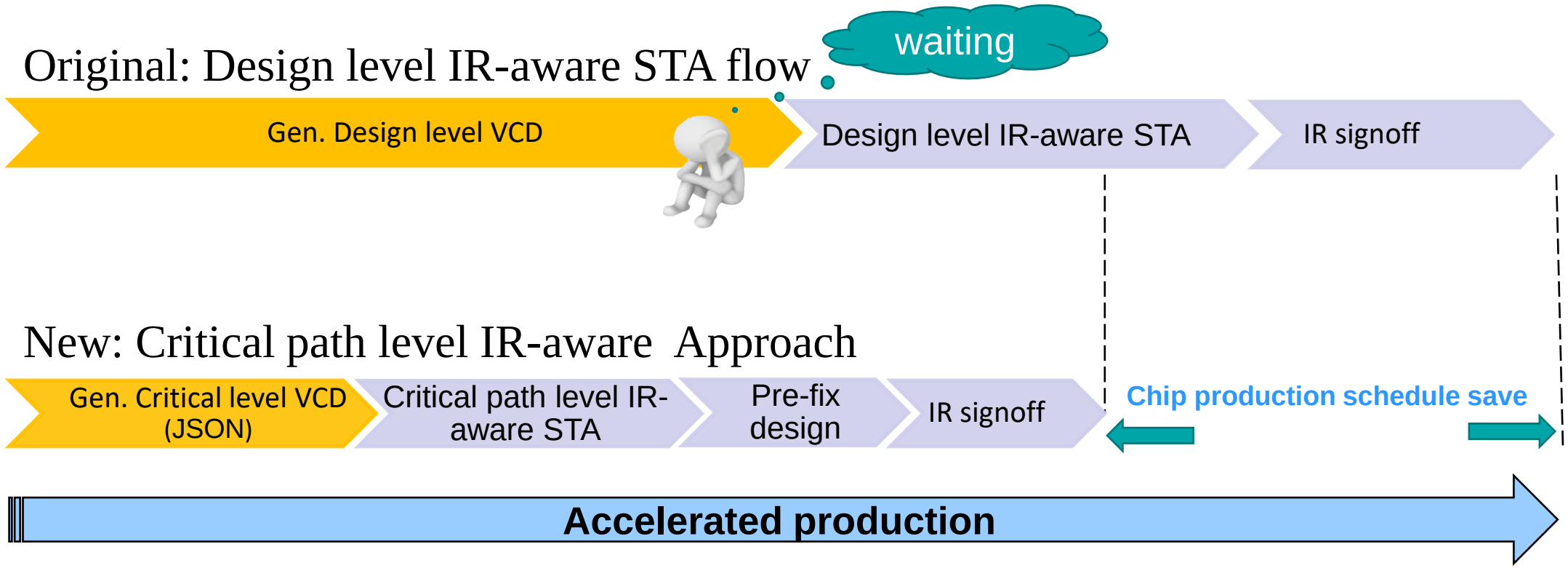
Motivation

- Design level IR-aware STA spend much time to wait postsim VCD file generation
- If analyzing critical path level IR-aware STA cover design level, it speed up IR-aware STA analysis/ECO before IR sign-off



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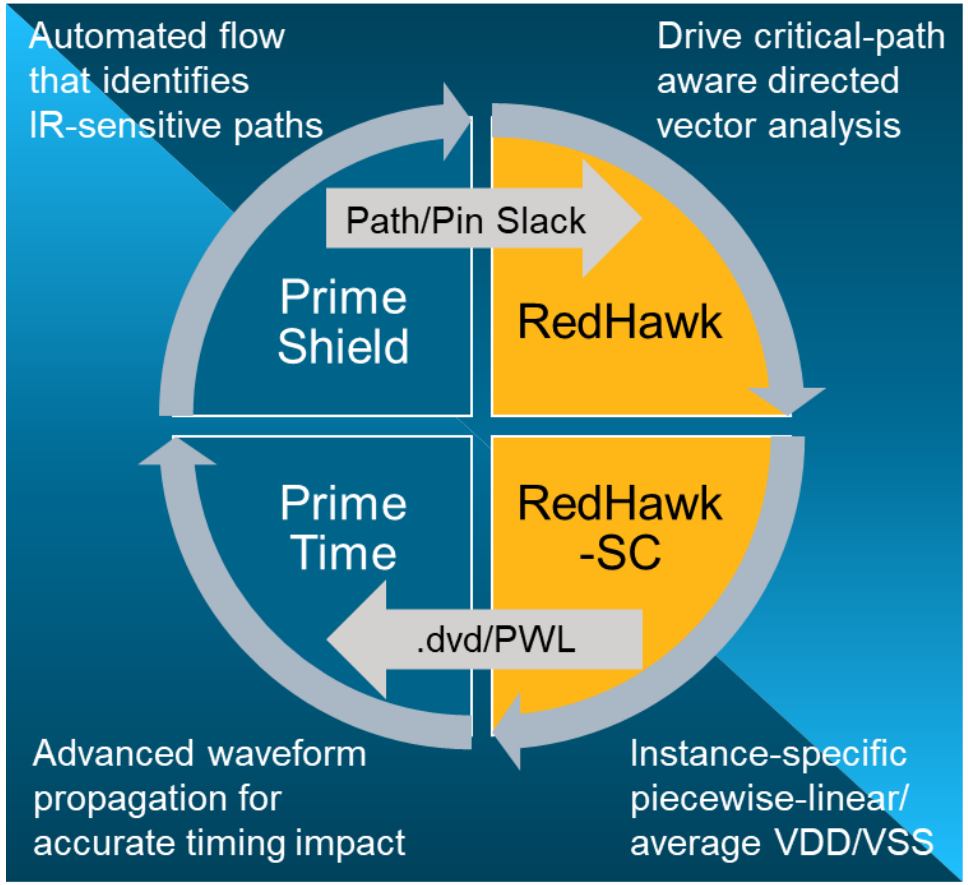
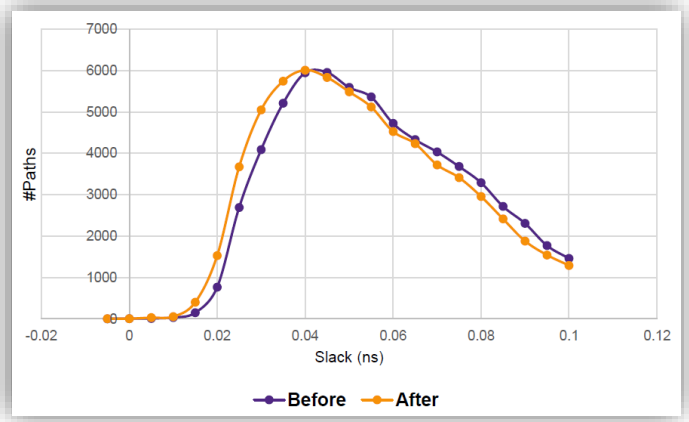
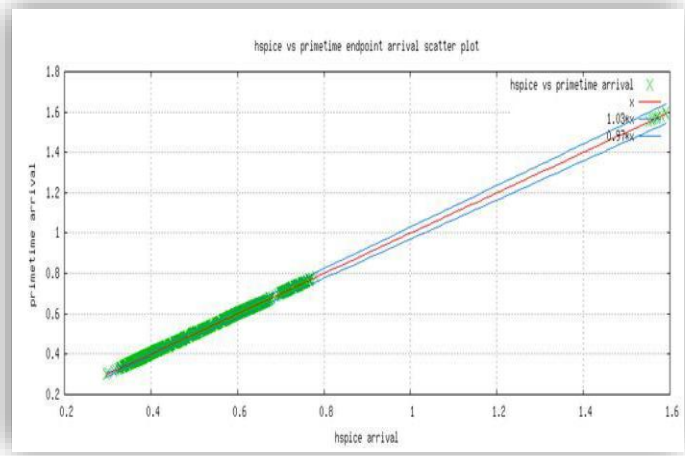
Introduction

- A high-fidelity Ansys-Synopsys voltage-timing solution
  - Prevents IR-related timing failures in silicon, and maximizes design PPA

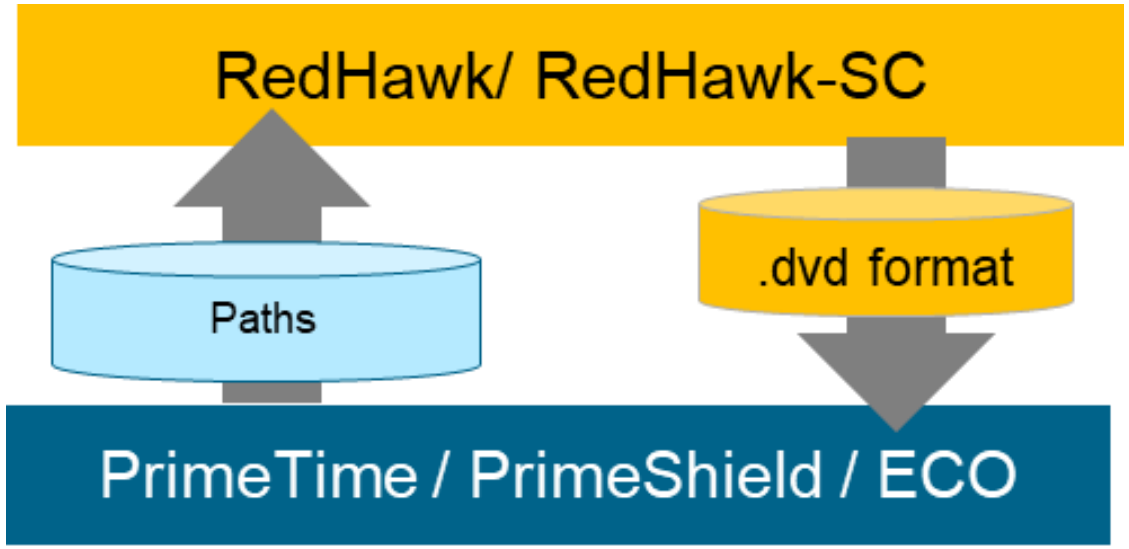


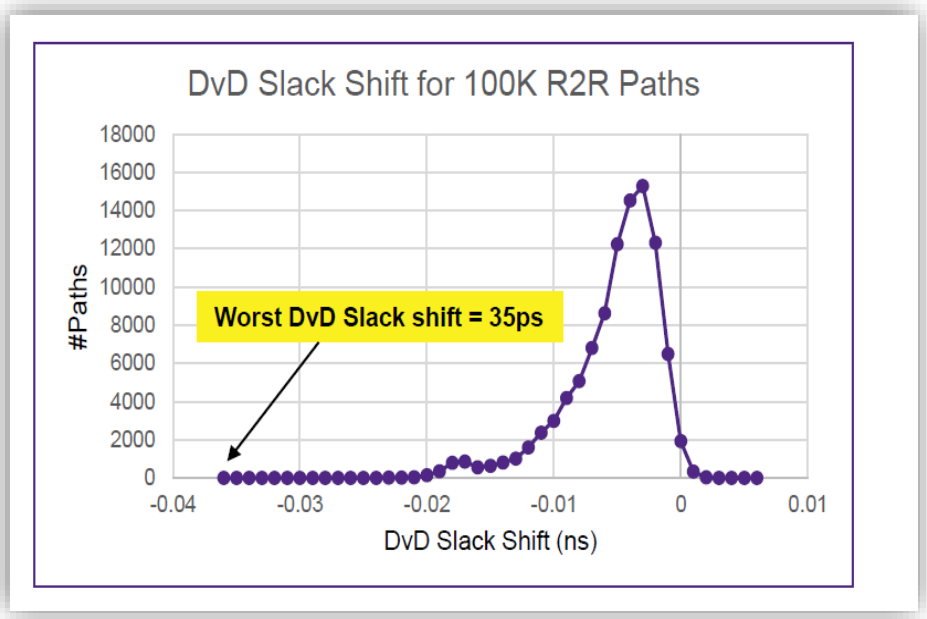




Introduction

- IR-Aware STA
  - Native dynamic voltage drop (DvD) support with instance-specific separate VDD and VSS





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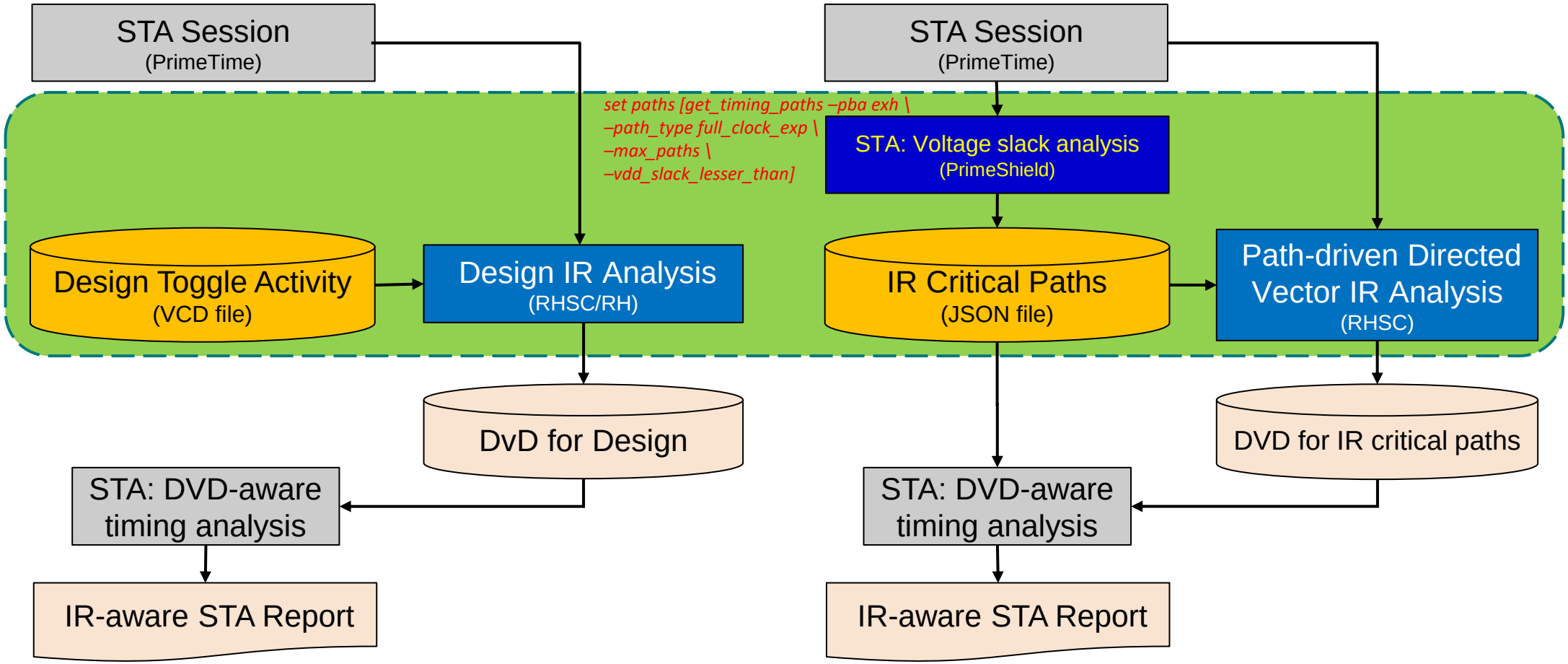
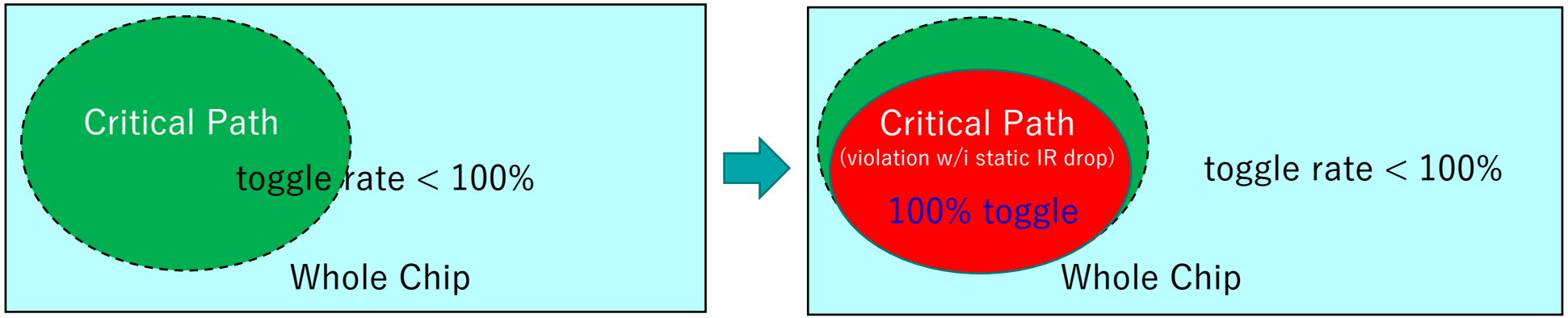
Methodology

- Design Level vs. Critical Path Level IR-aware STA

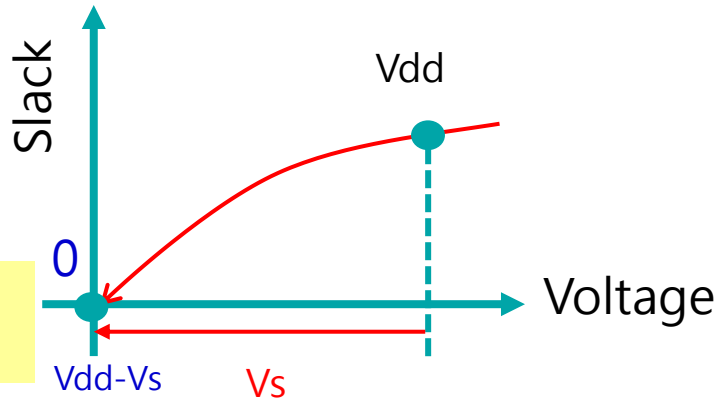


Methodology

- Critical Path Level IR Analysis
  - 100% input pattern toggle rate at critical path level IR-aware STA



  - Find violation critical paths w/ static IR drop via PrimeShield
    - Voltage Slack(Vs) is the shift voltage which make path slack<0
    - Find the critical paths which will violation w/i static IR drop
      - Target paths: Vs ≦ Vdd* static IR(%)



PrimeShield command:

%>get_timing_paths –slack_greater_than 0 –vdd_slack_lesser_than Vs

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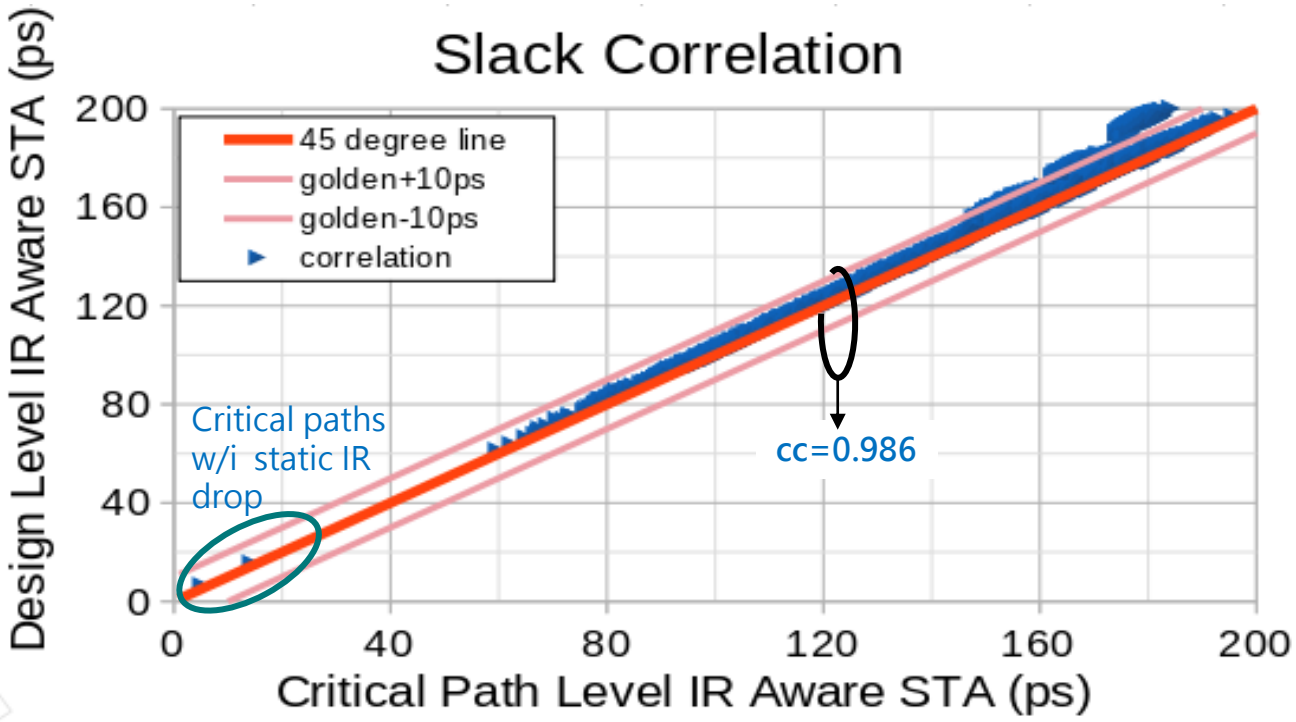
Experiment Result

- IR-aware STA Correlation
  - Explore Case:
    - T12FFC design for test chip
    - Corner: SSG/0.9V/125C for setup
    - PT/PS version: 2021.06
    - Critical paths order: 10^4
  - Critical paths w/ IR drop:

Path	Item	Design Level	Critical Path Level	Diff.
#1	Slack	6 ps	5.4 ps	-0.6 ps
	IR-drop	12.5 mV	13.6 mV	1.1 mV
#2	Slack	15 ps	14.6 ps	-0.4ps
	IR-drop	8.3 mV	12.1 mV	3.8 mV



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- Tool enhancement
  - Command “slack_lesser_than” could be ignore when set “slack_greater_than >= 0”
  - Accurate PWL IR-aware analysis

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Conclusion

- This work successfully using PrimeShield to speed up IR-aware STA analysis/ECO before IR sign-off
- “Critical path level” vs. “Design level” IR aware STA correlation
  - cc = 0.986 high correlative
  - “Critical path level” cover “Design level” IR aware STA


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