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GUC 2.5D/3D Multi-Die System Design

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GUC Advanced Package Technology (APT) Development

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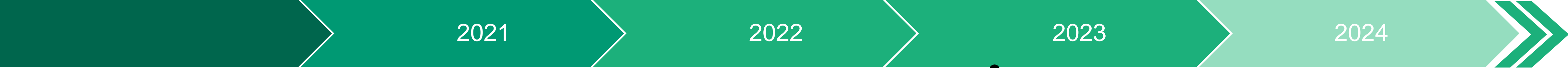
CoWoS-S Flow
- Interposer design 7.2G
- eDTC insertion
- 3D stack PV & Multi-die IR

CoWoS-R Flow
- 3D stack PV
- Multi-die IR

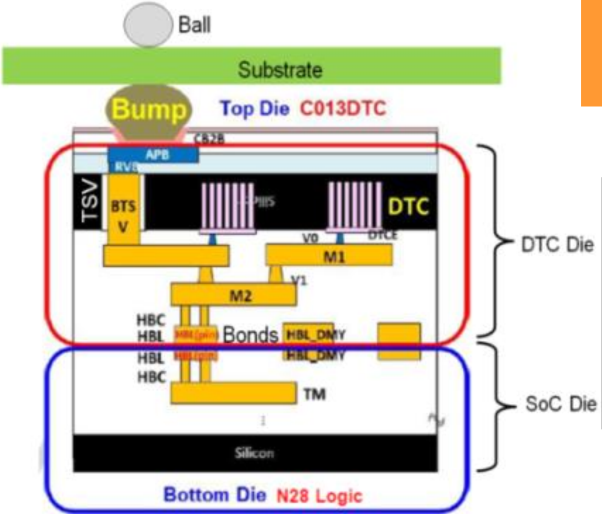
SoIC-WoW Flow
- Hybrid-bond Planning
- Cross-die STA signoff
- Multi-die IR & 3D stack PV
- Thermal analysis

CoWoS-L Flow
- Local Silicon Interconnect
- eDTC insertion
- 3D stack PV & Multi-die IR

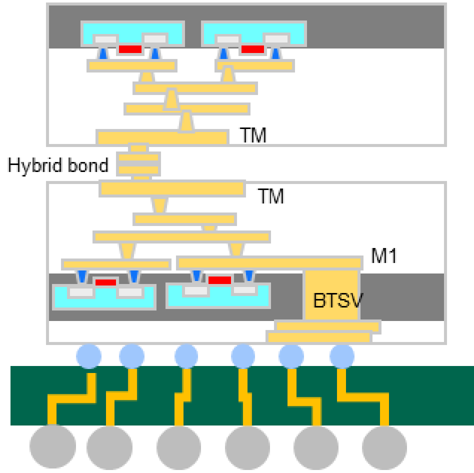


SoIC-WoW w/ DTC TPO
- TK1 pilot
- Bottom Die: N28 SoC
  Top Die: CL013 DTC

SoIC-WoW TPO
- TK1 pilot
- Bottom Die: N7 SoC
  Top Die: N7 Cache Memory



- IR drop 20% → 14.7% for multi-core ramp-up
- Improve Vmin 20mV in ACSCAN ATE test



- 3D hierarchical low power design (8 blocks + 2 tops)
- CTS plan for cross-die OCV reduction, MMMC-STA critical corner analysis
- PG TSV #/pitch plan, BTSV array macro design

3DFabric – Versatile from 2.5D to 3D Chiplets

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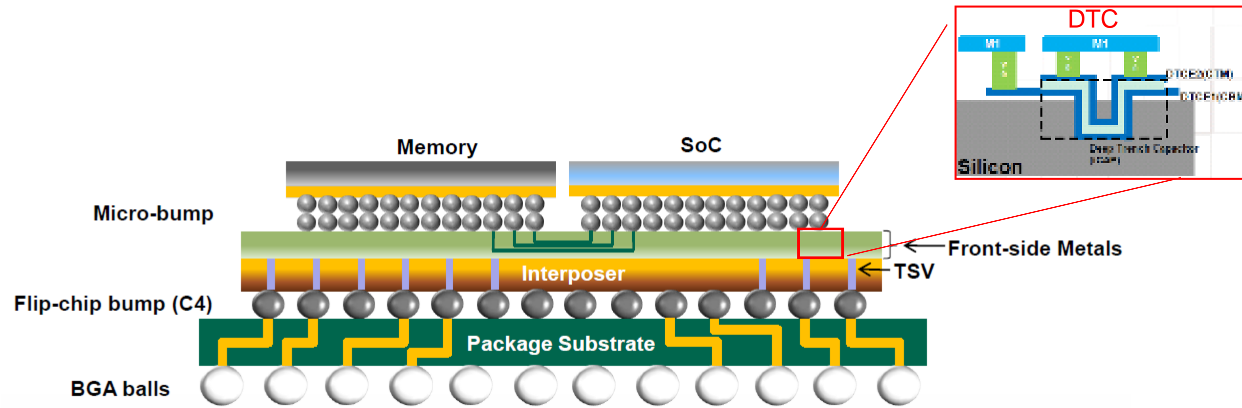

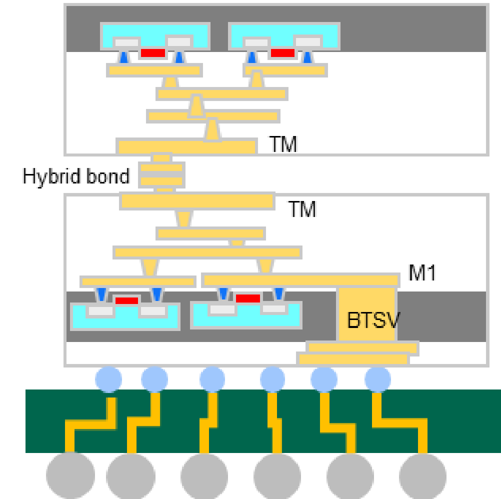

- Benefits in heterogeneous integration and flexibility.
- Use TSV to connect stacked dies vertically
  - More complex issues like stress, thermal and others
- Deep trench capacitor can provide good PI & SI performance

- Benefit with smaller chip size
- Use hybrid bonding connects dies and provides better PPA
- Use TSV through logical dies to connect to substrate. Challenges SoC PnR, thermal, and PI

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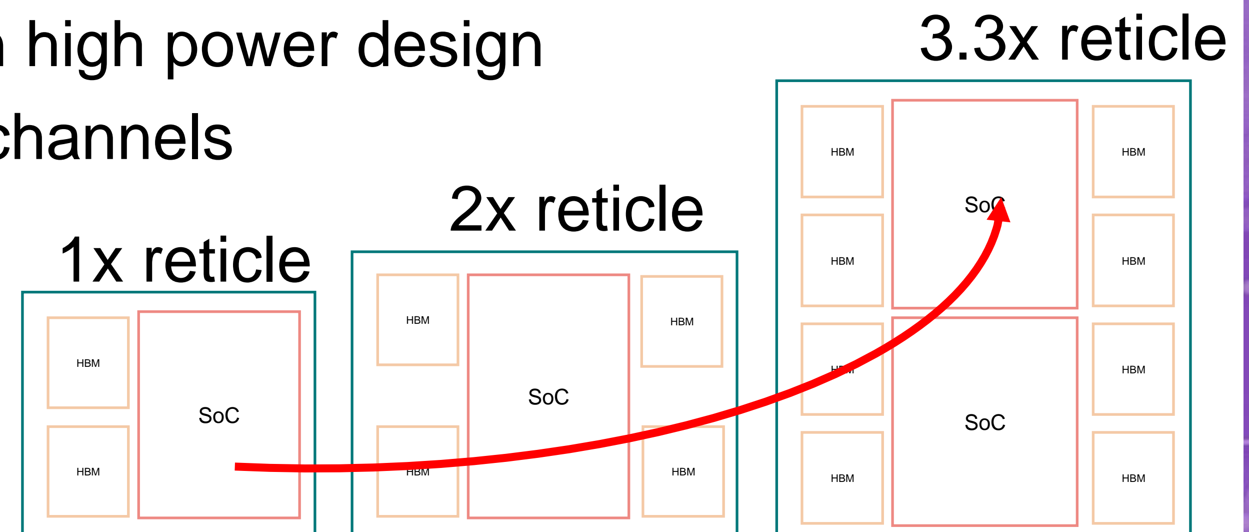
2.5D CoWoS Design

2.5D CoWoS Design Challenges

- Interposer size getting bigger and bigger
  - Important to do cross die bump assignment for better IR quality
  - Increased iterations of cross die micro bump assignment update
  - More assemble issues on the die floorplan – Implicit uncheckable rule handling
- Micro bump location needs to be frozen in early stage
  - Interposer stitching is important in SoC floorplan
- Need robust die to die routing pattern to meet the performance spec
- Interposer eDTC capacitor is needed in high power design
- SI/PI simulation takes long time for all channels
  - Need to make sure channels are balanced



CoWoS Die Planning and Prototype

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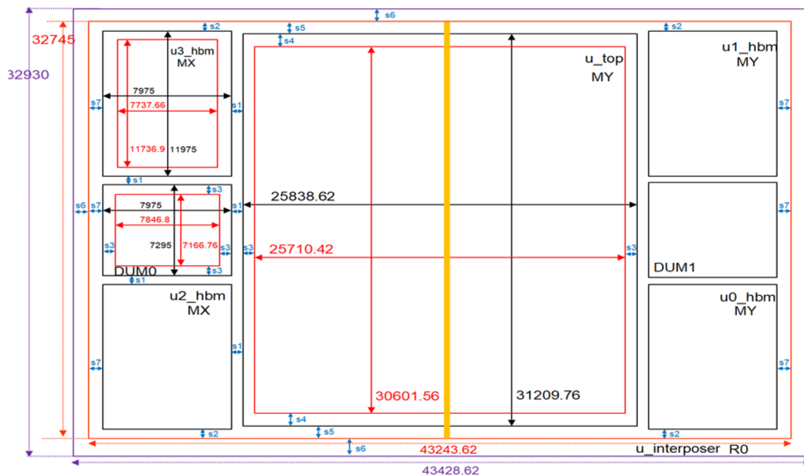
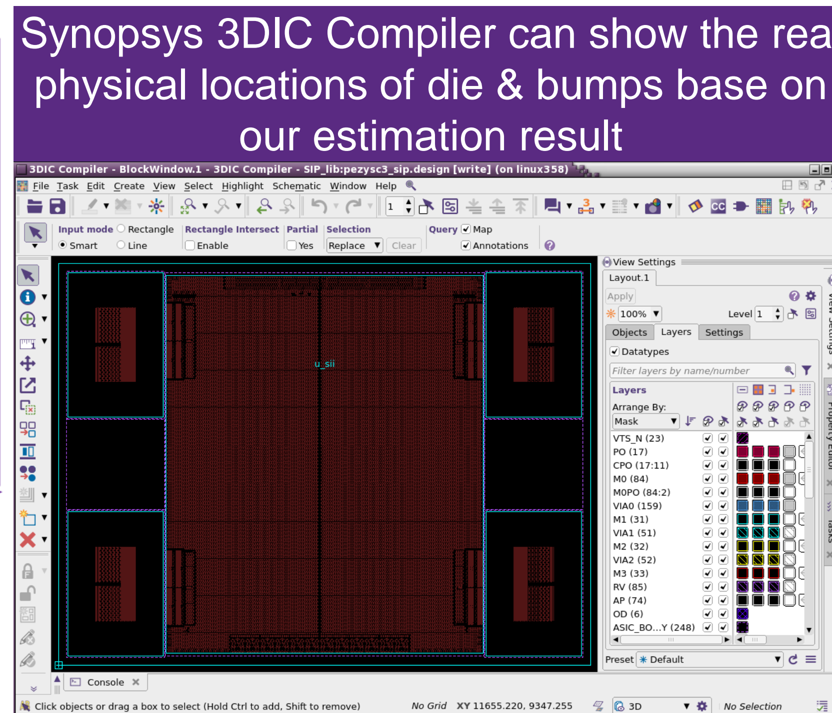
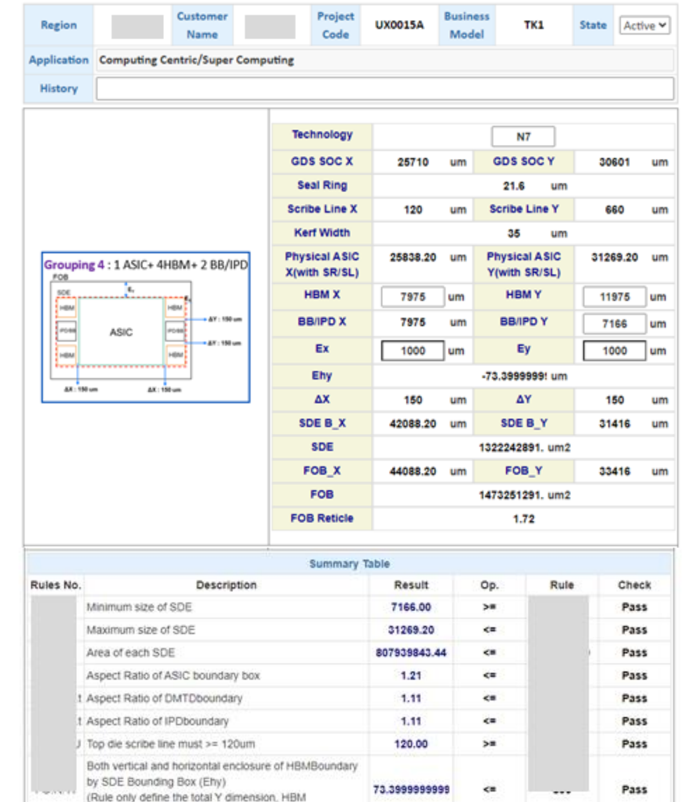
- Floorplan & Size Estimation
  - Foundry design rule consideration
  - Fast verify the available SoC/Interposer size
  - Consider with scribeline, kerf, mask reticle size, dummy die insertion







Region		Customer Name		Project Code	UX0015A	Business Model	TK1	State	Active
Application	Computing Centric/Super Computing								
History									

Grouping 4 : 1 ASIC+ 4HBM+ 2 BB/IPD

Technology	N7			
GDS SOC X	25710 um	GDS SOC Y	30601 um	
Seal Ring	21.6 um			
Scribe Line X	120 um	Scribe Line Y	660 um	
Kerf Width	35 um			
Physical ASIC X(with SR/SL)	25838.20 um	Physical ASIC Y(with SR/SL)	31269.20 um	
HBM X	7975 um	HBM Y	11975 um	
BB/IPD X	7975 um	BB/IPD Y	7166 um	
Ex	1000 um	Ey	1000 um	
Ehy	-73.3999999! um			
ΔX	150 um	ΔY	150 um	
SDE B_X	42088.20 um	SDE B_Y	31416 um	
SDE	1322242891. um2			
FOB_X	44088.20 um	FOB_Y	33416 um	
FOB	1473251291. um2			
FOB Reticle	1.72			

Summary Table

Rules No.	Description	Result	Op.	Rule	Check
	Minimum size of SDE	7166.00	>=		Pass
	Maximum size of SDE	31269.20	<=		Pass
	Area of each SDE	807939843.44	<=		Pass
	Aspect Ratio of ASIC boundary box	1.21	<=		Pass
	Aspect Ratio of DMTDboundary	1.11	<=		Pass
	Aspect Ratio of IPDboundary	1.11	<=		Pass
	Top die scribe line must >= 120um	120.00	>=		Pass
	Both vertical and horizontal enclosure of HBMBoundary by SDE Bounding Box (Ehy) (Rule only define the total Y dimension, HBM	73.3999999999	<=		Pass

CoWoS Top Die Floorplanning with Synopsys 3DIC Compiler

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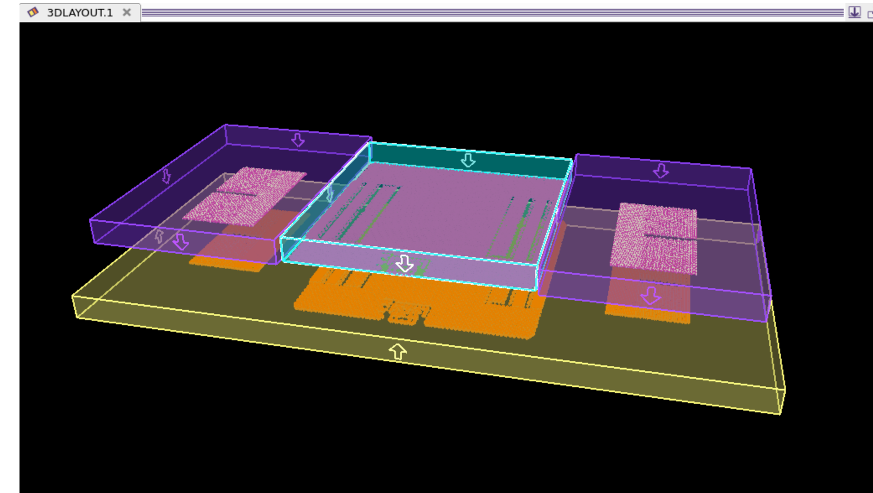
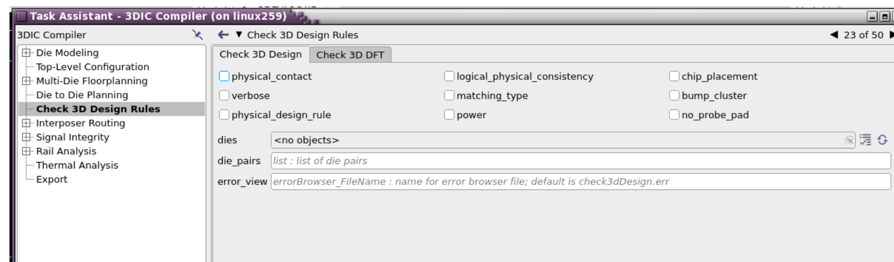
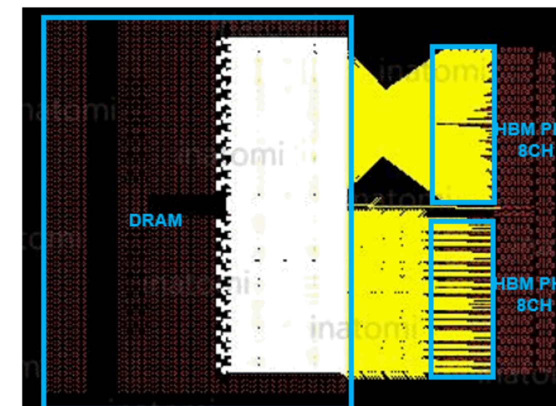


- Multi-die bump planning
  - Top die floorplan
  - Bump mirroring from top die to interposer
  - SoC IP and partition block floorplan
- Quick verification on planning stage
  - Bump alignment, logical connectivity, probepad connection, route-ability check



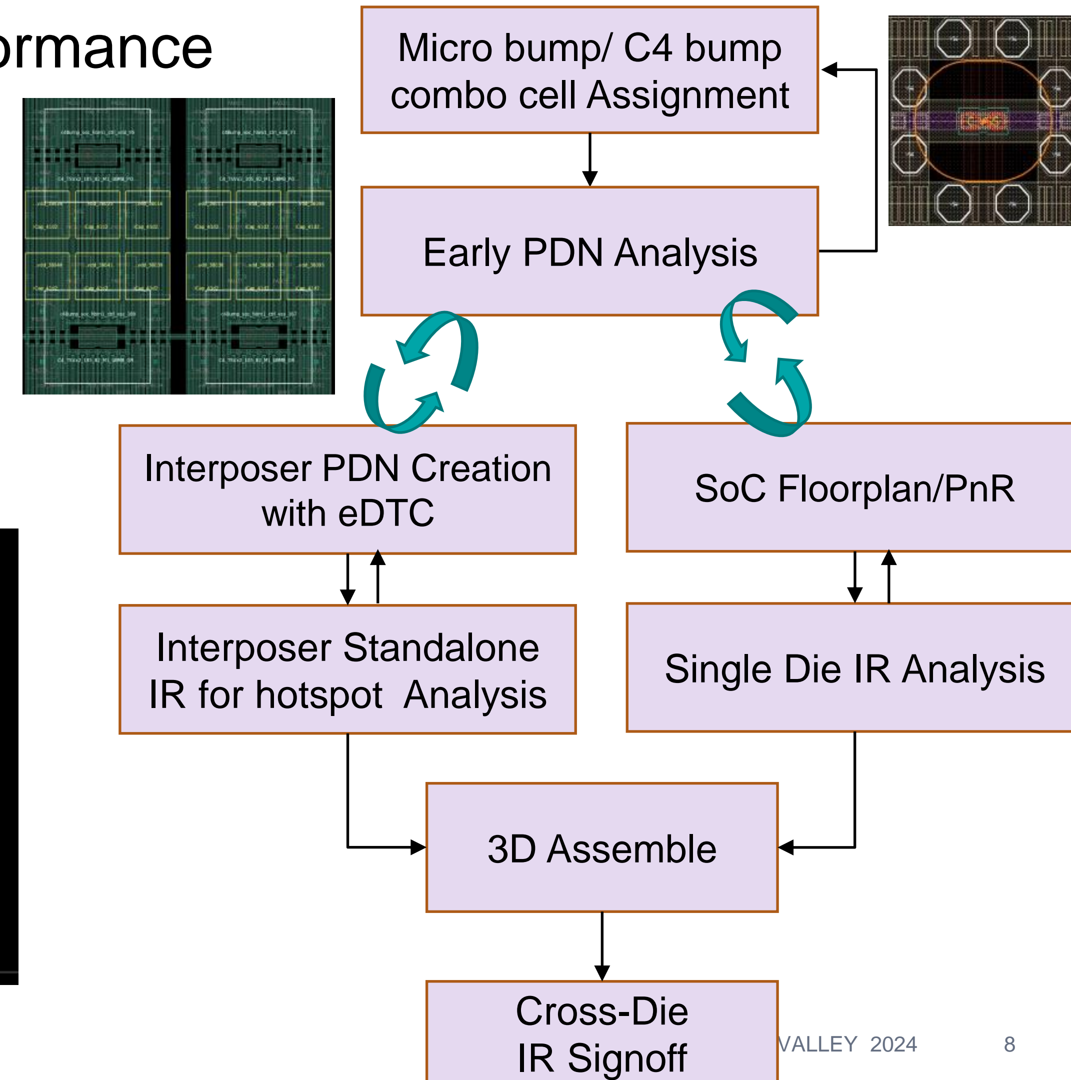


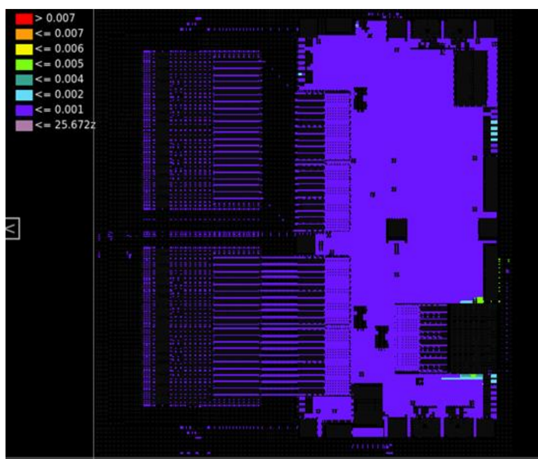
  - Early stage to check SoC IP harden correctness
    - Flyline check routability

CoWoS Bump/DTC PDN Co-design

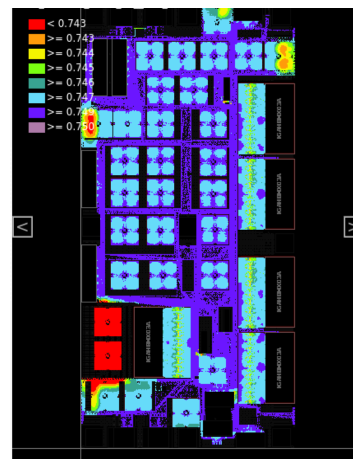
Synopsys 3DIC Compiler can help with bump mirroring and provide stacked view

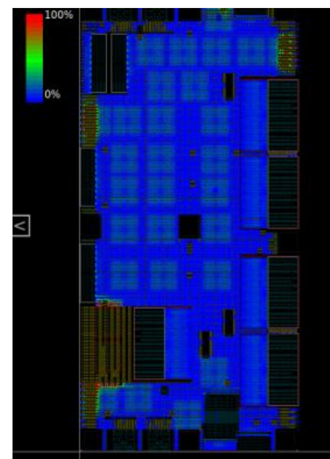
- Use combo C4 bump to have better power performance
- Reduce PG bump change iterations
- Deep Trench Capacitor PDN co-design
- Interposer single-die IR verification
  - Quick static IR verification from ubump to C4bump
  - Attach power on ubump as the current sink





Interposer single die IR





SoC+Interposer cross die IR

CoWoS HBM D2D Routing

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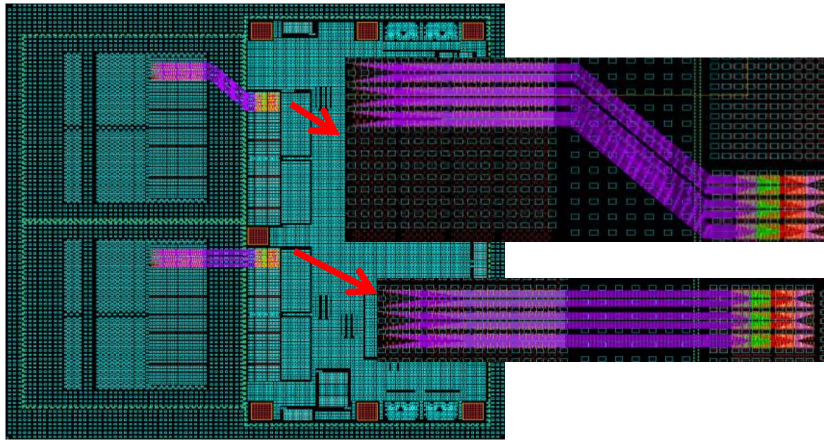
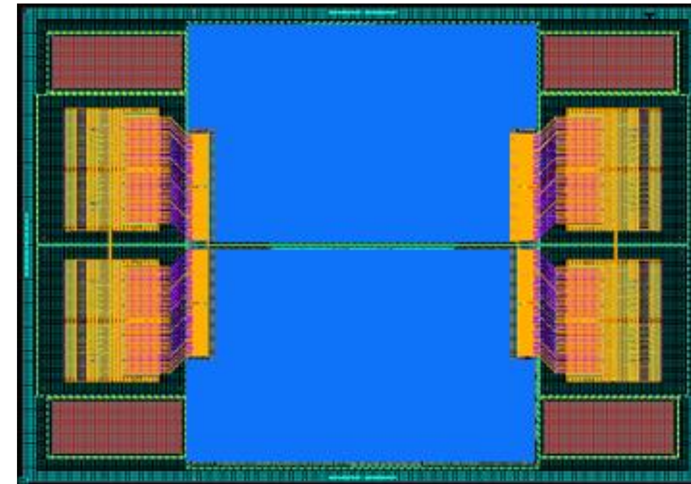
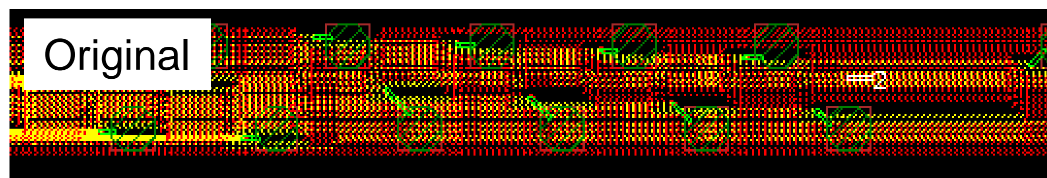
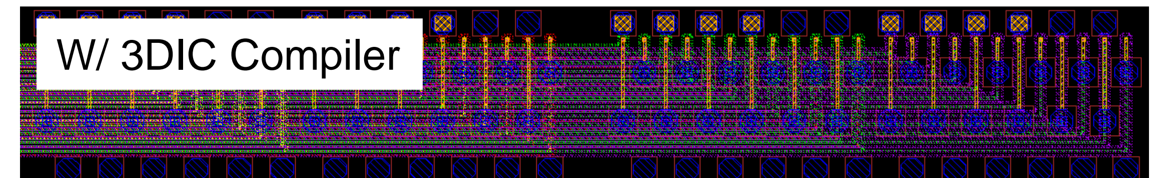
- GUC in-house routing pattern can overdrive HBM3 to 7.2Gbps





- Synopsys 3DIC Compiler D2D Routing Pattern
  - Work at 7.2Gbps through SI simulation
  - Shorten channel signal routing runtime by 50%
  - Easy for channel routing balance





Synopsys 3DIC Compiler HBM Auto Router

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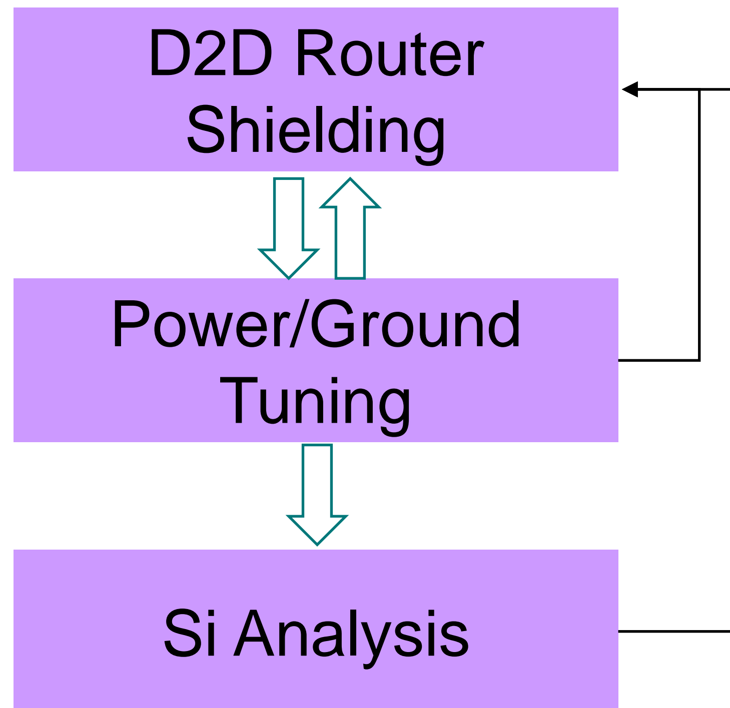
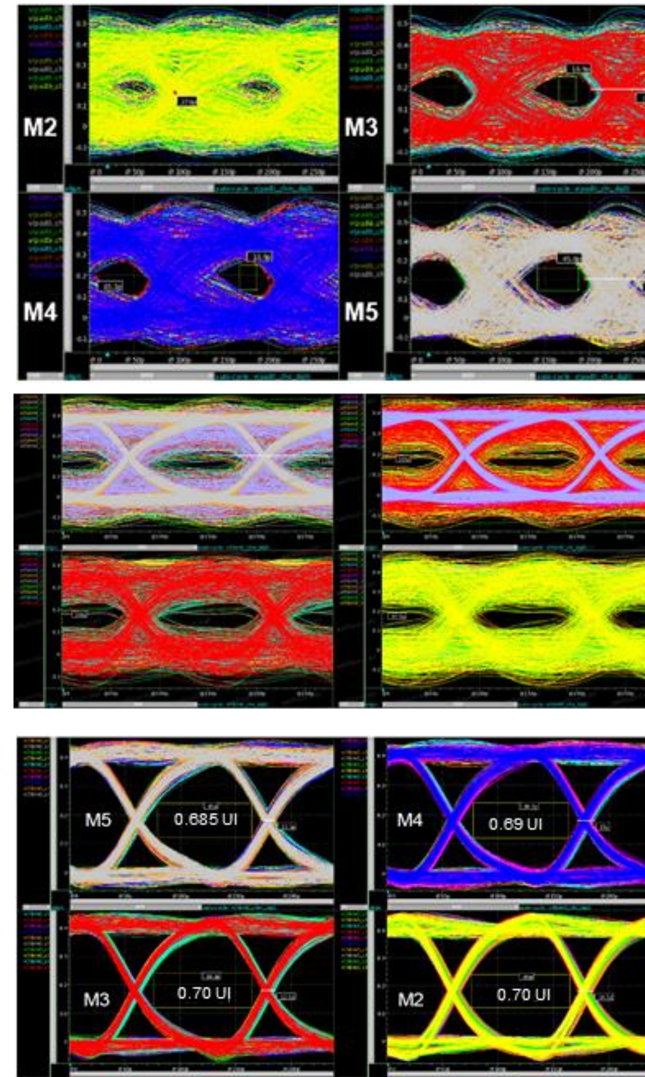
- HBM3 SI Analysis @ 7.2Gbps
  - Result with simple ground shielding
  - Result with default GUC PG pattern
  - Result with PG and shielding fine tune





0.1UI

0.3UI ~ 0.5UI

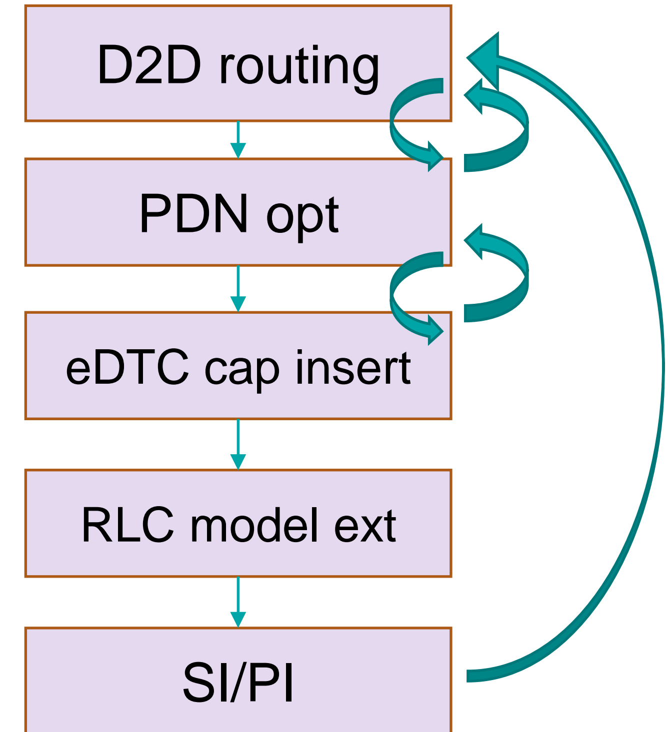
0.685UI

Meet GUC Criteria : 0.5UI

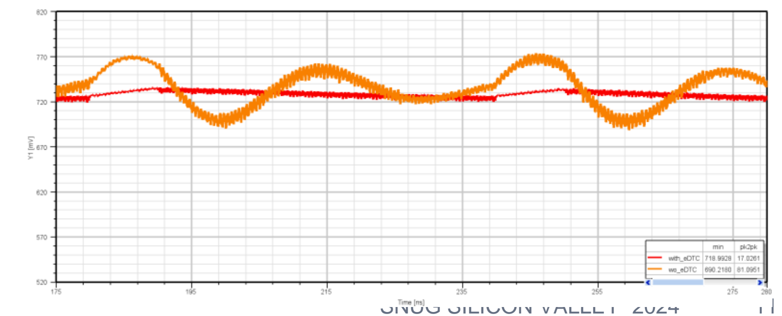
Summary

Synopsys 3DIC Compiler addresses design challenges

- Need to have a useful router
  - 3DIC Compiler can easily modify width, spacing, shielding style
- Need to have a good PG structure
  - GUC has in-house power/ground pattern
- Need to handle critical electrical effect
  - Return loss, crosstalk, insertion loss, etc.
- Need several iterations of pattern fine tune
  - Reduce the iterations with 3DIC Compiler



	Initial Develop	Adjust Pattern	RLC extraction, SI simulation
Scripting	weeks	days	
3DIC Compiler router	days	hours	Weeks to Days
Fully Layout	weeks	week	



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3DIC WoW Design

3D Stacking Design Challenges

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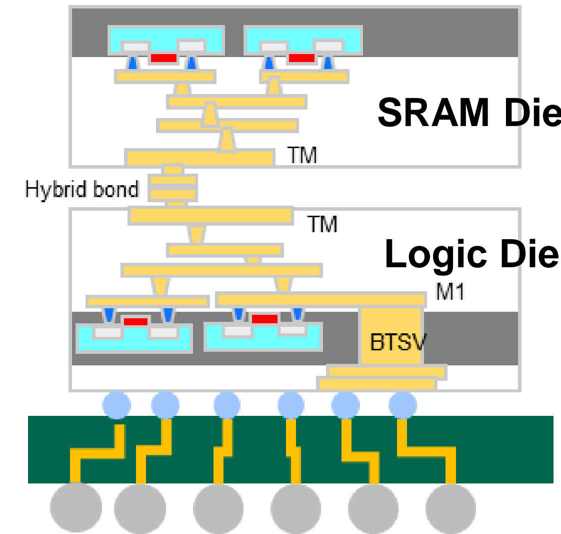
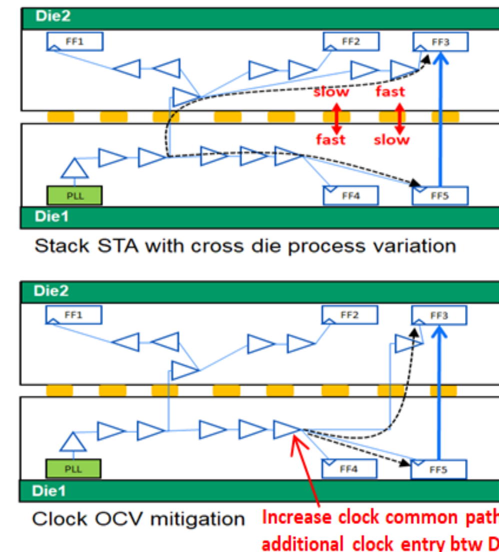
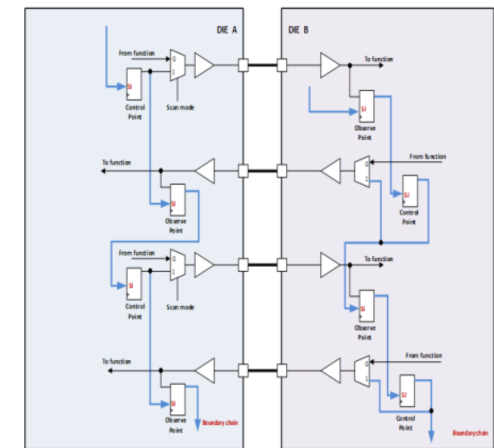
- **Die-to-die interface hybrid-bond assignment**
  - Cross-die hierarchical block stacking & flip alignment for 3D hierarchical design
  - 3D clocking for cross-die OCV reduction
  - P/G and signal hybrid-bond co-design
- **3D-stacking power plan, IR/EM sign-off**
  - Power consumption, TSV #/pitch estimation
  - P/G BTSV array macro design
- **3D-stacking STA: cross-die coupling extraction and process variation**
- **3D-stacking thermal analysis**
- **3D PV: DRC/LVS/3D-stacking check**
- **DFT scan scheme for fault detection**





Stack STA with cross die process variation

Clock OCV mitigation



Scan wrapper for HB fault detection

GUC is Adopting 3Dblox Design Flow

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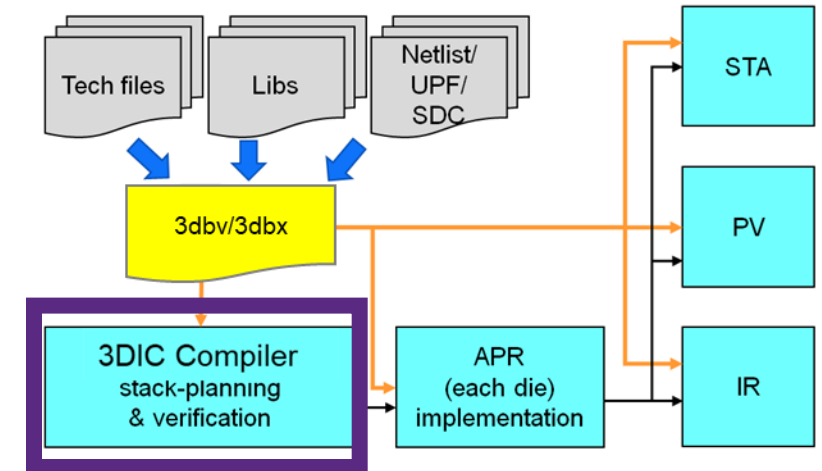
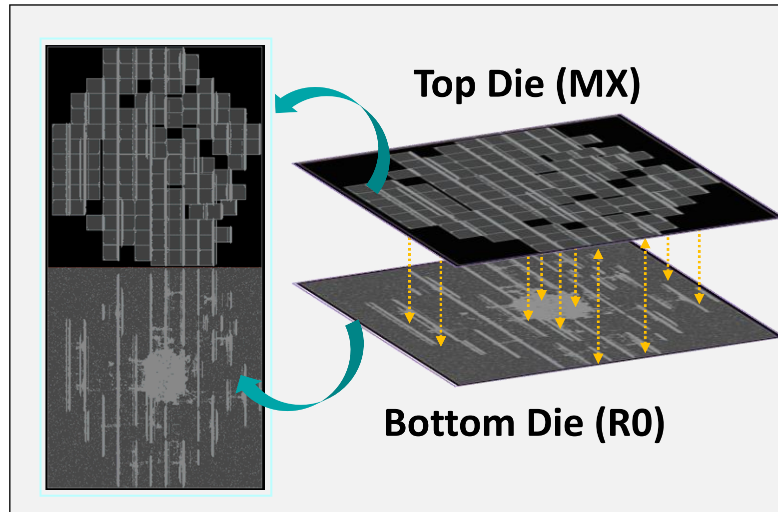
- 3Dblox is a specification of chiplets stacking and connectivity to enable 3D fast prototyping
  - 3Dblox spec (3dbv/3dbx) is defined and fine tuned in early 3D design planning, that verifies the 3D design intent
  - Golden spec to streamline flow integration of P&R, sign-off
- GUC is adopting 3Dblox in 2.5D / 3D chiplet design
  - Synopsys 3DIC Compiler eases adoption of 3Dblox

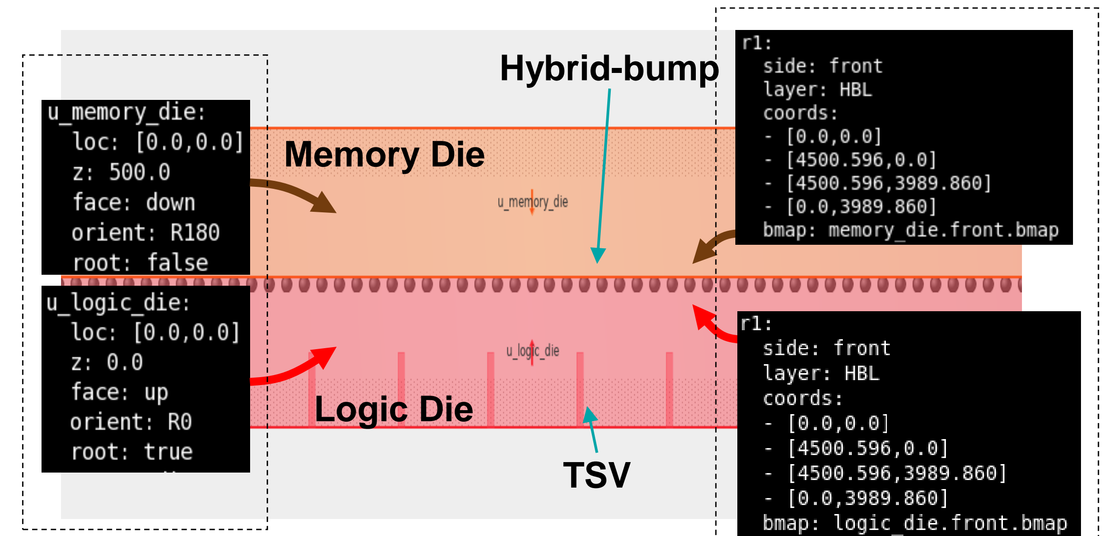





```
Design:
  name: system_top
  external:
    verilog_file: [system_top.v]
    upf_file: [system_top.upf]

ChipletInst:
  u_logic_die:
    master: logic_die
    external:
      verilog_file: [logic_die.v]
      upf_file: [logic_die.upf]
      sdc_file: …

  u_memory_die:
    master: memory_die
    external:
      verilog_file: [memory_die.v]
      upf_file: [memory_die.upf]
      sdc_file: …
```



Stack spec

Connection spec

2.5D/3DIC Implementation with 3Dblox

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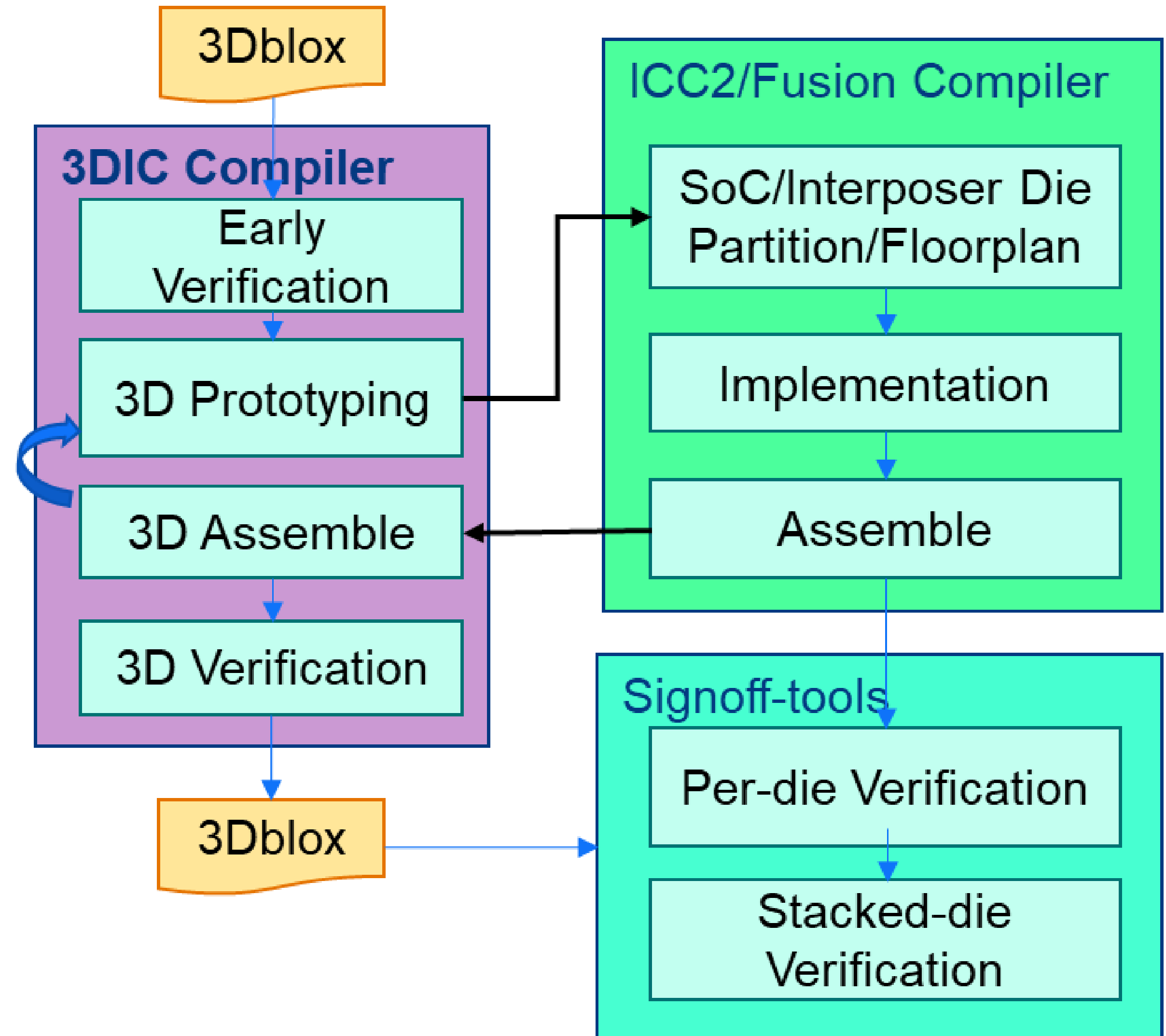
Synopsys 3DIC Compiler

- 3D Prototyping & Early Verification
  - Cross die bump assignment
  - Early PDN verification
- 3D Assemble & 3D Verification
  - Bump alignment check
  - Path Assertion
  - Synopsys StarRC cross die VIB extraction
- Signoff by using 3Dblox to physical verification and RC extraction



Synopsys 3DIC Compiler

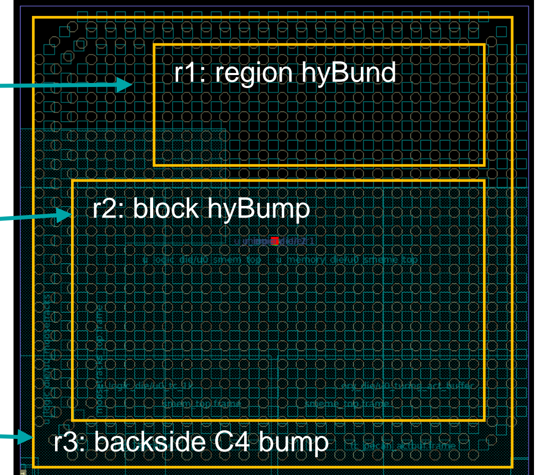
3D Bump Assignment and Alignment Check

- 3Dblox specify regions for bump assignment. It's useful for the partial bump update

top die 3dbv

```
regions:
  r1:
    side: front
    layer: HBL
    coords:
    - [898.0,2239.840]
    - [4500.496,2239.840]
    - [4500.496,3989.860]
    - [898.0,3989.860]
    bmap: memory_die.front.bmap
  r2:
    side: front
    layer: HBL
    coords:
    - [0.0,0.0]
    - [4500.556,0.0]
    - [4500.596,2239.860]
    - [0.0,2239.8R6]
    bmap: top_die.front.bmap.block1_region

  r3:
    side: back
    layer: APS
    coords:
    - [0.0,0.0]
    - [4500.596,0.0]
    - [4500.596,3989.860]
    - [0.0,3989.860]
    bmap: top_die.back.bmap
```



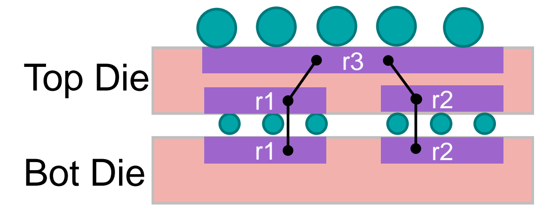
- 3Dblox path assessment can quickly check cross die bump alignment

system.3dbx

```
Connection:
  Conn1:
    top: u_bot_die.regions.r1
    bot: u_top_die.regions.r1
    thickness: 0.0

  Conn2:
    top: u_bot_die.regions.r2
    bot: u_top_die.regions.r2
    thickness: 0.0
```

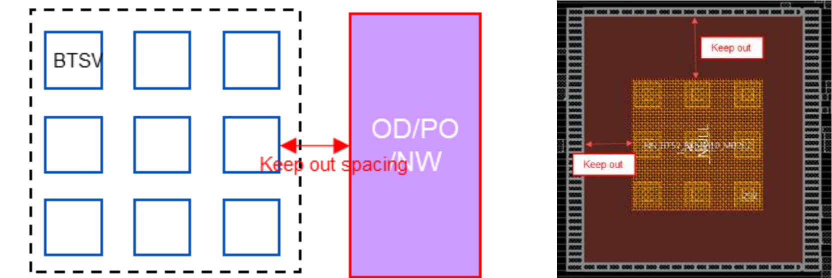
```
Path:
  Path1:
    - u_bot_die.regions.r1
    - u_top_die.regions.r1
    - u_top_die.regions.r3
  Path2:
    - u_bot_die.regions.r2
    - u_top_die.regions.r2
    - u_top_die.regions.r3
```

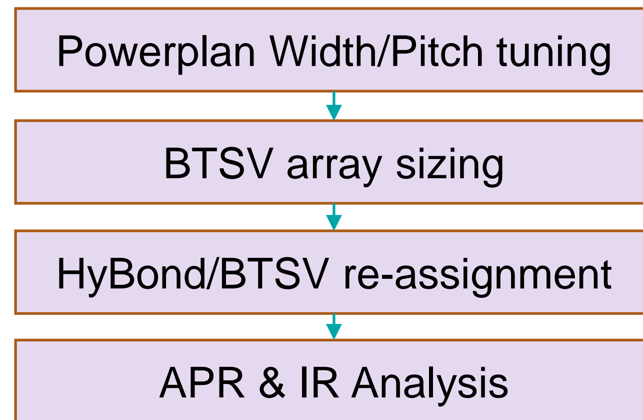


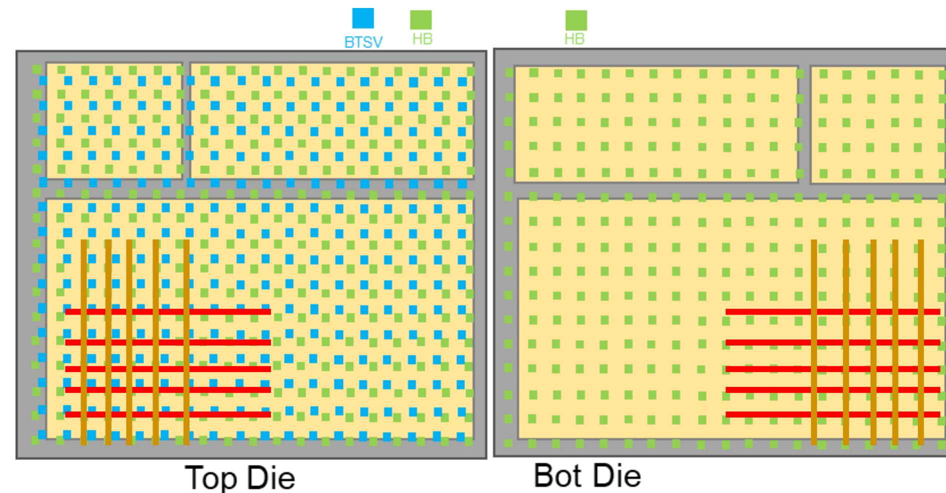
- Cross die bump alignment check helps physical and logical verification

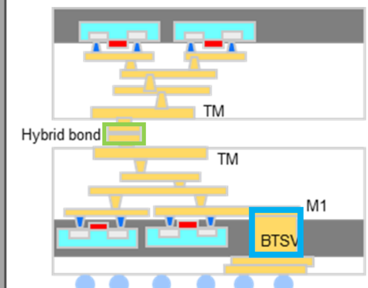
Power Plan with BTSV Array Structure

- ◆BTSV has OD/PO/NW keep-out spacing, a trade off between power and routability
- ◆Achieve it with considering metal width, bump pitch, BTSV array size







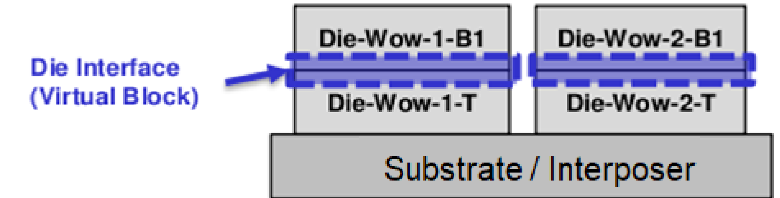


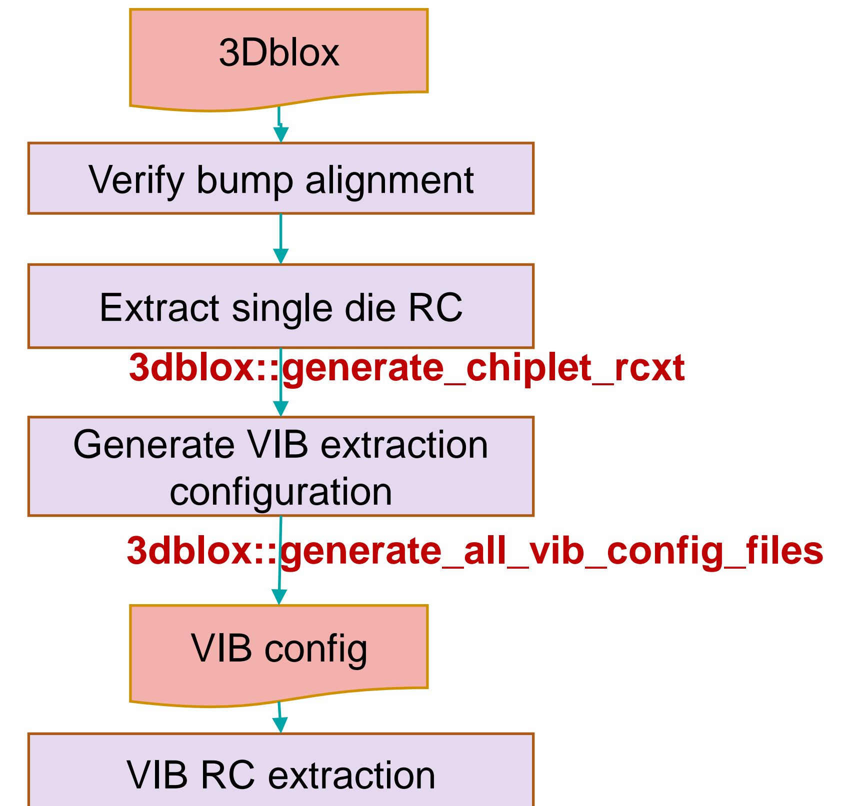
◆Synopsys 3DIC Complier rail analysis

- ■Leverage in-design Ansys Redhawk_SC with early PG constrains for quick early IR analysis. It reduces our design iterations.

3D Cross-Die VIB RC Extraction

- For cross die STA, it needs to consider interface RC parasitic
- Synopsys StarRC support cross-die virtual interface block (VIB) RC extraction
- Synopsys 3DIC Compiler integrate VIB extraction by verifying interface alignment with 3Dblox and generating StarRC VIB configuration
  - 3Dblox specify DEF, LEF, LIB, RC files for each die
- GUC used to achieve it with scripting on die stacking and bump alignment, a long development to pipe-clean the flow





Conclusion

Conclusion

- 2.5D/3DIC have become more and more complex. It’s essential to have an assembly tool to handle whole design in 3D view.
- Synopsys 3DIC Compiler improves our HBM routing results, simplifies 3DIC stacking, and improves design quality.
- 3Dblox facilitates the specification of 3D design intent, good for data preparation, version control, and easy communication in design hand-off.
- With 3Dblox & Synopsys 3DIC Compiler, we save numerous design iteration, resulting in much shorter time to market.

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THANK YOU

Our
Technology,
Your
Innovation™