Enabling Next-Generation Advanced ASICs

Using Synopsys high-speed interface IPs

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GUC

Agenda

Synopsys IP Enables High End ASIC

Success Stories of Automotive ASIC Collaboration

Test Requirements for Automotive IC

Trends in Automotive Semiconductors

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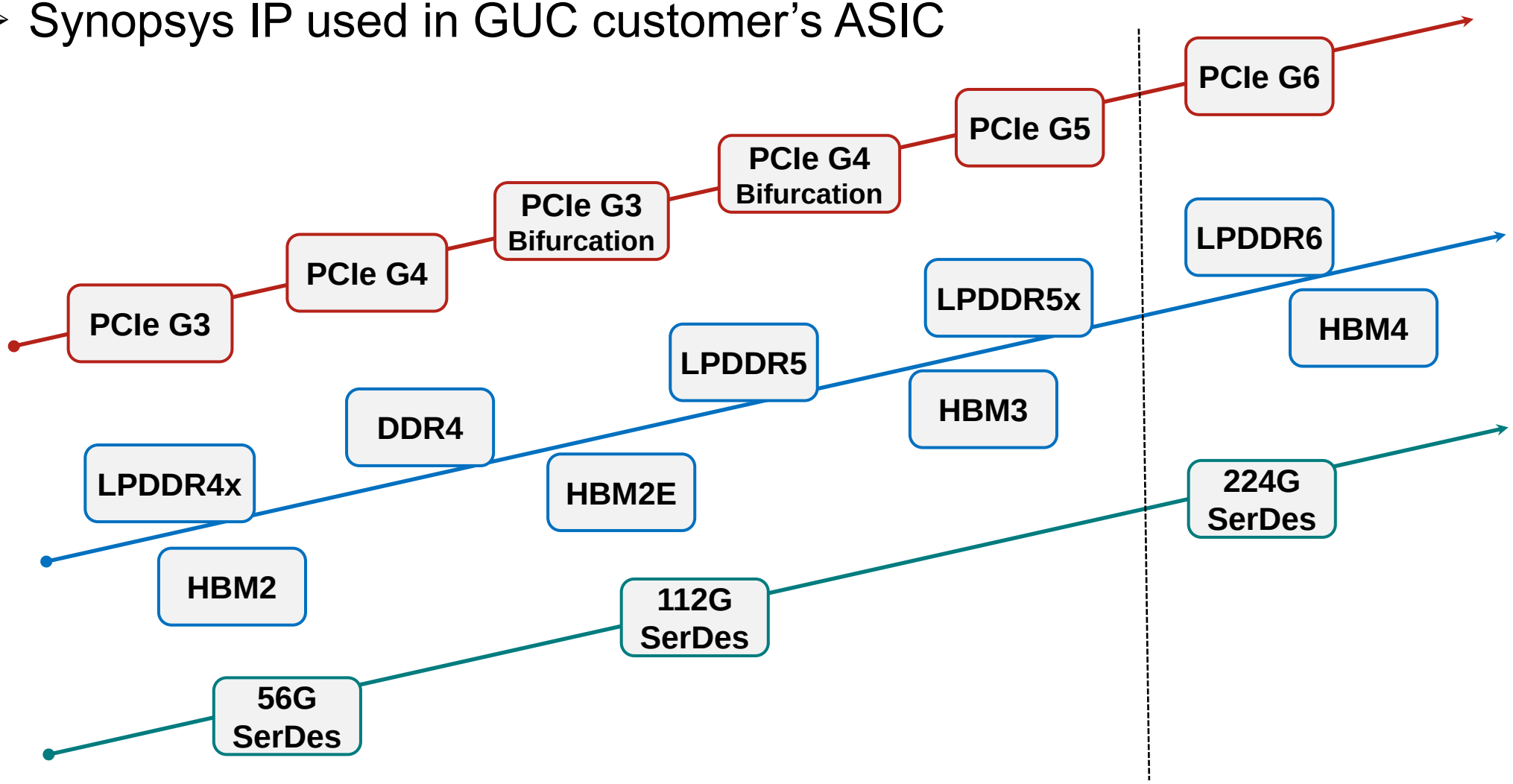
IP Significance in Modern ASICs

- High-speed Interface IPs play a key role in enabling advanced ASICs
  - AI / HPC / Automotive / Networking SoC becoming bigger and more complex
    - billion gate count, reticle size (~800mm^2), hundreds of IP blocks
  - High-speed Interface IP speed/bandwidth doubles each generation
    - PCIe, USB, DDR/LPDDR, SerDes…
  - Key factors: power and area efficiency, backward compatibility, interoperability, IP readiness & robustness
- Automotive grade IP requirement for ADAS and V2X ASIC
  - ISO26262 ASIL
  - AEC-Q100/104

High-Speed Interface IP Adoption

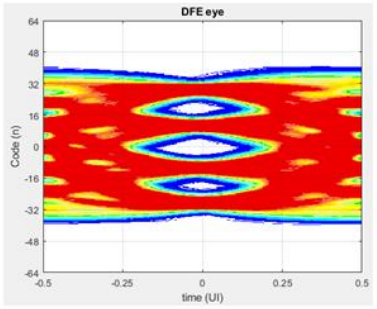
- Synopsys IP used in GUC customer's ASIC



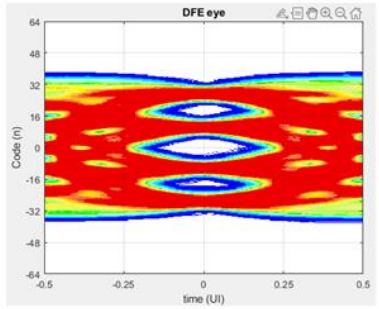
High-Speed SerDes IP

➢Synopsys 112G SerDes Cosim Result

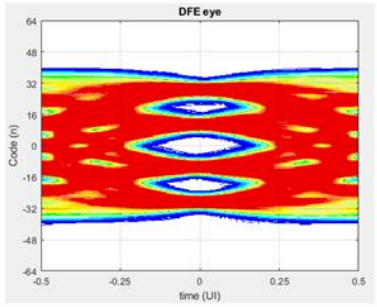
PHY0_TX0



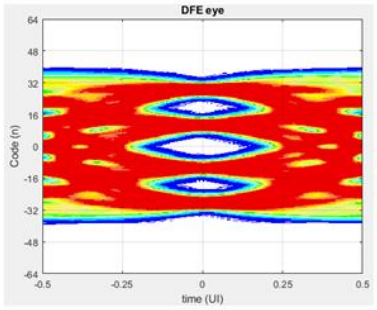
PHY0_TX3



PHY0_RX0



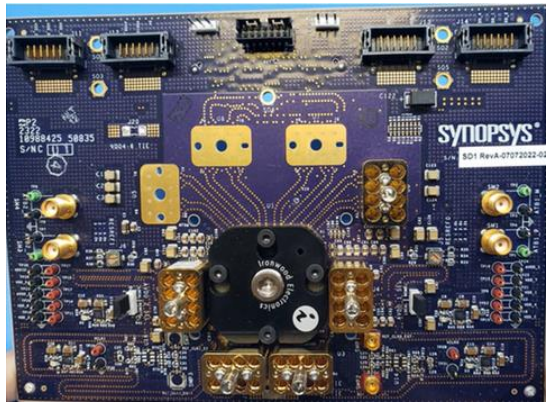
PHY0_RX3

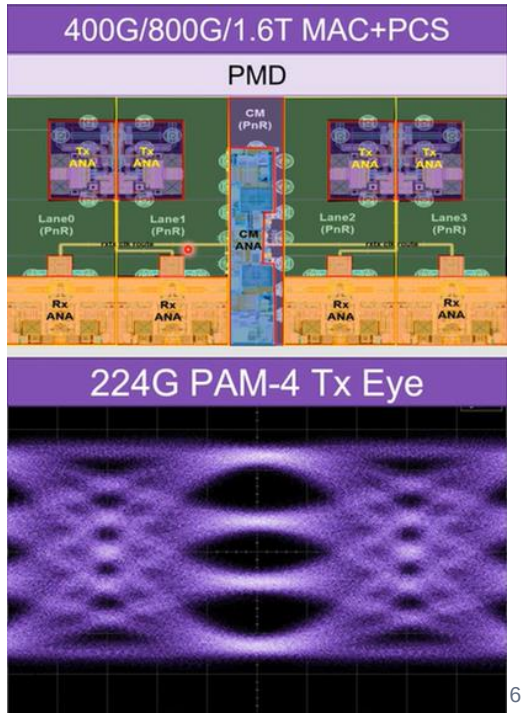


	Calculate BER Result	SPEC
PHY0_TX0_SScorner	1.785708E-06	<1.000E-05
PHY0_RX0_SScorner	1.785708E-06	
PHY0_TX3_SScorner	1.785708E-06	
PHY0_RX3_SScorner	1.785708E-06	

➢Synopsys 224G SerDes Evaluation

- Healthy eye opening
- Exceed spec RX performance





GUC Spec-in SoC with Synopsys IPs

GUC The Advanced ASIC Leader

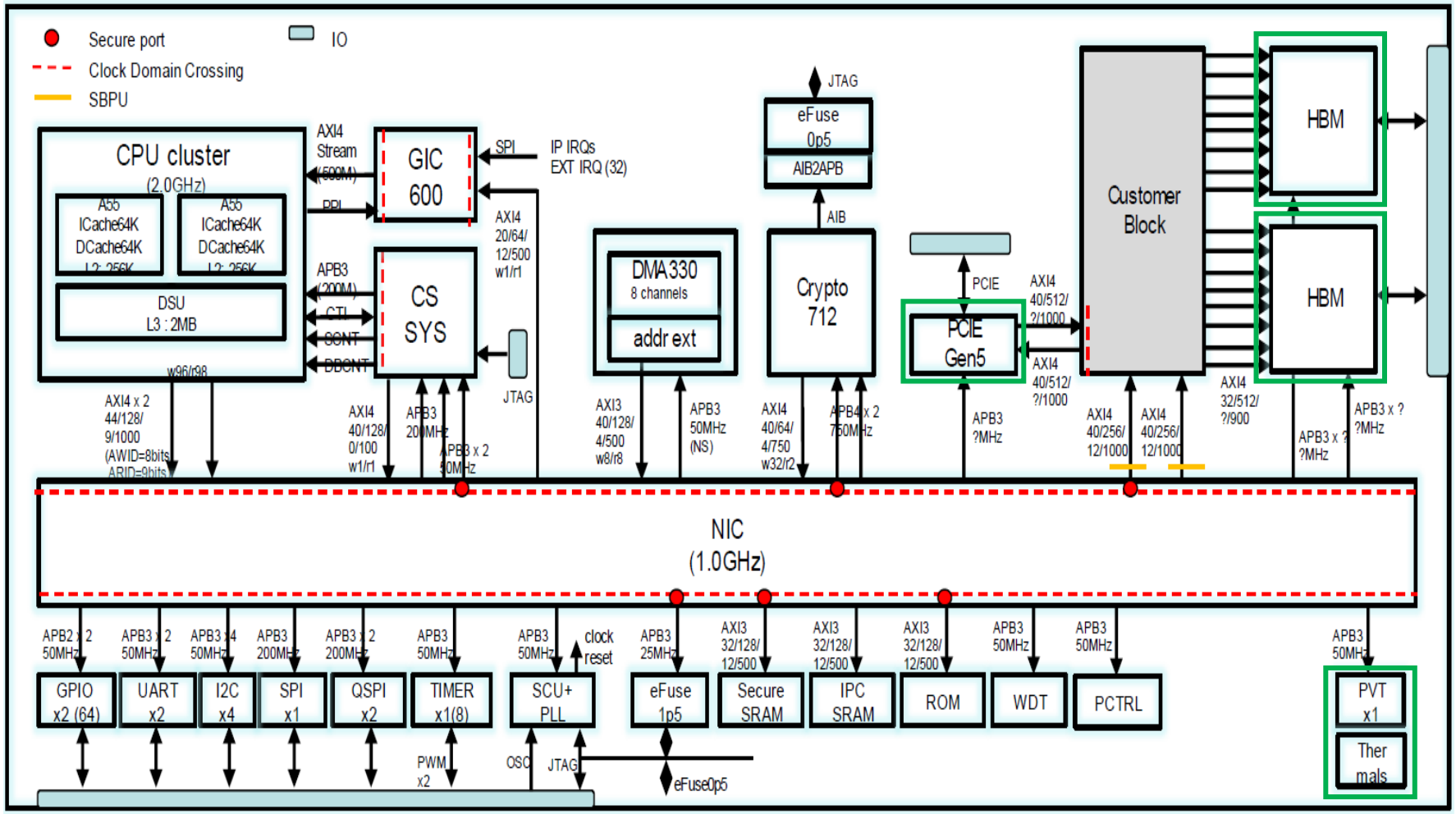
snug

➢Full Spec-in design service from Spec to Silicon to Production

– Provide one-stop spec-in service covering architecture optimization, IP solution, IP/subsystem/chip integration/verification, SW service, and system emulation

	Application	Process	Key features	Logic Gates	Technical highlights
1	AI Datacenter	5FF	CA55x10, Customer Octa AI engines PCIe5, HBM3, Thermal sensor, Voltage monitor, Process detector, PVT	~5000M	AI performance Complex PCIe5 bifurcation, HBM3 sub-system
2	AI AR/VR	7FF	CM55, CU55, MIPI, Customer AI engine	~13M	MIPI TX/RX SS
3	Networking	12FFC	CA53x4, DDR4, PCIe3, SATA3, Ethernet, USB2	~35M	5G networking bus matrix bandwidth optimization
4	AI Data Center	12FFC	Customer AI engine, PCIe4	~1000M	AI engine performance Complex HS IPSS
5	8K Camera	12FFC	CA35x4, CA5, Crypto, PCIe3, HDMI2.0, DP1.4, DSI, MPHY, LPDDR4x, customer ISP	~160M	Critical bus timing DDR access efficiency Complex HS IPSS
6	8K Camera	12FFC	CA35x4/x1, Crypto, PCIe3, LPDDR4x, customer ISP	~80M	Critical bus timing DDR access efficiency
7	Automotive	16FFC	Customer engine, ADC MIPI, SerDes, LBIST	~30M	High speed ADC LBIST in automotive
8	HBM2/CoWoS	16FF+	CA72x2, HBM2, PCIe4	~50M	HBM, CA72 performance CoWoS flow
9	AI Vision	28HPC+	Customer AI engine, CA5, H264, PCIe3, DSI/CSI	~85M	DDR access efficiency Bus matrix optimization

Synopsys IP - AI accelerator example



- SoC Top-Level design, verification, FPGA, emulation, Firmware, board design, silicon bring-up, and validation
- CA-55 10-core subsystem
- PCIe5 subsystem
- HBM3 subsystem
- Chip size : 632mm²
- Power : 400W

➢ SNPS IP Used
- HBM, Thermal sensor, Voltage monitor, Process detector, PVT controller

GUC + Synopsys (Total Service Package)

- IP Configuration based on Customer's spec
  - Complex IP has hundreds of configurations
- Subsystem Integration
  - Integrate the PHY, I/O, controller, system bus, clock, reset, glue logic…etc
  - HBM, DDR/LPDDR, PCIe, USB, HDMI, MIPI…
- Design Verification
  - Verify IP subsystem from block level to chip top function
  - Synopsys Verification IP (VIP), VCS
- Software & Prototyping
  - Driver, Software, FPGA, prototyping
  - Synopsys daughter board (PCIe, SATA…)
- Testing & Qualification
  - Chip level DFT design and ATE pattern
  - Synopsys TestMAX family

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Automotive Product Requirements ISO26262

– What is ISO26262?

– ISO26262 is a functional safety standard for automotive products.

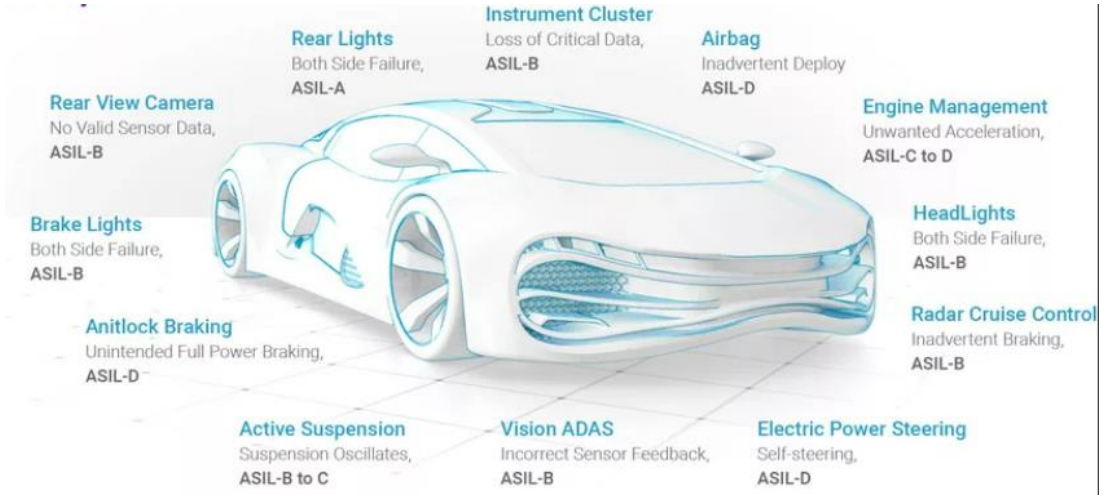
– 4 ASILs (Automotive Safety Integrity Level) establish a risk classification system—based on the probability and acceptability of harm.

– 4 ASILs→ A, B, C, and D.

– ASIL A represents the lowest degree. ASIL D represents the highest degree of automotive hazard.

- Systems like airbags, anti-lock brakes, and power steering require an ASIL-D. Failure of these systems pose the highest risk

- Components like rear lights require only an ASIL-A grade. Head lights and brake lights generally would be ASIL-B while cruise control would generally be ASIL-C.



Automotive Product Requirements AEC-Q100/104

➢What is AEC Q100/104 ?

- Qualification criteria covers failure mechanism based stress tests, minimum stress test driven qualification requirements and test conditions for qualifying ICs (Integrated Circuits).

- The idea is to determine devices which can pass the defined stress tests. This provides devices which can offer certain level of quality and reliability in the application.

- AEC Q100 defines four temperature grades from 0 to 3. These ranges are based on operating range of ICs.

Grade	Ambient operating temperature range
0	- 40°C to +150°C
1	- 40°C to +125°C
2	- 40°C to +105°C
3	- 40°C to +85°C

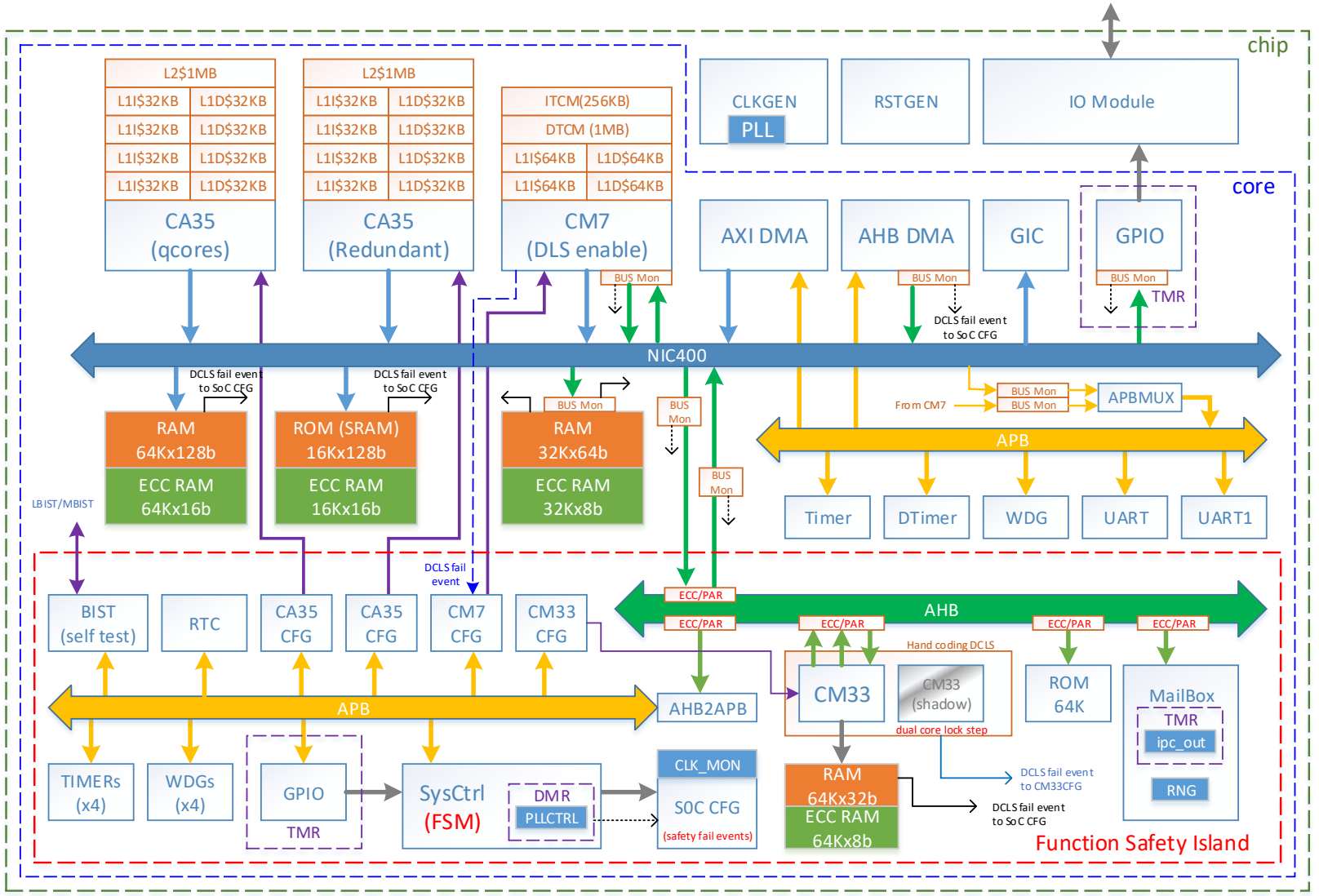
AEC-Q100 includes 4 temperature grades. (Table: Synopsys)

- AEC Q104 covers stress tests and its qualification requirements based on failure mechanism for Multichip Modules (MCM). It also mentions reference test conditions. Single MCM consists of multiple electronic components in single package enclosure. This document can be applied to MCMs which can be soldered directly to PCB.

- Based on pass/fail criteria, multichip modules are chosen which can provide certain level of reliability and quality in the application.

Success Story - ADAS Example

- **CPUs**
  - Cortex A35 (1.57GHz)
  - Cortex M7 (785MHz)
    - Enable dual lock step
  - Cortex M33 (131MHz)
    - Design for dual core lock step
- **Reliability for Design**
  - Manual Coding for SM
    - ECC for SRAM
    - ECC & parity check for bus
    - Bus monitor
    - Clock monitor
  - SM inserted by Synthesis tools
    - TMR/DMR inserted
    - Failsafe FSM coding
    - ECC/EDC & parity inserted
- **Function safety island**
  - Self test by CM33
    - LBIST/MBIST for CPU & TOP
  - Safety monitor & management



DFT Approach for Low DPPM

	General Product	Automotive Product	Note
Digital	• SAF > 98.5% • Transition > 80%	• SAF > 99% (1) • Transition > 85% (2) • Pseudo Stuck-at IDDQ fault > 80% (3) • Small Delay (Optional) • Bridge (Optional)	[AEC_Q100 Standard] 1. SAF > 98% (97% if IDDQ is included) 2. Transition > 80% 3. Pseudo Stuck-at IDDQ fault > 70%
SRAM	• March 68N • Checkerboard & Inverse background data • Physical mapping	• March 68N • Checkerboard & Inverse background data • Physical mapping	Automotive qualified memory IP is required
ROM	• ReadOnly 2N	• ReadOnly 2N	Automotive qualified memory IP is required
Analog	• Functionality check • Specification check	• Functionality check • Specification check • Increase analog testability (1) • Analog test modes built in (2) • Analog BIST (3)	1. Internal reference voltage monitor 2. Analog bias tuning setting to touch performance boundary 3. Analog loop back

DFM Approach for Reliability

➢DFM Technology for TSMC process nodes

DFM Technology	40LP 40G	28HPM 28HPC+	16FF+ 16FFC	12FFC	7FF	5FF	3FF (roadmap)
Dummy Fill Insertion	V	V	V	V	V	V	V
LDE Consideration	V	V	V	V	V	V	V
Process Control Pattern (TCD / ICOVL)	V	V	V	V	V	V	V
DFM via	V	V	V	V	V	V	V
Extended Physical Rule Check	V	-	V	V	V	V	V
Tightened EM Specifications	V	V	V	V	V	V	V

V : General Product
V : Automotive Product

Mission Profile & Sign-off Reliability

➢Aging Effect

– Re-K aging timing library to guard-band the digital circuit design timing in setup critical corner

– Add aging mismatch OCV to consider clock variation

Mission profile

Customer	$T_{ambient}$	$T_{junction}$	Voltage	Time	Cum.
-	-	125	1.1*Vnom	3 years	0.0001%

◆ Provide waveform info for AC aging (frequency, duty cycle, etc.)

TSMC QR provide ΔVth

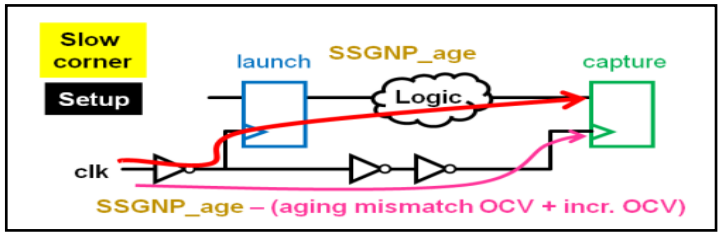
Devices	DC aging (BTI only)		AC aging (BTI + HCI)	
	ΔVth @99.9999%	ΔVth @0.0001%	ΔVth @99.9999%	ΔVth @0.0001%
NMOS-SVT	a1	A1	a2	A2
NMOS-LVT	b1	B1	b2	B2

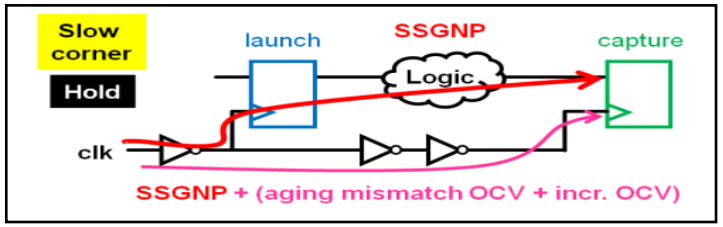
TSMC/GUC Lib Re-K

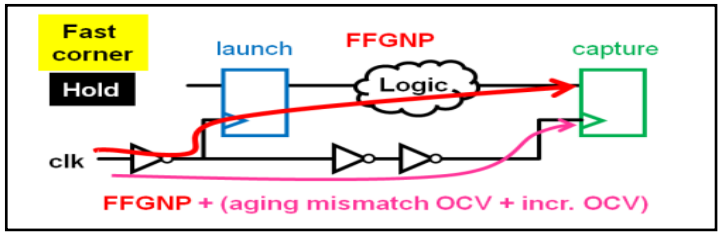
Pick either DC or AC aging to do lifetime corner (LC) simulation
➔ Get (1) stdcell & SRAM aging timing Lib. (2) Aging mismatch OCV
(turn on LC mode:.param lcflag=1, set ΔVth by lc_dvtlin_ parameters)

Sign-off

Setup time aging mismatch OCV = D_{BC}/D_{WC}
Hold time aging mismatch OCV = $1+D_{WC}-D_{BC}$
$D_{WC} = Delay_{WC}/Delay_{T0}$, $D_{BC} = Delay_{BC}/Delay_{T0}$

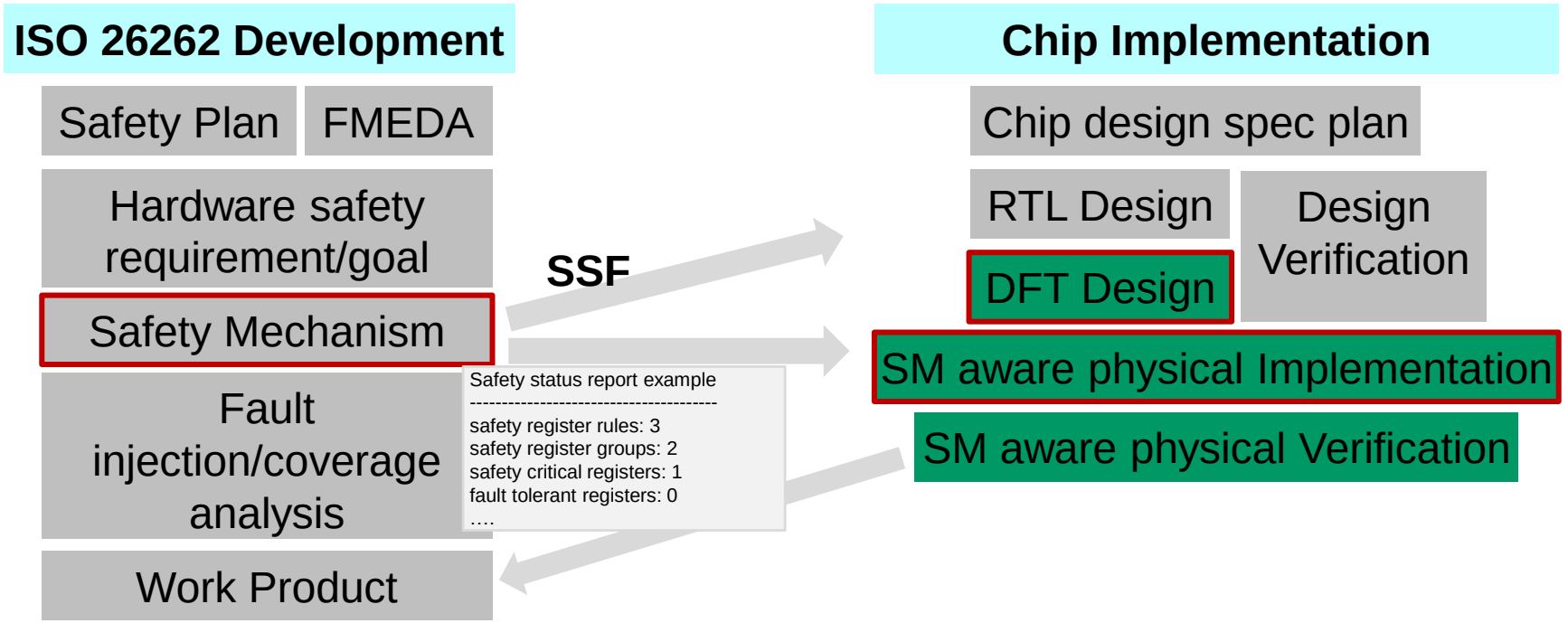






Safety Mechanism Handoff (for Implementation)

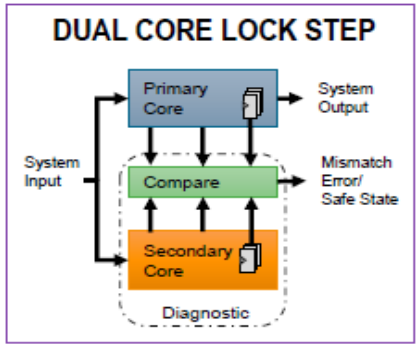
- SM spec handoff for DFT design and physical implementation
  - SSF (Safety Specification Format)
- Implementation results output for ISO26262 report (work product) reference
  - Safety status report, DFT test coverage, …

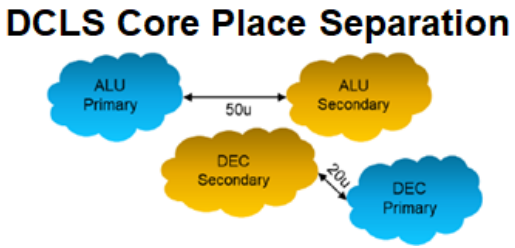


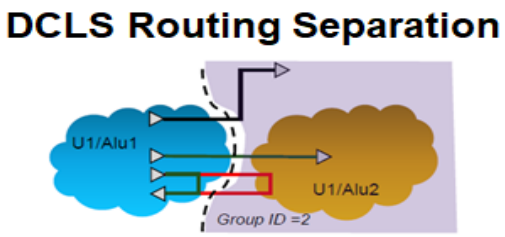
Safety Mechanism Aware Implementation Flow

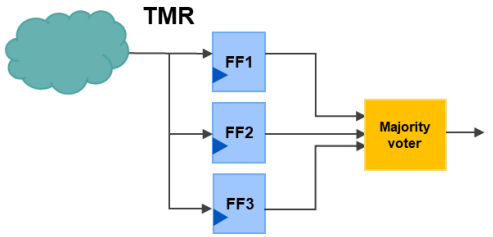
➢Follow SSF to implement, maintain, and verify Safety Mechanism

Safety Mechanism	Synopsys EDA	Flow Enable Feature
Safety Register (TMR, DMR)	V (FC)	Synthesis – Voter logic synthesis P&R – Radial distance separation; TMR well, rail separation; TAP cell isolation
Verification	V (Formality, ICV)	Logic verification – Formal EQ check Physical verification – Independent FFI check
Dual Core Lock Step (DCLS)	V (FC)	Core place separation CTS-aware clustering of FFs Routing separation
Redundant Via Insertion (RVI)	V (FC)	RVI-aware routing

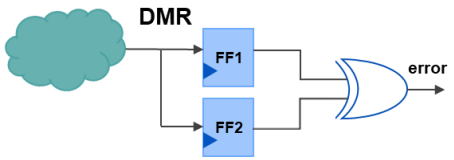








Triple modular redundancy (TMR)
Each identified register is replaced by 3 registers and its voting logic, output is self-corrected

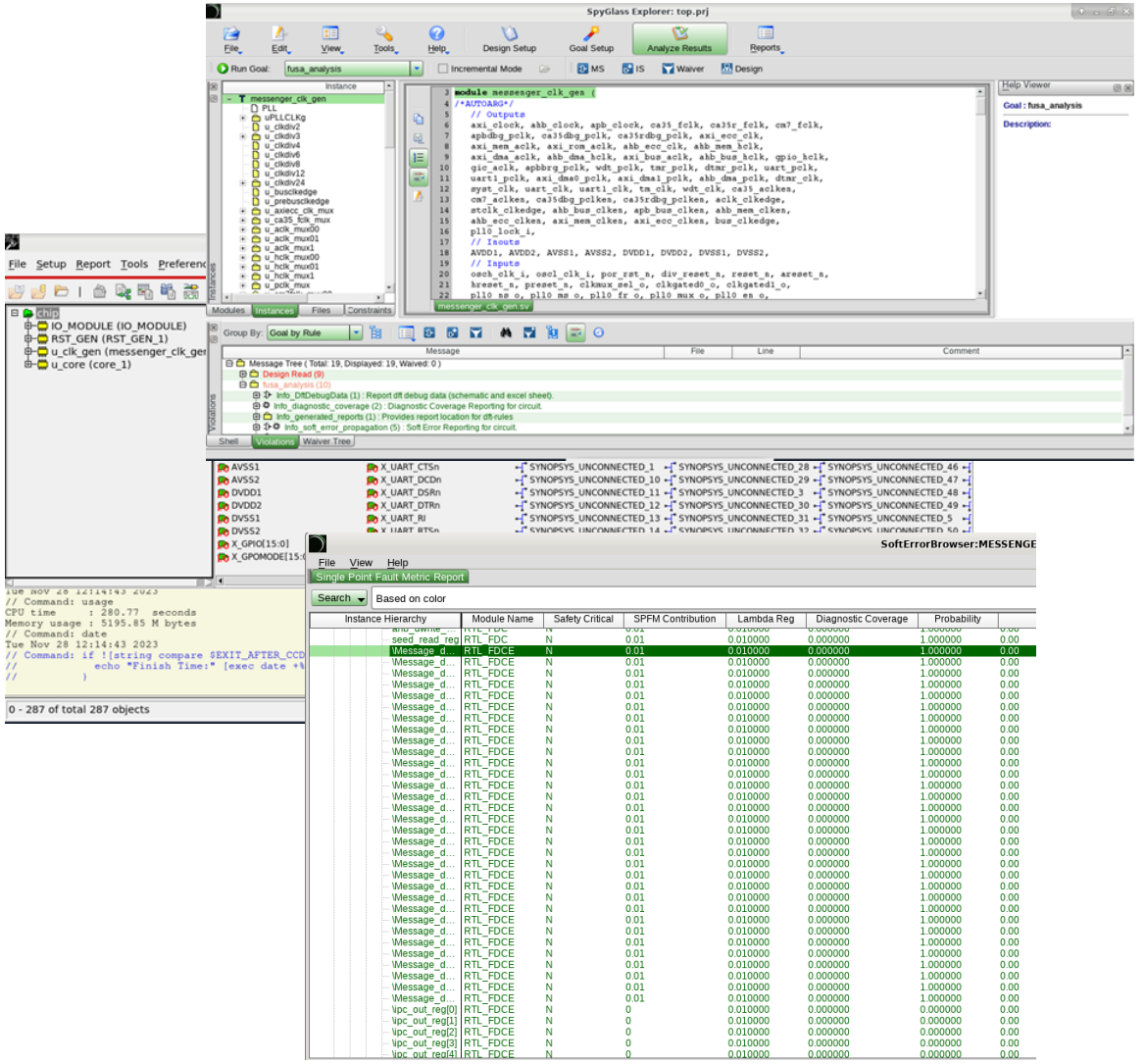


Dual modular redundancy (DMR)
Each identified register is replaced by 2 registers with error detection

Dual Core Lock Step (DCLS)
DCLS improves system reliability by running two identical logic cores in parallel and parses their outputs through a comparator logic

Safety Mechanism Design Analysis

- FuSa Analysis
  - Soft error analysis using Spyglass
  - Static analysis ensures minimum impact design schedule and efficient design improvement
  - SPFM (Single Point Fault Metric) report
- Clock Domain Synchronization Assurance
  - Find combinatorial paths that are crossing clock domains without synchronization
  - Generates report for all paths that user can then use to synchronize the path
- Constraint Checking
  - Check constraints prior to RTL synthesis
  - Check constraints syntax and for timing constraints applied to non-existent or invalid types of arguments/objects



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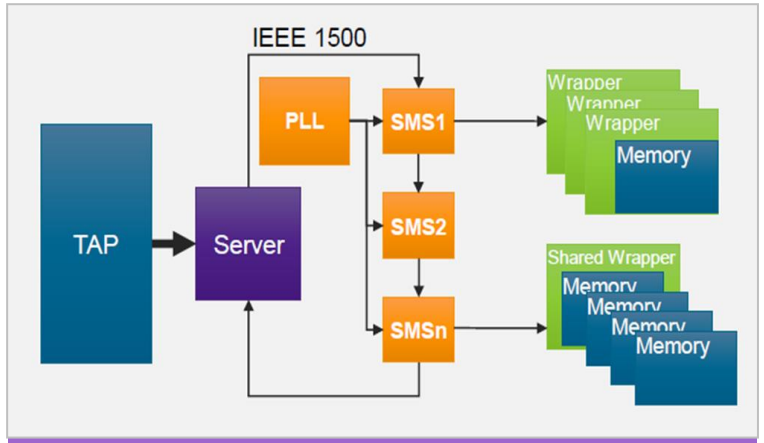
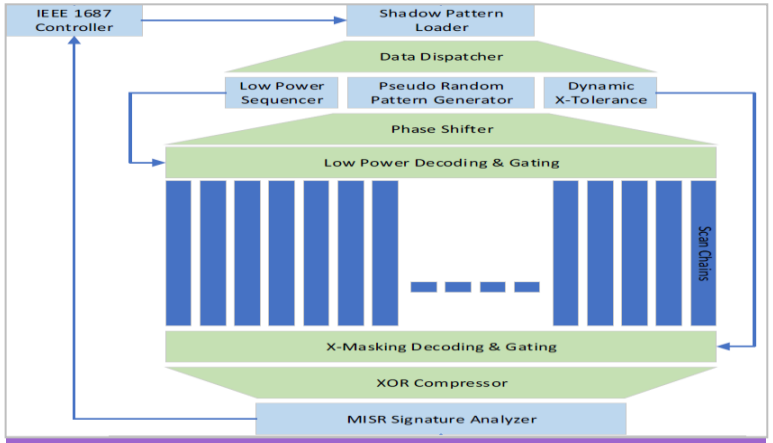
Test Requirements for Automotive IC

- In-System test is important for Automotive and Safety-critical applications
- Logic BIST and SRAM BIST are often leveraged for system BIST design purposes



TestMAX SMS

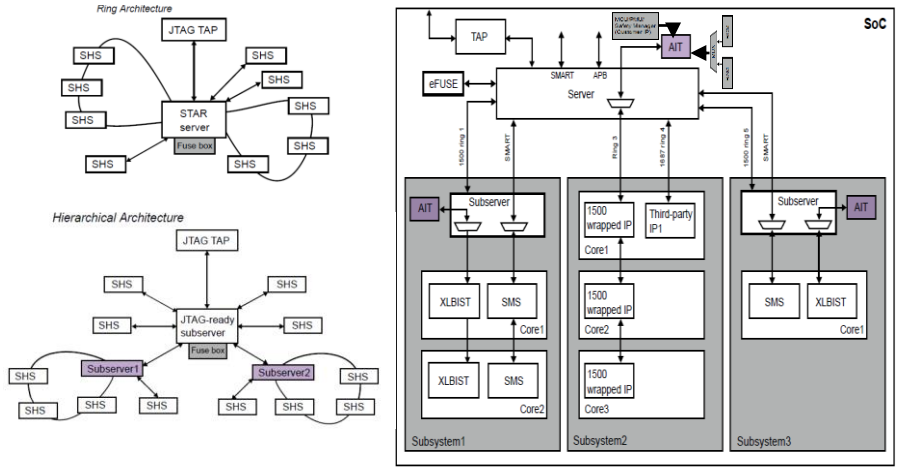


TestMAX XLBIST

In-System Test Challenges

- LBIST/MBIST in safety function scenarios decision: Power on, In system, …
- Safety target to meet : Test coverage, system test time for each safety function scenarios
- Various Test architectures and Access interface selection
  - star/ring/hierarchical, JTAG/Smart/AIT/APB
- Tradeoff between test time, test coverage and power

Various architectures and access interfaces



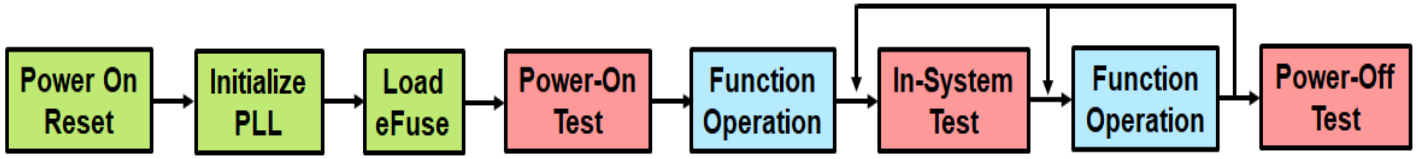
Conflict between test time, test coverage, power

Impact \ Target	Test time	Test coverage	Power (IR)
Test time		↗	↗
Test coverage	↘		↘
Power	↗	↗	

- Need a systematic method to implement system BIST

Prioritize Test Structure

➢Determine Priority (test time, test coverage, power) for each System test scenario

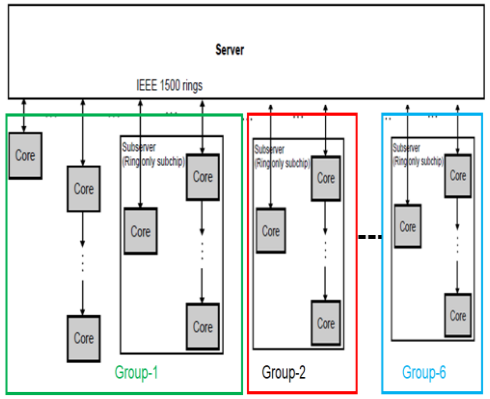


	Power-On Test	In-System Test	Power-Off Test
Test Time	Priority-1 (limited)	Priority-3	Priority-3
Test Coverage	Priority-2 (low bound)	Priority-1 (high)	Priority-1 (high)
Power Aware	Priority-2	Priority-2	Priority-2

➢Power-aware DFT plan (consider power consumption for each test scenario)

– Lower the power by grouping, serial test, limiting parallel test objects

	Power-On Test	In-System Test	Power-Off Test
MBIST	5 groups, 4 rings in each group Test in serial by each group	Under 58 BIST processor active at the same time	Under 58 BIST processor active at the same time
XLBIST	6 groups, 12 LBIST in each group Test in serial by each group	Under 12 LBIST controller active at the same time	Under 12 LBIST controller active at the same time

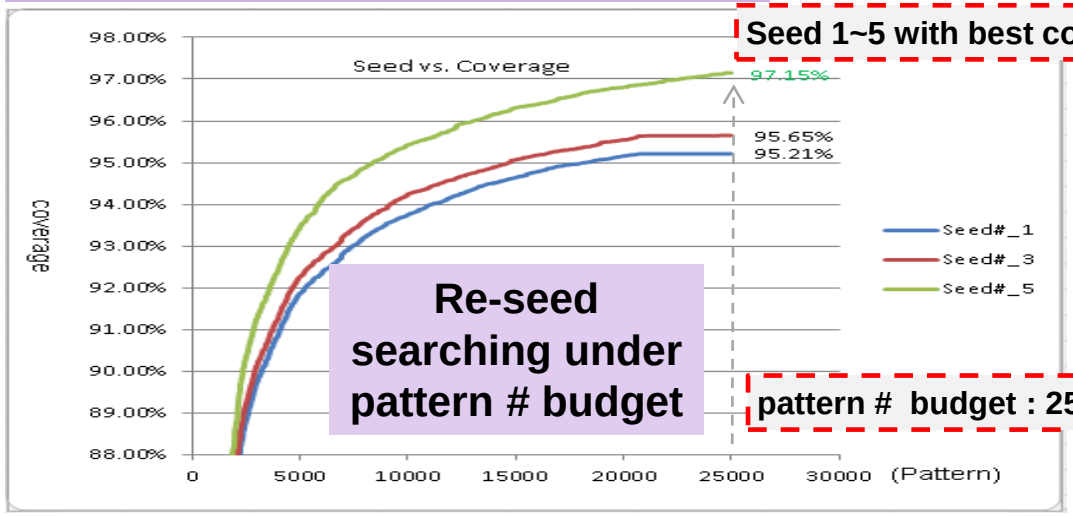


Power-On Test

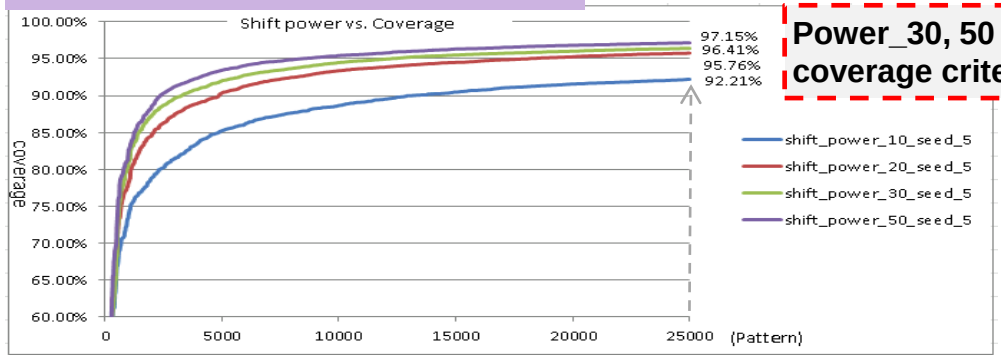
LBIST Implementation Decision for Test Time/Coverage/Power

- Priority of Power-On test scenario
  - Test time first, test coverage with low bound criteria, toggle for power consideration
- Budget for pattern number
  - Base on test time spec to define each block pattern number budget (under 25K)
- Optimization for test coverage criteria
  - By re-seed searching, determine the sufficiency seed# which meet coverage criteria
- Optimization for toggle
  - By different toggle constraint trail, determine the best toggle which meets coverage criteria

Optimization for test coverage



Optimization for toggle

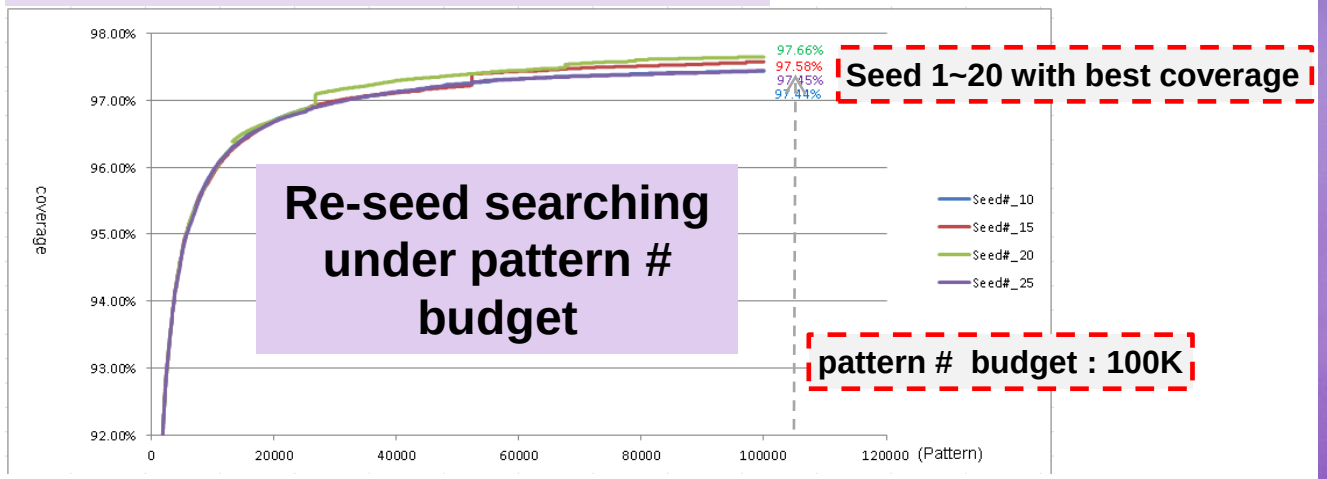


In-System, Power-Off Test

LBIST Implementation Decision for Test Time/Coverage/Power

- Priority of In-System/Power-Off test scenario
  - Test coverage first, toggle for power consideration, more test time budget
- Budget for pattern number
  - Base on test time spec to define each block pattern number budget (under 100K)
- Constraint toggle target
  - Refer Power-On test toggle result as constraint
- Optimization for test coverage criteria
  - By re-seed searching, come out the sufficiency seed# with best coverage

Optimization for test coverage



LBIST Results

- Optimization for test coverage under budgetary pattern number and toggle target
  - The toggle target is 30% for stuck-at and transition test
  - Improve test coverage by re-seed searching
    - Maximum seed numbers may not get better test coverage under budgetary pattern number

		Power-On Test			In-System, Power Off Test		
	Block	**# of Pattern**	**# of Seed**	**Coverage**	**# of Pattern**	**# of Seed**	
Stuck-at	Block-1	25k	5	96.41%	100k	20	97.66%
	Block-2	35k	10	96.92%	100k	25	97.62%
	Block-3	35k	10	93.95%	100k	20	94.90%
	…	…	…	…	…	…	…
Transition	Block-1	100k	12	86.72%	500k	25	91.98%
	Block-2	120k	15	87.53%	500k	25	91.85%
	Block-3	120k	15	84.19%	500k	25	91.40%
	…	…	…	…	…	…	…

Agenda

Synopsys IP Enables High End ASIC

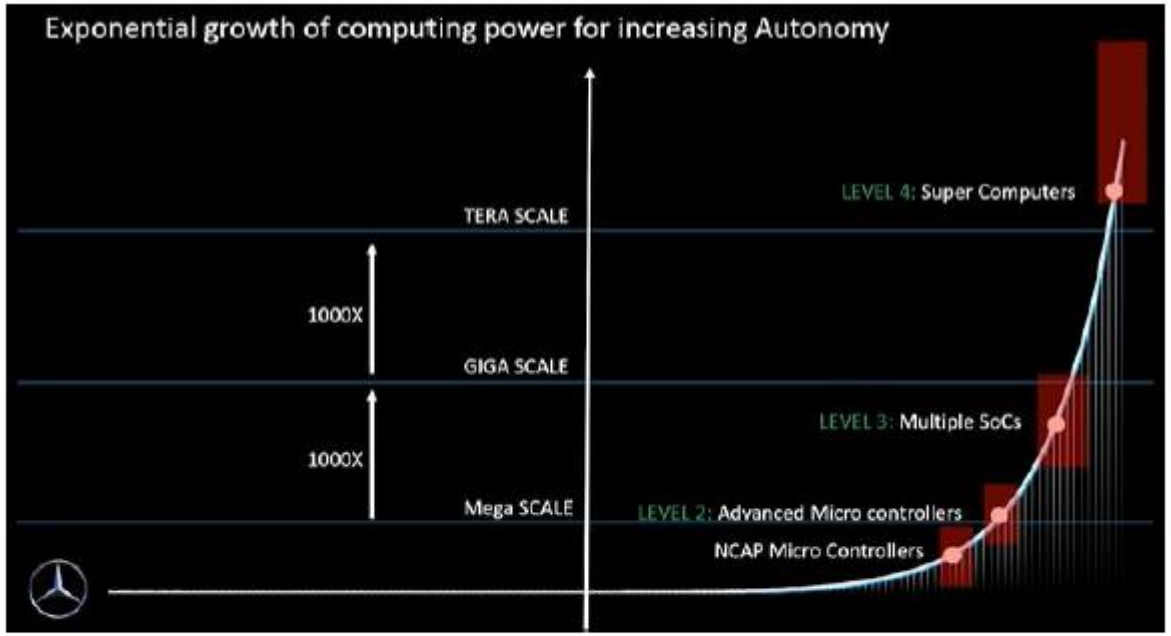
Success Stories of Automotive ASIC Collaboration

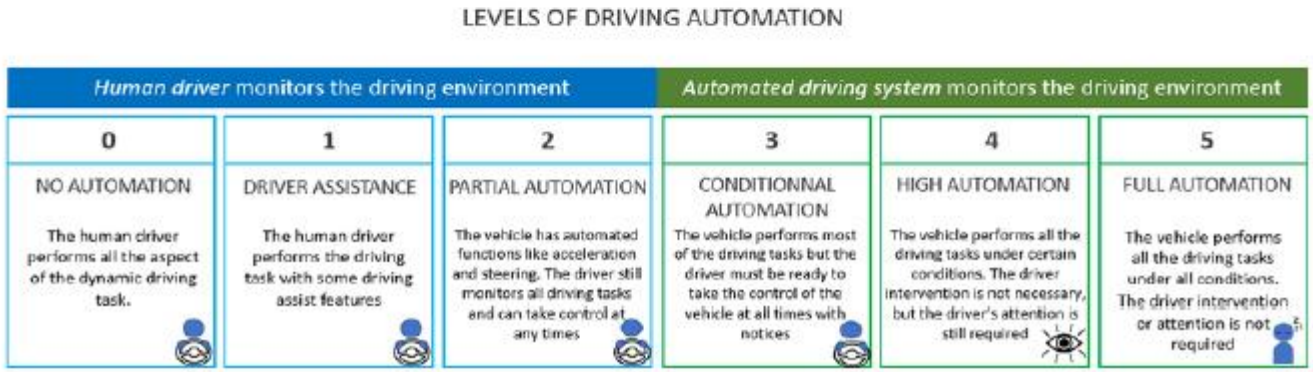
Test Requirements for Automotive IC

Trends in Automotive Semiconductors

Chiplets for Automotive Semiconductor

- Industry is moving to ADAS level 3 and 4
  - High performance computing required
  - High memory bandwidth required
  - Large die area (cost and yield)
  - High power consumption
  - Scalability and flexibility
- Automotive Semiconductor are following HPC trends of embracing chiplets and HBM for PPA
  - Die partition for optimal chip size/yield and system scalability/flexibility
  - UCIe standard for chiplet interoperability
  - HBM for high memory bandwidth requirement
  - Advanced packaging (CoWoS) for minimum link power consumption





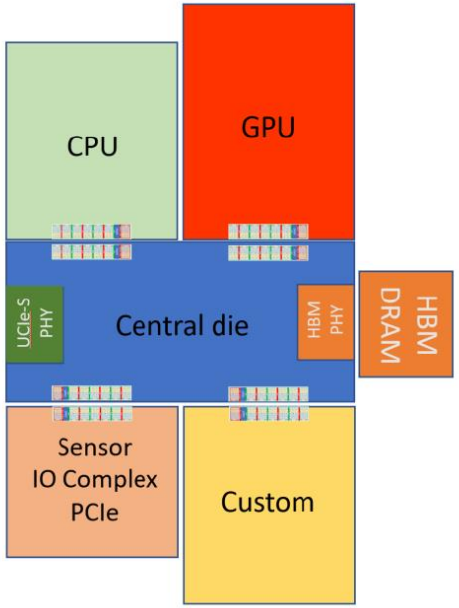
Explosion of compute Requirements for ADAS computers

Source: IEEE Hot Interconnect 2023

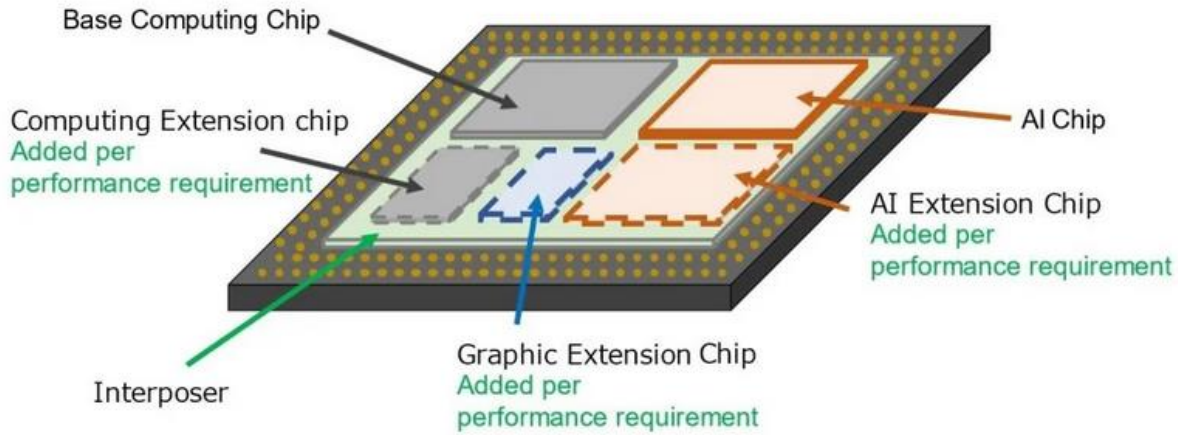
Chiplet for Automotive Semiconductor

- European Automakers are planning ADAS chiplet platforms, including center communication chiplet, CPU, ML accelerator, and HBM3

- Japanese Automakers have formed semiconductor research group ASRA (Advanced SoC Research for Automotive) to provide cutting-edge technologies to next generation vehicles including combining different semiconductor types in the SoC design, to achieve advanced computing power with safety and reliability.



ADAS Chiplet Configuration



Source: IEEE Hot Interconnect 2023

GUC Advanced Package Technology (APT)

CoWoS-S Flow
- Interposer design 7.2G
- eDTC insertion
- 3D stack PV & Multi-die IR

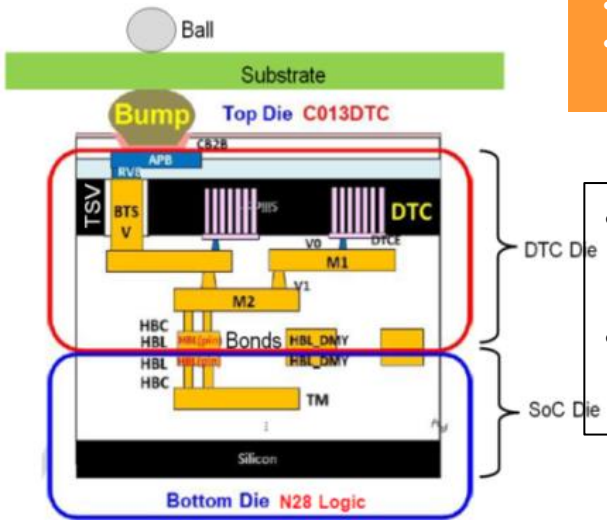
CoWoS-R Flow
- 3D stack PV
- Multi-die IR

SoIC-WoW Flow
- Hybrid-bump Planning
- Cross-die STA signoff
- Multi-die IR & 3D stack PV
- Thermal analysis

CoWoS-L Flow
- Local Silicon Interconnect
- eDTC insertion
- 3D stack PV & Multi-die IR

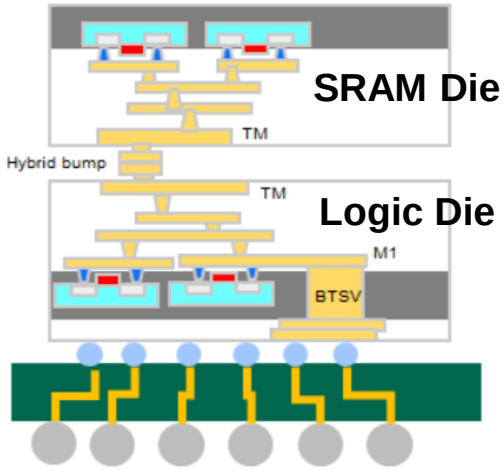
2021 | 2022 | 2023 | 2024

SoIC-WoW w/ DTC TPO
- TK1 pilot
- Bottom Die: N28 SoC
  Top Die: CL013 DTC



- IR drop 20% → 14.7% for multi-core ramp-up
- Improve Vmin 20mV in ACSCAN ATE test

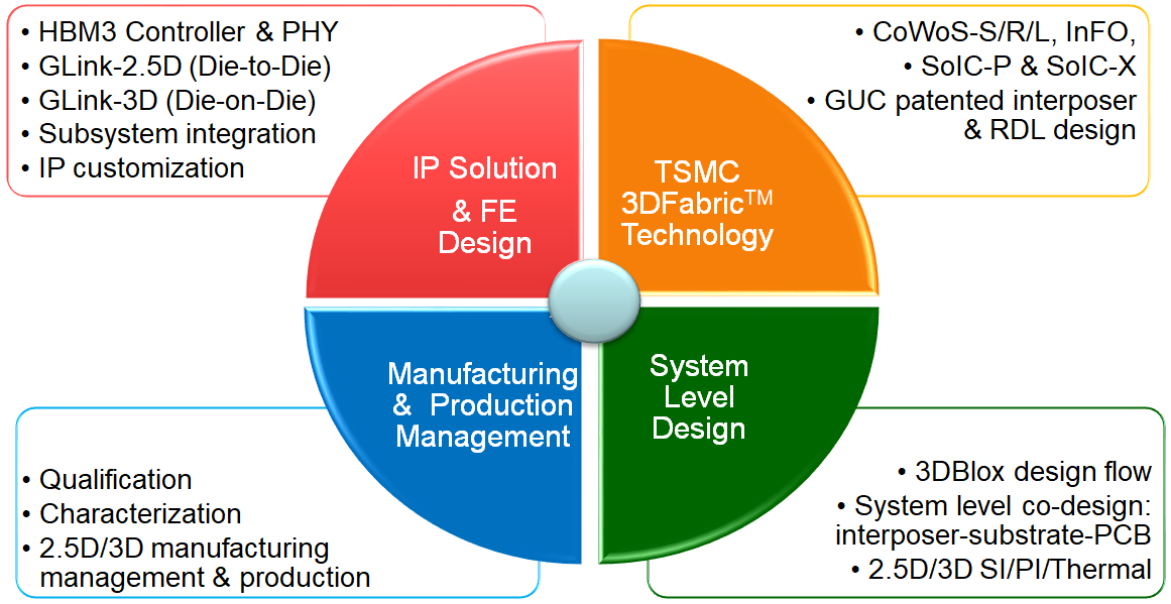
SoIC-WoW TPO
- TK1 pilot
- Bottom Die: N7 SoC
  Top Die: N7 Cache Memory



- 3D hierarchical low power design
- CTS plan for cross-die OCV reduction, MMMC-STA critical corner analysis
- PG TSV #/pitch plan, BTSV array macro design

Summary

- Synopsys provides a wide portfolio of high quality IP's to enable the design of high end SoC's for AI, HPC, Networking, and ADAS applications.
- GUC services include IP, FE design, System level design, SoC testing and production, using TSMC's advanced process and packaging technologies.
- 2.5D/3D chiplet is a trend for ADAS level 3 and above. GUC partners with Synopsys to provide customers with high performance, reliable SoC's.




THANK YOU
Our Technology, Your Innovation™