Unlimited Possibility of AI: Automatic and Flexible Floorplan Shrinking Methodology by DSO.ai

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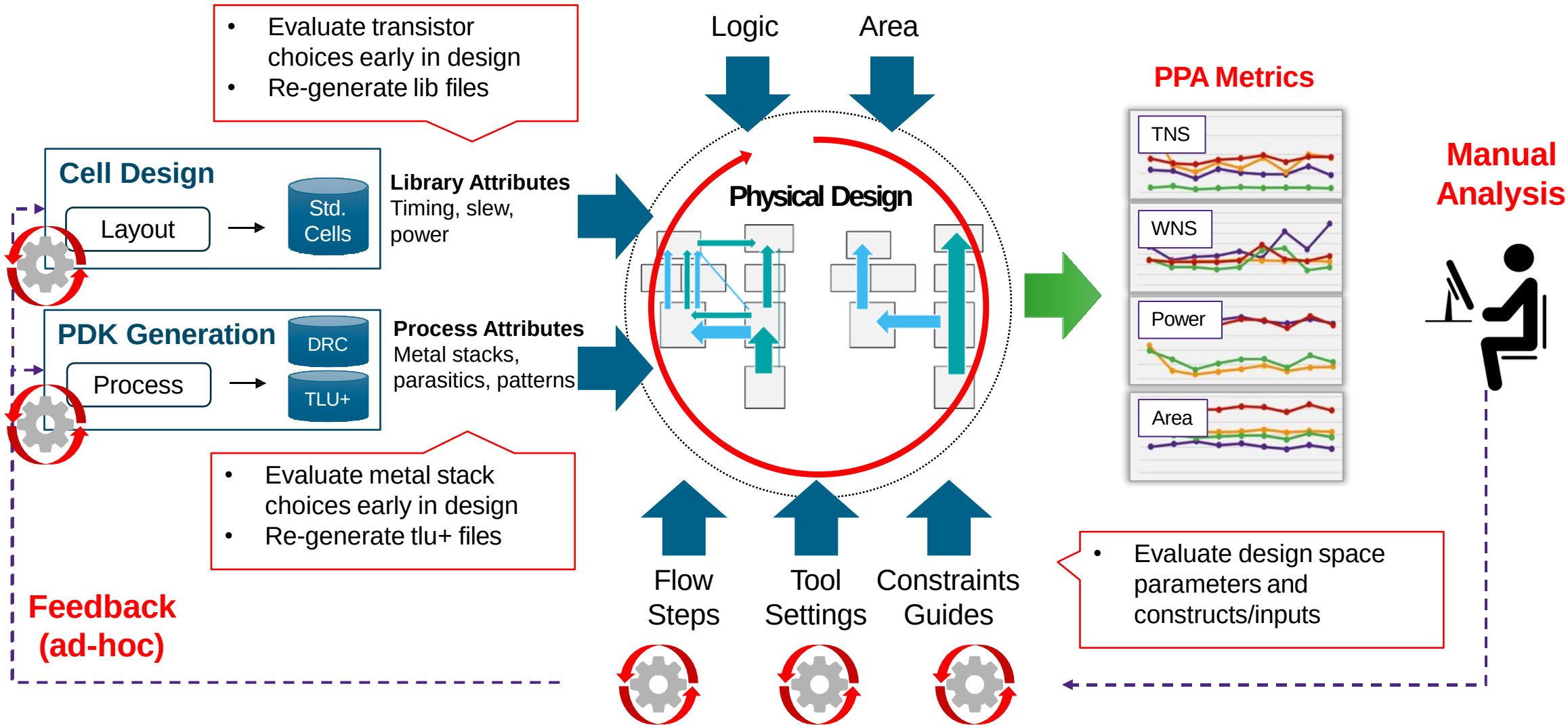
Agenda

- DSO.ai overview
- DSO.ai Floorplan Reduction and Macro Location Exploration Overview
- Experimental results
- Summary and Recommendations

DSO.ai Overview

AI Driven Design Space Optimization (DSO)

Addressing Broader Design-Technology Space



Design Space Optimization Loop

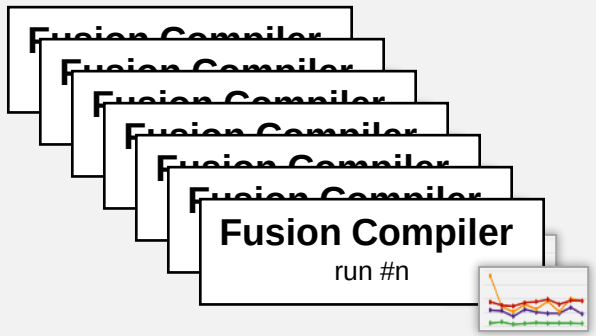
User provides

Parameters:
Search space (tool or design settings, etc.)

Objectives:
List of metrics to improve

Baseline Flow:
Scripts to be run in FC/ICCII/…

DSO.ai

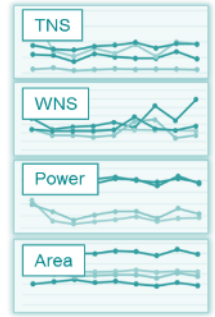


Run your design, flow, settings, scripts, reports,…

Record Results at the end of each FC run

User specify the compute envelope (cpu, memory)

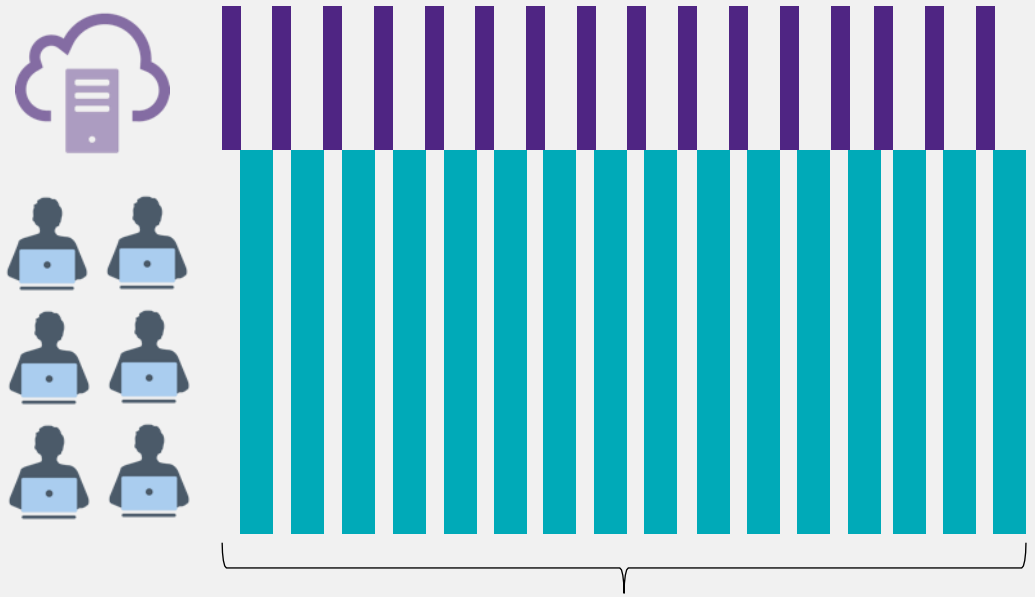
Training DB containing all results



Individual NDM databases

Meet Targets Faster, with Less Effort

Traditional: Manual Sweeps

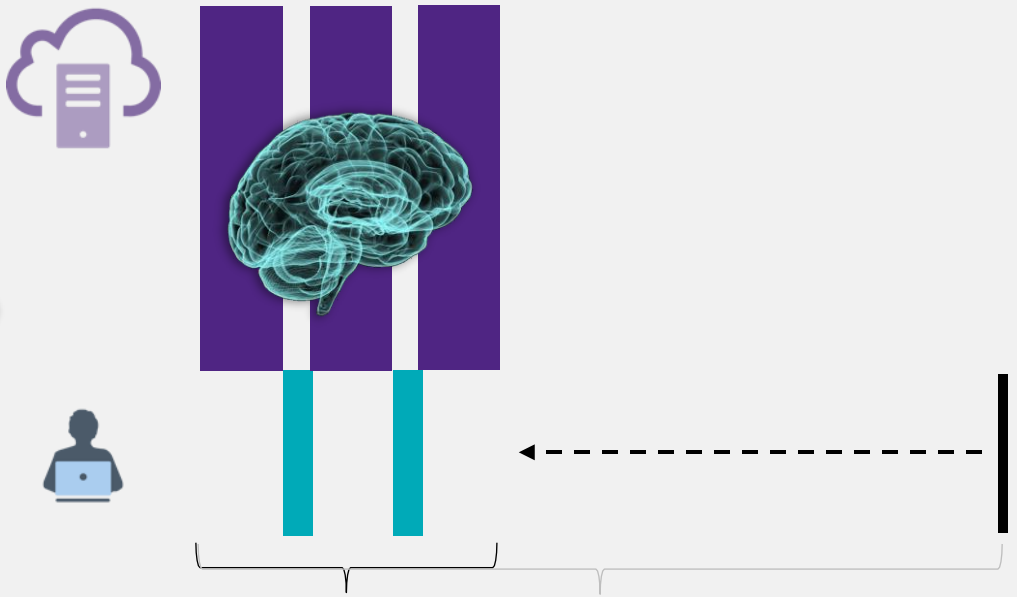


SEVERAL ENGINEERS

ACHIEVED TARGET PPA

PPA Push Time to Results on an SOC block. Does not include time for manual ECOs or data cleanup of early data drops

DSO.ai: Autonomous Search



1 ENGINEER

ACHIEVED TARGET PPA

Time to comparable PPA results on the same SOC block using DSO.ai

DSO.ai Floorplan Reduction and Macro Location Exploration Overview

Motivation

- **Why to explore floorplan reduction and macro location?**
  - Smaller die area affects the cost directly. Cost is the most annoying thing to let us wake up at midnight.

- **Why to explore floorplan reduction and macro location by DSO.ai?**
  - Traditionally, senior physical designers spend months exploring minimum floorplan and macro locations.
  - Now, with DSO.ai, designers can explore this huge design space efficiently, quickly, and automatically.

What Does DSO.ai Floorplan Toolbox Offer? – 1/4

- DSO.ai floorplan toolbox provides a set of **default** permutons and metrics to quickly explore floorplan reduction and macro location.
- Floorplan toolbox permutons are divided into three categories:
  - Floorplan sizing related permutons
  - Macro exploration related permutons
  - Congestion reduction permutons
- Floorplan toolbox metrics are divided into four categories:
  - Floorplan area gain
  - Timing
  - Congestion
  - Cell/pin density hot spot count

What Does DSO.ai Floorplan Toolbox Offer? – 2/4

Floorplan sizing related permutons

- **What do floorplan sizing related permutons offer?**
  - DSO.ai allows to use floorplan DEF as input to shrink floorplan
  - DSO.ai handles site row, wire track and port location automatically on shrinking floorplan
  - DSO.ai supports both rectangle and rectilinear floorplan shrinking
  - DSO.ai supports 5 different floorplan shrinking styles. We will show more detail in later page.

What Does DSO.ai Floorplan Toolbox Offer? – 3/4

DSO.ai floorplan shrinking styles

- **DSO.ai allows to alter floorplan by different styles:**

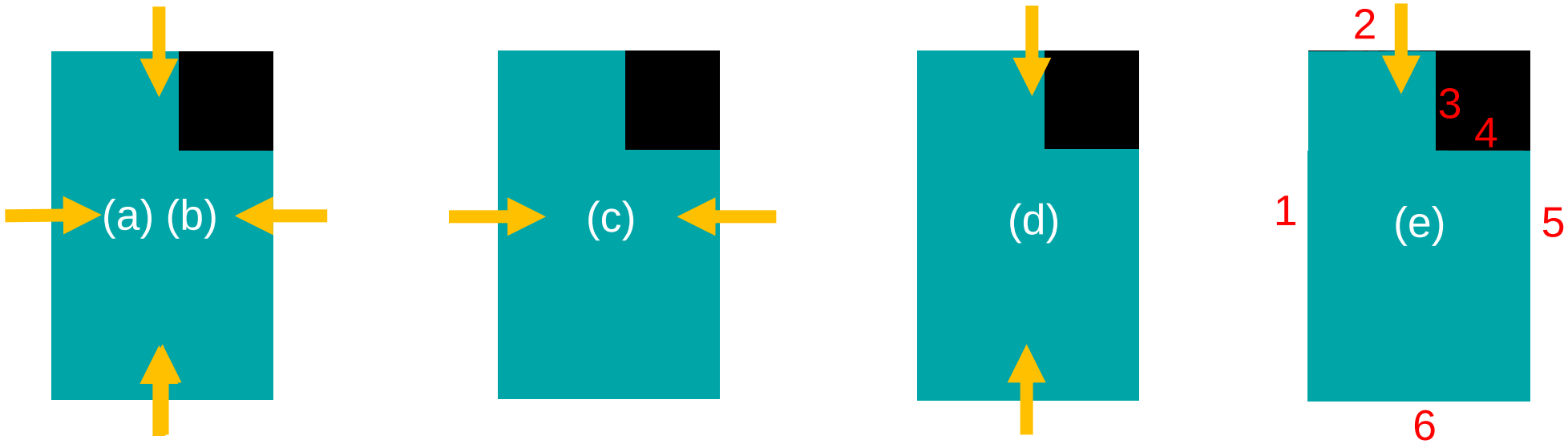
  (a). Scale area: shrink floorplan by scaling area but keep same aspect ratio as original floorplan

  (b). Scale height and width: shrink floorplan by scaling both height and width

  (c). Scale width only: shrink floorplan by scaling width only

  (d). Scale height only: shrink floorplan by scaling height only

  (e). Scale specific side: shrink floorplan by scaling specific sides, e.g., only shrink side 2



What Does DSO.ai Floorplan Toolbox Offer? – 4/4

Congestion reduction permutons

- **Why do we need congestion reduction permutons?**
  - Because the most critical thing after floorplan shrinking is how to keep or even improve routablility compared to baseline, DSO team introduced new congestion reduction permutons to mitigate congestion further.
  - Congestion reduction permutons can be used on non-shrinking congested design as well.

- **What does congestion reduction permutons offer?**
  - DSO.ai provides congestion reduction solutions for standard cell area and macro area, e.g.:
    - Auto congestion hotspot analysis and reduction
    - Auto pin density hotspot reduction

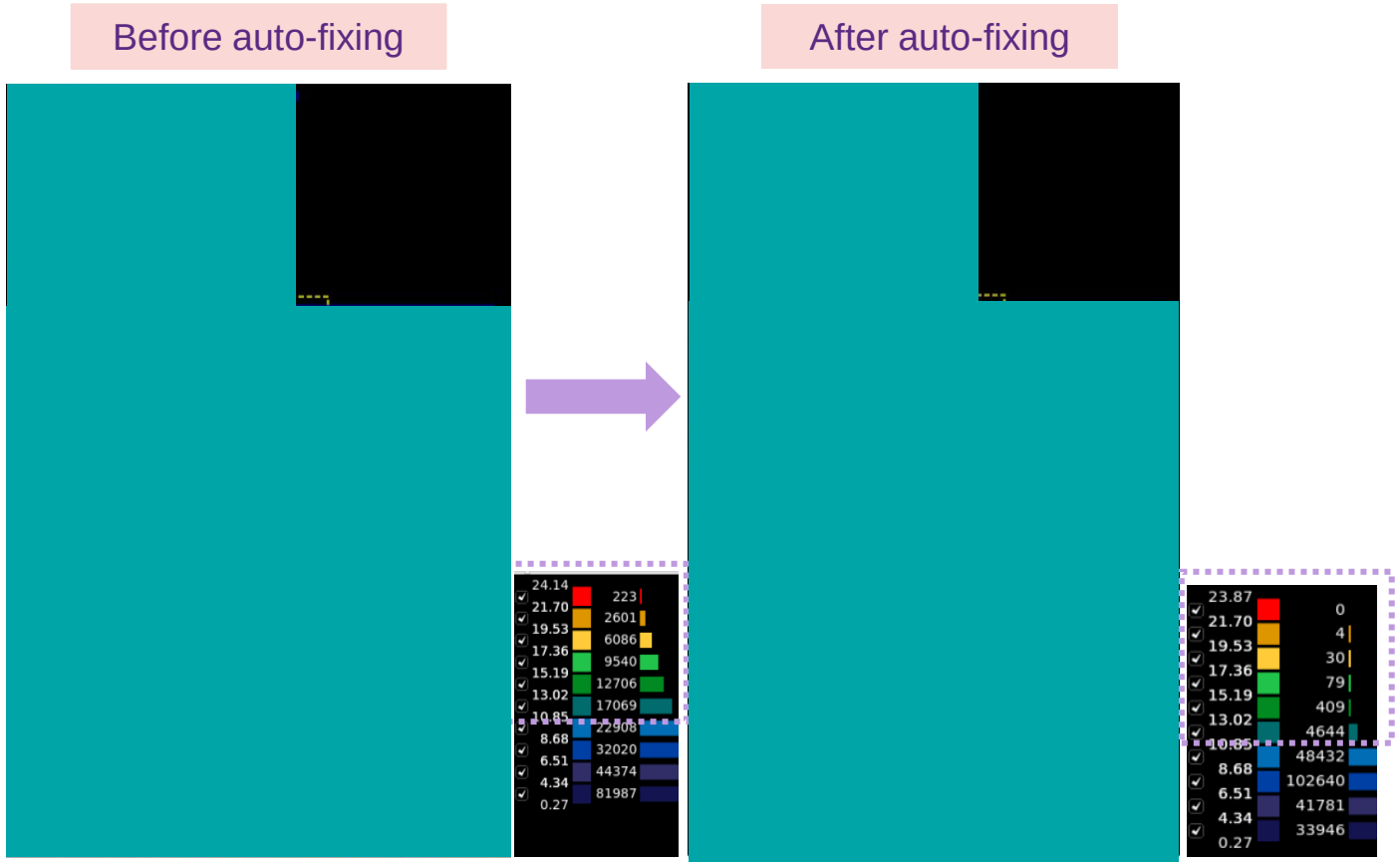
Auto Congestion Hotspot Analysis and Reduction by DSO.ai

Before auto-fixing
GRC : 2.44%

After auto-fixing
GRC : 2.17%

- Routing convergence becomes very challenging after shrinking floorplan even though user applies high effort congestion.
- DSO.ai has capability to automatically identify congestion hotspot area and then spread cells to reduce congestion further which might be took by user before.
- Runtime increment is expected

Auto Pin Density Hotspot Reduction by DSO.ai



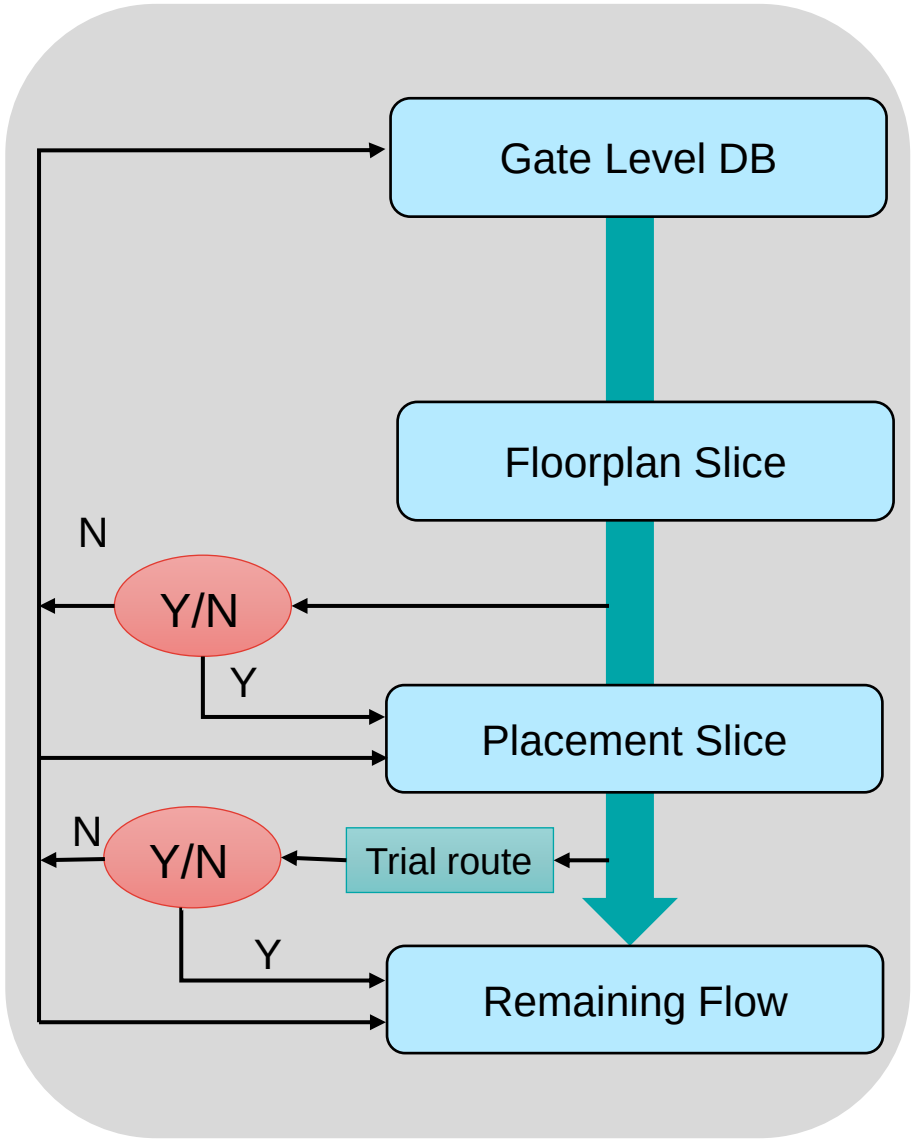
- Routing convergence becomes very challenging after shrinking floorplan even though user applies high effort congestion.
- DSO.ai provides different strategies to automatically fix congestion further due to high pin density hotspots which might also be took by user before.
- No runtime penalty

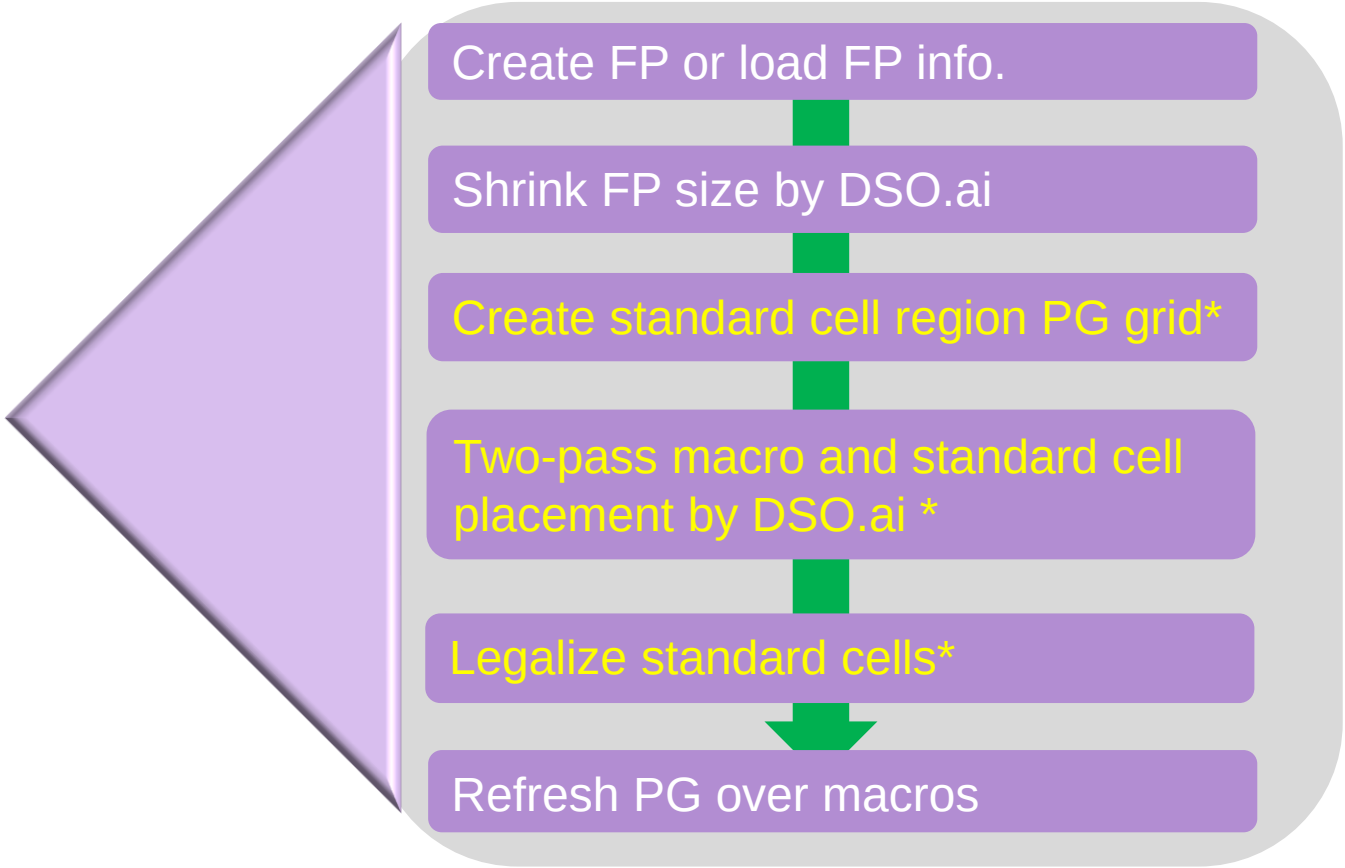
Prerequisites for Floorplan Reduction and Macro Location Exploration

- **What should you have before exploring floorplan reduction and macro location?**
  - FC/ICC2 floorplan and placement scripts which successfully run on the design
  - Power network synthesis script, to be inserted for accurate congestion analysis during the runs
  - Queue system to submit 30 jobs

- **What should you decide before exploring floorplan reduction and macro location?**
  - Floorplan shrinking style

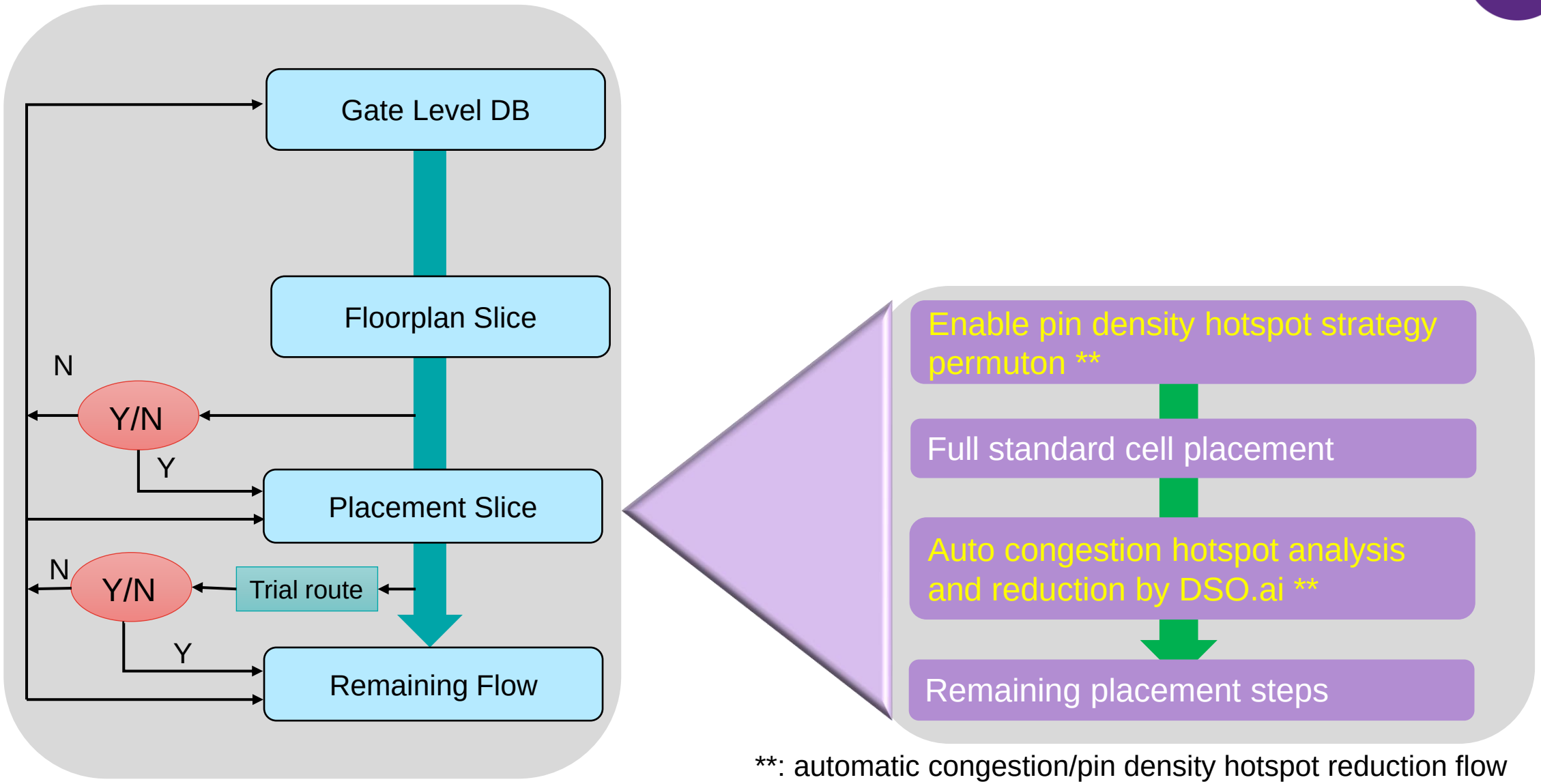
Floorplan Reduction and Macro Location Exploration Flow – 1/2





*: to have more precise congestion estimation

Floorplan Reduction and Macro Location Exploration Flow – 2/2



**: automatic congestion/pin density hotspot reduction flow

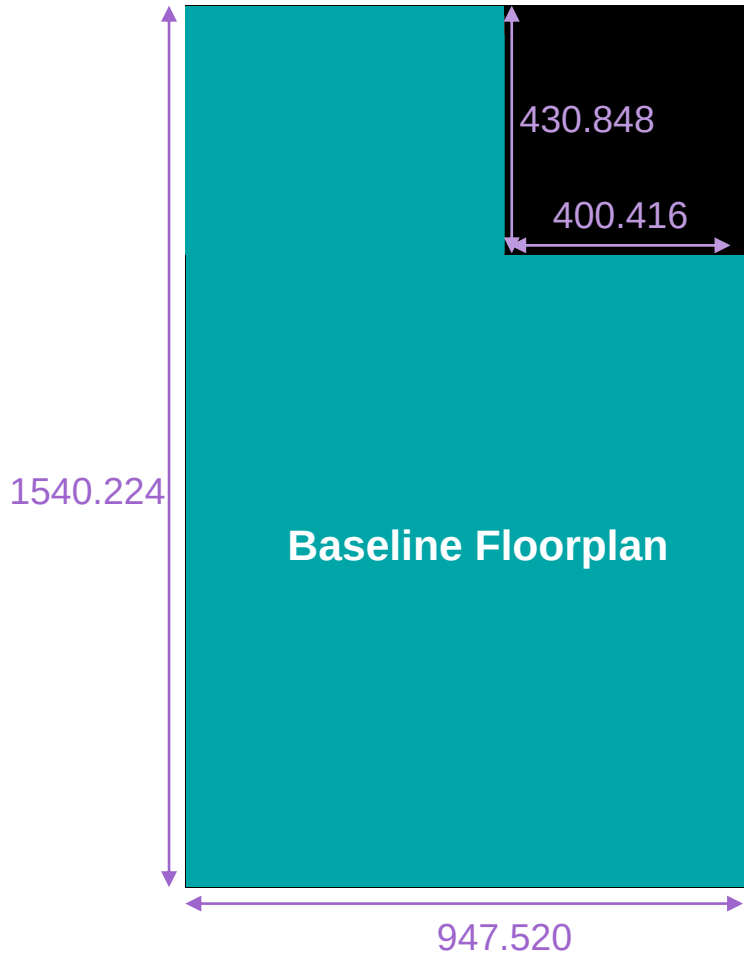
Experimental Results

Case Study 1: Scale Area

Objective and challenge of floorplan shrinking

- **Objective:**
  - Auto floorplan shrinking and macro location exploration by DSO.ai
- **Challenge:**
  - Routing can’t be easily converged even though with high effort congestion options. User must undergo some iterations of floorplan flow tuning to converge timing and routing.
  - There was a machine crunch. Only 3-4 machines (12-14 jobs) were used for this evaluation”.

Design Details	
Tech Library	TSMC 12nm
Cell Count	1.6M
Macro Count	194
DSO/ICC2 Version	V-2023.12/T-2022.03-SP3



Auto Congestion Hotspot Analysis and Reduction by DSO.ai

PPA Summary (3% Floorplan Reduction)

Baseline floorplan

	R2R Setup Time (ns)			R2R hold Time (ns)			GRC/DRC (Short)	Die Area (um^2)	U-Rate (%)	Total Power (mW)
	WNS	TNS	NVP	WNS	TNS	NVP				
route_opt	-0.072	-4.914	964	-0.016	-0.454	363	1269(326)	1286874	71.87	59.39

DSO floorplan - without auto-congestion hotspot analysis and reduction

	R2R Setup Time (ns)			R2R hold Time (ns)			GRC/DRC (Short)	Die Area (um^2)	U-Rate (%)	Total Power (mW)
	WNS	TNS	NVP	WNS	TNS	NVP				
route_opt							Un-routable			

DSO floorplan - with auto-congestion hotspot analysis and reduction

	R2R Setup Time (ns)			R2R hold Time (ns)			GRC/DRC (Short)	Die Area (um^2)	U-Rate (%)	Total Power (mW)
	WNS	TNS	NVP	WNS	TNS	NVP				
route_opt	-0.118	-11.212	1021	-0.021	-0.548	536	1768(157)	1248353	75.19	58.94

- We shrank floorplan 3% first but was not routable. Short hot spots were very correlated to pre-route congestion hot spots.
- DSO.ai BU introduced new toolbox to analyze and mitigate congestion hotspot at place slice automatically.
- 3% floorplan reduction became routable with new congestion reduction permutons.

Auto Pin Density Hotspot Reduction by DSO.ai

PPA Summary (5% Floorplan Reduction)

Baseline floorplan

	R2R Setup Time (ns)			R2R hold Time (ns)			GRC/DRC (Short)	Die Area (um^2)	U-Rate (%)	Total Power (mW)
	WNS	TNS	NVP	WNS	TNS	NVP				
route_opt	-0.072	-4.914	964	-0.016	-0.454	363	1269(326)	1286874	71.87	59.39

DSO floorplan - without auto pin density hotspot reduction

	R2R Setup Time (ns)			R2R hold Time (ns)			GRC/DRC (Short)	Die Area (um^2)	U-Rate (%)	Total Power (mW)
	WNS	TNS	NVP	WNS	TNS	NVP				
route_opt	-0.121	-16.009	2229	-0.014	-0.389	392	24816(2332)	1222679	77.02	59.14

DSO floorplan - with auto pin density hotspot reduction

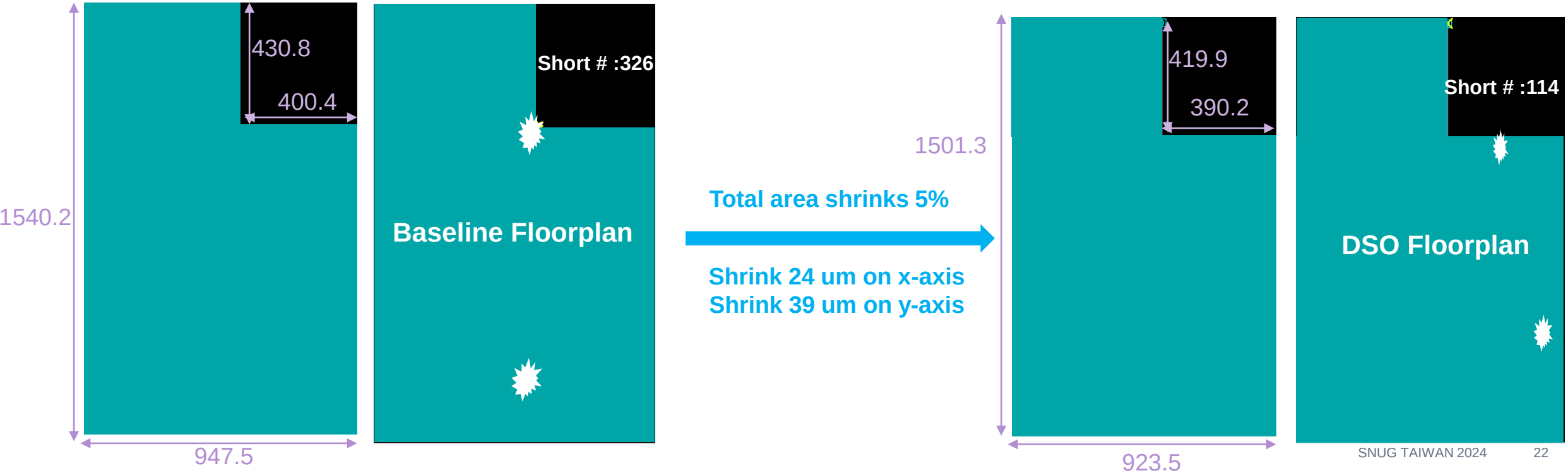
	R2R Setup Time (ns)			R2R hold Time (ns)			GRC/DRC (Short)	Die Area (um^2)	U-Rate (%)	Total Power (mW)
	WNS	TNS	NVP	WNS	TNS	NVP				
route_opt	-0.079	-15.932	1724	-0.058	-1.928	528	988(114)	1222679	77.80	59.95

- We shrank floorplan 5% afterwards but was not routable again. Short hot spots were very correlated to pin density hotspots.
- DSO.ai BU introduced new toolbox to reduce pin density hotspot at place slice automatically.
- 5% floorplan reduction became routable with new pin density reduction permuton.

Case Study 1: Scale Area

Summary (5% Floorplan Reduction)

- DSO.ai helps user to explore minimum floorplan and macro placement more quickly and with less effort. Floorplan width was reduced 24 um and height was reduced 39 um, respectively.
- DSO.ai achieved 5% floorplan reduction with better routability as well as comparable QoR on timing and power. Timing jump is easily recoverable.
- DSO.ai also pushed u-rate from 71.87% to 77.80% with less routing DRC and short. Serious short hot spot was mitigated, and short number reduces from 326 to 114.



Case Study 2: Shrink Specific Direction

Design overview and challenges of floorplan shrinking

- Design Overview

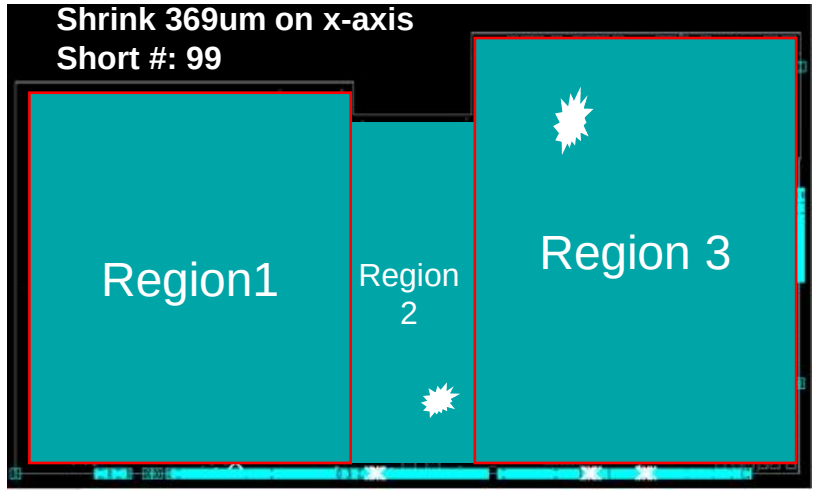
Design Details	
Tech Library	TSMC 22nm
Cell Count	2.4M
Macro Count	330
Height/Width (um)	1518 / 3072
DSO/ICC2 Version	V-2023.12/U-2022.12-SP5

- Challenges
  - A block from previous tape-out project
  - Multi-dimension irregular shape block
  - Only allow to shrink horizontal side
  - Target area reduction > 10%
  - Proven its routability until route_opt and the timing and power should be maintained

Case Study 2: Shrink Specific Direction

Scale all horizontal sides (FP1)

- Best floorplan shrinking result by DSO
  - DSO.ai helps to generate a 12% shrinking floorplan automatically and proven its routability in the end
  - Initial utilization of shrinking floorplan increased from 65.45% to 71.16%
  - Besides met over 10% area target, DSO also maintained similar timing and power compared to baseline



	QoR	Baseline	DSO Shrink 12 % (FP1)
Route_opt	Height / Width (um)	1518 / 3072	1518 / 2703
	WNS / TNS / NVP (R2R)	-0.275 / -4.8 / 934	-0.339 / -17.4 / 1233
	HWNS / HTNS / HNVP (R2R)	-0.255 / -28.5 / 1764	-0.220 / -84.1 / 3669
	Total Power (mW)	-	+0.54%
	DRC (Short)	622 (65)	440 (99)

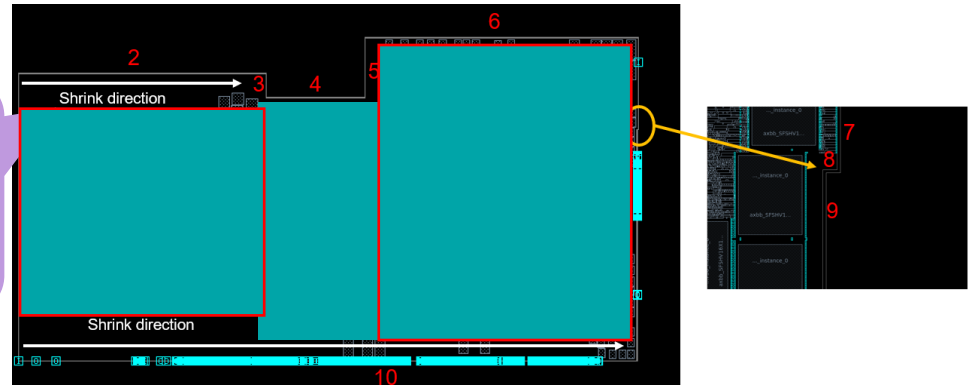
- Can DSO do better?

Case Study 2: Shrink Specific Direction

Scale specific horizontal sides only (FP2)

- How DSO exceed itself
  - DSO has the capability to shrink specific sides base on user's constraint.
  - By shrinking the side #2 & #10, the DRC(short), timing and power QoR are all better than baseline and FP1. Horizontal width reduced more to 2689um better than FP1 as well.

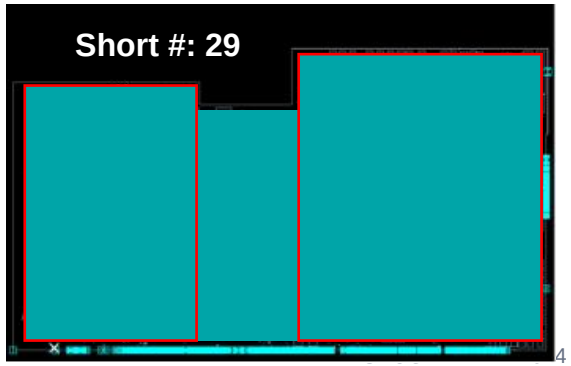
User could shrink the specific sides w/ the new toolbox



Area shrinks 12%

Shrink 383 um on x-axis

	QoR	Baseline	DSO Shrink 12 % (FP1)	DSO Shrink 12 % (FP2)
Route_opt	Height / Width (um)	1518 / 3072	1518 / 2703	1518 / 2689
	WNS/TNS/NVP (R2R)	-0.275/-4.8/934	-0.339/-17.4/1233	-0.09/-3.7/947
	HWNS/HTNS/HNVP (R2R)	-0.255/-28.5/1764	-0.22/-84.1/3669	-0.153/-18.8/ 1407
	Total Power (mW)	-	+0.54%	-3.88%
	DRC (Short)	622 (65)	440 (99)	527 (29)
	Rumtime (hrs)	25.78	22.45	22.54



Summary and Recommendations

Summary and Recommendations

Summary

- DSO.ai floorplan toolbox provides a set of default permutons and metrics to help user explore minimum floorplan and macro location more quickly and with less effort. TAT will be reduced from months to weeks.
- DSO.ai allows to use floorplan DEF as input to shrink floorplan
- DSO.ai supports both rectangle and rectilinear floorplan shrinking
- DSO.ai supports five different shrinking styles
- DSO.ai floorplan toolbox also provides congestion reduction permutons to mitigate congestion further which can be used on non-shrinking congested design as well.

Recommendations

- Enhance to handle designs with complex voltage area and bound shapes
- Enhance to find good result with less machine resources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