UPF Based Hybrid Emulation

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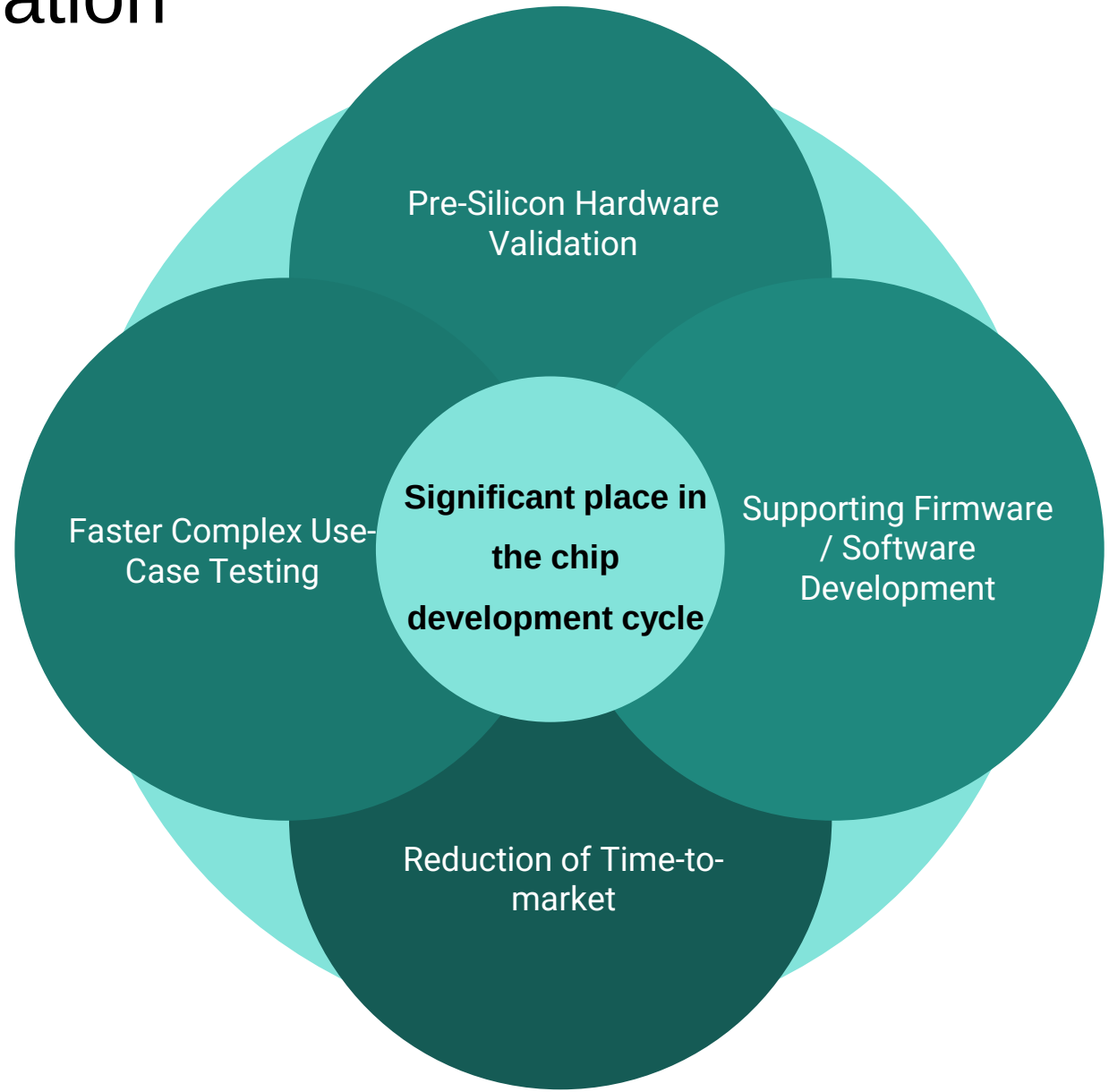
Presentation Content

- Role of Emulation
  - Full SoC Emulation
  - IP Hybrid Emulation
- UPF Based Emulation
  - Enablement Process / Challenges
  - Advantages
- UPF Based Hybrid Emulation
  - Advantages Over Pure Model
  - Tested Scenarios

Role of Emulation

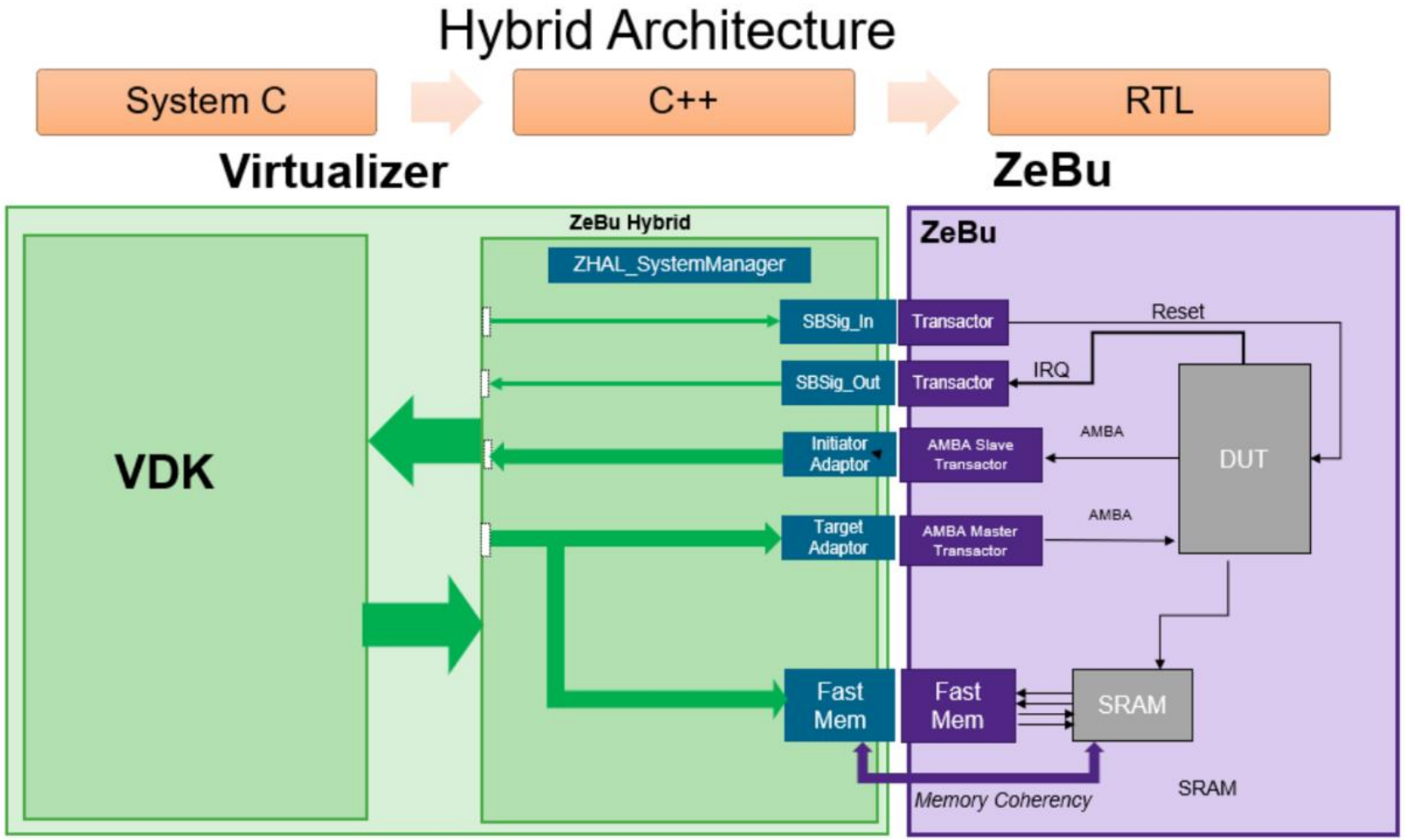
- Full SoC Emulation
- IP Hybrid Emulation

Role of Emulation



Role of Emulation

IP Hybrid Emulation



Role of Emulation

Full SoC vs IP Hybrid Emulation

Pure SoC Emulation	IP Hybrid Emulation
Full design directly mapped onto emulator hardware	IP / Subsystem mapped onto emulator hardware with a virtualized CPU
Model bringup happens at a later stage when RTL is more mature	Model bringup happens much early in the cycle
Larger model design size	Smaller model design size
Inherent timing accuracy between all components of the mode	Complex to maintain timing accuracy between emulated and virtual components
System level scenarios validated	Subsystem / IP level focus of validation
Thorough hardware verification	Early firmware / software development
Model’s clock frequency is slower	Model’s clock frequency is faster

UPF Based Emulation

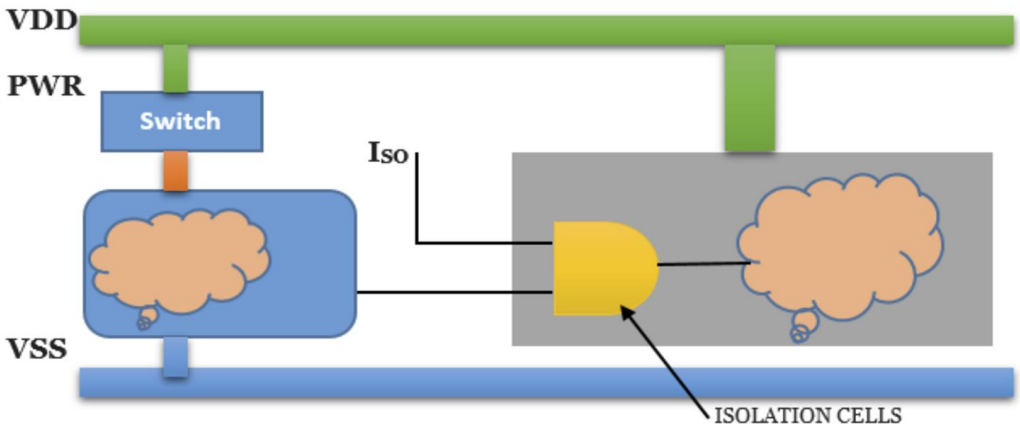
- Enablement Process / Challenges
- Advantages

UPF Based Emulation

Power is critical for most modern-day SoCs and UPF-based testing in emulation provides several advantages and a near-silicon readiness

Enablement Process / Challenges

- Emulates the power switches, isolation and retention cells
- Need to parse the UPF file as input during compile
- Requires aligning with design UPF for even the modeled components
- Dummy RTL hierarchies need to be introduced for the stubbed out components (mostly for AMS components)



UPF Based Emulation

Advantages

- Power-aware verification
  - Verifying and debugging power intent
  - Validate functionality of power modes and scenarios involving power switches, isolation and retention cells
  - Scrambling and corruption options available while testing
  - Accelerate power related issue identification and resolution
- Early power analysis
- Dynamic Frequency Scaling (DFS) verification
- Software/Hardware Power Co-verification
  - Allows for more power optimised firmware

UPF Based Hybrid Emulation

- Advantages Over Pure Model
- Tested Scenarios

UPF Based Hybrid Emulation

Advantages Over Pure Model

- Targeted power aware emulation
- Early identification of power-related issues
  - UPF is often enabled for the entire SoC at a more mature design phase where the benefits are not always fully leveraged
- Targeted power analysis or complex resource-intensive vectors and use cases for a given subsystem or IP

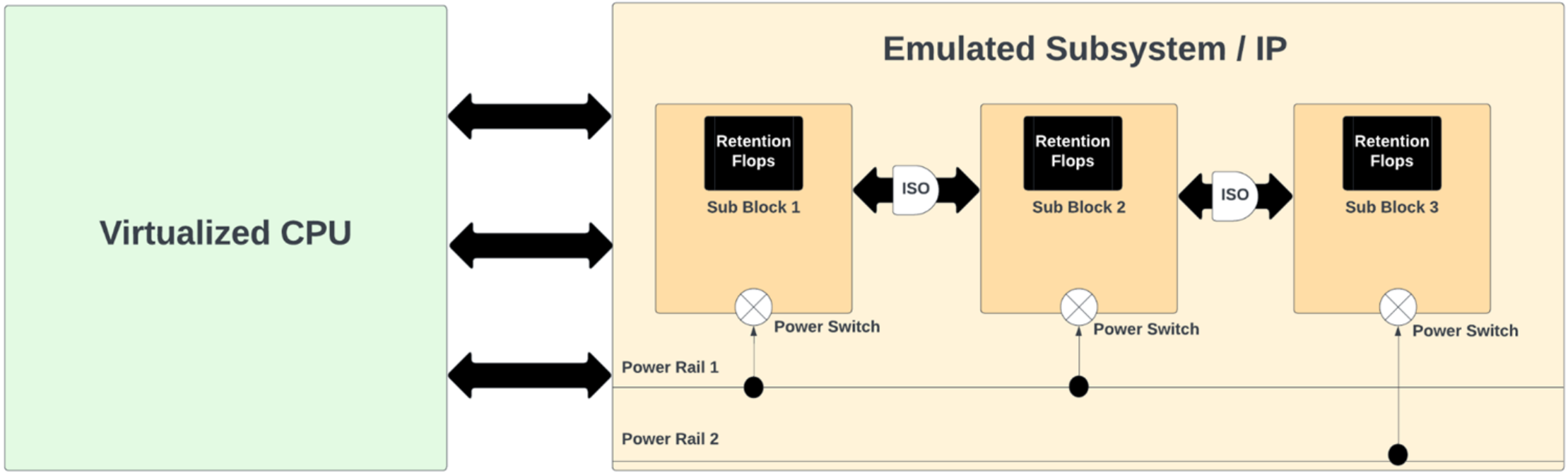
Points to keep in mind

- For any performance or power analysis, it is important to have the traffic contained within the subsystem or IP with minimal or no interaction with the virtual component.
- For a subsystem level hybrid emulation with different UPF for each submodule, a top level UPF files needs to be developed.

UPF Based Hybrid Emulation

Tested Scenarios and Issues Caught

- Functionality for power switches, retention and isolation cells
- Issues related to power down sequences caught

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