Accelerated Serial DFT SOC Scan Validation using ZeBu Emulator

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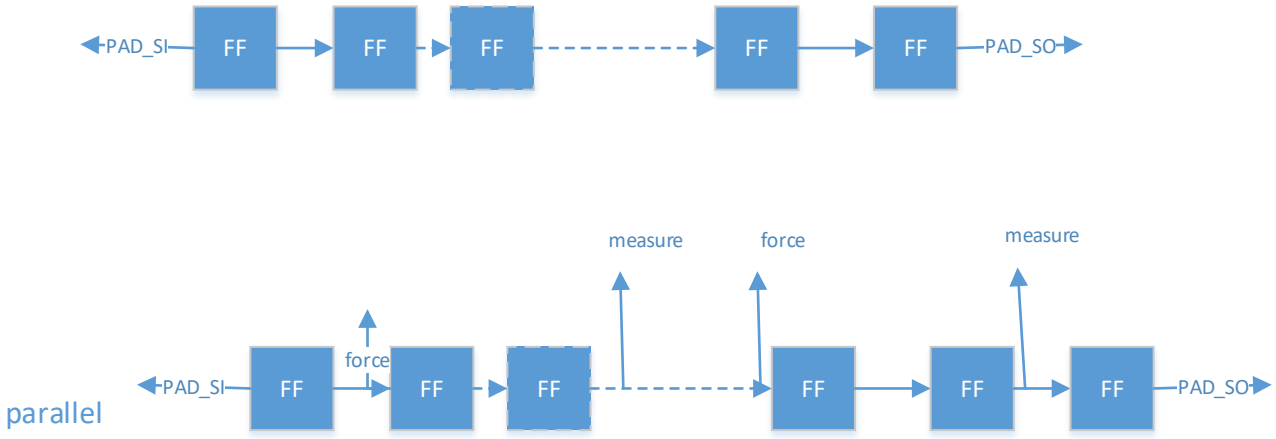
AGENDA

- Problem Statement
- Proposed work and methodology
- Results
- Scope for Improvement
- Conclusion

Problem Statement

Problem Statement

- SOC Scan Serial simulation for all the patterns can not be done due to the huge simulation run times and huge compute resources requirement.
- The full set Scan Serial simulation can be performed using the Zebu emulator.
- The SOCs of size 69M and 60M gates have been verified on zebu within hours.



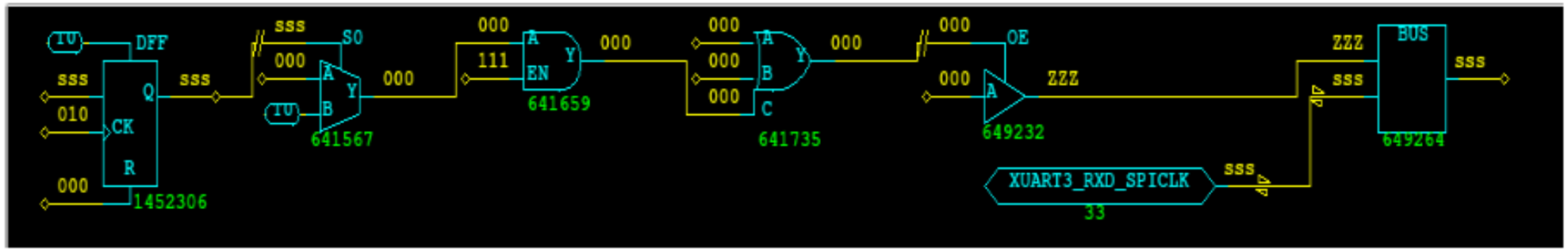
CASE STUDY

Case study

We have run the playback simulations for TD 200 patterns.
After Post silicon it was failing on 232 pattern

OE controllability issue on SCAN IN pad

PASS Case:



Proposed work and methodology

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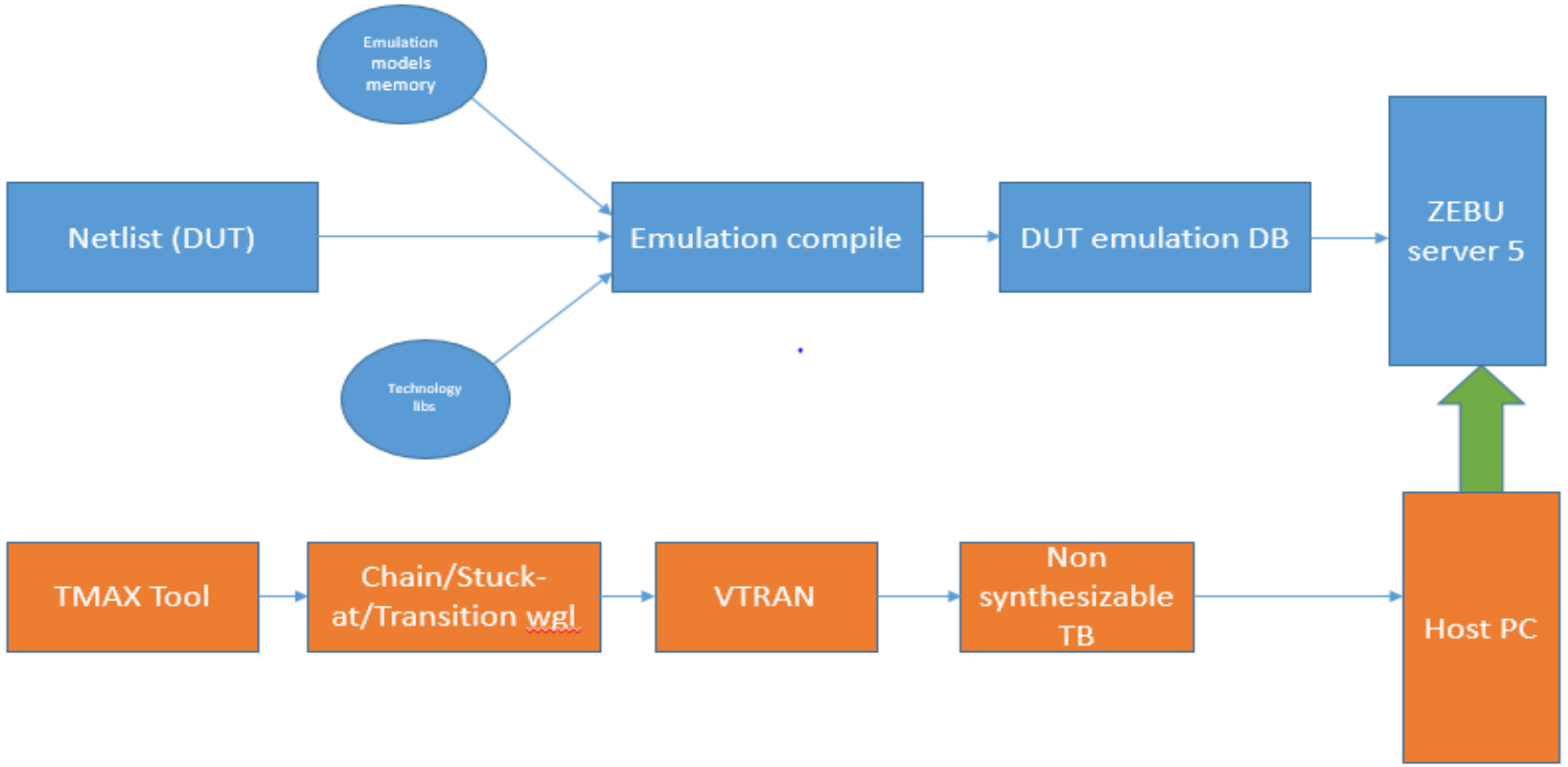
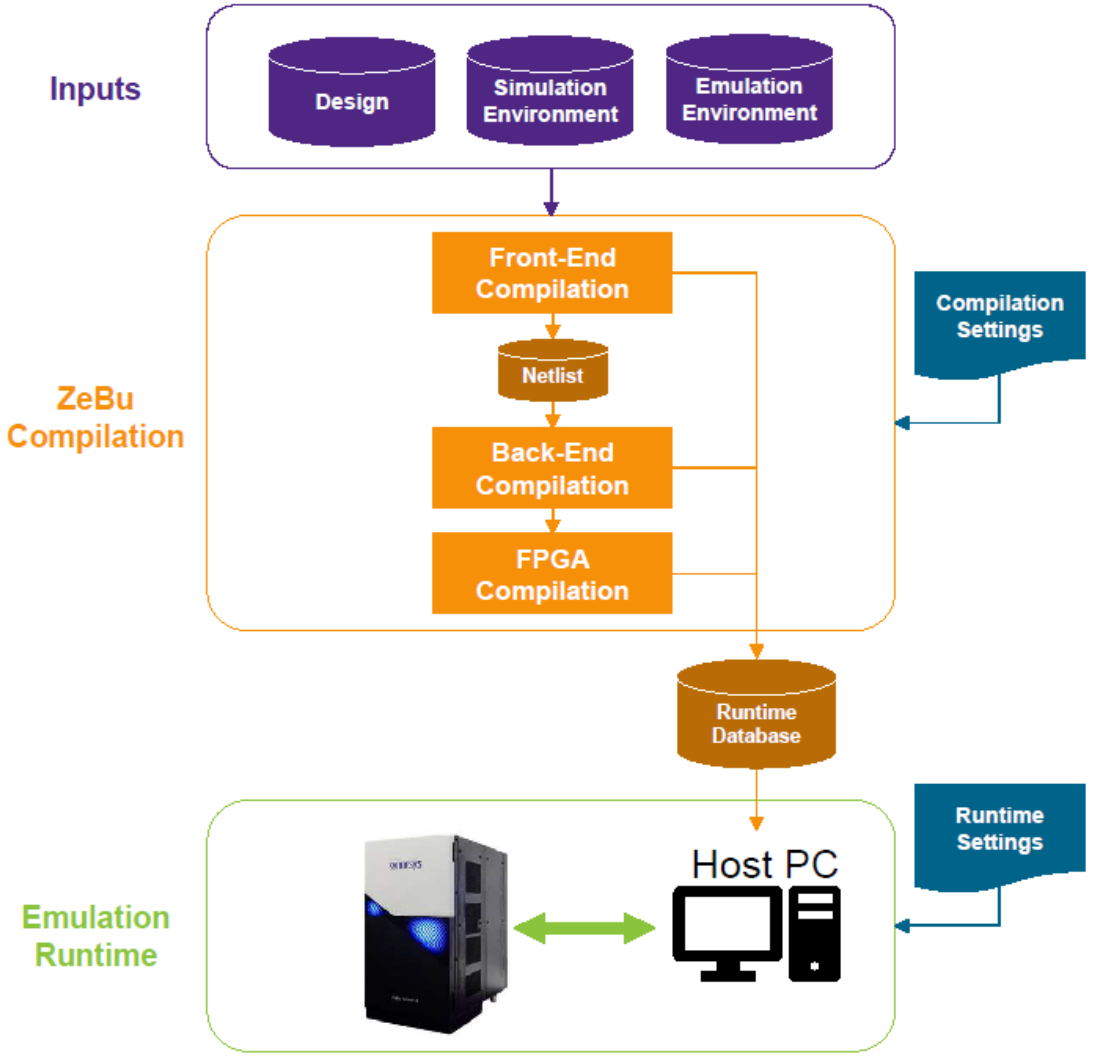
- Simxl flow : It provides an incremental approach to bringing up a working simulation environment into an emulation environment. The approach starts with a signal-based communication mechanism between SW (VCS) and HW (ZeBu).

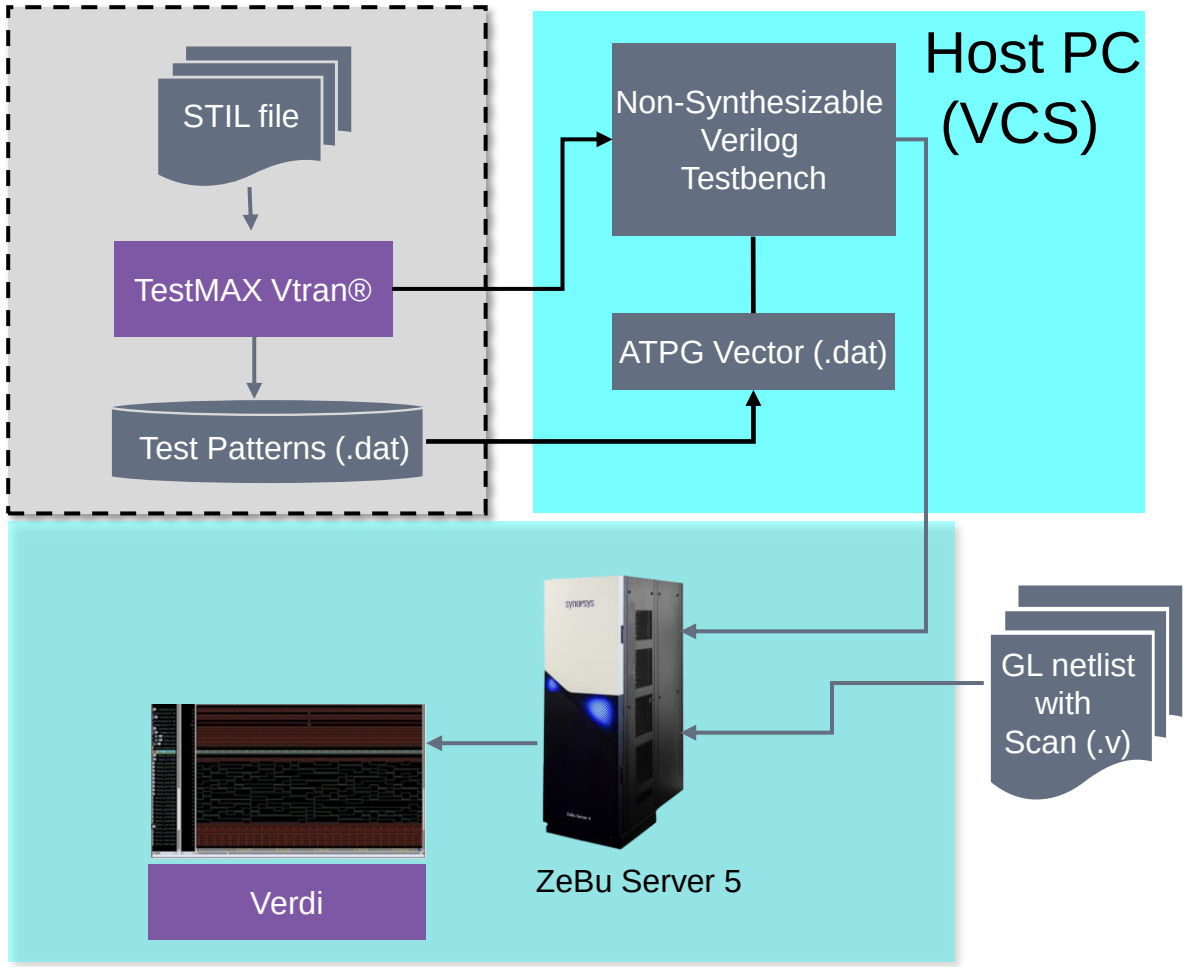


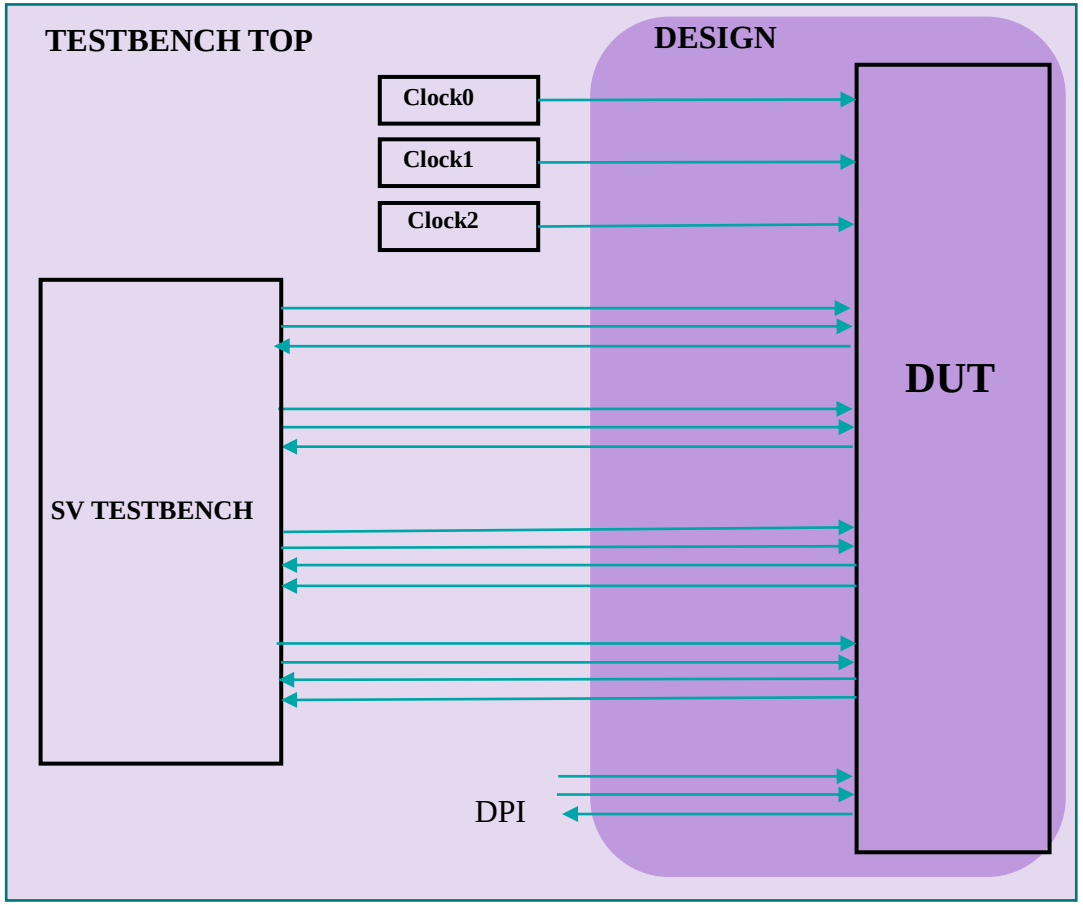
Execution Approach



Execution Approach

ZeBu Sim-XL Flow





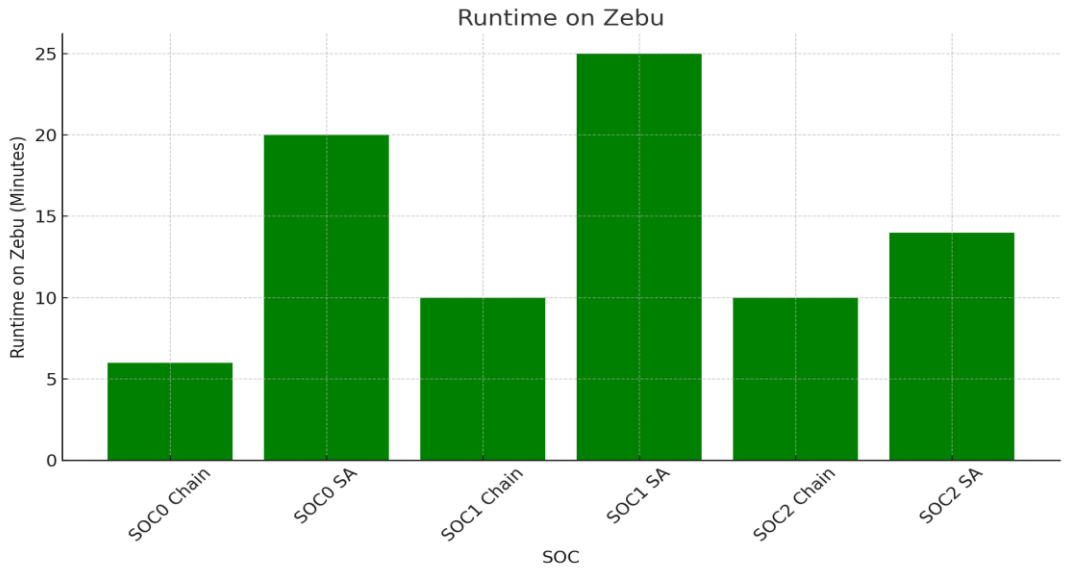
Technical Challenges

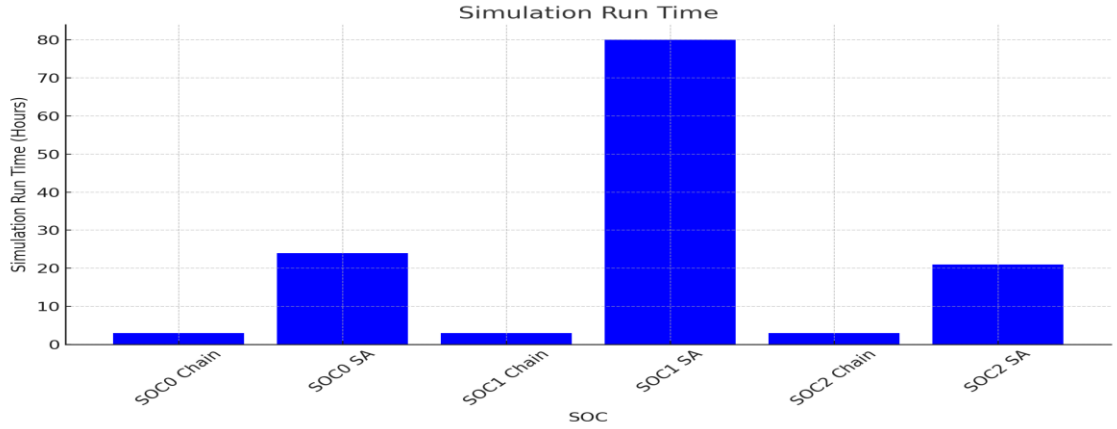
- Migration from simulation to emulation.
- Emulation models.
- Debug: ZTDB to FSDB
- Optimization on post pnr netlist.
- PLL models.
- Timing simulations.

RESULTS

Comparison of runtime for Simulation and Emulation

SOC	Simulation Run time	Runtime on zebu
SOC0 Chain	7 chain pattern -> 3Hours	6min
SOC0 SA	200 pattern -> 24 Hours	10k pattern -> 20min
SOC1 Chain	7 pattern -> 3Hours	10min
SOC1 SA	200 pattern -> 80 Hours	10k pattern -> 25min
SOC2 Chain	7 pattern -> 3 Hours	10min
SOC2 SA	200 pattern -> 21 Hours	2k pattern -> 14min





Months to Minutes

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SCOPE FOR IMPROVEMENT

Scope for Improvement

- In the Zebu-Simxl flow, Design under Test is mapped to hardware and the TB will run on the software. There is scope to make the synthesizable TB and map it to hardware.

- Currently the Design is partitioned and we are mapping each design to the hardware. Zebu should provide ways to map the complete design in one go.

CONCLUSION

Conclusion

- Achieved 50 to 100x gain when simulating the complete serial scan pattern set in emulator over GLS.

- The experimental results show that for 3 clusters, the chain pattern, complete stuck-at ATPG WGL format pattern set of 10K can be simulated in emulator within hours.


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YOUR
COMMUNITY