Emulation Based SOC level Power Estimation at Pre-Si Phase

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Power Profiling and Analysis using Zebu Empower

AGENDA

- MOTIVATION
- OVERVIEW
- POWER ESTIMATION FLOW
- RESULTS AND ANALYSIS
- CONCLUSION
- FUTURE SCOPE

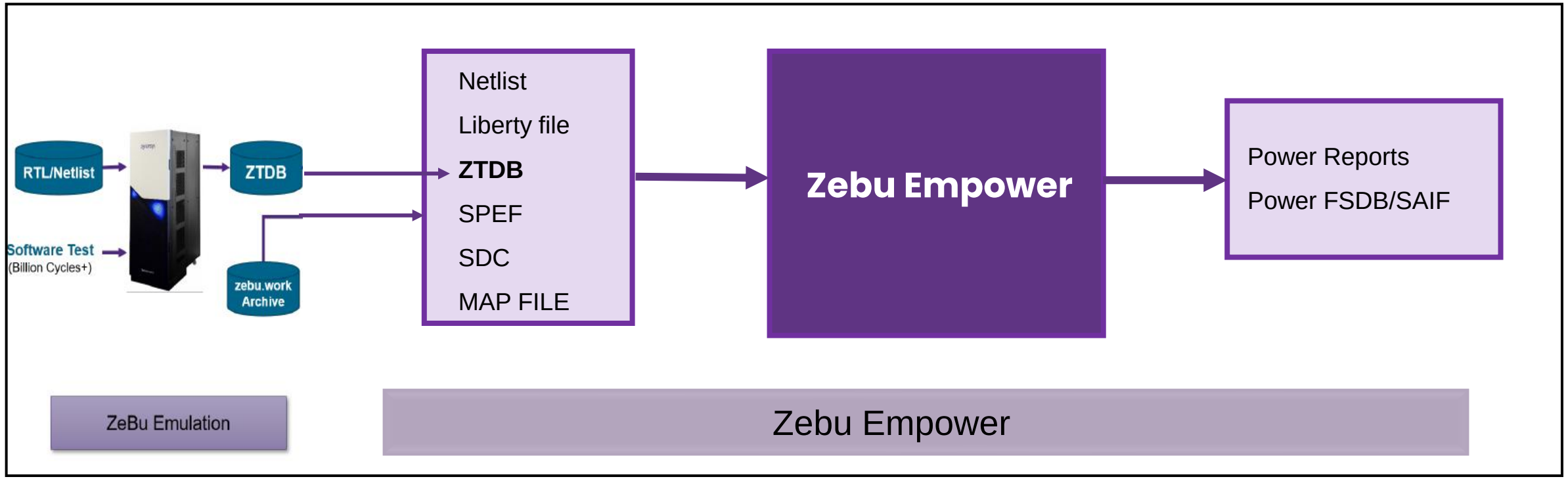
MOTIVATION

- Present Solution
  - Calculate IP/Subsytem level Power.
  - Scale it to SOC level using Scalars.
  - This statistical projection is bit pessimistic.

- Proposed Solution
  - Zebu Empower to address:
    - Profiling the time windows from a billions cycles vector.
    - Powe analysis of the Emulation based SOC Workloads.

Zebu Empower Overview

Can Handle Emulation Based/larger workloads.
Identify High activity Windows in long running use cases.



Zebu Empower Flow: Introduction

Fastest Power Emulator for Hardware-Software Power Verification

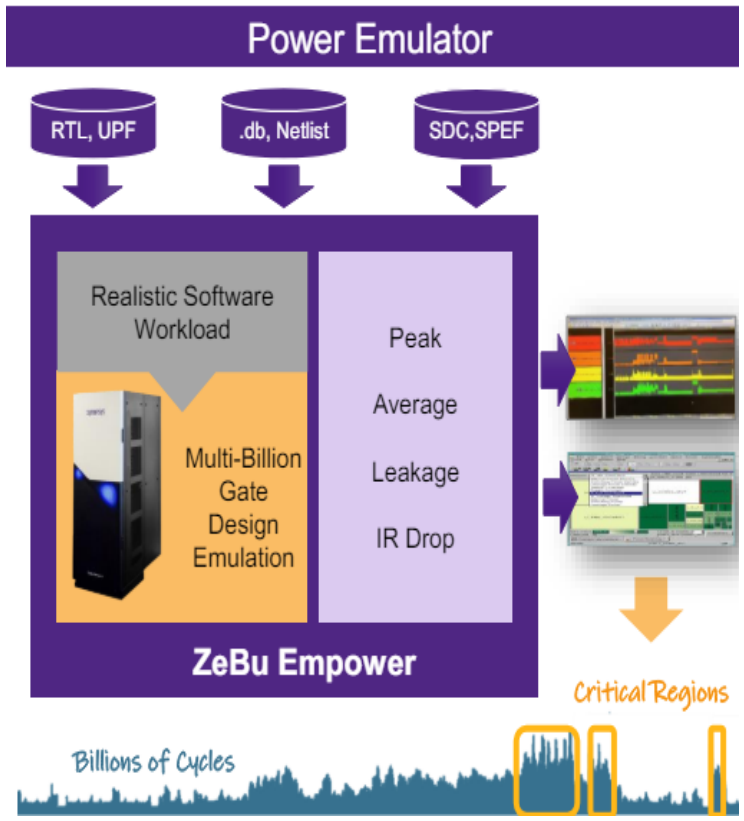


Figure-1: Zebu Empower Features

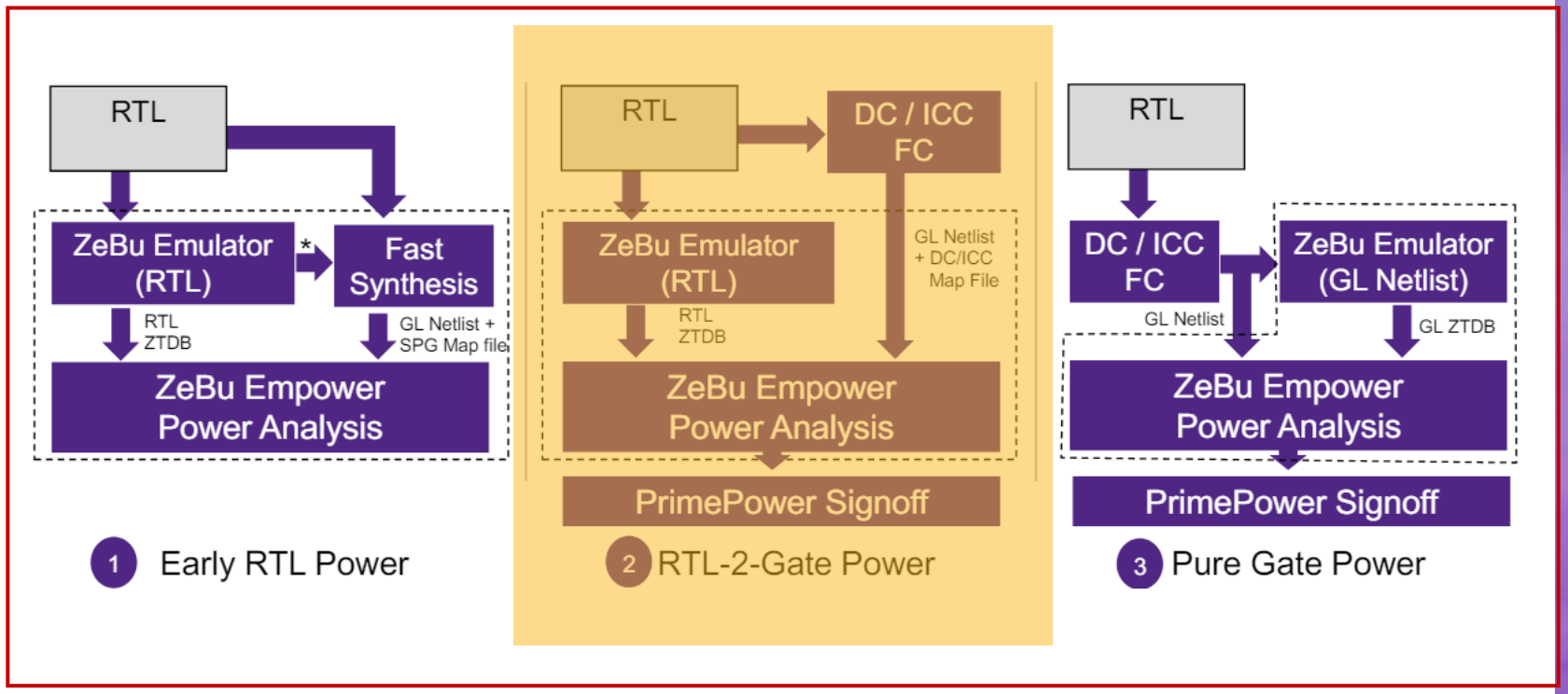
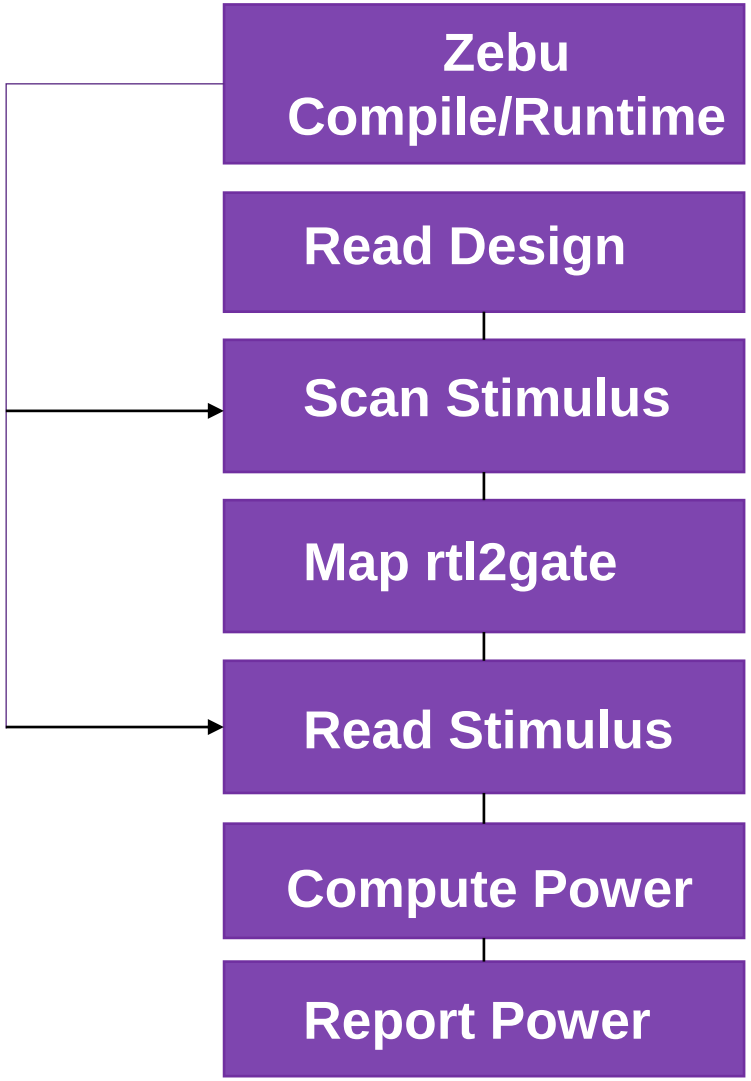


Figure-2: Standard Flow

Image Curtesy: Zebu Empower Ref. Manual

Zebu Empower Power Estimation Flow



- Add dumports and dumpvars for each hier and memories.
- Enable ZTDB Slicing at runtime.

- Sample liberty files
- Read design/SPEF/SDC files.
- Link both design and libs.

- Scan information of the ZTDB header, such as signals names, number of slices, duration, and slice windows

- mapping RTL name of the stimulus with gate name of the design.

- Reads the complete ZTDB/FSDB vectors and saved with name mapping.

- Calculate the power using fastest clock in the design

- Report Computed Power.

Zebu Empower Tool Flow

- **Inputs Liberty, Netlist, UPF, SDC, SPEF, Activity**
  - Liberty DB files for std-cells, memories, …
  - Netlist Verilog or System Verilog netlist
  - SDC (+ variants) create_clock, set_case_analysis, set_driving_cell, set_transition, set_load
  - SPEF Flat or hierarchical
  - Activity Gate ZTDB or Gate FSDB

- **Outputs Power, SAIF, FSDB**
  - Power Average power
  - GL-SAIF Full Gate SAIF for specified hierarchy/window
  - GL-FSDB Full Gate FSDB for specified hierarchy/window

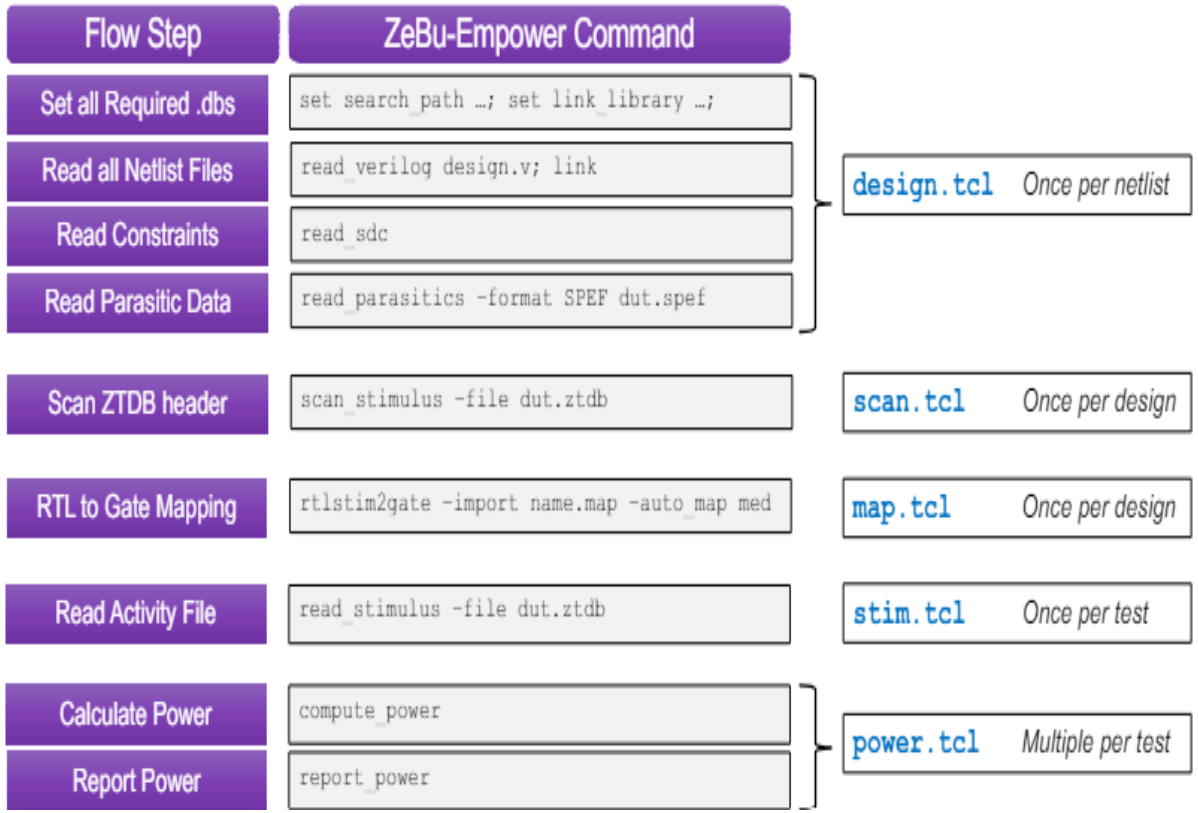


Figure-3: Zebu Empower Power Estimation Steps

Image Curtesy: Zebu Empower Ref. Manual

Zebu Compile

Changes required for Power Analysis during Emulation model build

- Power calculation requires waveforms for all gate-level nodes
  - Every gate-level net/pin must be available or calculated for power calculation
- ZeBu Waveforms
  - ZeBu generates data for Sequential cells + Memory I/O + Top-level I/O
  - QIWC (or for a small design FWC) is ideal (readback is usually too slow)
  - Add QIWC onto the design or portion of design for power-calculation
  - Sequential-only is more efficient - Less data, less ZeBu capacity required
- Combinational Signals
  - Waveform engine is needed to calculate all combinational nets
  - If we know the values of all flops, we can calculate all combinational nets
  - Waveform and power calculations occur automatically inside the ZeBu-Empower tool

```
// UTF
clock_delay -module {clk_gen}
debug -waveform_reconstruction TRUE
optimization -auto_inline_limit 30
```

```
// Flops - QIWC value set
initial begin: qiwc
  (* qiwc *) $dumpvars(0, top.dut);
end
```

```
// Ports - FWC must be separate value set to QIWC
initial begin: fwc
  (* fwc *) $dumpports(1, top.dut.cpu0);
  (* fwc *) $dumpports(1, top.dut.cpu0.mem0);
end
```

Figure-4: UTF Switches for Zebu Compile

Image Curtesy: Zebu Empower Ref. Manual

ZeBu Runtime

- Standard ZeBu Runtime (zRci)
  - Enable ZTDB slicing at runtime (10G-20G slice sizes), specify MB for size (default is cycles) – Dump QIWC+FWC using –awc switch

```
# zRci.tcl
config zebu_work ./zcui.work/zebu.work
start_zebu  qiwc

# Dump + RTL clocks + All-wc dump
config default_clock posedge "timestamp"
set fid [dump -file dmp.ztdb -awc  -sampling "timestamp"]

# Dump + Size Slice
dump -fid $fid -add_value_set or1200_flops_qiwc
dump -fid $fid -add_value_set or1200_ports_fwc
dump -fid $fid -interval 5000MB
dump -fid $fid -enable

# Run, Close, Quit
run 100000
finish
```

Figure-5: Switches for Zebu runtime

Image Curtesy: Zebu Empower Ref. Manual

Subsystem level Comparison with PrimePower

Subsystem	PrimePower mW			ZebuEmPower mW			Power Numbers
	Dynamic	Leakage	Total	Dynamic	Leakage	Total	Correlation in %
Subsystem-1	111.4	113.6	225.0	94.7	126.8	221.5	98%

Report Types:

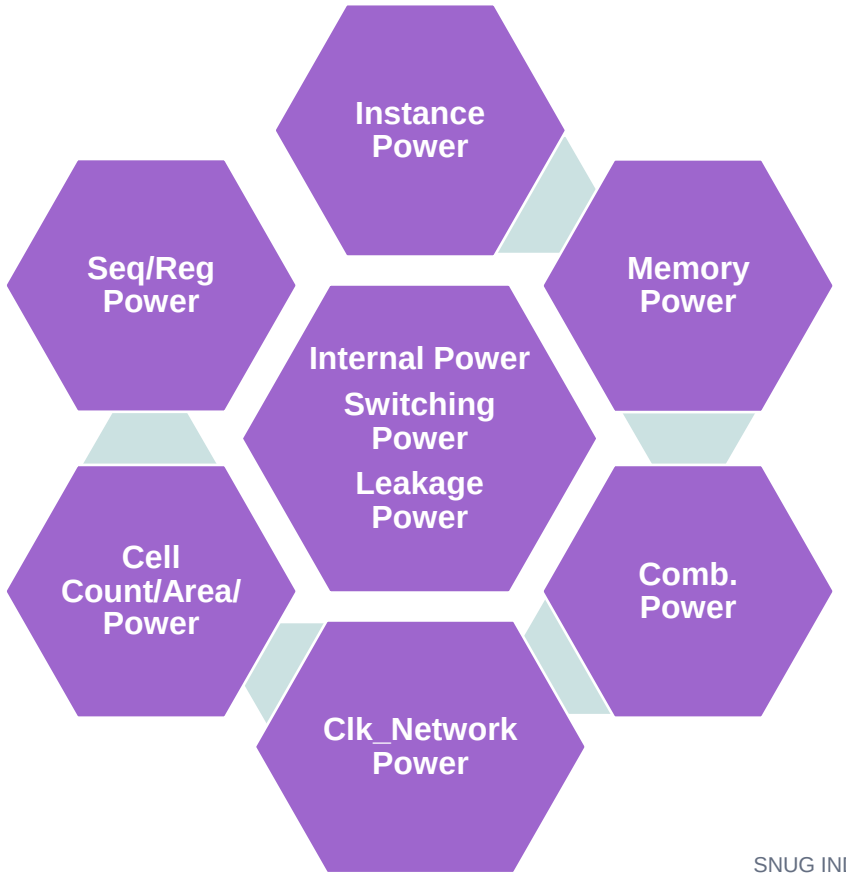
- Category – different power_groups.
- Hierarchy – L1 reports for each subsystems.
- Per cycle – power reported at each cycle.

Power Types:

- Internal Power.
- Switching Power.
- Dynamic Power.
- Peak Power along with Peak timestamp.

Annotation Reports:

1. Waveform Annotation Report.
2. Mapping Annotation Report.



Power Estimation for System level Use Case.

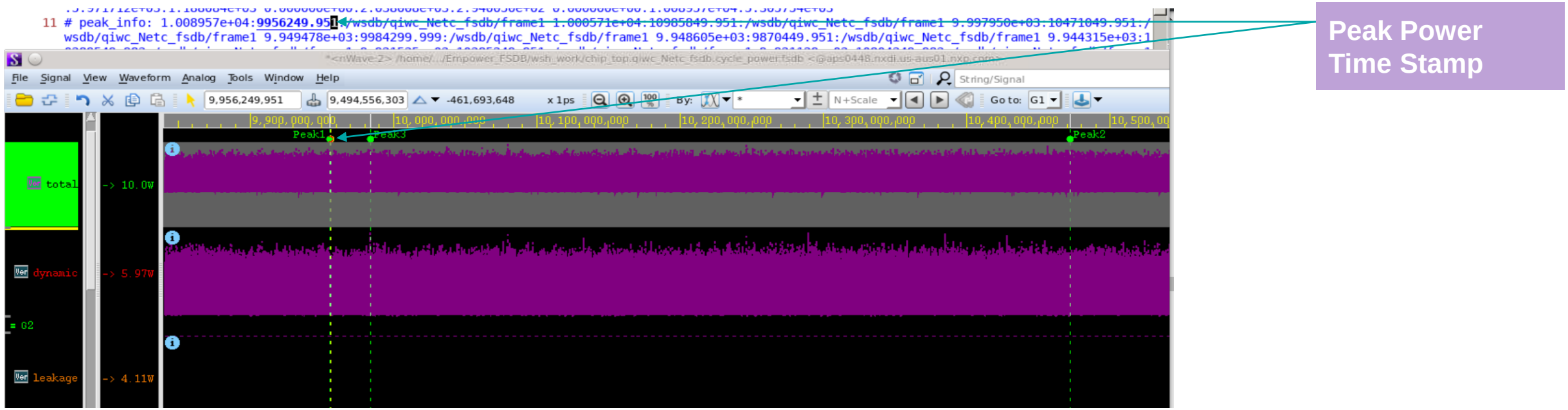
Power Number for SOC Use Case:

	Dynamic in mW	Leakage in mW	Total in mW
SOC	1188.1	4117.7	5305.8

Peak Power in mW	10089.56
Peak Time in nS	9956249.95

Per Core Power:

Subsystem Core	Dynamic Power in mW
Core1	52
Core2	51
Core3	51
Core4	53



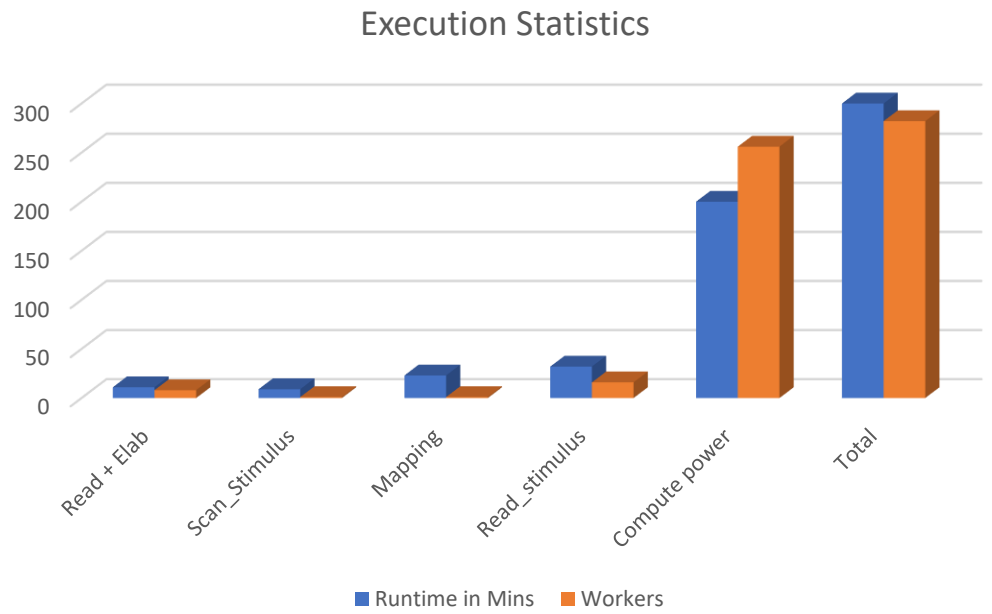
Peak Power Time Stamp

Image: Power FSDB in Verdi

Zebu Empower Runtime Statistics

The below table shows the runtime statistics of each stage of zebu empower flow:

Stage	Runtime in Mins	Workers
Read + Elab	11	8
Scan_Stimulus	9	1
Mapping	23	1
Read_stimulus	32	16
Compute power	200	256
Total	300	282



Few jobs run longer time since the vectors are huge ZTDB traces are of sizes in GBs/TBs.
Using efficient LSF configurations would help running the jobs faster.

Learnings and Enhancements

Learnings:

Learning	Comments
Zebu Compile : - Required to add “dumports” for all the primary inputs and outputs: • each subsystem hierarchy. • all the memory boundaries.	Feed back to Emulation teams to build Power Analysis friendly Models.
Zebu Empower Runtime: Runtime Performance Improvements for Bigger Jobs.	• High runtime was observed for some of the tasks during “Compute_Power” stage. Worked on the LSF settings for the efficient and faster execution.

Improvements:

Enhancements
• Enabling at RTL Stage by supporting RTL files as input files.
• Live streaming of the switching data from emulator directly into the zebu empower tool
• Glitch Power Analysis

Conclusion

1. Zebu Empower provides solution for SOC Power Analysis.
    1. Power Profiling.
    2. Average/Peak Power Numbers.
2. Long vector power analysis and power profiling.
3. It’s a Power Engine for processing Emulation Size Data (TB).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