Enabling PCIe and NVMe pre-silicon validation with real devices using EP1 emulator

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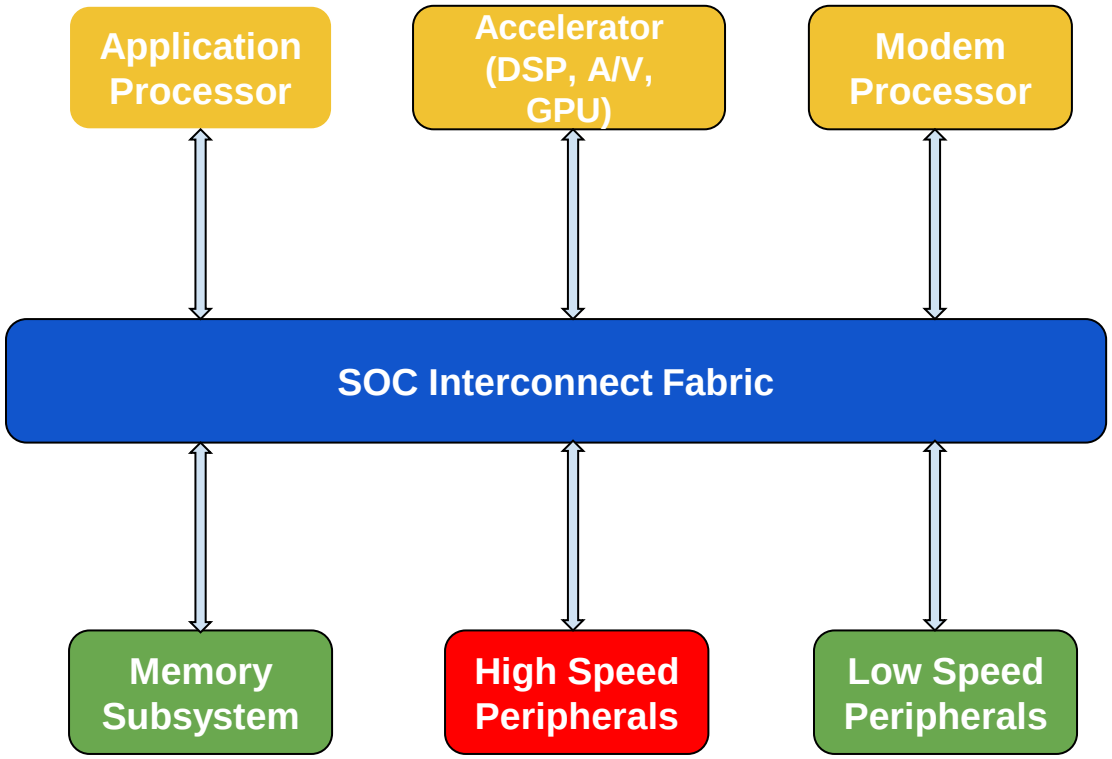
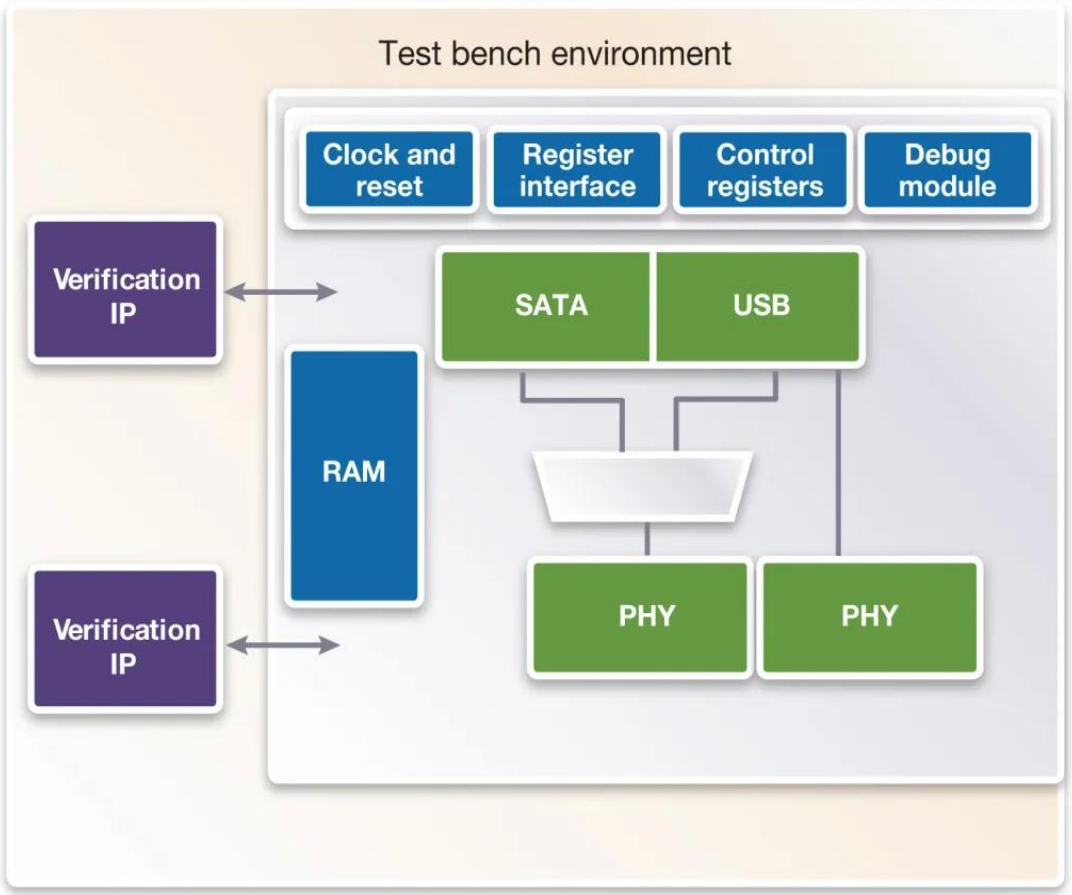
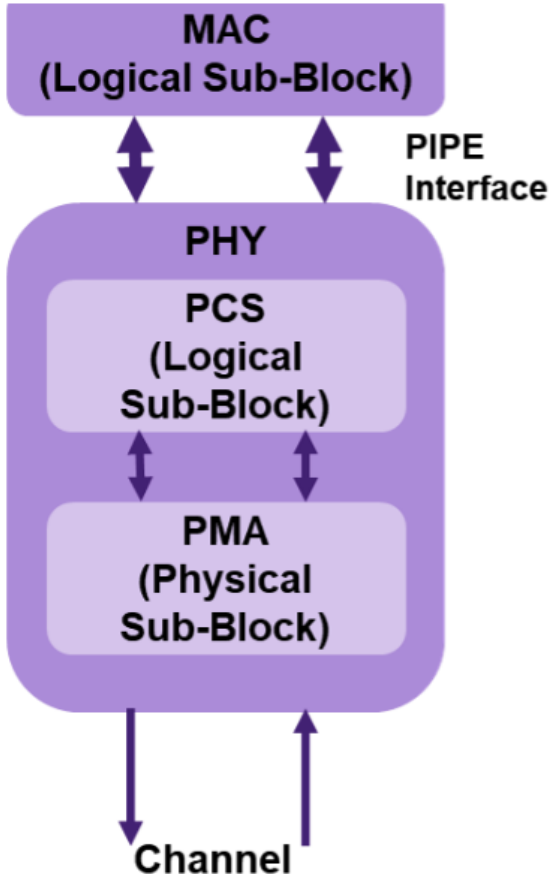
Mobile SOC Architecture



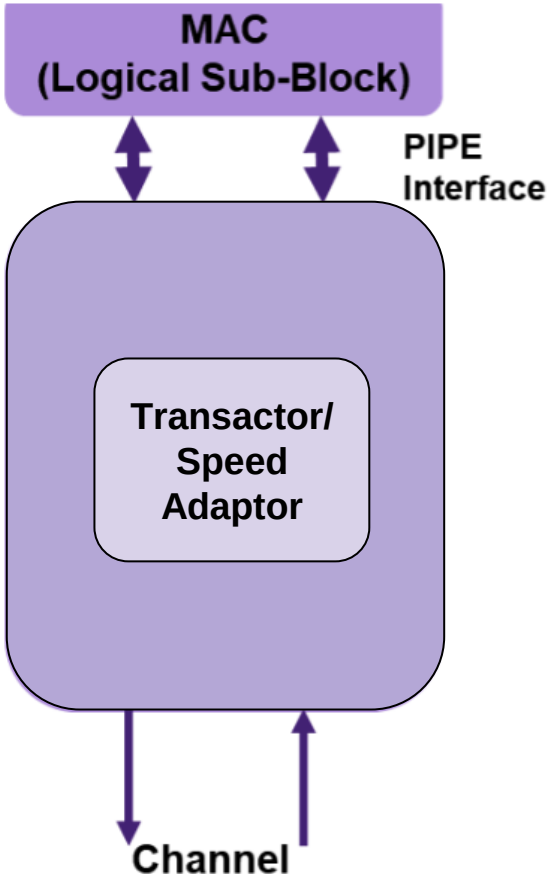
Interface Verification



PCIe System



PCIe Emulation



Our High Speed Interface validation challenges

- SOC has multiple High Speed IO interfaces eg. PCIe/USB/UFS/Camera/Display
- Transactors are used for and early RTL validation of HS interface subsystems. Transactors are good for early adoption and wide scale deployment
- We faced the following challenges with transactors
  - Interoperability testing with different devices.
  - Validation of Power Management features in real world use case scenario
  - Validation of real PHY
  - Testing of connect-disconnect features
  - Testing of real world interrupts
  - Low performance of SOC emulation model with all transactors plugged in.
- This presentation discusses how on PCIe Speed Adaptor + EP1 emulator solution addressed these challenges

Emulator selection

EP1 was selected vs

- ZeBu(ZS4/ZS5): Less interconnect options for real world connectivity
- Easy access to SA(Emulators are in datacenter, EP1 can be in a silicon bring up lab)

EP1 offered

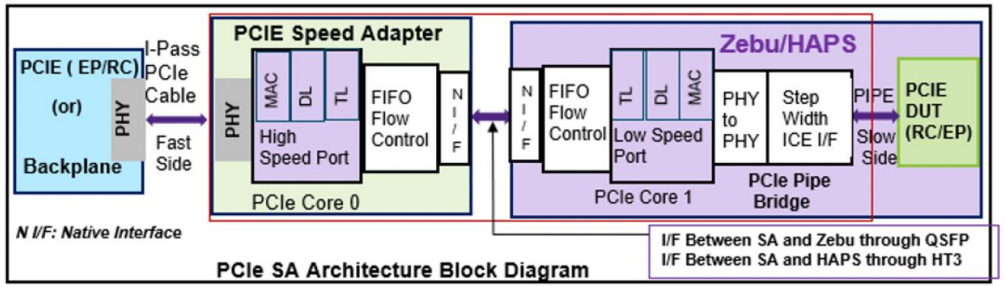
- Emulation S/W stack(Push button compile, full debug visibility)
- Prototyping H/W(Flexibility and richness of interconnectivity)
- ICE Hybrid
  - (Interface Of Interest) which is PCIe was connected in ICE mode
  - Other interfaces were using transactors(UART, Storage, DRAM etc).

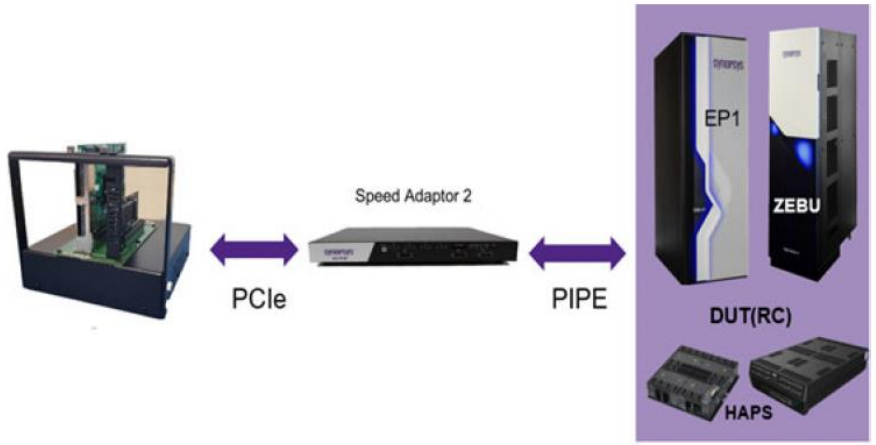
PCIe Speed Adaptor

- Speed Adaptor:
  Based on the PCIe switch with TLP bypass architecture. Has flow control based speed adaptation logic between high speed (connects to real device) and low speed interfaces (connects to DUT)

- DUT:
  PCIe Root Complex on EP1 emulator (through PIPE interface can be any Gen and Lane width up to Gen5-x16)

- Endpoint device:
  Gen4 OTS PCIe and NVMe cards (on backplane through real PHY with Gen1-x4 Speed)





Accomplishments

- PCIe Gen-4 enumerated(different OTS card validated)
- NVMe cards functional(basic and bulk data transfer tests)
- OS based System Validation suite implemented.
- 5MHz emulation performance
- ASPM test cases validated
- Real Time interrupts validated

Challenges

- Debug at High Speed side was a challenge. During initial phase protocol monitor was not available and had to use real testers for bring up
- Hardware RMAs.
- Flexible cabling: While helps in performance and ICE capabilities, it adds to installation and maintenance overheads

Roadmap

- Try Speed Adaptor on emulator, not EP1 for wide scale deployment
- Speed Adaptors for other HS interfaces.
- Checkpointing on Speed Adaptor setup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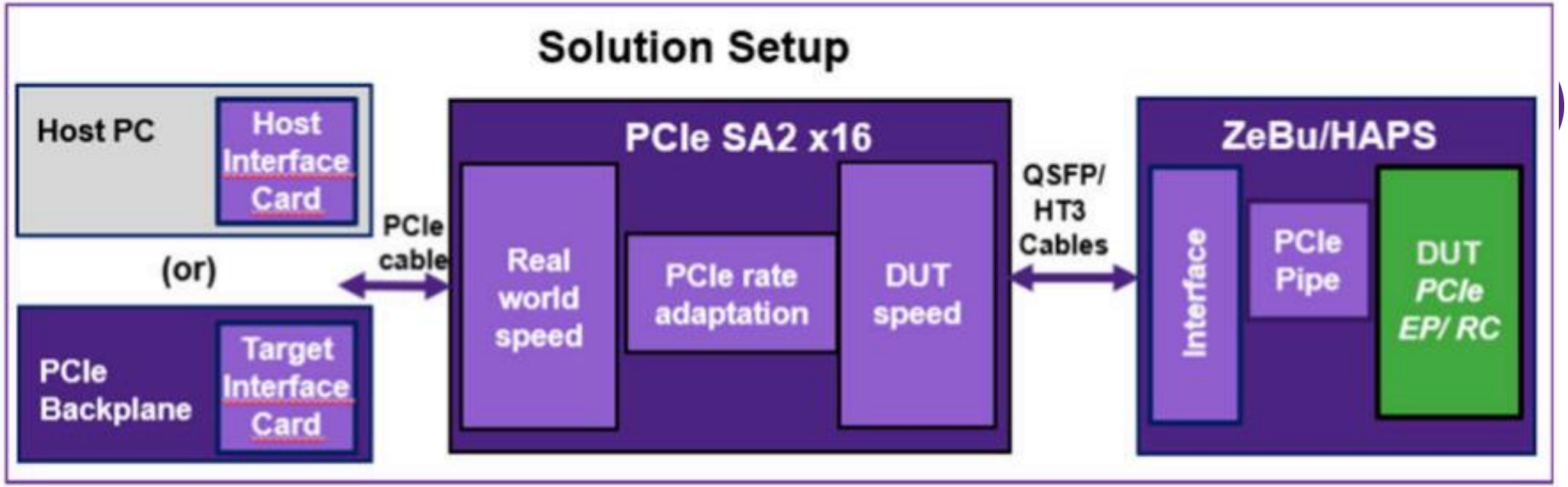
Back Up


Solution Setup
Host PC
Host Interface Card
(or)
PCIe Backplane
Target Interface Card
PCIe cable
PCIe SA2 x16
Real world speed
PCIe rate adaptation
DUT speed
QSFP/ HT3 Cables
ZeBu/HAPS
Interface
PCIe Pipe
DUT PCIe EP/ RC


User Supplied
Host PC
PCIe Backplane


PCIe Speed Adapter: included hardware
HIB plugs into PC (or)TIB plug into Backplane
PCIe cable
QSFP-DD to SFP+ Breakout cable
(Or)
QSFP Optical Kit
(Or)
HT3 Cables
Speed Adapter
(Or)
HT3C2HT3 Cables


ZeBu/HAPS System
ZS4/ZS5/ EP1
HAPS-80/100