Power Precision

Elevating IC Integrity with Power Replay

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Agenda

- Introduction
- Conventional method and Challenges
- PowerReplay Flow
- Results
- Conclusion & Future Work

Introduction

- VLSI design is progressing towards **Ultra Deep Sub-Micron technology** (UDSM) nodes to achieve higher level of performance, improved power efficiency and small form factor area.
- Lower technology nodes trend (Figure 1) shows a major challenge on **power** which directly impacts the **battery life** and energy consumption of the System On-Chip(SOC) device.
- **Accurate power** modeling during chip design allows designers to identify and mitigate power-related issues early in the design phase.
- Helps in optimizing power usage without compromising on performance, ensuring cost-effective and robust designs.
- The major challenge is obtaining the **accurate power** numbers which is always **late in the project cycle.**
- So, This presentation covers about how PowerReplay steps in and uses **left shift approach** in closing the design with signoff accuracy.

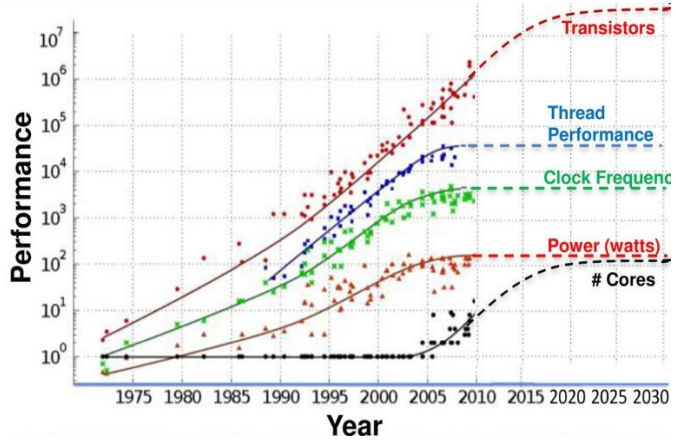


Figure 1: Technology scaling trend data

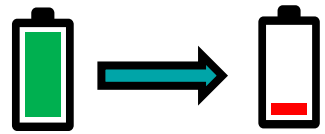
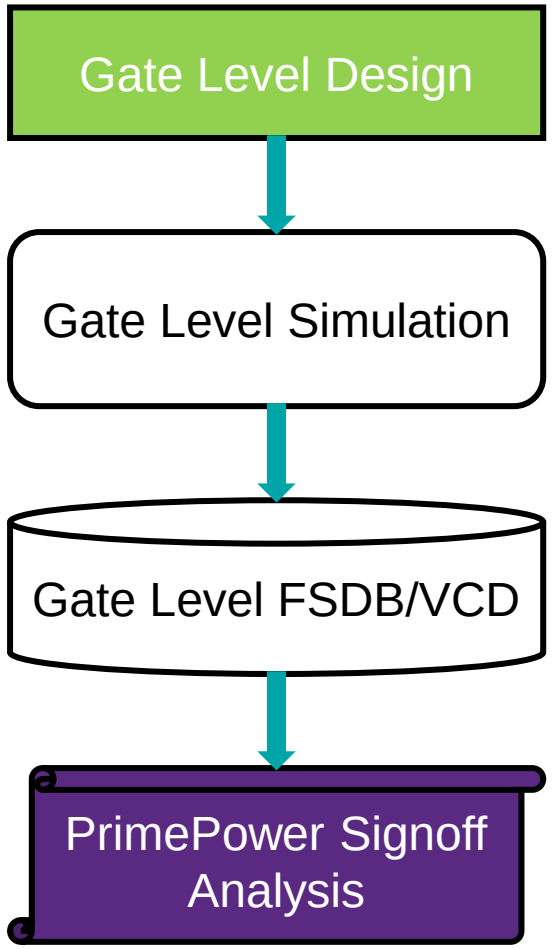


Figure 2: Battery charge drains faster due to power impact

***Figure 1 image reference from** SlidePlayer - Kunle Olukotun, Lance Hammond, Herb Sutter, Burton Smith

Conventional methods and Challenges

Conventional methods



Gate-Level Simulation:
Involves running full simulations on the synthesized gate-level netlist using realistic test vectors.
Limitation: Time-consuming and requires considerable computational resources, making frequent analysis impractical.

Vectorless Estimation:
Uses probabilistic models to estimate switching activity and hence power consumption.
Limitation: Potential for significant inaccuracies as actual conditions can differ markedly from estimated models.

Challenges

- **Delayed availability of Gate-Level FSDB:** Late availability of gate-level FSDB complicates SOC Integrity checks and delays final sign-offs.
- **Late findings of Power Issues:** Discovery of power issues during GLS simulation can impact project schedule.
- **Complexity of Modern Semiconductor Designs:** The intricate nature of contemporary designs increases the complexity of power simulations, potentially leading to longer runtimes as more detailed analyses are required to ensure accuracy.
- **Accuracy in Dynamic Power Estimation:** High accuracy in power estimation is crucial for making informed decisions during design iterations. Inaccuracies can lead to multiple design revisions, impacting the physical design closure and delaying the overall project timeline.

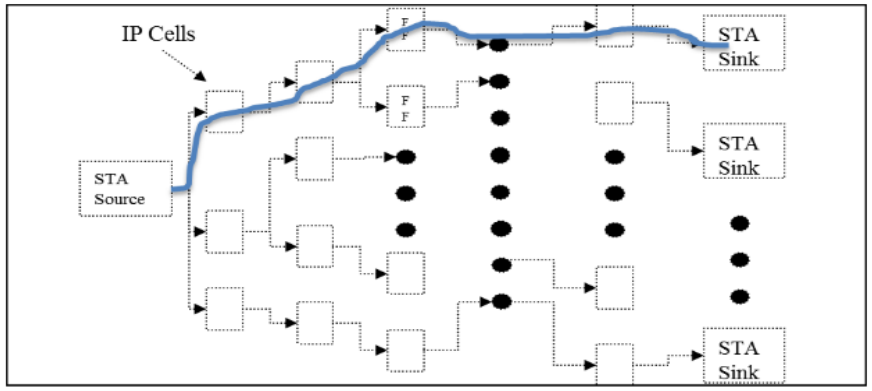


Figure 3: Gate VCD activity trace path

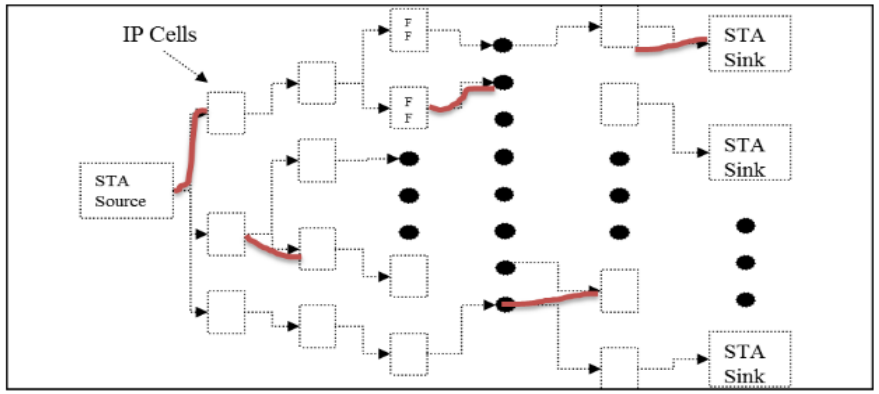
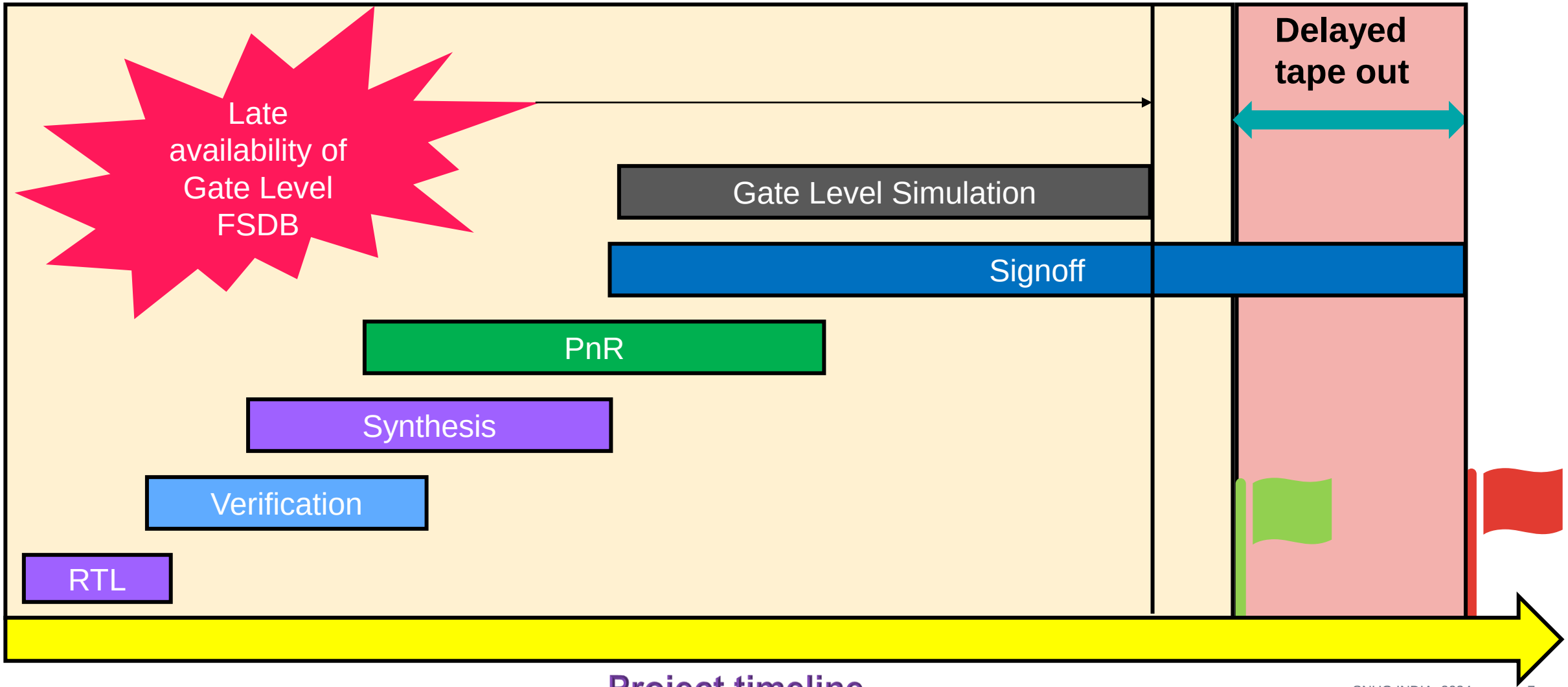


Figure 4: Vectorless implementation with random gate selection

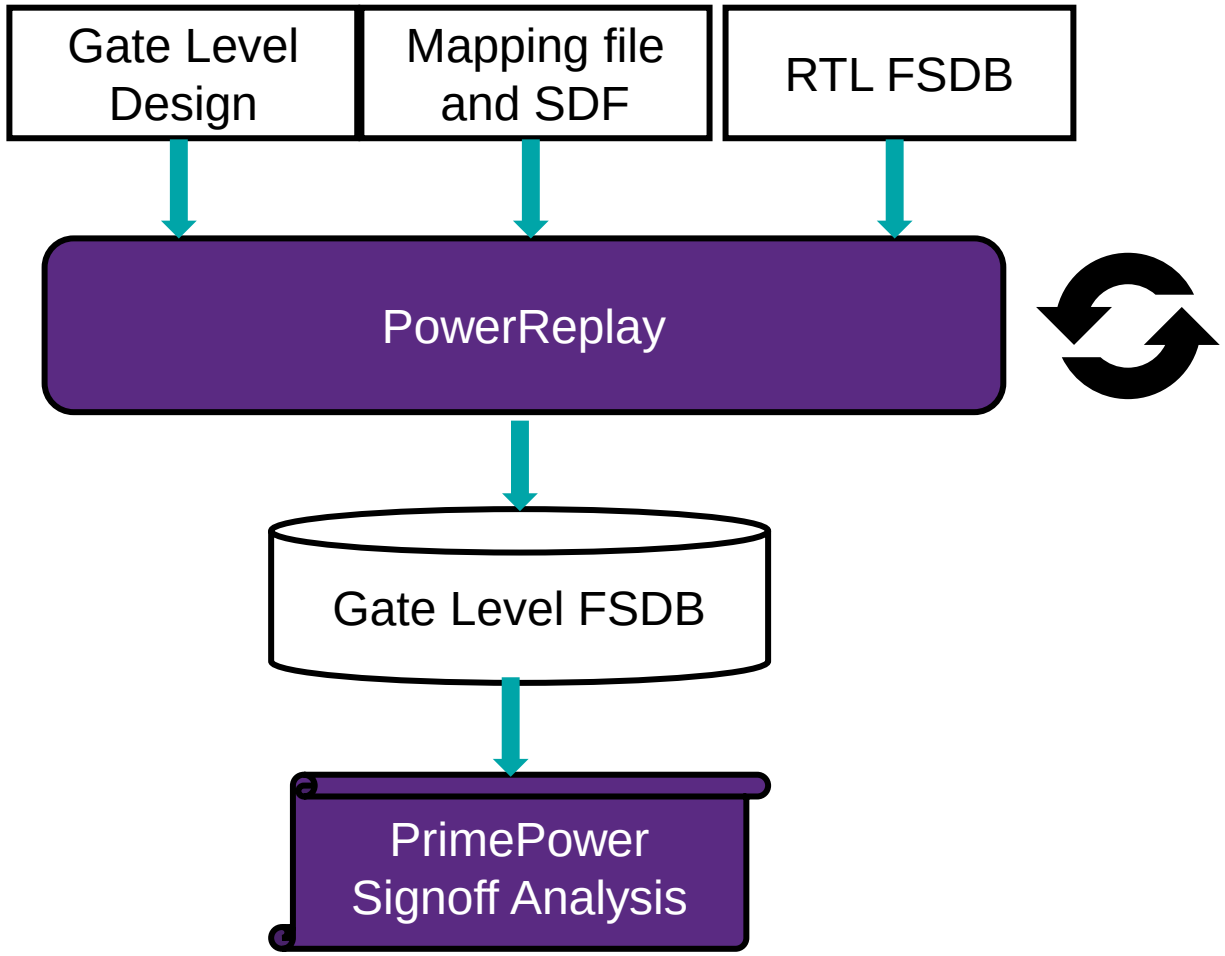
*Figure 3 & 4 image reference from semiengineering

GLS Simulation Impact



PowerReplay Flow

PowerReplay Flow



1. RTL-Gate Mapping
Using Good coverage RTL to Netlist mapping.

2. Replay Simulation
- Used RTL FSDB (from VCS or 3rd Party)
- Specify sim. windows & design scope
- Auto-generate Gate-level TB
- Leverage SDF from STA.
- Generate Gate-level FSDB

3. Power Analysis
Provide FSDB to PrimePower for Power analysis

PowerReplay Flow – Mapping feature

RTL FSDB

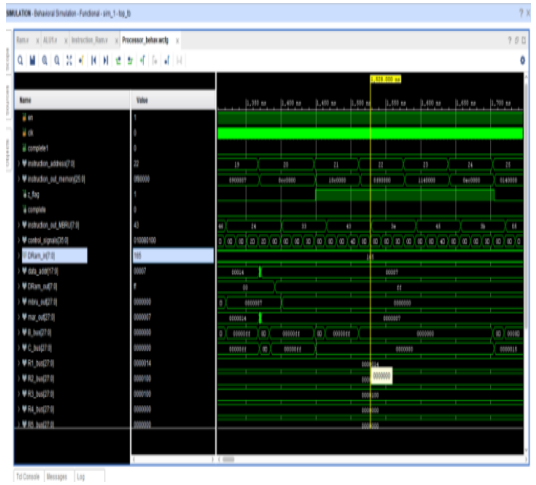
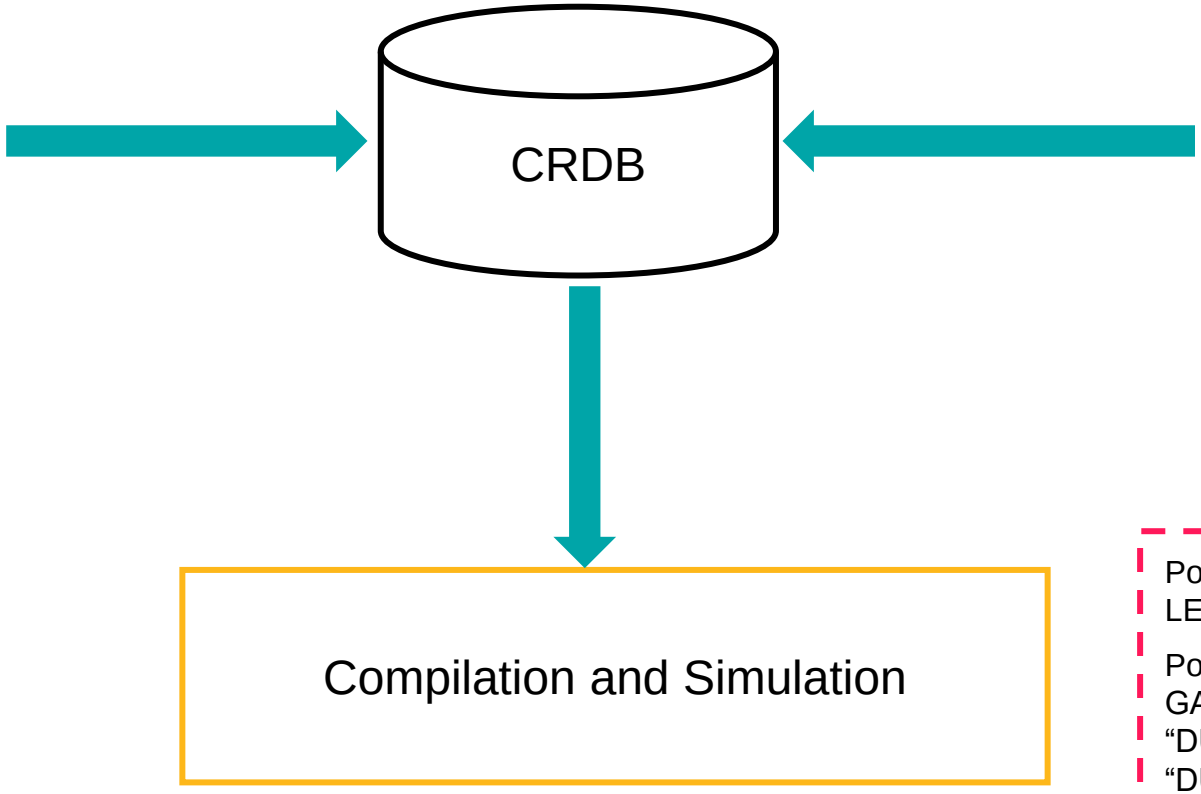


Figure 5



Gate level Netlist

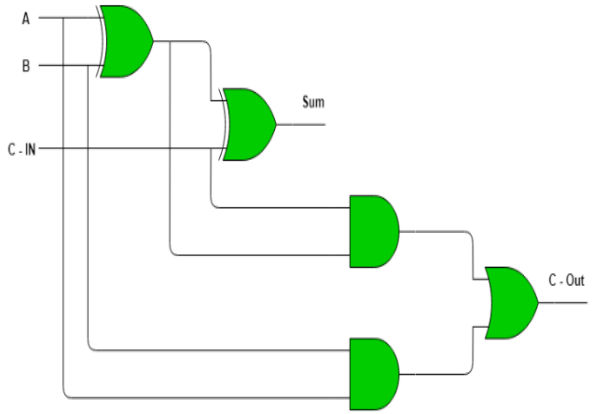


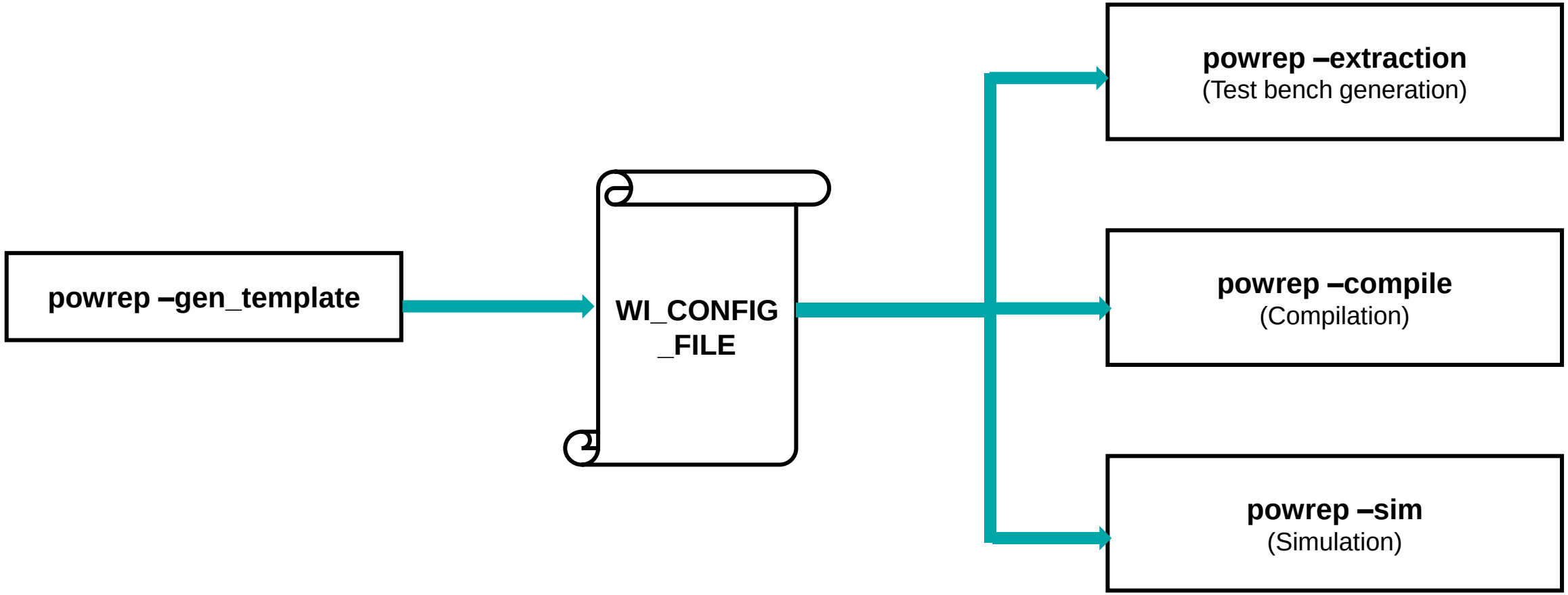
Figure 6

Powrep_convert_pp_map –map LEC.mapfile.pp –o pp.txt

Powrep –map –RTL_FSDB “rtl.fsdb” –GATE “-lib lib_gls” –top “DUT_<DESIGN>” –target_scope “DUT_<DESIGN>” –impmap pp.txt

*Figure 5 image reference from Linkedin
*Figure 6 image reference from geeksforgeeks

PowerReplay Flow – Config file flow



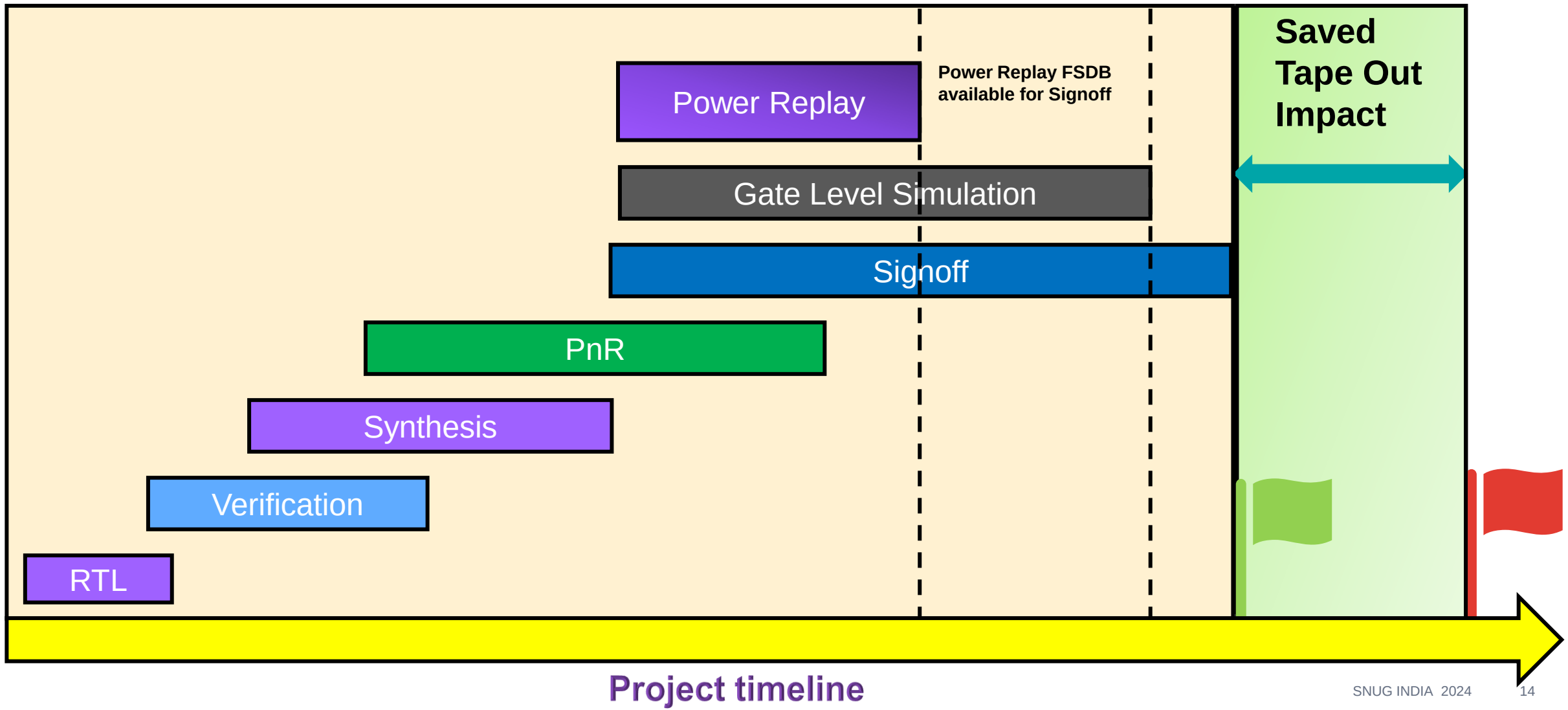
Sample Wi_config file

- set FSDB = Design.fsdb (RTL FSDB)
- set Scope = tb.DUT.Design
- set Map = gls_mapping.txt
- set Simulation_Compile_script = vcs_wi_compile.rc (Contains the VCS Gate Level Compile Command)
- set Simulation_Run_script = vcs_wi_run.rc (Contains the VCS Gate Level Run Command)
- set Checking_Rule = +mapping_quality
- set Begin_Time = <BEGIN_TIME>
- set End_Time = <END_TIME>
- set Time_Unit = ns
- set SDF = Design.sdf

PrimePower Template

- set_host_options –max_cores
- restore_session <SESSION_PATH>
- set power_enable_analysis true
- set power_analysis_mode time_based
- **read_fsdb -strip_path <SCOPE_PATH> -time {Begin time End time} <GATE_LEVEL_FSDB>**
- update_power
- **report_power -nosplit**
- report_switching_power

Left Shift Approach using PowerReplay

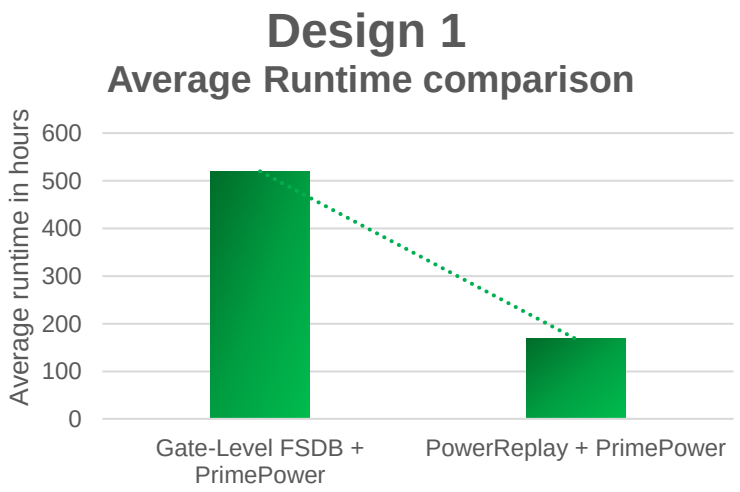


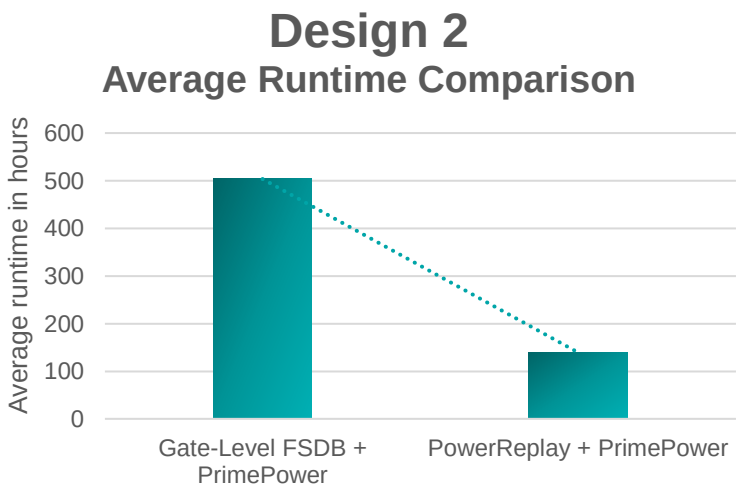
Results

Results

Designs	Gate Count	Total Power difference between Gate Level FSDB and PowerReplay FSDB	Peak Power difference between Gate Level FSDB and PowerReplay FSDB
Design 1	>800K	~2%	~14%
Design 2	>500K	~%5.3	~4.4%

98% Mapping coverage





Conclusion & Future Work

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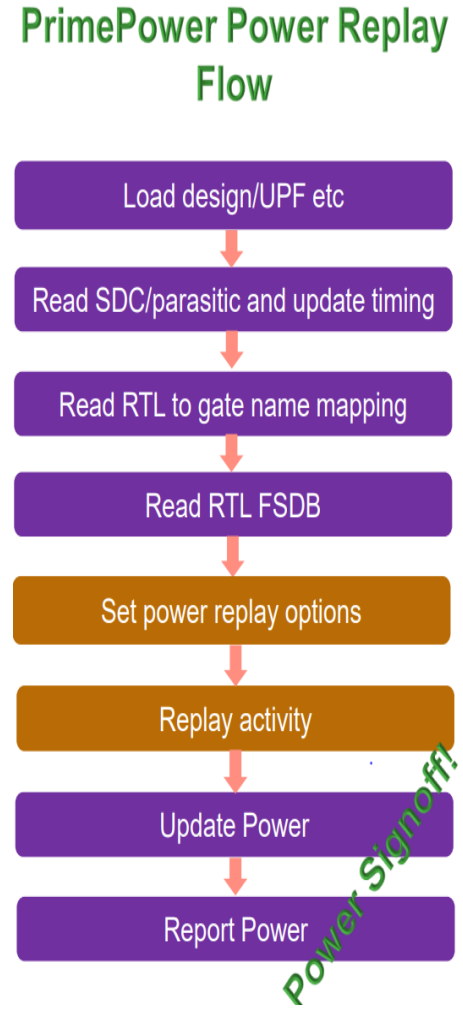
- **Efficiency and Time Savings**:
  - PowerReplay streamlines the power analysis process, significantly reducing the time from design to verification compared to traditional methods.
  - Enables quicker iterations and faster decision-making, leading to shorter project timelines.
  - TAT is almost improved by ~50%.
- **Enhanced Accuracy**:
  - Offers more precise power consumption analysis by using real-life scenarios earlier in the design cycle.
  - Helps in identifying and mitigating power-related issues well before they become costly to address in later stages.
- **Future Work:**
  - Exploration on Integrated Power Replay feature in PrimePower tool.
  - Work with Synopsys team to further improve the correlation between Simulation Gate level FSDB and Power Replay Gate level FSDB.

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