Navigating the Challenges of RC Parasitic analysis in IC Design: A Standardized Approach using StarRC Parasitic Explorer

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Agenda

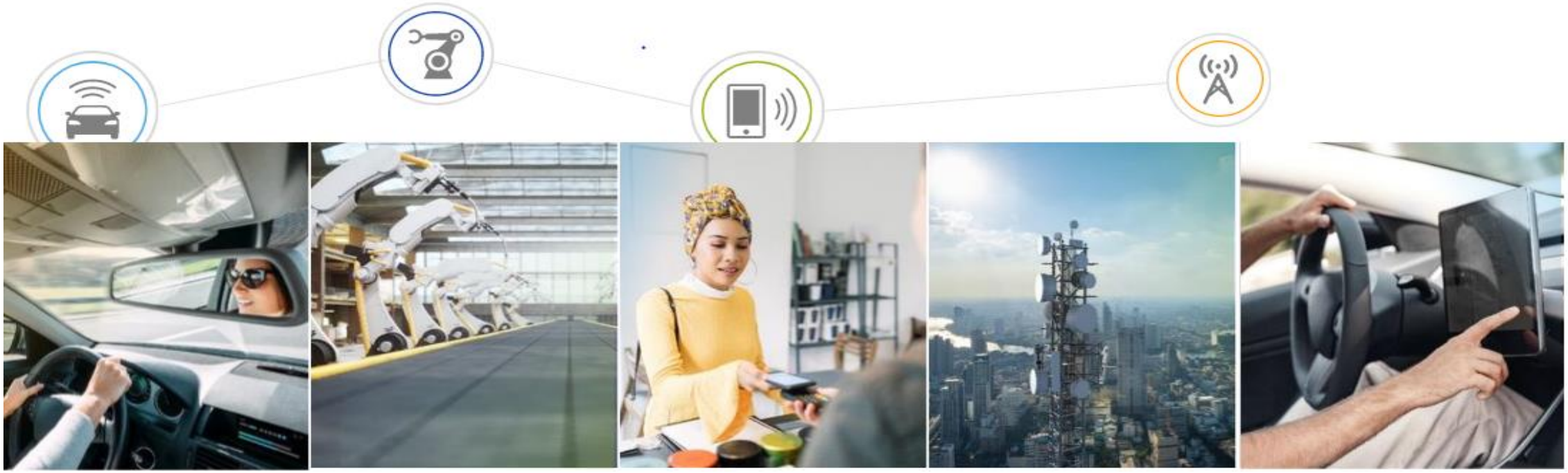
- Challenges and Motivation
- Proposed Approach
- Introduction to Parasitic Explorer
- Design Under Test
- Why Parasitic Explorer?
- Parasitic Explorer Flow and Methodology
- Results
- Unique Features
- Conclusions and Future Scope

NXP SEMICONDUCTORS OVERVIEW

SECURE CONNECTIONS FOR A SMARTER WORLD

OUR DIGITALLY ENHANCED WORLD IS EVOLVING TO ANTICIPATE AND AUTOMATE

NXP Semiconductors N.V. (NASDAQ: NXPI) is a global semiconductor company creating solutions that enable secure connections and infrastructure for a smarter world. NXP focuses on research, development and innovation in its target markets.

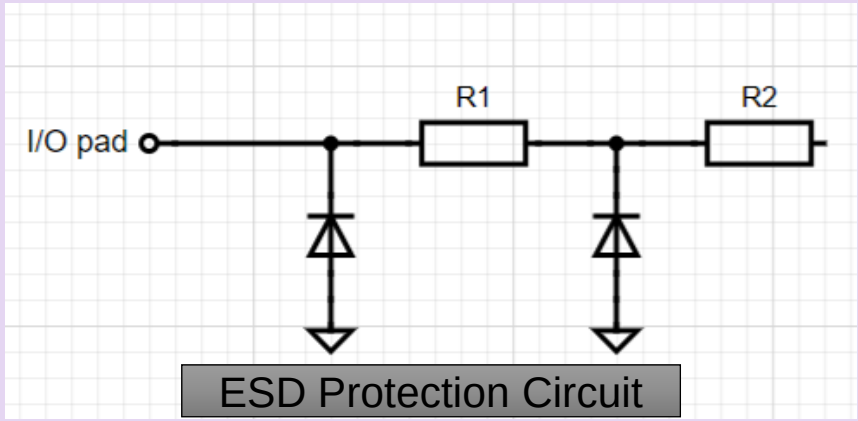


Challenges and Motivation

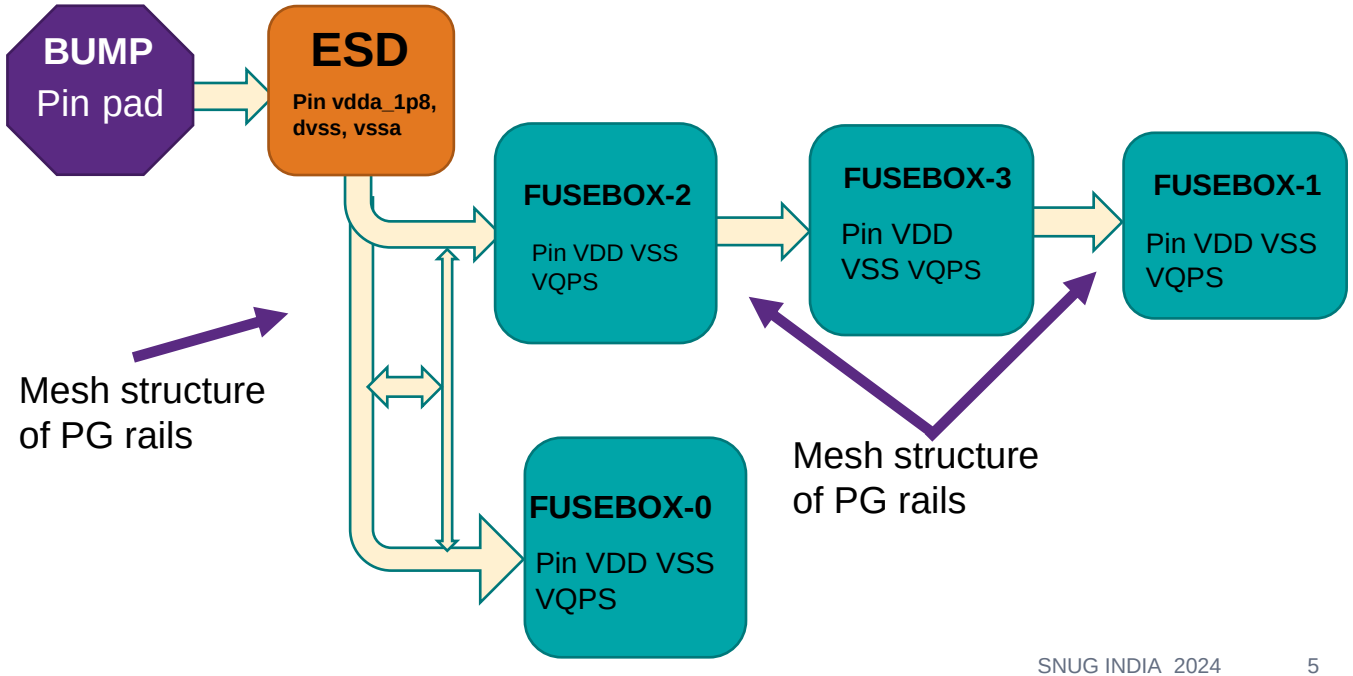
Challenges and Motivation

Calculating point to point resistance

- ESD can generate high peak voltage and current which can damage the IC.
- ESD protection offers less resistive path to these high currents.



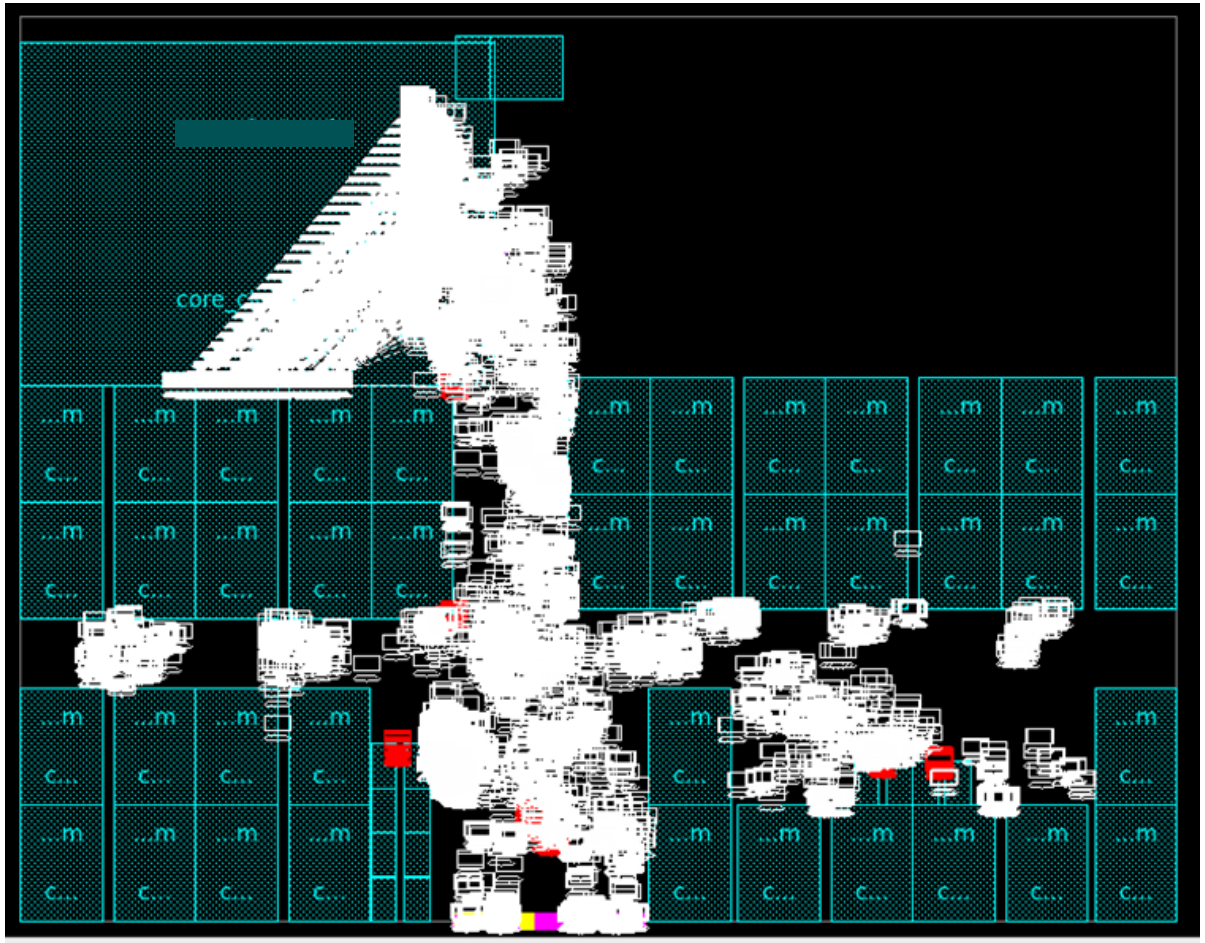
- Manual parasitic calculation of mesh structures like PG rails can be challenging
- Inaccurate calculations of parasitics can lead to design failure



Challenges and Motivation

Analyzing opens and shorts:

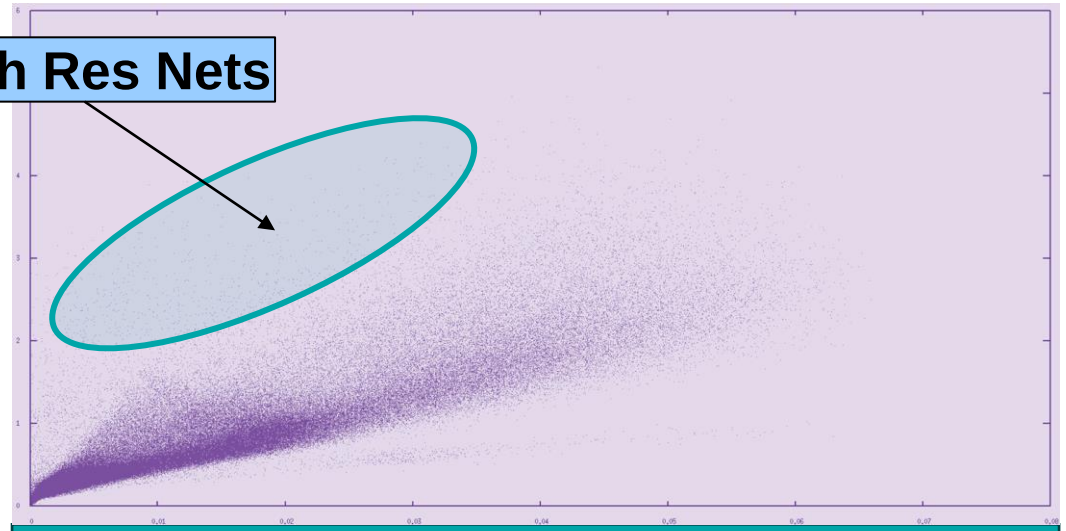
- Opens and shorts in a design can cause critical issues to a design.
- These errors need to be analyzed to ensure the functionality, performance, and reliability of a design.
- Debugging shorts and opens can be challenging without proper annotation.



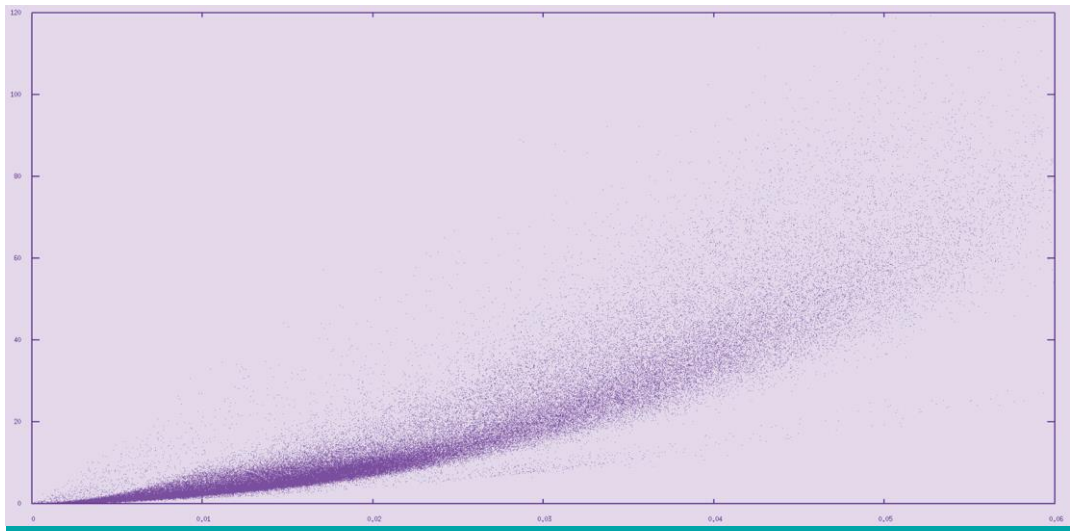
Challenges and Motivation

Identifying high resistance points

- With some conventional approaches, designers can only obtain RC values of specific pins required rather than a general analysis.
- Having all point-to-point resistance values of all pins in a design helps in identifying points with unusually high resistance and the dominant layer.



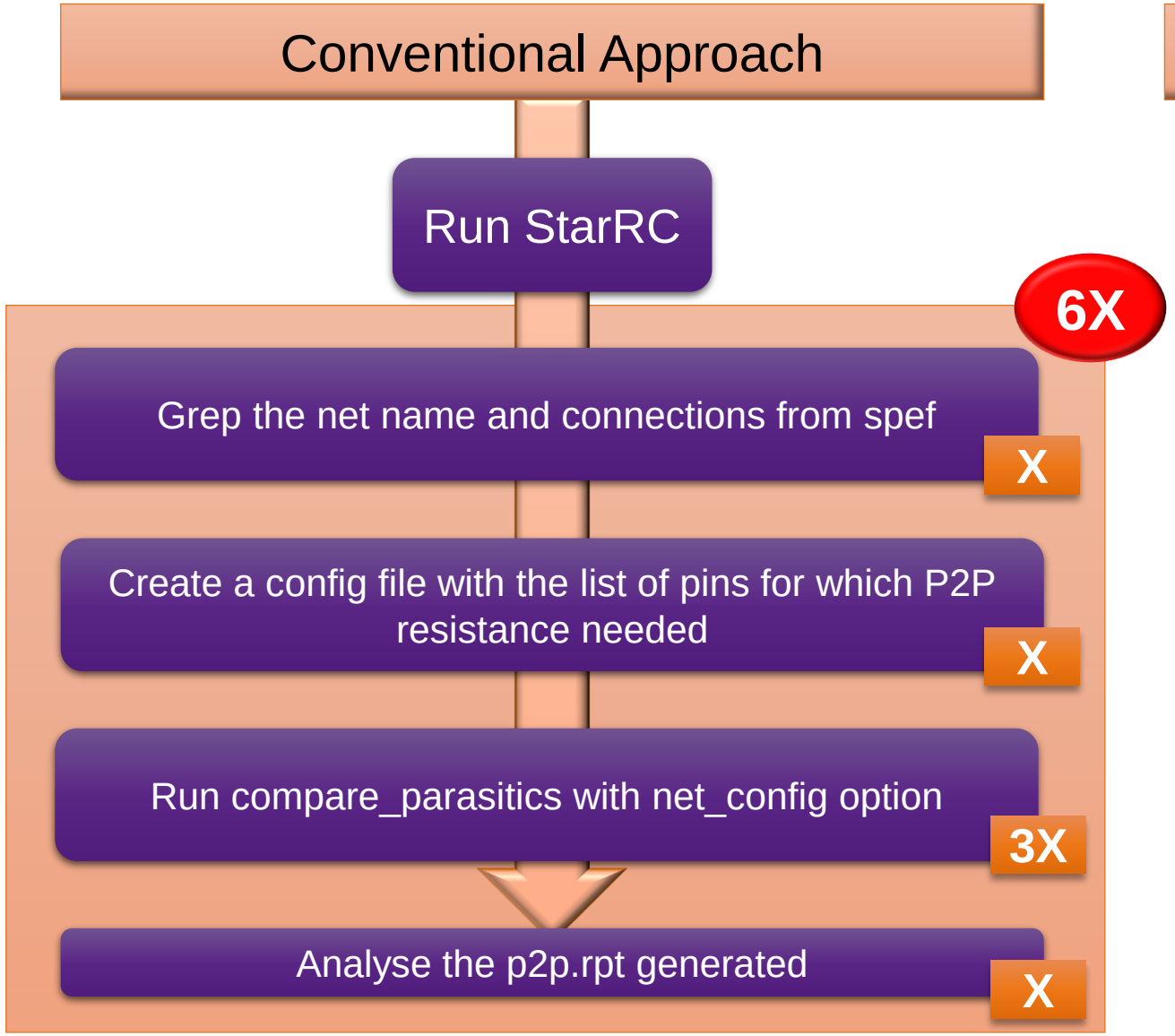
Net P2P Resistance vs. Capacitance

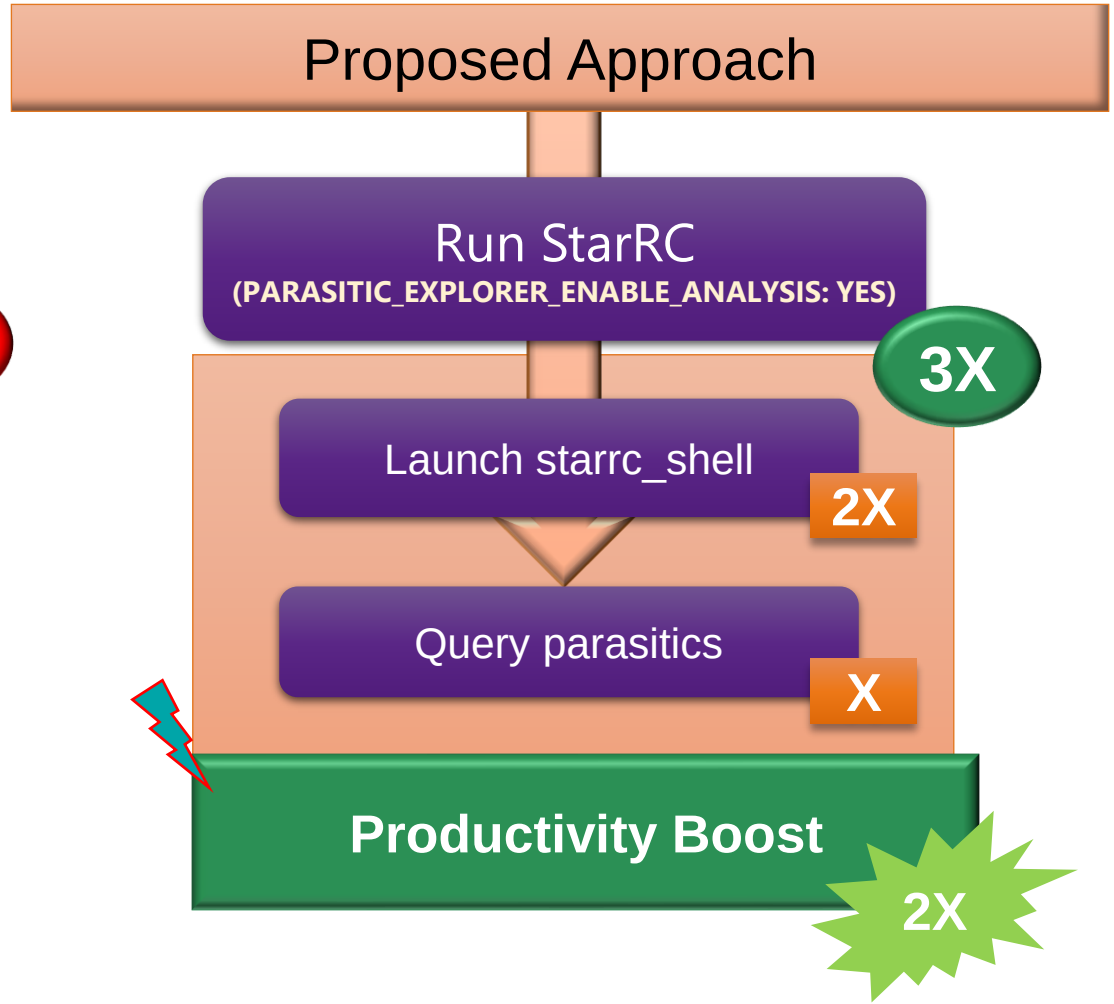


Net Elmore Delay vs. Capacitance

Proposed Approach

Conventional vs Proposed Approach

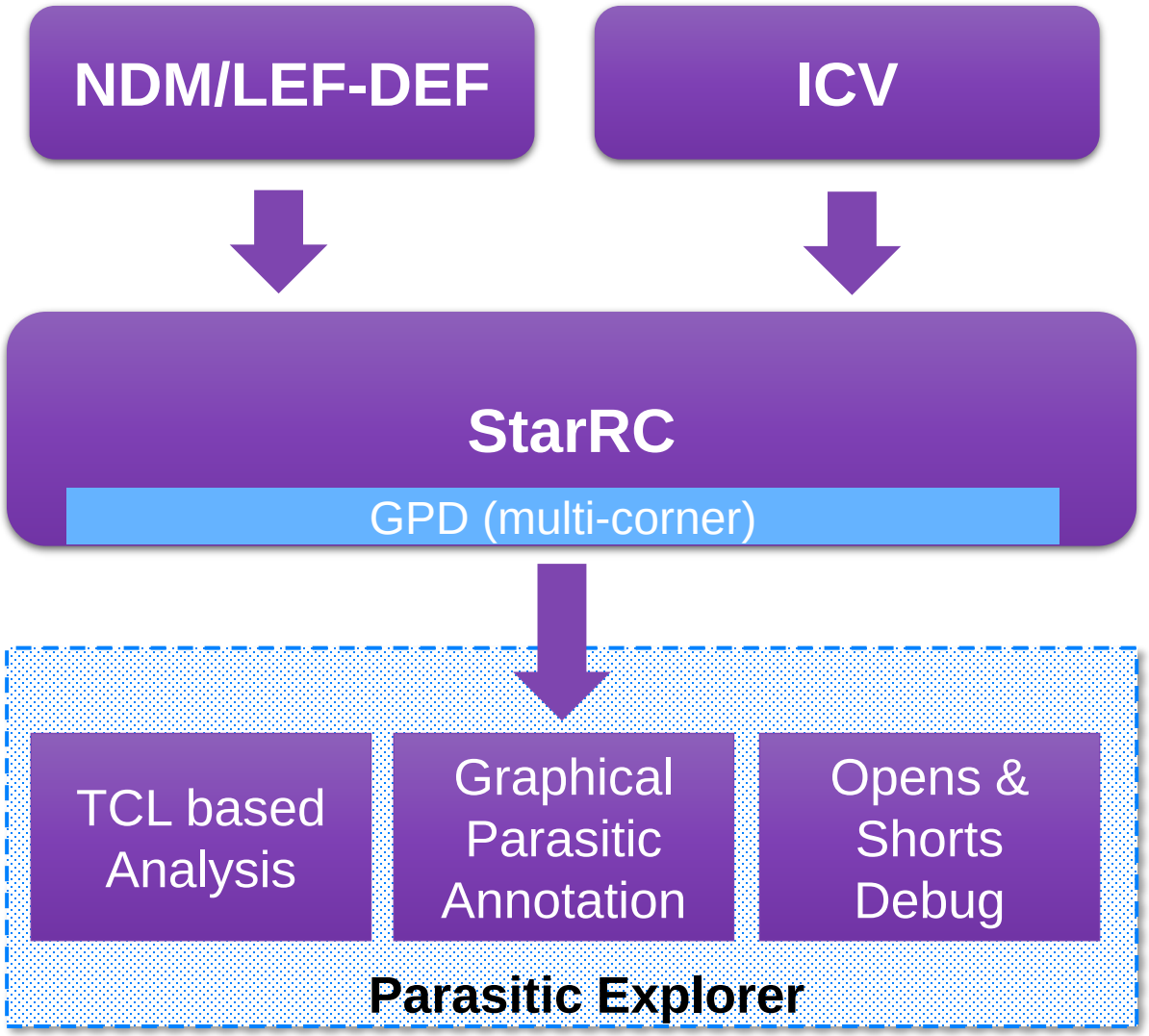




Parasitic Explorer

Introduction

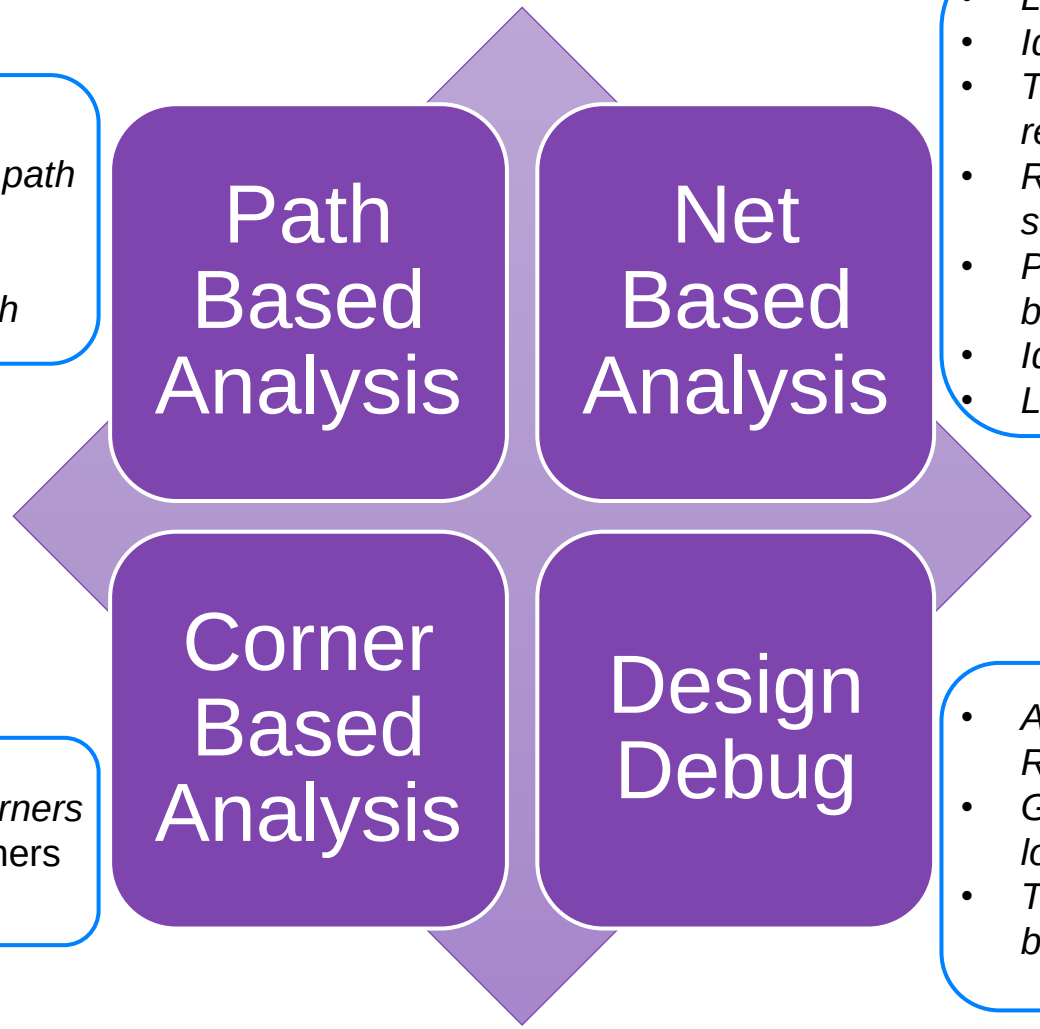
Parasitic Explorer - Introduction



- Advanced Parasitic Analysis environment for Gate and Transistor level flow
- Supports the core Tcl language with Synopsys Tcl extensions
- Graphical environment for Parasitic Annotation and opens and Shorts debug
- Easy to setup: No PDK is required
- Invoked through the command ‘starrc_shell’
- Available in pt_shell as well

Scope of using Parasitic Explorer

Interactive Design Analysis and Exploration



- *Dominant layer in a timing path*
- *Identify nets contributing higher RC on a path*
- Net with dominating RC on a timing path
- *Worst aggressor on a net in timing path*
- *Average aggressor on a net in timing path*

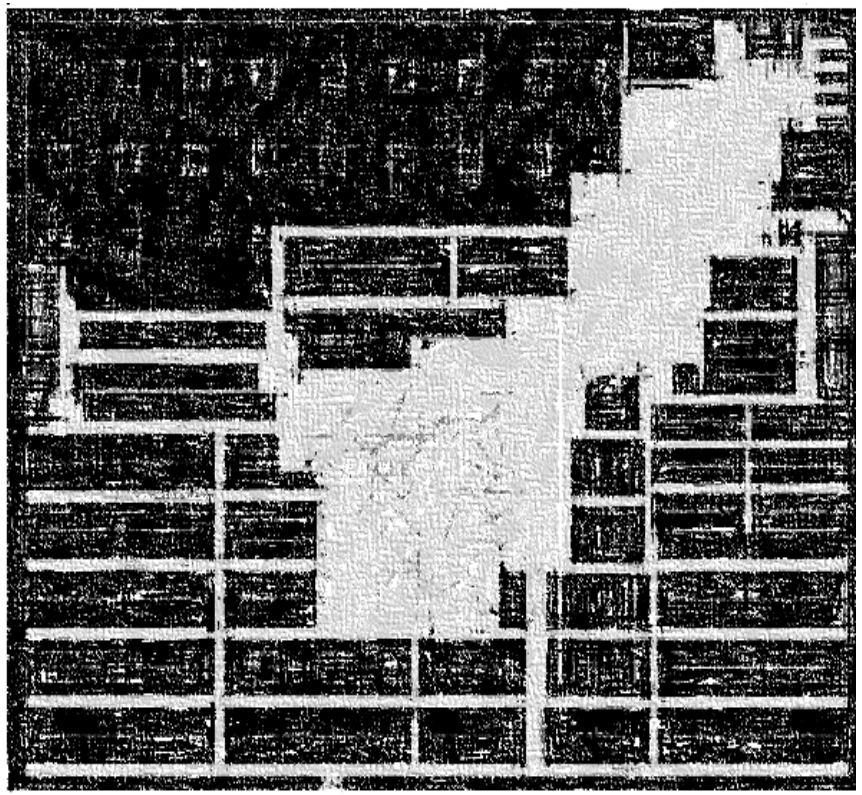
- *Layer wise length distribution of a net*
- *Identify nets routed on top metal layers*
- *Total Cap, Ground Cap, Resistance report*
- *Report width/layer of all resistor segments of a net*
- *Point to point equivalent resistance between driver and receiver*
- *Identify shortest resistive path on a net*
- *List all non-physical resistors for EM*

- *Capacitance variation between specific corners*
- Resistance variation between specific corners

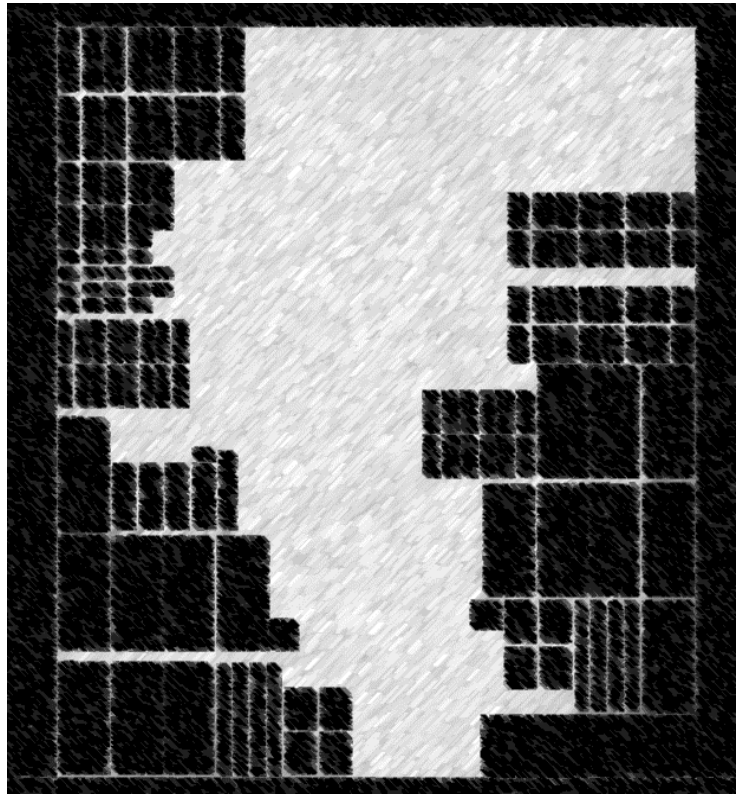
- *Annotate design with RC to visualize RC topology*
- *Get bounding box of a net to know its location*
- *Traverse opens and shorts thru error browser for dirty designs*

Design Under Test

Design Under Test



Design A
Instance count: 1.2M
16nm/10M
Metal track: 7.5T



Design B
Instance count: 8.9M
5nm/13M

Why Parasitic Explorer?

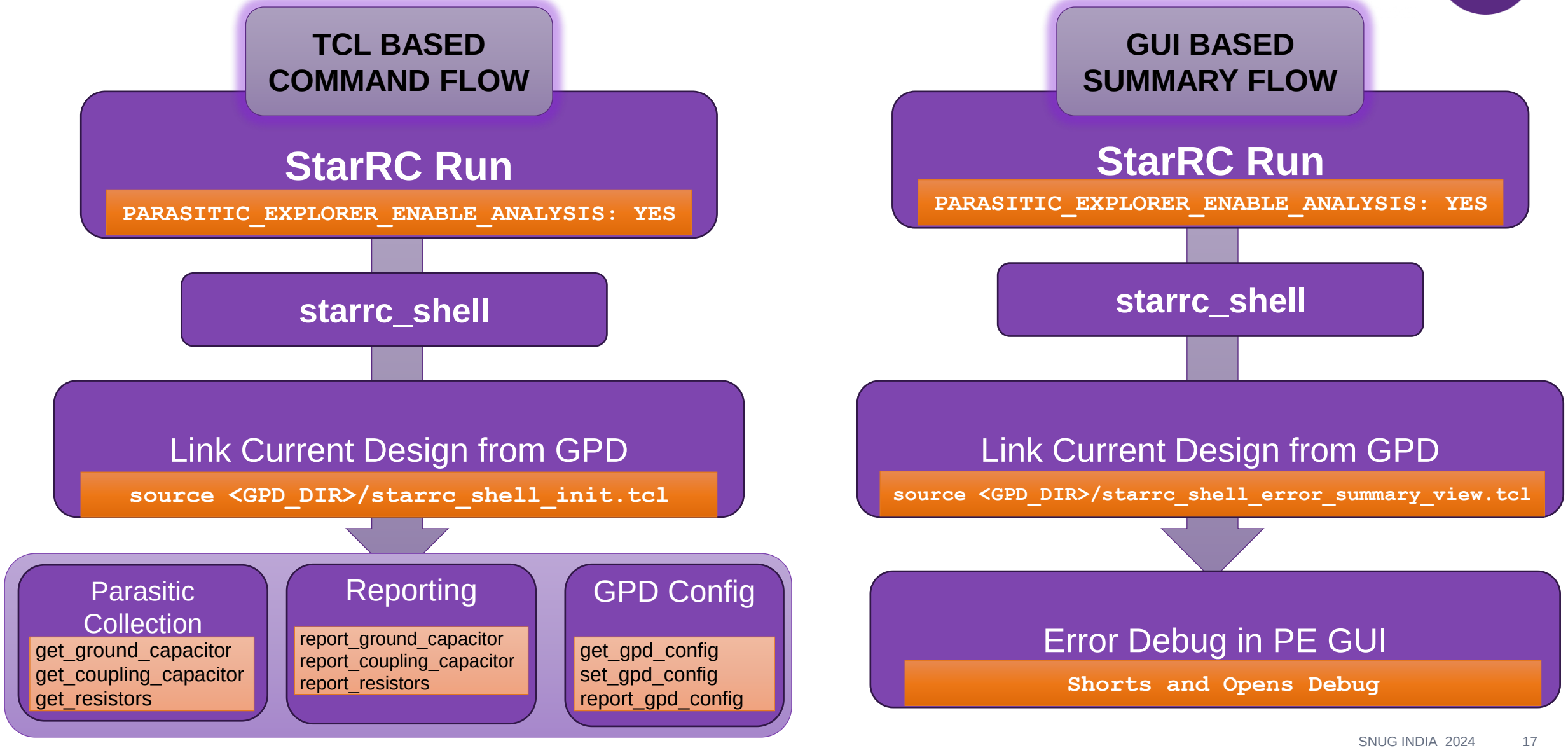
Point-to-point RC values	Layer-wise contribution of RC
• Query all the pin-to-pin resistance values for a given net with a single command. • P2P resistance between any two nodes can be directly calculated.	• Individual RC values and percentage contribution of each metal layer can be calculated for a given path. • Query RC dominant layer in the path.

Designer's Productivity Boost

Ease of Debuggability
Accurate Results
Faster Signoff

Parasitic Explorer Flow and Methodology

Parasitic Explorer Command Based Setup



Results

Results

report_rc_componets

```
starrc_shell> report_rc_components -of_objects sec_msb/n71
*****************************************
Report : RC Components
Design : toprt
Version: V-2023.12-SP4
Date   : Wed Jul 17 18:47:31 2024
Capacitive_load_unit  : 1e-12 Farad
Resistance_unit       : 1000 Ohm
*****************************************

Net              : sec_msb/n71
Total Resistance : 0.076384
Total Capacitance: 0.024688
Layer ResValue %ResContribution CapValue %CapContribution
===== ======== ================ ======== ================
M1    0.009314 12.193653        0.001591 6.444426
M2    0.046862 61.350545        0.021051 85.268146
M3    0.003828 5.011521         0.002046 8.287427
VIA1  0.013500 17.673858        0.000000 0.000000
VIA2  0.002880 3.770423         0.000000 0.000000
```

report_dominant_layer_in_path

```
starrc_shell> report_dominant_layer_in_path -of_objects "n290 n291"
*****************************************
Report : Dominant Layer in Path
Design : toprt
Version: V-2023.12-SP4
Date   : Wed Jul 17 18:59:04 2024
*****************************************

List of nets in specified timing path:
Warning: Nothing implicitly matched 'n290' (SEL-003)
net 1:
Warning: Nothing implicitly matched 'n291' (SEL-003)
net 2:
Total number of nets in the timing path: 2

R dominant layer: M3
Total R on M3: 0.087252

C dominant layer: M3
Total C on M3: 0.045069
```

report_point_to_point_resistance

```
starrc_shell> report_point_to_point_resistance -of_objects sec_msb/n71
*****************************************
Report : report_point_to_point_resistance
Version: V-2023.12-SP4
Date   : Wed Jul 17 19:01:12 2024
Resistance_unit : 1000 Ohm
*****************************************


NET: sec_msb/n71

Pin1                Pin2                 P2P R
====                ====                 =====
sec_msb/cnt_blk1/U31/B sec_msb/U1/A     0.028302
sec_msb/cnt_blk1/U31/B sec_msb/cnt_blk1/reg_blk1/U13/B 0.026487
sec_msb/cnt_blk1/U31/B sec_msb/cnt_blk1/reg_blk1/f0/Q 0.001155
sec_msb/cnt_blk1/U31/B sec_msb/cnt_blk1/U54/A 0.036678
sec_msb/cnt_blk1/U31/B sec_msb/cnt_blk1/U49/A 0.010691
sec_msb/U1/A        sec_msb/cnt_blk1/reg_blk1/U13/B 0.006315
sec_msb/U1/A        sec_msb/cnt_blk1/reg_blk1/f0/Q 0.029457
sec_msb/U1/A        sec_msb/cnt_blk1/U54/A 0.064980
sec_msb/U1/A        sec_msb/cnt_blk1/U49/A 0.038993
sec_msb/cnt_blk1/reg_blk1/U13/B sec_msb/cnt_blk1/reg_blk1/f0/Q 0.027642
sec_msb/cnt_blk1/reg_blk1/U13/B sec_msb/cnt_blk1/U54/A 0.063165
sec_msb/cnt_blk1/reg_blk1/U13/B sec_msb/cnt_blk1/U49/A 0.037178
sec_msb/cnt_blk1/reg_blk1/f0/Q sec_msb/cnt_blk1/U54/A 0.035523
sec_msb/cnt_blk1/reg_blk1/f0/Q sec_msb/cnt_blk1/U49/A 0.009536
sec_msb/cnt_blk1/U54/A sec_msb/cnt_blk1/U49/A 0.030488
```

get_point_to_point_resistance

```
starrc_shell> get_point_to_point_resistance -from sec_msb/cnt_blk1/U54/A -to sec_msb/cnt_blk1/U49/A
0.0304875
```

Results

report_coupling_capacitors

```
starrc_shell> report_coupling_capacitors -of_objects sec_msb/n71
****************************************
Report : Coupling Capacitors summary
Design : toprt
Version: V-2023.12-SP4
Date   : Wed Jul 17 19:12:57 2024
Capacitive_load_unit   : 1e-12 Farad
****************************************

Net : sec_msb/n71
tcap: 0.024688

Total CCAP      %Cc/Ct          Aggressor Net
==========      =====           =============
0.001325        5.366980        sec_msb/cnt_blk1/reg_in[0]
0.001034        4.188270        sec_msb/bcd[1]
0.000570        2.308814        sec_msb/cnt_blk1/n181
```

report_p2p_per_layer

```
starrc_shell> report_p2p_per_layer -from sec_msb/cnt_blk1/reg_blk1/f0/Q -to sec_msb/cnt_blk1/U49/A
****************************************
Report : point to point resistance per layer
Design : toprt
Version: V-2023.12-SP4
Date   : Wed Jul 17 19:15:49 2024
Resistance_unit: 1000 Ohm
****************************************

Net : sec_msb/n71
From: sec_msb/cnt_blk1/reg_blk1/f0/Q
To  : sec_msb/cnt_blk1/U49/A

Layer P2P_R      %P2P_R/Total
===== ========   ============
M1    0.001488   15.607333
M2    0.003547   37.201949
VIA1  0.004500   47.190718
```

Results

Comparing Conventional vs Proposed Approach

P2P resistance obtained with proposed approach

```
starrc_shell> get_point_to_point_resistance -from sec_lsb/conv_blk1/U28/D -to sec_lsb/conv_blk1/U12/X
0.014772
```

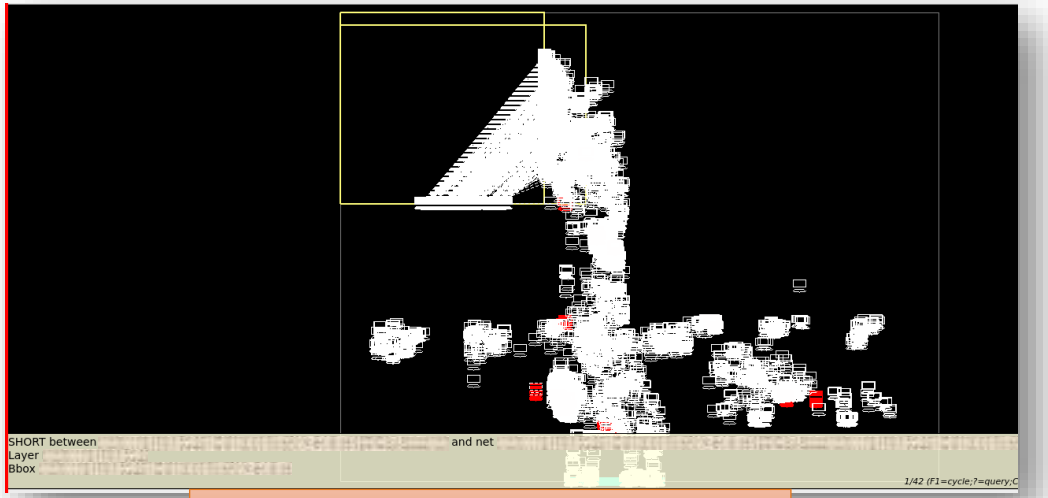
P2P resistance obtained with conventional approach

../toprt_pe.SPEF.typ	../toprt_pe.SPEF.typ	%diff	Netname	Pin1	Pin2
14.772	14.772	0.000	sec_lsb/conv_blk1/n23	sec_lsb/conv_blk1/U28:D	sec_lsb/conv_blk1/U12:X

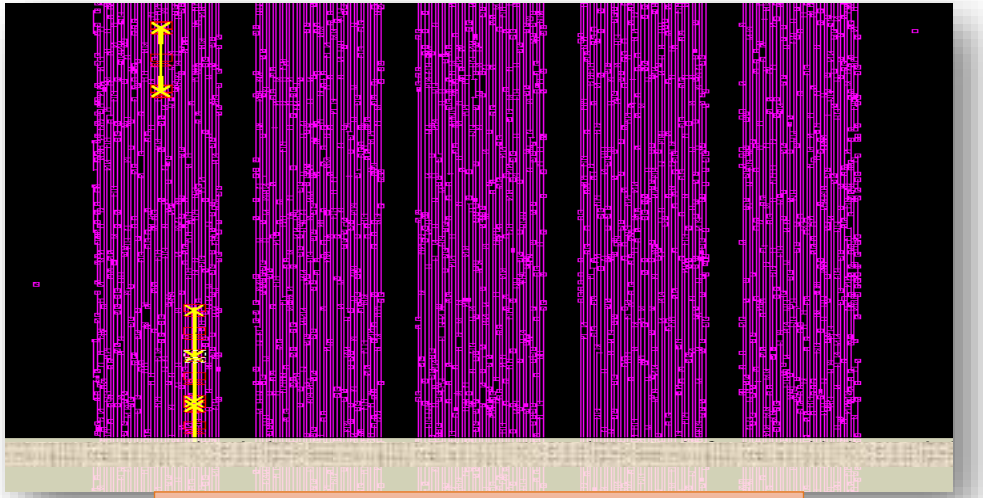
Accurate results obtained with 2X efficiency when using the proposed approach

Results

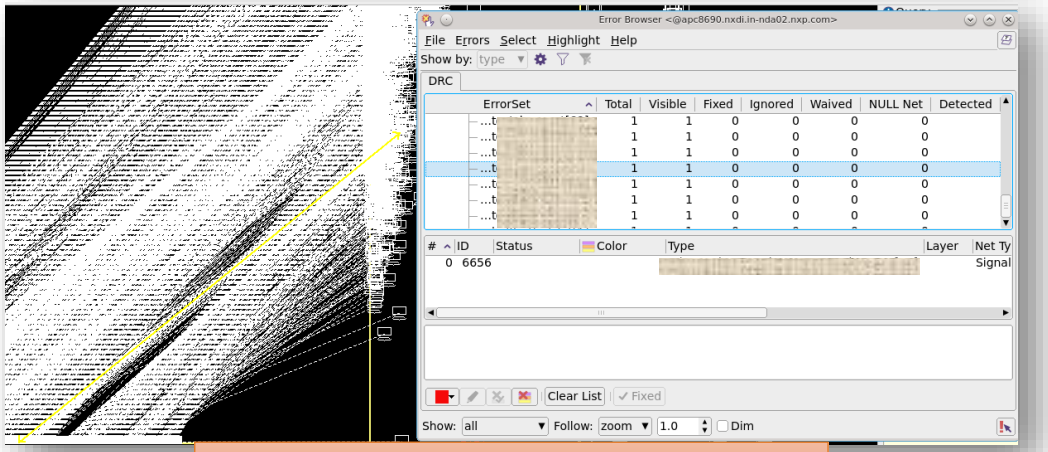
Visualization of Opens and Shorts



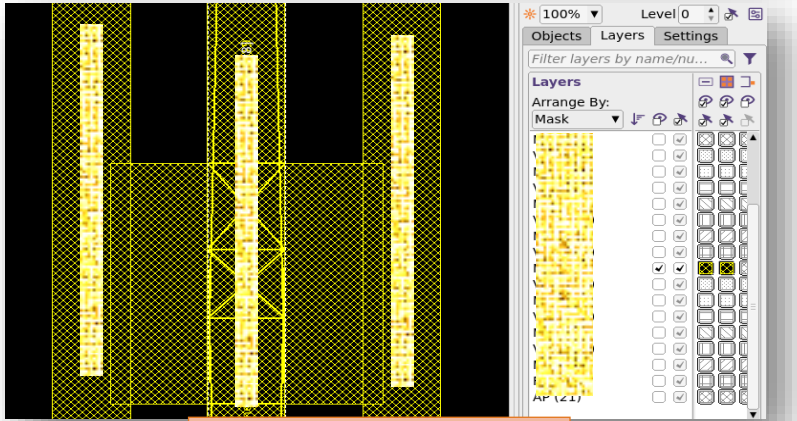
Summary view of Opens and Shorts



Highlighted Shorts using Error Browser



Highlighted Open using Error Browser



Analyzing Short on M7

Unique features

RC Scaler

- RC Scaling is done in PE environment
- Enables what-if analysis
  - without re-running extraction or changing design
  - to reduce IR drop fix iterations
  - while design porting
- RC Scale factor is supported for:
  - Specified NETs
  - Specified P2P pairs
  - Specified layers

1. Use Parasitic Explorer commands to scale parasitics.
   ```
   starrc_shell> scale_parasitics -config config_file
   ```
2. Use Parasitic Explorer commands to write out scaled GPD.
   ```
   starrc_shell> write_parasitics -pe -format gpd test.gpd
   ```

Config_file:

-net_list <net name> -res_factor <res_factor> -cc_factor <cc_factor> -gc_factor <gc_factor>

-net_list <net name> -res_factor <res_factor2> -cc_factor <cc_factor2> -gc_factor <gc_factor2>

-net_list <net name> -from <pin/port/node name> -to <pin/port/node name> -res_factor <res_factor> -cc_factor <cc_factor> -gc_factor <gc_factor>

-layer <layer name> -res_factor <res_factor> -cc_factor <cc_factor> -gc_factor <gc_factor>

-net_list <net name> -layer <layer name> -res_factor <res_factor> -cc_factor <cc_factor> -gc_factor <gc_factor>

Unique Features

starrc_gpd_read_opens_shorts

Usage:

starrc_gpd_read_opens_shorts # Read Opens/Short errors from StarRC, convert to a binary file which can be loaded in non-GUI or GUI Layout->View->Error Browser

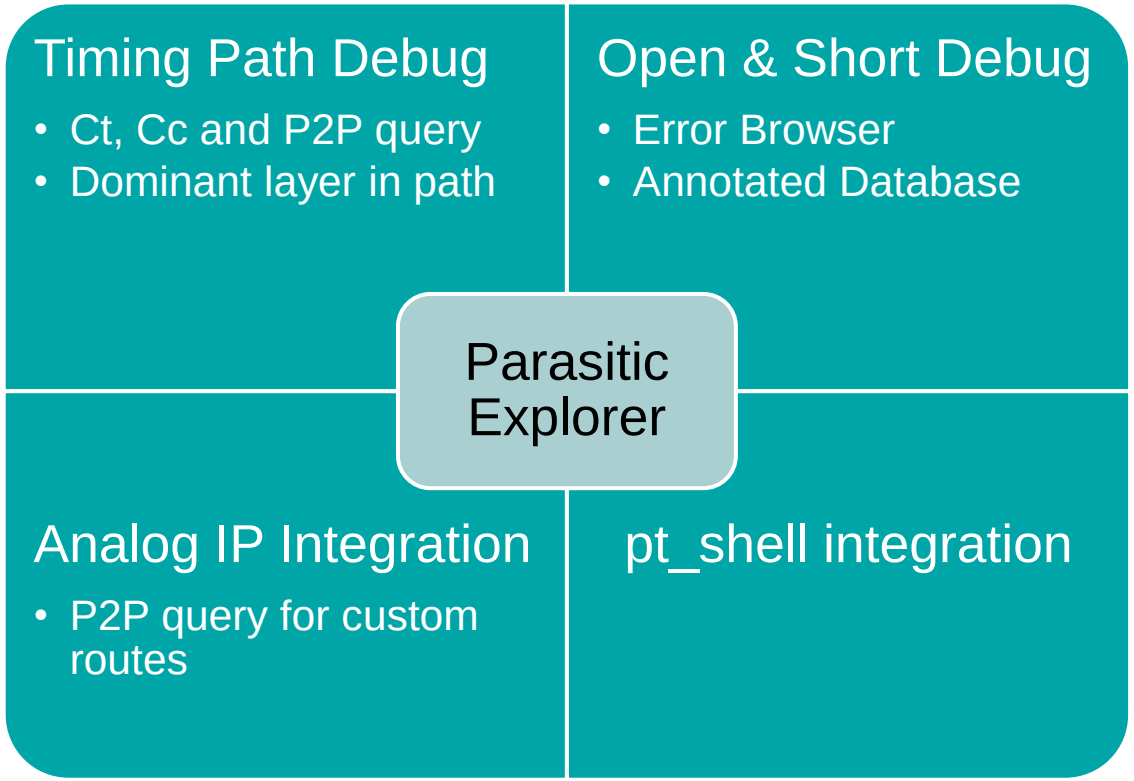
-gpd gpdDir	(GPD directory for the design)
[-error_file errorFile]	(File name that stores the error database (default starrc_openshort.err))
[-window window]	(Window (bounding box) for which open or short to be displayed)
[-type type]	(Type of violation: open/short/all (default)))
[-limit limit]	(Total number of errors to be shown for each type)
[-add_gui_selection]	(Highlight the affected net(s) in the GUI)
[-add_net_attributes addNetPar]	(Add attributes to net (append, replace (default)))
[-nets nets]	(List of net names for which open/shorts are to be shown)
[-summary_view]	(Brief visualization of all errors)
[-warning_limit warning_limit]	(Total number of warnings to be shown for each type)
[-short_types short_types]	(List of space-separated short types (net unselectable power fill-blockage nonselected skip_cell fill blockage) for which shorts are to be shown)

- Multiple error reports can be dumped and loaded in layout view for analysis
- Specific areas in the design can be selected for debugging

Conclusion and Future Scope

Conclusion

- Getting accurate P2P resistance values is critical when doing custom routing for integration of analog IPs, matching RC specs with respect to IP Integration guidelines
- Large RC parasitics can also lead to timing violations in critical path.
- Design complexity ↑ → Debugging Time ↑
- Achieved 2x productivity boost in addressing critical signoff issues
- Consequently, PE expedites design closures and enhances the turnaround time (TAT) of the overall design cycle



Future Scope

- Parasitic Explorer can be used to do early estimation of timing violations by looking into the parasitic profile of the design.
- RC Scalar can be used to do what-if analysis of parasitics before moving to newer technology nodes.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