A Novel STA Signoff Methodology for MultiTech 3DIC Systems

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Motivation and Proposed Solution

Motivation

- An accurate and efficient STA signoff methodology for cross die and MultiTech 3DIC systems.
- Planning and implementation of PVT to limit the risks of Vmin surge and hold robustness on SI.
- Accurate delay computation of cross die nets with bump physical redundancy.

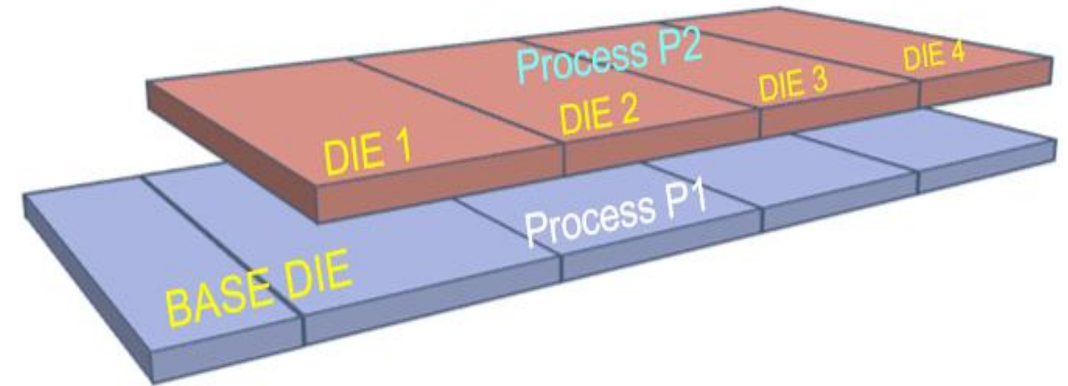

Figure 1 : Vertical stacking of dies

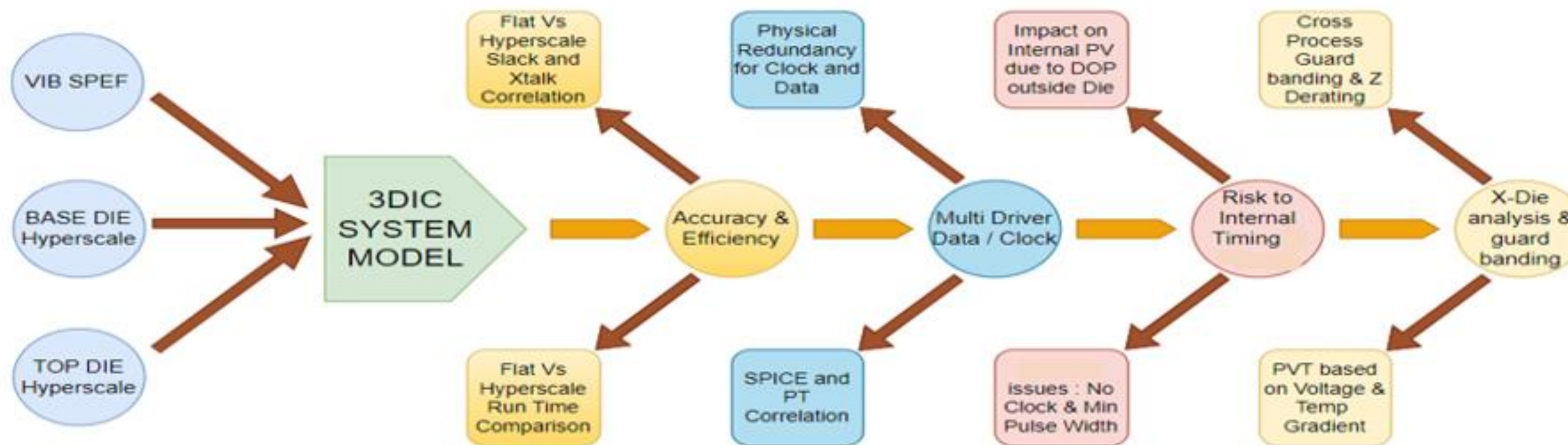

Figure 2 : Pillars of proposed STA methodology highlighting issues

Proposed Solution

- Custom abstraction techniques for addressing internal cones impacted by cross-die clock divergence, latch and high fanout abstraction improvements
- Efficient recognition of D2D cones for various Quality checks signoff
- Various aspects of multi-driver bump modelling and PT delay calculation risks reduced with RTL and spice modelling updates
- Dummy fill mechanism for intra die coupling in top metal and VIB spef for inter die coupling capacitances.
- PVT, derate planning and clock period guard banding for Voltage and temperature gradients.

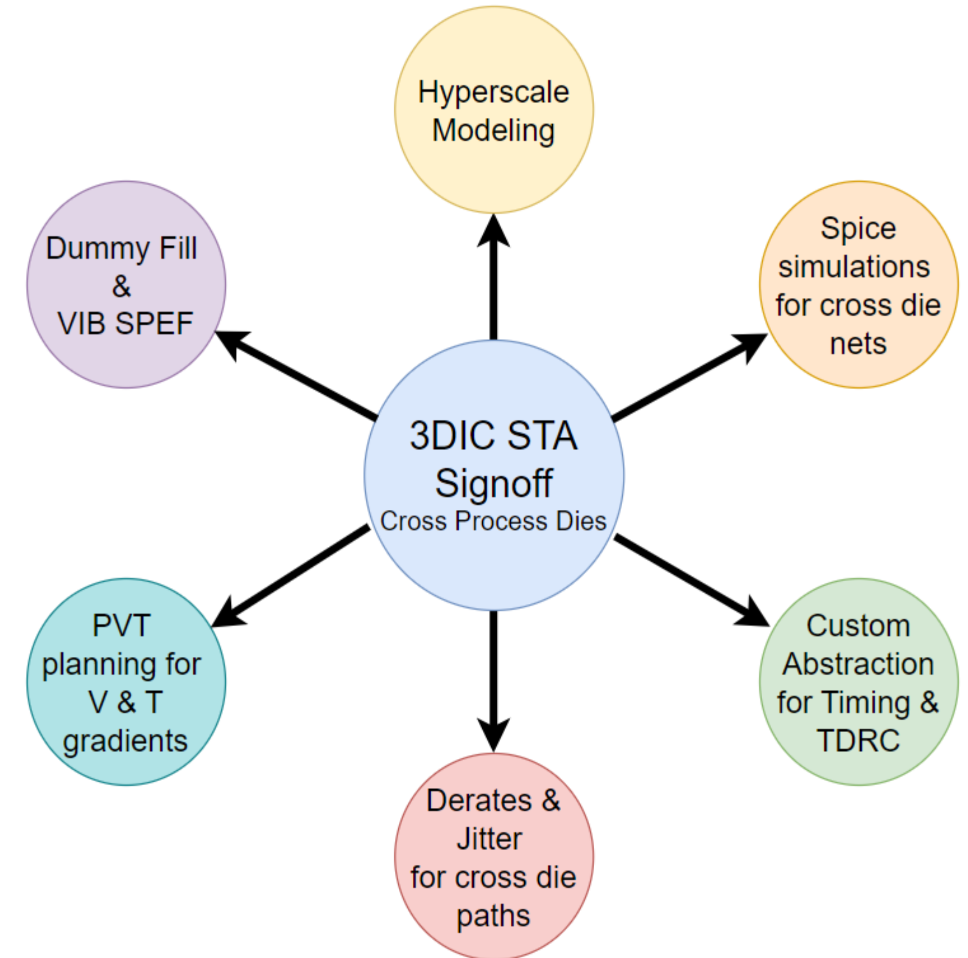

Figure 3 : Proposed STA methodology

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Modeling STA signoff using proposed methodology & Results

Design Modeling with nested hyperscale

- Custom hyperscale approach employed to model critical internal paths susceptible to cross die effects
- Nested hyperscale approach utilized to model partitions internal to individual dies.
- Intra die logic which was clocked with two separate clock ports are preserved in hyperscale for intra die analysis at system level using set_pin_abstraction commands
- Clock nets under a reasonable threshold of MPW budget were preserved in hyperscale for proper analysis at system level.

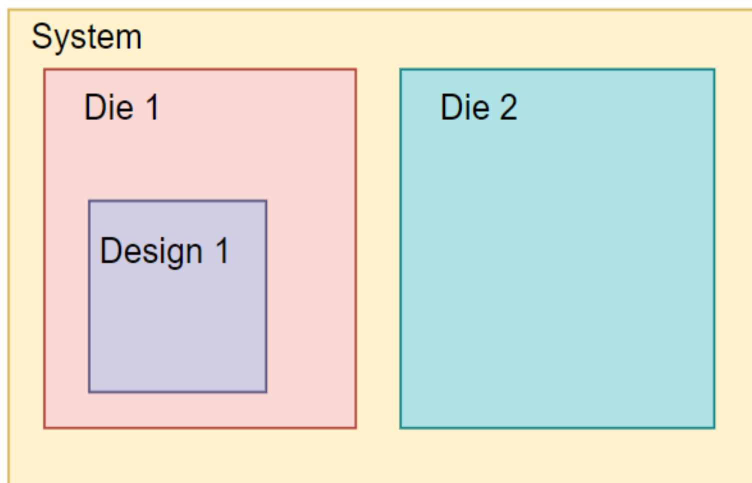

Figure 4 : Nested HS modeling approach

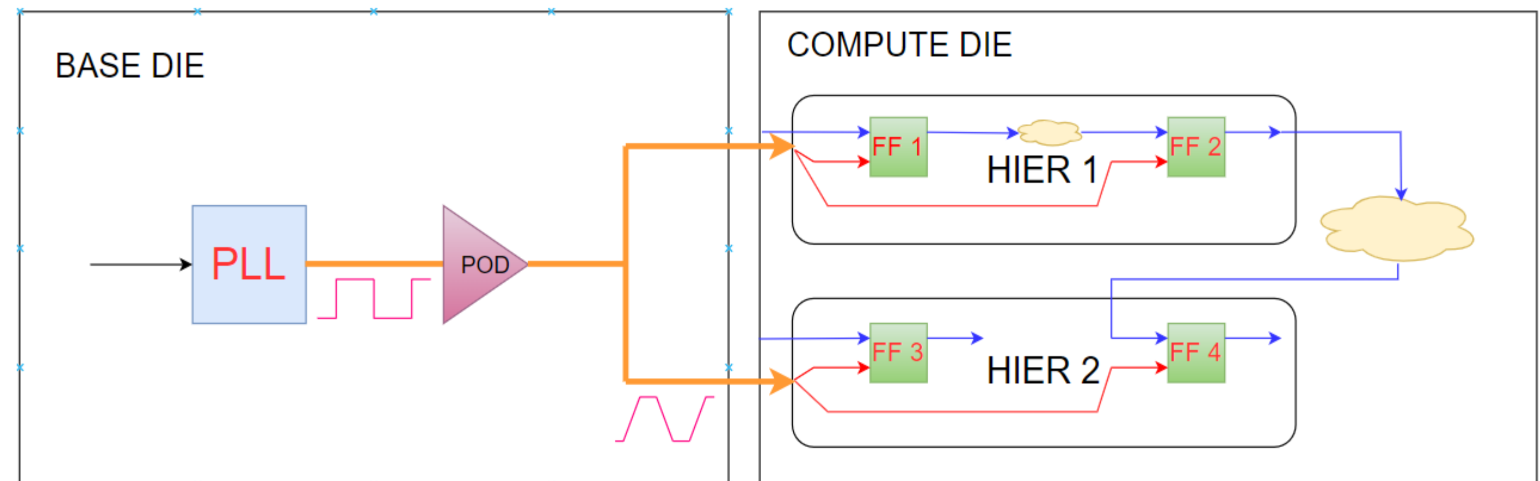

Figure 5 : Internal timing impact due to outside Clock POD

Design Modeling with nested hyperscale (cont.)

- Latch abstraction options modified to ensure full transparency of timing paths from a 2.5D DIE input to a 3D topmost die capture point.
- D2D cone recognition methodology was enhanced for quality check_timing, max_transition and max_capacitance sign off
- Logic preserved internally were analyzed for waivers using scripts and e-star for possible tool updates as shown below

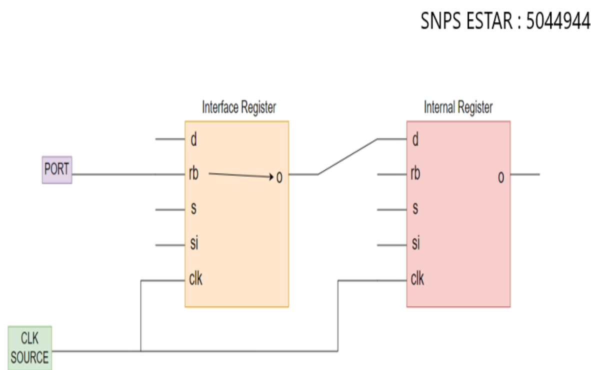

Figure 6 : Reset arc propagation

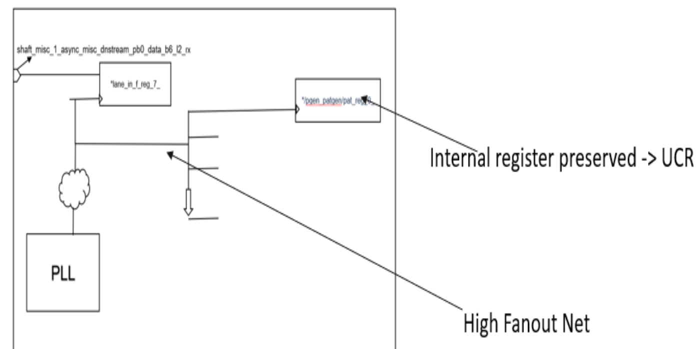

Figure 7 : Missing HS stub due to unbuffered CTS

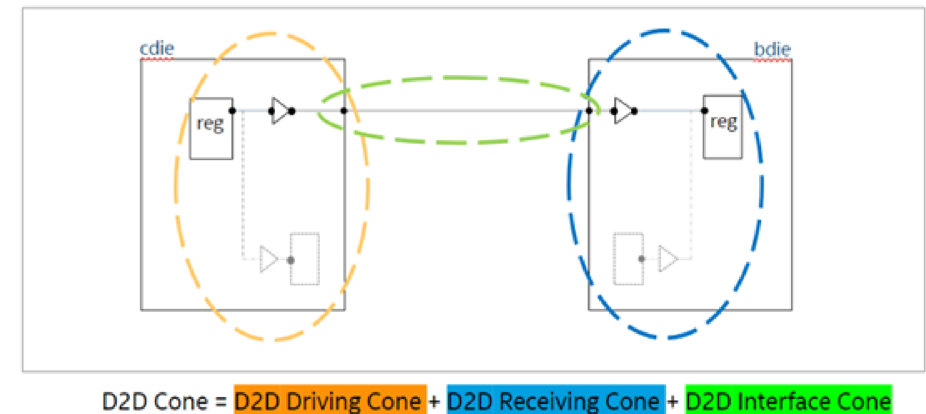

Figure 8 : Representation of D2D cone in a cross-die scenario

Parasitic Modeling

- Vertically stacked dies can lead to significant coupling capacitance between nets routed in adjacent layers of individual dies.
- Coupling capacitance can induce significant crosstalk, impacting timing convergence.
- Intra die parasitic extraction implemented using STARRC VMF Fill flow, mimicking top metal polygons.
- Inter die parasitic extraction implemented using 3DIC STARRC VIB spef, for coupling capacitances.
- Dummy spef for completing missing parasitic components of nets routed in top metals.

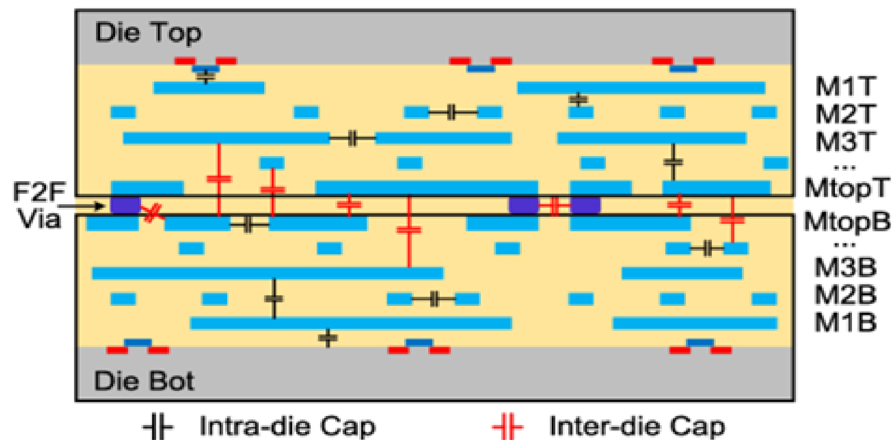

Figure 9 : Intra and Inter die capacitance across dies

```
****************************************************
Report  : read_parasitics snps_temp_file.spef
   -keep_capacitive_coupling
Design  : soc
Version: U-2022.12-SP5-1-VAL-20231222
Date    : Tue Apr 16 12:24:55 2024
****************************************************
```

Figure 10 : VIB spef for coupling and dummy spef for completion

Parasitic & Timing Model Accuracy

- Coupling capacitance of magnitude ~0.05 fF for inter die nets and ~4.5 fF for top metal intra die nets are observed.
- High correlation between Flat and custom hyperscale modeling as compared to Flat vs default hyperscale modeling approach ~ 80 % accuracy increase for internal paths

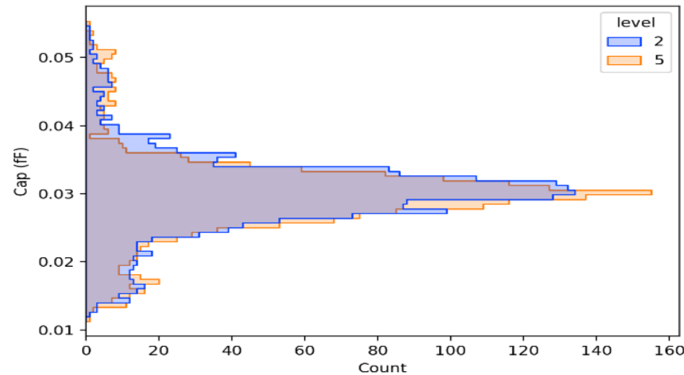

Figure 11 : VIB spef coupling capacitance histogram

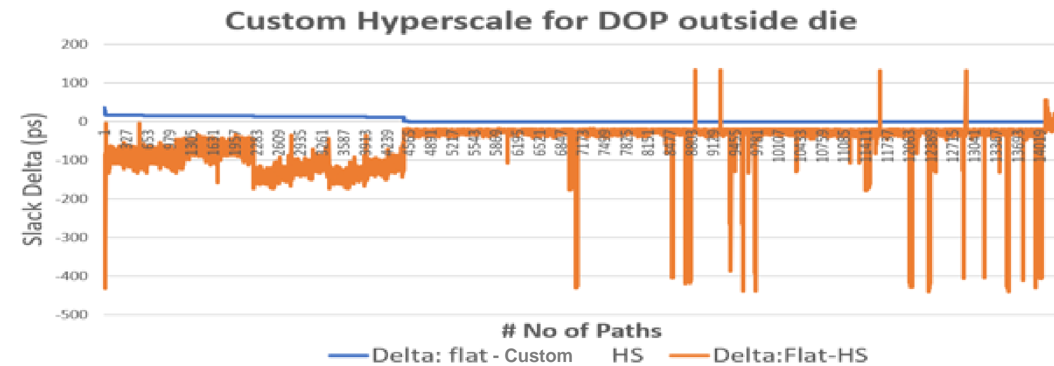

Figure 13 : Default vs Custom HS timing slacks comparison with Flat

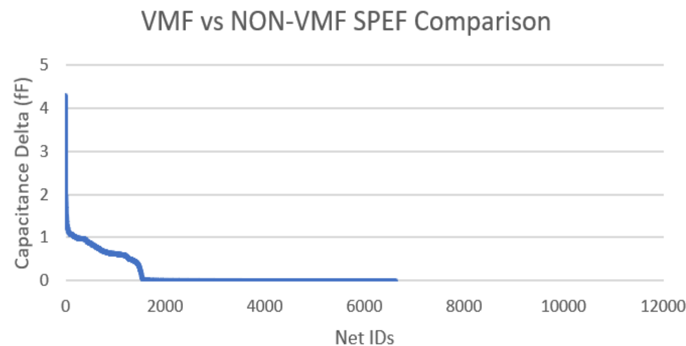

Figure 12 : VMF vs non – VMF SPEF comparison

StartClock	EndClock	Total Paths	Outliers	% outliers	Max Delta (ps)
hfclock1	hfclock1	35584	0	0	0.01
hfclock2	hfclock2	35584	0	0	0.5
hfclock3	hfclock3	1088	27	2.48	1.85
mfclock1	mfclock1	34086	1022	2.99	7.88
mfclock2	mfclock2	832	0	0	7.14
mfclock3	mfclock3	832	0	0	7.14

Figure 14 : Flat vs HS interface timing correlation

Mutli Driver Nets Delay Modeling

- Vertically stacked dies are prone to manufacturing defects leading to damaged cross die connectivity.
- Single IP driving multiple physical bumps (SDMN) is general MPIN case. Final observation came out to be non-MPIN due to dedicated shorting IP implemented with multiple net implementation in RTL
- Multi IPs driving same net (MDSN) lead to interface net delay delta between detailed RC extraction in PT and spice because of tool limitation of modeling accurate driver model.

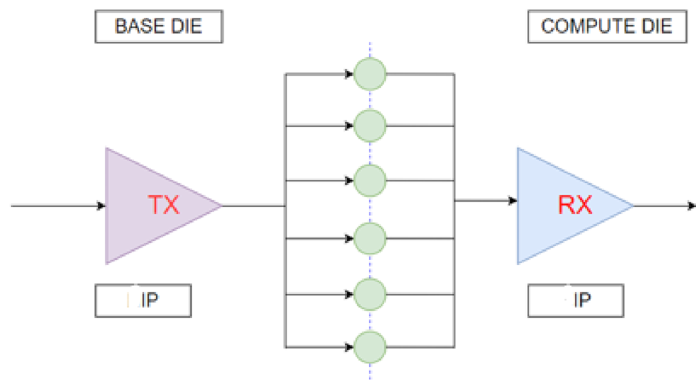

Figure 15 : SDMN implementation with 6 bump redundancy

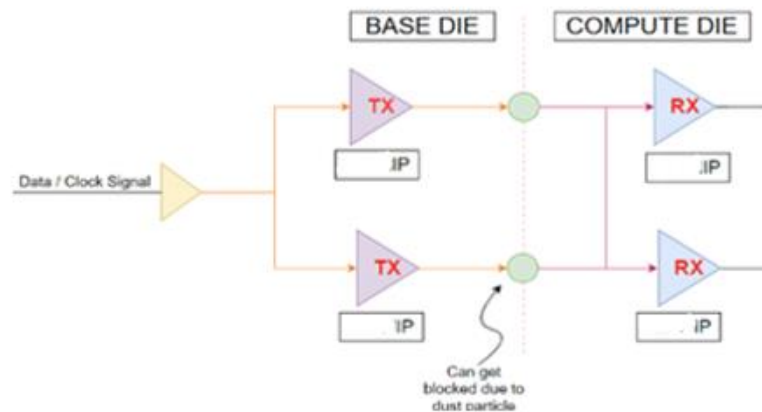

Figure 16 : MDSN implementation with 2 bump redundancy

Mutli Driver Nets Delay Modeling (contd.)

- PT perform lumped RC delay calculation when a single net does not driver all the multiple drivers of a MDSN topology. Traditional warning message is as below -

```
******************************************
Report: delay_calculation
Design: cbb32x4c
Version: U-2022.12-SP5-3-VAL-20240523
Date: Tue Jan 16 01:20:53 2024
******************************************
Warning: The net ‘hier1/die2die’ controls only a subset of the drivers of multidriven net
‘hier1/die2die2’ so detailed RC delay calculation cannot be used. (RC – 002)
RC delay calculation is being skipped because the from-net does not cover all of the drivers of the
multidriven net.
```

Figure 17 : PT warning for lumped RC calculation for MDSN segments

- Shorting the multi drivers using single buffer helps PT perform detailed RC delay calculation for MDSN topology.
- Minimizing skew between multiple drivers helps increase MDSN modeling accuracy.
- ~80 ps delta seen between lumped and detailed RC calculation on the MDSN segment on a high-speed cross die interface.
- Spice correlation showed delay calculation accuracy within < 10ps with PT.

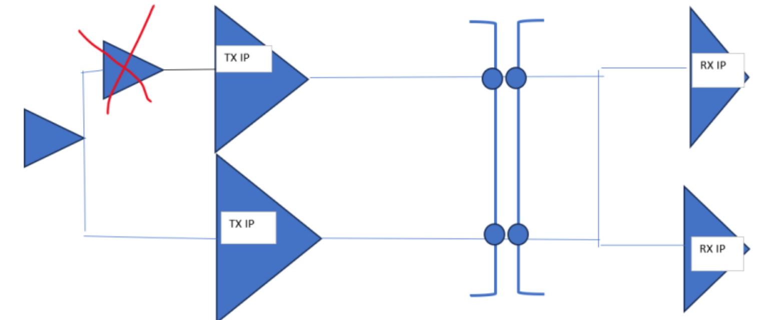

Figure 18 : RTL modification for detailed RC calculation

Spice results & Delay Accuracy

- Multi driver nets delay calculation by tool differs the spice delay numbers by ~ 5 ps, modelled as added penalty for interface paths.
- In case of defect, single bump configuration need modelling with extra delay of ~8 ps compared to two bump structure.

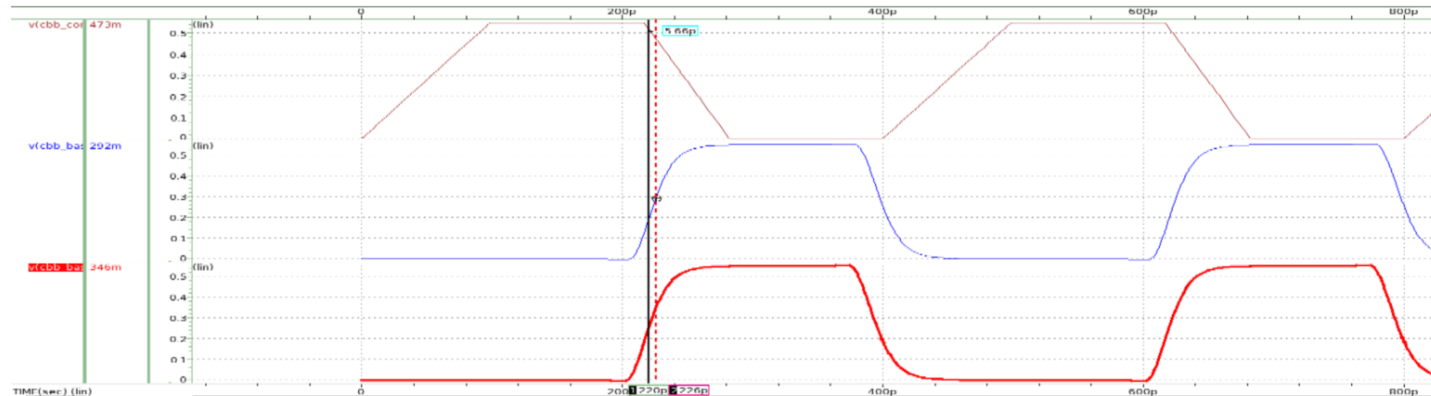

Figure 19 : SPICE simulation waveforms for SDMN architecture

Schematic components	Primetime		Spice		Delta	
	Transition	Delay	Transition	Delay	Transition	Delta
short_buf/a	59.3	0	59.2	0	0.1	0
short_buf/o	97.3	68.2	101.2	69.98	-3.9	-1.78
tx_hip/a	102.2	10.55	106.3	11.03	-4.1	-0.48
tx_hip/o	22.5	52.44	22.55	55.13	-0.05	-2.69
rx_hip/a	22.3	-0.055	22.51	0.0475	-0.21	-0.1025
Total		131.135		136.1875		-5.0525

Figure 20 : SPICE vs PT correlation & delay penalty

Schematic components	2 Bump Redundancy		1 Bump Connected		Delta	
	Transition	Delay	Transition	Delay	Transition	Delta
short_buf/a	59.2	0	59.2	0	0	0
short_buf/o	101.2	69.98	102.6	69.98	-1.4	0
tx_hip/a	106.3	11.03	106.5	11.03	-0.2	0
tx_hip/o	22.55	55.13	12.32	39.67	10.23	15.46
rx_hip/a	22.51	0.0475	21.57	23.02	0.94	-22.9725
rx_hip/o	20.56	35.93	20.59	36.03	-0.03	-0.1
Total		172.1175		179.73		-7.6125

Figure 21 : 2 Bump vs 1 Bump delay penalty

Constraints Modeling

- A dedicated clocking approach utilized at system level to constraint the system interface paths.
- Clock periods are aligned with the faster die to incorporate cross process scaling, including the added guard bands for jitter and PV2SI correlation.
- Different uncertainties are employed at system incorporating the duty cycle distortion calculation for phase paths.
- RTL coded exceptions (refresh using context) and global topologies constraints (TAP/SCAN..) are promoted to system level using fishtail / custom promotion methodologies.

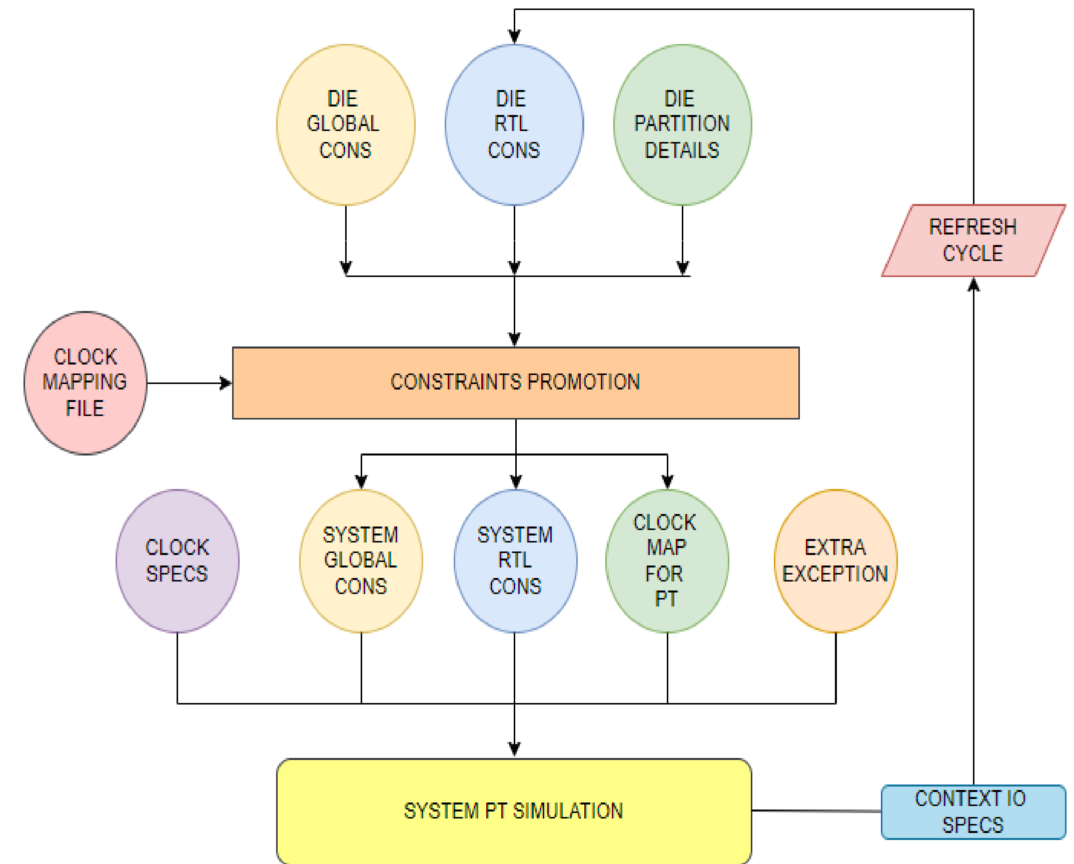

Figure 22 : Clock Mapping and Constraints Promotion Flow

PVT & Derate Modeling

- We observed significant voltage and temperature gradient between base and top die due to IR drop in PDN, different work loads and different process.
- New dedicated cross voltage and temperature corners are defined for hold closure incorporating these gradients.
- Base driving Vmin post fab, Base (fast) -> Top (slow) scenario is controlled by tighter CTs at top die. Base (slow) and Top (fast) is already covered.
- System is modelled with tighter CTs and helped aligning top die windows for accurate SI analysis. Extra uncertainty employed for possible mismatch between base and system windows.

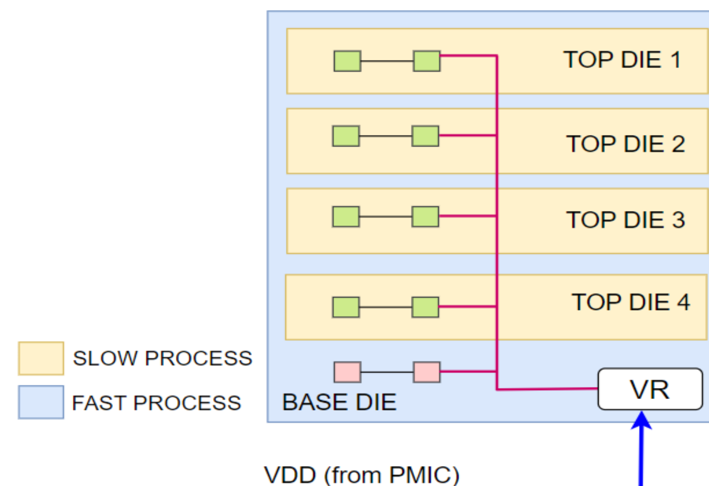

Figure 23 : VDD supply and Voltage regulator placement

Spatial Derate Modeling

- Side file approach used to model distance derate with manual transformation switched on.

  set_app_var read_parasitics_load_locations true

- Cross die introduces additional VT mistrack derates for modeling variation on one VT type across dies. Enumeration technique used to reduce extra pessimism for cells residing in same die having same VTs.

  set vt_mistracking_analysis_mode enumeration

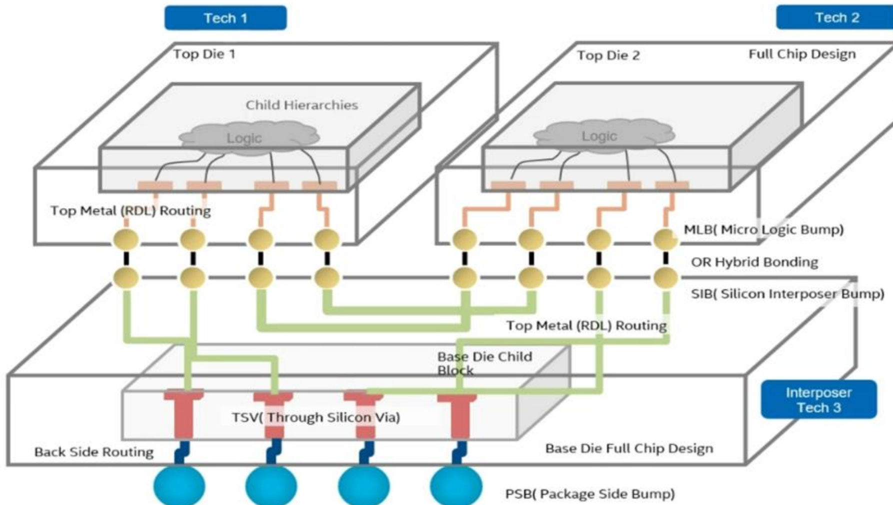

Figure 24 : Vertically stacked dies

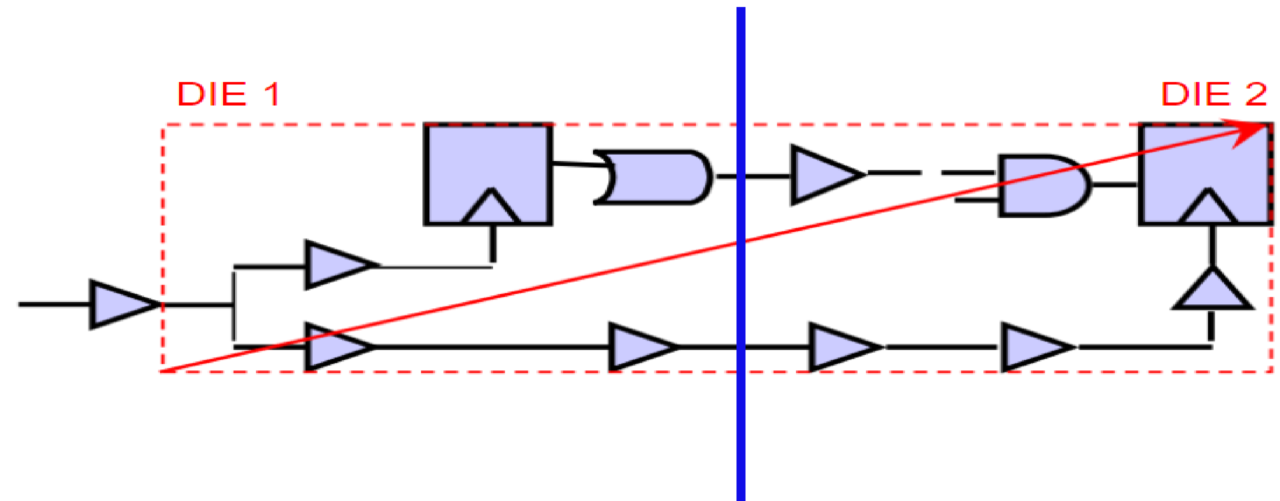

Figure 25 : Bounding box for PBA Cross Die path

Summary / Future Plans

Conclusion & Future Plans

- Custom hyperscale showed marginal decrease in overall abstraction of ~4 % and increase in run time of ~15 minutes, whereas increasing accuracy by ~80 % for intra die timing with POD outside die.
- Spice simulation MOW and penalty addition in tool, helped to achieve utmost accuracy for physically redundant multi driver nets.
- Many discussions are in progress with SNPS R&D team regarding bug fix updates in upcoming tool releases. It also includes enablement of Simultaneous Multi Corner (SMC) tool for corner reduction.

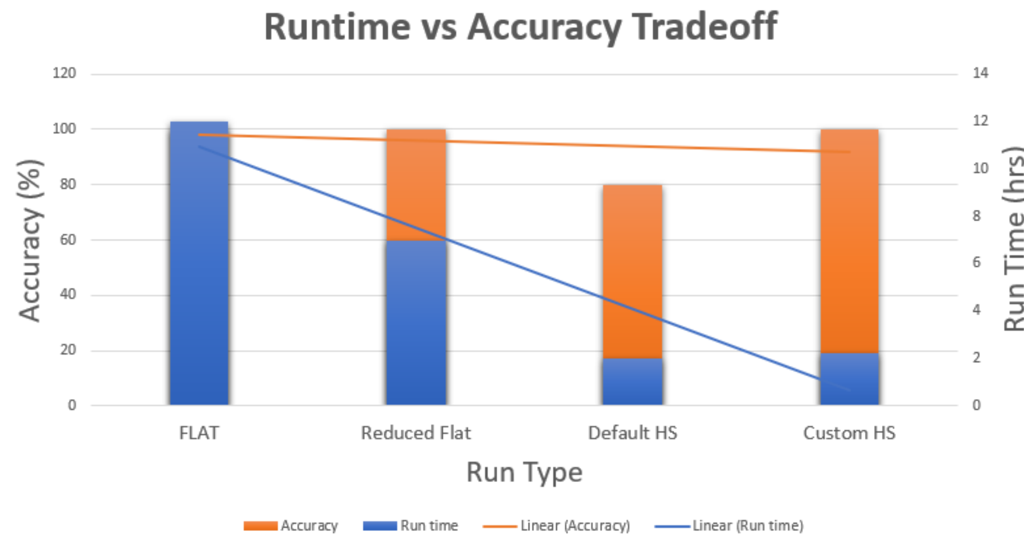

Figure 26 : Flat vs Custom HS vs Default HS Comparison

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