Navigating Extraction and Timing Closure in Multi-Die System - A Signoff Methodology

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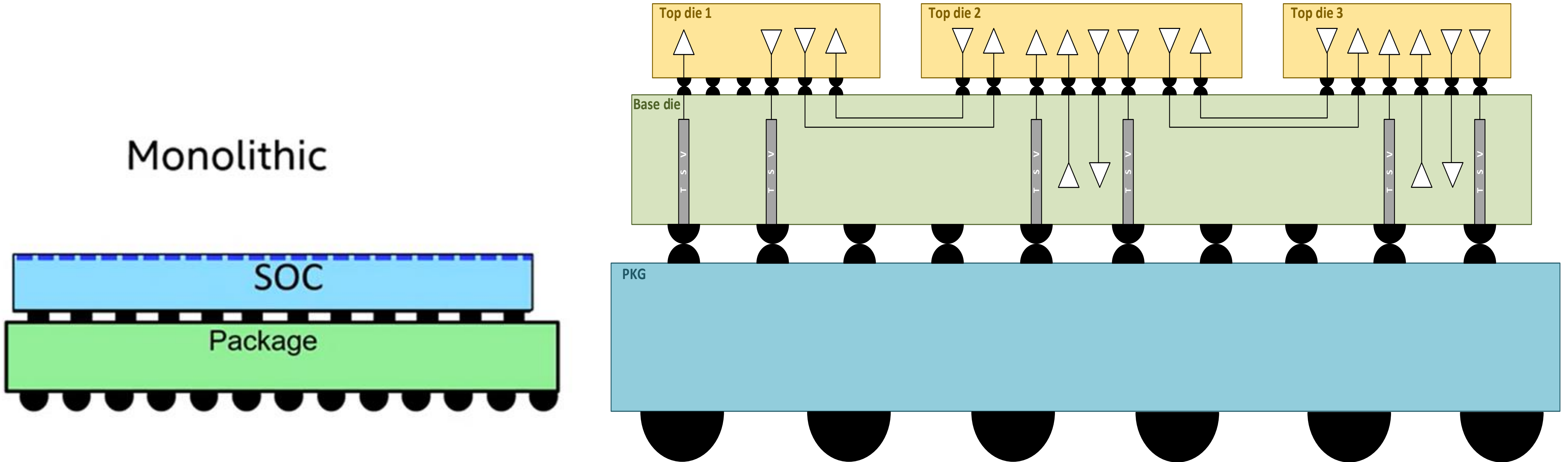
Agenda

- Multi-Die Systems
  - Types
  - Factors driving Multi-Die Systems
  - Basic Terminologies
- Extraction
  - 3DIC StarRC Flow
  - Need for Multi-Die modelling in RC
  - Virtual Interface Block
  - Outputs and Results
- Timing
  - Requirements for 3DIC STA Signoff Methodology
  - Building 3DIC STA environment
  - Performance comparison of Hyperscale v/s Flat
  - Hyperscale model validation
  - Derate Modelling and Parasitic annotation
  - Conclusion and Future Work

Rise of Multi-Die Systems



Source – Synopsys White Paper on Multi-Die Systems

- Traditional monolithic chips - Die is fabricated using single process node
- Multi-Die Systems - Disaggregation of multiple dies with different process nodes and then stacking and assembling them in a single package

Types of Multi-Die Systems

- Broadly classified as 2D, 2.5D and 3D

Choices Driven by PPA, Cost, Time to Market

Cost & Complexity

Organic Substrate
Die 1
Die 2
Substrate
2D

RDL Fanout
Die 1
Die 2
RDL
Substrate

Silicon Interposer
Die 1
Die 2
Interposer
Substrate

Si Bridge
Die 1
Die 2
Bridge
Substrate
2.5D

Hybrid Bonding
Die 2
Die 1
Substrate
3D

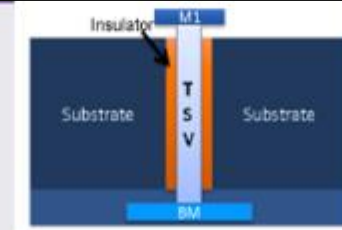
Source – Synopsys White Paper on Multi-Die Systems

Factors Influencing Multi-Die Systems

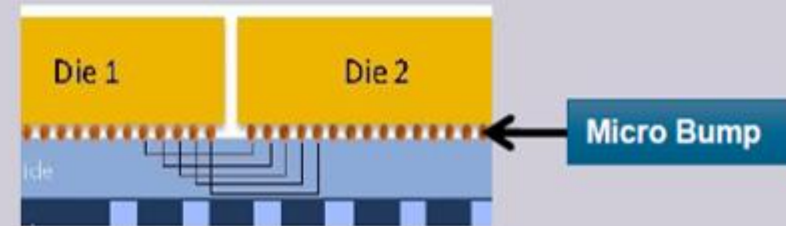
Benefit	Factor
Improved yield on smaller dies	Cost Effectiveness
Pack more functionality	Increased Functionality
Product variants	Modular Designs
Re-use silicon	Accelerate Time-To-Market

3DIC Basic Terminology

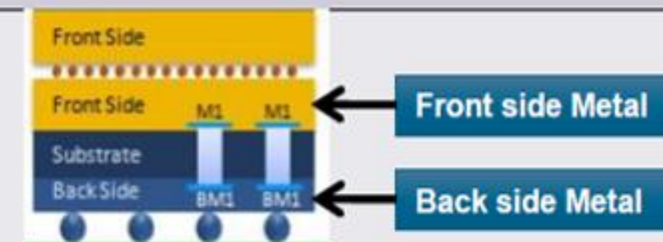
TSV
Through Silicon Via. A via that goes through the silicon substrate that enables connection from top to bottom.



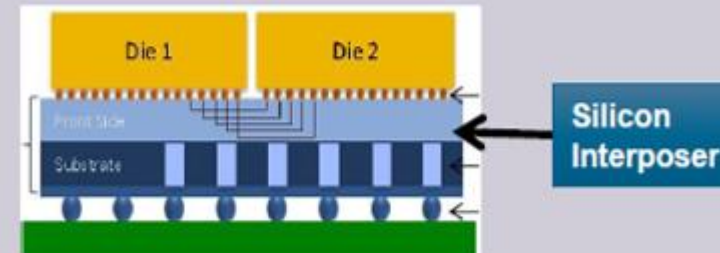
Micro-Bump(uBump)
Small solder ball are aligned between adjacent chips. They are used to connect one die to another. The aligned bumps are much smaller than flip-chip bumps.



Back side metal(MB)
Bumps are placed both on front side RDL layer and back side metal to form connection to both the “up” and “down” chips.



Silicon Interposer (Si-IP)
Chip-scale wiring structure that contains TSVs, enabling connection from one chip to another chip, or from one chip to the package.



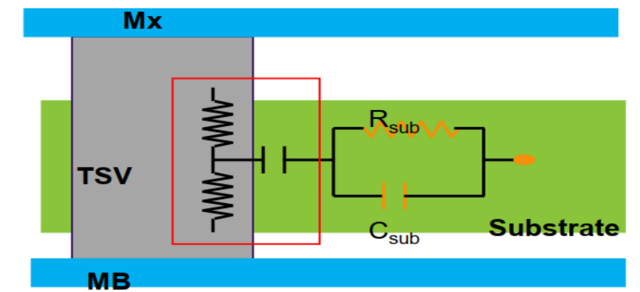
Source – Synopsys document on 3DIC extraction flow

Extraction Methodology

StarRC 3DIC Solutions

TSV

- TSV can be extracted as via or cell
- Linear dielectric around TSV modeled
- Resistance and ground cap for TSV is extracted
- TSV to TSV coupling is extracted(optional)
- TSV user defined sub-circuit(optional)



Source – Synopsys document on 3DIC extraction flow

Substrate

- Substrate optionally treated as floating node or grounded
- All metal layers (M1 to back metal BM1) capacitance extracted

Micro bump

- Optional user defined sub-circuit
- Resistance modeled using pseudo-via

Multi-Die Extraction Challenges/Solutions

Various coupling interactions possible in Multi-Die System

- Micro-bump coupling parasitics
- Coupling between the top routing layers of two stacked dies

Reduced complexity for interface modelling

- Multiple interfaces can exist in a Multi-Die system
- Extract each interface and merge to get the SPEF

Multi mode multi corner extraction

- SPEFs needed for all STA scenarios

StarRC 3DIC NDM Flow

NDM (Top)

Tech (Top)

Tech (Bot)

NDM (Bot)

StarRC

STAR (Top)

gen_starrc_vib

STAR (Bot)

StarRC

Merged ITF

Merged Design

Merged Map

StarRC FS

Top SPEF

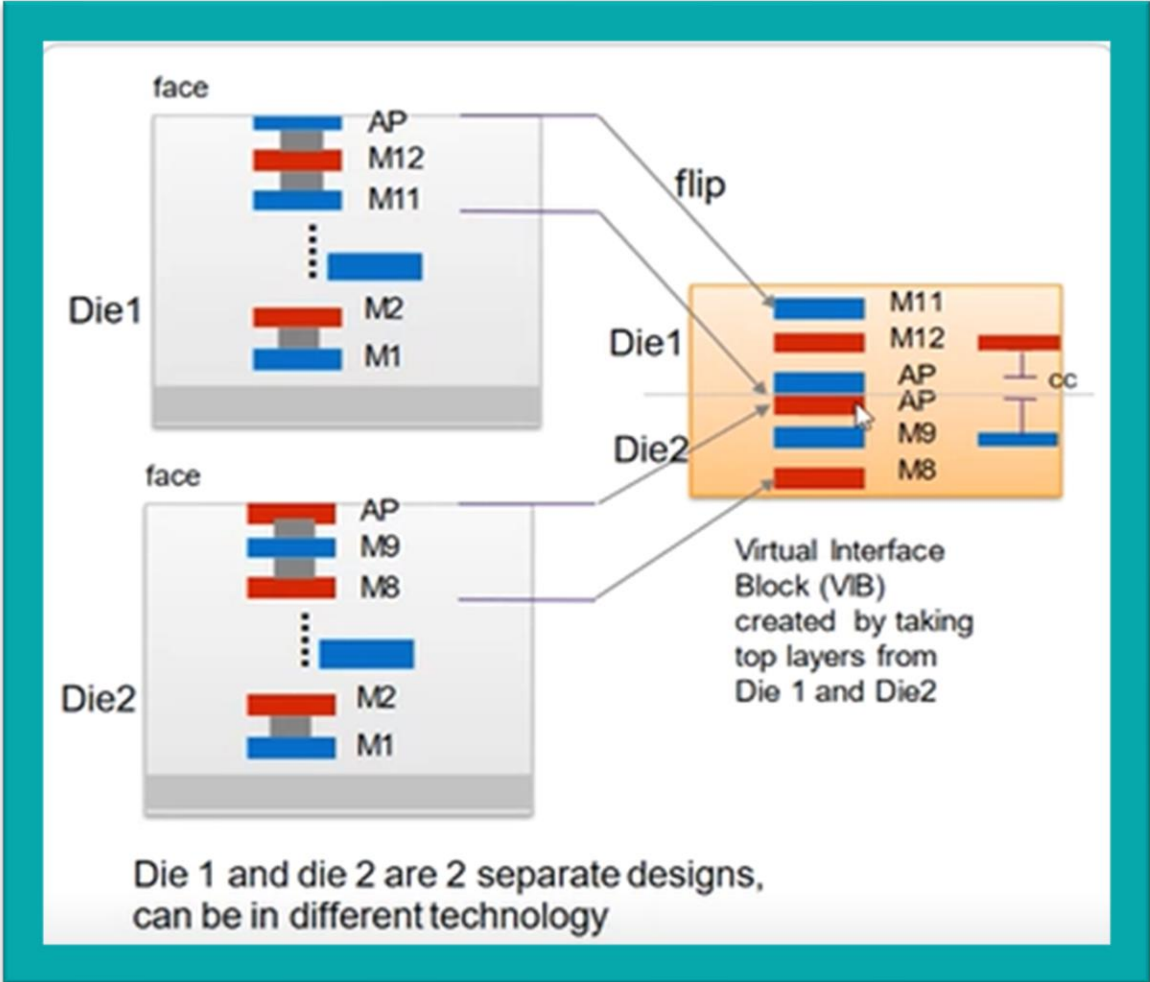
Inter-Die SPEF

Bot SPEF

Prime Time

Virtual Interface Block (VIB)

- ASCII Format
- Configurable layers
- Coupling cap extraction



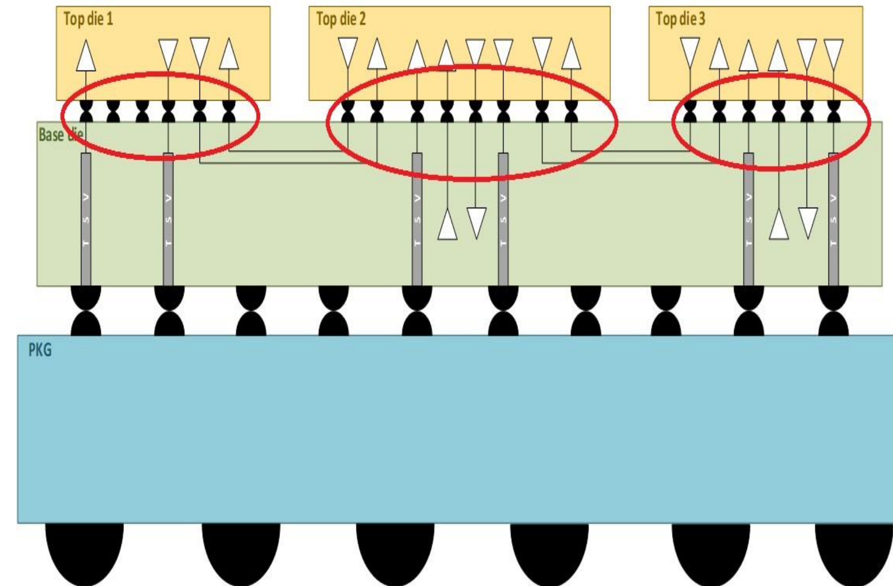
Source – Synopsys document on 3DIC extraction flow

D2D Extraction Method

Each VIB is extracted separately

Field Solver used to generate the VIB SPEF

VIB SPEFs for each corner is merged and used in STA



Source – Synopsys document on 3DIC extraction flow

snug

OUTPUTS

- Individual die SPEFs at Multi-Corner Multi-Mode scenarios
- VIB coupling cap SPEFs at 3DIC STA scenarios
- Accurate extraction of TSVs and bumps
- User controllable layer specification for VIB extraction

RESULTS

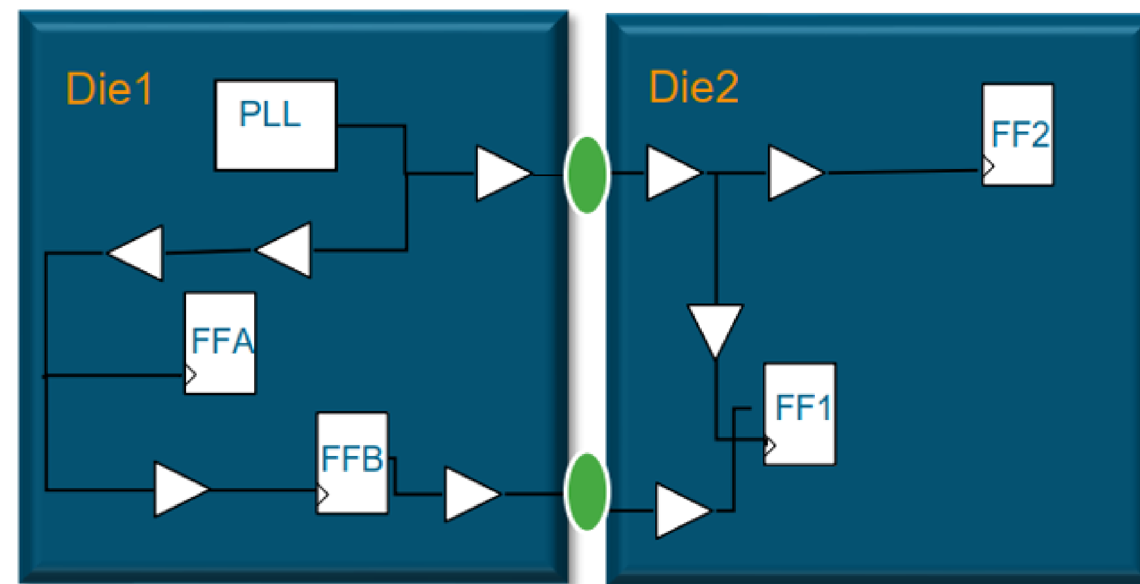
- Die-2-Die cap numbers are validated using test structure layouts
- **~95% correlation achieved**

STA Methodology

D2D Timing Topology

- Dies are connected through ubumps
- Timing path

  FFB (Die1) -> FF1 (Die2)
- Data and clock passes through Tx and Rx Hips
- Clock POD can be in any of the dies
- 3DIC STA model ensures setup and hold requirements of D2D paths



Source – Synopsys White Paper on Multi-Die Systems

3DIC STA Methodology Aspects

- Building 3DIC STA Environment
  - With Hyperscale Models
  - With Flat Collaterals
- Hyperscale vs Flat Comparison
- Hyperscale Model Validation - QRM
- Critical Path Retention Strategy
- Guardband / Derate Modelling
- Parasitic Annotation at 3DIC - VIB SPEF

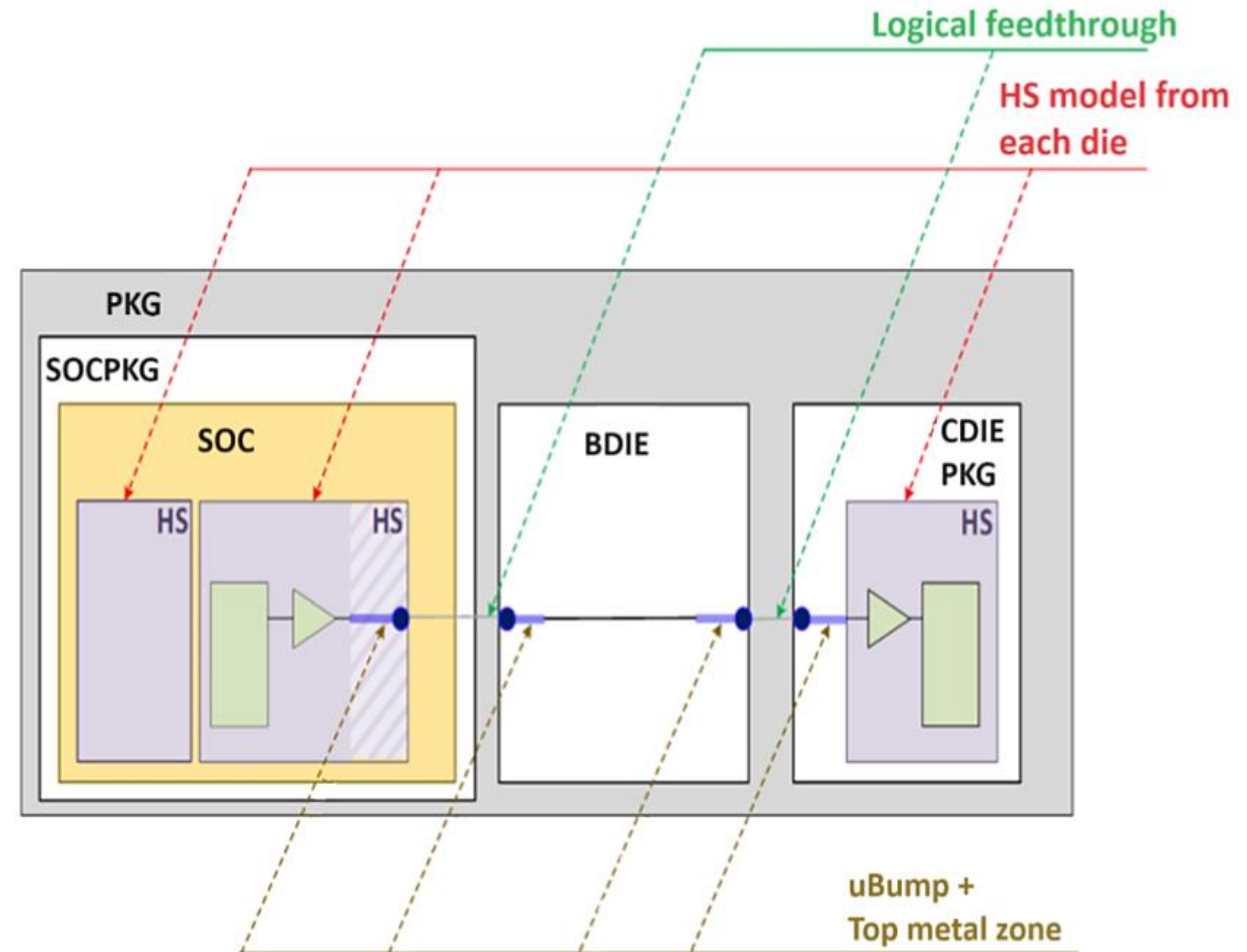
Building 3DIC STA Environment

Hyperscale Model

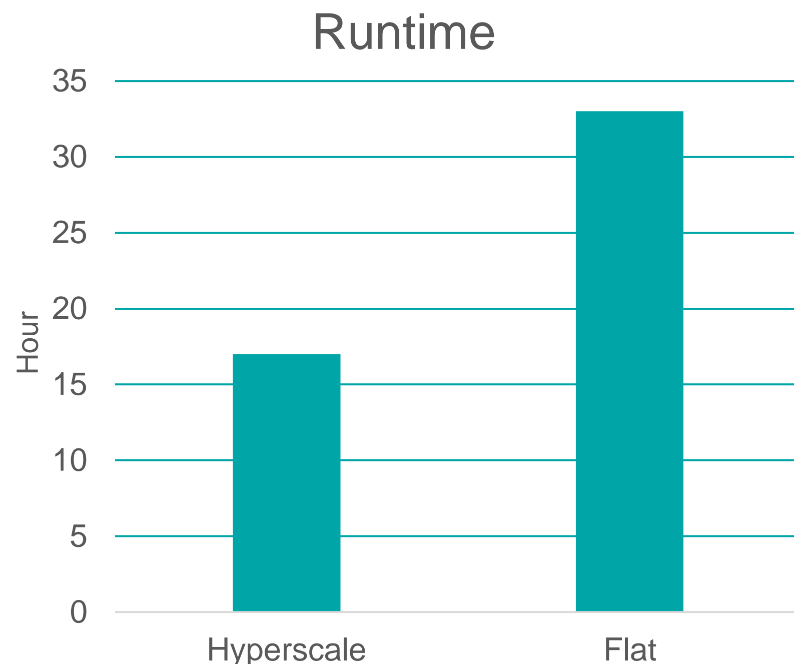
- Instantiation of dies as Hyperscale
- Generation of multiple PVT HS models
- Library rollup along with Hyperscale
- Ensure accuracy through QRM flow

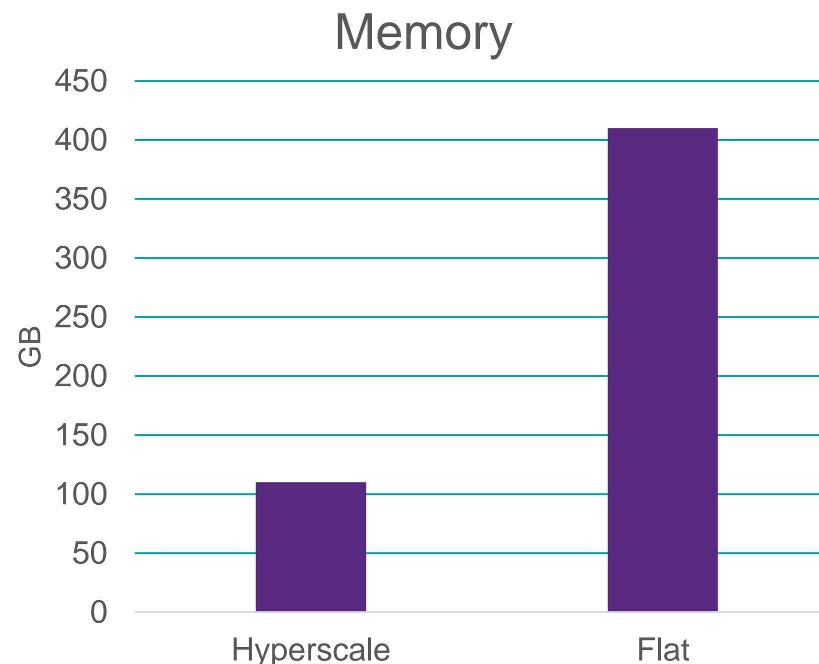
Flat STA

- Collaterals of each partition/subFC/die rolled up with libraries
- Read individual die Netlist, SPEF, UPF and Timing constraints



Hyperscale vs Flat Comparison

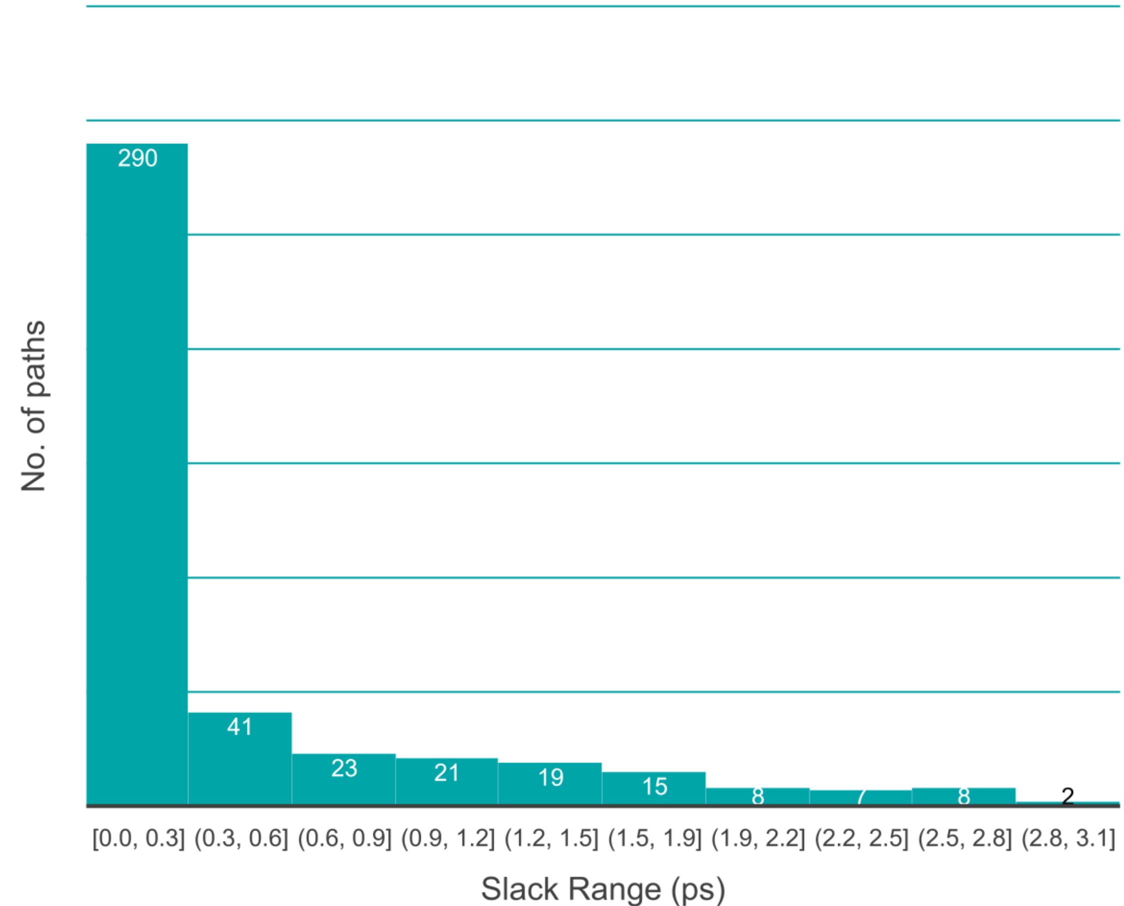




- Hyperscale Models gives **2x** faster runtime with **3.5x** lesser memory
- Flat STA has significant runtime penalty, typically used as Paranoia
- Hyperscale is the regular signoff closure methodology

Hyperscale Model Validation

- QRM flow ensures accuracy of Hyperscale
- **99% paths** correlating with Flat
- Max deviation **~ 3ps**



Critical Path Retention Strategy

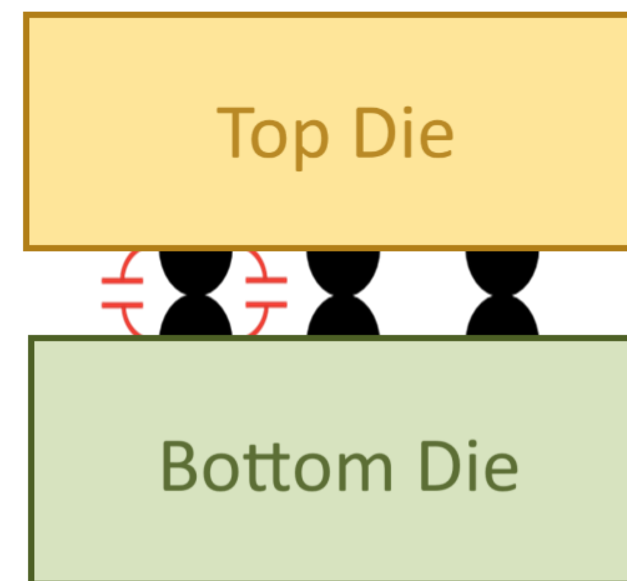
- Analysis of critical internal paths needed at 3DIC
- set_port_abstraction used to retain critical paths in HS models

Guardband and Derate Modelling

- D2D interface modelling
  - Material variation
  - Voltage drop
  - Foundry specific guardbands
- Aggregate the guardbands and derates for each die within 3DIC

Parasitic Annotation – VIB SPEF

- Die2Die bump connections are stitched with VIB SPEF
- Die level SPEF rolled up along with
  - Hyperscale Model
  - Flat collateral
- Correct SPEF annotation, key in timing closure



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Conclusion

Signoff flows deployed for production on several Multi-die projects with 2.5D / 3D configurations

Future work

Extraction

- Better compute management
- 3DIC compiler database consumption

STA

- Simultaneous multi corner analysis
- Spatial derating for cross die timing paths

THANK YOU

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