Forecasting the Timing and Static Power for Cells

Arm perspective

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Agenda

Introduction

Generation setup

Validation setup

Results from Arm® evaluation

Conclusion

Motivation
The dilemma of last minute PDK/PVT changes

Close on the current PDK/PVT (face issue of seeing competitor showing better benchmarks)

Wait for new characterized libs from vendor (late time to market).

Apply a pessimistic flat delay derate (pessimism can cause excessive tool TAT, not to mention the ECO after the implementation could be large).

Use the S2D technique (this will provide a realistic *estimated* derate for each and every path with +-3% of actual characterized liberty).

Note: S2D is not a SUBSTITUTE for actual characterized libraries

Introduction to S2D
S2D is an acronym for Spice to Design

What is S2D?

A method to assess timing and power impact of new spice model, in the absence of characterised new libraries within a range of ±3% of actual/New library data

Perturbation Effects

Threshold Voltage (Vth)

It is the gate voltage which controls the MOSFET. Vth is inversely proportional to delay

Saturation Current (Ids)

It is the current between drain to source when MOSFET is turned on. Ids is proportional to delay
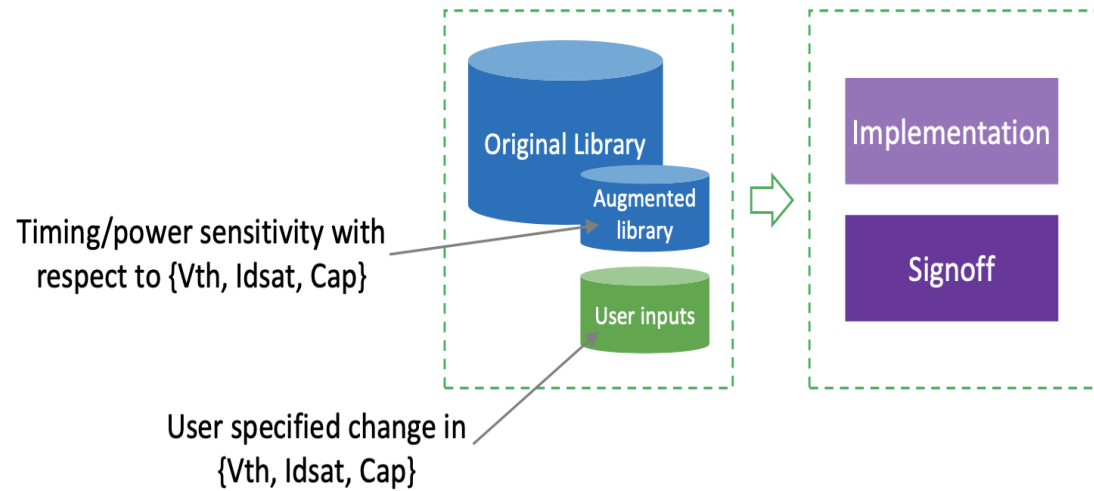
Analysis Types

PVTExplorer based S2D

User defined perturbation for Vth and Ids. PPA, Robustness analysis
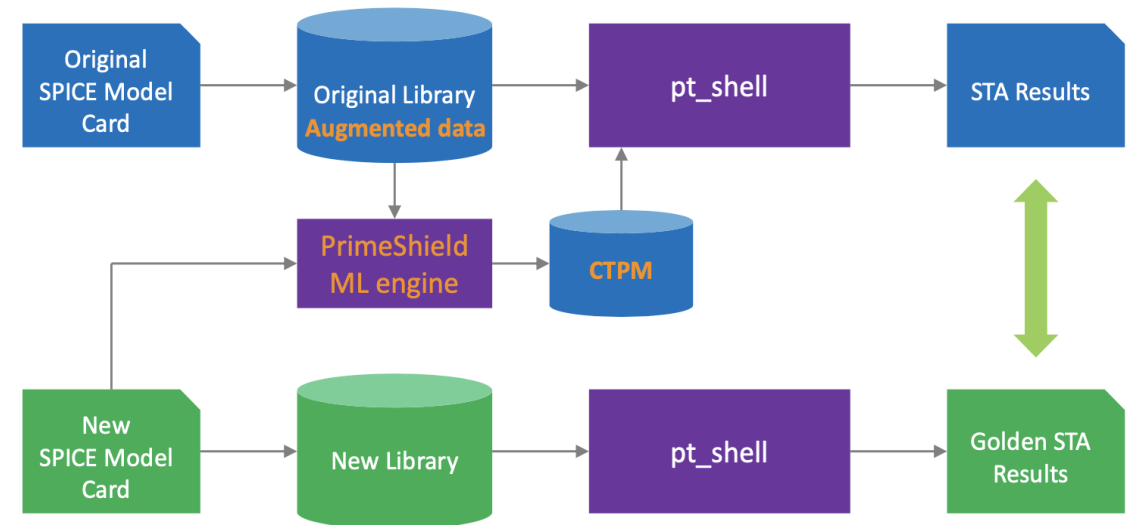
CTPM based S2d

ML analysis to determine the effects of a PDK change for the design Analyzing impact of new spice models

Analysis types

PVT Explorer based analysis

Original Library

Augmented library

User inputs

Implementation

Signoff

Timing/power sensitivity with respect to {Vth, Idsat, Cap}

User specified change in {Vth, Idsat, Cap}

CTPM based analysis

Original SPICE Model Card

Original Library
Augmented data

pt_shell

STA Results

PrimeShield ML engine

CTPM

New SPICE Model Card
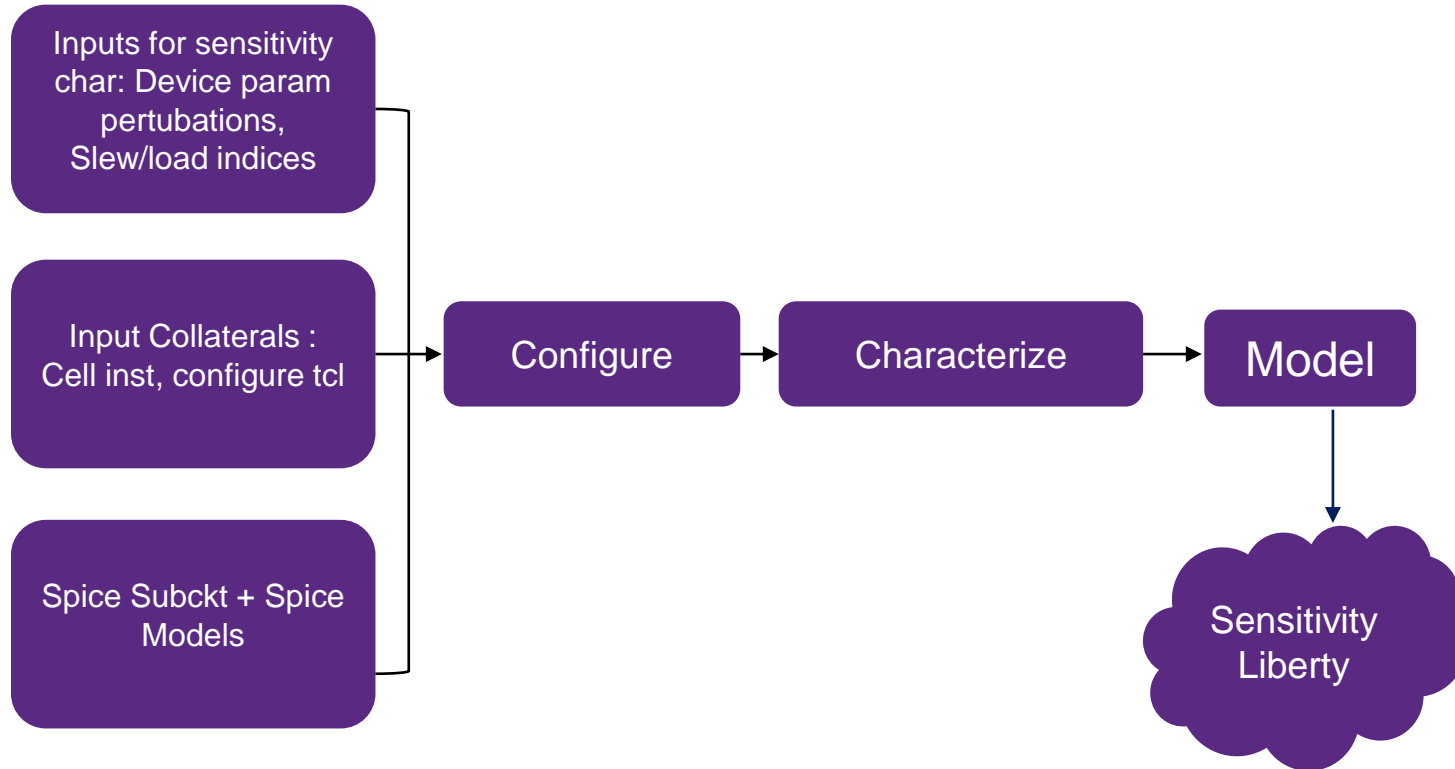
New Library

pt_shell

Golden STA Results

Note: The data is from Synopsys© Project Sicily

Generation of the Augmented Sensitivity Side-file

Data needed by Analysis tools to add derate from perturbation

Generation flow in Prime-Lib
S2D augmented sensitivity side-file generation

- Hspice simulator to be used as a model parser.
  - The simulator reads the models and perturbation parameters provided in the configuration. Then it creates a intermediate files, which is used by the PrimeLib.

- Pertubation parameters provided by foundry.

- Run the S2D char for the selected slew/load indices, to get full coverage of the delay/constraint tables.

- S2D data generated for delay/constraints/power/receiver_cap.

Simulation decks

Timing and Static power spice decks

ps_delay deck,

```
.data arc_data
+ slew_ck load_q temperature_tag __param_vdd .....
slew_time_hl_ck_45 ps_1 ps_2 ps_3 ps_4 ps_5 ps_6 ps_7 ps_8
+ 2.43e-13 2.71203e-17 -25 1.1 .... 2.7321e-12 0 0 0 0 0 0 0 0

+ 2.43e-13 2.71203e-17 -25 1.1 2.7321e-12 -1 0 0 0 0 0 0 0
```

```
.data arc_data
+ __dummy__ temperature_tag __param_vdd __param_vdde
__param_vnw __param_vpw __param_vss ps_1 ps_2 ps_3 ps_4
ps_5 ps_6 ps_7 ps_8
+ 0 -25 1.1 1.1 1.1 0 0 0 0 0 0 0 0 0 0 0
+ 0 -25 1.1 1.1 1.1 0 0 -1 0 0 0 0 0 0
+ 0 -25 1.1 1.1 1.1 0 0 1 0 0 0 0 0 0
```

ps_leakage deck

Checks on S2D

- Uses check_library utility from LibraryCompiler
  - Baseline liberty value check.
  - Any missing S2D tables
  - Trend Checks

```
set_check_library_options -sensitivity_lib -report_format {csv=1} -
tolerance {delay 0.02 0.002 slew 0.02 0.002 constraint 0.02 0.002
capacitance 0.02 0.0005 load_index 0.001 0.00001}

check_library -logic_library_name "./baseline.db ./sensitivity.db"

report_check_library_options

quit
```

Check_library cmd file

S2D table snippet

```
Sensitivity table:
  Param_name: p_vta_slvtnfet
  Pert_value: -0.050000
  Table_type; cell_rise
  VARIABLE_1: input_transition_time
  VARIABLE_2: output_net_total_cap
    INDEX_1: 0.00110600 0.02426870 0.19740000
    INDEX_2: 0.00002712 0.02240310 0.40686199
    VALUES: -0.00167352 -0.00237539 -0.00260401
            -0.00351806 -0.00424603 -0.00457861
            -0.01588330 -0.01731160 -0.01739000

Sensitivity table:
  Param_name: ids_mult_slvtnfet
  Pert_ratio: -0.150000
  Table_type: cell_rise
  VARIABLE_1: input_transition_time
  VARIABLE_2: output_net_total_cap
    INDEX_1: 0.00110600 0.02426870 0.19740000
    INDEX_2: 0.00002712 0.02240310 0.40686199
    VALUES: 0.00148183 0.00190724 0.00220797
            0.00178256 0.00219025 0.00245375
            0.00479302 0.00528656 0.00569219
```
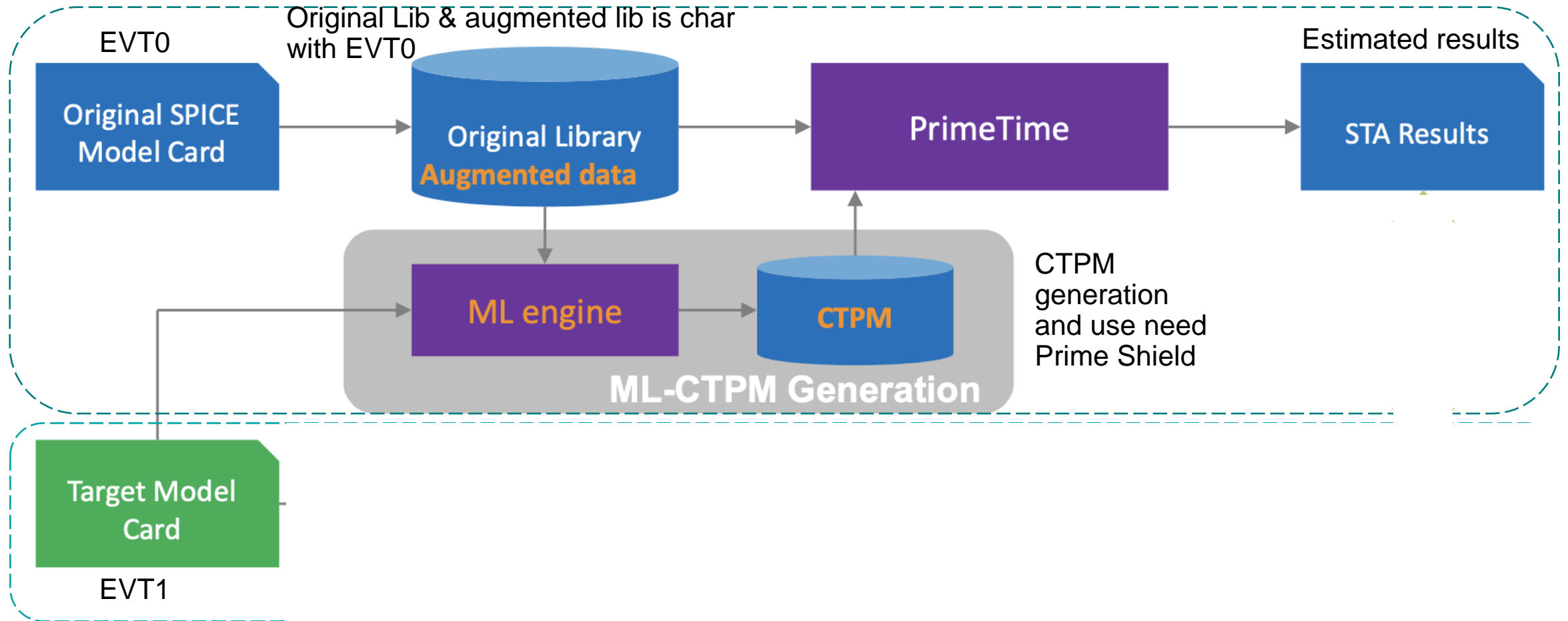
The check_library reports will remain empty if there is no violations

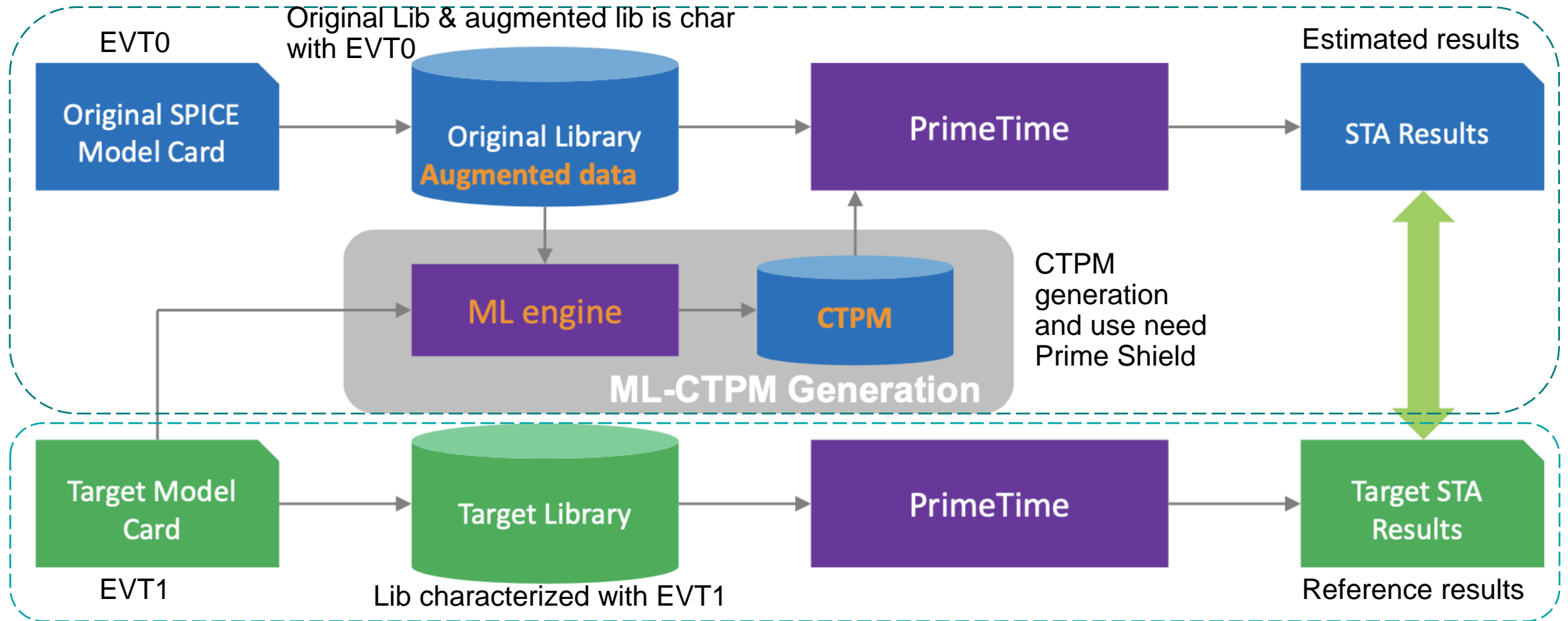# Analysis on entire cell set in the base toolkit library
Checking how CTPM S2D works on library cell set

Collaterals & Flow

EVT0

Original Lib & augmented lib is char with EVT0

Estimated results

Original SPICE Model Card → **Original Library** / **Augmented data** → **PrimeTime** → **STA Results**

ML-CTPM Generation: **ML engine** → **CTPM**

CTPM generation and use need Prime Shield

Target Model Card

EVT1

Note: Basic data is from Synopsys© Project Sicily

Collaterals & Flow

Note: Basic data is from Synopsys© Project Sicily

Analysis Setup details – library coverage

Library:

- sc6_ln03gapss0_base_slvt_ffpg_nominal_min_1p05v_m25c (fast corner lib-ccs-tn)
- sc6_ln03gapss0_base_slvt_sspg_nominal_max_0p50v_125c (near threshold corner)

Design:

- Is a netlist covering all cells in the Samsung 3GAP library

Tool used:

- **PrimeTime:** 2022.12-SP5-1-VAL-20240115_EngBuild
- **Hspice:** 2023.03-SP2-1

Process:

- The S2D CTPM flow uses a machine learning algorithm to determine the perturbation applied to each node of the design paths. This is then used in PT to report the estimated timing numbers of paths. Another PT run is performed on the newly characterized liberty. PT reports between S2D & NEWPDK run are compared
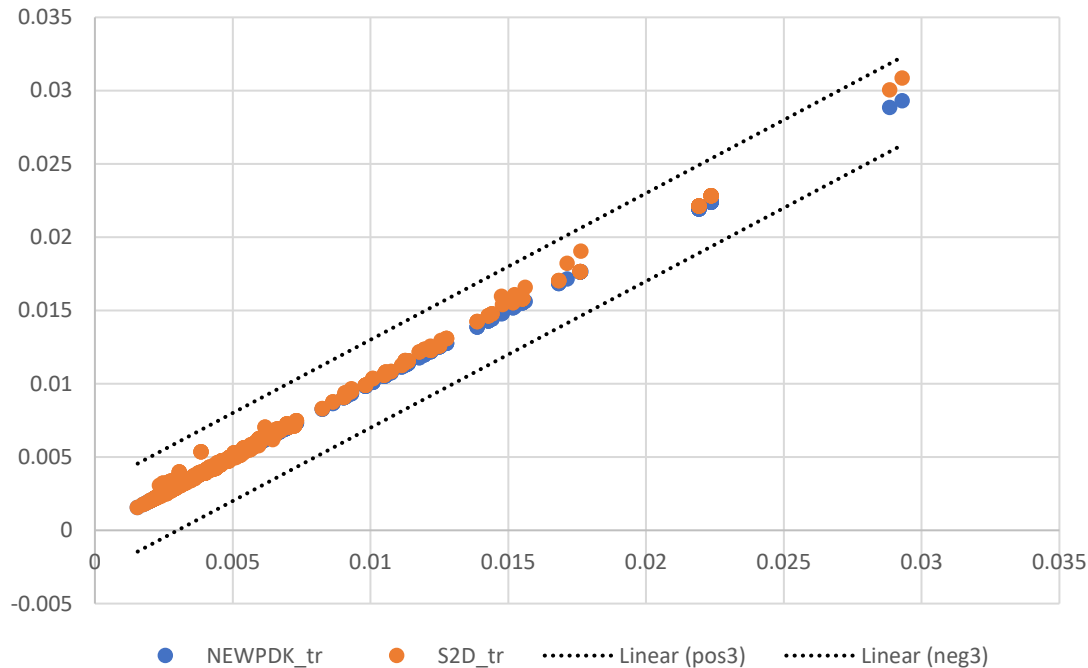
Expectation:

- The delay difference between S2D estimated STA and NEWPDK STA should be within +-3%
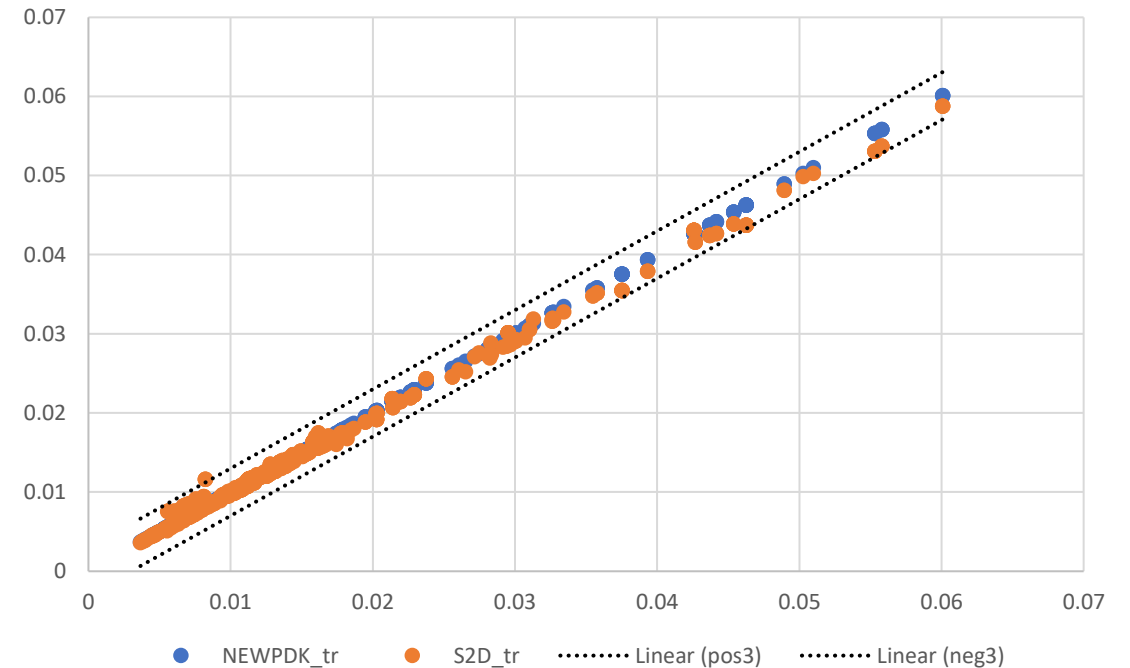
Results from CTPM based solution

Transition time Analysis done on EVT0 + S2D & EVT1 of Samsung 3GAP process

S2D vs NEWPDK Transition Plot FFPG-Base

Transition-FFPG	S2D	NEW-PDK	ABS-DIFF(ps)	%-DIFF
MIN	0.001547	0.001547	0	0%
AVG	0.005506	0.005441	0.064	-1%
MAX	0.030841	0.029301	1.54	-5%

S2D vs NEWPDK Transition Plot SSPG-Base

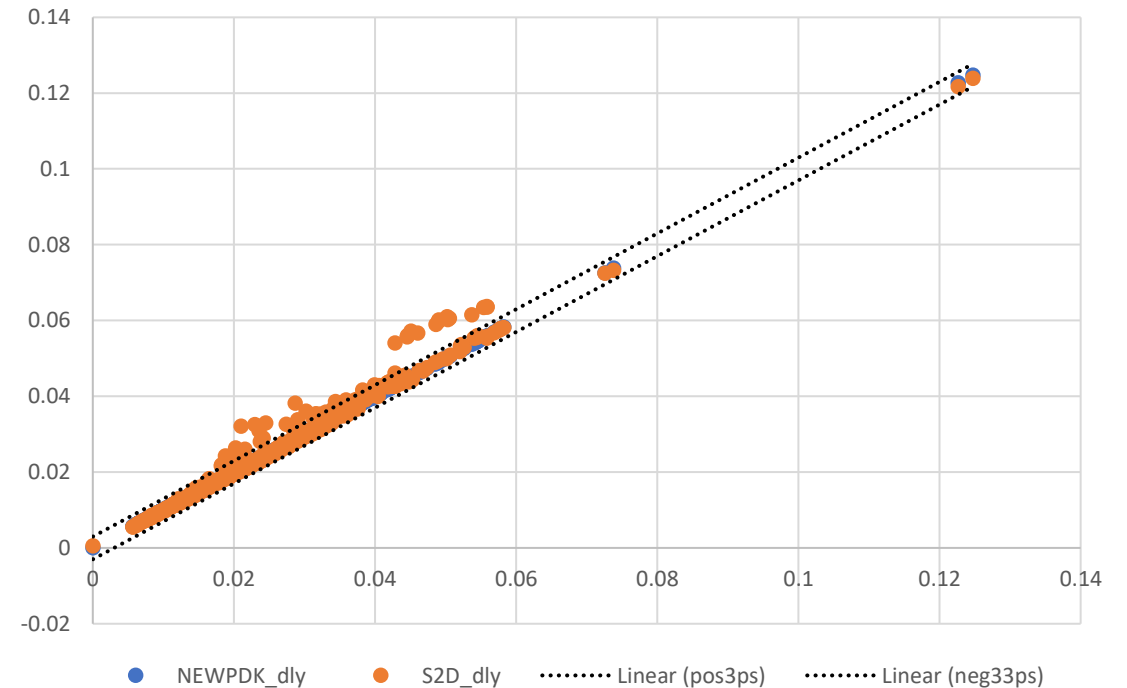| Transition-SSPG	S2D	NEW-PDK	ABS-DIFF(ps)	%-DIFF
MIN	0.003567	0.003647	0.08	2%
AVG	0.013748	0.013945	0.197	1%
MAX	0.058754	0.060068	1.314	2%

Results from CTPM based solution

Delay time Analysis done on EVT0 + S2D & EVT1 of Samsung 3GAP process

S2D vs NEWPDK Delay Plot FFPG-Base
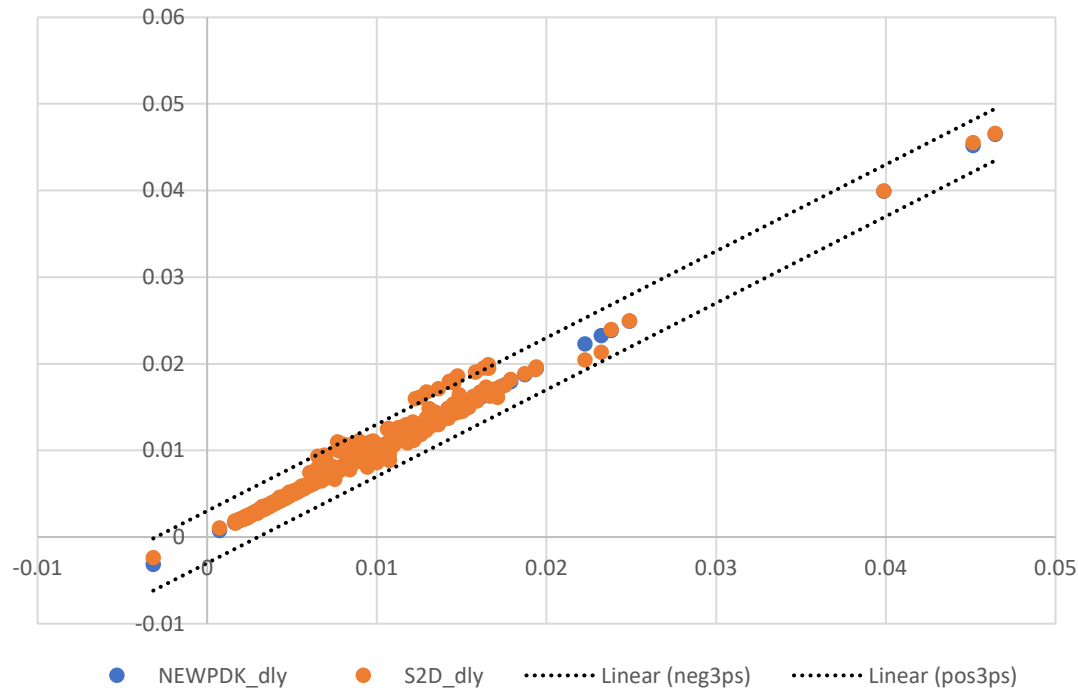
Delay-FFPG	S2D	NEW-PDK	ABS-DIFF	%-DIFF
MIN	-0.002406	-0.003174	0.768	24%
AVG	0.007654	0.007527	0.126	-2%
MAX	0.046573	0.046452	0.121	0%

S2D vs NEWPDK Delay Plot SSPG-Base

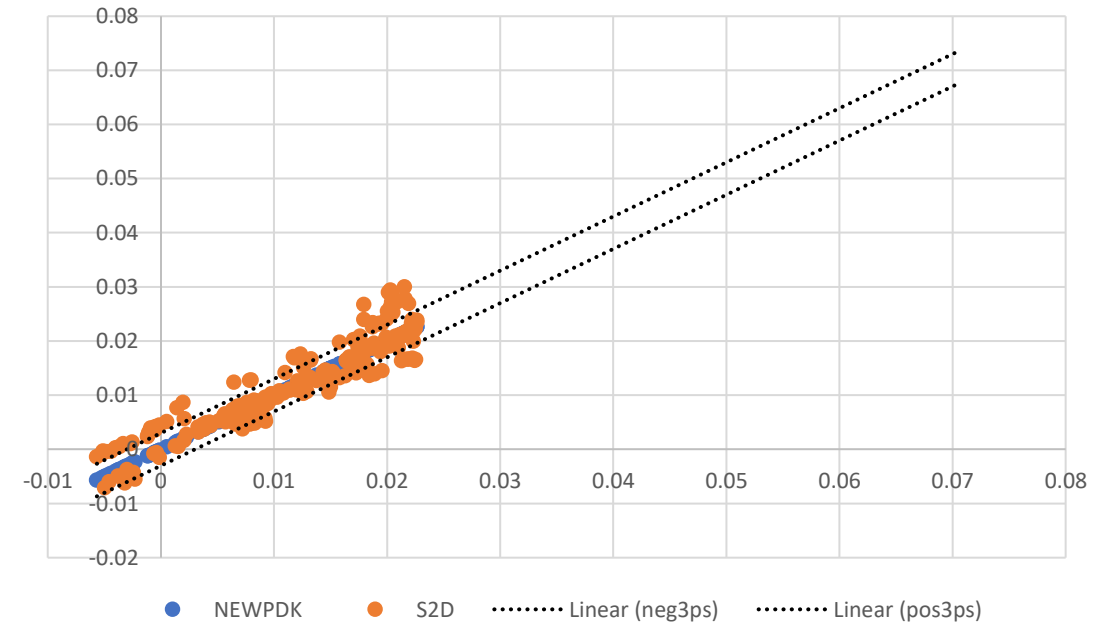| Delay-SSPG	S2D	NEW-PDK	ABS-DIFF	%-DIFF
MIN	0.000459	0.000013	0.446	-97%
AVG	0.023880	0.023982	0.102	0%
MAX	0.165214	0.171294	6.08	4%

Results from CTPM based solution

Constraint Analysis done on EVT0 + S2D & EVT1 of Samsung 3GAP process

S2D vs NEWPDK FConstraint Plot FPG-Base
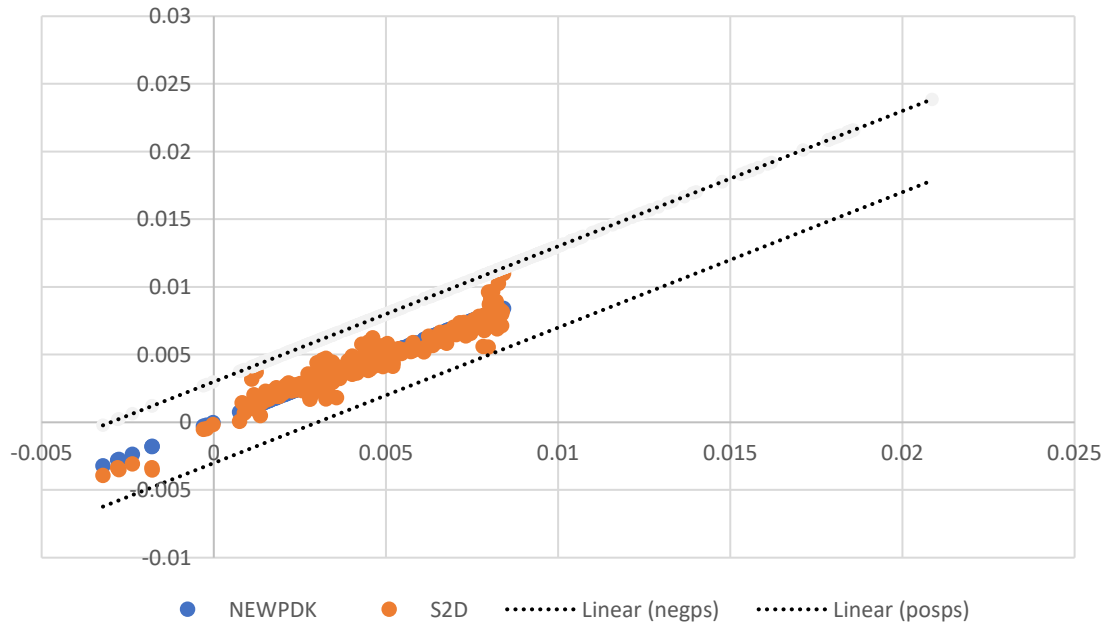
Constraint-FFPG	S2D	NEW-PDK	ABS-DIFF(ps)	%-DIFF
MIN	-0.003916	-0.003219	0.697	-22%
AVG	0.007251	0.007269	0.018	0%
MAX	0.020466	0.020863	0.397	2%

S2D vs NEWPDK Constraint Plot SSPG-Base

Constraint-SSPG	S2D	NEW-PDK	ABS-DIFF(ps)	%-DIFF
MIN	-0.007079	-0.005668	1.411	-25%
AVG	0.019820	0.020502	0.682	3%
MAX	0.064736	0.070211	5.475	8%

Summary on Timing
Snapshot of the analysis result for library coverage netlist

		FFPG(Diff)ps	FFPG (%)	SSPG(Diff)ps	SSPG (%)
	Min	0	0%	0.08	2%
Transition	Avg	-0.064	-1%	0.197	1%
	Max	-1.54	-5%	1.314	2%
	Min	-0.768	24%	-0.446	-97%
Delay	Avg	-0.126	-2%	0.102	0%
	Max	-0.121	0%	6.08	4%
	Min	0.697	-22%	1.411	-25%
Constraint	Avg	0.018	0%	0.682	3%
	Max	0.397	2%	5.475	8%

- SSPG fares badly w.r.t FFPG one reason being SSPG is a near threshold library

- The average for most of cells is within +-3% range

- The constraints and transition data is expected to normalizes over design

Summary on Static Power – Total Power
Snapshot of the analysis result for library coverage netlist

	FFPG(Diff)			SSPG(Diff)		
	EVT0	S2D	EVT1	EVT0	S2D	EVT1
Leakage	2.616e-5	2.616e-5	2.561e-5	8.373e-5	8.373e-5	8.175e-5
Internal	9.513e-5	9.590e-5	9.542e-5	1.307e-5	1.312e-5	1.315e-5

- No perturbation is observed on leakage power

- We see the effect on internal power

- Working with Synopsys to understand this behavior

Conclusion

S2D-CTPM flow is a value add for timing, providing few months advantage

- **The average for most of the library cells is within ±3% or ±3ps range**
- **Outliers seen were few and mostly on complex function cells like MBFF**

The S2D-CTPM flow for static power is under evaluation

- The values for Leakage power are closer to the older PVT, which is not expected
- Synopsys is working on this limitation