Advancing Signoff Convergence with PrimeClosure™ in the age of AI

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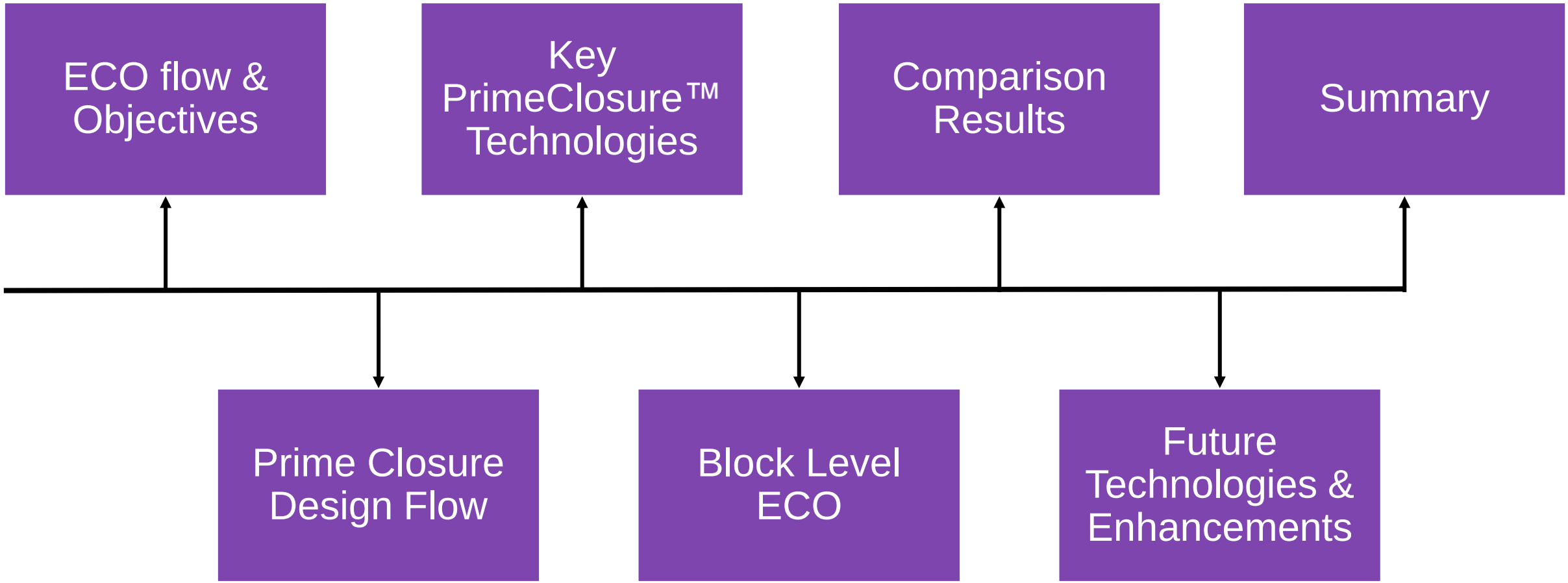
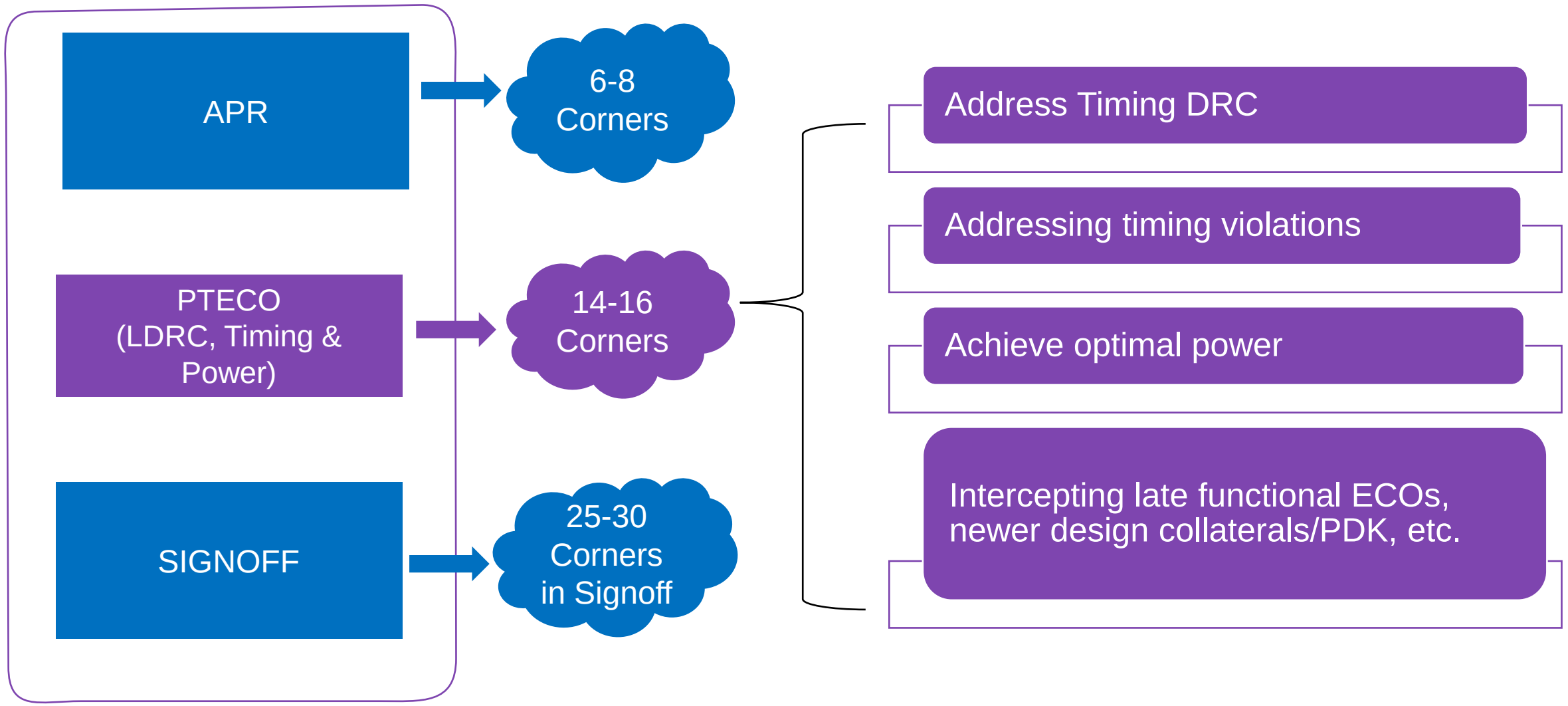
Intel Graphics Team

AGENDA


ECO flow & Objectives
Key PrimeClosure™ Technologies
Comparison Results
Summary
Prime Closure Design Flow
Block Level ECO
Future Technologies & Enhancements

ECO & It’s Objectives

ECO Flow & Objectives



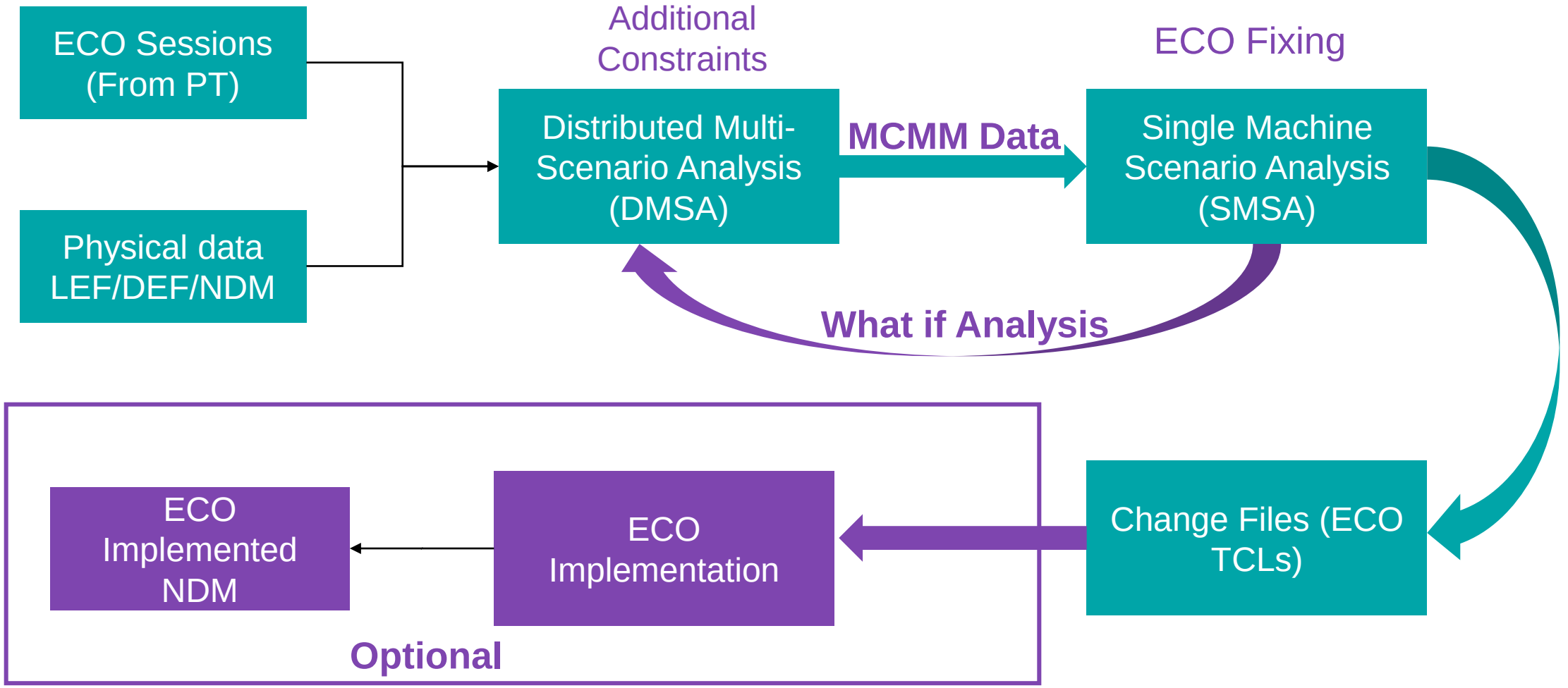
Current Available Tool Solutions

	PRIMETIME (DMSA)	TWEAKER
Data Preparation Efforts	Low	Medium/High
Physical Aware ECOs	Yes	Yes
Timing Correlation (Signoff PT)	~100%	~95%
Distributed Machine Feature	Yes	Can be split if Partition violation count is High
Hierarchical ECO support	Yes	Yes
Multi-corner Support	Yes	Yes (100+ corners on same machine)

PrimeClosure™: Next-Generation ECO (Integrated the strengths of PTECO™ and Tweaker™ ECO + New Technologies)

PrimeClosure™ Design Flow

PrimeClosure™ Design flow



Key PrimeClosure™ Technologies

Key PrimeClosure™ Technologies

- SMSA
- Cross Version
- AI-driven ECO
- Clock Surgery

Key PrimeClosure™ Technologies

1. SMSA: Single-Machine Multi-Scenario Analysis

Single ECO database

- All scenario timing data is merged into one ECO database using the timing collaterals generated by the PrimeTime tool.
- ECO fixing happens on this ECO database using single Machine

High-Capacity and Less Compute Resources

- Capable of optimizing 100+ scenarios with fewer machines, and subsystem/top-level.

Key PrimeClosure™ Technologies

2. Cross Version Compatibility

- Primetime DMSA has limitation that Timing Session and DMSA needs to use Same PT version

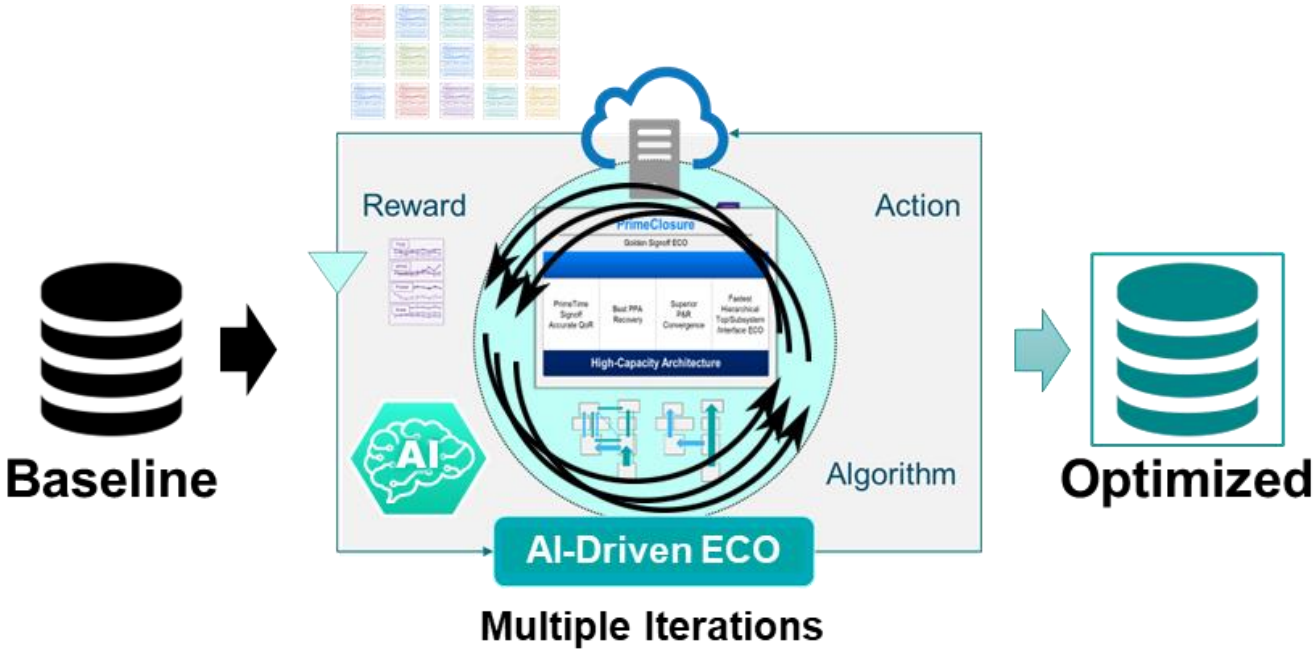
- Prime Closure has cross version compatibility feature which allows Timing session and Prime Closure can be on different version.

Key PrimeClosure™ Technologies

3. AI-driven ECO – Early Version

Integrated Delphi (AI-driven ECO Space Optimization) technology, which allows different ECO parameter values (built-in Permutons) to achieve better PPA/design convergence results.

AI-driven ECO for Last-Mile Closure



Original Timing Fixing Settings

set slk_auto_sizing_max_shift_distance 4
set slk_fix_hold_watch_driving_pin_setup_slack false
set slk_fix_hold_watch_driving_pin_hold_slack false
set slk_fix_hold_watch_driving_pin_slack false

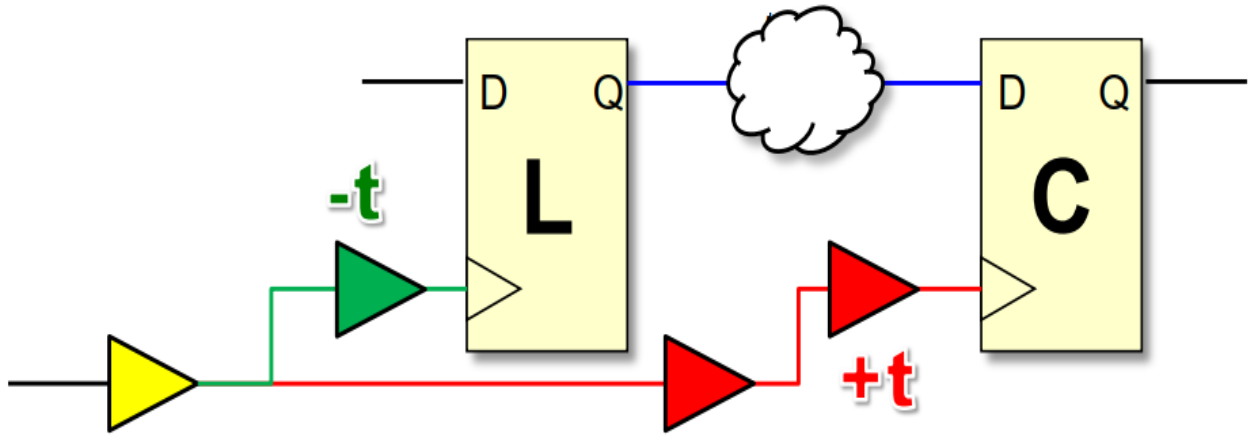
Built-In Permutons

set slk_auto_sizing_max_shift_distance [0, 4, 8]
set slk_fix_hold_watch_driving_pin_setup_slack ---
set slk_fix_hold_watch_driving_pin_hold_slack ---
set slk_fix_hold_watch_driving_pin_slack ---

Key PrimeClosure™ Technologies

4. Clock-Surgery

- Address setup timing speed-paths with useful clock skew.



New Options/Enhancements

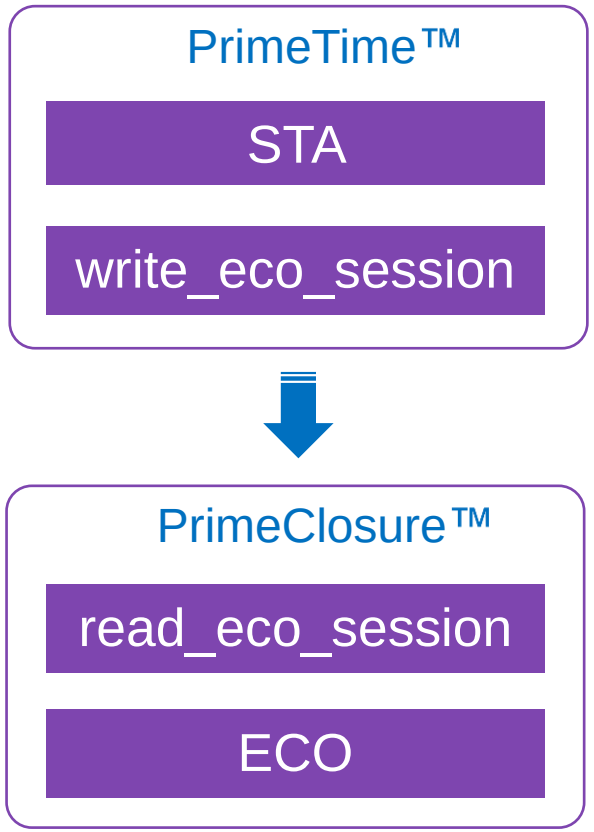
- Restrict the maximum clock level (*-max_level_in_clock 5*)
- Exclude/Ignore IO related endpoints (*-ignore_boundary_flops 1*)

Fix at the starting point **(Green: Pull-in):**
Decrease clock delay by upsizing and/or bypass

Fix at the endpoint **(Red: Push-out):**
Increase clock delay by downsizing and/or inserting

Block Level ECO

Data Exchange from PrimeTime™ to PrimeClosure™




```
# Generate sessions for PT and PC
save_session ./pt_session_scen1

write_eco_session <pre_eco_session_scen1>  \
 -include {smsa_data}  \
   -smsa_data_type {setup hold max_transition max_capacitance  \
       max_fanout power drc_max_transition drc_max_capacitance pin_slew}  \
   -smsa_data_format binary  -smsa_pba_mode exhaustive \
 -link_session $sh_launch_dir/pt_session_scen1
```

Reuse/Link the existing STA session to save disk-space

Design 1 (~1.3M instances)	PT Session (GB)	PC session (GB)	PC session (GB) (-link_session)	PC session (with -link_session and Without SMSA data) (KB)
PVT1	4.4	5.6	1.2	56
PVT2	4.4	5.6	1.2	56
PVT3	4.4	5.6	1.2	56
PVT4	4.4	5.6	1.2	56
PVT5	5	6.2	1.2	80
PVT6	5	6.2	1.2	80
PVT7	6.6	8.3	1.7	116
PVT8	6.6	8.3	1.7	116
Percentage		126 %	26 %	0.0015%

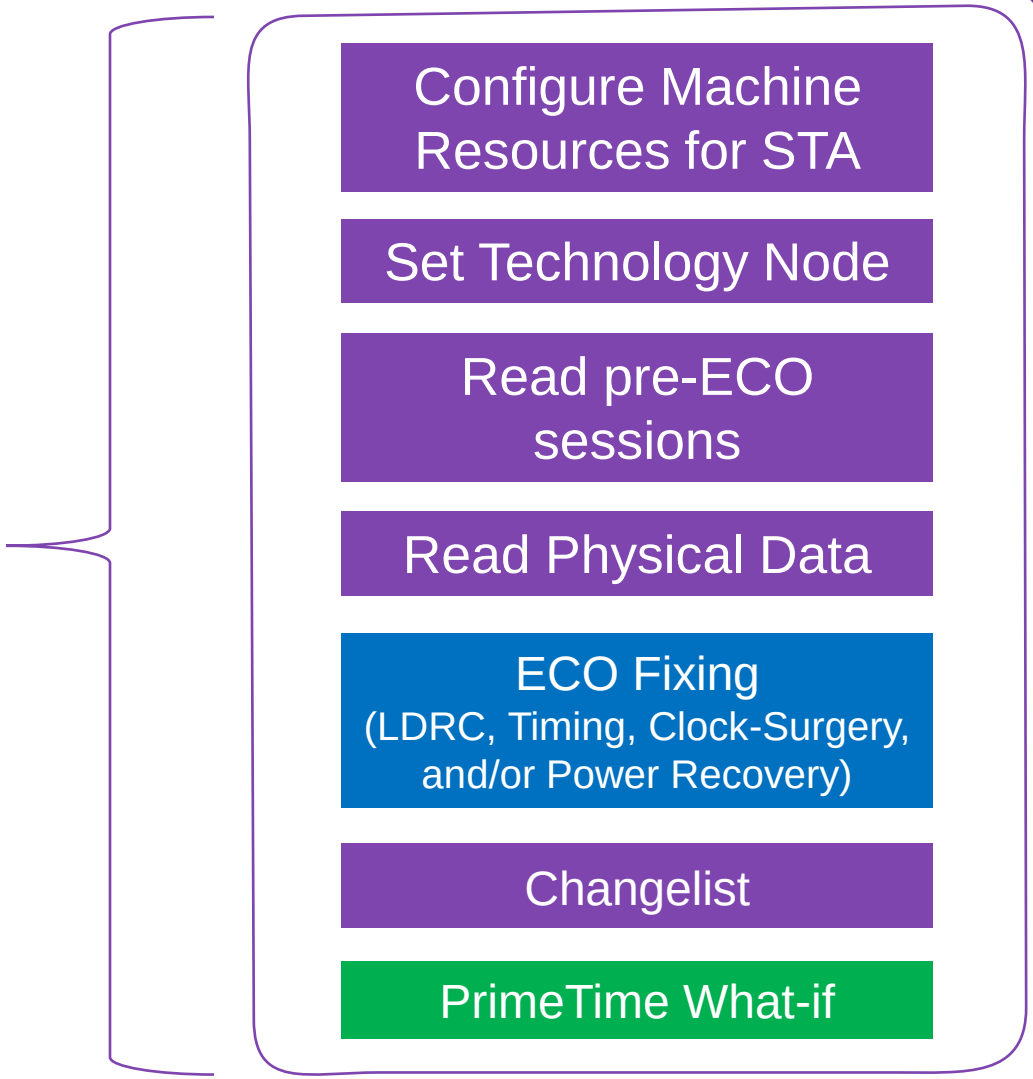
Comparison of PT and PC Save Session File Sizes (GB)

PrimeClosure™ Recipe

pc_script.tcl

```
set multi_scenario_working_directory PC_DMSA; set_host_options -num_processes 12
set_technology –node <N>

read_eco_session pre_eco_session

# Additional settings from set_eco_options can be included here
read_physical_data  -tech $tech_lef  -lef $lef_files \
                -physical_icc2_lib design.ndm  -physical_icc2_blocks pre_eco
start_eco -mode dmsa
start_eco -mode smsa

fix_eco_drc
fix_eco_timing -type setup
fix_eco_timing -type hold

fix_eco_power
start_eco -mode dmsa
start_eco -mode smsa
fix_eco_drc -type max_transition -verbose -methods {recovery}
fix_eco_timing -type setup -methods {recovery}

ecotclout -icc2 <eco_changes.tcl>
report_eco_summary -summary
```

pc_shell –f pc_script.tcl –output_log ./logs/run.log



An Example of PrimeClosure™ Log File

report_eco_summary -summary

```
Setup violations (Pre-ECO->Post-ECO)
-------------------------------------------------------------------------------
                Total      reg ->    reg   in ->  reg  reg ->  out   in ->  out
-------------------------------------------------------------------------------
WNS    -0.16 ->  -0.04    -0.16 ->  -0.04 0.00 -> 0.00 0.00 -> 0.00 0.00 -> 0.00
TNS   -88.05 ->  -4.62    -88.05 ->  -4.62 0.00 -> 0.00 0.00 -> 0.00 0.00 -> 0.00
NUM    13231 ->    611    13231 ->    611    0 ->    0    0 ->    0    0 ->    0
-------------------------------------------------------------------------------

Hold violations (Pre-ECO->Post-ECO)
-------------------------------------------------------------------------------
                Total      reg ->    reg   in ->  reg  reg ->  out   in ->  out
-------------------------------------------------------------------------------
WNS    -0.06 ->  -0.05    -0.06 ->  -0.05 0.00 -> 0.00 0.00 -> 0.00 0.00 -> 0.00
TNS   -16.38 ->  -1.34    -16.38 ->  -1.34 0.00 -> 0.00 0.00 -> 0.00 0.00 -> 0.00
NUM    7514 ->    293     7514 ->    293    0 ->    0    0 ->    0    0 ->    0
-------------------------------------------------------------------------------
```

```
#-------------------------------------------------
# autofix detail log summary:
#-------------------------------------------------
# B004 Blocked by Timing Window (Setup)(1)
# B010 Improved slack < min improved slack(75)
# B012 Blocked by sizing non-STD cell(8)
# B025 Blocked by Timing Window (Setup) (Input Pin)(5)
# B051 Blocked by don't use setting(1787)
# B073 Blocked by twf clock pin(34)
# B086 Blocked by fix setup/cons without sizing down(1718)
# B126 Blocked by auto-sizing area ratio(1767)
#-------------------------------------------------
```

*Blocking Codes for Unresolvable **Setup** Viols*

```
#-------------------------------------------------
# autofix detail log summary:
#-------------------------------------------------
# B003 Blocked by no setup margin (twf)(1)
# B004 Blocked by Timing Window (Setup)(3)
# B006 Blocked by Driving Timing Window (Setup)(1)
#-------------------------------------------------
```

*Blocking Codes for Unresolvable **Hold** Viols*

An Example of ECO Implementation Log File

source <eco_changes.tcl>

```
ECO: === Summary of dropped ECOs due to target pre-check          ===
ECO: === Enabled by PrimeClosure variable (eco_tcl_pre_check_target)  ===
ECO:                        accept        drop       total
ECO: ------------------------------------------------------------
ECO:    insertion             2000           0        2000
ECO:    deletion                23           0          23
ECO:    dummy_load               0           0           0
ECO:    sizing              193872           0      193872
ECO:    by_pass                  0           0           0
ECO:    pin_swap                 0           0           0
ECO:    other_eco                0           0           0
```

legalize_placement -post_route -incremental

```
        Number of cells moved: 2180 (0.16%)   Orientation changes only: 211
    Average cell displacement: 0.0003 um (AW: 0.0003 um = 0.0021 rh)
        Max cell displacement: 1.9433 um = 13.5902 rh
Number of large displacements: 215
```

Comparison Results

Prime Closure™ Vs Primetime™

Comparison Results

Timing

PARTITION	TOTAL SETUP TNS (ROUTE)	TOTAL SETUP VP (ROUTE)	TOTAL SETUP TNS (PTECO)	TOTAL SETUP VP (PTECO)	TOTAL SETUP TNS (PCECO)	TOTAL SETUP VP (PCECO)
DESIGN1	-16.30	2672	-1.88	491	-1.20	324
DESIGN2	-14.596	1851	-0.418	175	-0.276	77
DESIGN3	-25.107	4121	-0.242	90	-0.137	65
DESIGN4	-40.66	7570	-1.012	148	-1.233	184
DESIGN5	-32.155	4370	-0.061	44	-0.068	52
Percentage					19.39 %	25.95%

19% Setup TNS improvement with PC

PARTITION	TOTAL HOLD TNS (ROUTE)	TOTAL HOLD VP (ROUTE)	TOTAL HOLD TNS (PTECO)	TOTAL HOLD VP (PTECO)	TOTAL HOLD TNS (PCECO)	TOTAL HOLD VP (PCECO)
DESIGN1	-6.00	2242	-0.15	52	-0.30	73
DESIGN2	-11.564	4764	-0.425	231	-0.314	247
DESIGN3	-6.279	2295	-0.089	87	-0.145	97
DESIGN4	-5.282	2177	-0.396	115	-0.345	96
DESIGN5	-13.003	3510	-0.197	159	-0.129	90
Percentage					1.83 %	6.37%

1.8% Hold TNS improvement with PC

Comparison Results

Power

PARTITION	TOTAL POWER PTECO(mW)	TOTAL DYNAMIC POWER PTECO(mW)	TOTAL LEKAGE POWER PTECO(mW)	TOTAL POWER PCECO(mW)	TOTAL DYNAMIC POWER PCECO(mW)	TOTAL LEKAGE POWER PCECO(mW)
DESIGN1	24.62	16.12	8.5	23.94	16.15	7.8
DESIGN2	13.69	9.56	4.12	13.39	9.55	3.84
DESIGN3	22.26	18.45	3.8	22.24	18.44	3.8
DESIGN4	34.27	27.26	7.01	34.06	27.26	6.77
DESIGN5	20.13	16.08	4.05	19.8	15.99	3.81
Percentage				**1.34**%	**0.09**%	**5.31**%

5.3% Leakage improvement with PC

Comparison Results

Runtime

PARTITION	INSTANCE COUNT (M)	RUNTIME PTECO (HH:MM)	RUNTIME PCECO (HH:MM)
DESIGN1	1	9:53	7:28
DESIGN2	1.35	14:30	11:30
DESIGN3	1.3	13:50	11:10
DESIGN4	0.33	3:54	2:50
DESIGN5	1.44	15:50	13:25
Percentage			19.80%

20% Runtime improvement with PC

Comparison Results

Routing

PARTITION	SHORTS (PTECO)	DRC (PTECO)	SHORTS (PCECO)	DRC (PCECO)
DESIGN1	15	144	28	167
DESIGN2	27	362	27	362
DESIGN3	9	174	11	171
DESIGN4	29	243	29	260
DESIGN5	12	114	9	107
Percentage			**13.04**%	**2.89**%

Resource Utilization (Cores and Memory)

	PTECO	PCECO
CORES	92 Cores/Hr.	24.4 Cores/Hr.
Memory	1088GB/Hr.	345.6GB/Hr.

72% Less Cores with PC

68% Less Memory with PC

HOW? Resource Distribution Illustration (PTECO vs. PC): ~10 hours normalized runtime

PTECO

1 x 8C/192GB (Master) × **10-hours DMSA**

14 x 6C/64GB (Slaves) × **10-hours DMSA**

PrimeClosure

1 x 16C/256GB (Master) × **1-hour DMSA**
9-hours SMSA

14 x 6C/64GB (Slaves) × **1-hour DMSA**

Comparison Results

- AI-driven ECO (Leakage Power Saving)

Design 4	PTECO	PC	PC (AI-driven)	Diff (vs PTECO)
LVT%	5.63	5.86	5.31	-0.32
SVT%	67.31	64.65	62.45	-4.86
HVT%	27.06	29.50	32.24	5.18
PTPX				
Total Power [mw]	2.612	2.510	2.419	7%
Dyanamic Power [mw]	0.330	0.330	0.330	0%
Leakage Power [mw]	2.281	2.180	2.088	8%
		4%	4%	
Timing				
R2R Setup TNS	-1.06	-0.32	-0.32	70%
Number of R2R Setup Viols	8	6	7	-1
Number of R2R Hold Viols	78	89	87	9

High-Leakage Cell Usage

Low-Leakage Cell Usage

Total ~8% reduction in leakage power without affecting timing:-

i. ~4% leakage power saving has been achieved with PrimeClosure (vs PTECO).

ii. Another ~4% leakage power reduction is observed with PrimeClosure AI-driven ECO enabled.

A fully automated flow for further advancing PPA

Future Technologies & Enhancements

Production release of new & advanced 'AI-driven ECO' technology.

Clock-Surgery with splitting/cloning technique

Improving Ease-of-Use : Eliminating DEFs and LEFs input collaterals when NDM

Summary

Timing	19% Setup TNS improvement 2% Hold TNS improvement	**Resource**	68% Less Memory 72% Less Cores
Power	5.3% Leakage improvement	**Runtime**	20% Runtime improvement

In conclusion, PrimeClosure™ has the potential to reduce ECO efforts and iterations at advanced nodes for high-speed and high-density designs, while also accelerating design closure and time-to-market.


THANK YOU
Our Technology, Your Innovation™

Comparison Results (Block ECO)

- With Clock-Surgery Enabled

Timing
(Intra-Block Only + post-ECO)

Block	Advanced Node	# of New Clock Cells	Total Setup TNS (Before)	Total Setup TNS (After)	Total Hold Viols (Before)	Total Hold Viols (After)
Design 2	N	28	-8.9	-7.7	94	348
Design 5	N+1	1	-3.24	-3.02	409	1108
Average Diff				12%		-953

Routing

Total DRC (Before)	Total DRC (After)	Total Short (Before)	Total Short (After)
852	867	20	17
97	99	23	24
	-17		2

Power

Total PWR (Before)	Total PWR (After)	Leakage PWR (Before)	Leakage PWR (After)
39.02	39.08	6.64	6.72
30.34	30.45	12.5	12.6
	-0.25%		-0.94%

Total Setup TNS is further improved by **~12%**

Comparable

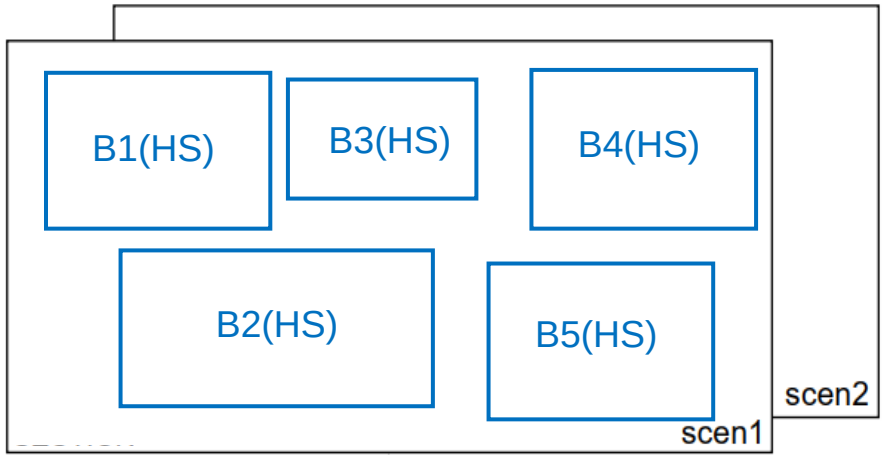
Power is only increased slightly

An additional ECO loop may be required to address hold degradation at lower buckets, primarily caused by pre- and post-ECO miscorrelation.

Hierarchical ECO

Hierarchical ECO Flow at Section/Full-Chip Level (w/ Hyperscale)

Section STA (w/ HS)



Only focus on inter-block/section optimization to reduce runtime and memory usage

write_eco_session

```
# Start pt_shell -m for ECO (non DMSA)
read_verilog; link;
# Each scenario includes HS block models:
# set_hier_config -block Block1 -path $model_block1
# set_hier_config -block Block4 -path $model_block4

update_timing

write_eco_session -include {pt_session smsa_data} \
-smsa_data_types {setup hold max_transition
max_capacitance pin_slew drc_max_transition
drc_max_capacitance } -smsa_data_format binary

-smsa_netlist_data {<path to block1.v> <path to
block2.v> <path to block3.v> {<path to block4.v> {<path
to block5.v> {<path to Top.v> } \
-smsa_spef_data {<path to block1.spef.gz> <path to
block2.spef.gz> <path to block3.spef.gz> {<path to
block4.spef.gz> {<path to block5.spef.gz> {<path to
Top.spef.gz> } \
$sh_launch_dir/section_eco_sess_binary_scen1
```

Path to full Verilog file

Path to full Spef file

pt_shell

scen2

Hierarchical ECO Flow at Section/Full-Chip Level (Recipe)

pc_script.tcl

```
set multi_scenario_working_directory PC_DMSA; set_host_options -num_processes 12
set_technology –node <N>

# Additional settings from set_eco_options can be included here
read_physical_data  -tech $tech_lef  -lef $lef_files

# Voltage areas
read_physical_data -def {Top.def} -physical_constraint_file {Topva.tcl}
read_physical_data -def {B1.def} -physical_constraint_file {B1va.tcl}
read_physical_data -def {B2.def} -physical_constraint_file {B2va.tcl}
…

read_eco_session section_pre_eco_scen1 -scenario_name scen1 # Section level sessions
read_eco_session section_pre_eco_scen2 -scenario_name scen2 # Section level sessions
start_eco -mode smsa -smsa_data_type {setup hold max_transition pin_slew
    drc_max_transition drc_max_capacitance} \

# Enable technology specific settings
fix_eco_drc
fix_eco_timing -type setup
fix_eco_timing -type hold

# report_eco_summary or other SMSA reporting commands
ecotclout -icc2 <eco_changes.tcl>
```

- Configure Machine Resources for STA
- Enable technology specific settings
- Provide the standard LEF, DEF and VA (Voltage Area) inputs for physical information for TOP and blocks
- Read PT pre-ECO sessions
- Conduct ECO operations
- Write out hierarchical changes for implementation.

Hierarchical ECO Flow at Section Level (Comparison Results)

Section Hyperscale Testcase

- Consists of 16 blocks
- ~14M instances (~30% involving inter-block logics)

PTECO

	Total Violations			
	Before PTECO		After PTECO	
Scenario	Setup	Hold	Setup	Hold
PVT1_vmid_min	0	861	0	2
PVT2_vmid_min	0	523	0	3
PVT3_vhigh_min	0	6104	0	55
PVT4_vlow_min	0	356	0	0
PVT5_vlow_max	8	0	0	0
PVT6_vmid_min	0	1907	0	1
PVT7_vmid_max	121	0	0	0
PVT8_vlow_max	10	0	0	0
PVT9_vmid_max	835	0	25	0
PVT10_vmid_max	194	0	0	0
PVT11_vhigh_max	1504	0	235	0
PVT12_vhigh_max	1426	0	366	0
Total	**4098**	**9751**	**626**	**61**
Fix-Rate			**85%**	**99%**

PrimeClosure

Group : all_group	Original setup	hold	Current setup	hold
Critical Path Slack:	-0.05	-0.21	-0.04	-0.08
Total Negative Slack:	-155.68	-278.73	-33.10	-11.17
No. of Violating Paths:	16497	29025	3076	674
TNS of Violating Endpoints:	-20.60	-58.9	-3.08	-1.82
No. of Violating Endpoints:	1879	8345	284	164

Hold

Setup

Key takeaway: Based on pre-ECO what-if analysis, PrimeClosure demonstrates >20% better setup timing than PTECO in terms of violations.

Comparison Results (Block ECO)

- With Clock-Surgery Enabled

Timing
(Intra-Block Only + post-ECO)

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PVT5_vlow_max	8	0	0	0
PVT6_vmid_min	0	1907	0	1
PVT7_vmid_max	121	0	0	0
PVT8_vlow_max	10	0	0	0
PVT9_vmid_max	835	0	25	0
PVT10_vmid_max	194	0	0	0
PVT11_vhigh_max	1504	0	235	0
PVT12_vhigh_max	1426	0	366	0
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