Efficiency Unleashed: Signoff Abstract Model's (SAM) Resource Mastery, Guaranteed QoR and Turbocharged TAT in Static Multi Voltage Verification (SMVV) space

Shauvik Panda
Abhijeet Kumar
Mugdha D Alurkar
Intel India Pvt. Ltd.

Agenda

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- Traditional Static LP Verification Challenges
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- Retention Principle
- Incremental Features of SAM
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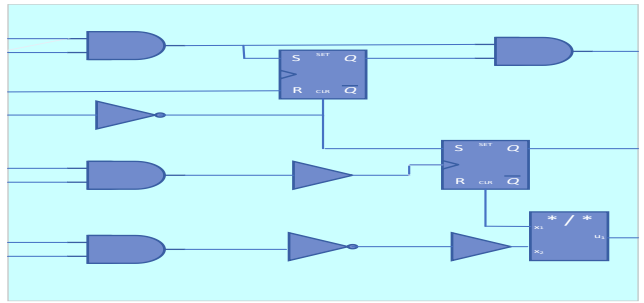
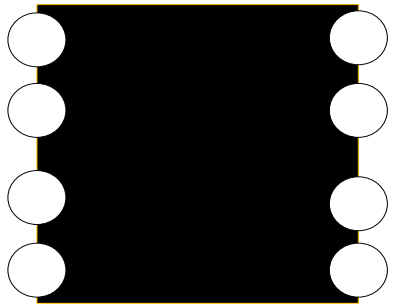
Traditional Static LP verification Challenges

- As Design sizes grow and advanced power-aware architectures become prevalent, it is crucial to implement early and efficient Static Multi Voltage Verification (SMVV) as a part of convergence and signoff.
- LP checker tool will perform comprehensive SMVV for UPF correctness & implemented power-intent later in the design flow.
- Traditional SMVV follows 2 approaches:
  - Full Flat Flow
    - Full Low Power (LP) coverage.
    - High resource requirement .
    - High Turn Around Time (TAT).



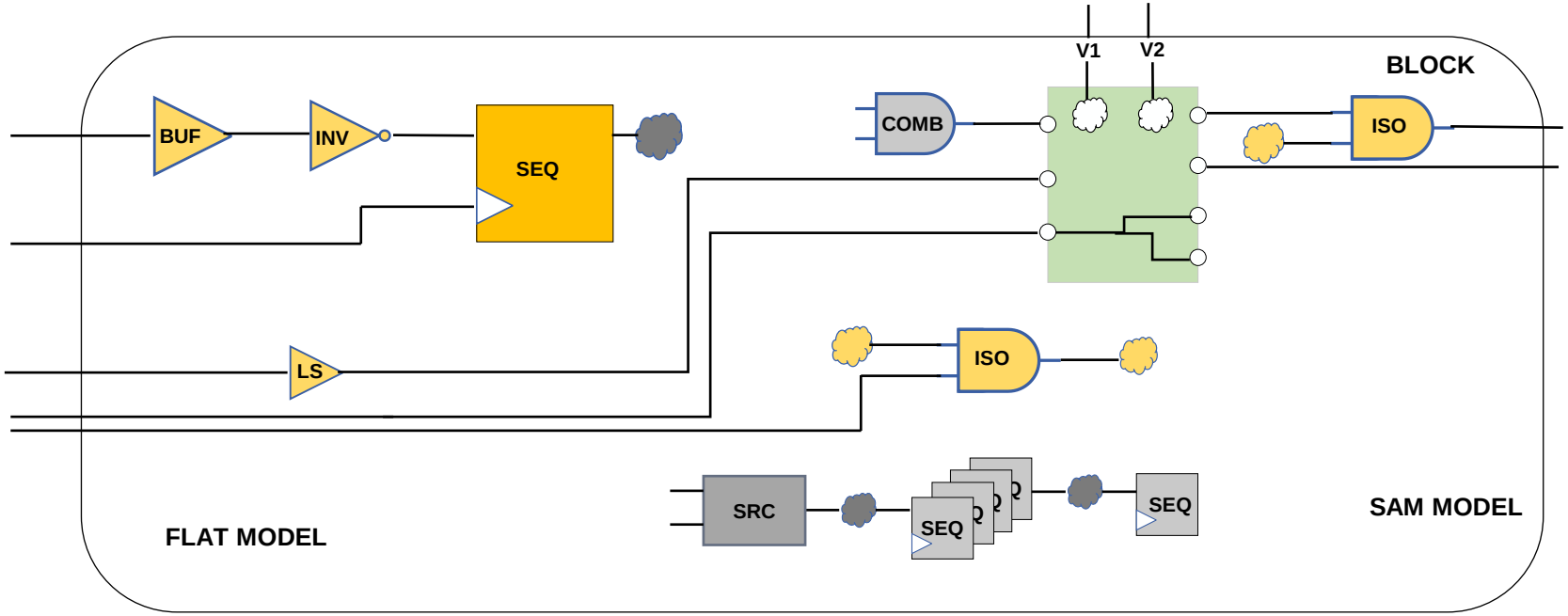
  - Black Box Flow
    - Lesser TAT and resource requirement.
    - Less coverage.
    - LP information lost.



Need a robust solution overcoming TAT and resource upshift while maintaining LP coverage intact.

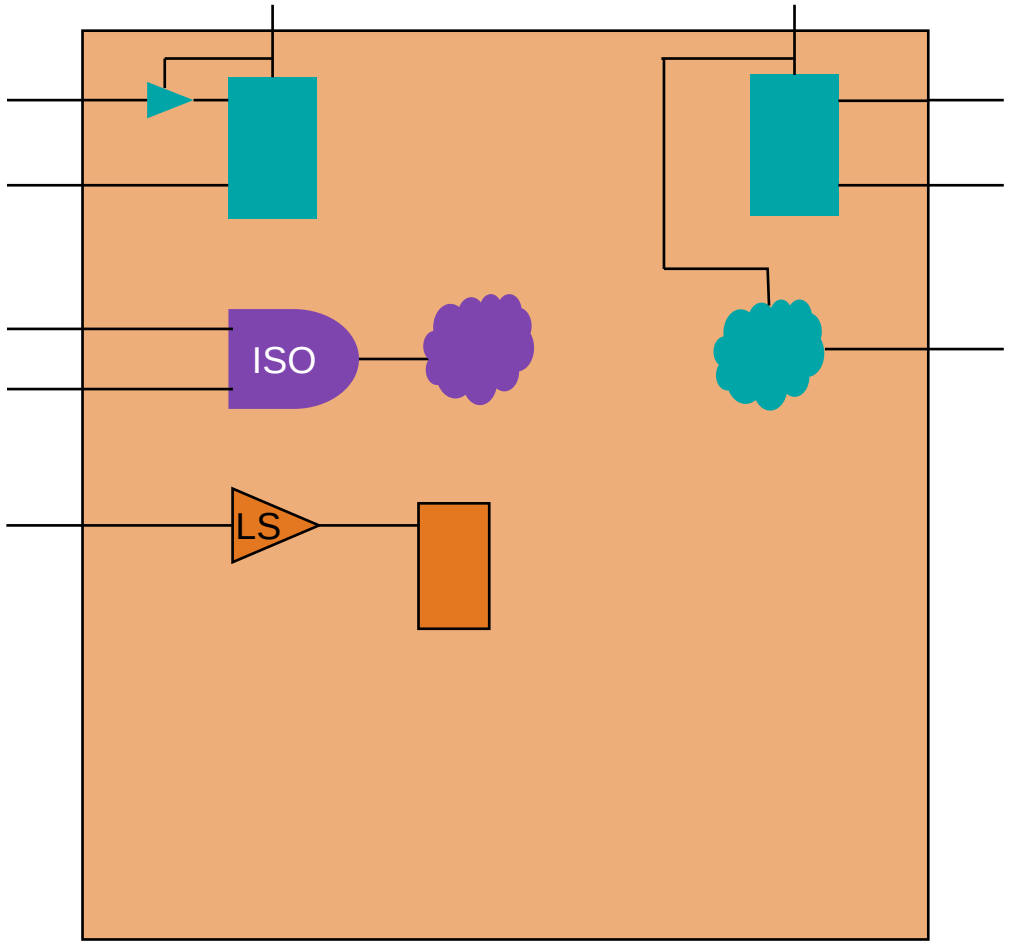
What is SAM Model?

- Signoff Abstract Model (SAM) is a leaner retained model created out of original netlist taking into consideration the UPF constructs.
- The main retention logic principle it follows “starting from all Primary Input (PI)/Primary Output (PO) traverses forward/backward, goes through all buffers, inverters, power management cells and stop at first cell/operator which is not part of the aforementioned elements”.
- The model goes in hand with flat UPF.



Retention Principle

1. PI & PO connected cells
2. All supply nets connected to retained PG pins
3. ISO cells connected to PI/PO
4. LS cells connected to PI/PO



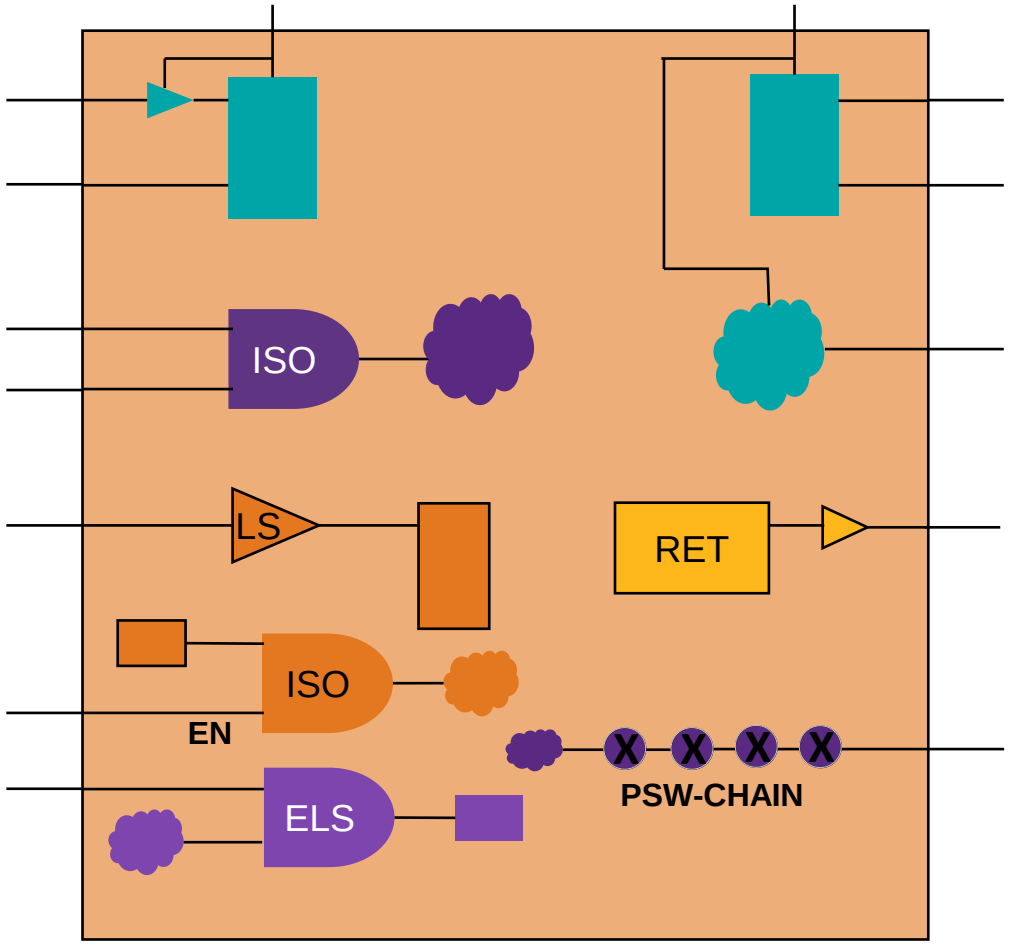
Retention Principle (Contd.)

5. Retention cells connected to PI/PO

6. LP cells control pin connected to PI/PO

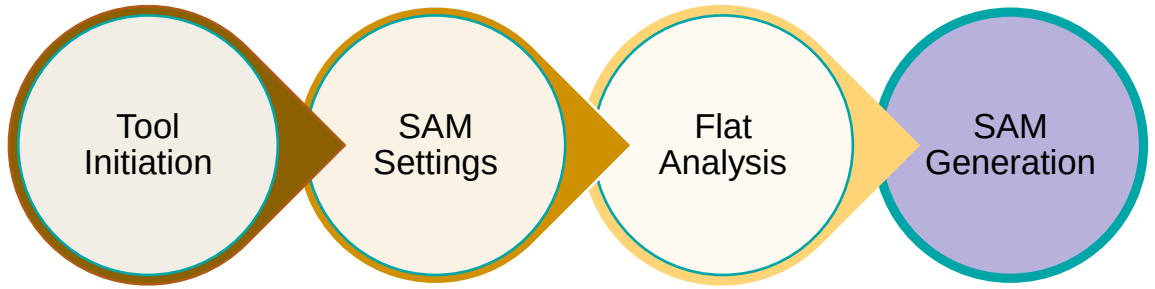
7. Full crossover path of all input of LP Cells if any connected to PI/PO

8. Full Power switch chain if any input/output connected to PI/PO

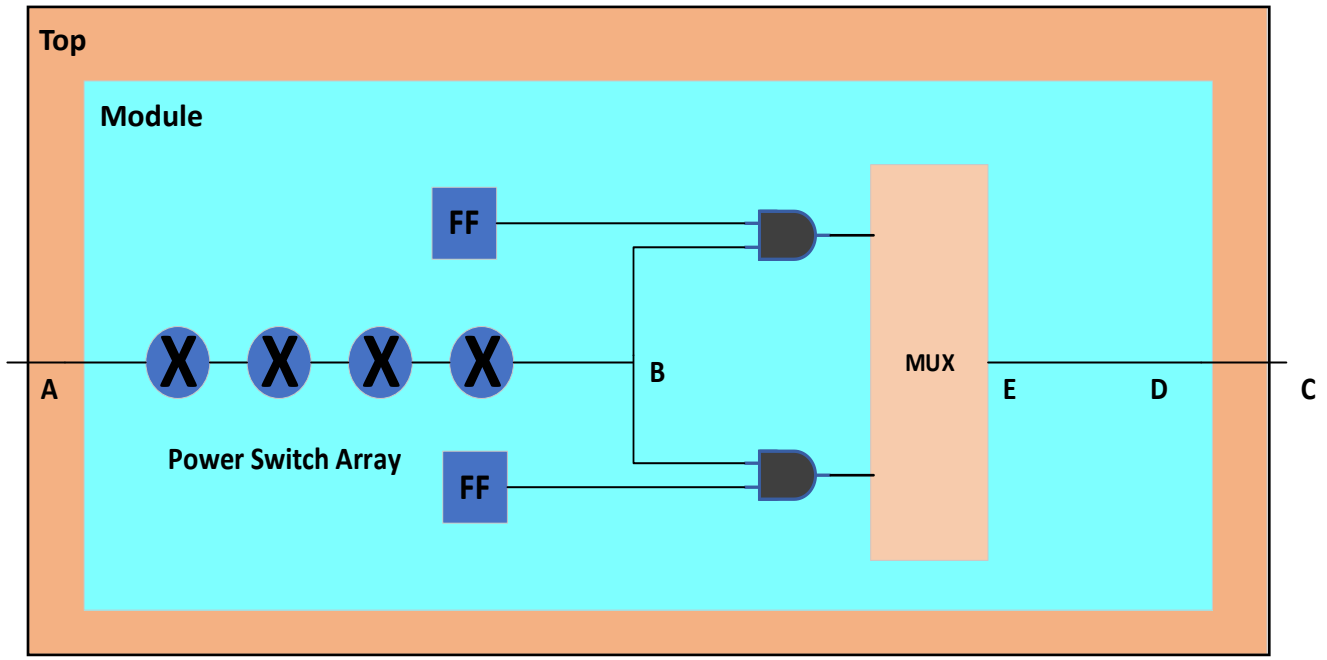


Incremental SAM Updates

- Single Go Execution-
  - Normal LP Execution with SAM generation.
  - Unaltered Block QoR.

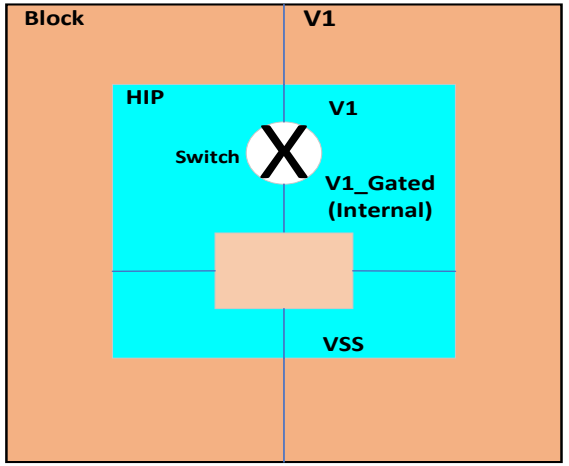


- Power Switch Retention-
  - Retention principle supports PI/PO related connection. (e.g. A->B and C -> E retention)
  - Update to more retention due to connection validation. (e.g. Flop, AND gate & Multiplexer)



Incremental SAM Updates (Contd.)

- Support for Virtual Supplies-
  - Virtual supplies present in PST.
  - PST merging requires these definitions preserved.



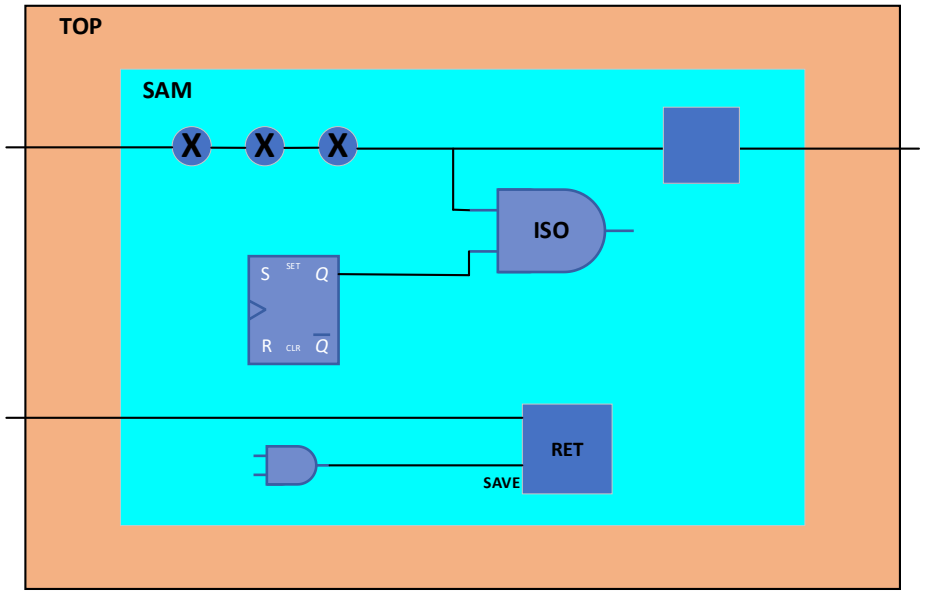
Create_supply_net V1_Gated

Connect_supply_net V1_Gataed –ports HIP/V1_Gated

Add_port_State .. V1_Gated ..

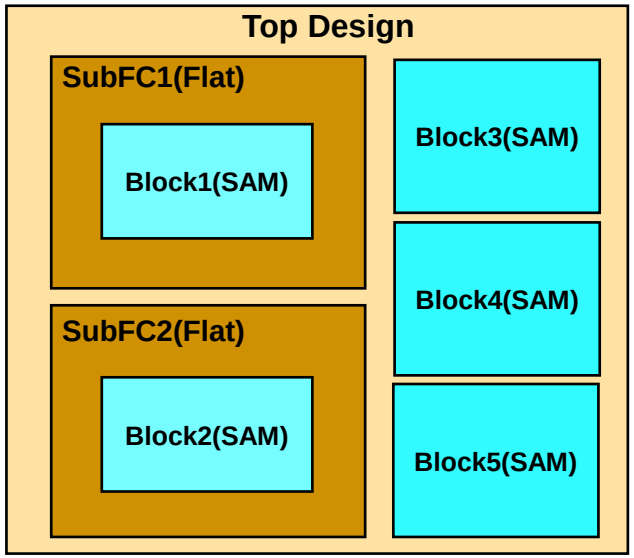
Create_pst .. –supplies { .. V1_Gated ..}

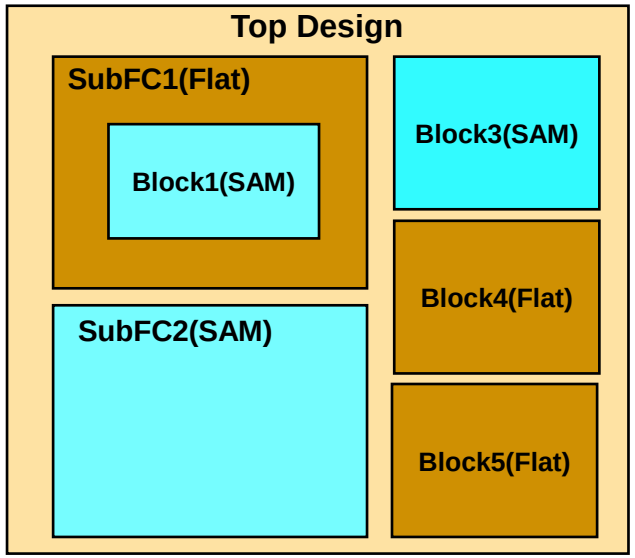
- Extra Logic Retention
  - Extra retention for control signals.
  - Control and driving logic preserved.

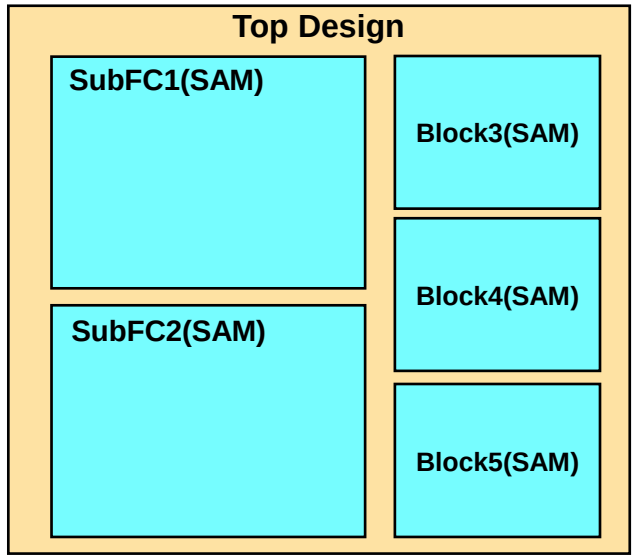


SAM Execution Model

- SAM models can be used in different versatile combinations as per design need.
- Best execution model will always be - All blocks are used as SAM in design.

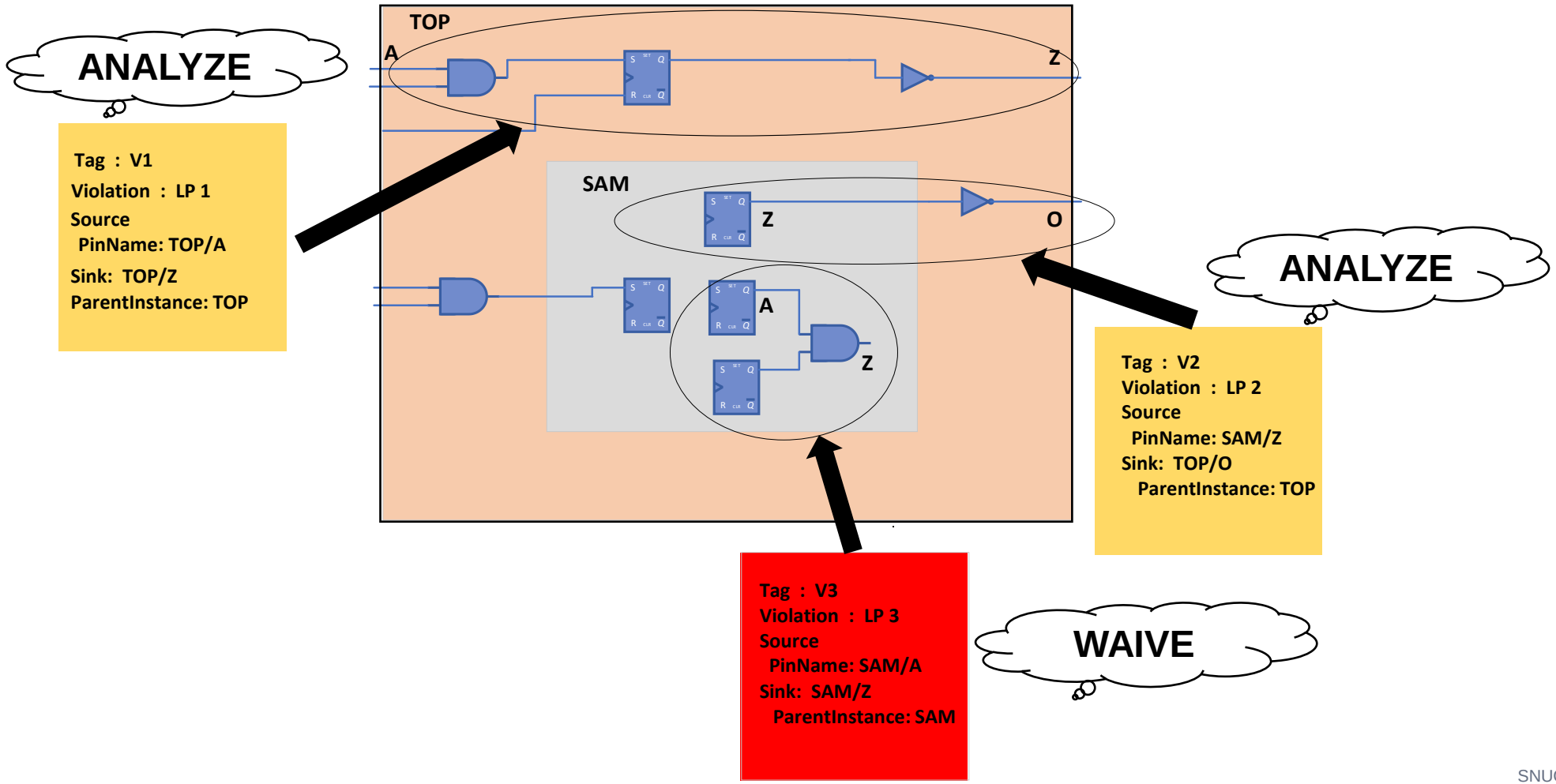






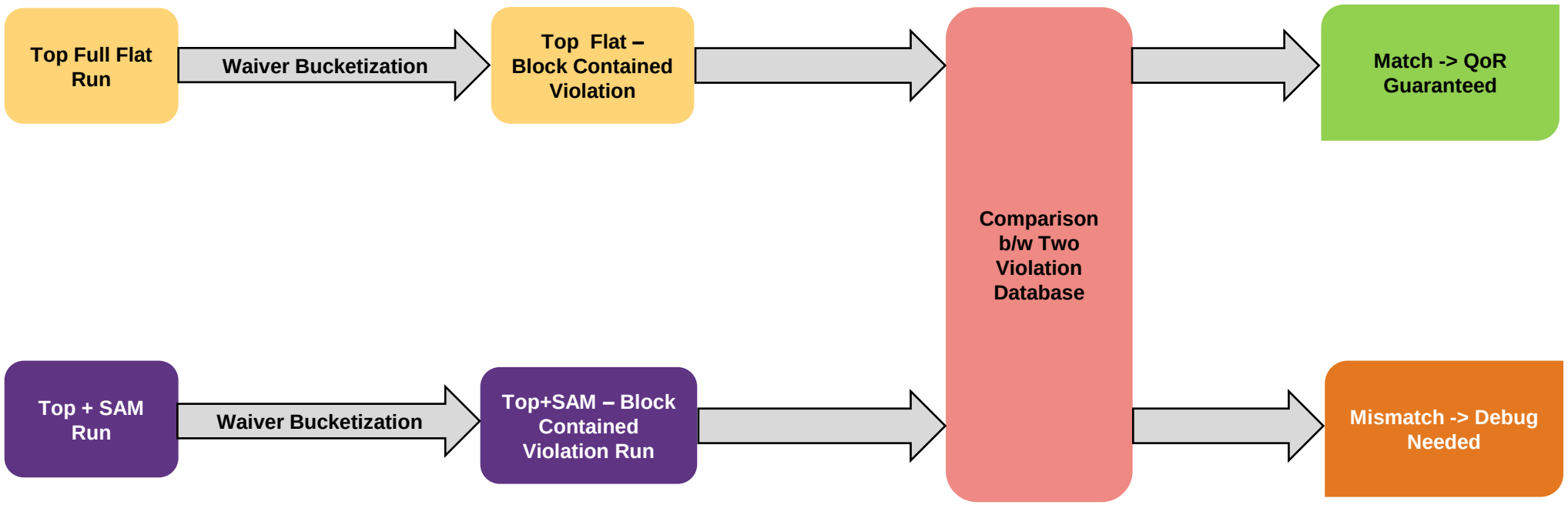
QoR Flow

- Subtractive QoR flow
  - Waiving pure block contained issues.

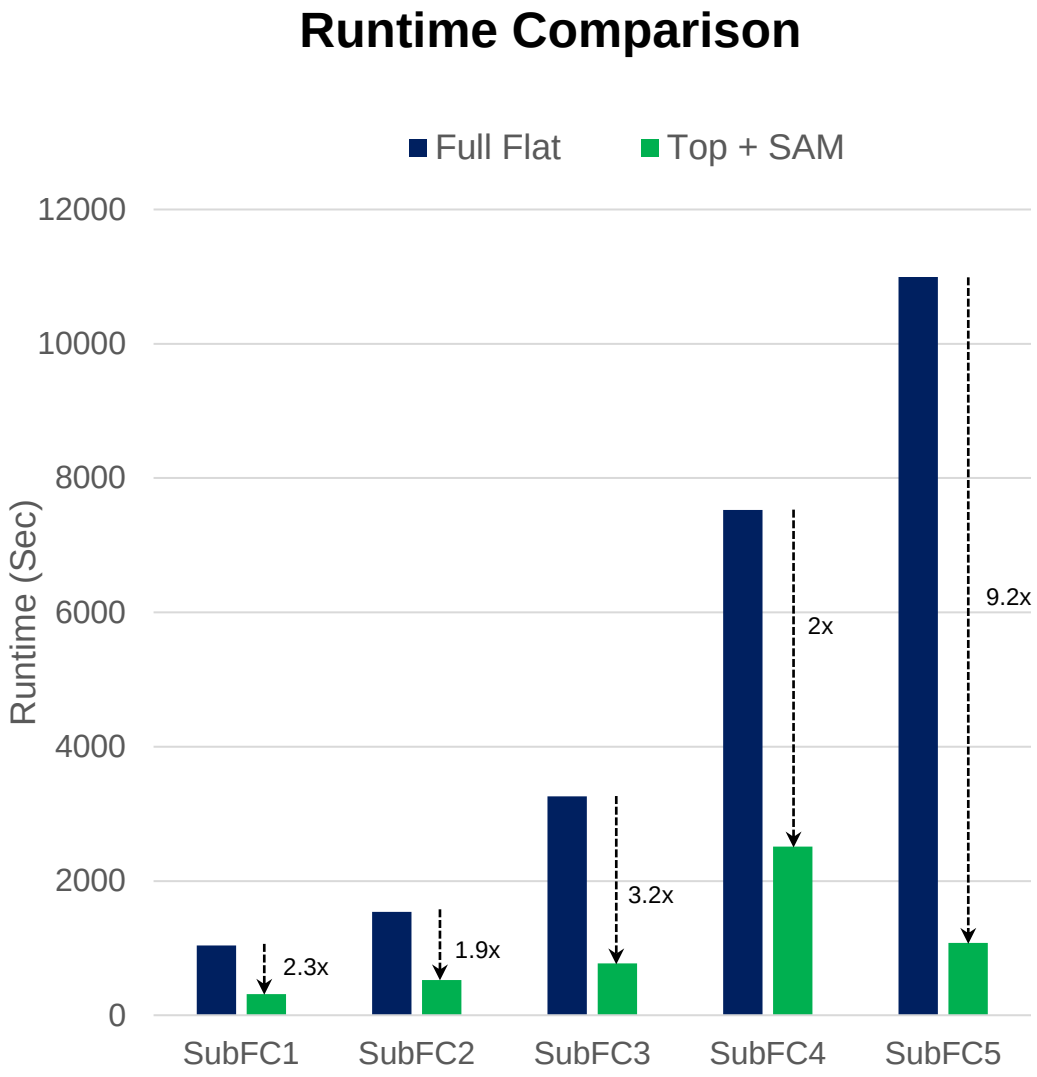


QoR Flow (Contd.)

Paranoia checks can perform comparing with full flat run.



Result


Runtime Comparison
Full Flat
Top + SAM
Runtime (Sec)
12000
10000
8000
6000
4000
2000
0
2.3x
1.9x
3.2x
2x
9.2x
SubFC1
SubFC2
SubFC3
SubFC4
SubFC5


Memory Comparison
Full Flat
Top + SAM
Memory (GB)
120
100
80
60
40
20
0
0.6x
0.6x
0.9x
1.2x
3.1x
SubFC1
SubFC2
SubFC3
SubFC4
SubFC5

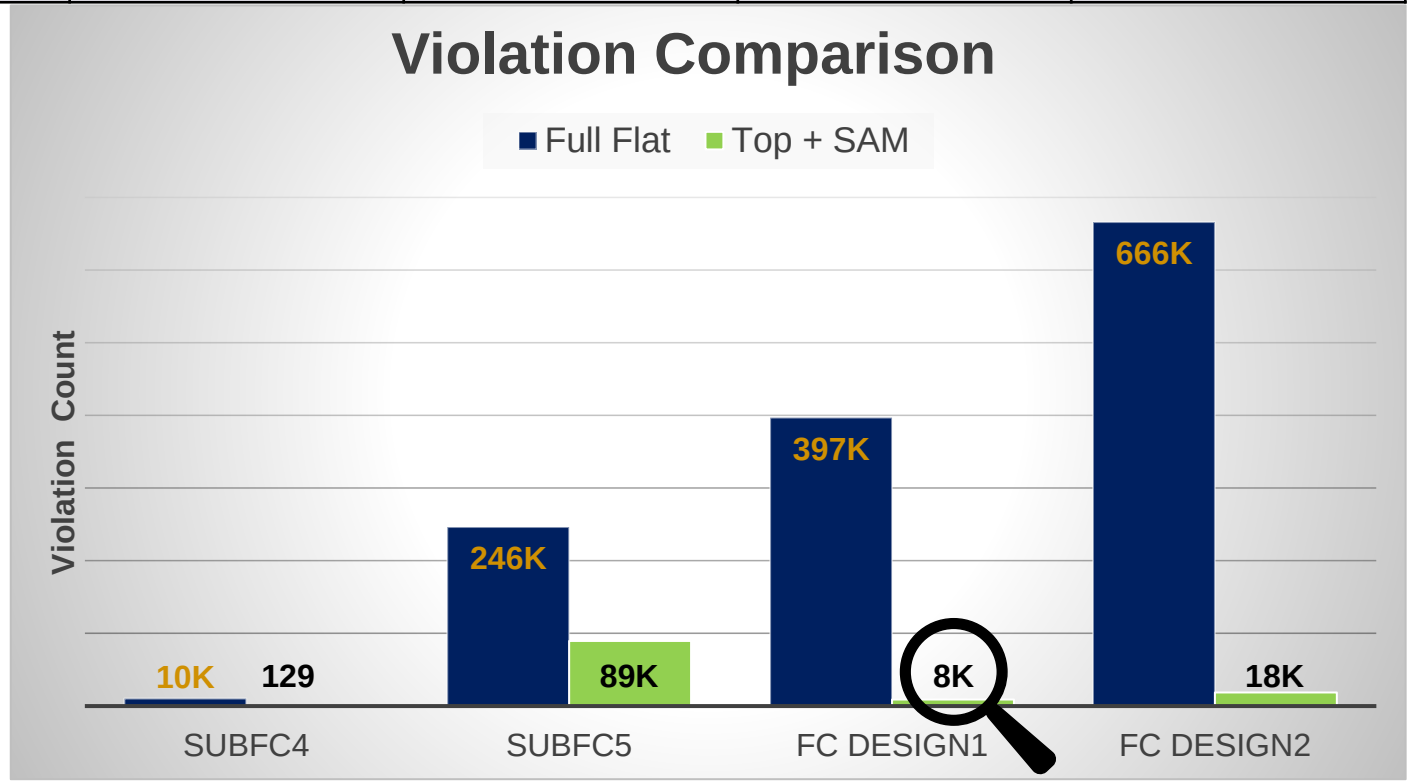
Result (Contd.)

Design	Full Flat Runtime (Hrs)	Top + SAM Runtime (Hrs)	Benefit	Full Flat Memory (GB)	Top + SAM Memory (GB)	Benefit
FC Design1	94.8	10.1	9.39	351	98	3.58
FC Design2	114	11.45	9.95	412	101	4.07

Runtime benefit : 3 to 10x

Memory resource benefit : 1.5 to 4x

Debug cycle reduced ~30% due to removal of block contained violations



Conclusion

- The Donut netlist model created by SAM offers both runtime improvement and resource reduction, making it most efficient static LP verification method.
- Guaranteed QoR with a shorter debug cycle accelerates the static LP convergence goals.
- Recommended methodology for all future multi-billion gates design.

- Working with vendor on-
  - ❑ On the fly identification and generation of SAM.
  - ❑ Further lighter, faster version of SAM.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