A Comprehensive Framework to Overcome Interoperability Challenges using Synopsys PCIe Gen6 Verification IP

Arvind Kumar
Pramod Prasad
Vignesh Murali Babu
Gautam Kumar

DCSG
BROADCOM

Agenda

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- Importance and Need for Latest Gen. PCIe Devices
- Complexities in Development of PCIe Designs
- Interoperability of Verification for Different Designs
- Key features required for PHY IP Verification Sign-off
- Utilizing the Synopsys PCIe GEN-6 VIP for Early Test Bring Up, Scoping & Strategy

Importance and Need for Latest Gen. PCIe Devices

Importance and Need for latest Gen. PCIe Devices

- Each generation of PCIe offers faster data transfer speeds and PCIe Gen 6 is the latest generation offering significant advantages over previous generations
- PCIe Gen-6 offers a whopping 128 GB/s bandwidth for a standard x16 lane configuration
- This increase in bandwidth is crucial for feeding the ever-growing data demands of booming technologies like AI & ML. Faster data movements b/w components such as CPUs & GPUs makes the AI & ML tasks which rely on massive datasets & complex computations to yield better training times
- PCIe Gen 6 ensures that the systems are compatible with the future hardware that might demand higher bandwidths

Complexities in Development of PCIe Designs

Protocol Complexity

- PCIe Gen 6 almost feels like a completely re-branded version of the specification as compared to its predecessors, and still maintaining the backwards compatibility
- New transfer speeds, new data encodings, new packet structures, new error correction mechanisms, all to keep up with the signal integrity and maintain reliable communication across the link

Verification & Validation

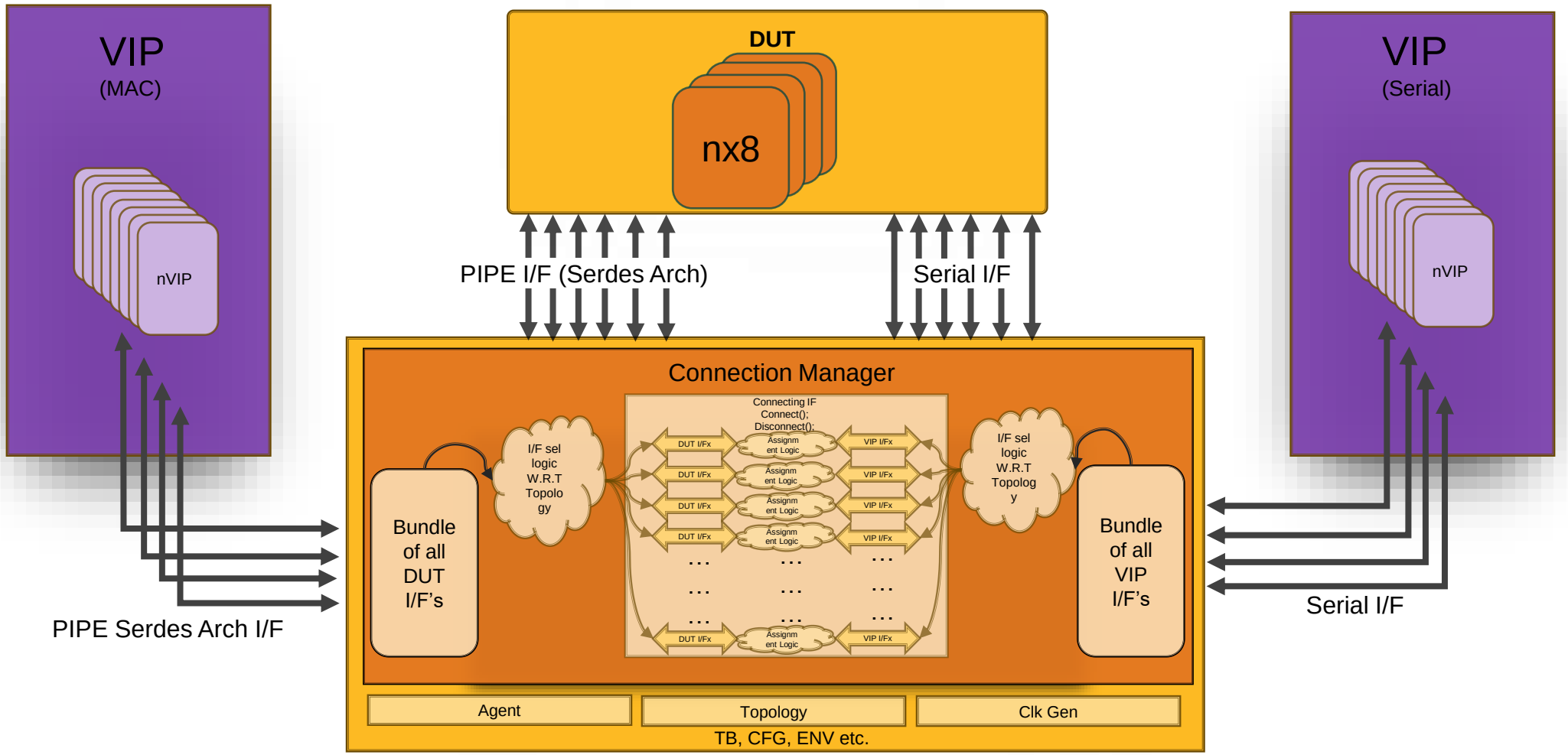
- Developing such complex protocol designs is a mammoth task and verification of it is a much more cumbersome and challenging task
- This is where a well architected Test bench and the VIPs come into picture to thoroughly verify & validate the designs within crunch timelines

PCIe Based Designs at BRCM for Interoperability Validation

1. PIPE subsystem with PIPE 6.0 SerDes Arch with MAC and Remote PHY connectivity
2. PCIe Switch Gen6
3. PCS with PIPE 5.x features

Design – 1

PIPE subsystem with PIPE 6.0 SerDes Arch with MAC and Remote PHY connectivity

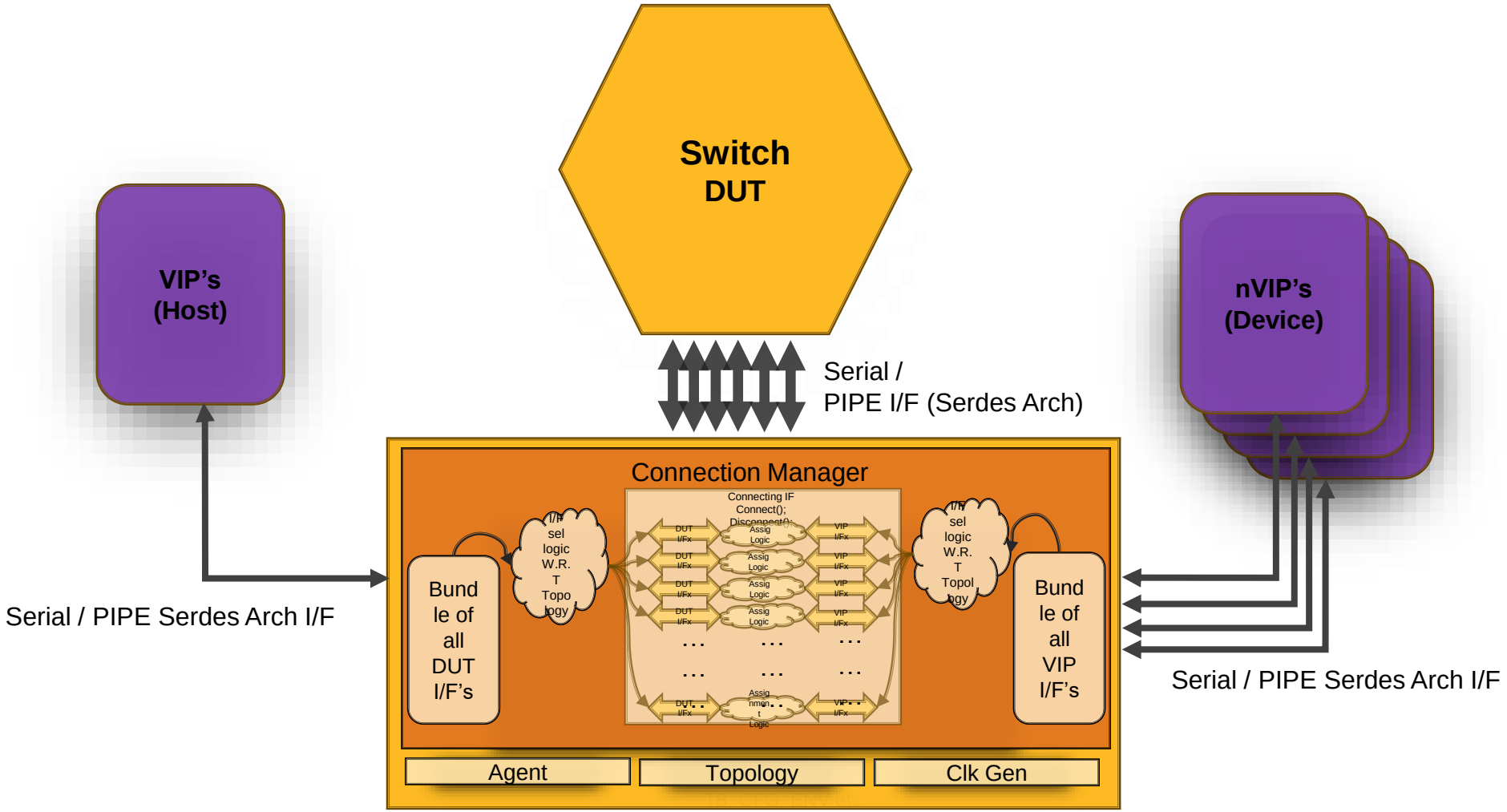


PIPE Subsystem

- Verification of PCIe PIPE Sub-system Gen6 64 GT/s Serdes Architecture pipe parallel interface on one side and remote serial link partner on the other end with (NRZ / PAM4) signalling
- Multiple random topologies utilizing the VIP class configurable link-width capabilities with X1 / X2 / X4 / X8 / X16 PCIe links
- All clocking topologies
  - IR (Independent RefClk) – SRNS / SRIS
  - Common Clocking – with and without SSC
  - Configurable ppm tolerance, ssc spread, ssc modulation rate
- Score boarding, end to end TL / DL / PL / Flit
- Lane margining (Local), Power down – L0p, Dynamic link speed change, link width change
- Equalization with random eq presets, user configurable coefficients, bypass cases, abort cases

Design – 2

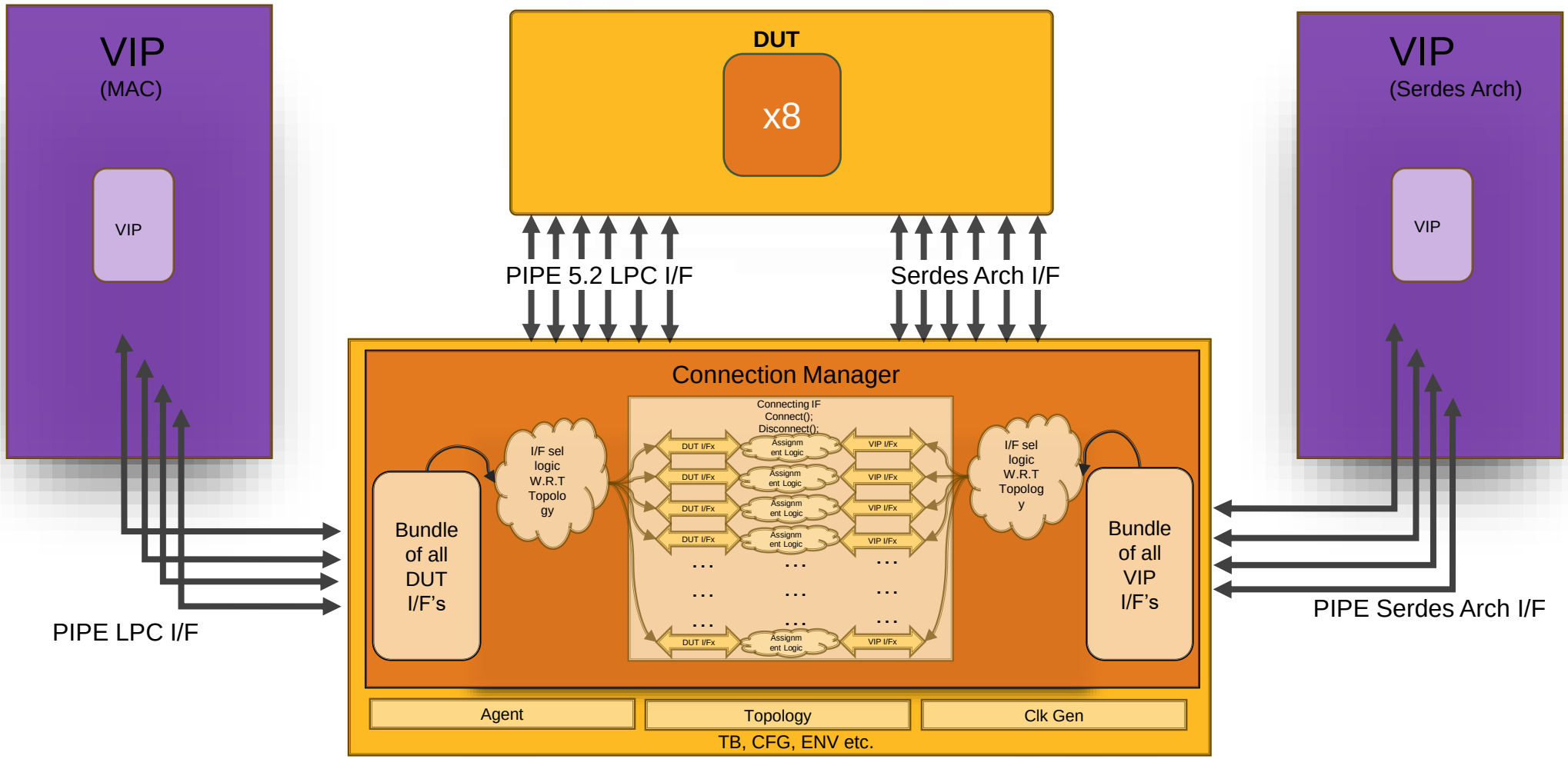
PCIe Switch Gen6 with PIPE Serdes arch interface, Serial interface



PCIe Switch

- Verification of PCIe PIPE Sub-system Gen6 64 GT/s Serdes Architecture pipe parallel interface in one mode and remote serial link partner on other end with (NRZ / PAM4) signalling in another mode
- Multiple random topologies utilizing the VIP class configurable link-width capabilities with X1 / X2 / X4 / X8 / X16 PCIe links.
- All clocking topologies
  - IR (Independent RefClk) – SRNS / SRIS
  - Common Clocking – with SSC, without SSC
  - Configurable ppm tolerance, ssc spread, ssc modulation rate
- Score boarding, end to end TL / DL / PL / FLIT
- Error injection
- PCIe Compliance testing

Design – 3
PCS with PIPE 5.x features



PCS PIPE 5.x

- Verification of PCIe PIPE PCS dut with low pin count M-PIPE interface on one side and Serdes Architecture S-pipe interface on the other side
- Clocking topologies
  - SRNS
  - SRIS
- Score boarding, end to end TL / DL / PL
- Power down – L0s, L1, L1 sub-states (L1.1, L1.2)
- Equalization at all Gen3 and above speeds with random presets, user configurable coefficients, bypass cases, abort cases
- Reset cases (hot reset, link disable etc.)

Key Features Required for PHY IP Verification Sign-off

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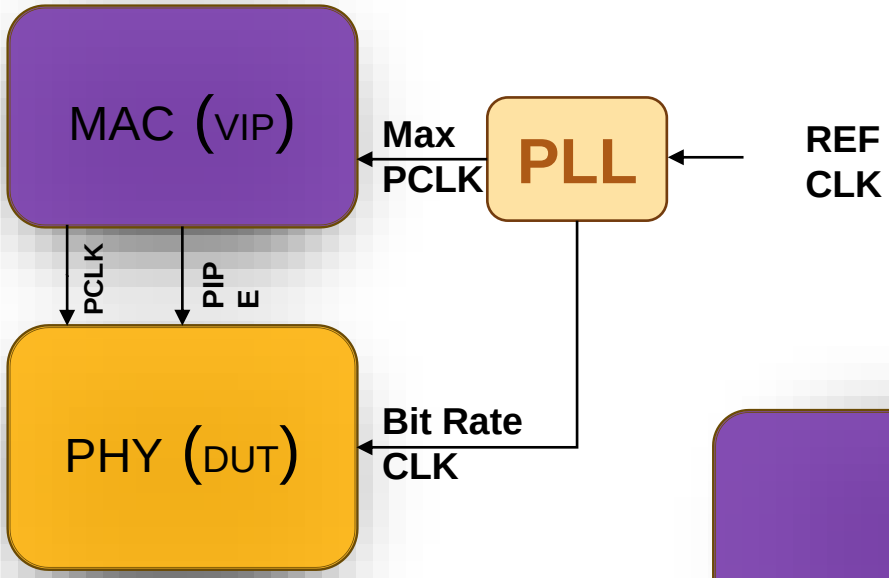
- Different test-bench topology architectures
- Keeping interoperability and maximum reuse across environments
- Support for PIPE architectures, clocking architectures
- PCIe Protocol verification - PCIe traffic verification, dynamic reset and reconfiguration, equalization, compliance, loopback, lane margining, and error verification
- Scoreboarding at every layer (TL,DL,PL,FLIT) data integrity

Utilizing the PCIe GEN-6 VIP

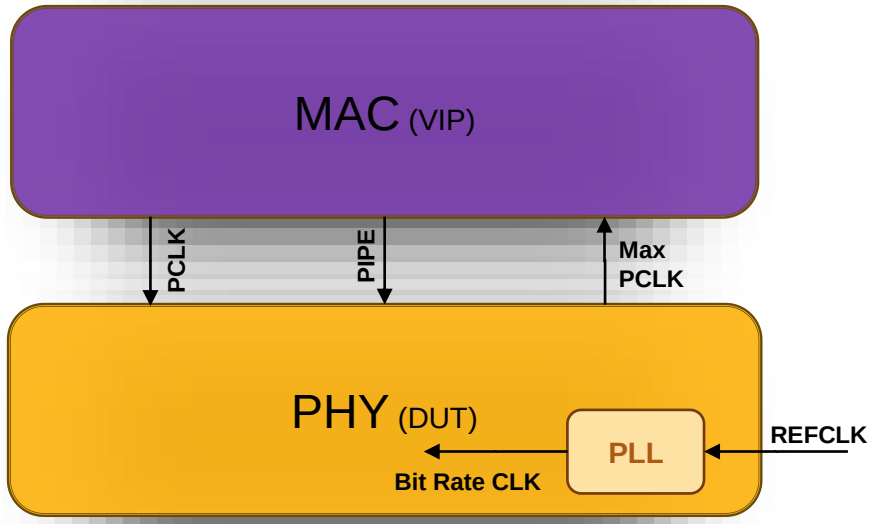
- The early availability of PCIe Gen6 VIP helped in scoping out and putting up a strategy for the verification plan of the design
- The extensive Gen-6 feature lists available as part of VIP, which helped for quick test completion turnaround time
- Feature lists along with support for custom enhancements which helped to focus on key & critical verification goals like skipping physical layer rates, bypass equalization, LTSSM timers
- Descriptive Transaction logs (Symbol log, TLP log, FLIT log) with timestamps helps in faster analysis
- Diagnostic/statistical variable for debug, coverage, checks, and verification closure
- Enhanced VIP support for compliance testing (fine control of compliance iterations by transitioning to a designated rate/setting shortening the simulation run-time)

PCIE PIPE Clocking Architectures

- PCLK as phy input with external PLL mode
  - PIPE S-pipe VIP PCLK as input with DUT generated PCLK and PLL outside the DUT
  - PIPE M-pipe VIP Max PCLK as input with TB generated PCLK
- PCLK as phy input with phy owned PLL
  - PIPE M-pipe VIP Max_PCLK as input from DUT generated clock



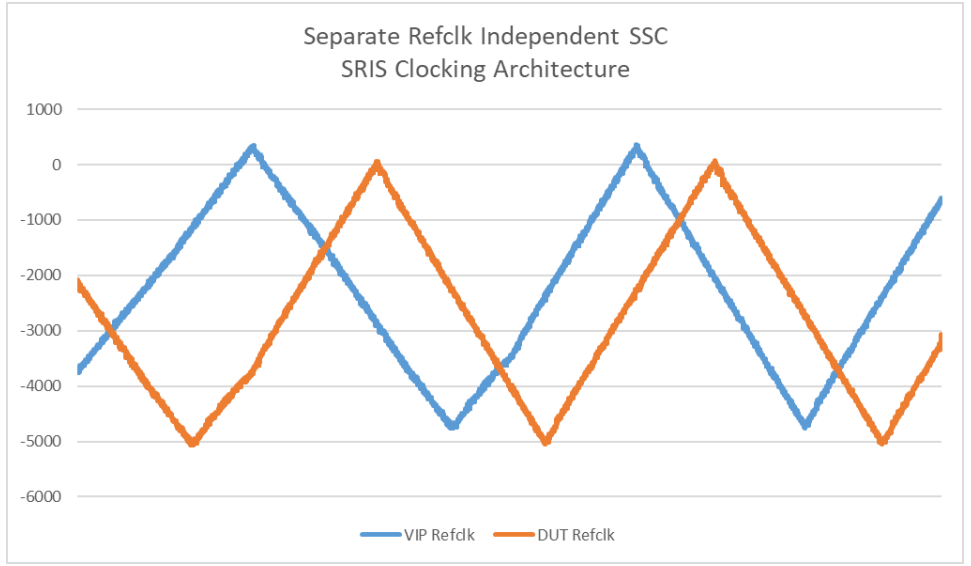
PCLK as PHY Input with External PLL

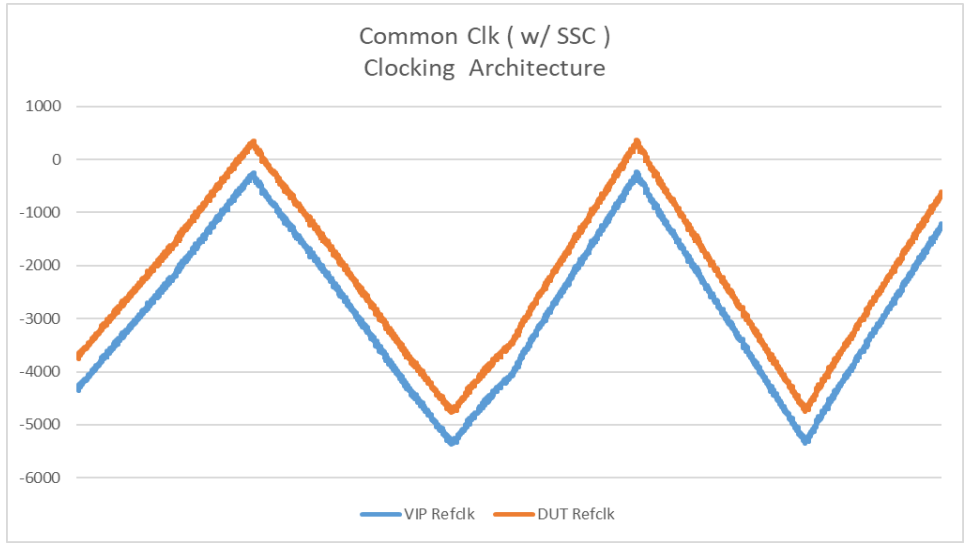


PCLK as PHY Input with Phy owned PLL

PCIE Clocking Architectures

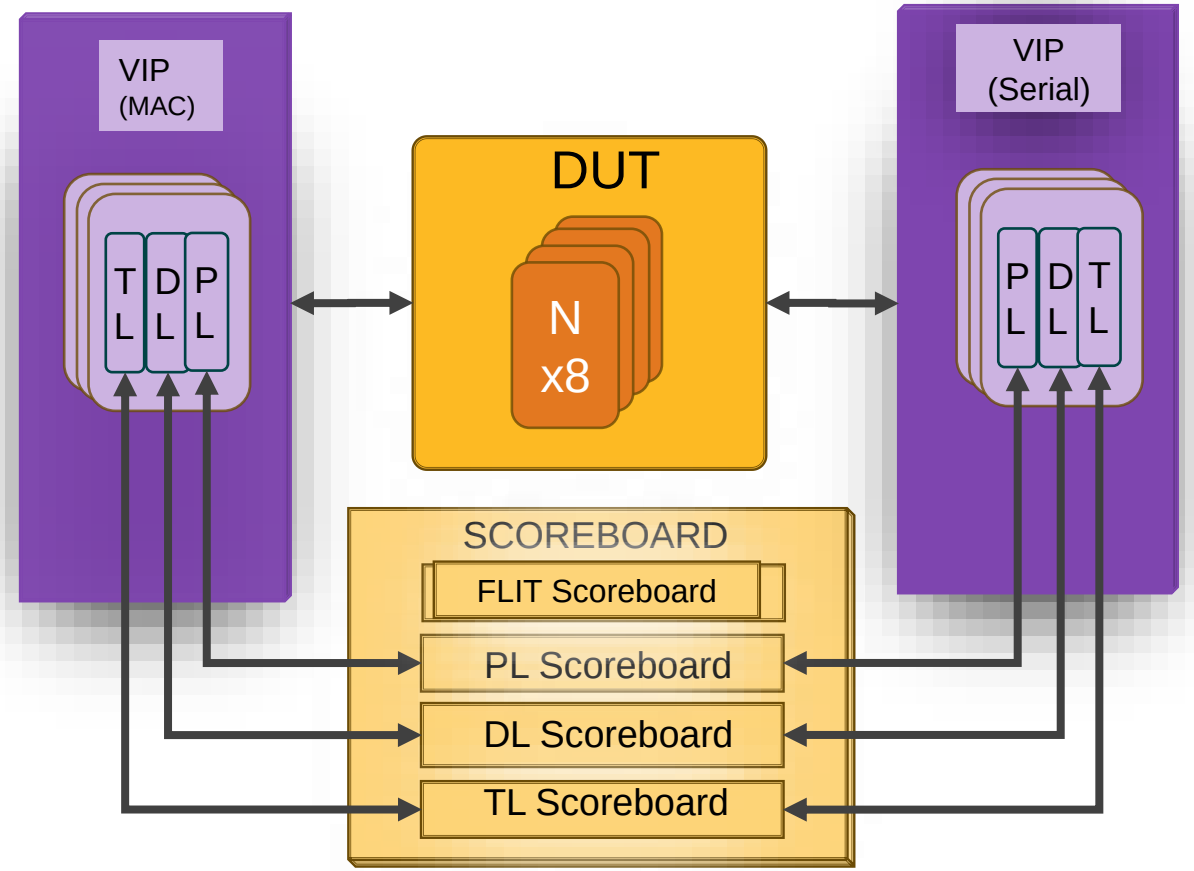
- IR
  - SRNS
  - SRIS
  - Mixed Clocking (Some VIP instances SRNS, some SRIS in the same simulation & topology)
- CC
  - Common Clock with SSC
  - Common Clock without SSC





Scoreboard

- VIP's analysis ports at different protocol layers (TL/DL/PL/FLIT) used in data integrity scoreboarding
- VIP provides packets with field level information of the corresponding type (TLP/DLLP/OS)
- This enabled us to scoreboard all TLPs, DLLPs and OS in both Tx and Rx
- When in Flit mode, VIP's Flit packets used to do point to point scoreboarding of entire Flits



Error Verification

- PHY verification involves error verification at PL
  - Ordered sets (OS) corruption
  - Elastic FIFO overflow/underflow
  - Decode/Disparity Errors
- VIP’s callbacks used to corrupt individual symbols of all OS types and to create Decode/Disparity Errors
- Configurability of VIP to set the required clk ppm helped in verifying EFIFO errors
- VIP’s sequences used in creating other cases such as
  - Equalization Abort
  - Hot Reset
  - Link Disable
  - Lane margining

Summary

Summary

- Reusability of configs & sequences across different project test-benches and topologies
- Parameterized topologies, configurations, and integration with Synopsys Verification IP provided scalability across different designs
- Config driven connection manager provides seamless connectivity between design and VIP for different interfaces (PIPE / Serial / Serdes Arch)
- Support for run-time reconfiguration
- Synopsys VIP Improved runtime performance with reset and clock disable support
- Synopsys VIP Improved debug efficiency by having layered transaction logs

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