3D Process Simulation-Assisted Device Failure Analysis with Virtual Defect Injection in IC layout

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ABSTRACT

The development and use of nanotechnology has enabled the creation of submicron electronic devices with unprecedented levels of functionality, speed, and efficiency. While most of the semiconductor industry and its consumers are becoming increasingly dependent on nanoelectronics, these devices are becoming more susceptible to defects and transient faults. Non-Visual Defects (NVD) is a category of semiconductor material and process-induced defect that cause electrical failures but are not detected with visual wafer inspection tools or with fault localization tools. Devices with NVD may fail at any stage of their life cycle and may benefit from complex Failure Analysis (FA) investigations including software support to analyze design and diagnostic data. For a higher FA success rate, these investigations can be further supplemented with Technology Computer-Aided Design (TCAD) Process Simulation software to simulate a failure prior to actual physical analysis on limited device samples. In this work, we will showcase an innovative technique for simulating NVD using a 3D process model to pinpoint the exact process step where the defect was introduced. By injecting a new virtual defect layer in the original device data, we can emulate the failing device. We also present a real-life case study where defect simulation correlates well with the actual Transmission Electron Microscope (TEM) cross-section results.

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1. Introduction

With the growing complexity of semiconductor manufacturing processes, maintaining a high yield, or achieving process entitlement is paramount to reduce overall Time-To-Market (TTM) of silicon products and production costs [2].

One of the major challenges in solving the yield issues on early design lots is to identify the systematic defects and narrow them out to perform Root Cause Analysis (RCA) and FA. Failures in Integrated Circuits (IC) can be identified using structural testing techniques like Design for Test (DFT) which identifies possible candidate occurrences that may have caused the observed failure. Additional information such as design hotspots which are simulated and flagged through Lithography Rule Check (LRC) or stress models, is also collected to identify the defects. This data, if examined manually can take tremendous time to analyse and generate coherent information. Hence getting to the root cause of a single defect can become a long process.

Therefore, it becomes increasingly important to use statistical analysis to reduce the data volume and narrow down to a selection of best representative candidates for FA. These candidates are correlated and studied using lab analytical equipments and non-destructive FA techniques, which can be used to isolate faults. Some examples include Infrared (IR) Thermography, Photon Emission Microscopy (PEM), IR-Laser Stimulation and Electro-Optical techniques to localize the failure site. These methods can be further supplemented with software assistance such as CAD Navigation tools and Process Simulation Software for enhancing the existing fault isolation process [6][9].

2. FA Candidate Selection

By performing statistical analysis on design, manufacturing and test data, FA candidates can be reduced to a much lower number by identifying the ones which match the failure mechanism and are highly likely to represent the defects [8]. These candidates can then be imported into a CAD design software to perform RCA and confirm the defects (See Figure 1).

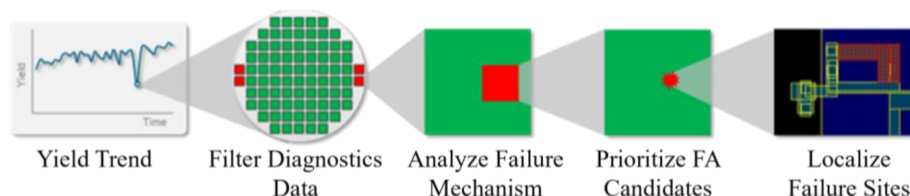

Figure 1. Volume Diagnostics for FA candidate selection.

Once the FA candidates are imported in CAD software, Electrical Fault Analysis (EFA) techniques can be used for fault isolation. However, NVD is a category of defect that causes electrical failures but cannot be clearly detected because they are beyond the imaging capabilities of Scanning Electron Microscopy [4] or undetectable with fault isolation techniques. Hence, TEM and other destructive Physical Failure Analysis (PFA) techniques must be used in such cases, which in turn creates many challenges for the FA engineer. In the subsequent sections, we will discuss these challenges and introduce a new workflow for virtual defect injection using TCAD Process Simulation software.

3. Defect Simulation

PFA also includes the usage of destructive techniques on device samples namely decapsulation, wet chemical etching, delayering, Focused Ion Beam (FIB) … [3]. However, executing these procedures accurately can be very challenging, especially for advanced technology nodes with shrinking device dimensions, where a simple error in sample preparation may lead to sample destruction or misinterpretation of the analyzed faults [5]. FA engineers cannot afford to make these errors, especially

when they receive limited Return Merchandise Authorization (RMA) samples in case of Customer Quality Complaint (CQC).

Furthermore, PFA is a time-consuming process and often the structural results cannot clearly explain or match the electrical characteristics of the analyzed devices [3].

TCAD simulation can be an effective tool to supplement the existing FA workflows and reduce PFA iterations. Using TCAD process simulation software, a structurally accurate and realistic device model can be created based on actual manufacturing process technology (layer) information [9] (see Figure 2).

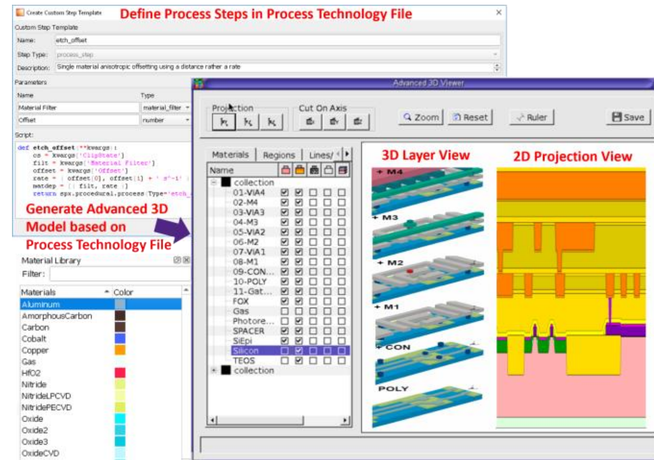

Figure 2. A process technology file is created based on manufacturing process technology information and design layers information.

This 3D process model can then function as a 'digital twin' of the actual device and can be used in conjunction with CAD software tools to pinpoint the critical process steps at defect location and assist in pre-visualization of the process layers and confirming the failure (see Figure 3).

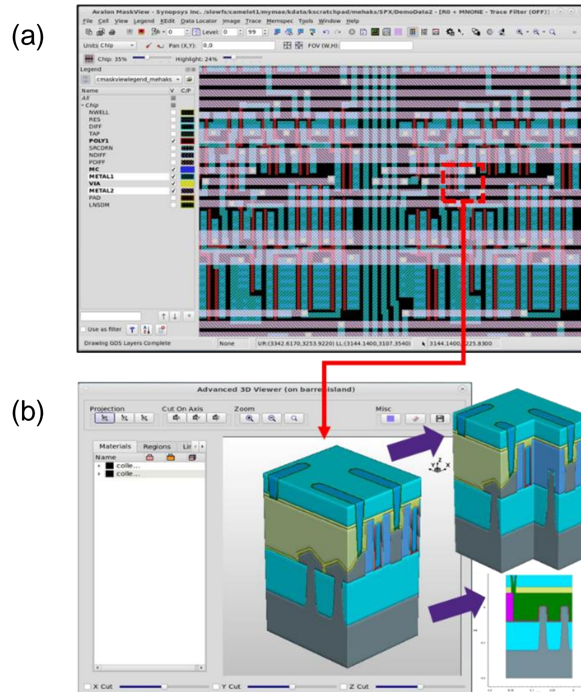

Figure 3. Selection of Region of Interest (ROI) for analysis (a), 3D cross-sectional view of ROI (with desired cut-sections and projections) exposing all the process layers (b).

3.1 Electronic Virtual (EV) Defect Injection

Furthering this concept, our work showcases a new feature to simulate the defect formation mechanism without altering the device sample physically. This is based on the principle of simulating a cut/deposit using an Electronic Virtual (EV) layer on top of the CAD layout with user defined features and annotations (i.e., virtual bridging between 2 metal lines).

Using the interoperable link between Synopsys CAD tools – Avalon™ and Sentaurus™ Process Explorer (SPX) software, users can create a new virtual deposition/depletion/etching layer in layout data that emulates the nature of defect (short/open). Once the probable location of the defect is identified in the CAD layout by observing the failing signals, EV layers can be used to imitate the behaviour of possible defects.

Based on the defect, EV layer can be of two types:

1. Cut EV Layer to simulate an etch/open.
2. Deposit EV Layer to simulate a bridge/short (see Figure 4).

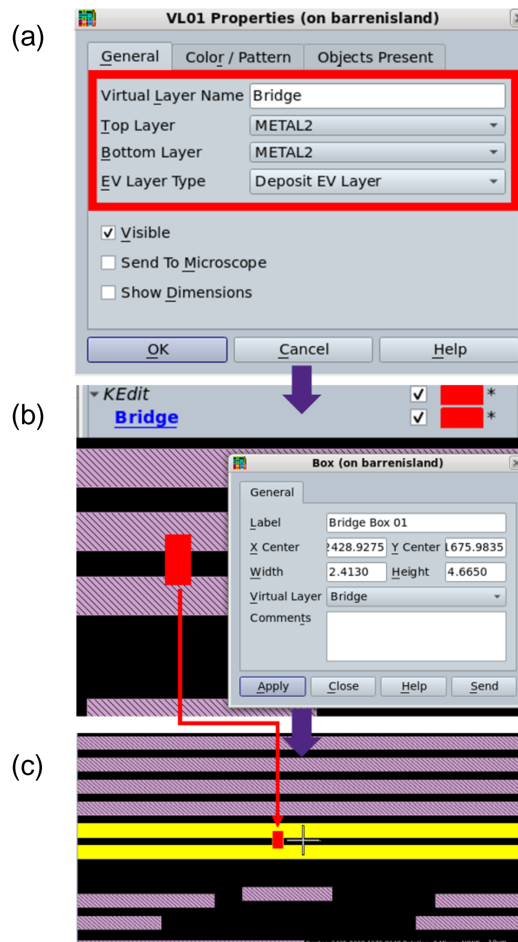

Figure 4. A deposition EV layer has been added in METAL2 (a), bridge defect between two nets is simulated by drawing a rectangular box in the layout (b), net-to-net short is simulated using the previously added defect (c).

Thereby, the simulated 3D cross-sectional views will also include the defect i.e., CAD annotations as part of the layout data. Using this technique, defects can be virtually injected in the device, and this can facilitate the FA engineer to pinpoint the location and nature of the device failure.

In Figure 5 a metal bridge defect was simulated in a sample device by creating a new deposition EV layer in its layout data using Avalon™.

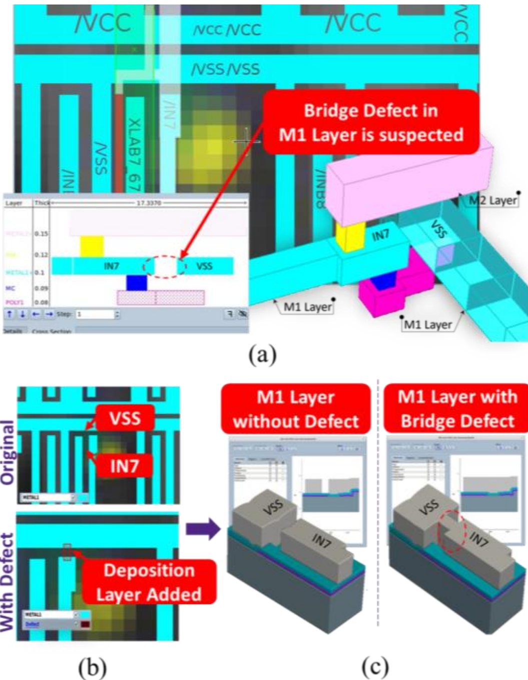

Figure 5. Sample workflow showing the process of injecting NVD in device process layers to simulate a failure.

The final image in this workflow provides insight into the detailed structure of the process layer responsible for the defect. Therefore, this novel concept provides an additional software support to the FA engineer and helps in improving the existing workflows. Since the entire analysis is solely based on CAD Navigation and defect simulation, no destructive analysis is performed on the sample. Hence, this method also helps in saving significant time and money by preventing some iterative PFA activities on a golden device.

4. Case Study

The case study presented here is related to an NXP Wi-Fi Front-End unit with SiGe BiCMOS technology exhibiting a lower TX power failure in one of its channels. The degraded electrical performances are explained by an atypical voltage drop (0V) and an under-current consumption of a specific VCC power supply of the failing channel.

4.1 Background

A similar case has been analysed previously with a standard FA workflow. In that case, the incriminated sub-circuit was identified owing to an abnormal mapping of light emission i.e., missing emission spots and thermal laser stimulation techniques, but the exact failure location was not pinpointed by the fault isolation techniques. After a detailed study, the most suspected nets in the circuitry of the failing channel were identified for FIB-pads (Focused Ion Beam) creation. But surprisingly, the micro-probing tests heeled the electrical functionality of the channel, and the unit was recovered – making this a classical example of how destructive procedures can result in irreversible damage and a ruined analysis [11].

4.2 Bench-Setup & Fault Isolation

To increase the success rate on the new case study the FIB-pads and the micro-probing operations were excluded to prevent any potential degradation or a recovery of the unit. Therefore, a different FA approach based on the previously described defect simulation workflow was applied here.

First, a more sophisticated electrical setup was established to reproduce the electrical tests using the production ATB (Analog Test Bus) pattern file in combination with a Python script and a waveform generator to stimulate and verify the failing channel in an FA lab environment. This setup was then coupled with an Optical Beam Induced Resistance CHange (OBIRCH) amplifier of a fault localization tool via a Current Probe Head (CPH) module. Then, backside fault localization methods like Lock-In Thermography (LIT), Photons Emission Microscopy (PEM), and OBIRCH were used, and the test results were compared to a reference unit. These methods helped in establishing a connection between the new test results to the ones obtained from the previous case. However, the exact defect location could still not be pinpointed.

Figure 6 is a comparative Current Probe Head OBIRCH analysis with 20x lens magnification, showing the most relevant OBIRCH mapping difference in TX_preDriver and bias_currentmirror blocks of the failing channel. The OBIRCH analysis with ATB setup confirmed missing sensitivities in TX_preDriver circuit (see red rectangle) and most interestingly it highlighted an additional minor OBIRCH spot near the two stages (see red arrow) - which was not detected in the previous case.

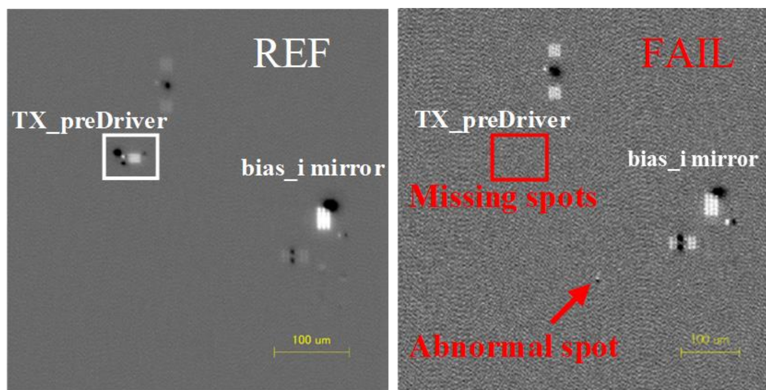

Figure 6. Comparative Current Probe Head OBIRCH analysis (Good vs Fail) with 20x magnification factor.

Figure 7 is a focused OBIRCH analysis with higher magnification and layout overlay on the abnormal spot location, revealing Seebeck Effect Imaging (SEI) sensitivities (consequences) on poly resistor terminals (Net4_11) of an independent circuit (not linked to TX_preDriver and Bias_CE_Currentmirror blocks).

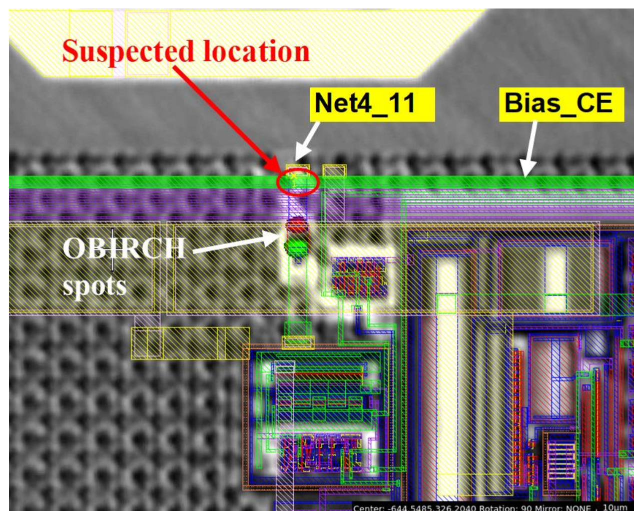

Figure 7. Superimposed OBIRCH image with 20X4X magnification showing sensitive locations but it is not pinpointing the suspected defect location.

4.3 Avalon™ Design Study

A detailed design study based on layout and schematic data with Avalon™ software helped in identifying the susceptible circuits in its MaskView and SchemView application using the Crossmap functionality. Due to confidentiality, the layout and schematic information cannot be provided here. Instead, only trace signals/highlights and simplified schematic drawing are given to illustrate the study.

Figure 8a shows the trace/highlight of Bias_CE signal in green colour connecting the TX_pre_Driver and the current mirror circuit. That green trace is mainly composed by Metal3 layer. Figure 8b shows its associated and simplified schematic drawing.

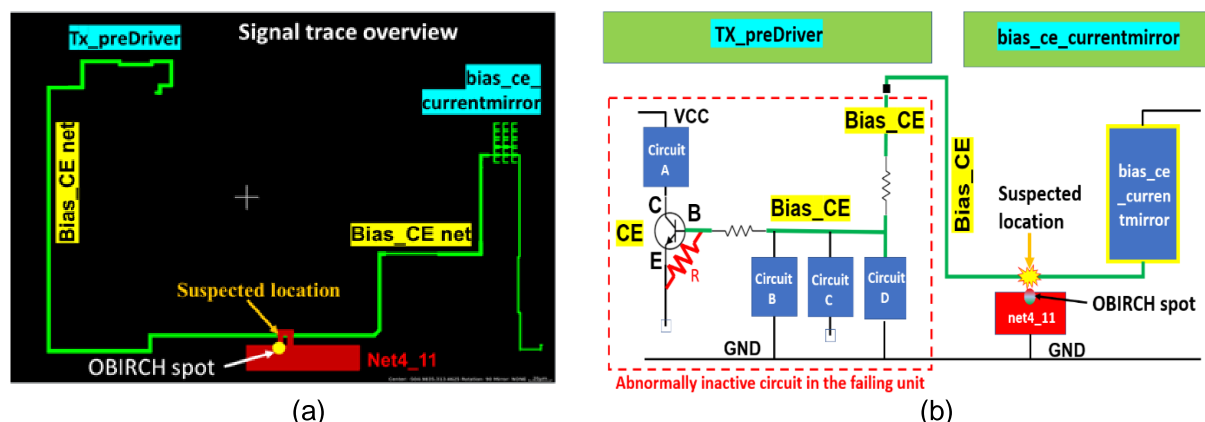

Figure 8. Design Layout view with traced signals in Avalon™ MaskView (a) and its associated simplified schematic drawing (b) showing the suspected defect location.

4.4 Cadence – Electrical simulation

An electrical simulation function was then operated with Cadence design simulation tool based on ranked failure hypotheses. The top ranked hypothesis was validated when an artificial electrical resistance of 2kΩ (fault) was injected between Base and Emitter electrodes of the CE component (Figure 8b), demonstrating thus that the electrical simulation results of the main parameters (VCC, ICC, V/I_{BIAS_CE},..) were fitting with the Lab bench measurements. This meant that a physical defect was necessarily present on the Bias_CE_net path as highlighted in Figure 8.

This validates the hypothesis elaborated in section 4.3, e.g. bridge/short defect between these two identified nets. But its location was yet to be determined.

To accurately predict and pinpoint the defect location, a rule-based layout search was performed to identify Critical Dimension (CD) locations in Avalon MaskView between the two highlighted nets (BIAS_CE, Net4_11). After this suspect location was found a defect injection (EVL) and bridged/shorted traces were done in IC Layout (Avalon) at the suspected location. The following sections provide the details of the workflow.

4.5 Defect Injection in Avalon™ MaskView

To confirm this hypothesis and to better visualize the abnormal link between the correct trace signal of Bias_CE and the abnormal OBIRCH signal on Net4_11, a virtual defect was injected in the layout (Avalon™ tool) by depositing an EV Layer (as explained previously) at Metal3 level and at the most suspected location to bridge the two nets (Net4_11 and Bias_CE) virtually as described in Figure 9. Note that the entire spacing between the adjacent Metal3 lines could be a potential place for a defect. The placement of the injected defect was arbitrary and manually set at a position that included a stack of vias on Net4_11 to consider the possible involvement of more materials in the suspected bridging damage.

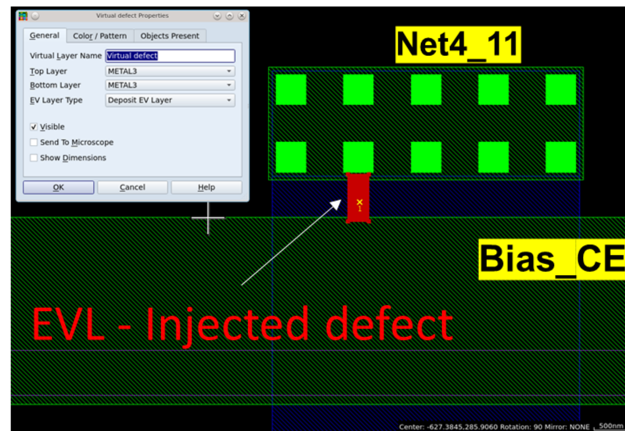

Figure 9. Defect injection in the layout (Avalon™ MaskView) by using Electronic Virtual Layer (EVL) at Metal3 to bridge the adjacent Bias_CE and Net4_11 nets.

Finally, the trace signal operation was re-executed to refresh the new layout connectivity. In Figure 10a the trace signal in the modified layout helped in visualizing the incorrect signal path between Bias_CE and Net4_11 nets and correlate the incorrect electrical activity of the rejected unit. Figure 10b is the reference trace used for comparison with the original design.

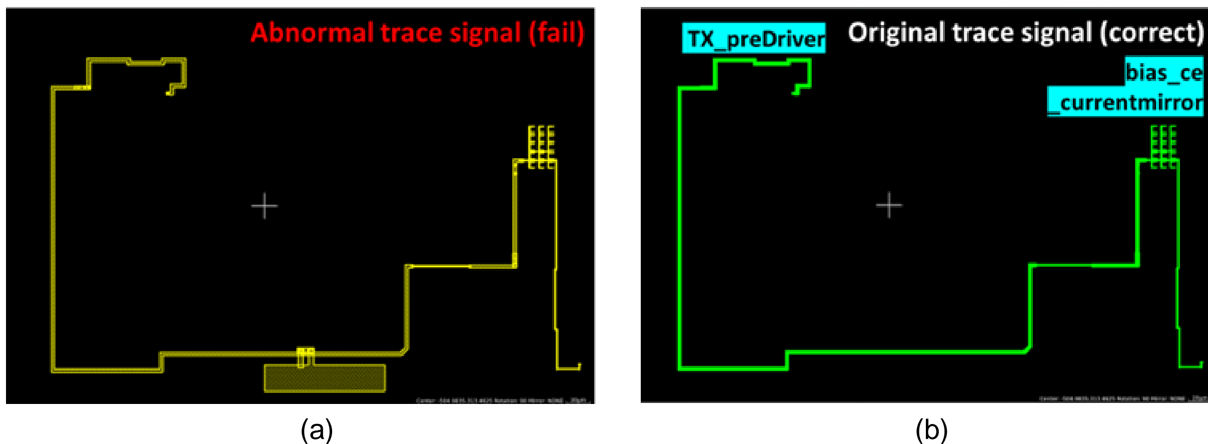

Figure 10. Avalon™ MaskView extracts - Visualization of the trace signal after the defect injection in the layout (a), comparison with a reference trace signal from the original design (b).

Although the exact defect location in the die was still unknown, but preliminary results from all the different methodologies - OBIRCH, Avalon™, and Cadence converged to the same hypothesis – the defect location indicated in Figure 9 was very likely to be the fault position (NVD).

To preview and accurately emulate this hypothetic defect, a 3D Process emulation was performed prior to the real PFA operations to increase the success rate on the rejected sample and to prevent repeating similar operations on a golden sample.

4.6 SPX Process Technology Creation & Defect Injection

Further investigations were pursued with the aforementioned ‘digital twin’ approach to predict a physical defect and to guide more efficiently the Physical Failure Analysis (PFA) flow. First, a 3D process simulation technology file (Flow) was developed by the FA engineer in the SPX software [7][9] based on the manufacturing process data of the silicon die, the process materials, and the design layers information. Once the process technology file was created and validated it could be used either independently in the SPX software (development mode) or integrated with the Avalon™ database to

enable the advanced 3D cross-section view.

Thereafter, a virtual defect (horizontal metal bridge) was injected in the IC-layout in the most suspected Metal3 layer and at the most suspected location as depicted in Figure 11. A clip centred on the injected defect location was created as a box to define the XY dimensions of the virtual TEM lamella in SPX layout window (see white rectangle in Figure 11) [7]. This is where the 3D process emulation was executed via the Flow and Route interface of SPX software – which can be coined as 'TEM rendering'.

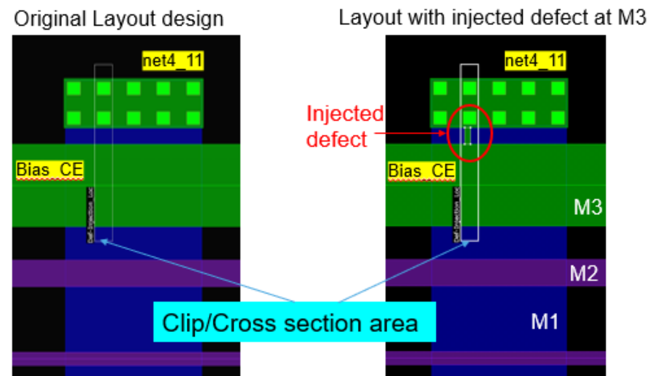

Figure 11. Close top view of the IC-layout at the most suspected location at Metal3 level showing the involved signals/nets. Left picture is the original top-view design layout. Right picture is the modified top-view design layout with the injected defect (highlighted by the red circle) in SPX software.

Like a FIB-TEM process, the 3D simulated lamella was virtually thinned by slicing in the appropriate direction until the position of the injected defect was reached. This 3D simulated TEM cross-section allowed a preview of the entire manufacturing process technology of the lamella and provided an insight into the probable physical defect between the adjacent nets (Bias_CE and Net4_11).

4.7 SPX: 3D Process Technology Simulation

Figure 12 shows the associated 3D virtual cross-sectional views of the original IC-layout without defect (left picture) and the modified IC-layout with the injected Metal3 bridge defect (right picture) at the suspected location.

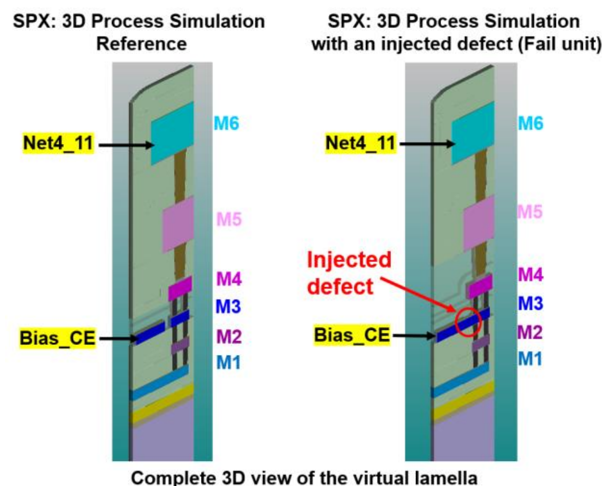

Figure 12. SPX 3D process simulation overview of the clip. Left and right pictures show the virtual 3D cross-section of the entire metal stack, respectively without (reference) and with the injected defect (fail).

To better visualize the simulated Metal3 defect, all top layers above ILD3 were disabled and ILD3 layer was set in high transparency mode to strengthen the failure hypothesis and predict the possible defect as shown in Figure 13.

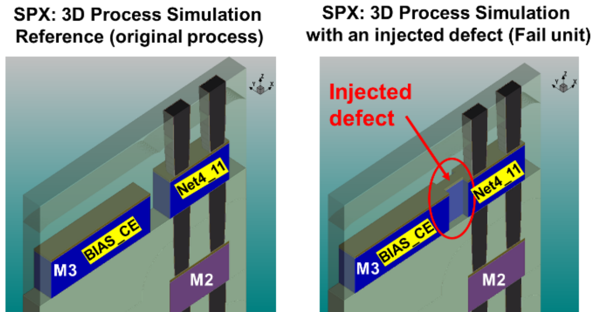

Figure 13. Focused 3D isometric views respectively from IC-Layout without (reference) and with defect injection at Metal3 layer (fail).

4.8 Physical Failure Analysis

Based on these 3D views, a PFA with a delayering approach was done on the ROI, as suggested by the above simulation. A visual anomaly was observed as described in Figure 14, confirming the failure hypothesis depicted in Figures 9, 11, and 13.

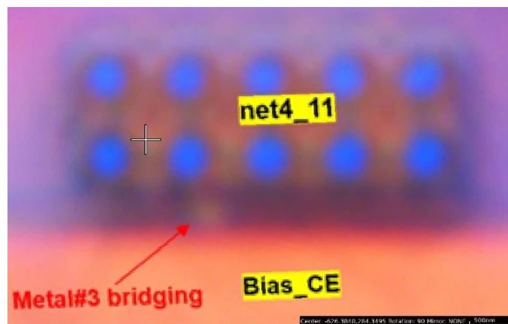

Figure 14. High magnification optical image with water lens showing a visual anomaly at M3 layer like the simulation.

Only after these consolidated results, a real physical FIB-TEM lamella was operated on the CQC unit at the identified failure location following the clip of Figure 11. The TEM analysis revealed a physical Metal3 bridging failure between the adjacent metal lines as predicted by the SPX 3D process simulations. Images in Figure 15 are STEM Mass Contrast Images with low and high magnifications and confirm the Metal3 bridging defect between Bias_CE and Net4_11 at the suspected and predicted location.

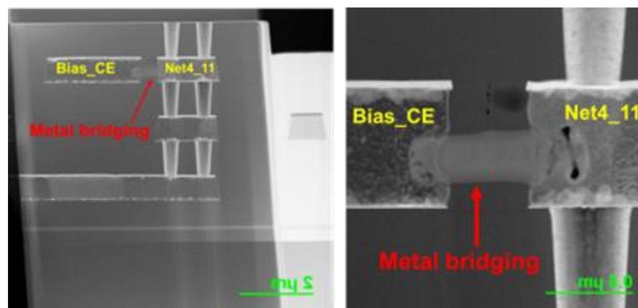

Figure 15. TEM pictures showing the physical defect bridging the adjacent Metal3 lines.

An Electrically Induced Physical Damage (EIPD) signature was seen similarly to the 3D simulation results, thus confirming the failure hypothesis and resolving the analysis.

5. Discussion

In this paper the ‘digital twin’ approach has been applied on a real CQC case with a suspected metal bridging/short between two adjacent metal lines, which was not detected and not pinpointed by the fault isolation techniques/tools (NVD). The method has demonstrated its benefits to maximize the confidence in the fault location prediction and to pre-visualize the physical defect via the 3D process simulation prior any PFA, and to increase the FA success rate.

The current case study can represent the most common category of bridges/hard short circuits failures where the approach can be successful. To further expand the deployment and the success of this approach to more complex physical failures, a list of identified improvements needs to be addressed, particularly by EDA vendors, to make the approach more autonomous and streamlined.

Currently, the most notable improvement could be the automatic creation of defect models in the schematic correlated to the injected defects in the IC-layout (LVS). This would facilitate a defect cross-mapping capability between layout and schematic, and reduce the overall design study effort and time.

Another improvement could be providing an extensive library of virtual defects to the FA engineer. For e.g., to have more control of structure and positioning of defects in the process layers, and to also control the thickness and shapes of defects in the layout interfaces (MaskView, Layout-SPX).

Some of these improvements are positively ongoing to unlock the full potential of the proposed workflow and to increase its efficiency by using a single design platform.

This paper discusses an important topic in advanced IC failure analysis - interdisciplinary approach to solve complex issues. Conventionally, a design software is used by an FA engineer in view-only mode. In contrast, we propose a possibility to extend this usage to editing mode by providing the capability to annotate the IC-layout with fault injection; without needing any help from the designers. Ultimately, this technique can enable the FA engineer to understand the consequences of these changes in the device schematic and more importantly they can pre-visualize these consequences in the physical process layers prior to actual PFA.

6. Conclusion

To address the challenges posed by NVD, an innovative approach based on defect injection in layout IC combined with 3D process simulation is introduced to assist FA engineers. The method has been described and demonstrated on a CQC case study. In the mentioned case-study, fault localization was unsuccessful on the failing sample and therefore it was hypothesized with NVD.

It is only in the end, that we could find some physicals remnant of the defect using TEM analysis. However, it must be noted that the defect emulation technique mentioned in the paper is not limited to NVD devices but can supplement the existing fault localization workflows in general i.e., from simulating metal bridge defects to complex NVD such as, stress induced leakage current (SILC), contamination etc. – which cannot be affordably detected using SEM and even TEM).

The digital twin approach has been assessed autonomously by FA engineers and has facilitated in resolving the failure.

7. Acknowledgements

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Finally, we would like to thank Dr. Detlef Conrad, Sr. Corporate Application Engineer from Synopsys Switzerland, for the fruitful discussions and sharing his expertise and for always considering the feedback, suggestions, and proposals to be integrated in Sentaurus™ Process Explorer (SPX) software for the benefit of the large FA community.

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