SAIF Based DPS and IRAP for Power and Power Grid Optimization for Complex IPs

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Intel

Agenda

- Introduction
- Proposed Method
- Setup and Strategy
- Implementation Results
- Conclusion and Future Work
- Acknowledgement

Introduction

Introduction

IP design teams aims to deliver better quality deliverables, but the factor of IR reliability and power comes as a bottle neck and pull them back from timely deliverable

Design may need to be tweaked to reduce power and modify power grid based on the results from the signoff tools, which is time consuming

Introduction

Std Cell count	5M
Technology	Intel3
Area	507587.82 um2
Operating Frequency	4GHz
Macro Cell count	262

Table 1: Design Specifications for Block 1

Std Cell count	35K
Technology	Intel 18A
Area	28978um2
Operating Frequency	625MHz
Macro Cell count	1

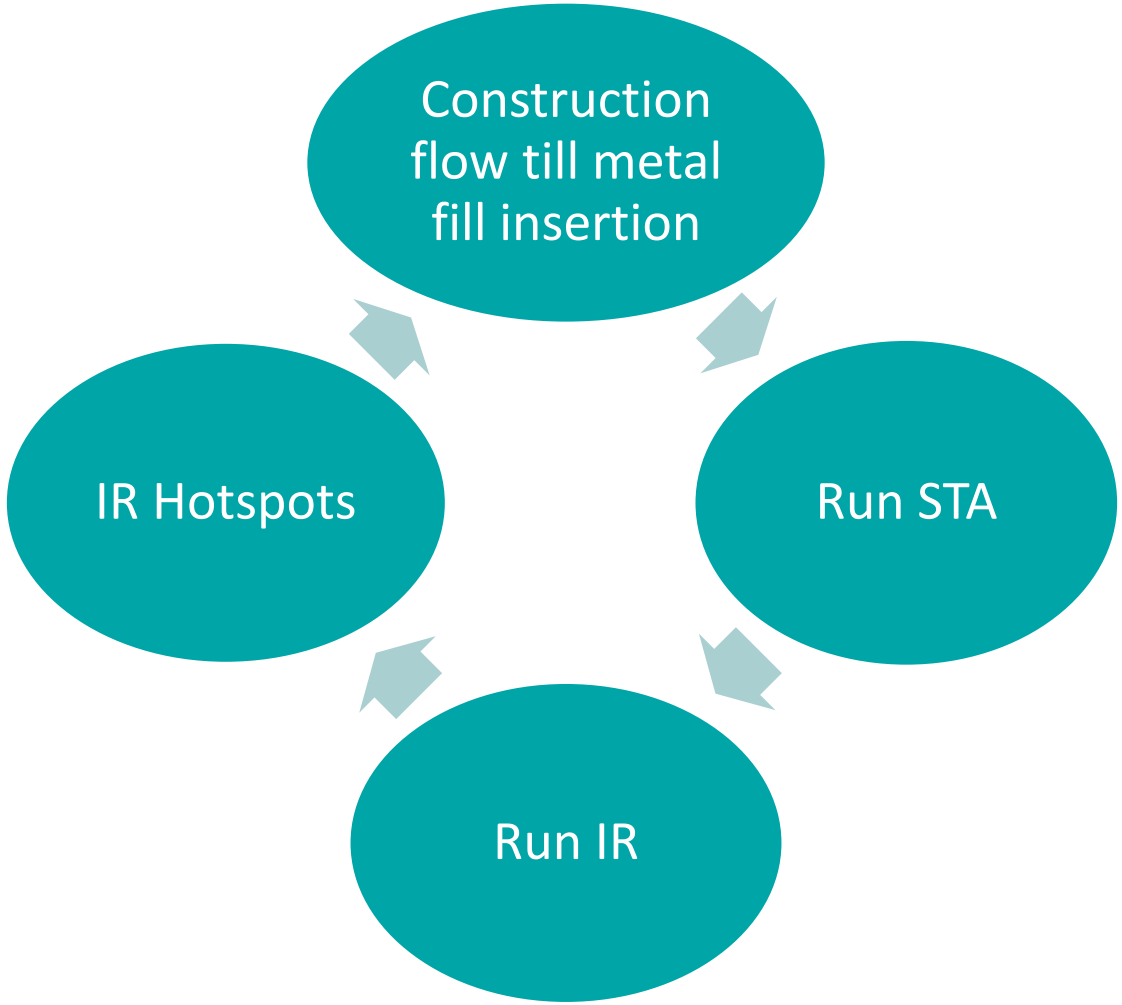
Table 2: Design Specifications for Block 2

There are certain IPs which are instantiated multiple times in the SOC.

Delivering them with robust power grid with better reliability results and reduced power along with improvised TAT, these IPs will improve the total power consumption and reliability results of SOC. Also, IPs can be delivered quicker.

Proposed Method

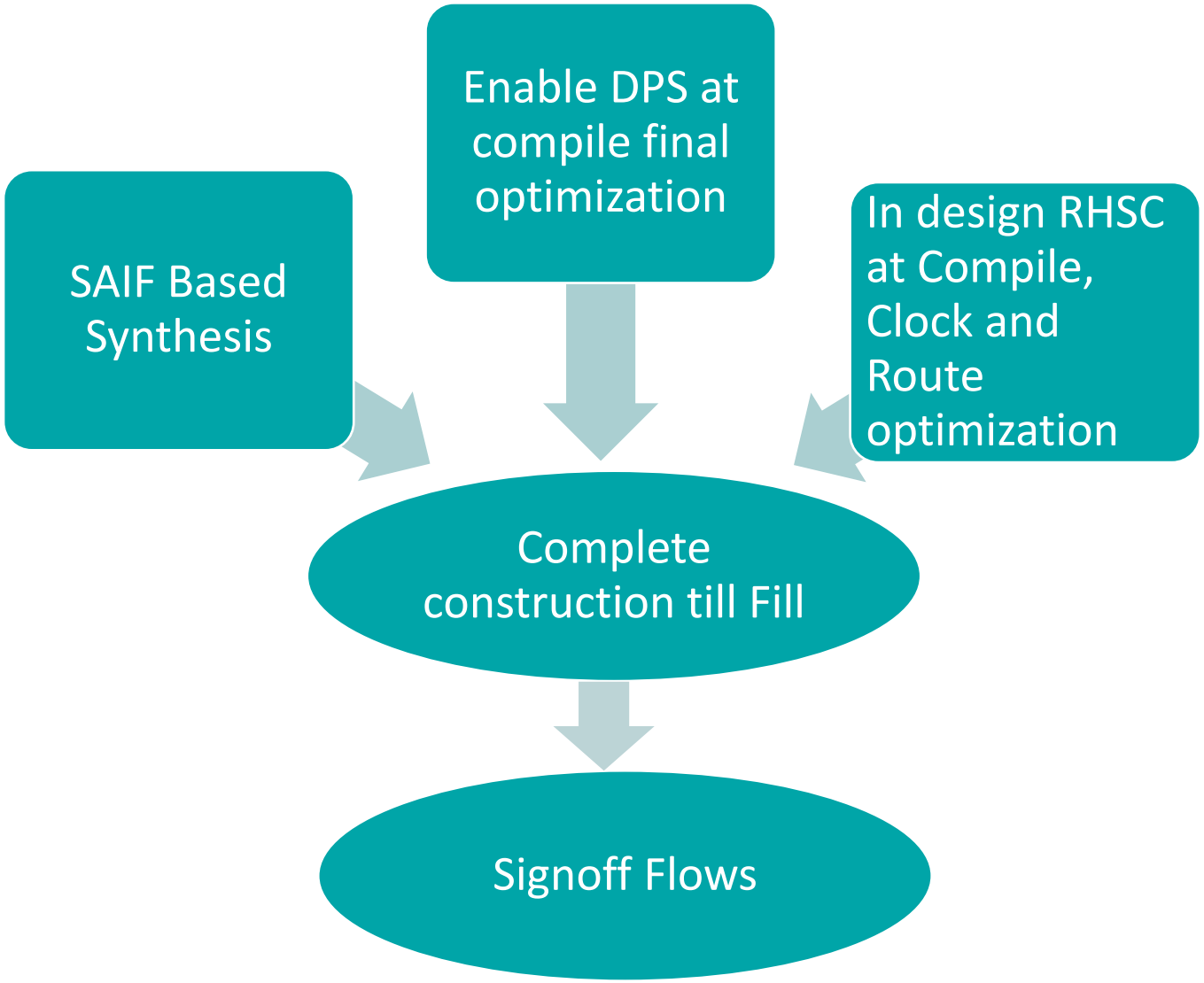
Traditional Method



Challenges:

- Time Consuming due to multiple iterations
- Uncertainty over impact on timing/other reliability issues.

Proposed Method



Why this Method.?

- Breaks the Traditional cycle chain
- Improved TAT
- Reduced Violation count
- By the end of fill you can know the impact of IR in your design

DPS and IRAP – An Introduction

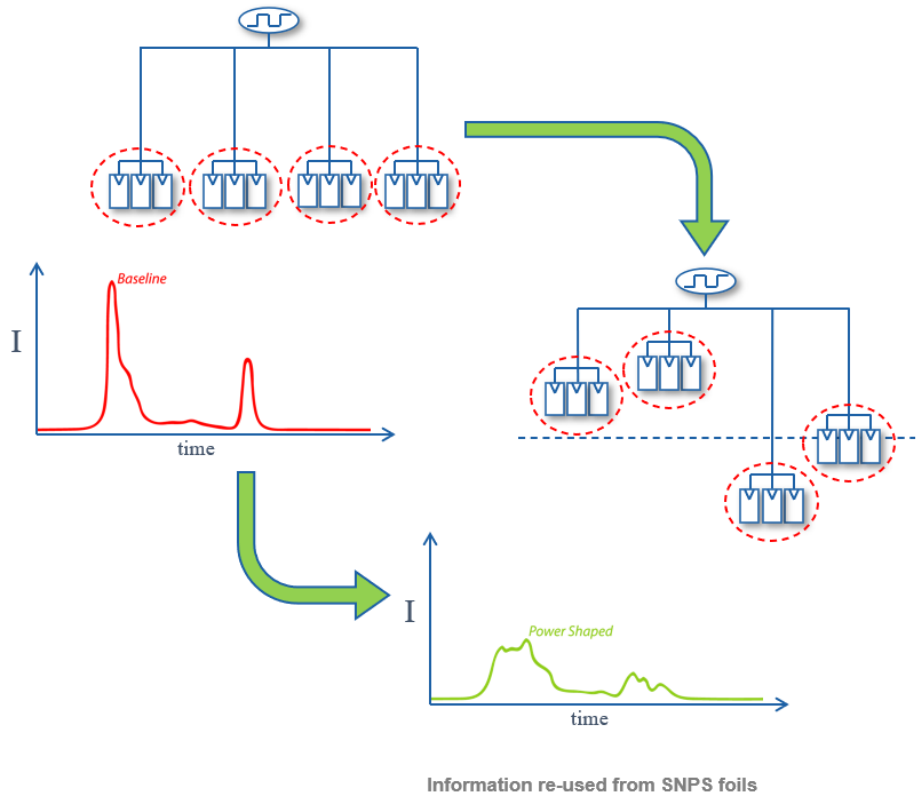


Figure-1: DPS – Dynamic Power Shaping

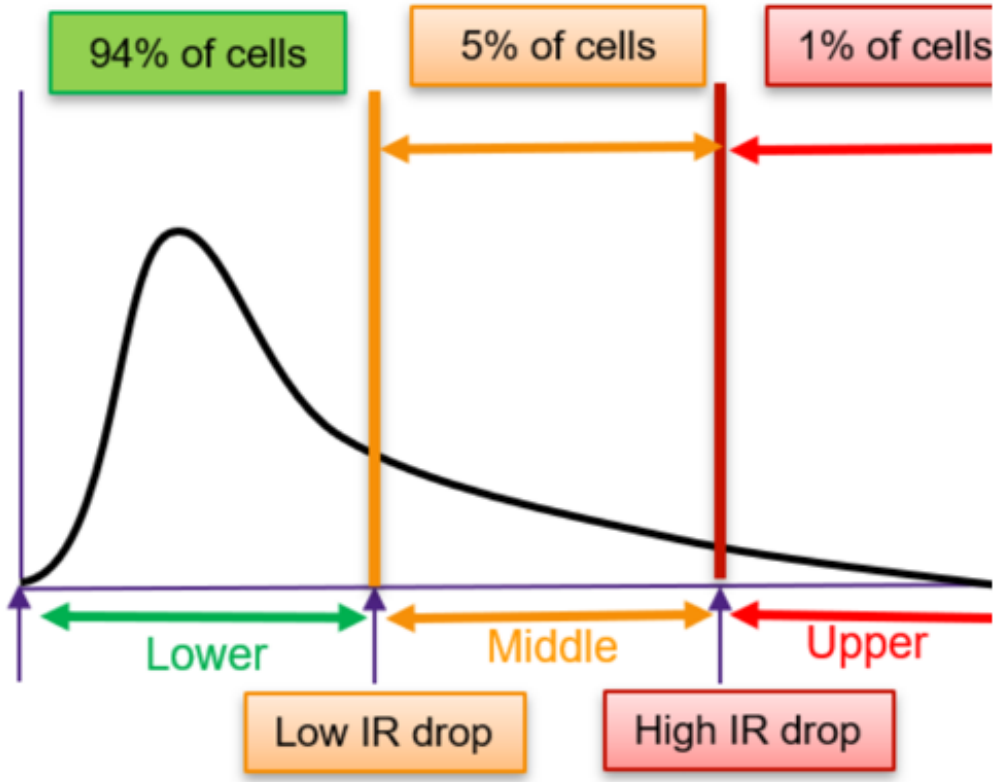


Figure-2: IR Aware Placement

Setup and Strategy

Steps to Implement

Setting up the Proposed Method

Saif Synthesis

- Saif_map –start; read_saif
- Propagate Switching Activity

DPS

- set_app_options -name compile.flow.enable_dps -value true
- set_app_options -name ccd.dps.flow_reporting -value {*}
- set_app_options -name ccd.dps.focus_power_scenarios –value scenario_name

IRAP

- set_app_options -name rail.allow_redhawk_license_checkout -value true
- set_app_options -name rail.pad_files –value <pad/bump locations>
- set_app_options -name place.coarse.ir_drop_aware –value true
- set_app_options -name opt.common.ir_drop_threshold –value <IR Threshold>
- set_app_options -name rail.tech_file <IR Tech file>
- analyze_rail -nets –voltage_drop static/dynamic

Implementation Results

IR Aware Placement and DPS Results

```
REDHAWK_RESULT was loaded successfully.
open_rail_result Peak Memory: 229408.730 MB  CPU Time: 615.141 seconds Elapsed Time: 397.867 seconds (70299.641 70697.508)
Placer: reannotation successful
Placer: reading RH power
Placer: Power Density: found supply net vcc[redacted]
Placer: Power Density: found supply net vcc[redacted]
Placer: Power Density: found supply net vcc[redacted]
Placer: Power Density: found supply net vss
Placer: Power Density: Using layer m2 (default) for Effective R extraction
Information: Analyze net vcc[redacted]
Information: Analyze net vcc[redacted]
Information: Analyze net vcc[redacted]
Information: Analyze net vcc[redacted]
Information: Analyze net vss
Information: include net vcc[redacted] to analyze
Information: include net vcc[redacted] to analyze
Information: include net vcc[redacted] to analyze
Information: include net vcc[redacted] to analyze
Information: include net vss to analyze
Information: #net: 5 #node: 73165160
Information: Using MMD Ordering...
Information: Allocated    18205.8 Mbytes for effective resistance calculation.
Information: Calculating effective resistance values using 4 thread(s).
Progress: 0%
Progress: 10%
Progress: 20%
Progress: 100%
Placer: Power Density: found effective R for supply net vcc[redacted]
Placer: Power Density: found effective R for supply net vcc[redacted]
Placer: Power Density: found effective R for supply net vcc[redacted]
Placer: Power Density: found effective R for supply net vss
Info: using [redacted]
PLACER: IRDP:
#instances: 736531
#instances annotated with RH power: 519375 (70%)
```

```
Placer: IR aware: voltage drop targets
Voltage area ----lower bin---- low vdrop target ------middle bin----- high vdrop target ------upper bin------ eff.voltage supply nets
             #cells %cells vdrop %vdrop        #cells %cells      vdrop %vdrop        #cells %cells       min   max   pwr   gnd
------------ ------ ------ ----- ------ ---------- ------ ---------- ------ ---------- ------ ------ ----- ----- ----- -----
  DEFAULT_VA 386527  94.0% 0.103   9.4%      20559   5.0% (D) 0.154   14.0%       4111   1.0% (D) 0.550 0.550 vcc[redacted] vss
[redacted]    11602  94.0% 0.061   5.6%        617   5.0% (D) 0.099    9.0%        123   1.0% (D) 0.550 0.550 vcc[redacted] vss
vcc[redacted] 89918  94.0% 0.094   8.6%       4782   5.0% (D) 0.132   12.0%        956   1.0% (D) 0.550 0.550 vcc[redacted] vss
Voltage area names:
```

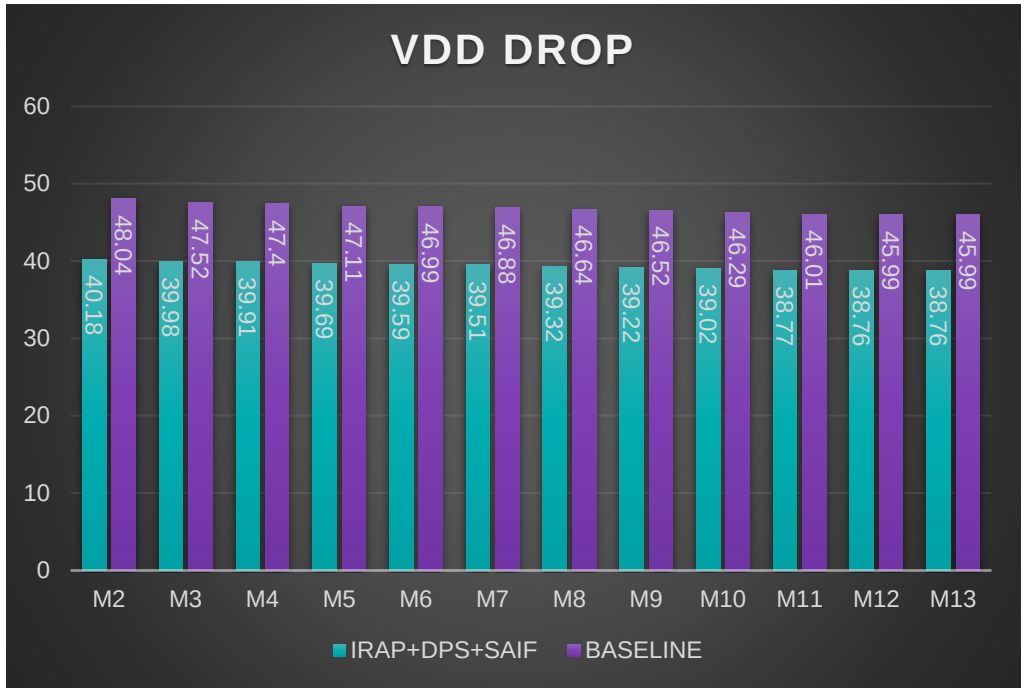
Figure-1: Log File entries from Clock Route Opt db

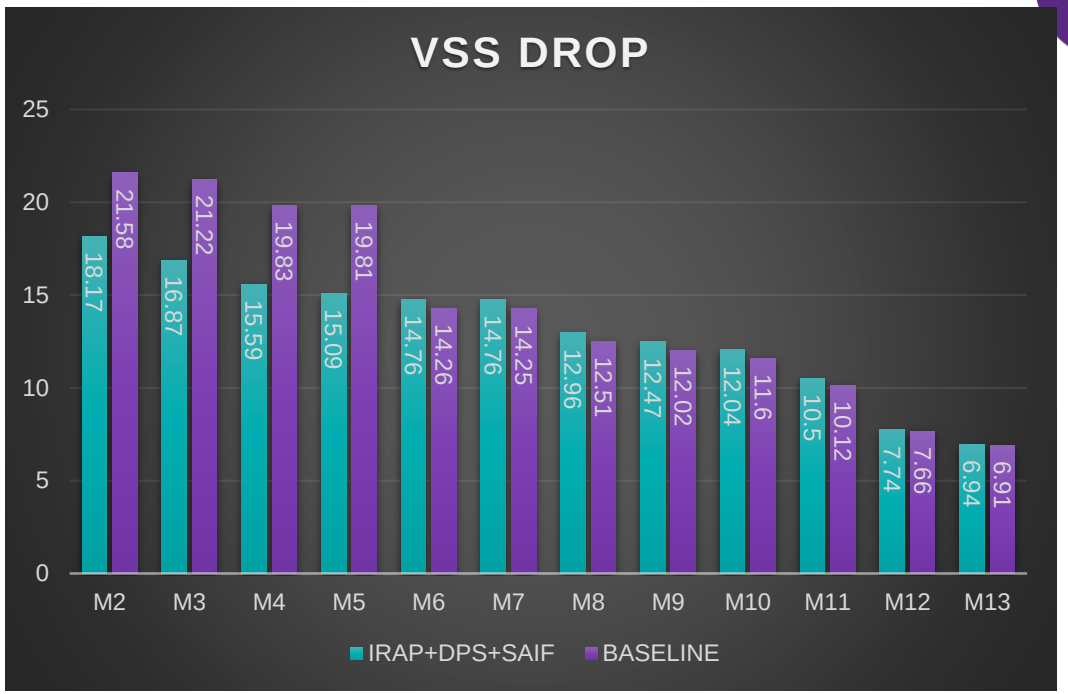
DPS Result

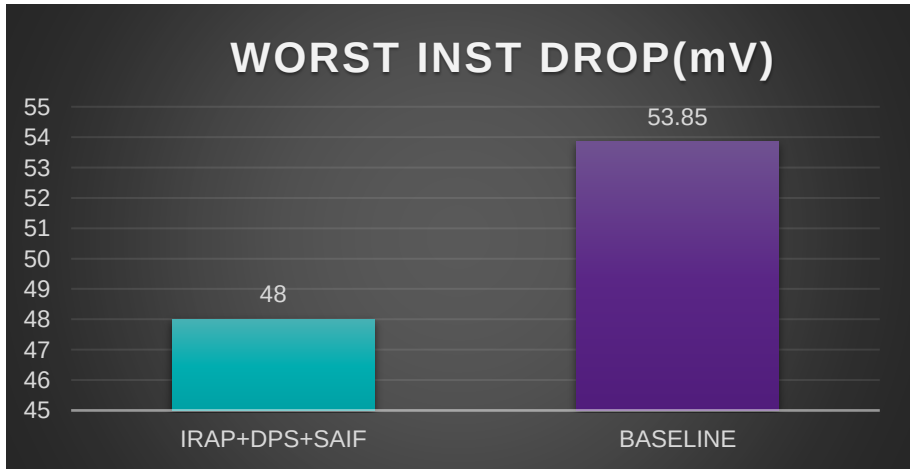
Baseline	Optimized	Reduction
12.399mA	11.102mA	10.5%
0.621mA	0.544mA	12.4%
1.242mA	0.844mA	32.0%

Figure-2: DPS data from compile final reports

Voltage Drop Comparison







RHSC IR DROP HEAT MAP COMPARISON

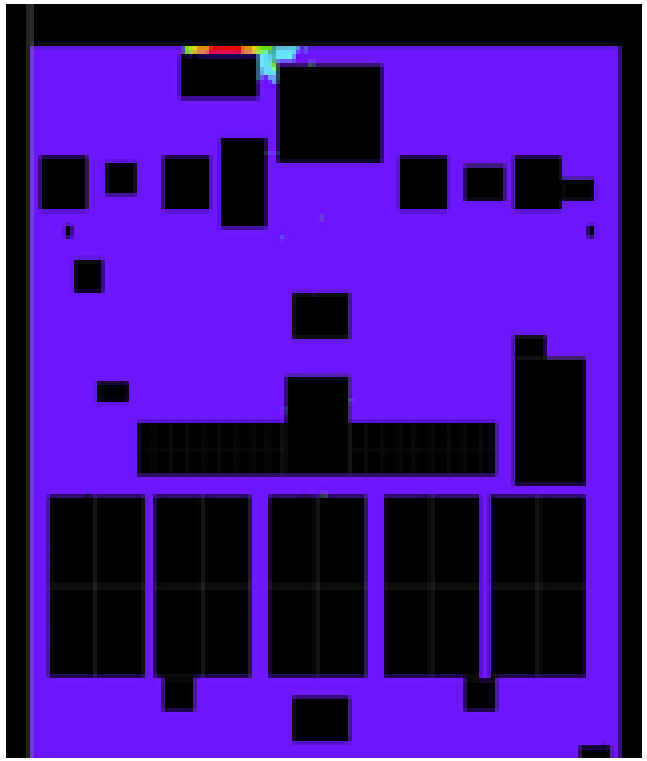


Figure-1: From RHSC Signoff Results from Traditional Method

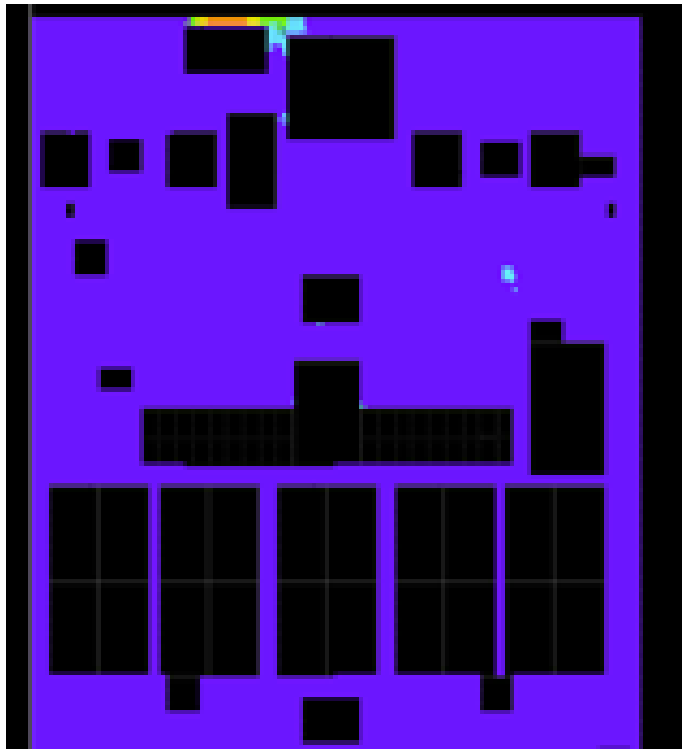


Figure-2: From RHSC Signoff Results from Proposed Method

Power Comparison Summary

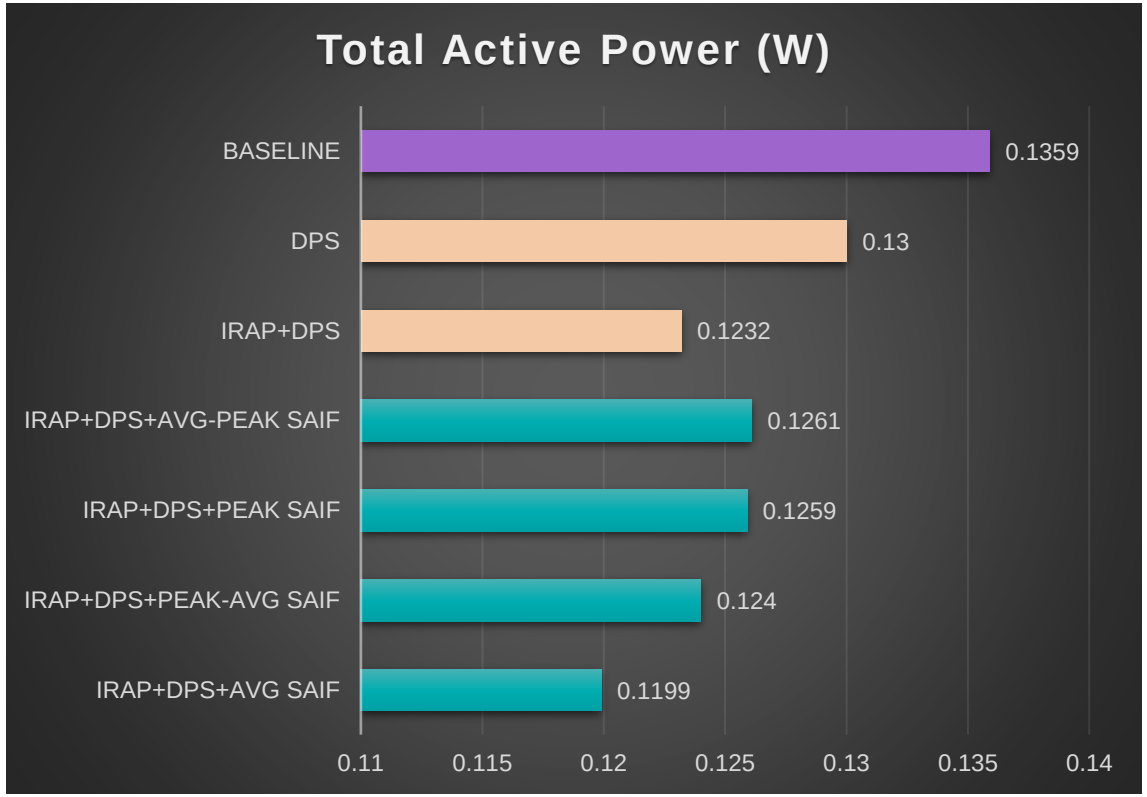


Figure-1: Computed total power in active mode across multiple experiments

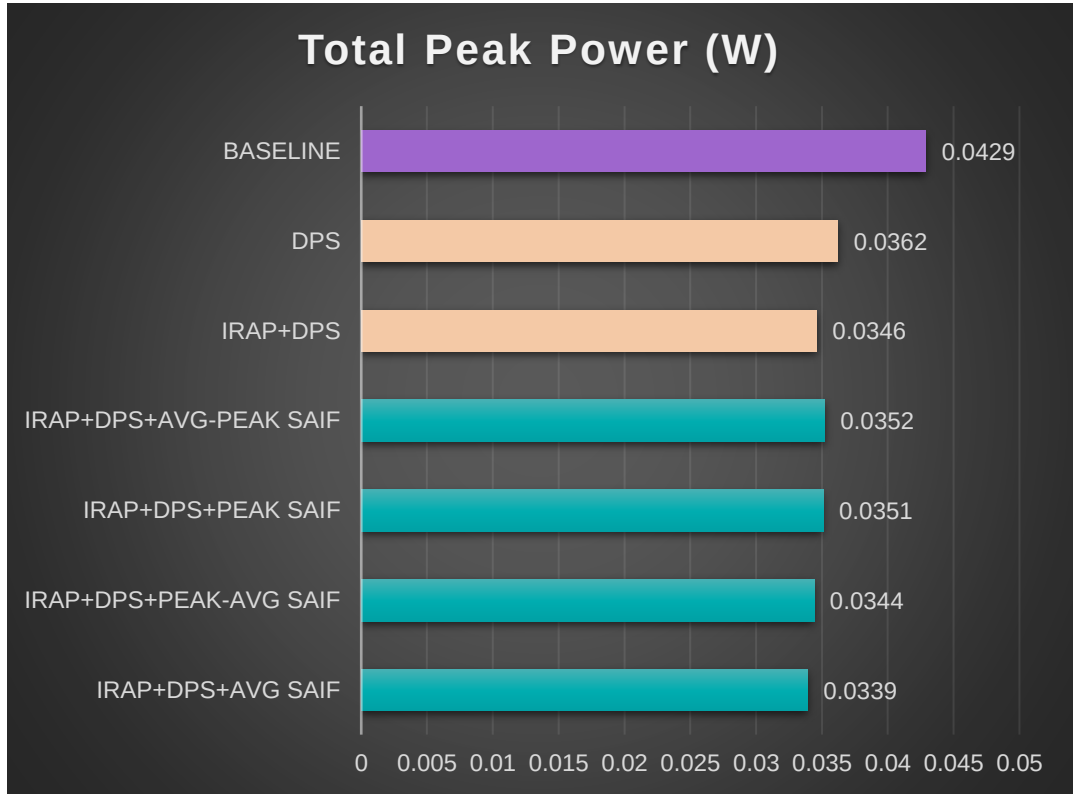


Figure-2: Computed total power in peak mode across multiple experiments

DPS Results – Block 2

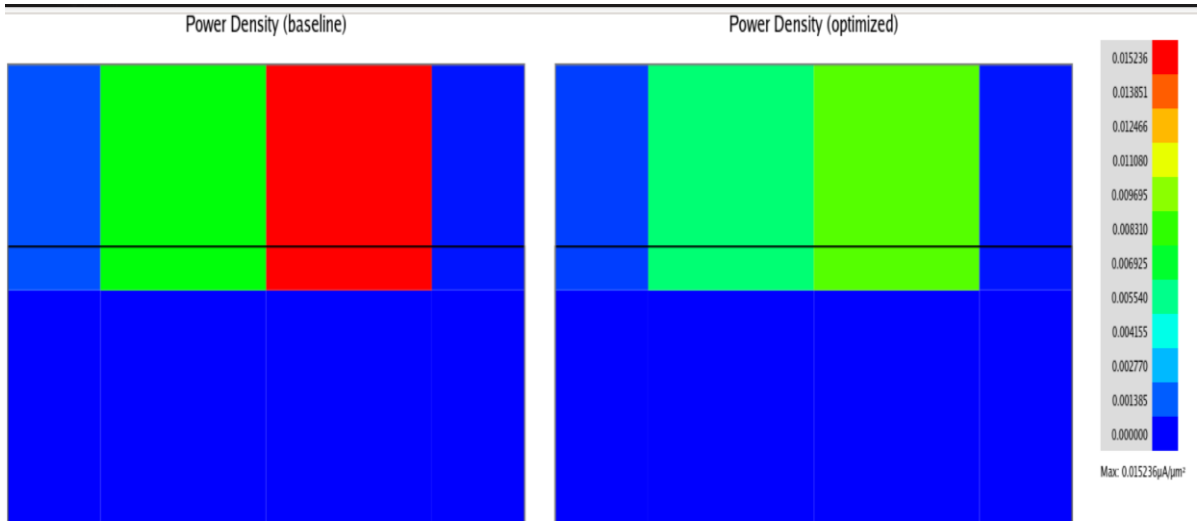


Figure-1: Ungated supply optimization from DPS

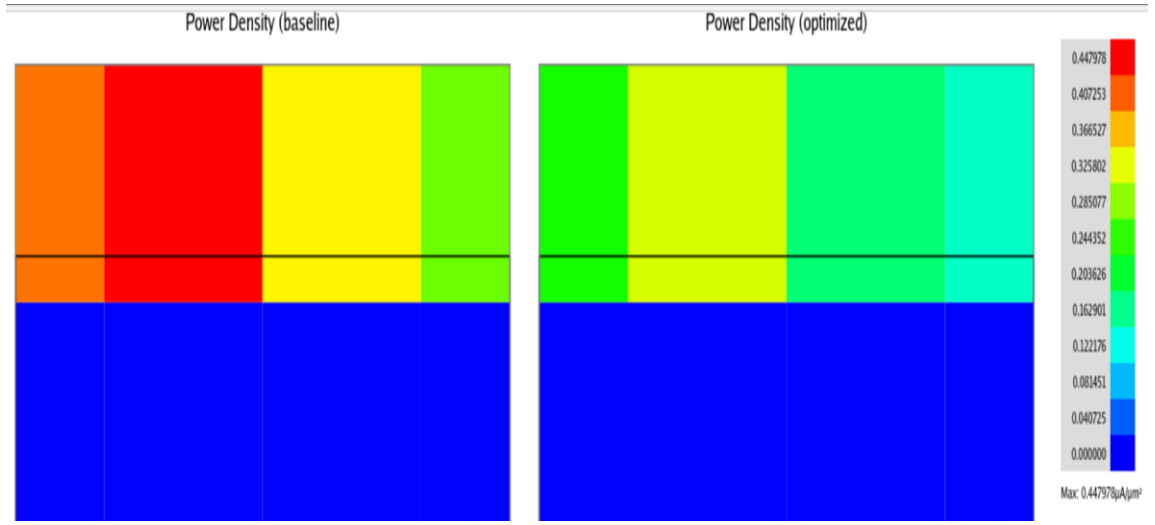
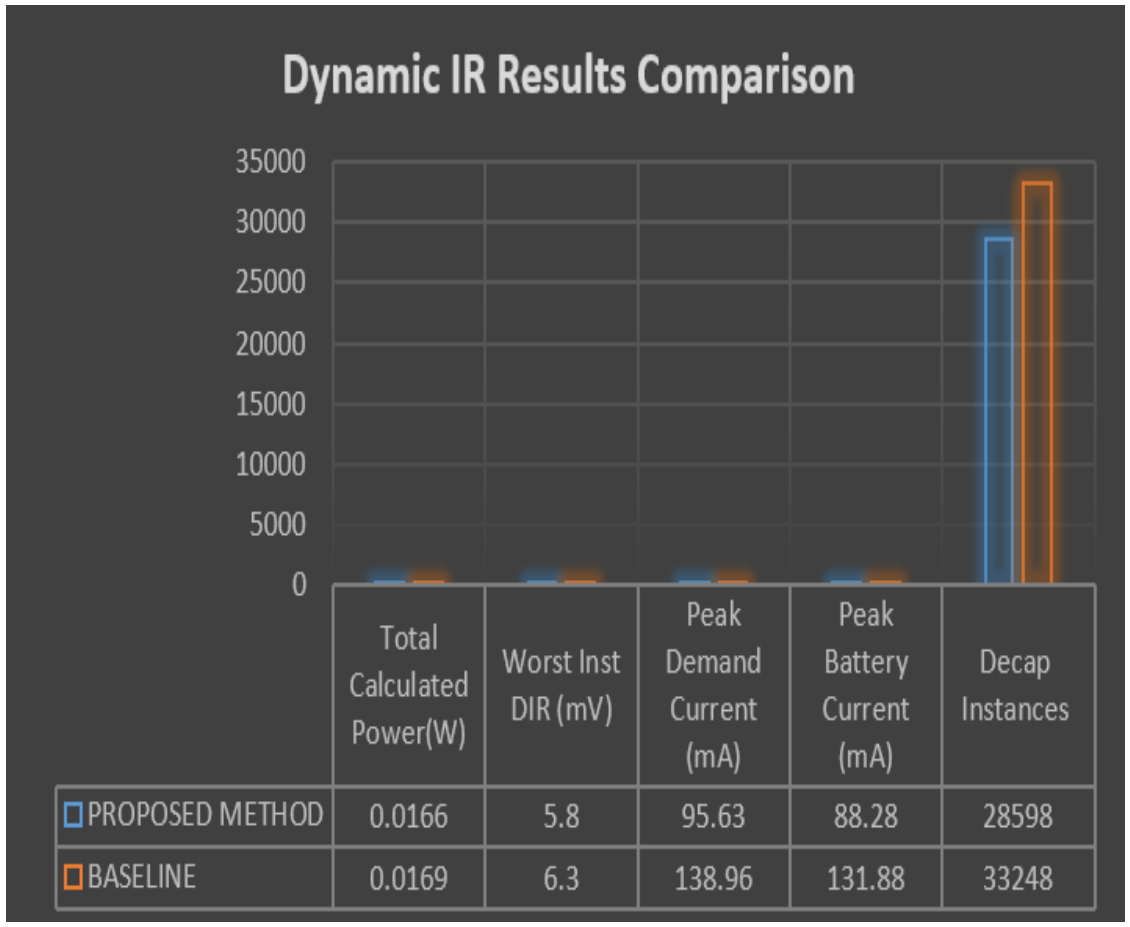


Figure-2: Gated Supply Optimization from DPS

Dynamic IR Results – Block 2



	Total Calculated Power(W)	Worst Inst DIR (mV)	Peak Demand Current (mA)	Peak Battery Current (mA)	Decap Instances
PROPOSED METHOD	0.0166	5.8	95.63	88.28	28598
BASELINE	0.0169	6.3	138.96	131.88	33248

Figure: Results comparison between traditional method vs the proposed method

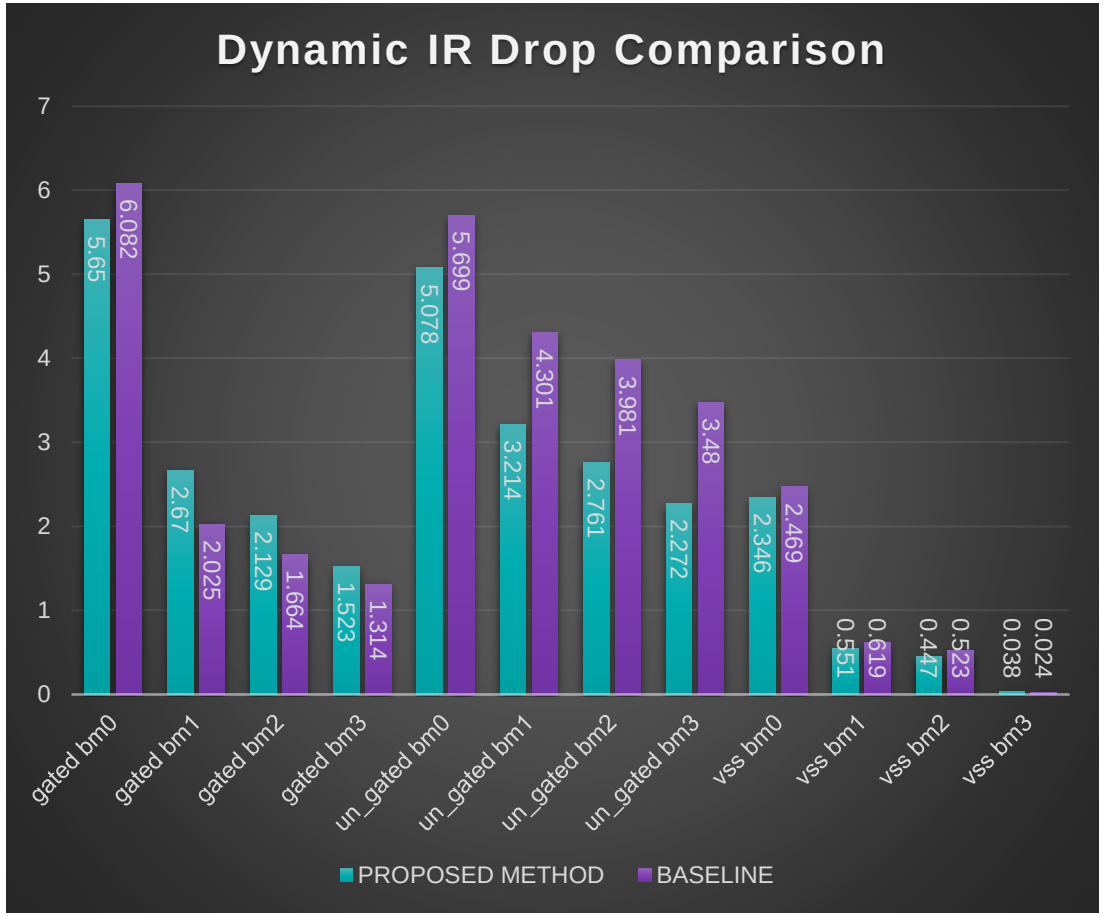


Figure: Dynamic IR drop comparison between traditional vs proposed method

Final Signoff Results Comparison – Block 2

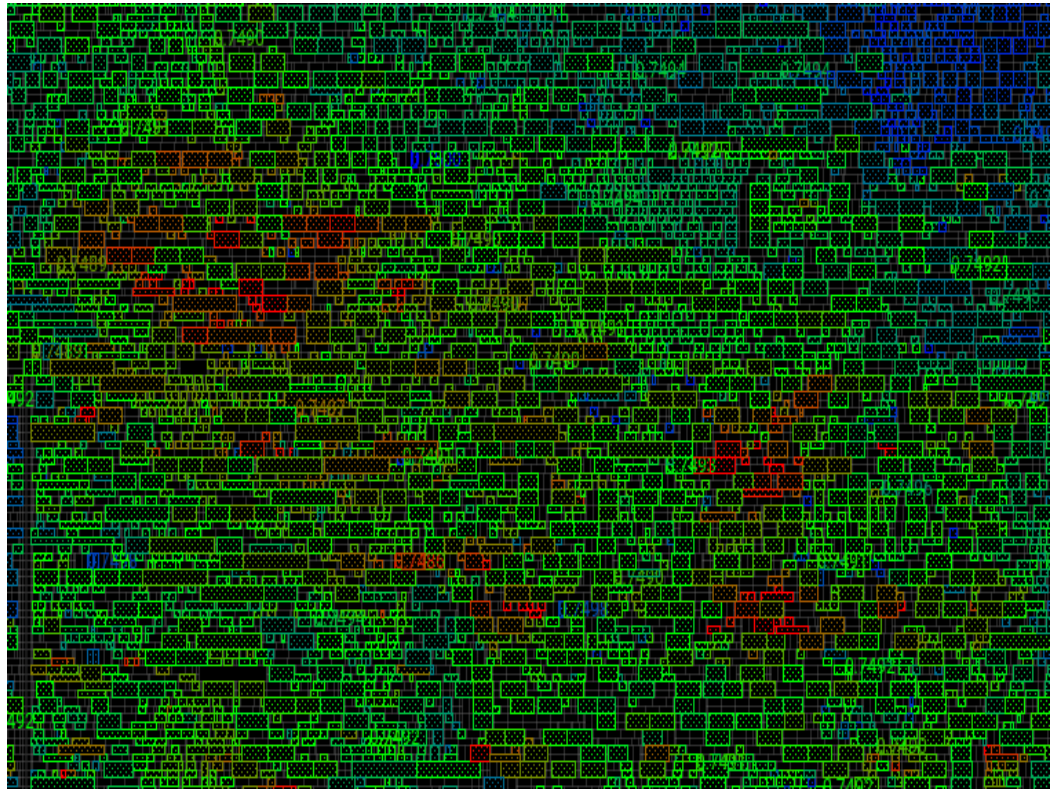


Figure -1: From RHSC tw_min violations heatmap from traditional method signoff runs

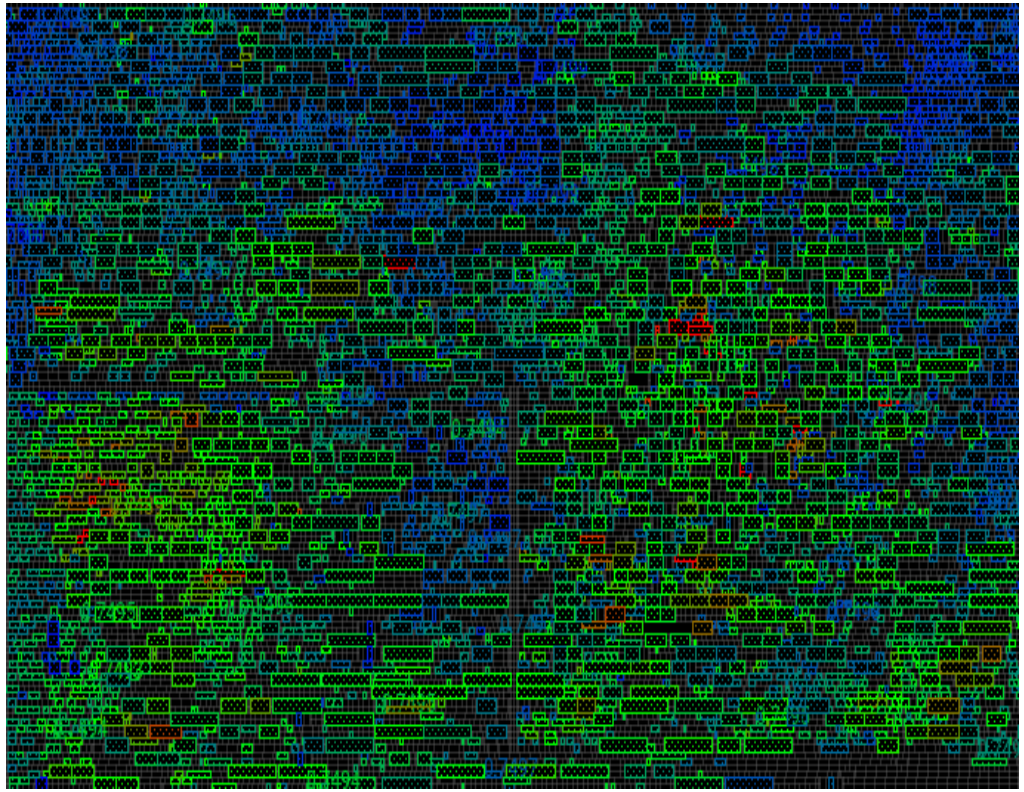
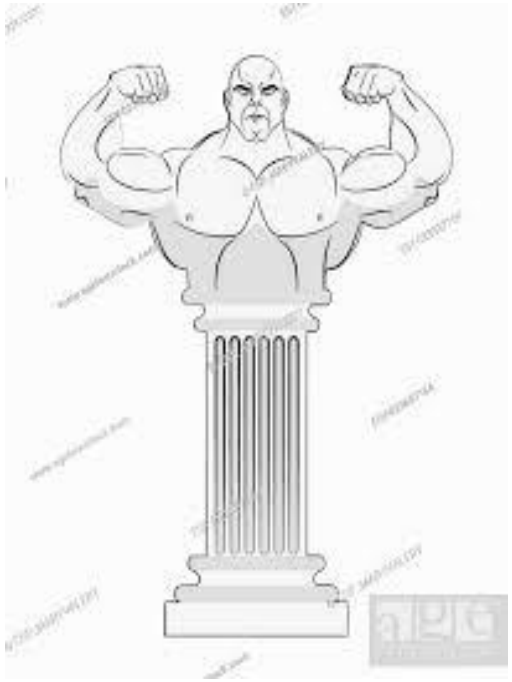


Figure -2: From RHSC tw_min violations heatmap from proposed method signoff runs

Conclusion and Future Work

Why This Method



Reduced Turn Around Time

Easy to implement app options and RHSC license

Provides you a Robust Power Grid

Conclusion & Future Work

To Conclude:

- We can observe that the SAIF based DPS and IRAP is providing us a better improvement in voltage drop and as a by product we can also see there is an improvement in power.
- With this method we can reduce 20%-30% TAT.

Future Work:

- Trying out InDesign PrimePower along with this method to check for further improvement in power.
- Trying PG Grid augmentation feature along with the proposed method.

Acknowledgments

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