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Advanced Implementation Techniques For Achieving Best PPA in High Performance Designs

Sudhakar Vadiraj Alur, Kishorkumar Chavada,
Ramnarayan Thukkaram , Ujjwal Prakash
Qualcomm India Private Limited

Agenda

- Introduction
- Implementation challenges
- Synthesis Flow Enhancements
- Synthesis Strategy
- PnR Challenges and Solutions
- Results
- Conclusion

Introduction

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- Goal:-
  - Address congestion with reduced metal layer stack.
  - Converge on PPA targets.
  - Meet strict BBOX area requirements.

- Design Details:-
  - Subsystem ranging in Millions of instances.
  - Frequency in the GHz range.
  - Multiple power domains.
  - Multi scenario closure.

Implementation Challenges

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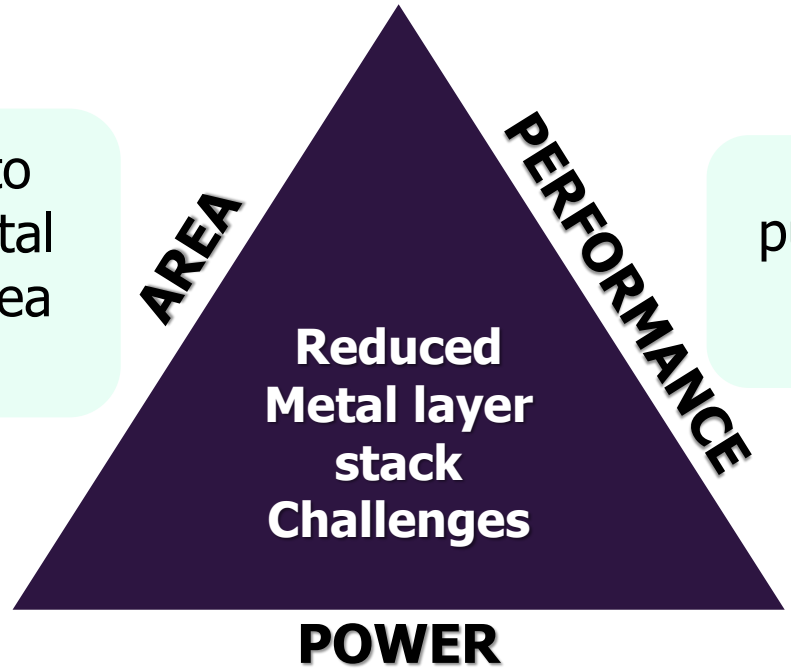
Stringent target to meet Reduced metal layer stack w/o area overhead



Aggressive FMAX push to provide best in class HPC with given constraints

Dynamic/Leakage Power targets

Synthesis Flow Enhancements

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Traditional Recipe

- Able to achieve PPA targets.

Increased BBOX

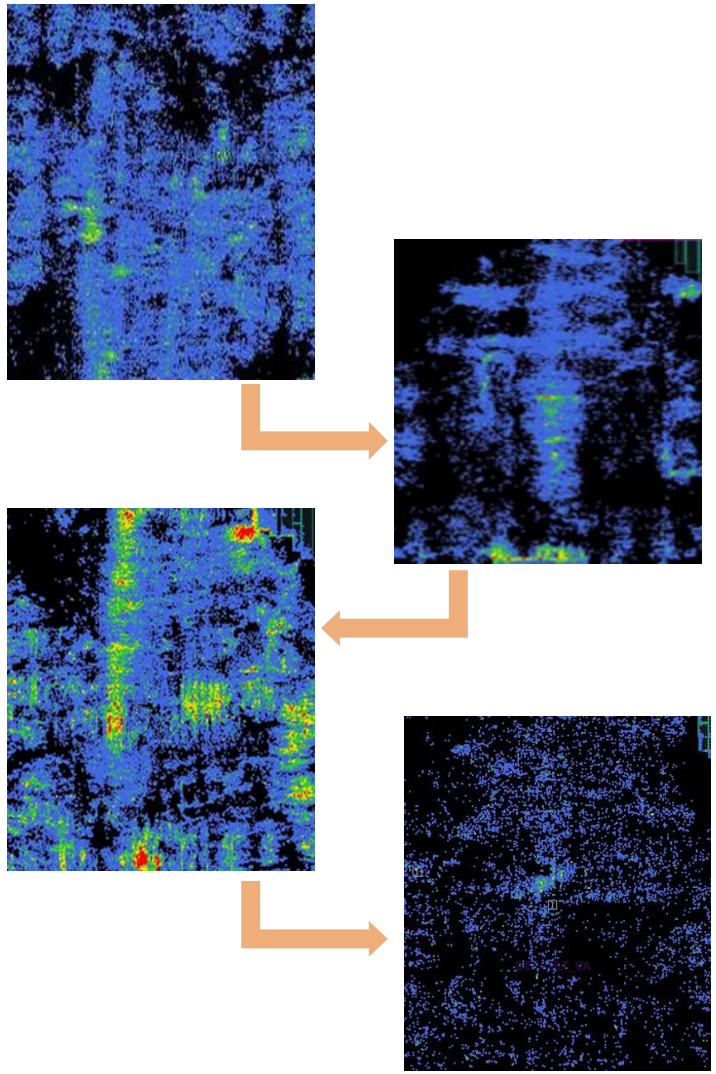
- Stdcell area increased due to reduced metal stack.
- Significant increase on congestion and impacts Power/ Performance.

ISO BBOX

- High congestion , Database was not routable at PRO (high short count).

Final Recipe

- Converged the design in given BBOX
- Congestion improved at PRO with few hundred shorts.



Synthesis Flow Enhancements (Contd.)

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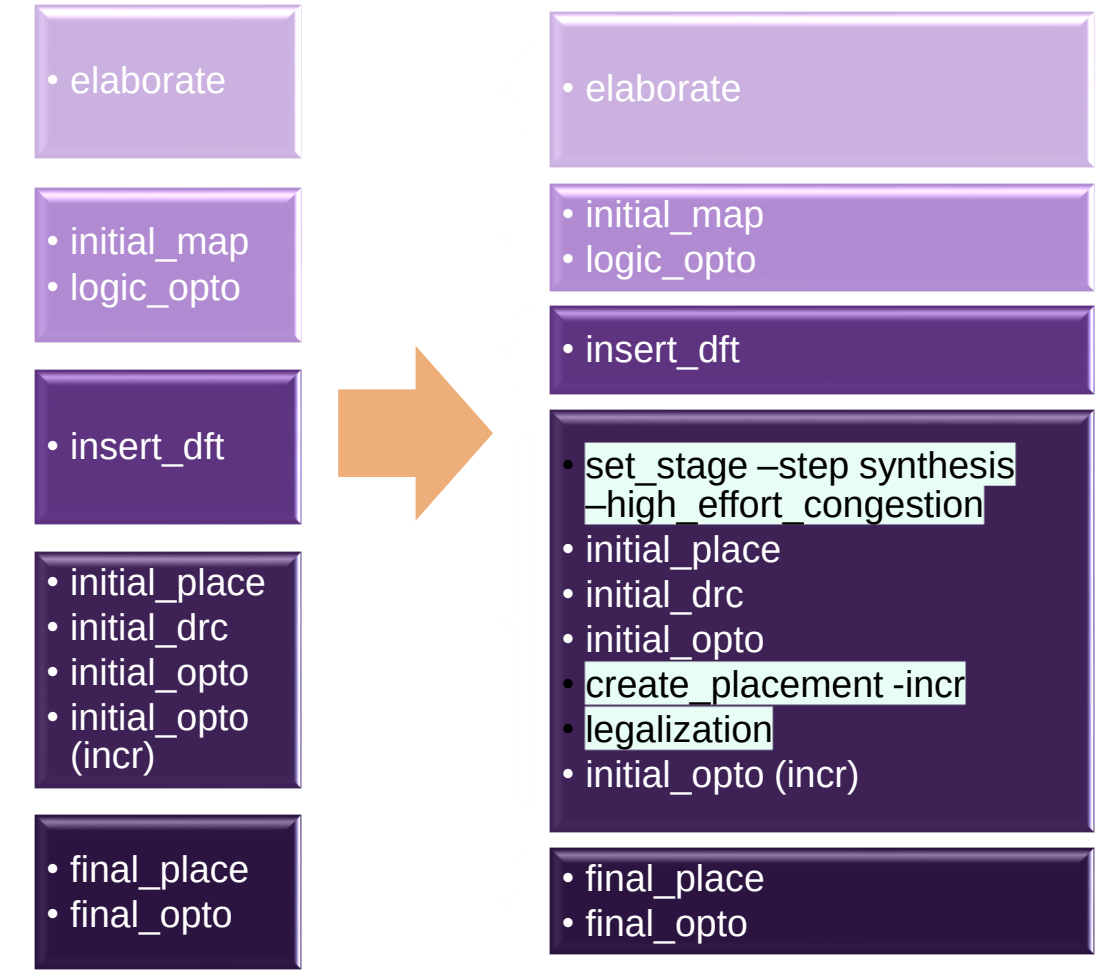
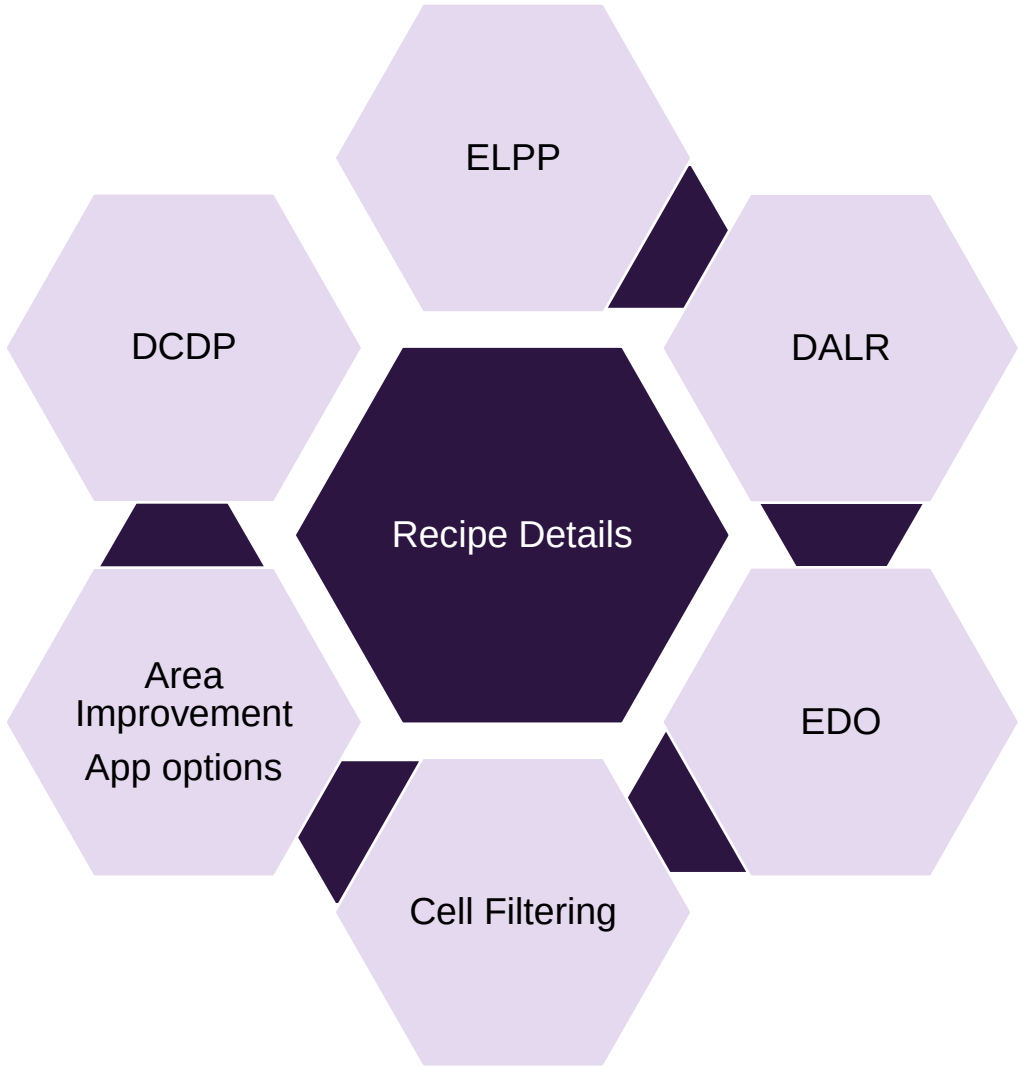
- ***set_technology –node***
- ***set_stage –step synthesis –high_effort_congestion***
- ***set_qor_strategy –metric timing –stage synthesis –mode balanced*** mega switch
- ***create_placement -incr*** and ***legalize*** post first initial_opto compile



Synthesis Strategy

- Direct Congestion Driven Placement (DCDP):- optimizes congestion as part of placer directly.
- Enhanced Low Power Placement (ELPP):- Switching Power Reduction During Placement.
- Destructive Advanced Logic Restructuring (DALR):- Restructure logic across hierarchies to improve QoR.
- Enhanced Delay Optimization (EDO):- Better delay optimization on Path Groups.
- Cell Filtering:- Filter high pin count cells at Initial Map to avoid congestion.
- Area Improvement:- Improve area optimization.



Synthesis Results

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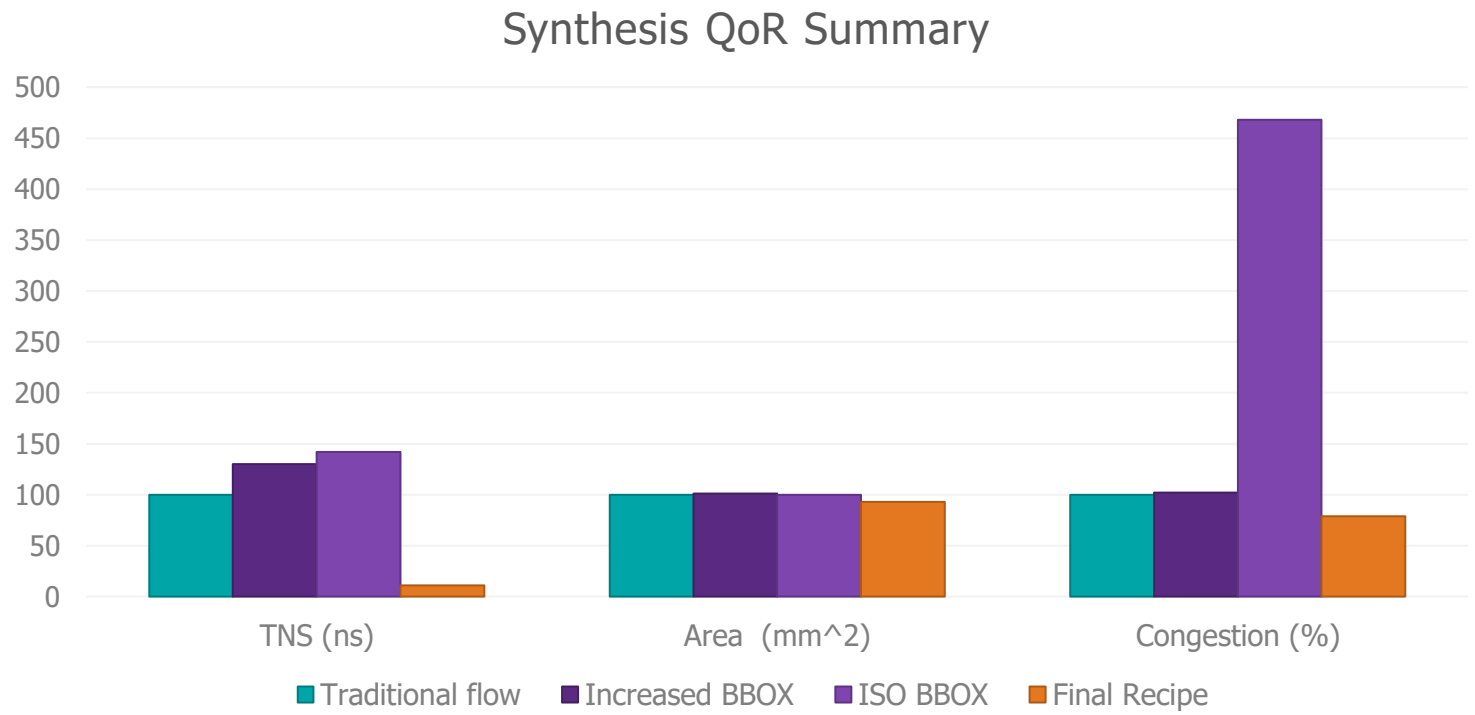
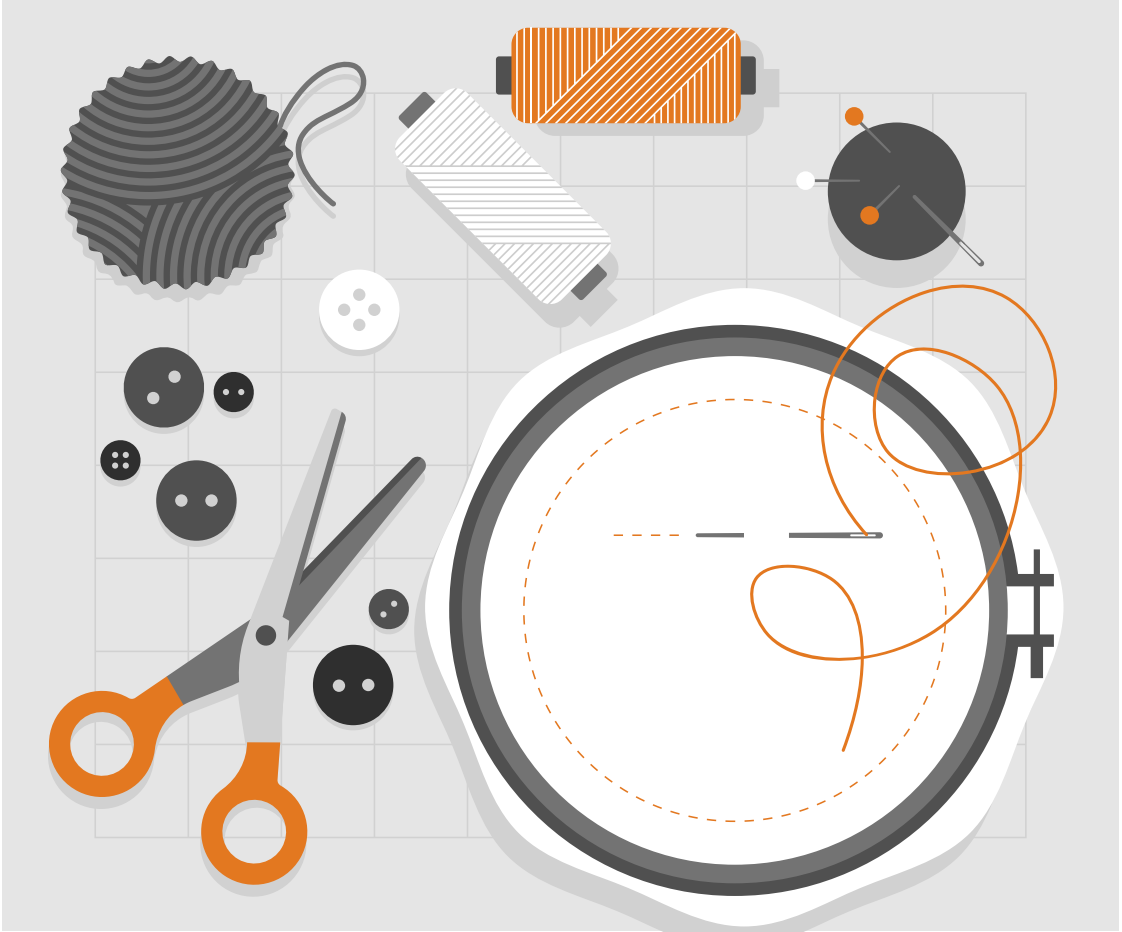


- Able to improve timing and congestion issues compared to traditional flow.
- Area impact was minimal.
- Trade off on total power vs higher frequency/ routing challenges.

Synth Netlist Handover to PD Team



PnR Challenges

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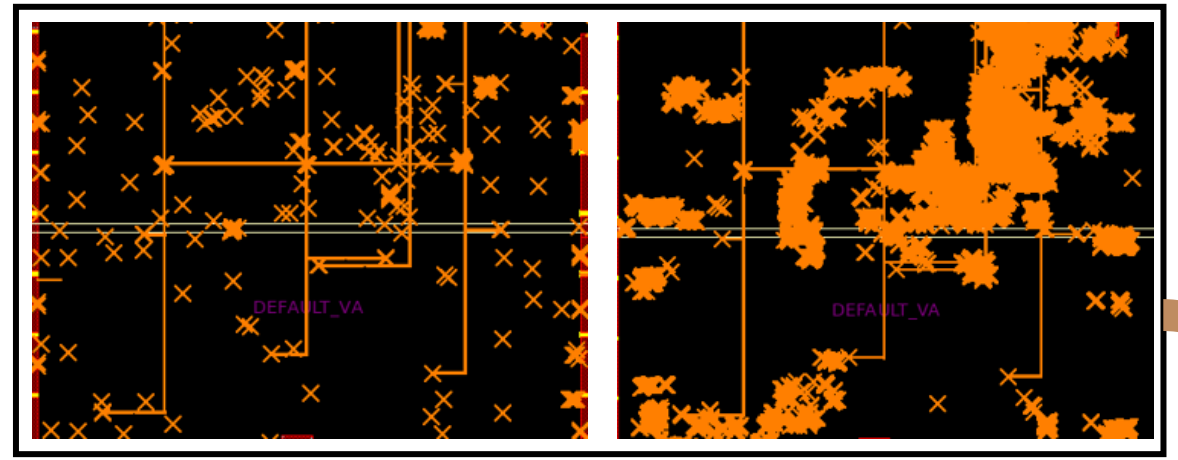
Congestion/Area

Route to PRO route degradation

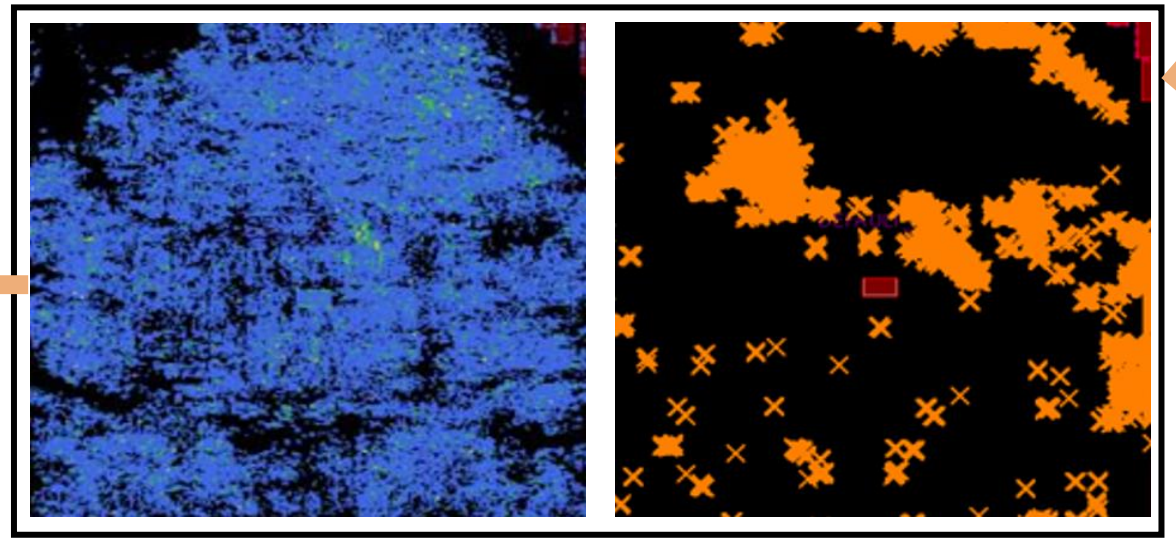
Baseline	Place Congestion	Route DRC/ Short	Post-Route DRC/Short
More ML version and recipe	Ref	Ref	Ref
Intermediate version and recipe	⬇ 15%	~10%/~80%	~44%/~96%
Final version and recipe	⬇ 34%	~83%/~90%	~96%/~99%

Route

Post-Route



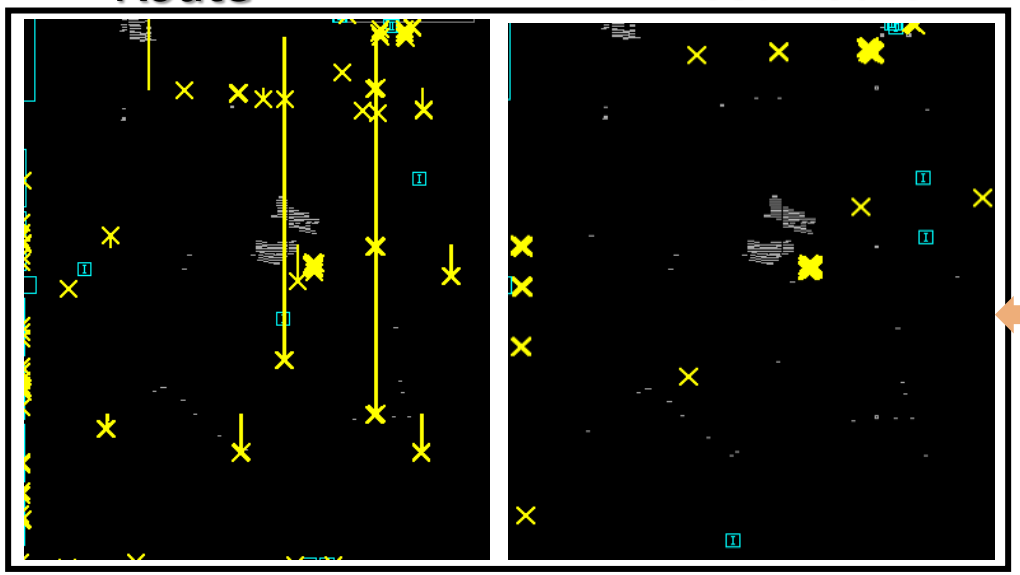
Baseline



Intermediate

Route

Post-Route



Final

PnR Challenges

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Congestion/Area Improvement Solutions

Area

- Hold aware budgeting with selective hold critical scenarios
- ADC (Auto Density Control) true & initial_place options
- set_qor_strategy -metric total_power -mode balanced
- time.enable_ccs_rcv_cap
- time.delay_calc_waveform_analysis_mode

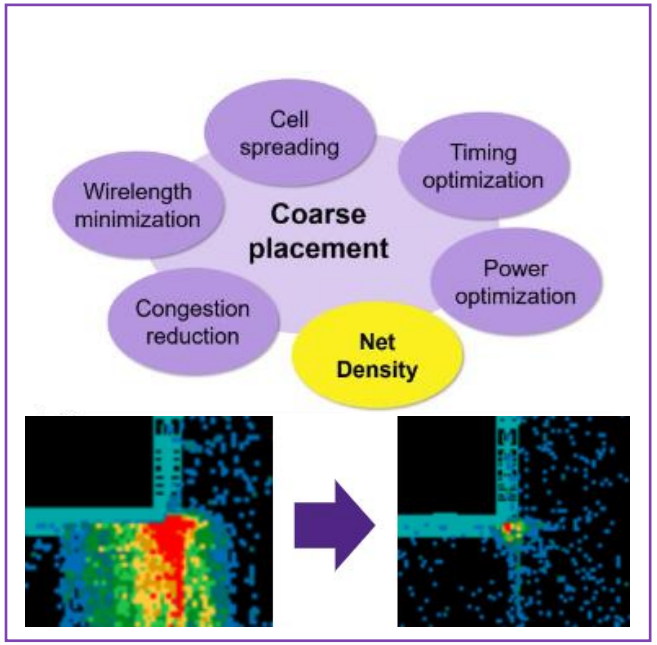
Congestion

- DCDP (Direct Congestion Driven Placement)
- place.coarse.experimental_delay_weight
- DTDP (Direct Timing Driven Placement) Scenario selection
- place.coarse.target_routing_density
- place_opt.initial_drc.global_route_based

Post-CTS

- MLGR New model + via derates all corners + hold_inst tbc
- Set_qor_strategy –metric timing -mode balanced
- set_app_options -name opt.common.power_flow -value preserve_area

DCDP



PnR Challenges

Performance

- GR-DR miscorrelation
  - SI impact
  - Lower layer routing
  - CLK NDRs
- CCD offset trials
  - Early MSCTS
- Hold BW regions
- DCD degradation
- Setup-hold critical paths
- Latency improvements

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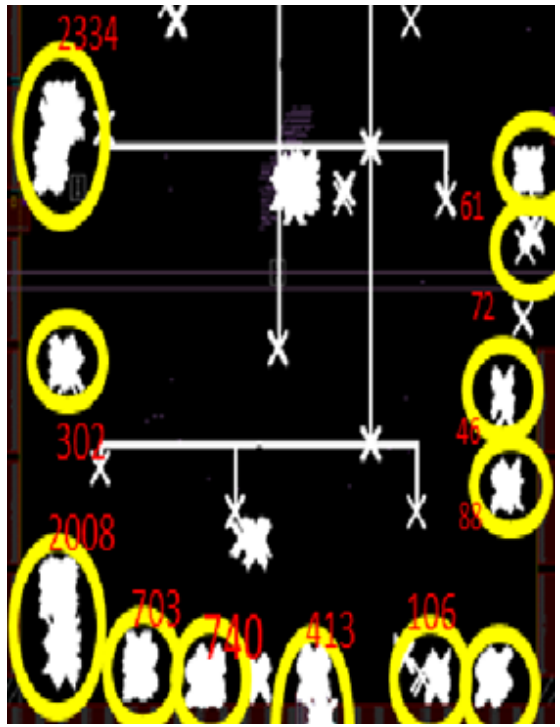
	Post-CTS Non-SI	Route Non-SI	Post-CTS SI	Route SI
Setup TNS	Ref	minor change	Ref	20X ⬆
Hold TNS	Ref	minor change	Ref	3X ⬆



PnR Challenges

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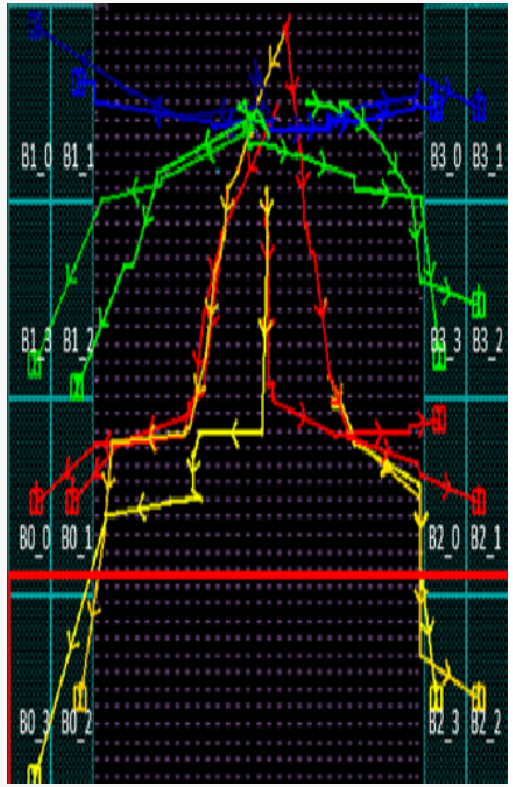
Performance Improvement Solutions

- For bridging the GR-DR miscorrelation
  - SNPS provided MLGR models for reduced metal stack
  - Via derates to mimic the DR fallout
- Hold BWs
  - DCDP across stages
  - HAB flow
  - TBC for hold buffer count reduction
- CCD refinements
  - Staggered CCD approach
  - 900% ⬇TNS for these PG's
  - 89% ⬇in FEP



Baseline					
Default Recipe	R2R TNS	R2R NVE	R2R H TNS	R2R H NVE	Util %
Post-CTS	Ref1	Ref2	Ref3	Ref4	Ref5
Route	65X	26X	16X	8X	+1%
Post-Route	0.6X	0.9X	0.3X	0.6X	+5%
Intermediate					
Default Recipe	R2R TNS	R2R NVE	R2R H TNS	R2R H NVE	Util %
Post-CTS	Ref1	Ref2	Ref3	Ref4	Ref5
Route	22X	11X	12X	5X	+0.5%
Post-Route	0.25X	0.6X	0.25X	0.37X	+3%
Final					
Default Recipe	R2R TNS	R2R NVE	R2R H TNS	R2R H NVE	Util %
Post-CTS	Ref1	Ref2	Ref3	Ref4	Ref5
Route	10X	5X	1X	22X	0%
Post-Route	0.15X	0.30%	0.7X	0.7X	+1%

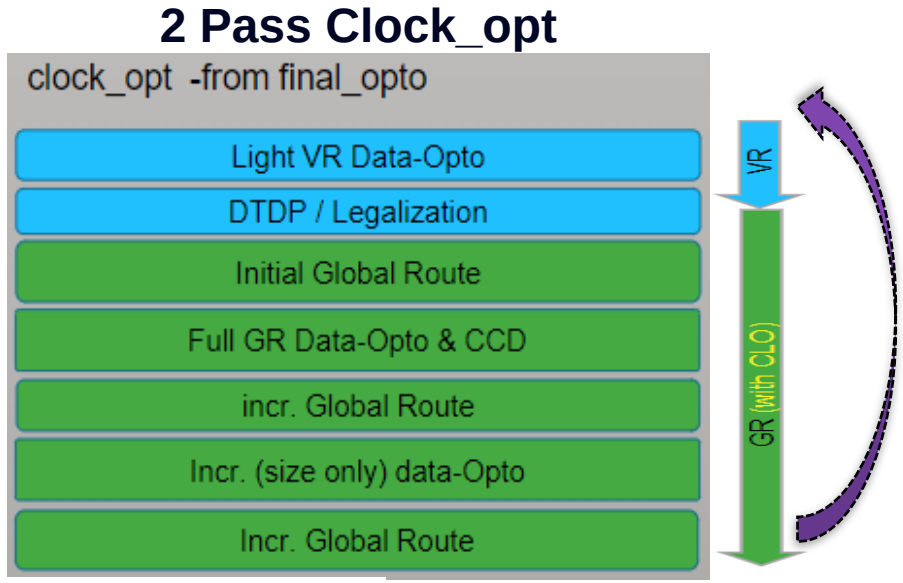
PnR Challenges

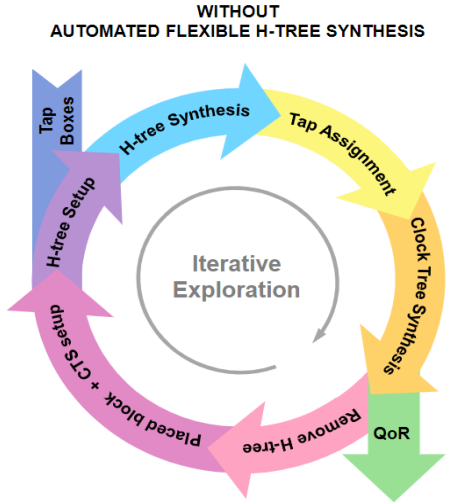
Performance Improvement Solutions (Contd.)

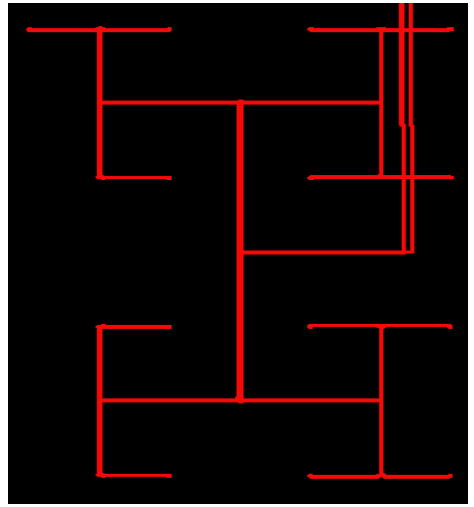
- DCD improvements
  - cts.common.prefer_inverter_for_delay_insertion true
  - cts.compile.repeater_selection inverters_only

- Setup-hold critical paths
  - Two pass clock-opt ; SNPS tbc
  - Manual ECO for left over paths.

- Latency improvement
  - Flex H-tree based MSCTS
  - split_clock_cells -latency_driven -cells [get_cells a1]
  - 10%⬇ in latency & 15%⬇ in skew
  - 40% improvement in hold TNS.







PnR Challenges

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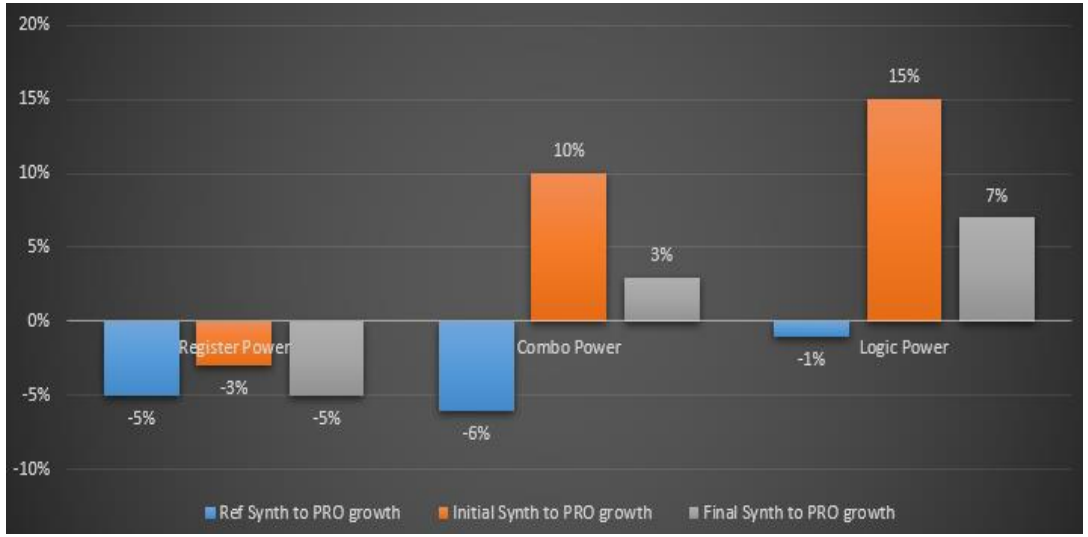
Power

- Synth -> Post-Route
  - ~15% increase in logic power Dyn power
  - ~44% increase in Lkg power
- Power critical cores are multi instantiated.
- Reduced layer shooting up congestion and timing violations; in turn tool upsizing and excessive buffer for fixing violations
- GR-DR miscorrelation
- High SI impact from GR->DR



	Ref Synth to PRO growth	Initial Synth to PRO growth	Final Synth to PRO growth
Register Power	-5%	-3%	-5%
Combo Power	-6%	10%	3%
Logic Power	-1%	15%	7%

PnR Challenges

Power Improvement Solutions

- **Synth stage:**
  - EIO/EDO
- **Place stage:**
  - InDesign PrimePower
    - Generate refreshed Saif using input FSDB's
    - Generated Saif read back in FC with accurate switching activity
    - Two pass Final Place & Final opto
- **PCO stage:**
  - Two pass clock_opt
- **Post Route stage:**
  - Lower DCVS FMAX Relaxation

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Traditional flow

Initial_place

HFN

Initial_opto

Final_place

Final_opto

Qualcomm IDPP-Place flow

Update_indesign_activity Initial_place

Update_indesign_activity HFN

Update_indesign_activity Initial_opto

Update_indesign_activity Final_place

Update_indesign_activity Final_opto

Update_indesign_activity Incr. Final_place Incr. Final_opto

PnR Challenges

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Power Improvement Results

Recipe	% Dynamic Improvement	Std cell area	DRC	Leakage
EIO/EDO	0.60%	Same	NA	4%
IDPP	1.50%	Same	NA	-6.50%
Two pass final Place & opto	0.02%	-0.28%	Same	-2.30%
2Pass Clock_opt	1.10%	-0.12%	Same	-2.80%
FMAX Reduction at PRO	2.60%	-3%	-415%	Same
Total	7%			

Final Results

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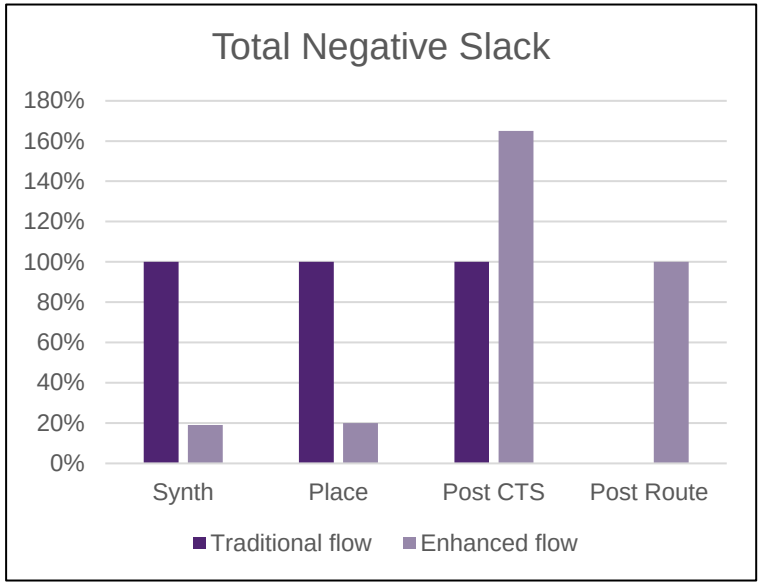

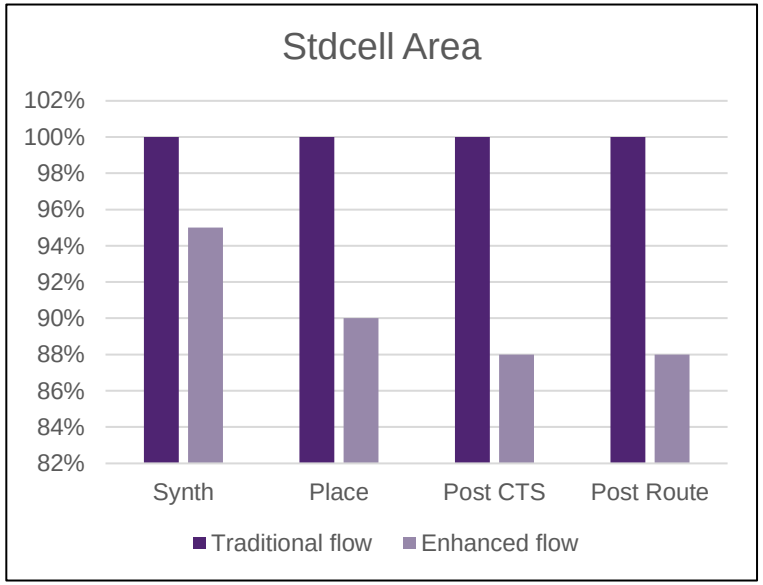

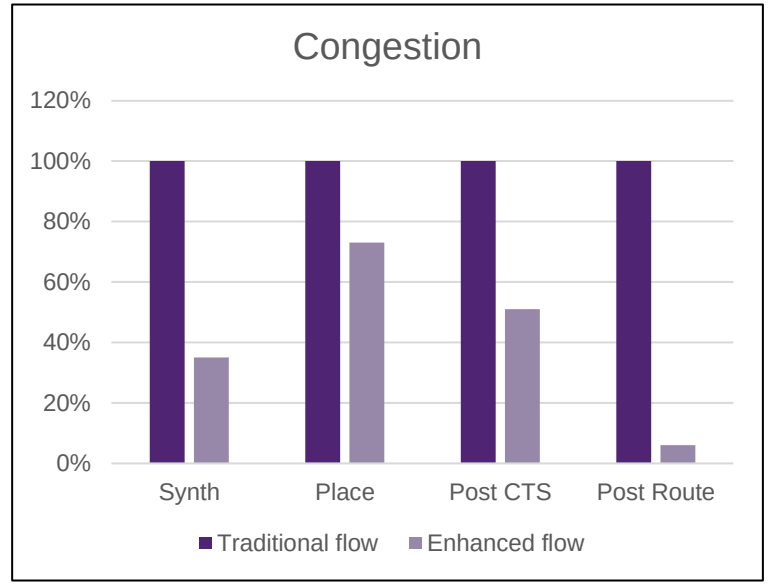

- Timing(TNS) in enhanced flow was converged but traditional flow in post route tool does not complete.
- Stdcell Area is better in Enhanced flow.
- Design not routable with Traditional flow, was route-able in enhanced flow.

Conclusion

- Achieved our increased target frequency with reduced metal layers.
- With congestion improvement database was routable.
- This flow is now default for all high-performance cores trying to achieve higher frequency.

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THANK YOU

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PnR Challenges

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Congestion/Area

Place

- ~~Hold aware budgeting with selective hold critical scenarios~~
- set_qor_strategy -metric total_power -mode balanced
- AWP CCS
- ~~set_app_options -name time.enable_ccs_rcv_cap -value true~~
- ~~set_app_options -name time.delay_calc_waveform_analysis_mode -value full_design~~
- ~~Custom values for place.coarse.experimental_delay_weight~~
- ~~DCDP~~
- ~~Careful selection of DTDP scenario after lot of trials~~
- ~~Ultra congestion effort~~
- ADC true & initial_place options
- Custom values for place.coarse.congestion_driven_max_util
- Custom values for place.coarse.target_routing_density
- Place_opt ccd
- place_opt.initial_drc.global_route_based (for notch congestion)

Post-CTS onwards

- MLGR New model + via derates all corners + hold_inst tbc
- Set_qor_strategy timing
- set_app_options -name opt.common.power_flow -value preserve_area