

7NM SoC ESD & LUP reliability signoff using IC Validator PERC



Sunil Kharate

Broadcom



Dinesh Londhe

Agenda

Agenda



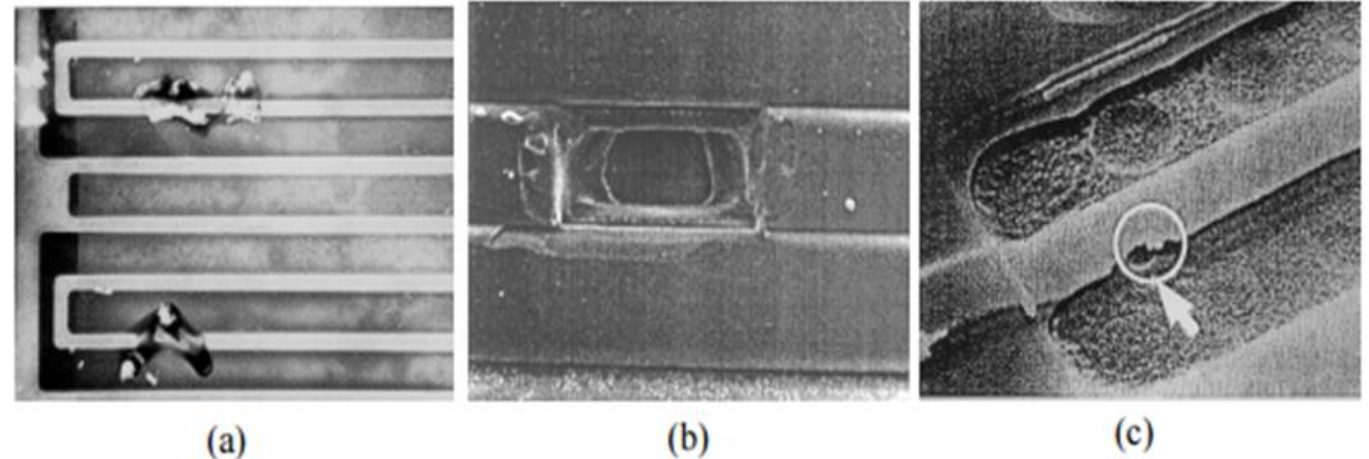
- ESD & LUP Overview
- ICV PERC Flow
- PERC reported Issues and Solutions
- Conclusion
- Acknowledgement

ESD & LUP Overview

ESD & LUP Overview

Why is ESD protection needed?

- Whenever two electrically different bodies make contact there will be a transfer of charge to equalize the electrical potential
- Specifically for ICs examples can be touching by a human being, contacting by a piece of handling equipment, etc.
- Depending on the amount and rate of charge transferred the process can be damaging to the IC



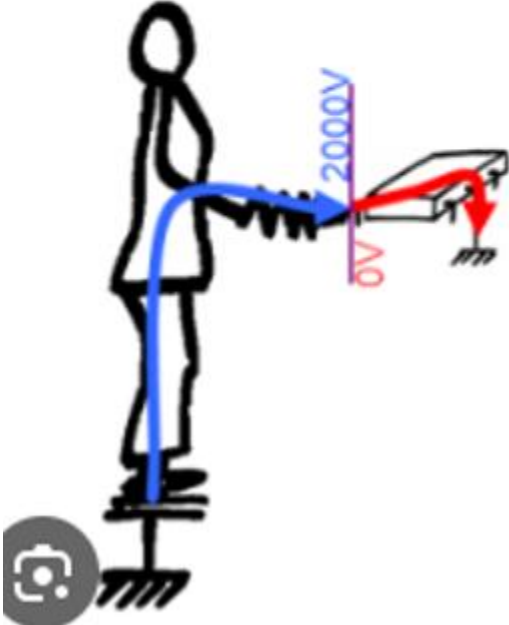
ESD Failures in ICs: (a) junction breakdown, (b) metal/via damage, (c) gate oxide damage

ESD & LUP Overview

Types of ESD models

HBM

100pF, 1500 Ohm
(external source)
2kV – 1.33A – 10n/150ns



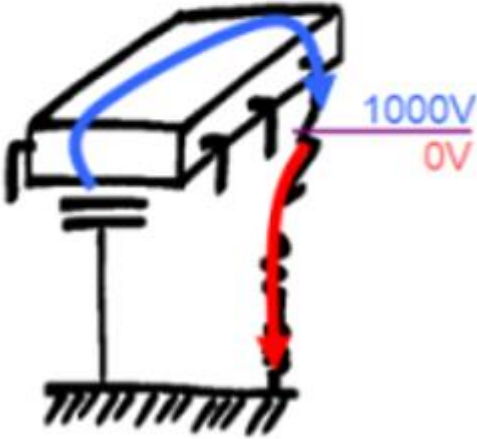
MM

200pF, 0 Ohm
(external source)
200V – 3.5A – 20n/250ns



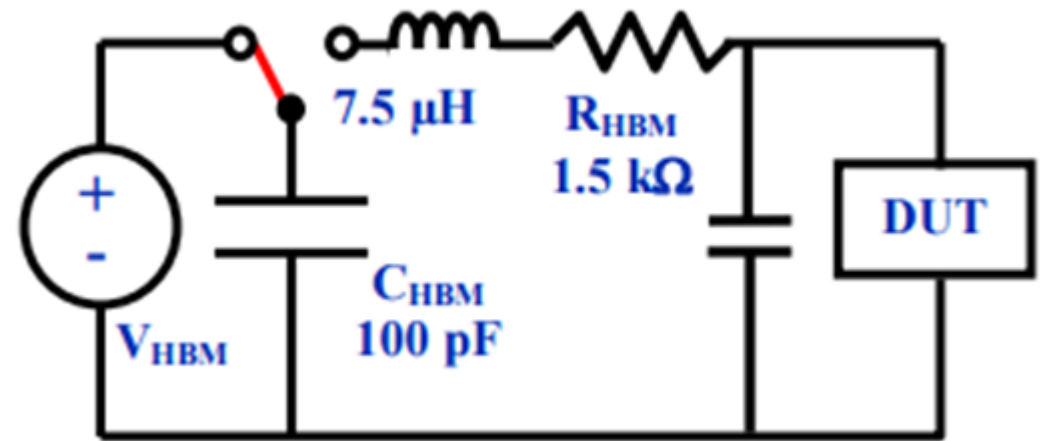
CDM

package cap. vs. gnd
(IC is part of stress model)
1kV – 10A – 1n/5ns



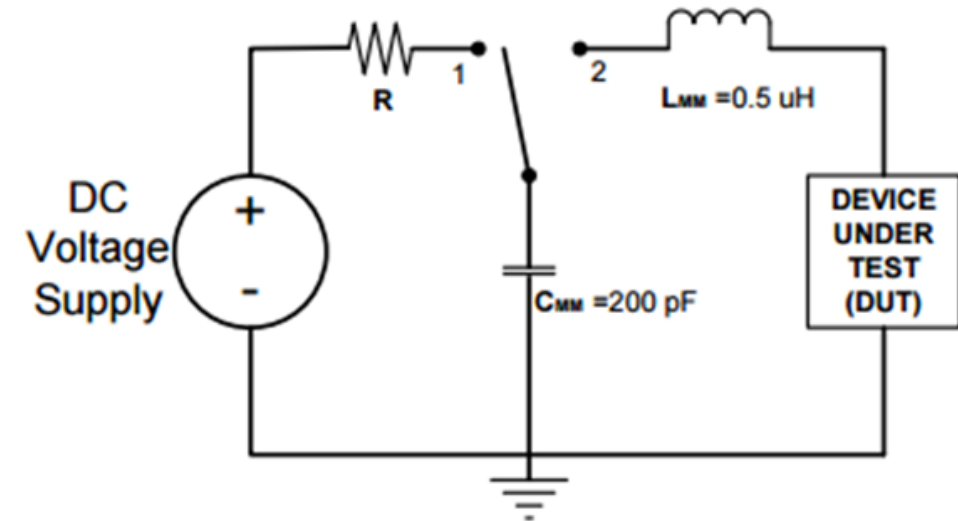
Human Body Model (HBM)

- Simulates a charged person touching an IC
- The capacitance of a typical human body is 100pF
- Discharge resistance is 1.5kOhm
- It is a relatively slow pulse with a 150ns time constant
- The goal is to pass 2kV in both positive and negative polarities of stress and all pin combinations



Machine Model (MM)

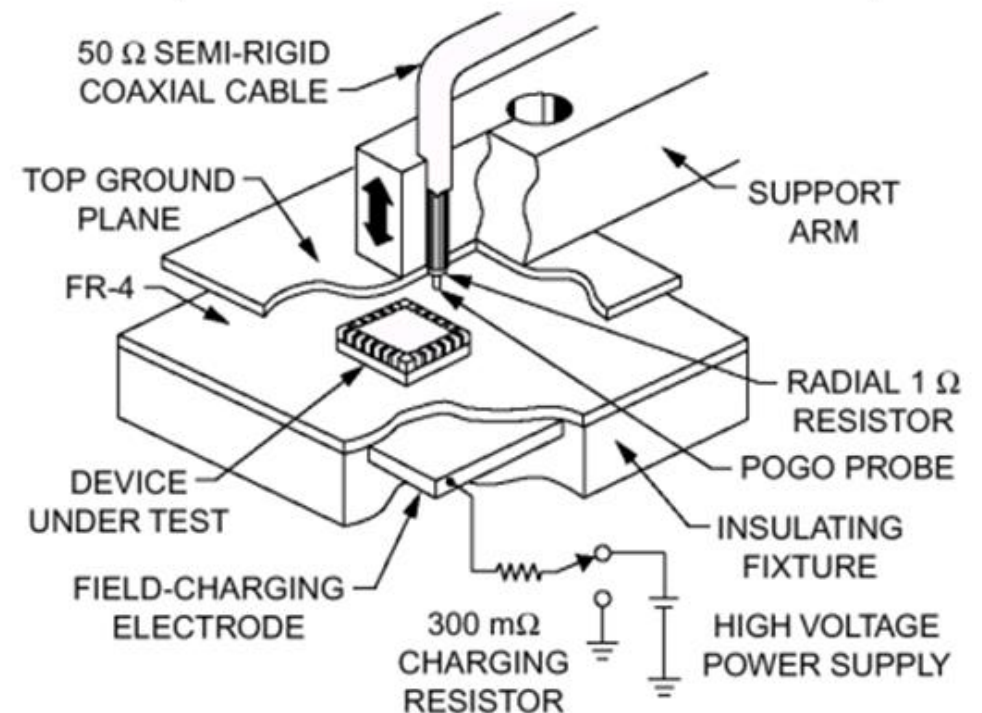
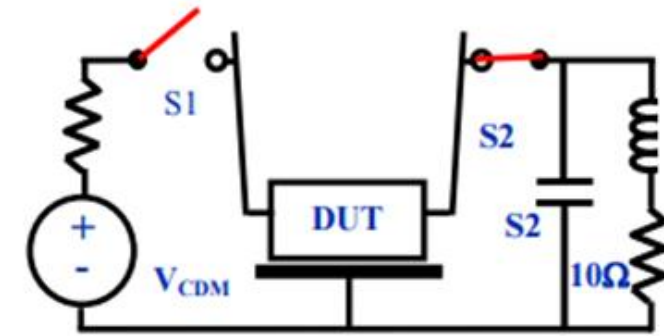
- Simulates a charged metallic handler touching an IC
- The capacitance is 200pF
- Arc resistance is 10-20 ohms
- It is an oscillatory pulse with a few tens of ns period
- Failure modes are similar to HBM – mainly junction breakdown
- 2kV HBM is equivalent to ~200V MM



Charged Device Model (CDM)

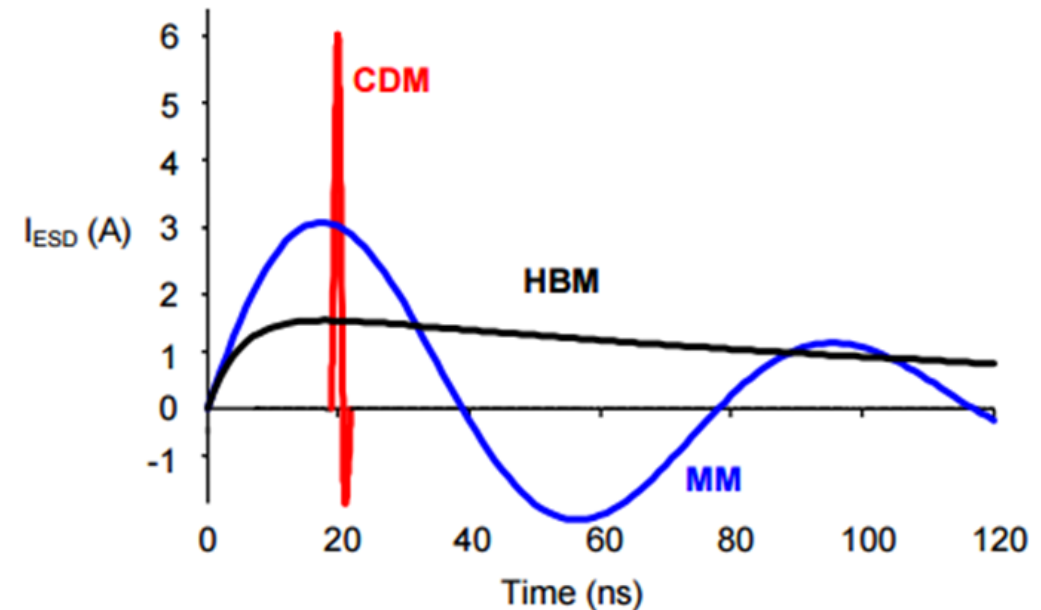


- Simulates a triboelectrically charged device discharging through one pin to ground
- The capacitance is device/package dependent
- Resistance is very low; 1 ohm is used in the tester for consistency
- It is an oscillatory decaying pulse with a fraction of ns period
- Failure modes are usually dielectric breakdown
- Goal is to pass 500V; high speed pins may only pass 200V

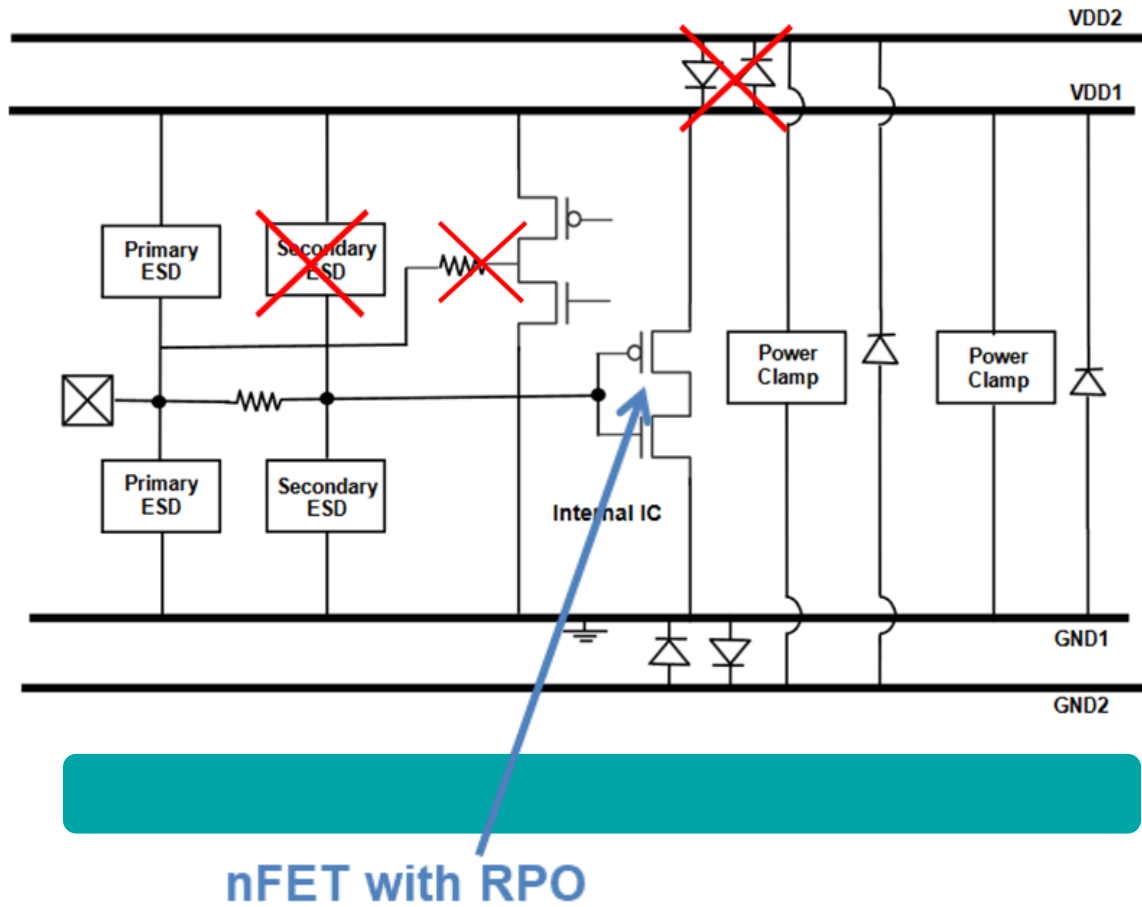


Pulse shapes of the various ESD models

- HBM is the slowest pulse with a time constant of 150ns
- CDM is the fastest, yet the highest peak current pulse
- Because of the similar failure modes between HBM and MM most IC companies adopted a policy of just stressing for HBM and CDM



General configuration of IC Protection

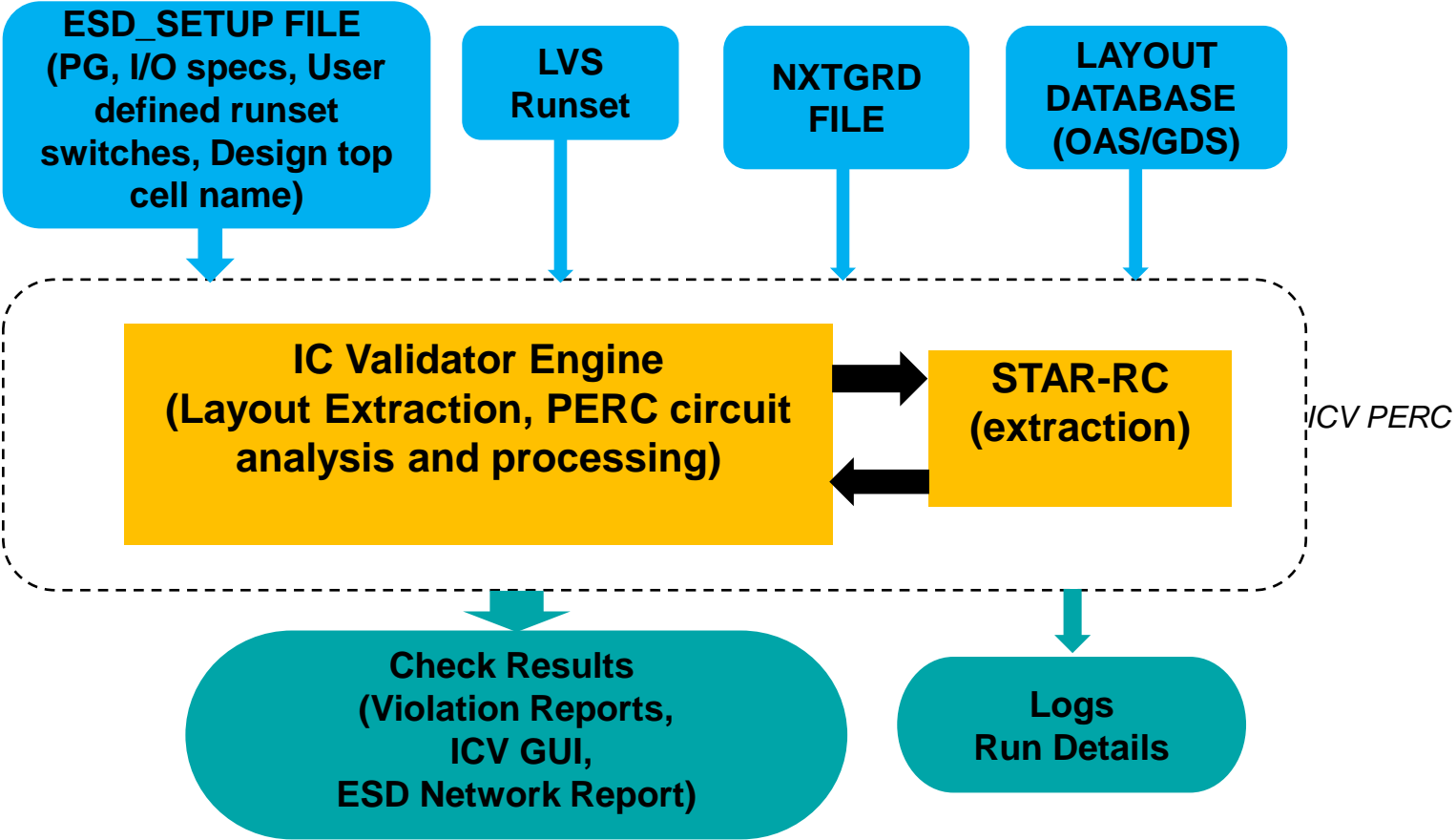


- A network of diodes and ESD clamps provides the ESD discharge paths
- VDD1 to VDD2 back-to back (b2b) diodes - although good for ESD are not desirable since they create dependency between power supplies
- The secondary ESD to VDD1 is not needed
- The resistor to both pFET and nFET of the output driver is replaced with nFET with RPO in the drain

IC Validator PERC Flow

ICV PERC Flow

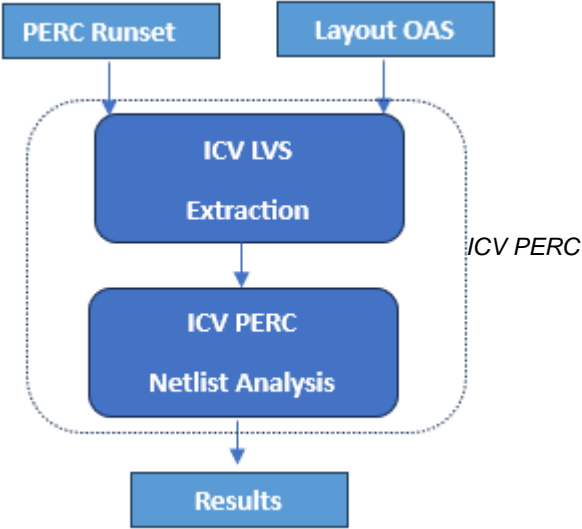
Flow Chart



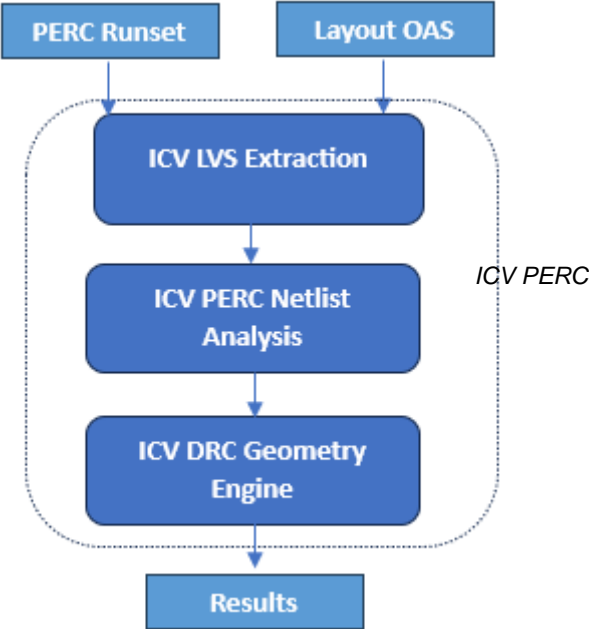
ICV PERC Flow

Different Modes

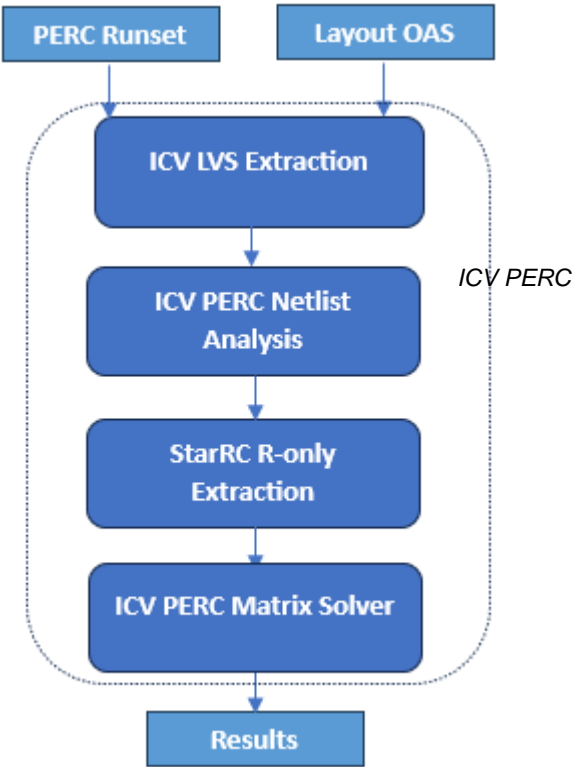
TOPO Check



LDL Check



P2P/CD Check



Rule Coverage



Topology Checks (TOPO)	Layout Driven Check (LDL)	Effective Resistance Check (P2P)	Current Density Check (CD)
Checks primary I/O ESD	Checks primary I/O ESD	Checks primary I/O ESD	Checks primary I/O ESD
Secondary IO ESD	Power Clamp	Secondary IO ESD	Secondary IO ESD
Power Clamp	Cross Domain	IO/PG to Clamp Path	Power Clamp Path
Cross Domain ESD	Gate Victim	Clamp to Clamp Path	Current Density Check (CD)
Ground B2B Diode	Latch-up	Ground B2B Diode Path	Checks primary I/O ESD
		PG Pad to Pickup Path	Secondary IO ESD

ICV PERC Flow

Debug Flow

CHECK ESD_NETWORK_REPORT AND RULES



CHECK TOP LEVEL POWER CLAMP VIOLATIONS



CHECK CROSS DOMAIN VIOLATIONS (IF THERE IS NO COMMON GROUND).



CHECK OTHER INTEGRATION LEVEL PERC VIOLATIONS



CROSS CHECK IP INTERNAL VIOLATION WAIVERS

ICV PERC Violations & Solutions

TOPO Check



Violation: ESD.NET.1gU

- Issue: Primary ESD protection missing for I/O pin

The screenshot shows a design tool interface with several panels. At the top, there are tabs for 'Load Results', 'Run Summary', 'Extraction Errors', and 'PERC Results'. Below the tabs is a search bar and a toolbar with icons for various functions. The main area is divided into two primary sections: 'Violation Browser' on the left and 'Info Rule Browser' at the bottom. The 'Violation Browser' table lists various error types and their counts. The 'Info Rule Browser' table shows the flat count for the 'soc' cell. On the right side, there is a 'Netlist Information Window' showing details for a specific violation.

Cell/Violation/Error	Error	Flat Errors	Total Errors
soc		3319	3319
LUP.WARN.4U		33	33
ESD.WARN.4.2gU		1	1
ESD.NET.1gU		2	2
NET2		1	1
NET1		1	1
ESD.NET.1.1gU		177	177
ESD.CDM.B.2gU		2548	2548
ESD.CDM.B.1gU		4	4
ESD.CDM.6g		27	27
ESD.CDM.4gU		1	1
ESD.9.0.1gU		220	220
ESD.8gU		4	4
ESD.8.1gU		114	114
ESD.47gU		169	169
ESD.45.0.1gU		11	11
ESD.43gU		2	2
ESD.31g		2	2
ESD.15gU		4	4

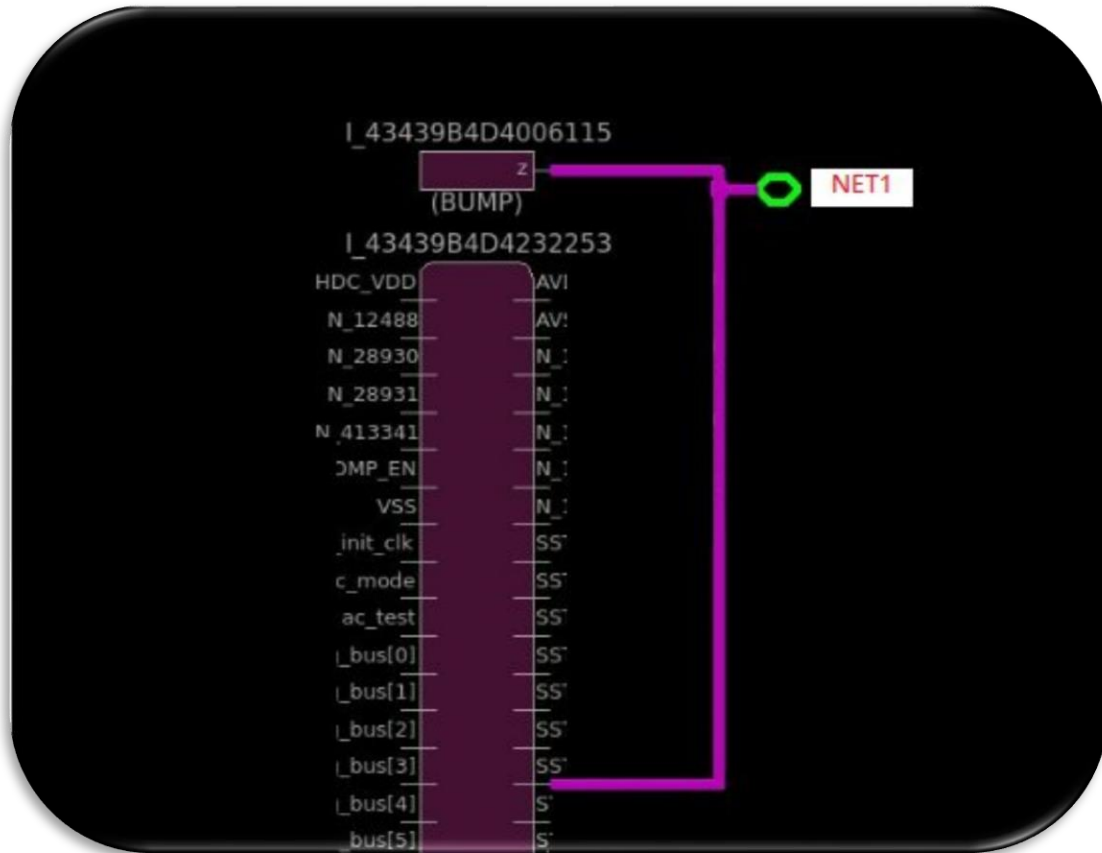
Cell/Rule/Object	Info	Flat Count
soc		296

ID	Obj	Type	Name	Notes
2	Err	Port	NET1	Tags: [io]

ESD.NET.1gU: For I/O pin ESD protection scheme, the primary ESD protection (1st ESD) devices are required and it can be one of the following listed devices: (1) Drain-ballasted (Cascode) NMOS (re
[PRIMARYNMOS] missing primary MOS; [PRIMARYUPDIO] missing I/O->Power diode; [PRIMARYDOW
missing I/O->Ground diode
Port

TOPO Check

Violation: ESD.NET.1gU



Solutions:

Topo check done in initial phase to check primary ESD protection.

P2P Check



Violation: ESD.DISTP2P

- Issue: BUMP to Clamp distance is more, resistance is more than spec.

Load Results x Run Summary x Extraction Errors x PERC Results x Parasitic Paths x

Search (Alt+E) [Icons]

Violation Browser

Cell/Violation/Error	Error	Flat Errors	Total Errors
soc	1897	1897	1897
ESD.DISTP2P.1.1.0gU	2	2	2
Path 2: NET2 ... 0.1624 = 39.7581	1	1	1
Path 1: NET2 ... 0.1465 = 39.7401	1	1	1
ESD.CDM.P.7gU	2	2	2
ESD.CDM.P.1.0gU	2	2	2
ESD.CDM.P.4gU	3	3	3
ESD.CDM.P.7.1.2gU	4	4	4
ESD.CDM.P.7.4gU	8	8	8
ESD.8.1gU	10	10	10
ESD.CDM.P.3gU	20	20	20
ESD.CDM.P.5.1gU	27	27	27
ESD.14.5gU	30	30	30
ESD.CDM.P.8gU	32	32	32
ESD.CDM.P.2gU	43	43	43
ESD.CDM.P.9gU	46	46	46
ESD.14.6gU	63	63	63
ESD.CDM.P.10gU	92	92	92
ESD.14.8gU	127	127	127
ESD.CDM.P.1gU	198	198	198
ESD.14.7gU	1188	1188	1188

Details

ID	Obj	Type	Name
2	Err	Path	
		Port	NET2
		Pin	_93E8CAEF3294837/I_93E8CAEF13309946/I_93E8CAEF
		Pin	_93E8CAEF3294837/I_93E8CAEF13309946/I_93E8CAEF
		Pin	Highlight Path Fly Line
		Pin	Highlight Path Fly Line With Vprobe
		Pin	Highlight Nets
		Pin	Select all of the same violation
		Pin	PERC Path Heatmap...
		Pin	_93E8CAEF3294837/I_93E8CAEF13309946/I_93E8CAEF
		Pin	_93E8CAEF3294837/I_93E8CAEF13309946/I_93E8CAEF
		Pin	_93E8CAEF3294837/I_93E8CAEF13309946/I_93E8CAEF
		Pin	_93E8CAEF3294837/I_93E8CAEF13309946/I_93E8CAEF

ESD.DISTP2P.1.1.0gU: Metal Bus resistance of R0 in ESD.DISTP2P.1.1gU <=

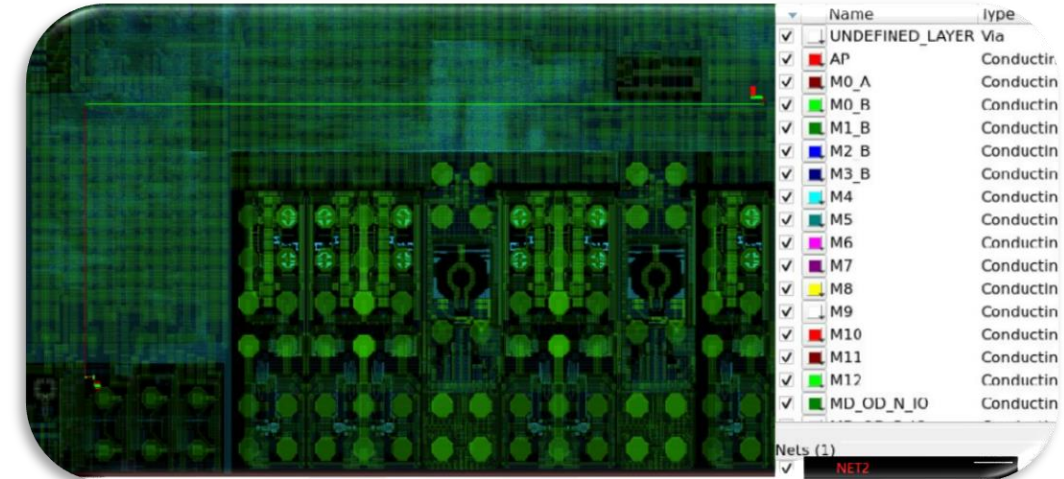
Info Rule Browser

Cell/Rule/Object	Info	Flat Count
soc		363

P2P Check

Violation: ESD.DISTP2P : PERC PATH HEATMAP

Layer ID	Name	Type	Contribution (%)	R (Ω)
0	Total		100.000000	39.758100
20	M12	Conducting	67.290372	26.753373
19	M11	Conducting	25.038859	9.954975
18	M10	Conducting	6.753456	2.685046
45	VIA11	Via	0.224224	0.089147
44	VIA10	Via	0.214761	0.085385
31	n_odtap_io	Via	0.162031	0.064421
3	AP	Conducting	0.035155	0.013977
26	VD_MD_OD_N_IO	Via	0.031970	0.012711
34	VIA0	Via	0.029111	0.011574
16	M8	Conducting	0.020571	0.008178
7	M1_B	Conducting	0.018946	0.007533
33	RV	Via	0.017332	0.006891
15	M7	Conducting	0.015375	0.006113
14	M6	Conducting	0.014079	0.005598
42	VIA8	Via	0.013812	0.005492
13	M5	Conducting	0.013202	0.005249
35	VIA1	Via	0.010780	0.004286
12	M4	Conducting	0.010058	0.003999
37	VIA3	Via	0.010054	0.003997
36	VIA2	Via	0.009793	0.003894
9	M2_B	Conducting	0.009207	0.003661
11	M3_B	Conducting	0.008373	0.003329
41	VIA7	Via	0.008075	0.003211
21	MD_OD_N_IO	Conducting	0.007529	0.002993
40	VIA6	Via	0.005404	0.002149
39	VIA5	Via	0.004371	0.001738



Solutions: we moved bump closure to clamp to reduce the M11 and M12 resistance.

P2P Check



Violation: ESD.CDM*

- Issue: BUMP to Clamp resistance is out of specs.

The screenshot shows a software interface with several tabs: Load Results, Run Summary, Extraction Errors, PERC Results, and Parasitic Paths. The main window is divided into a Violation Browser and a Details panel.

Violation Browser

Cell/Violation/Error	Error	Flat Errors	Total Errors
soc	1897	1897	1897
ESD.CDM.P.1gU	198	198	198
Path 61: X1711755 ... + 0.2519 = 0.6514	1	1	1
Path 132: X1711755... + 0.6616 = 1.0553	1	1	1
Path 193: X1711755... + 0.2202 = 0.6142	1	1	1

Details

ID	Obj	Type	Name
132	Err	Path	
		Pin	
		Net	
		Pin	
		Pin	
		Pin	
		Pin	
		Pin	
		Pin	
		Pin	
		Pin	
		Pin	

ESD.CDM.P.1gU: Metal Bus resistance of IOPAD to ESD dual diode R1 & R3. <= [redacted] . Metal Bus resistance of IOPAD to ESD snapback NMOS (nch_HIA18) R3. <= [redacted] . No needed to take "R0" into account.

R1 Component of Source Pin : I/O Net -> Sink Pins : Primary Down Diode Protection Pins: [redacted] :: Full path resistance (R0 + R1): [redacted]

Info Rule Browser

Cell/Rule/Object	Info	Flat Count
soc		363

P2P Check

Violation: ESD.CDM*

Highlight Path

Colored by...
Physical Layer

Layers (43)

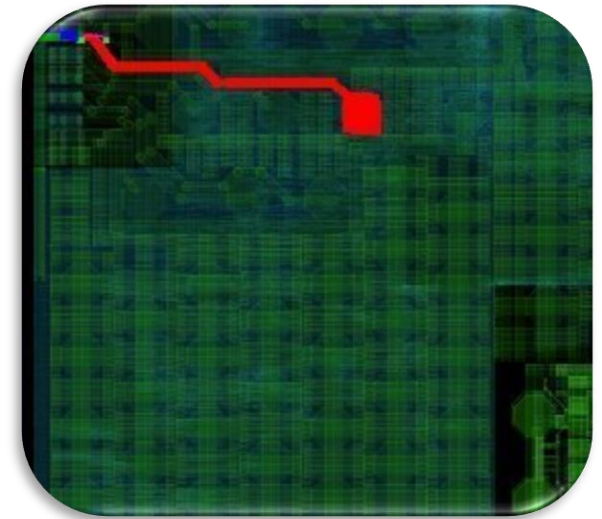
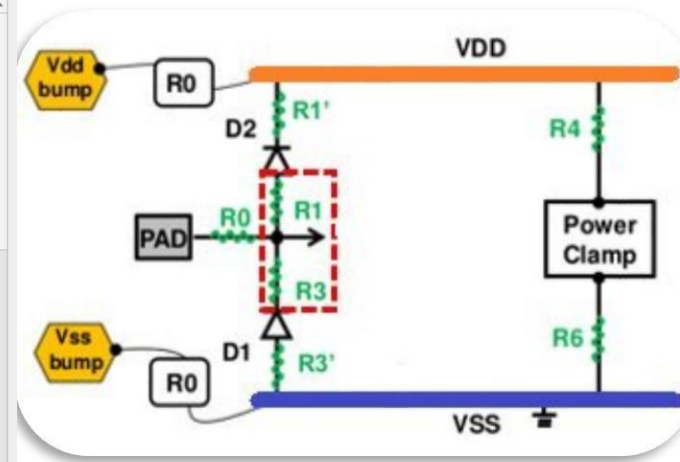
- UNDEFINED_LAYER Via
- AP Cor
- M0_A Cor
- M0_B Cor
- M1_A Cor
- M1_B Cor
- M2_A Cor
- M2_B Cor
- M3_B Cor

Nets (1)

- PRE_WUS

Hide VUE Highlight

Layer ID	Name	Type	Contribution (%)	R (Ω)
0	Total		100.000000	1.055300
2	AP	Conducting	38.110293	0.402178
16	M10	Conducting	16.371720	0.172771
10	M4	Conducting	11.008453	0.116172
9	M3_B	Conducting	7.971019	0.084118
29	n_odtap_io	Via	7.686878	0.081120
7	M2_A	Conducting	3.177618	0.033533
34	VIA2	Via	2.745804	0.028976
36	VIA4	Via	1.929169	0.020359
4	M0_B	Conducting	1.618626	0.017081
33	VIA1	Via	1.548119	0.016337
24	VD_MD_OD_N_IO	Via	1.461454	0.015423
32	VIA0	Via	1.436966	0.015164
18	M12	Conducting	0.808833	0.008536
35	VIA3	Via	0.539968	0.005698
8	M2_B	Conducting	0.359760	0.003797
19	MD_OD_N_IO	Conducting	0.353838	0.003734
37	VIA5	Via	0.318662	0.003363
38	VIA6	Via	0.311403	0.003286



Solution: We reduced R3 resistance value by reducing route length of RDL

CD Check



Violation: ESD.CD*

Issue: minimum ESD current for primary ESD discharge path is more than specs

Violation Browser

Cell/Violation/Error	Error	Flat Count
soc	412	
ESD.CD.1gU	299	
Path 1: X65 PA...Multiple Sinks	1	
Path 2: X51 PA...Multiple Sinks	1	
Path 3: X31 PA...Multiple Sinks	1	
Path 4: X66 PA...Multiple Sinks	1	
Path 5: X85 PA...Multiple Sinks	1	
Path 6: X18 PA...Multiple Sinks	1	
Path 7: X52 PA...Multiple Sinks	1	
Path 8: X17 PA...Multiple Sinks	1	
Path 9: X63 PA...Multiple Sinks	1	
Path 10: X48 P...Multiple Sinks	1	
Path 11: X14 P...Multiple Sinks	1	
Path 12: X47 P...Multiple Sinks	1	
Path 13: X13 P...Multiple Sinks	1	
Path 14: X50 P...Multiple Sinks	1	
Path 15: X15 P...Multiple Sinks	1	

Info Rule Browser

Cell/Rule/Object	Info	Flat Count
soc	298	298

Details

ID	Obj	Type	Name	Notes
1	Err	Path		I=1300.0000 (mA), Tags: [cd_io_primary_mos,cd_io_primary
		Pin	PAD	(Source) PAD_DEV_FC (1186.0980, 3826.1800)
		Net		
		Pin	I 1275A449470303/X973 DRN (Sink) tndiff sdi (1147.5460, 4144.9800)	

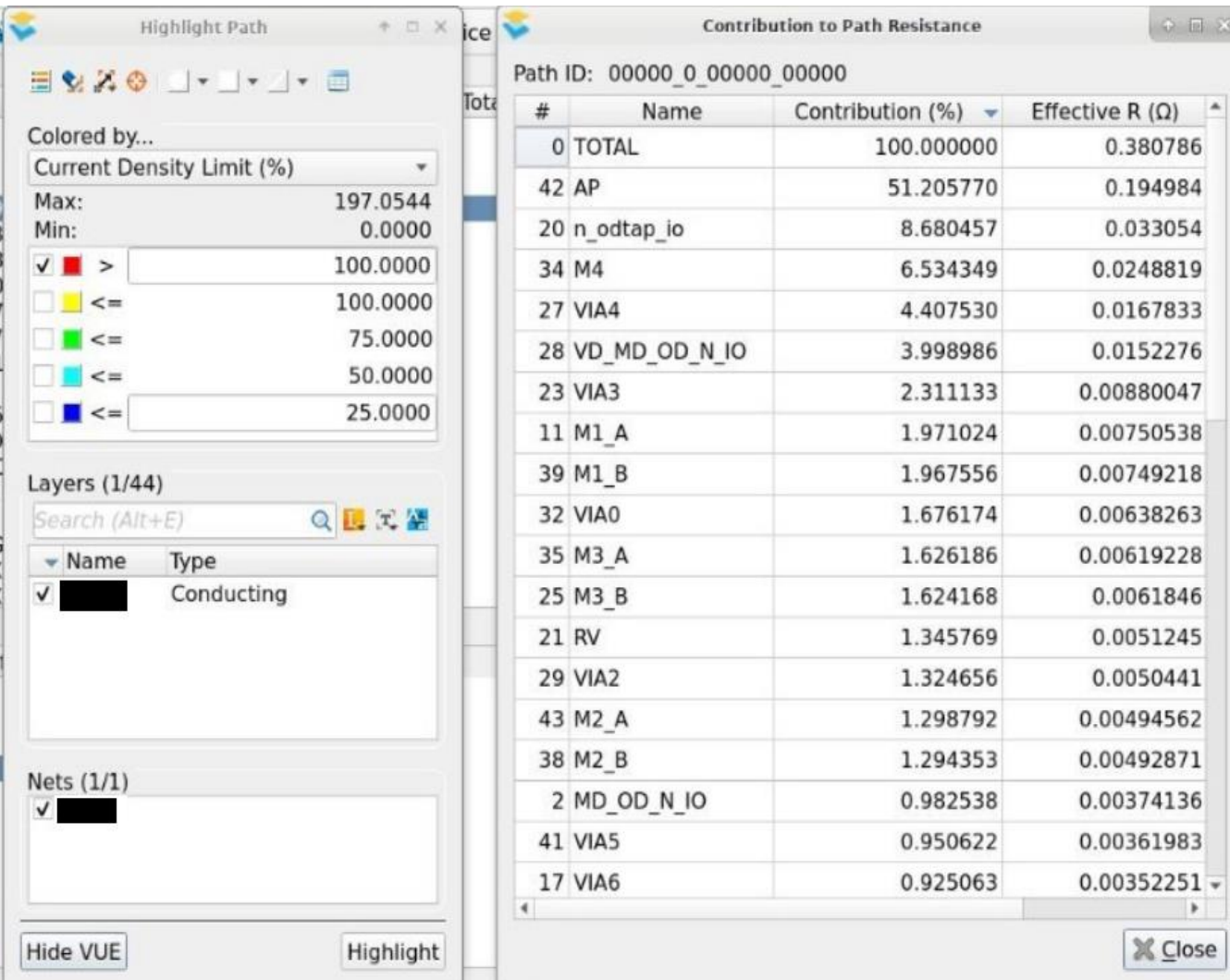
ESD.CD.1gU: Suggested minimum ESD current (unit: A, IESD) for the primary ESD discharge path >= == [redacted]
 Primary ESD devices include dual-diode, drain-ballasted NMOS, drain-ballasted cascoded NMOS, power clamp and back to back (b2b) diode. Primary ESD discharge current path includes: 1) Metal line width connecting the "bond pad" and the primary ESD device; 2) The M0_OD1/M0_OD2 area in the primary ESD device; 3) The Via number in the primary ESD device.

ID	Net	Layer	Limit (%)	CD	CD Limit	I (mA)	Width (μm)	length (μm)	a (μm)	V1 (mV)	V2 (mV)
1	[redacted]	M0	103.7022	50.2956	48.5000	11.7692	0.2340	90.7370	n/a	128.3516	123.3416
1	[redacted]	M0	113.8502	55.2174	48.5000	12.9209	0.2340	90.7370	n/a	133.8519	128.3516
1	[redacted]	M0	126.1877	61.2011	48.5000	14.3210	0.2340	90.7370	n/a	139.9482	133.8519
1	[redacted]	M0	141.3970	68.5775	48.5000	16.0471	0.2340	90.7370	n/a	146.7793	139.9482
1	[redacted]	M0	184.6024	89.5321	48.5000	20.9505	0.2340	90.7370	n/a	154.5297	156.2019
1	[redacted]	M0	160.4254	77.8063	48.5000	18.2067	0.2340	90.7370	n/a	154.5297	146.7793
1	[redacted]	M0	120.4090	58.3984	48.5000	13.6652	0.2340	90.7370	n/a	159.8678	162.5392
1	[redacted]	M0	101.1193	49.0428	48.5000	11.4760	0.2340	90.7370	n/a	158.7735	163.2206
1	[redacted]	M0	163.6519	79.3712	48.5000	18.5728	0.2340	90.7370	n/a	152.4050	157.4539
1	[redacted]	M0	142.2894	69.0104	48.5000	16.1484	0.2340	90.7370	n/a	145.5308	152.4050

ESD Network Report Details

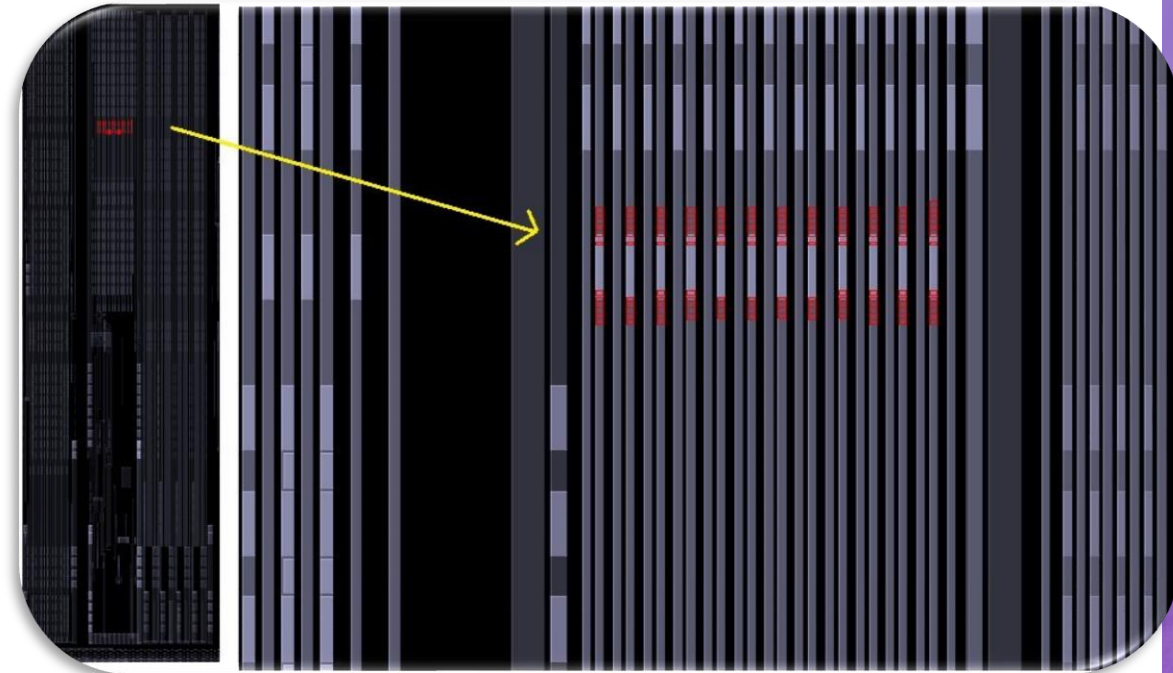
CD Check

Violation: ESD.CD*



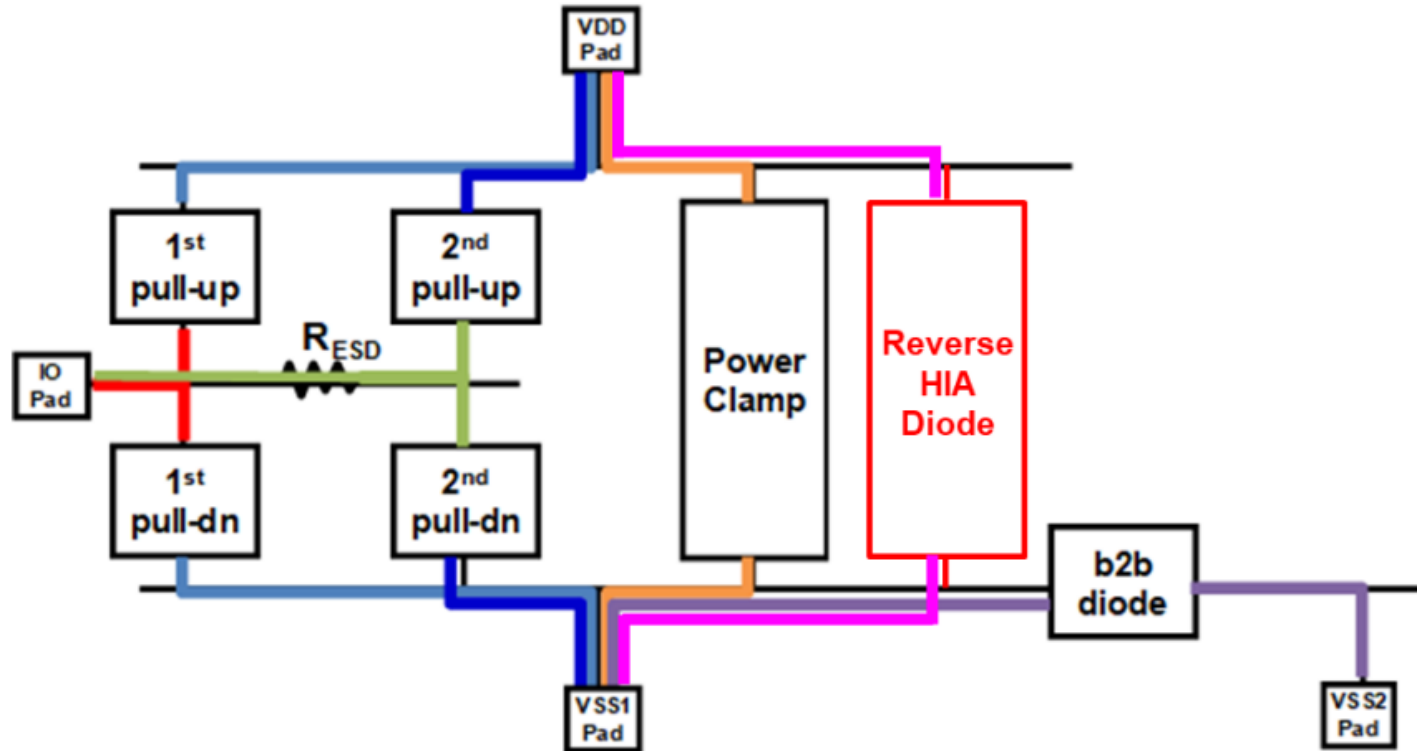
The screenshot shows two windows from a PCB design tool. The 'Highlight Path' window on the left is configured with 'Current Density Limit (%)' as the coloration metric, with a maximum value of 197.0544 and a minimum of 0.0000. A red color bar is selected for values greater than 100.0000. The 'Layers (1/44)' section shows the 'Conducting' layer selected. The 'Nets (1/1)' section shows a single net selected. The 'Contribution to Path Resistance' window on the right displays a table for Path ID: 00000_0_00000_00000.

#	Name	Contribution (%)	Effective R (Ω)
0	TOTAL	100.000000	0.380786
42	AP	51.205770	0.194984
20	n_odtap_io	8.680457	0.033054
34	M4	6.534349	0.0248819
27	VIA4	4.407530	0.0167833
28	VD_MD_OD_N_IO	3.998986	0.0152276
23	VIA3	2.311133	0.00880047
11	M1_A	1.971024	0.00750538
39	M1_B	1.967556	0.00749218
32	VIA0	1.676174	0.00638263
35	M3_A	1.626186	0.00619228
25	M3_B	1.624168	0.0061846
21	RV	1.345769	0.0051245
29	VIA2	1.324656	0.0050441
43	M2_A	1.298792	0.00494562
38	M2_B	1.294353	0.00492871
2	MD_OD_N_IO	0.982538	0.00374136
41	VIA5	0.950622	0.00361983
17	VIA6	0.925063	0.00352251



CD Check

Violation: ESD.CD*



Solution: We reviewed the violations, violations on RDL/PG connections are fixed by increasing width of layers.

Violations inside IP/IO PADS reviewed with designers.

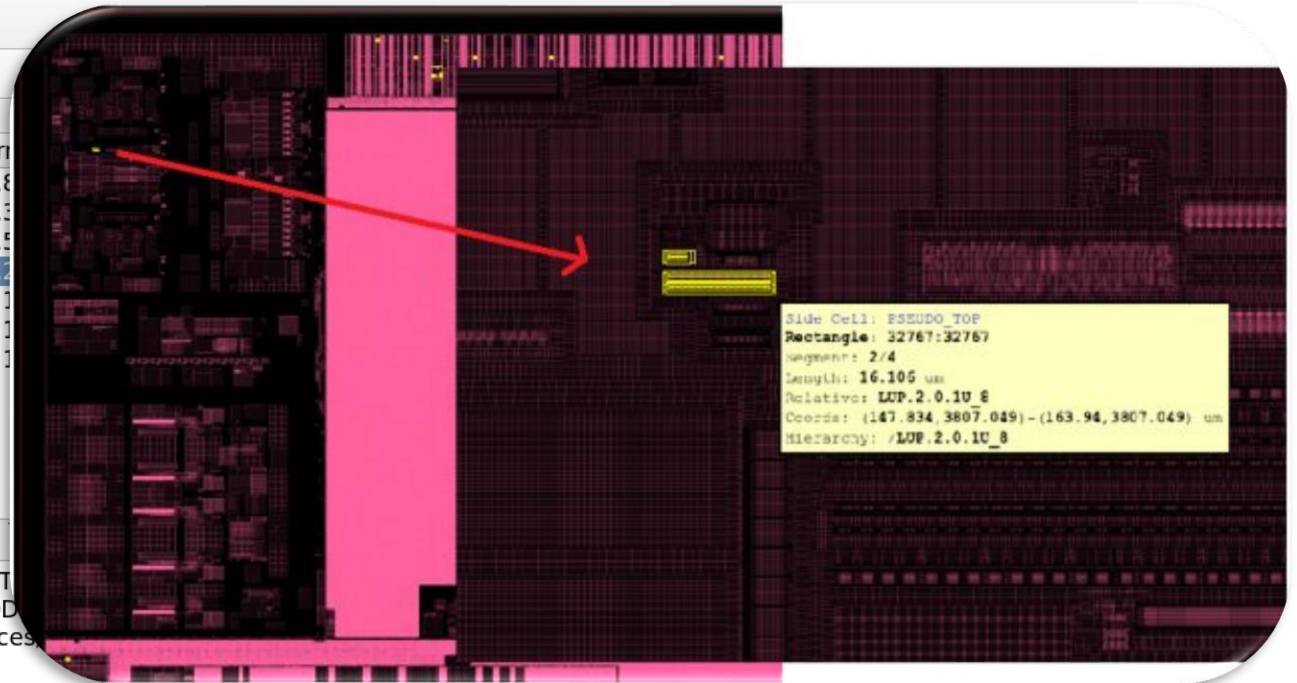
LDL Check

Violation: Latch-up

Issue: LUP.2*U, LUP.1*U, LUP.14* violations reported related to N+/P+ guard-ring and their tied connection to power/ground

Top-cell/Violation/Function	Error	Waive	Total Error
soc	257,679	158	257,837
▶ ESD.CDM.C.2gU	244,381	0	244,381
▶ ESD.CDM.2gU	9,505	0	9,505
▶ LUP.2.0.1U	3,287	0	3,287
▶ LUP.1.0.1U	149	0	149
▶ LUP.14.0.1U	139	0	139
▶ layout_grid_errors:non_45_edge	138	0	138
▶ ESD.43.1gU	28	0	28
▶ ESD.CDM.1gU	22	0	22
▶ LUP.2.1U	21	0	21
▶ ESD.CDM.C.3.2gU	6	0	6
▶ ESD.9.5gU	2	0	2

Violation Detail
LUP.2.0.1U: The N+/P+ guard-ring for LUP.2 should be tied to power/ground accordingly. a. ACT [RWSTRAP OD injector] connect to ultra-low noise signal pin. For the detail of ultra-low noise OD by LUPIEDMY [REDACTED]. It is not recommended to use LUPIEDMY before silicon proven. d. Devices



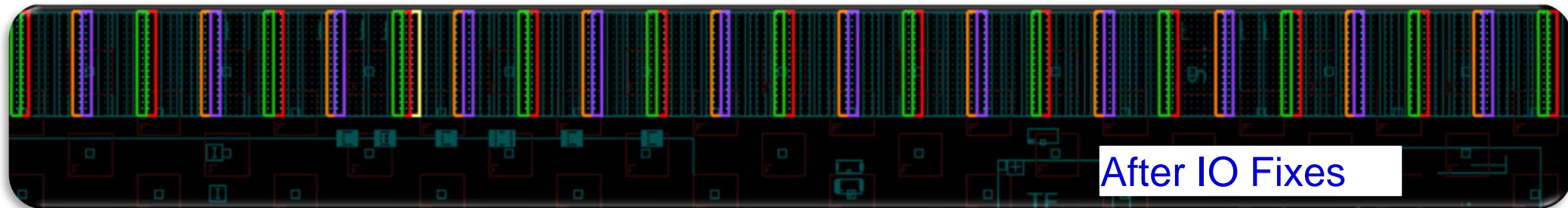
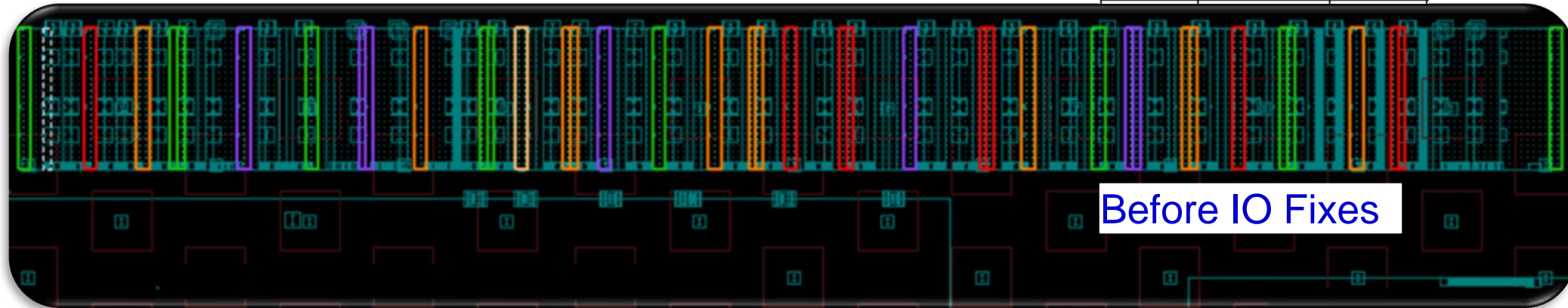
Solution:

- We reviewed violations with design team and vendors.
- Violations which needs Devices/Guard-rings covered by LUP dummy layer are waived.

IO Ring ESD Fixes

IO Ring SSO Ratio/PG IO distribution

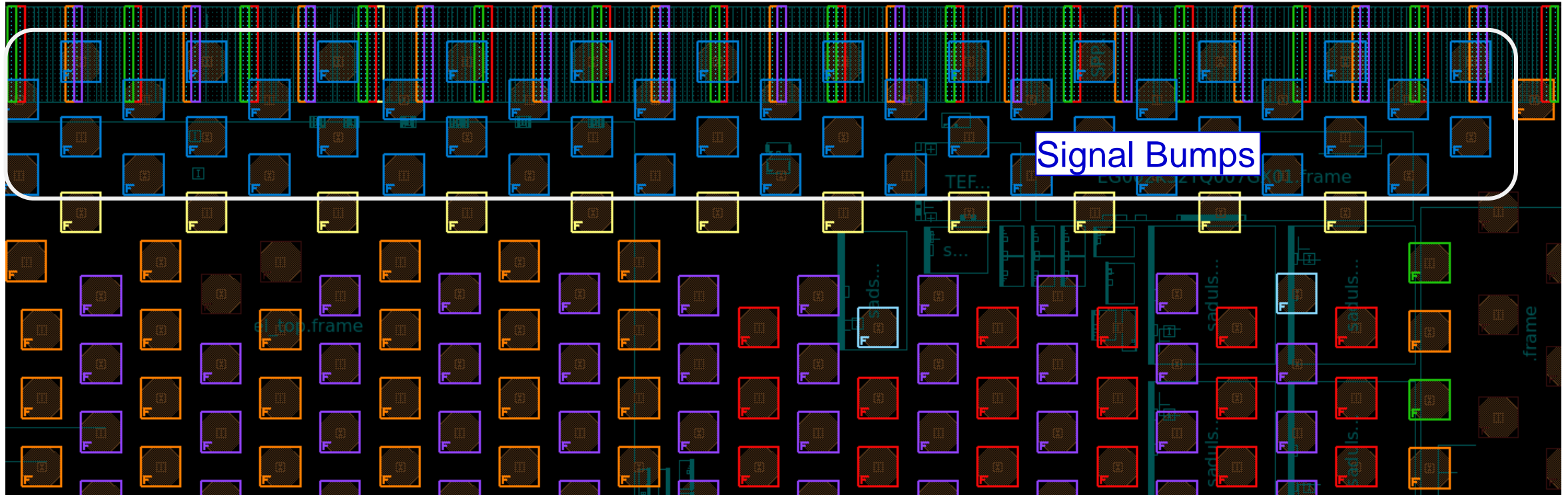
green	VSSIO
purple	VSS
red	VDD
orange	VDDIO



IO Ring ESD Fixes

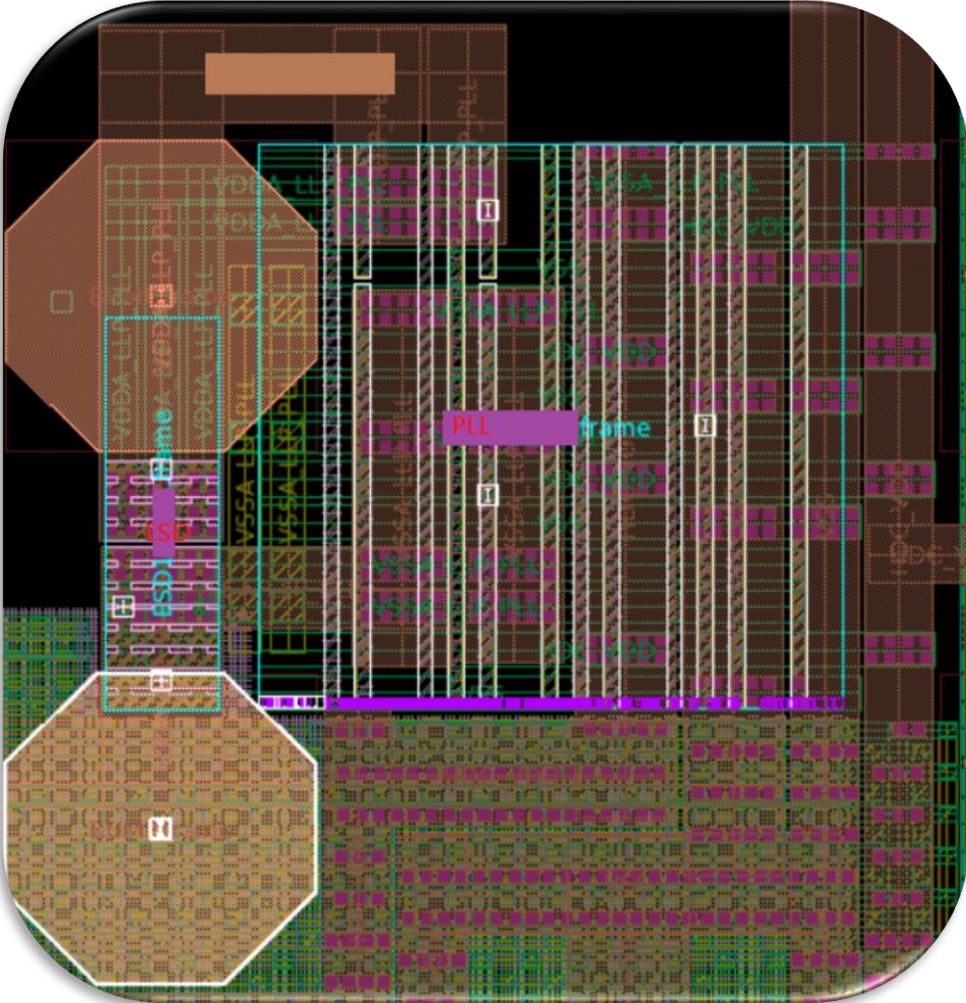
Bump Dept has reduced for Signals

green	VSSIO
purple	VSS
red	VDD
orange	VDDIO



Signal Bumps

IP ESD Fixes



M9 (39)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
VIA9 (59)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
M10 (40)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
VIA10 (60)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
M11 (41)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
VIA11 (61)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
M12 (42)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
RV (85)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			
AP (74)	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>			

ESD, Bump Position and RDL routes for IP (e.g PLL) is important

Other useful reports

- esd_network_report

ICV PERC - ESD Network Report for soc

Summary of Clamp Network

Power	Ground	Clamp Type	Width (um)
AVDD	AVSS15	Single	4027.97
R_VDDIO	R_VSSIO	Single	81789.31
HDC_VDD	VSS	Single	70723.10
CORE_VDD	VSSD	Single	4475.52

Summary of I/O ESD Network

I/O	Power	Ground	Primary Up (Type)	Primary Down (Type)	Secondary Up (Type)	Secondary Down (Type)	Clamp Type	Width (um)
			PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)			Single	12083.90

Summary of Back-To-Back Diode Network

Inter-connected ground net groups	Net pair with back-to-back diode

Summary of Power / Ground / IO Nets

```
# Design Power Net definition(s) -> [HDC_VDD,
# Design Ground Net definition(s) -> [VSSIO,
# Design I/O Net definition(s) -> [
```

- perc_report/perc_configs.txt, pcgroups.txt
- run_details/block.rules : list of executed rules

Run time Details



PERC MODEs	CPU	Run time	Comment
TOPO	8	4 hrs	
LDL	8	3 hrs	Input Mode- Layout
P2P (full path & heatmap)	8	17 hrs	Need more computing resource #define CHECK_FULL_PATH_P2P #define P2P_HEATMAP_ENABLE
P2P (without full path, heatmap)	8	7 hrs	
CD (full path)	8	6 hrs	Need more computing resource "define CHECK_FULL_PATH_CD

P2P runs involving CHECK_PICK_UP_P2P. We use marker layout .gds/oas generated from LDL run.

Conclusion

Conclusion



- ICV PERC reduces the Risk of Costly Failures and Delays
- The ICV PERC Features helped us in SoC ESD reliability signoff are mainly Path HEATMAP visualizer, calculation of resistance contribution by layer, diverse types of detail reports for root cause analysis.
- ICV PERC was significantly important for our soc ESD LUP reliability signoff of our 7nm designs as it checked issues of designs which is not checked with signoff DRC check

Acknowledgement



- We thank "Akhil, Bhavani & Soumyajit " from Synopsys team for valuable support.
- We thank "Sachin Bastimane" from Broadcom.

References

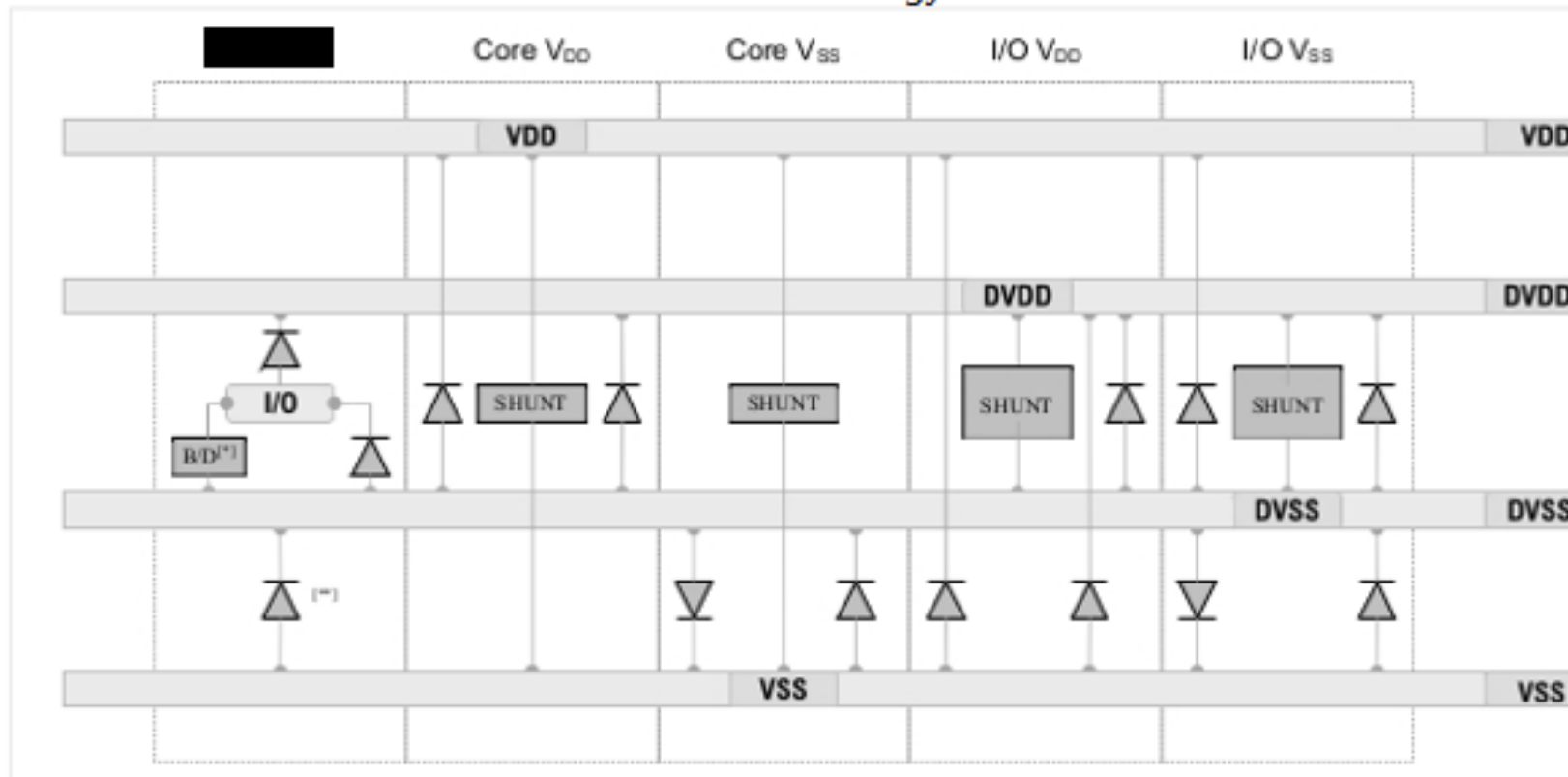
- <https://solvnet.synopsys.com/>
- ICV PERC / IC Validator User Guide
- TSMC 7nm Design Rule Manual
- Synopsys document on ICV PERC

THANK YOU

Our
Technology,
Your
Innovation™

IO Ring ESD Fixes

Generic Power PADS ESD Strategy



Other useful reports

perc_report/perc_configs.txt

*** User defined Config ***

Switch	value
LVS_RUNSET	<code>_ESD_LU/NEW_SETUP/1P12M_1X1Xa1Ya4Y2Yy2R/DFM_LV S_RC_ICV_N7_1p12M_1X1Xa1Ya4Y2Yy2R_ALRDL.1.2b.p erc</code>
NXTGRD_FILE	<code>_ESD_LU/NEW_SETUP/cln7_1p12m_1x1xalya4y2yy2r_m im_ut-alrdl_typical.nxtgrd</code>
CD_PRE_CHECK	False
CHECK_FULL_PATH_P2P	True
CHECK_PICK_UP_P2P	True
DISABLE_IDOMY	False
DISABLE_PG_SANITY_CHECK	False
DISABLE_XDOMAIN_ALL	True
ENABLE_R0_CHECK	TRUE
EXPORT_ONE_VICTIM	False
GROUP_PWR_CLAMP	0
Hi_CDM	True
INPUT_MODE	LAYOUT_MODE
INT_PWR_LIMIT	10000
LAYOUT_FORMAT	OASIS
LDL	False
METAL_STACK	1P12M_1X1Xa1Ya4Y2Yy2R
NETLIST_FORMAT	SPICE
P2P_HEATMAP_ENABLE	True
P2P_PRE_CHECK	False
PC_GROUP_DISTANCE	5
PC_GROUP_FILTER	100
PC_GROUP_WIDTH	2000
REF_OBJ_COUNT	5
TOPO	False
USER_STARRC_OPTIONS	starrc_options_p2p_a.txt
P2P	True

/perc_reports/*

```
perc_configs.txt
pcgroups.txt
esd_network_report.txt
esd_network_report.html
p2p_topo_violation.txt
p2p_results.xls
p2p_results.txt
p2p_results.html
```

Other useful reports



perc_report/pcgroups.txt

```
-----  
POWER CLAMP GROUP: RC_CORE_VDD (Power) -> RC_VSSD (Ground)  
  
RC_CORE_VDD  
  
    PCGroup_172 (width=2237.760000; x=610.000000; y=2490.000000; device count=4320, [nch_svt_mac]) [nmos]  
    PCGroup_173 (width=2237.760000; x=690.000000; y=2830.000000; device count=4320, [nch_svt_mac]) [nmos]  
  
RC_VSSD  
-----  
POWER CLAMP GROUP: VDDIO_A (Power) -> VSS (Ground)  
  
VDDIO_A  
  
    PCGroup_90 (width=2033.982000; x=920.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_91 (width=2033.982000; x=1080.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_92 (width=2033.982000; x=1125.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_93 (width=2033.982000; x=1235.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_94 (width=2033.982000; x=1305.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_95 (width=2033.982000; x=1380.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_96 (width=2033.982000; x=1450.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_97 (width=2033.982000; x=1540.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_98 (width=2033.982000; x=1585.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_99 (width=2033.982000; x=1650.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_100 (width=2033.982000; x=1770.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_101 (width=2033.982000; x=1845.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_102 (width=2033.982000; x=2000.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_103 (width=2033.982000; x=2060.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_104 (width=2033.982000; x=2265.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_105 (width=2033.982000; x=2360.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_106 (width=2033.982000; x=2460.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_107 (width=2033.982000; x=2595.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]  
    PCGroup_108 (width=2033.982000; x=2705.000000; y=4090.000000; device count=3519, [nch_18_mac]) [nmos]
```

Sample run esd check command

```

bsub -q [redacted] -n 20 -R "select [type == local] rusage[mem=500000]" icv esd_setup.rs -host_init 20 \
-D LVS_RUNSET=[redacted] 1P12M_[redacted]/DFM_LVS_RC_ICV_N7_1p12M_1X1)
1Ya4Y2Yy2R_ALRDL.1.2b.perc \
-D NXTGRD_FILE=[redacted] cln7_1p12m_[redacted]_mim_ut-alrdl_typical.r
tgrd \
-I [redacted]/1P12M_1X1Xa1Ya4Y2Yy2R/runset \
-vue -ex
## NOTE:
# This is a simple setting.

```