3D die disaggregation construction & convergence

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Acknowledgment

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Agenda

- IC Evolution
- 3D design planning & convergence
- Results
- Future Scope

IC Evolution

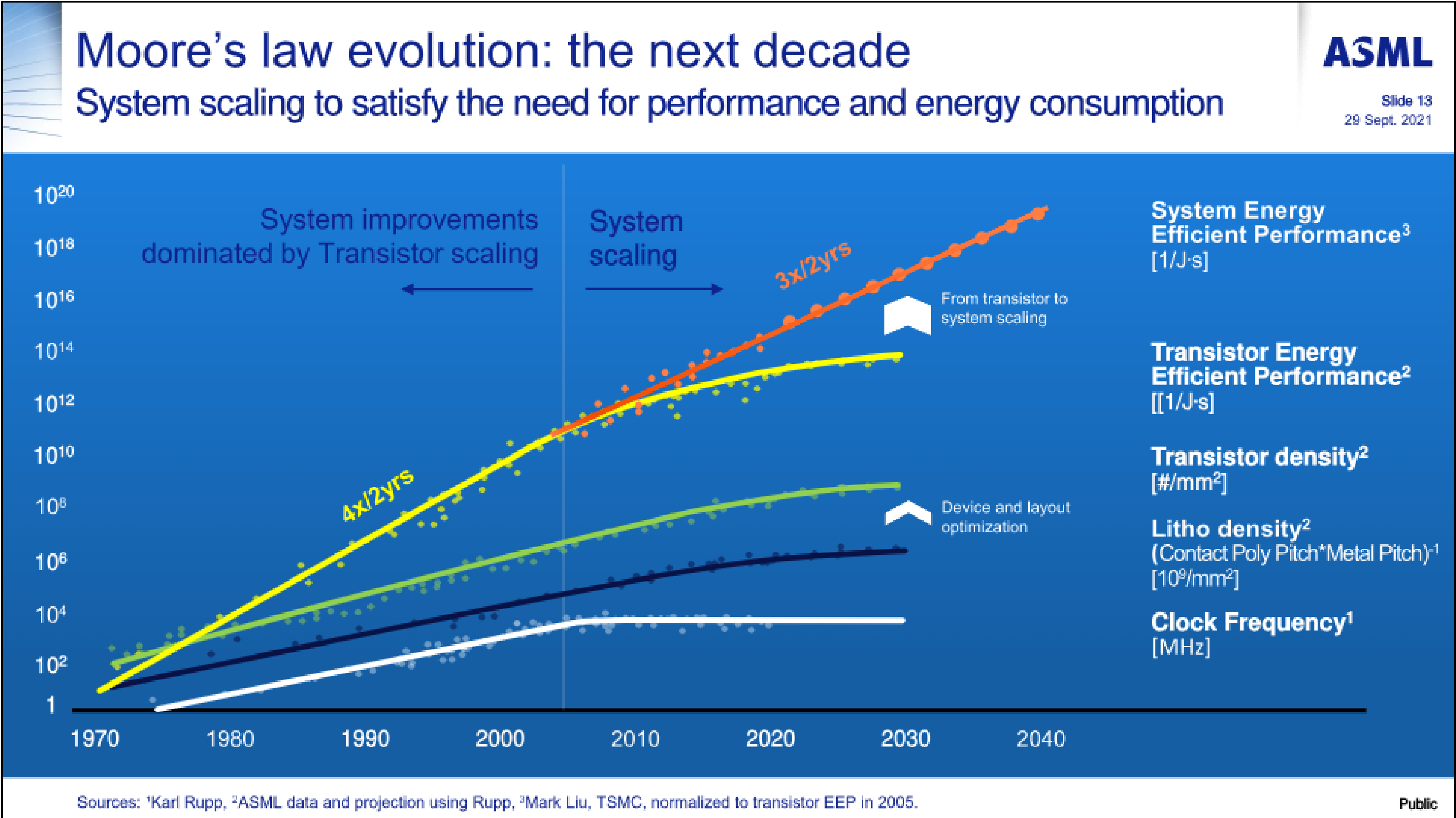
Moore's Law

IC Evolution

Moore's Law

"Number of transistors in an integrated circuit (IC) doubles about every two years"

- Moore's Law



Architecture Evolution

Past-Present-Future

- **1980** — **Intel 386**: Design with schematics/ Sea of gates/transistors
- **1990** — **Pentium**: Design with HDL/Sea of cells/blocks
- **2005** — **Core Duo**: Design with functional IP
- **2013** — **Hasswell**: Design with 2D chiplets
- **2017** — **KabyLake**: 2D chiplets & 2.5D
- **2019** — **Lakefield**: 3D logic on Logic stacking
- **2022** — **Ponte Vecchio**: 2D + 3D Large design
- **FUTURE**
  - **Scalable Architecture**
  - **More disaggregation**
  - **Mix-n-Match (Heterogeneous Integration)**
  - **Flexible across process nodes**

2D+3D disaggregation is the way forward

IC Evolution - needs

<u>Monolithic</u>
Function
Timing
Power

<u>2D MCP</u>
Functional
Timing
Power
IP planning wrt PKG

<u>2.5D Disaggregation</u>
Functional
Timing
Power
PKG Reliability
Interface die planning
PPA impacts

<u>2.5D + 3D</u>
System-level design planning
Functional
Timing
Power
PKG Reliability
Thermal
Mechanical
PPA impacts

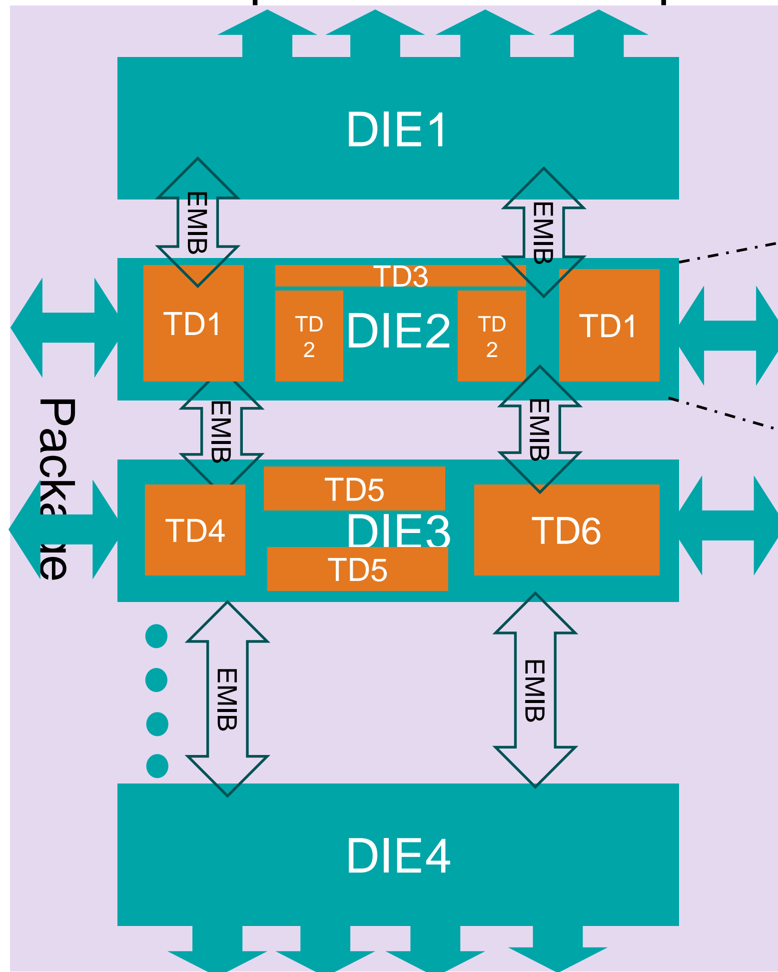
3D chip design must account for numerous factors, especially different multi-physics elements

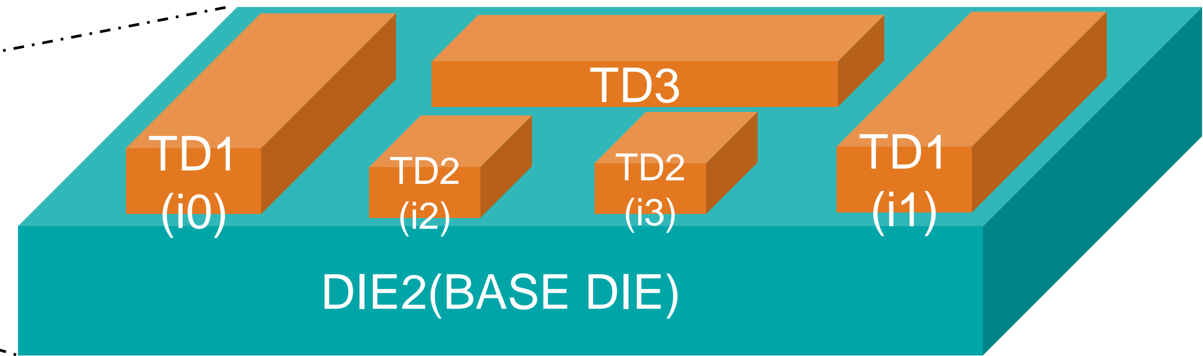
3D design planning & convergence

System level perspective

3D design planning

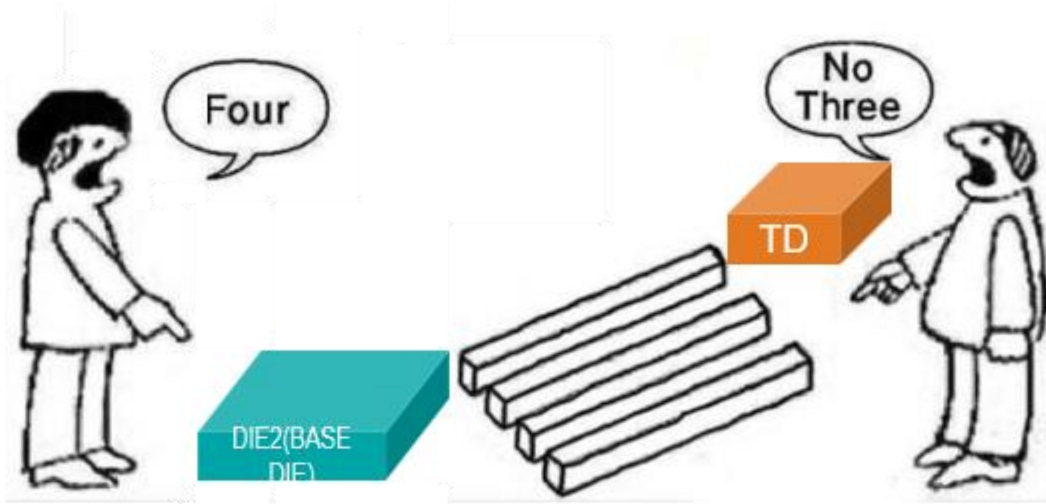
*This is representative floorplan where we used 3DIC tool for overall design convergence





Can we integrate all individually planned dies

System planning



Plan the die separately and integrate

Top-down planning

- Helps to plan system connectivity
  - Through die connections
- Die Alignments
- Interface optimization

Co-designing is the key for convergence

3D design planning

sequences

- 3D System creation
- Bump Management
- 3D floorplan checks
- 3D early construction checks
- 3D signoff collateral generation
- Overall System convergence**

** Beyond the scope of this presentation

3D design planning

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- Collaterals for signoff
- System convergence

3D System creation

- System level netlist/RTL creation no longer front-end only activity.
  - It needs to see how connections will be made in backend and create then connectivity accordingly.
  - Different categories of connections must be considered.
    - Category 1 : Package I/O direct connections to Top die
    - Category 2a : Package I/O connects to Base die but also has micro bump connections
    - Category 2b : Top die connections only to micro bumps
    - Category 3: Package I/O connects to Base die only.
    - Category 4 : signal connections between top & base dies
    - Category 5 (P/G) : connections to all dies

3D System Creation

System collaterals
- RTL
- UPF

PDK

Build Individual dies
- Read RTL
- Read UPF
- Read boundaries
- Read bump plan (if exists or mirror later)
- Signal routing
- Checkers & collaterals

<die>.ndm

PDK

Build 3D System
- Read RTL
- Read UPF
- Read floorplan
- Plan cross die bumps
- Plan Cross die routings
- Checkers & collaterals

Collaterals for signoff

3D design planning

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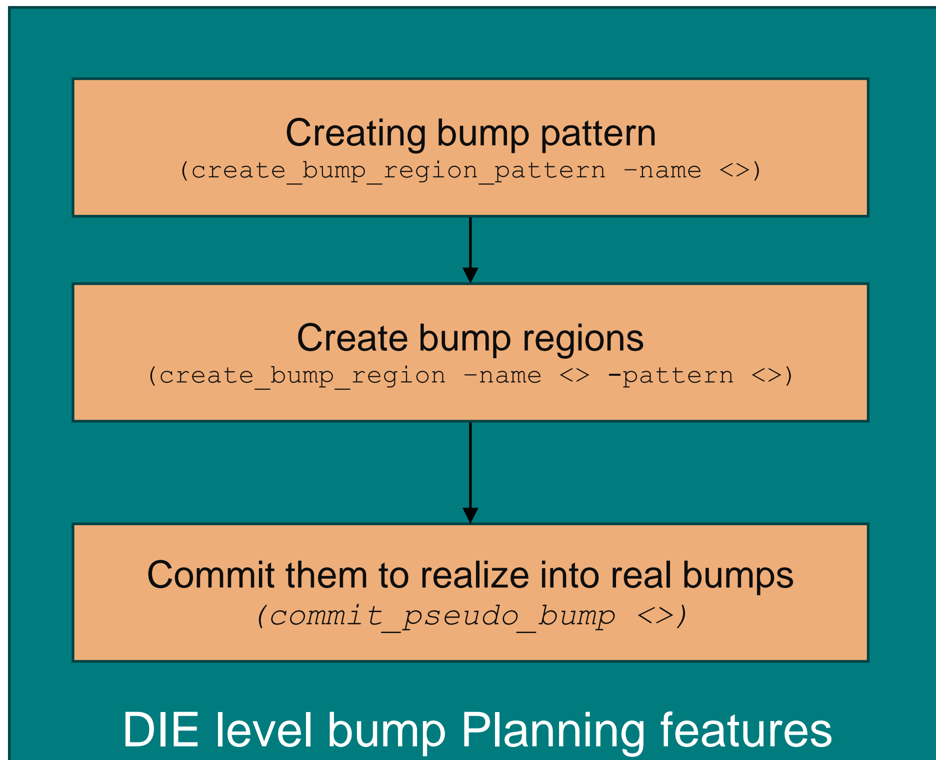
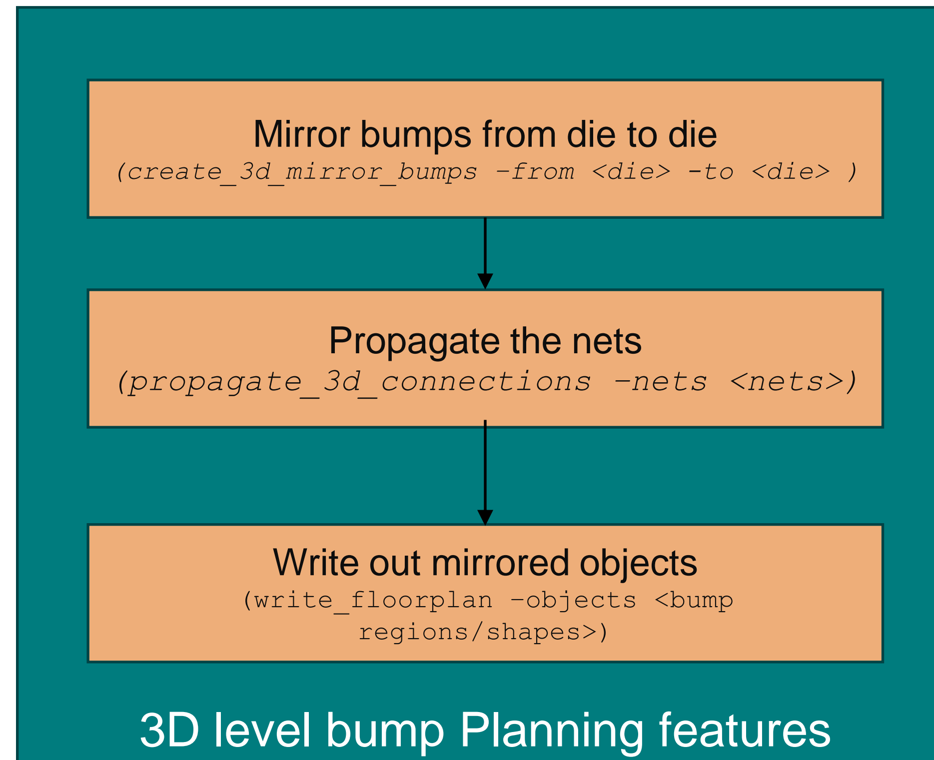
BUMP Management

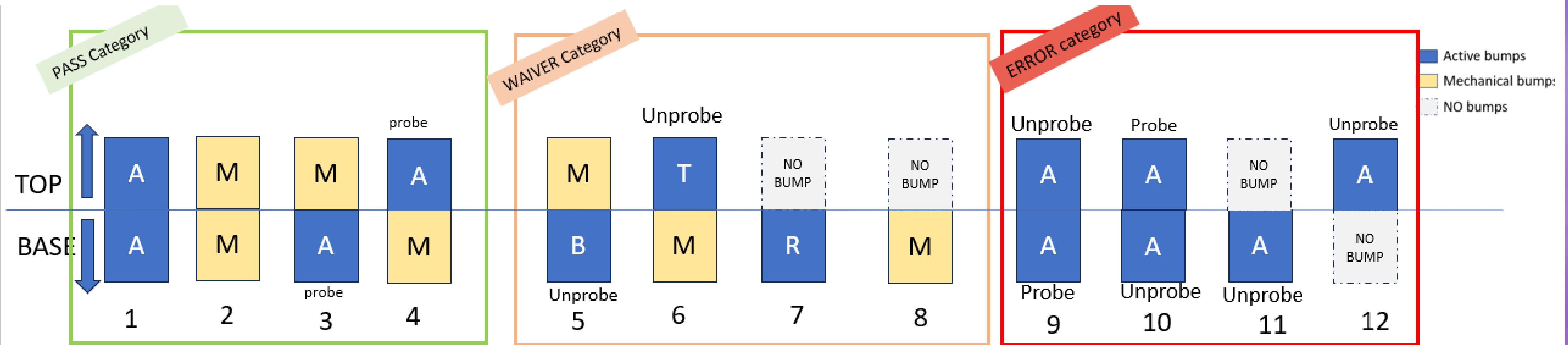
- Bump planning is carried out during individual die construction using fusion compiler tool native “pseudo bump methodology”
- Main challenges we faced for 3d IC are
  - Bump mirroring
  - Capacity handling
  - Handshaking across different hierarchies.





BUMP alignments

- We used 3d IC shell tool native command *check_3d_design* exclusively to catch all alignment issues
- The following different combinations were verified



A → Logical connection exists between both BASE die(MPH bump) and TOP(BPH bump) die
M → Mechanical(dummy) bumps
B → Logical port/net only exists in BASE die and no business with TOP die ; but due to sort bringing in MPH bumps
T → Logical port/net only exists in TOP die and no business with BASE die ; but due to sort bringing in BPH bumps
R/R1/R2 → Some connection only exists in BASE die but DUMMY dies exists on top.
NO BUMP → No bump exists as DUMMY die is placed.

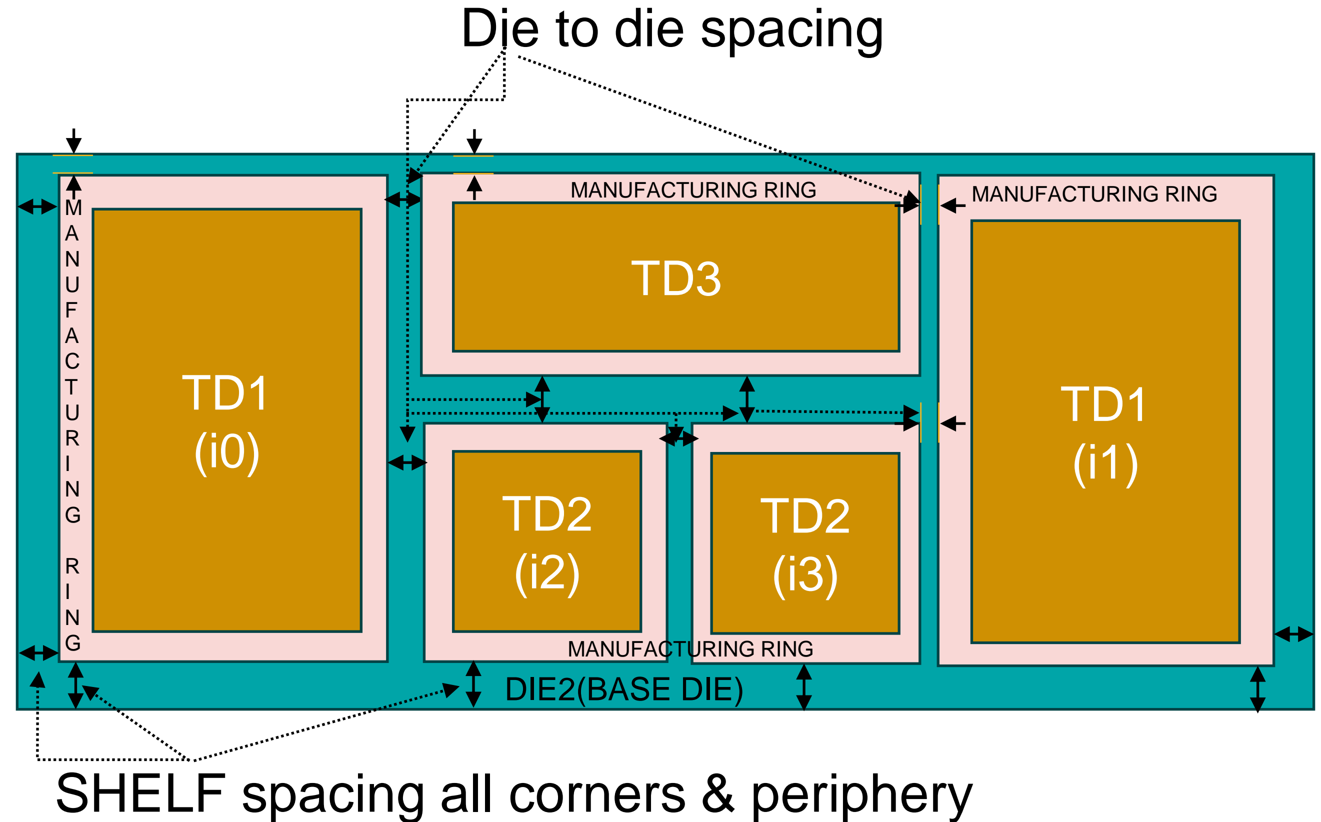
3D design planning

sequences

- 3D System creation
- Bump Management
- **3D floorplan checks**
- 3D early construction checks
- Collaterals for signoff
- System convergence

3D floorplan checks

- Created “seal ring” for manufacturing objects
  - 3D checks are based on physical die sizes which includes sealring.
  - `create_manufacturing_shapes <>`
    - `Ex : create_manufacturing_shape -name sealring -boundary <> -type seal_ring`
- DIE to DIE & SHELF design rules are verifying with utility procedures using “sealring” objects.
  - Utility 1 : `die_2_die_rules_check (TOP die to TOP die spacing checks)`
  - Utility 2 : `die_2_shelf_design_check (Base die edge to top die edge enclosure)`



3D design planning

sequences

- 3D System creation
- Bump Management
- 3D floorplan checks
- **3D early construction checks**
- Collaterals for signoff
- System convergence

3D early construction checks

Individual DIE level

```
check_shorts
check_opens
check_port_missing_terminals
check_for_collaterals
check_mv_design
```

3D level

```
Check_3d_design -physical
Check_3d_design -logical
collaterals for 3D signoff(extraction, vclp, fev, LV)
Collaterals for 3D PDN analysis(config file generation)
Check for port attributes
```

These checks helped system level early convergence, thus stabilizing individual dies floorplan

snug

Results

Advantages of TOPs-DOWN approach

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- Helps in managing the work independently, in parallel with each dies.
  - No bottom-up dependency.
- Complete system level connectivity information which helps in early sign-off.
- Faster convergence as design data is available from DAY-1 vs late data availability in bottom-up approach.
- Dirty data can be handled easily.
- Since results are in-design, quicker feedback loop possible.

Runtime - 3DIC bump planning feature

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Many issues got fixed throughout the project, in terms of

- Corner case bug fixes for committing pseudo bumps
- Corner case bug fixes for generating “floorplan.tcl”
- Addressed run time challenges.

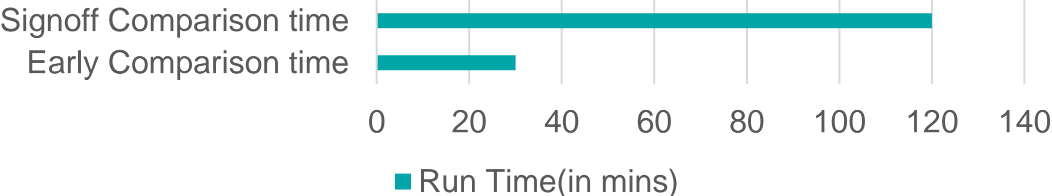
Total Bumps (~8M)

	Bump regions	No. of bumps	Consumption runtime (without 3DIC bump planning feature)	Consumption runtime (with 3DIC bump planning feature)
Base die backside	452	~40K	45mins	15mins
Base die front side	2592	>4M	30hrs	1hr
Top dies backside	167	>350K	2 hrs	10mins

	Manual creation (~time)	With Mirroring feature
Top die side bumps creation	manual creation is iterative and ~takes a day’s time	Within < 1 hr

Early checks – Comparison metrics

	3D construction early results	Signoff results (3D LV result with bottom up .oasis of individual dies)	Comments
3D LVS results	MATCH	MATCH	All logical connections were caught early on
3D bump alignments	~81% coverage	100% (Gold standard)	Probe bumps vs non-probe bumps are not understood by the tool
Marker cell alignment	NOT Covered	Covered	No alignment checks at present. future request
Short checks	Covered	Covered	This helped to fix all shorts early on.
Die spacing	Covered (though utility)	Covered	Future request : Native command request
runset dependency	NO	YES	In-design comparison is simpler



Simple, quick & easy to run (in-design) comparison

Future Scope

Future Scope

Capacity handling

1. Push-down(/pop-up) of bumps
2. collateral generation
3. collateral consumption
4. attributes setting
5. Checkers

all features of 3D planning

Floorplan improvements

1. Category-wise error GUI for faster analysis/debug
2. Mirroring of routes

In-design validation improvements

1. Die to die validation
2. Fix all false violations
3. check-3d-design to include all 2D pin verification options

Multi-physics

1. Indesign PDN
2. Indesign themal/stress
3. Design space exploration with multi-physics

Etc.

Co-design

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THANK YOU

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BackUp

3D LVS results

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- LVS comparison using blackbox & whitebox approaches, for covering TSV connections
- Below are category-wise results.

Marker cell mis alignment,	
Type of violation	Viol count
topdie_0	2
topdie_1	2

#SL No	Rule
1	dummy with real bump pair not allowed
2	Missing bump pair not allowed
3	Probe paired with active bump not allowed
4	Center to center alignment misses for bumps
5	marker/alignment cell pair alignment

Category 5 : Mechanical bumps in top die paired with unprobed bumps in base die : basedie specific supply bumps are present in base die on these dummy bump locations	
violation	Viol count
topdie 0	5514
topdie 1	5530

Category 6 : Mechanical bumps in base die paired with unprobed bumps in top die : top die only supply bumps are present in top die on these dummy bump locations	
violation	Viol count
topdie 0	5215
topdie 1	5224

Category 9 : unprobe bumps in base die paired with probed bumps in top die :	
violation	Viol count
topdie_0	8443
topdie_1	8436

Category 10: unprobed/dummy bumps in top die paired with probed bumps in base die :	
violation	Viol count
topdie_0	4071
topdie_1	4064

P/G connections in 3D