Comprehensive Verification and Performance Analysis of HBM3 Memory Subsystem

Ankitkumar Patel - Annapurna Labs (AWS)
Co-authored by Gaurav Chugh & Heena Mathur - Synopsys

Agenda

- Objectives
- HBM3 (High Bandwidth Memory) Subsystem Architecture
- Verification Requirements
- Memory Subsystem Performance Analysis
- Conclusion

Objectives

Objectives

- Comprehensive Verification of HBM3 Memory Subsystem
- Signoff with different JEDEC and Memory Vendor Configurations
- Performance Analysis sign off
- Coverage Closure

HBM3 Subsystem Architecture

HBM3 Subsystem Architecture

- 16 Channels – 32 Pseudo Channel
- DRAM Capacity

  4/8/16/24/32/64 GB
- Different Data Rates

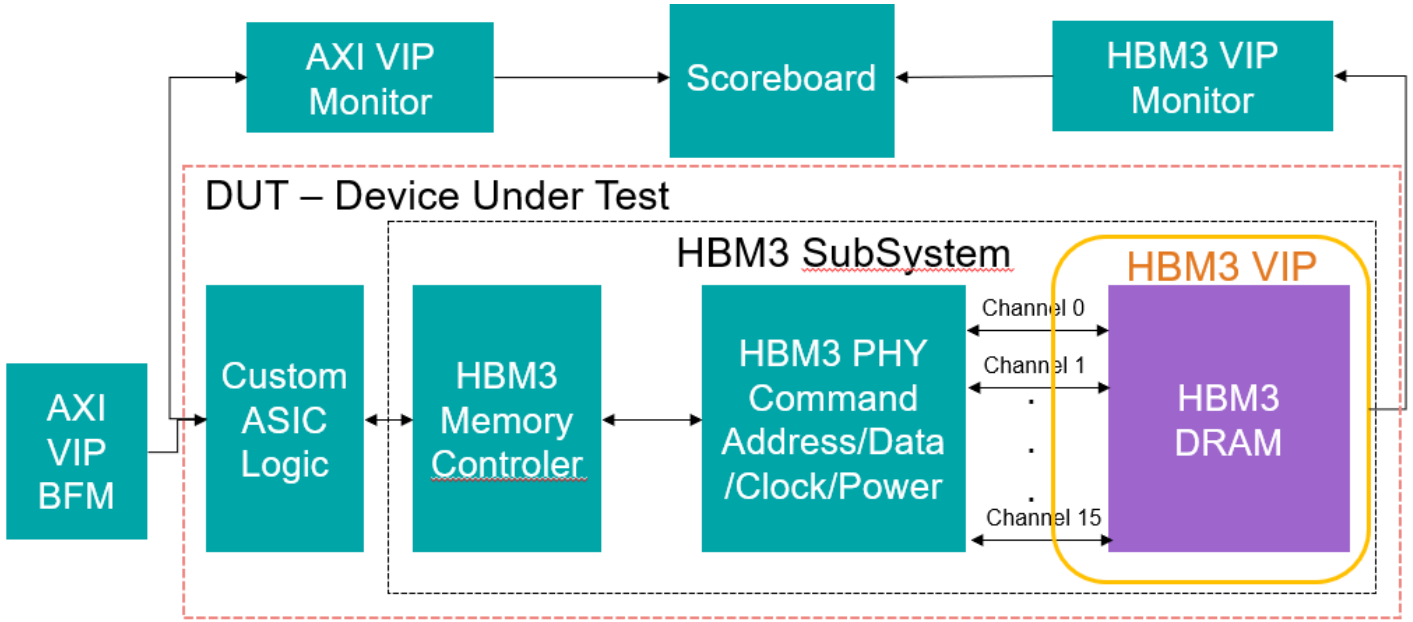
  4800Mbps, 5600Mbps & 6400Mbps
- BW Requirement

  25.6GBps
- HBM3 Key Features

  Training (DWORD, CA & Periodic Phase)

  IEEE Repairs

  Bank Group & Refresh Management
- End-to-End Data integrity check between AXI Interface & HBM3 DRAM Interface
- Protocol Compliance Checks at AXI & HBM3 Interface with AXI & HBM3 VIP Monitor
- HBM3 & AXI VIP – Synopsys



Verification Requirements

Verification Requirements

Requirements	Solutions
Scalability from subsystem to SoC	• Reuse SV & UVM Env at SoC testbench
Scalability from HBM3 to next generation of HBM	• HBM3 VIP Supports backward compatibility as well as future generation of HBM without need of testbench changes
Configurability for different JEDEC & memory vendor datasheets	• HBM3 VIP supports Different Vendor Catalog load during run time without need for recompilation or TB changes
Robust set of protocol & timing checks	• Leverage exhaustive protocol and timing checks from HBM3 VIP
Hooks for analyzing performance data at HBM3 Interface	• Leverage HBM3 VIP Performance Metrices (Bandwidth, Page hit/miss, Irregular page accesses, Unoptimized command spacing) • Used HBM3 VIP callbacks to implement Custom Performance Monitor for monitoring custom workload traffic

Verification Requirements

Requirements	Solutions
Error injection capability to test end to end Interrupt flow	• 1 or 2 bit ECC Error, Sev error, etc
Simulation speed-up requirements	• Bypass Training • Backdoor Mode Register Settings
End-to-end data integrity between AXI Interface to HBM3 Interface	• Custom scoreboard implemented by leveraging Synopsys AXI & HBM3 VIP callbacks
Coverage model for verification signoff	• Leverage HBM3 VIP comprehensive coverage model
Gate-level simulation	• HBM Subsystem - DW & CA training with Write & Read Traffic
Ease of debug capabilities	• Transaction log, Synopsys Verdi® Protocol Analyzer, Debug Ports, Error Message • Backdoor HBM3 DRAM initialization with known/random value

Memory Subsystem Performance Analysis

Memory Subsystem Performance Analysis

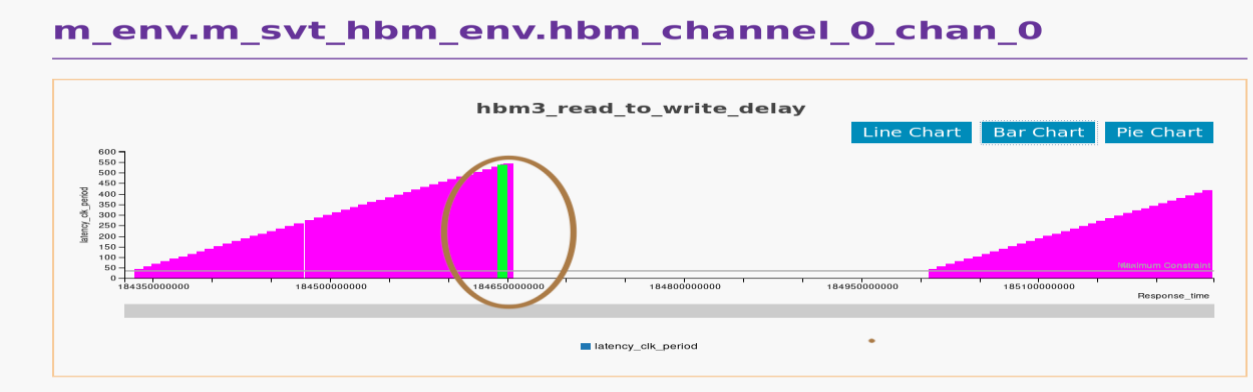
- Different Traffic Pattern Analysis
  - Write only/Read Only/Write-Read Mix
  - Sequential Address Access
  - Random Address Access
- Identify Unnecessary bubbles on Command & Data Interface
  - HBM Controller/HBM PHY/Custom Wrapper logic
  - With large number of write-read transaction flowing through HBM3 DRAM.
  - For different row & column commands to identify any bubbles (Idle Cycle) inside HBM Subsystem
  - Page open/close policy
- Root Cause analysis of performance Bottlenecks
  - Review row & column commands from performance analyzer to identify throughput bottlenecks

Memory Subsystem Performance Analysis

- Key Performance Matrices to achieve HBM subsystem performance throughput goals
  - Bandwidth
  - Page hit/miss ratios
  - Irregular page accesses
  - Unoptimized command spacing
  - Read-Write grouping
- Developed custom performance monitor based on HBM3 VIP callbacks
  - Transaction_started & Transaction_ended to extract custom throughput requirements for different traffic workloads.
- Auto Test Pass/Fail status based on throughput goal requirements for different traffic pattern

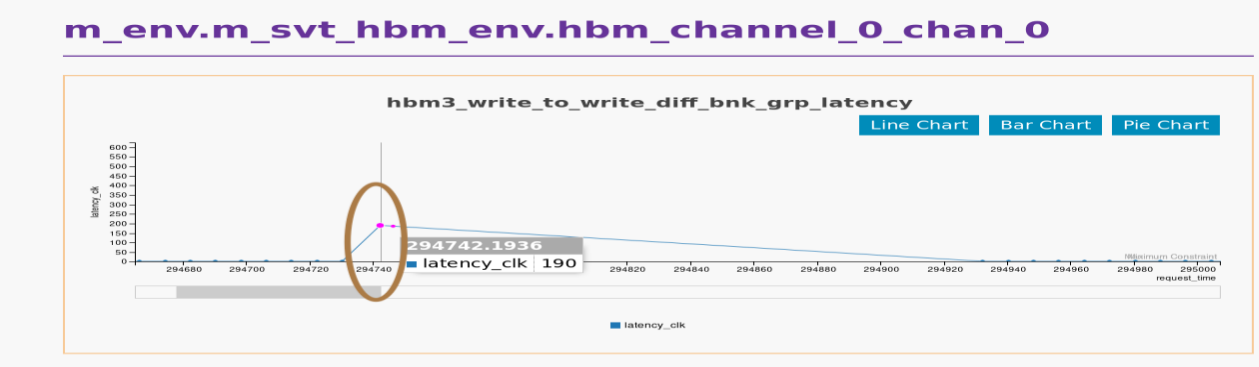
Memory Subsystem Performance Analysis

- Performance Analyzer helps to identify any gaps between read to write switching



latency_clk_period	sponse_tir	spec_value_clk	name
498	...121000	35.11	trtw
50	...121000	35.11	trtw
50	...621000	35.11	trtw
502	...621000	35.11	trtw
506	...121000	35.11	trtw
510	...621000	35.11	trtw
514	...121000	35.11	trtw
518	...621000	35.11	trtw
522	...121000	35.11	trtw
526	...621000	35.11	trtw
530	...121000	35.11	trtw
534	...621000	35.11	trtw
538	...121000	35.11	trtw
54	...621000	35.11	trtw
54	...121000	35.11	trtw
542	...621000	35.11	trtw
546	...121000	35.11	trtw
58	...121000	35.11	trtw
58	...621000	35.11	trtw
62	...621000	35.11	trtw
62	...121000	35.11	trtw
66	...121000	35.11	trtw
66	...371000	35.11	trtw
66	...621000	35.11	trtw

- Identify gap between write to write for different bank group latency



latency_clk	equest_tim	sponse_tir	spec_value_clk	name
566	...442.19	...121000	2	tccds
190	...742.19	...621000	2	tccds
186	...746.19	...621000	2	tccds
182	...750.19	...621000	2	tccds
10	...616.19	...371000	2	tccds
6	...620.19	...371000	2	tccds
2	...624.19	...371000	2	tccds
2	...626.19	...621000	2	tccds
2	...628.19	...871000	2	tccds
2	...630.19	...121000	2	tccds
2	...632.19	...371000	2	tccds
2	...634.19	...621000	2	tccds
2	...636.19	...871000	2	tccds
2	...638.19	...121000	2	tccds
2	...640.19	...371000	2	tccds
2	...642.19	...621000	2	tccds
2	...644.19	...871000	2	tccds
2	...646.19	...121000	2	tccds
2	...648.19	...371000	2	tccds
2	...650.19	...621000	2	tccds
2	...652.19	...871000	2	tccds
2	...654.19	...121000	2	tccds
2	...656.19	...371000	2	tccds
2	...658.19	...621000	2	tccds

Conclusion

Conclusion

- Deliver high quality HBM Memory subsystem RTL to SoC
- Meet desired throughout goals for different traffic workloads
- Exercise HBM Memory subsystem for different Transaction sizes & Address alignments
- HBM Memory subsystem RTL meet JEDEC & Vendor Timing and Protocol compliance
- Meet HBM3 Coverage requirements

HBM3 Subsystem Requirements

- 16 Channels – 32 Pseudo Channel
- DRAM Capacity
  - 4/8/16/24/32/64 GB
- Different Data Rates
  - 4800Mbps, 5600Mbps & 6400Mbps
- BW Requirement
  - 25.6GBps
- HBM3 Key Features
  - Training (DWORD, CA & Periodic Phase)
  - IEEE Repairs
  - Bank Group & Refresh Management
- End to End Data integrity check between AXI Interface & HBM3 DRAM Interface
- Protocol Compliance Checks at AXI & HBM3 Interface with AXI & HBM3 VIP Monitor

Synopsys HBM3 Verification IP helped us close all our signoff criteria


THANK YOU
YOUR
INNOVATION
YOUR
COMMUNITY