

Next-Generation Verdi: Overview of New Debug and Verification Management

Myles Glisson Synopsys

SNUG SILICON VALLEY 2024

2

Agenda

- Motivation and Debug Flow
- Synopsys Verdi
 Verification Management System
- Refreshed Verdi Graphical User Interface (GUI)
- Verdi Integrated Design Environment (IDE)
- AI-Based Regression Binning
- AI-Based Bug Prediction
- Root Cause Analysis Components
- AI-Based Message Analysis
- Debug Decision Tree
- Summary + Q&A



SYNOPSYS

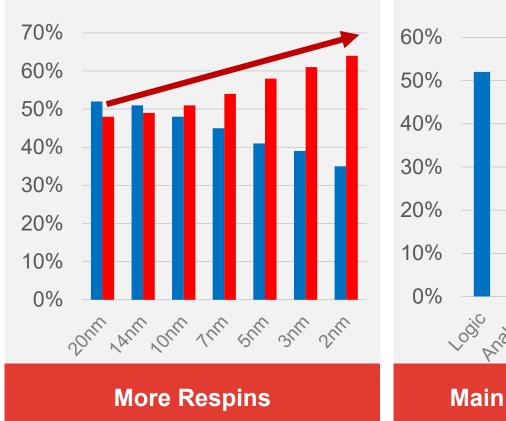


Motivation and Debug Flow

Impact on Right First-Time Silicon

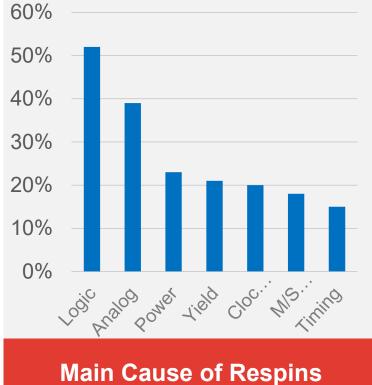




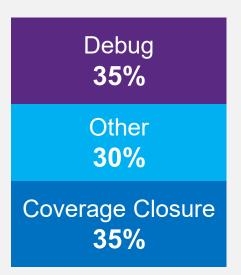


Fewer First-Time Right

Logic Bugs Dominating

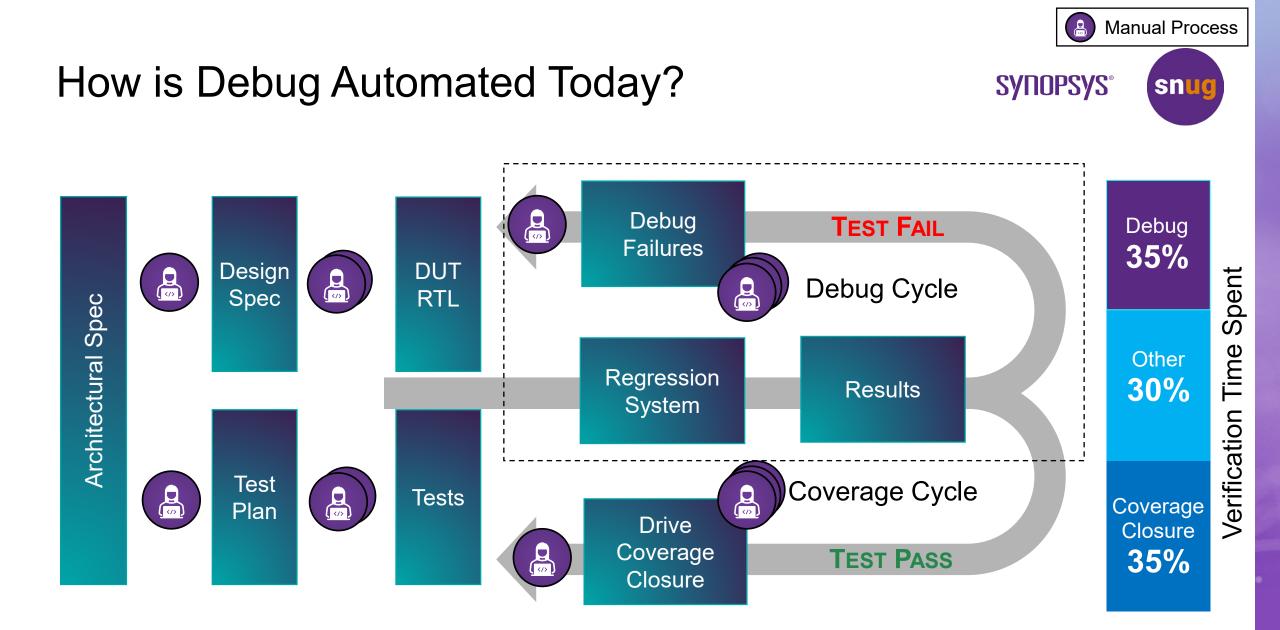


Verification Time Spent



Need to Reduce Debug Time!

Source: Wilson Report 2022

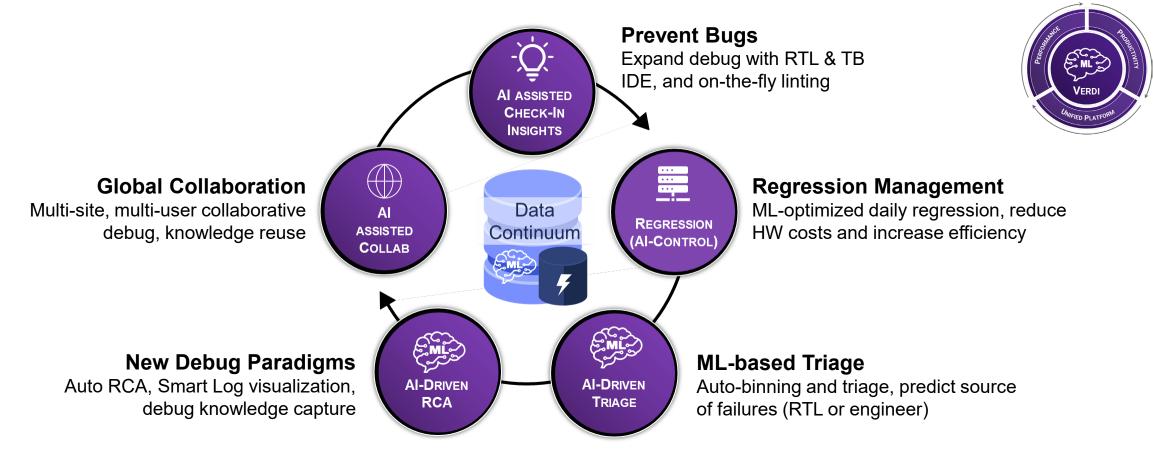


AI-Assisted Debug Flow

SYNOPSYS° sn



Next-Generation Debug: Improves debug productivity up to 10X



ML-Based, Automated Regression Debug **SYNOPSYS**[®] snug Verdi Failure Probe sim Coverage Code Regression Planner Test Runner check-in Aggregator Re-run Re-run **VMS** Failing Passing Ref snapshot* tests tests **RCA Manager** DUT Risk XRCA \cap RCA \triangleright Ranking Verdi Report Binning **Debug Facilitator** Clusters Smart Log/Msg **TB RCA** Probe Analysis Engines GUI Bucketized reg • Bug prediction, Engines root • GUI complements failures code change that cause the bugs (if the engines caused failures ref snapshot • RCA Manager & Representative Report for review exists) cases

7

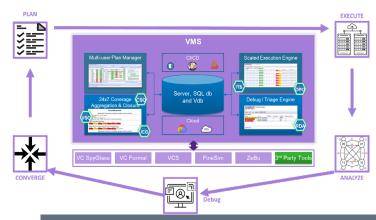


Verdi Verification Management System

Verification Management System

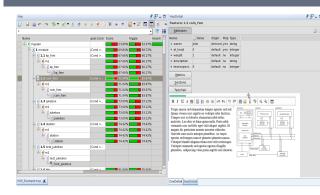


Manager and Dashboard



Test planning, execution & debug, coverage merge and annotation

 Enables verification data-over-time to be mined for analytics

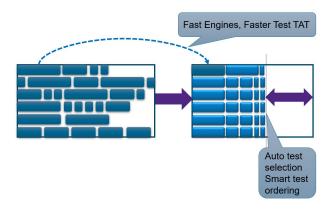


Planner

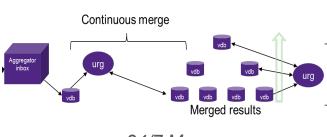
Coverage

- Multi-user test
 scheduling/planning
- Supports change history and restore
- API for automated report generation and updates

Runner



- Runs regressions
- Order tests to eliminate long tail
- Synopsys VCS® engine performance enhancement



24/7 Merge

- Continuously merges
 incoming coverage
- Integrated tagged VDB from ad hoc regression runs
- Can generate moving window merge VDB



Refreshed Verdi Graphical User Interface (GUI)



Modern design style for comfortable view

- 4 color themes and better color system
- Flat icon design
- Consistent fonts
- Provide Bright/ Dark/ Classic modes

Intuitive tools access

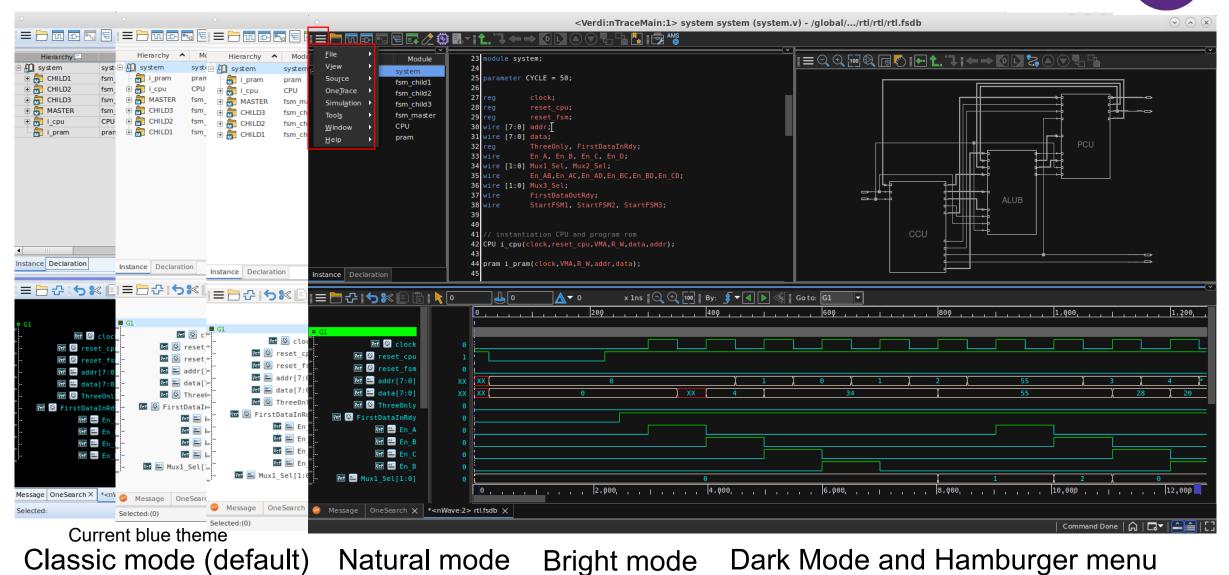
- Hamburger menu
- App launcher
- Maximized debug spacing with Auto 'hide'

Updated search and find

- Efficiently find targets with new search pane
- Unified search for string/signal/command
- Dedicated floating find bar in each window

Don't worry! - Menu commands remain in the same location

Classic Mode Color Theme



SYNOPSYS[®]

Snu



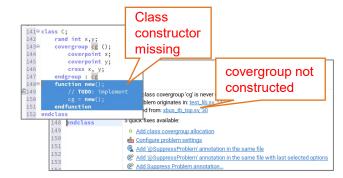
Verdi Integrated Design Environment (IDE)



IDE

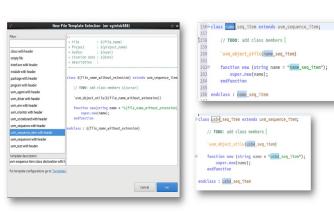
	euclide_workspace - euclide_example_project/rtl/memory_bank/memb_	sank.v - synop	eys Eucode				
File Edit Navigate Search Project I	lun Window Help						
B • 2 0 0 3 € € 4 •	• 😡 Eclipse • 🖂 • 🛛 🕸 🏦 🐮 🖓 • 🖓 🖉 🖗 • 🗍 🤋 • 🖗 • 🗘 •				Quick Ao		8 3
🔓 Project Explorer 🛙 👘 🗆	😰 classified_affo 👔 adder.x 😥 cffo_pkg.sv 😰 cffo_tb_top.sv 😰 interfaces.sv	R *memb_b	ank.v II 🗇		(): Outine II		- 0
E 🐧 🔻	10/*. 2 * File : nemory back y					E A	8 0
·	3 * Project : built demo				type fitter te:	e.	
Common	4 * Author : Gilad 5 * Creation date : Jan 24, 2017						
Core	6 * Description :				* 9 memb.b		
 B memory_back 	7 •	*****			 input. 	db - hiera	chical inst
	50 module memb bank import memb pkp::*; #{						
😥 membupkg v	10 parameter MEM BANK SIZE = 16, 11 parameter MEM LINE SIZE = 128,						
E memb.top.v	11 parameter MEM LINE SIZE = 128, 12 parameter TAG WIDTH = 8,						
2 tan_interface.v	13 parameter MEM BANK ADDR WIDIM = \$clog2(MEM BANK SIZE) 140) (
P Co stans	15 input rst n.						
Comple_al.cud	16 input clk, 17 two interface.mod target two port						
анн. и ами. т. Со. — о т	100); 20 localparam INPUT_FILE_WIDTH = NEMB_RED_TYPE_NIDTH + NEM_RANK_ADDM_NIDTH + 21 June Transmit Strip WIDTH-101 (newst 40, in Asta + Stee sert ran tune, two set			the most ra			
анна, п али то со., то о	19 20 localparan IMPUT_FILE_WIDTH = MEMB_RE0_TYPE_WIDTH + NEW_BANK_ADDR_WIDTH + 21			i tan Mirt ra	3		- 0
Ŧ	13 33 localparas Jawl FJLE J2DIN = NAM JAN JYFE J2DIN + NAM JAN	ert ron selde	tin net on fati				
vype filter text	$ \begin{array}{c} 10 \\ 11 \\ 12 \\ 12 \\ 12 \\ 13 \\ 10 \\ 10 \\ 10 \\ 10 \\ 10 \\ 10 \\ 10$			Location		D 1	
v type filter text @ mesh.menb.ton.if - txx.interfac	$\label{eq:constraint} \begin{array}{c} 12\\ 12\\ 12\\ 12\\ 12\\ 12\\ 12\\ 12\\ 12\\ 12\\$	rt ran addr Resource	tun sort ran dati Path	Location		Type	
 ▼ type filter test meshumembutonuf - tesuinterfac * * membubank - membubank 	1 Secolarem 2007 (712 / 2214 + NBB / 82 / 714 / 2214 + KBB / 840 / 840 / 2214 + 21 size (1996 / 712 / 2214 + 1916 / 121 / 2016 / 121 / 2016	Resource	Path feutide_example.p	Location /euclide_example.	.project/dw/cff (Type LuclidE an	kysis prod
v type filter text. @ mesh.memb.ton.if - texstefsc * ff meeh.bask - memb.bask @ pagt.db - common.file @ bcd.2.7keg - bcd.2.7keg	If the local same about printing print in these prints prints in the print print print in the print pri	rt ren addr Resource cffo_scoreboar common_arb_r	Path feuclide_example.p	Location /euclide_example. /euclide_example.	.project/dw/cff (Type lucidE an	ilysis prob
v type filter text. @ nexth.membit.ton_if - tax.interfac * P membit.bank - membit.bank @ input.ub - common_iffo	Bendpares about prote gather weak years after a war pane about prote gather war pane about prote gather war pane about protection about p	rt ron addr Resource offo_scoreboar common_arb_r memb_bank.v	Path feutide_example_p feutide_example_p feutide_example_p	Location /euclide_example. /euclide_example. /euclide_example.	.project/dw/cff 8 .project/nti/cor 8 .project/nti/me 8	Type SuctidE an SuctidE an	iliysis prod iliysis prod
v type filter text @ nsph.menb.tm.# - tex.interfac " n nexb.bask - nerm.bask @ inpst.db - common, filo back_2.2 may Selected Venezby, memb.tap.memb.bask	If the local same about printing print in these prints prints in the print print print in the print pri	Resource cffo_scoreboar commo_arb_s memb_bank.v memb_bank.v	Path Path /euclide_evample_p /euclide_evample.p /euclide_evample.p	Location /euclide_example. /euclide_example. /euclide_example. /euclide_example.	project/dw/cff (project/mi/cor (project/mi/me (project/mi/me (Type JuclidE an JuclidE an FuclidE an	iliysis prob iliysis prob iliysis prob

- Synopsys Euclidebased design environment
- Customizable look (ex dark mode)
- Supports design and testbench creation

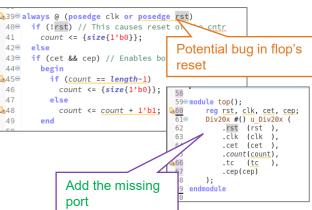


- Checks on-the-fly
- Supports UVM and SystemVerilog
- Addresses potential sim compile issues

Smart Code Template



- A selection of predefined and userextensible templates for UVM classes
- Once actual class name is given, the generated code adapts automatically



Design Lint

Testbench Lint

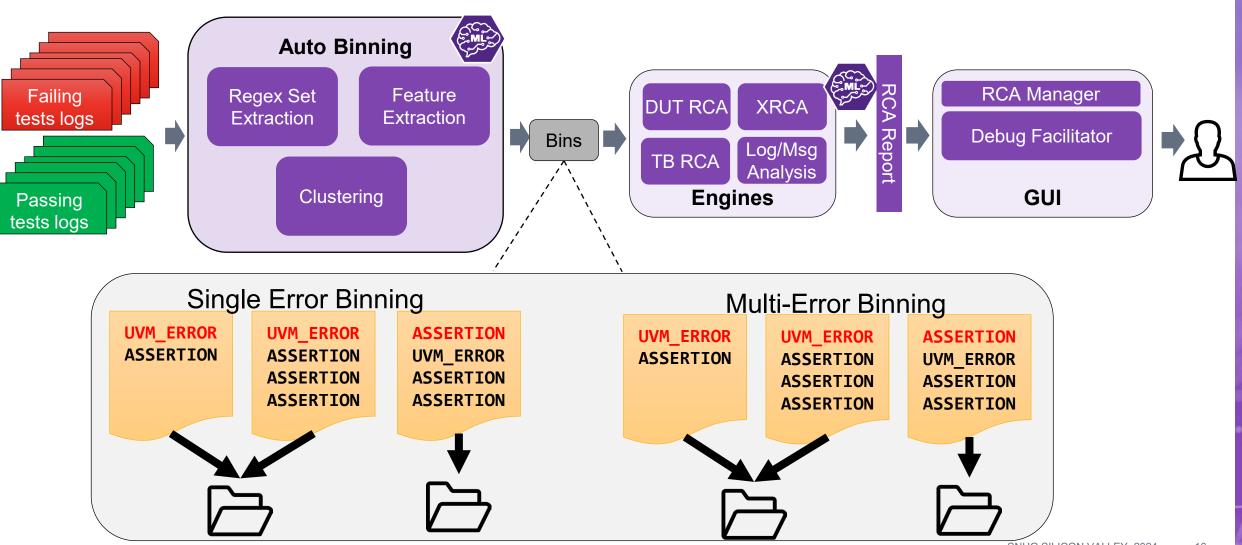
- · Checks on-the-fly
- Errors and warnings noted on relevant code
- Rules and severities are easily configurable



AI-Based Regression Binning

Regression Binning with ML







AI-Based Bug Prediction

Features Failed CLs Extract features Training Passed CLs

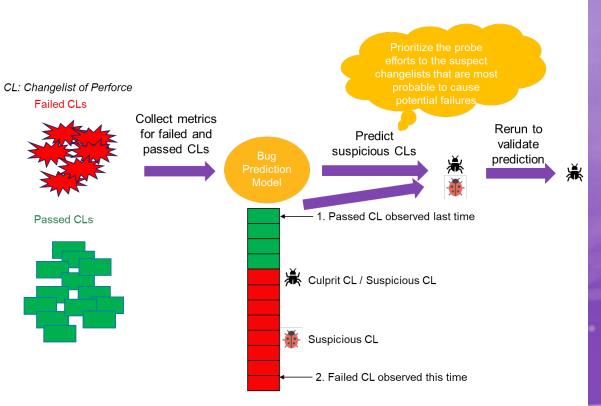
Train the bug prediction model

Smart Probe

ML-based ranking of change lists to root cause regression failures

Customer has an existing probe DB Existing **Probe History** Collect Data with Probe Engine Customer has no probe DB # of CL Changed Lines # of CL Revisions

Bug prediction use model







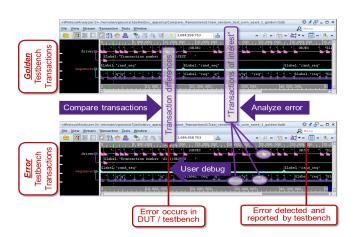
Root Cause Analysis Components

RDA Component Technology





TBRCA

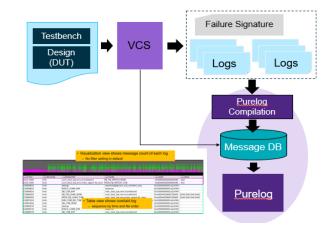


- Transaction Diff Diff the • transaction in the reference vs failing FSDB
- Message Analysis No ref FSDB required. Analyze info from the "error" message.
- Report transaction of interest linked to the error

DUTRCA

- Adopt roll back mechanism and ٠ TraceDiff technology to narrow down DUT problem
- Temporal Flow View to analyze ٠ root cause path

PureLog



- Display messages in table and message chart view
- Intuitive filter, search, data mining operations
- API to access database
- ML technology to ٠ detect abnormal message

TraceDiff



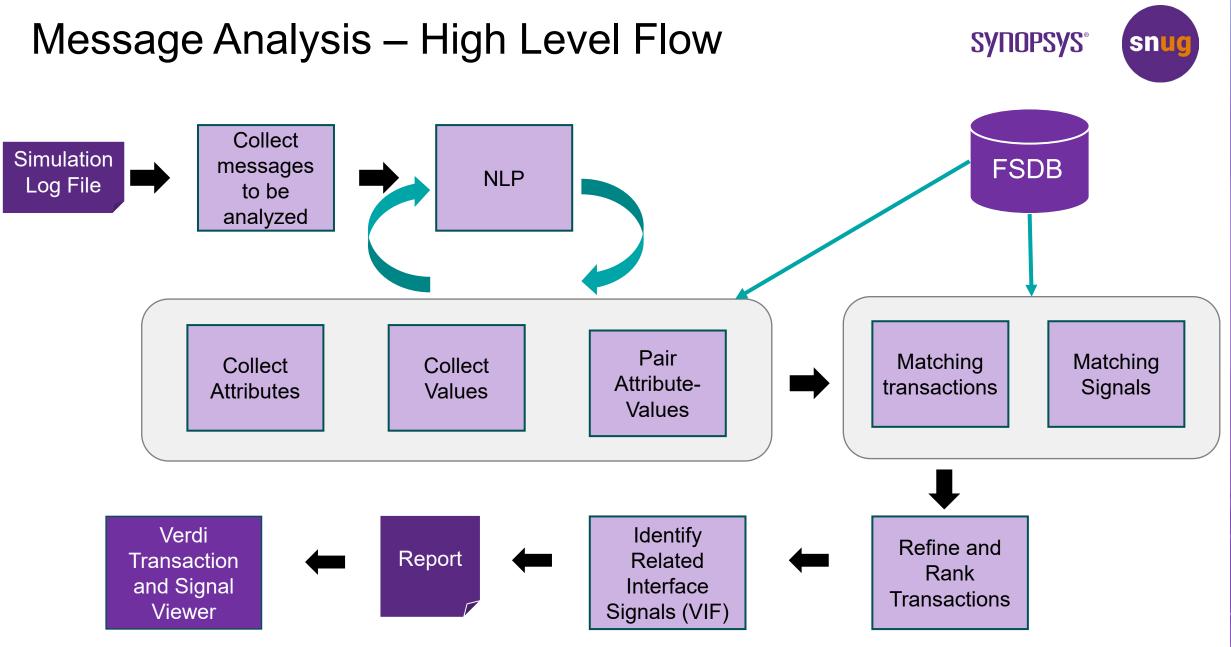
XRCA / with X-Pessimism

٠

- Scan X signals in FSDB and trace the root cause of X
- Handle large amount of X signals in batch mode
- Formal engine to identify X pessimism to remove the noise



AI-Based Message Analysis



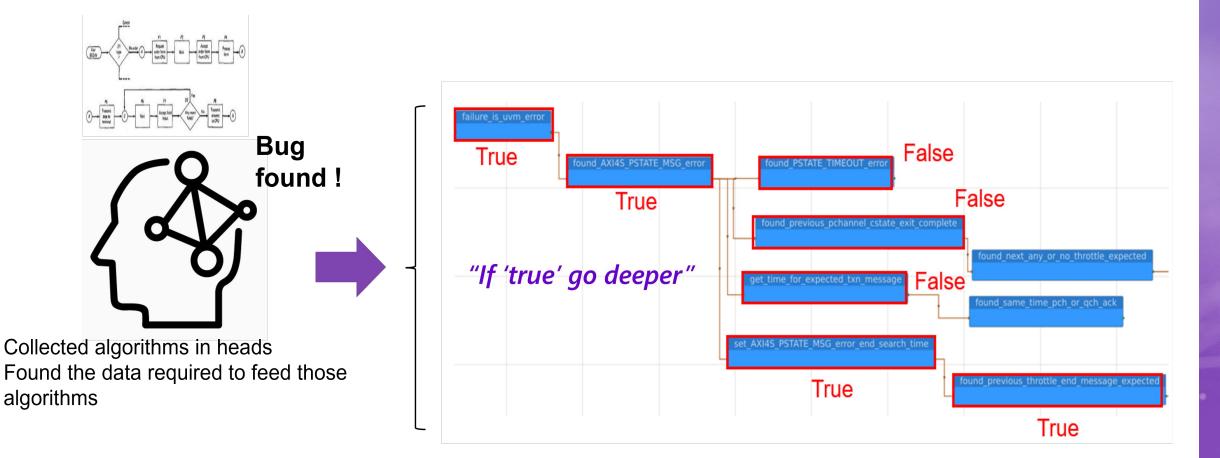


Debug Decision Tree

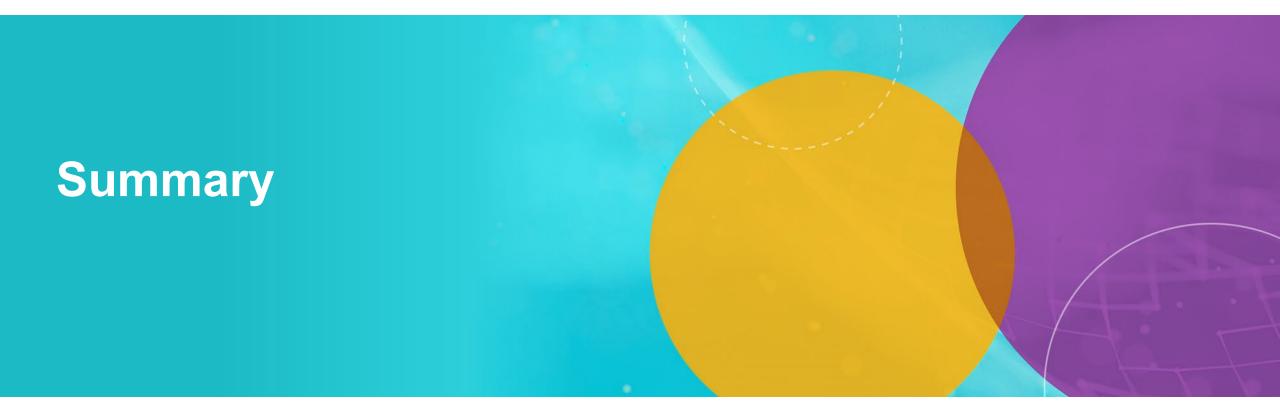
Debug Decision Tree (DDT)



A tool for capturing, sharing, and executing debug knowledge across platforms











- Manual regression debug is tedious, but you can automate it with AI and advanced RCA technologies to debug any failing simulations in Next-Gen Verdi.
- Use the VMS to create a verification plan, then have it manage your simulation env, and gather all the coverage data for analysis in that plan.
- Create correct code by construction by using Euclide in Verdi's redesigned GUI which will allow for quicker and more accurate code generation for your testbenches and design.
- Regression binning classifies many failed tests into a few bins of with similar errors.
- Bug prediction reduces the time spent locating reference snapshots for debug engines.
- Message analysis identifies transactions and VIFs that are related to the error message.
- Debug Decision Tree allows the user to train as set of conditions that can then be checked in new debug cycles.



THANK YOU

YOUR INNOVATION YOUR COMMUNITY