Advanced LLE Aware Design Methodology

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Introduction

- In advanced process node, the impact of LLE so large that it cannot be ignored, and has become a level that must be considered at the design stage

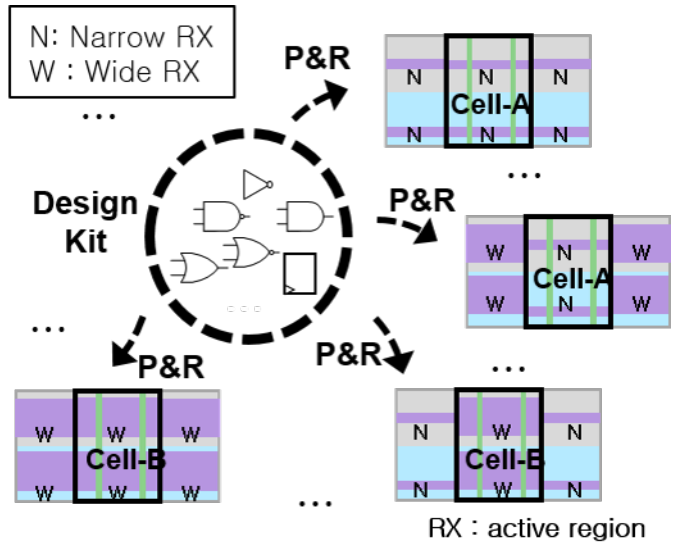
- In this presentation, we introduce LLE aware design methodology from characterization to timing signoff for accurate timing and power analysis

Motivation

- LLE (Local Layout Effect)
  - Electronic characteristics change according to the neighbor pattern

- Motivation
  - Conventional design method for DK characterization uses min/max overlay for timing min/max bound
  - There are various Nano-Sheet (NS) options
  - Lots of design contexts from NS combinations
  - Fixed overlay makes mismatch between overlay and actual context
  - Need to fill the gap between actual context and fixed overlay

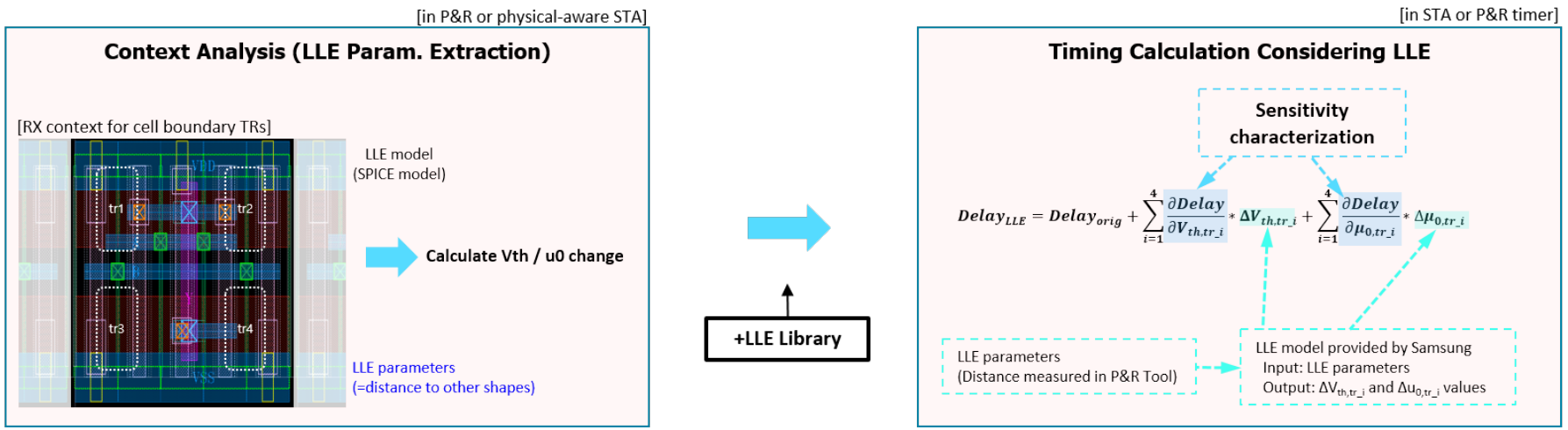
- LLE aware design methodology is needed



Proposal Idea

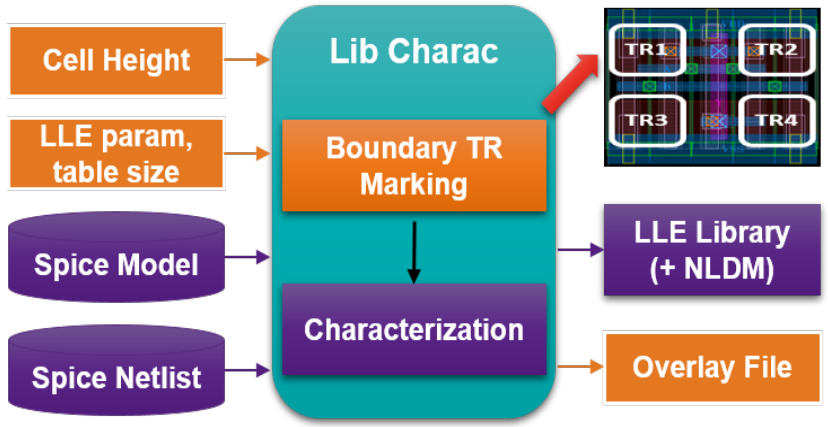
- Basic Concept
  - LLE impact is presented as Vth and u0 change, and then translated into delay change
  - LLE related context can be extracted from physical DB
  - LLE impact on delay can be calculated with design context (Vth, u0 change)

- LLE Sensitivity Library
  - Timing impact per cell boundary transistor's parameter shift is characterized for each timing arc



Sensitivity Library Characterization

- Sensitivity Characterization
  - LLE impact is modelled for
    - Boundary transistors
    - timing (delay/slew), leakage power
    - Perturbation parameters (Vth, u0)
  - Needed information
    - Cell height for boundary transistor recognition
    - Perturbation values for LLE parameters
    - Index points (table size)



Sample Liberty Format

```
cell(test_cell) {
leakage_power() {
   related_pg_pin : "VDD" ;
   when : "!A&!B&!CI&!CO&!S" ;
   value : "2.91394e-05" ;      ## origin leakage value
   ...
   lle_delta_leakage_power(lle_lkg_delta_2) {
     related_params : "vth" ;   ## param definition > Vth or u0
     related_devices : "tr1" ;   ## boundary tr definition > tr1, tr2, tr3, tr4 ....
     index_1("-0.015, 0.015"); ## perturbation value of parameter
     values("2.87158e-09, -2.56085e-09");  ## sensitivity (delta value)
   }
   ...
}
  ...
 pin(Y)
   timing() {
   ...
     cell_fall(8x8) {
       index_1("...");
       index_2("...");
       values("..."); ;      ## origin timing table
     }
     ...
     lle_delta_cell_fall(lle_1x3x3) {
       related_params : "vth" ;   ## param definition > Vth or u0
       related_devces : "tr1" ;   ## boundary tr definition > tr1, tr2, tr3, tr4 ....
       index_1("0.015");          ## perturbation value of parameter
       index_2("0.0011535, 0.102186, 0.809411");  ## index from origin index
       index_3("8.5511e-05, 0.00230265, 0.0355597");
       values("-1.51201e-06, -2.65675e-07, 6.45165e-09",\
              "-1.87921e-07, -3.77126e-07, -1.41947e-07",\
              "1.25844e-06, -1.54662e-05, -1.19289e-05");  ## sensitivity (delta value
     }
...
     }
}
```

LLE Aware Place and Route

- PNR engine considers LLE effect in timing and leakage power calculation
  - Optimize and legalize with resizing cells by using LLE sensitivity for accurate data

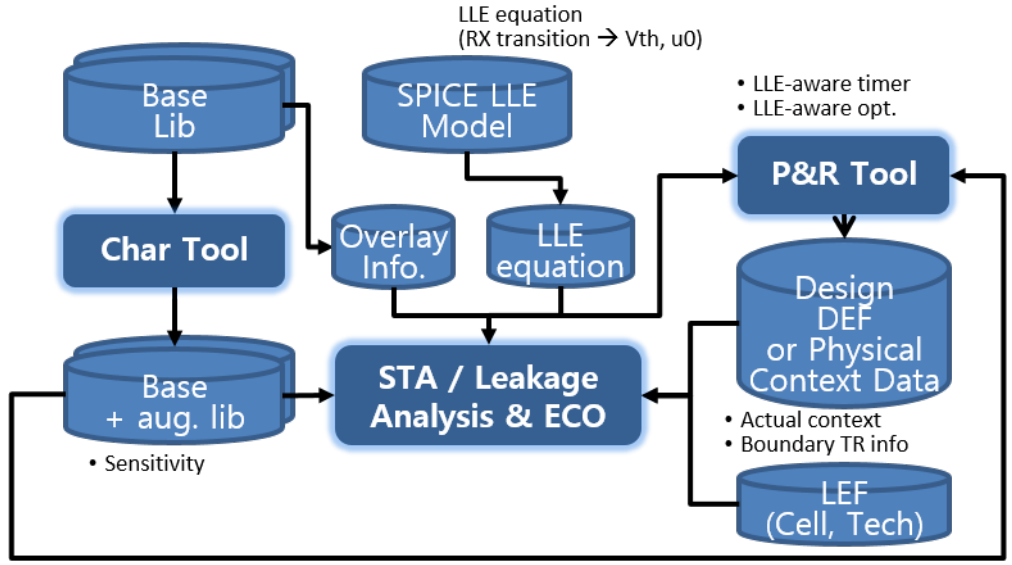
LLE-aware timing & leakage calculation

(*) Empty spaces are assumed to be filled following filler app option

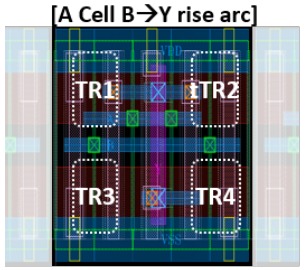
Optimization with LLE-applied data

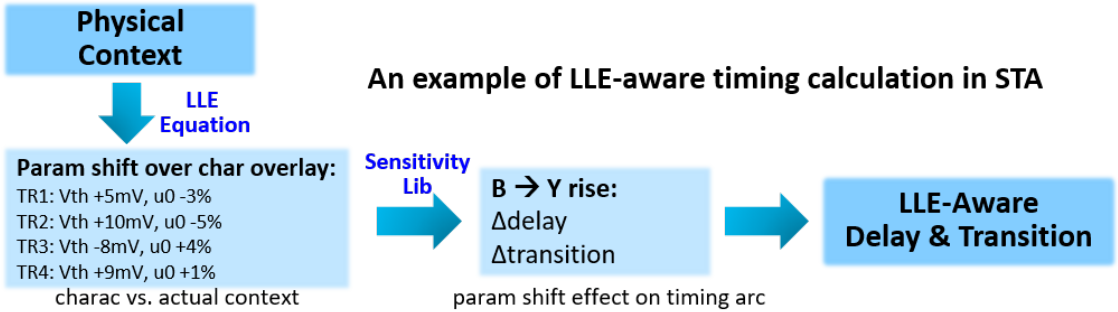
LLE Aware Timing Analysis

- Overall Flow and Required Collaterals
  - LLE sensitivity libraries
    - Timing arc sensitivity per victim transistor impact
  - LLE model and overlay information
    - DLL compiled with LLE impact equations
    - Characterization Overlay (as a shift baseline)
  - DEF and LEF (Design context)
    - For context information and boundary TR mapping



- Delay Calculation in STA
  - Recognize neighbor cell (transition or not)
  - Calculate parameter shift value (Vth, u0)
  - Apply parameter shift value
  - Delay calculation

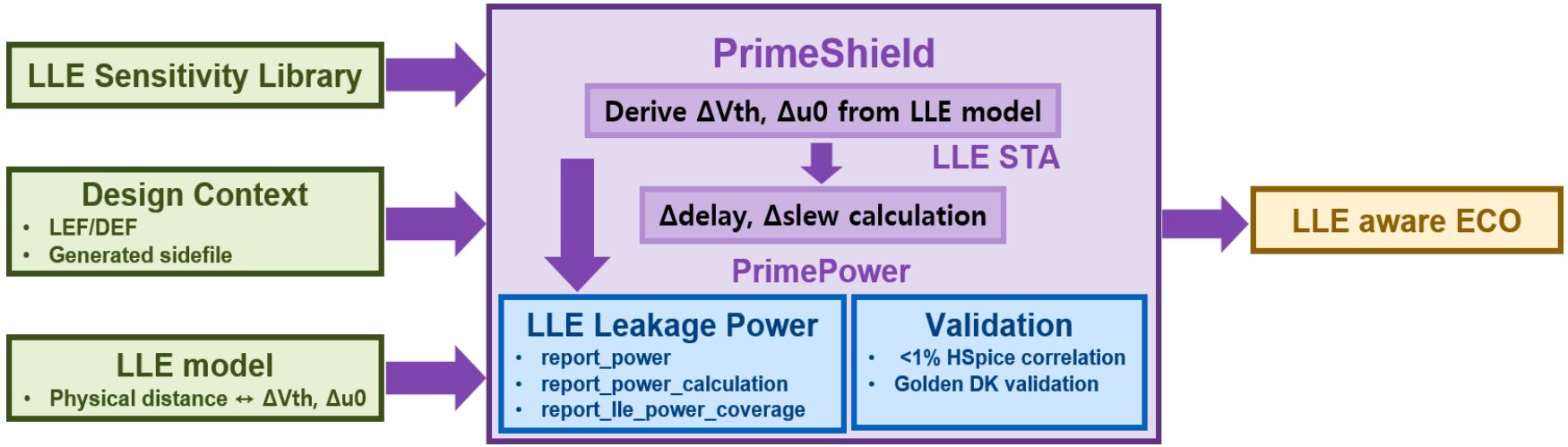




LLE Aware Power Analysis

- Overall Flow and Required Collaterals
  - Similar design flow and input collaterals as LLE STA

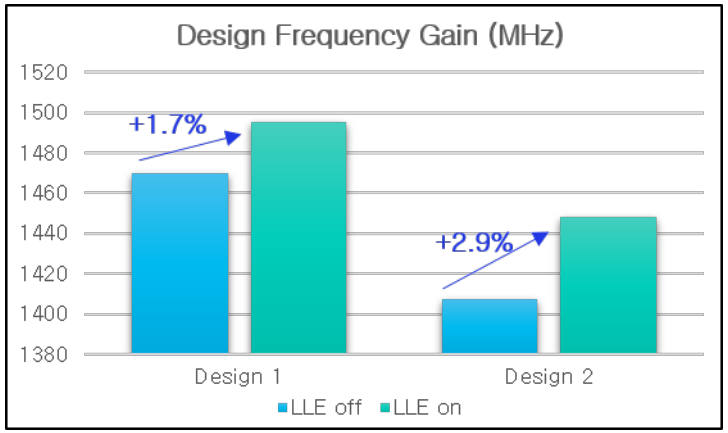
- LLE Leakage power calculation
  - Leakage varies linearly with mobility (u0) and quadratically with threshold voltage (Vth) shift
  - For FFPG (SSPG) corner, leakage generally *decreases* (*increases)* when LLE is ON
  - PrimePower leakage power accuracy within 1% of HSpice simulation and Golden DK results
  - New “physDB lite mode” flow for full chip LLE signoff support

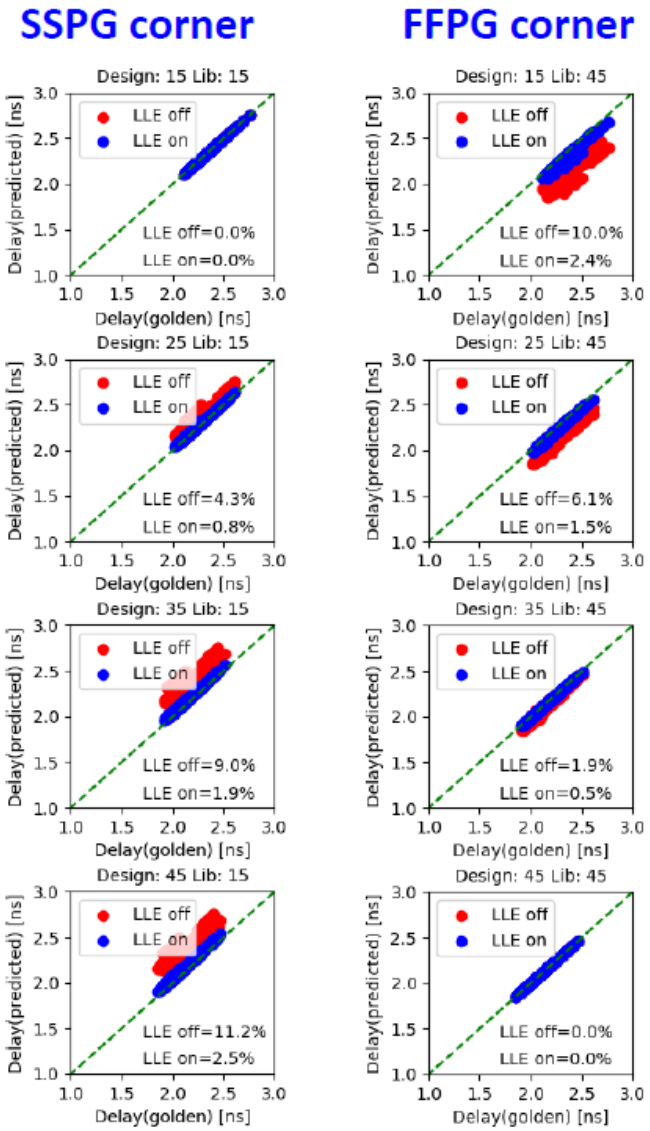


Validation and Design Gain

- Validation : STA-SPICE Correlation
  - Design with various NS width cells
  - Between all instances, have enough space for filler cell
  - Same NS filler cells are inserted in this space
  - Check STA-SPICE correlation by all NS cases
  - Shows better correlation with LLE aware Flow

- Signoff Gain
  - Shows around 2% design frequency gain





Conclusion

- In advanced node, LLE impact in design flow is no longer negligible
  - Especially with conventional overlay condition
- LLE impact can be reflected in design flow with the methodology presented
- LLE impact of each boundary transistor should be modelled in library by SPICE parameters
- In PNR stage, the tool optimizes design by resizing consuming LLE sensitivity
- In STA stage, the tool determines updated timing of each cell by considering it's neighbors
- In power analysis, the tool calculates accurate leakage power with LLE term
- Considering LLE impact yielded 2-3% frequency gain on designs

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THANK YOU

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