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Dtech GCAD

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Interconnect Skew-Driven BEOL Robustness Methodologies

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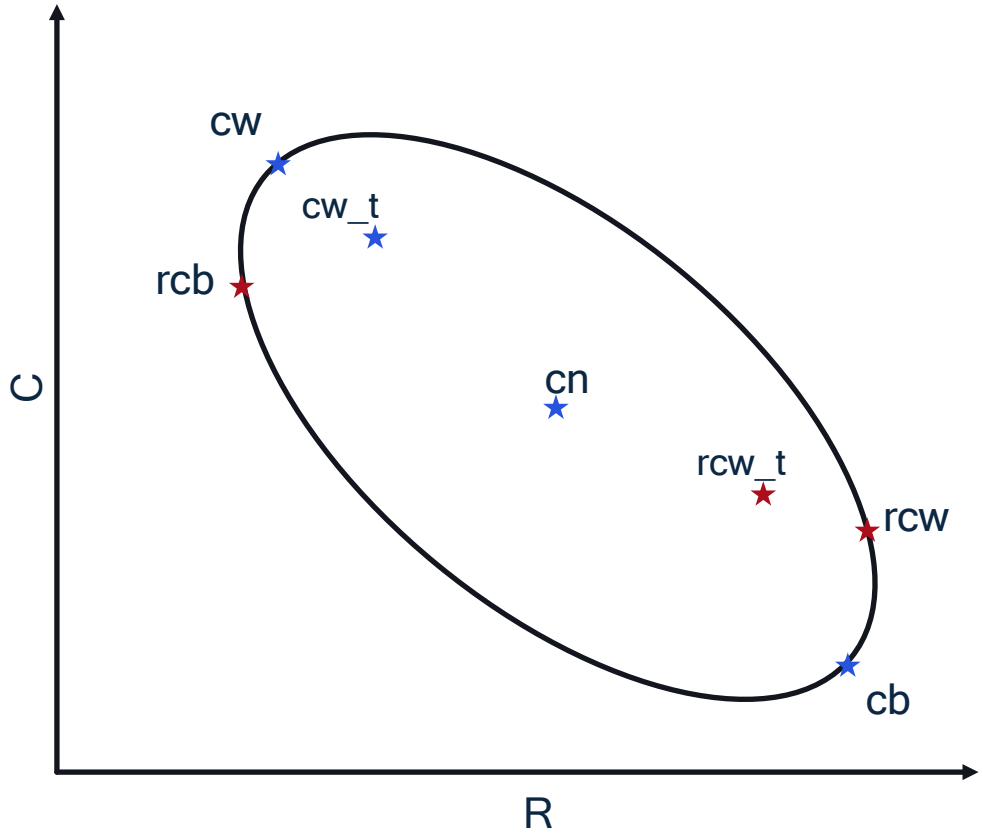
Background: RC Corners

- Account for interconnect global variation
- Cover temperature, dual-patterning, _t (different sigma coverage)
- 3sigma corners are to bound R and C shifts

Corner	Width	Thickness	Spacing	Height
cb	Min	Min	Max	Max
rcb	Max	Max	Max	Max
cw	Max	Max	Min	Min
rcw	Min	Min	Min	Min

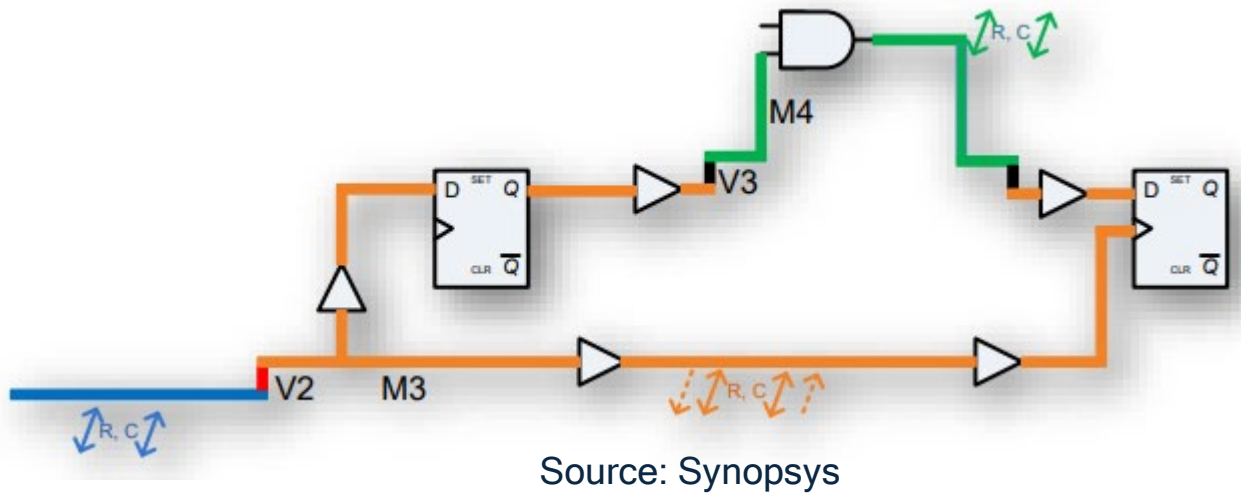


Interconnect Skew: Enumeration Problem

- Current STA run assumes all metal layers belong to the same RC corner
- Metal variations are highly correlated within each layer, but uncorrelated among different layers
- To properly capture the metal mistracking effects we need to enumerate across many STA runs → not feasible

Run	M0	M1	…	M_{Top}
1	CW	CW	CW	CW
2	CW	CW	CW	CN
…	…	…	…	…
2^N	CN	CN	CN	CN

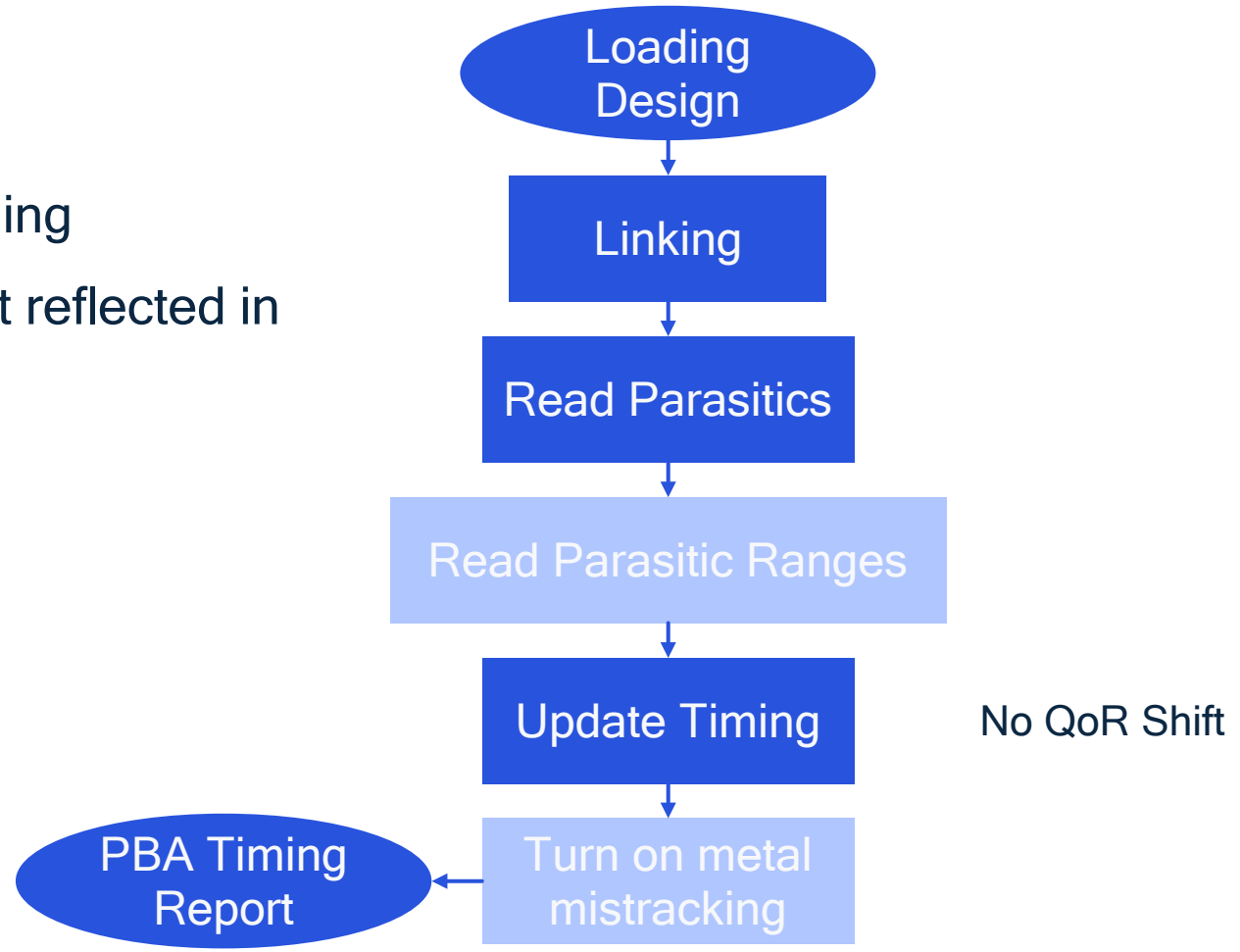
- PrimeShield (PS) Interconnect Skew
  - Model cancellation of same-layer variations
  - Use signoff calculation engine
  - Reasonable runtime



Source: Synopsys

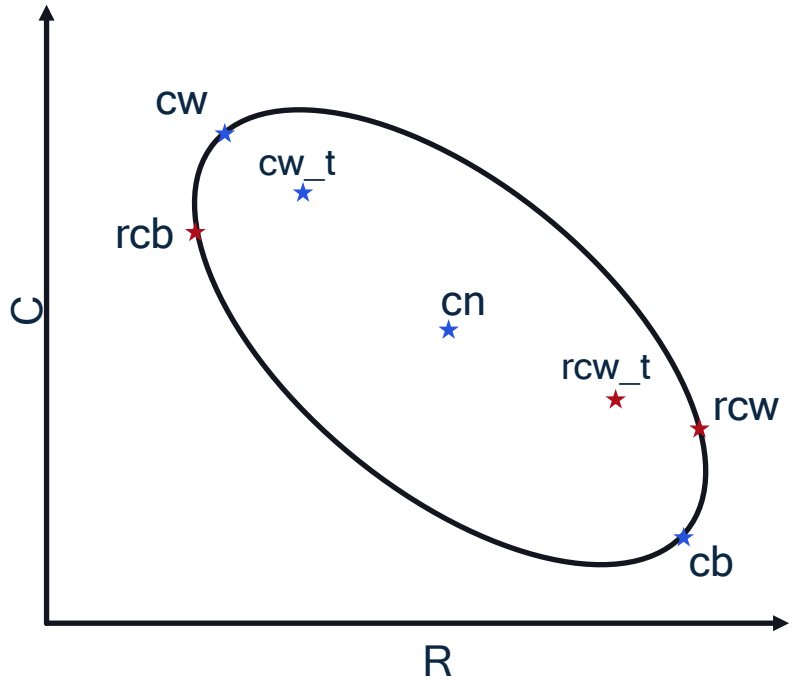
Interconnect Skew: Flow

- Same as regular STA flow
- Read parasitic ranges
- No QoR change through update_timing
- Metal mistracking induced slack shift reflected in PBA timing report
- Work with both SPEF and GPD



Interconnect Skew: Sample Flow

```
set ps_enable_analysis true
# Load libraries, netlist and linking the design
read_parasitics test.spef.gz
set_parasitics_range -cap {0.8 1.0} -res {1.0 1.2} -layer {M0 M0_mask1 M0_mask2}*
set_parasitics_range -cap {0.8 1.0} -res {1.0 1.2} -layer {M1}*

set_parasitics_range -cap {0.8 1.0} -res {1.0 1.2} -layer {Mtop}*
update_timing -full
set paths [get_timing_paths -pba_mode path -path_type full_clock_expanded -max_paths 1000 -nworst 10 \
            -slack_lesser_than 0.1] → Normal PBA

‘’’
save_session
restore_session

‘’’

set interconnect_skew_enable_path_analysis true

set paths_new [get_timing_paths -pba_mode path -path_type full_clock_expanded -max_paths 1000 \
                -nworst 10 -slack_lesser_than 0.1] → Interconnect skew PBA
set path [index_collection $paths_new 1]
get_attr $path slack → slack updated with metal mistracking impact
get_attr $path interconnect_skew_slack_shift

report_path_robustness -type interconnect_skew $path
```



* Ranges are only for illustration purposes

Interconnect Skew: Example Timing Report

```
  Startpoint: */.../reg1 (negative level-sensitive latch clocked by XXX)
  Endpoint: */.../reg2 (rising edge-triggered flip-flop clocked by XXX)
  Last common pin: */.../clk
  Path Group: XXX
  Path Type: max  (recalculated)
  Sigma: 3.0
  Point                                    Incr       Path
  ------------------------------------------------------------------------
  clock XXX (fall edge)                    0.4200     0.4200
  clock source latency                     0.0000     0.4200
  sclk (in)                                0.0019 &   0.4219 f
  u_xxx/.../z                              0.0159 &   0.4378 f
...
clock reconvergence pessimism              0.0005     1.1414
  inter-clock uncertainty                 -0.1020     1.0394
  library setup time                      -0.0270     1.0124
  data required time                                  1.0124
  ------------------------------------------------------------------------
  data required time                                  1.0124
  data arrival time                                  -1.9498
  ------------------------------------------------------------------------
  Interconnect skew adjustment             0.0150    -0.9224
  statistical adjustment                   0.0125    -0.9099
  slack (VIOLATED)                                   -0.9099
```

Interconnect Skew: report_path_robustness

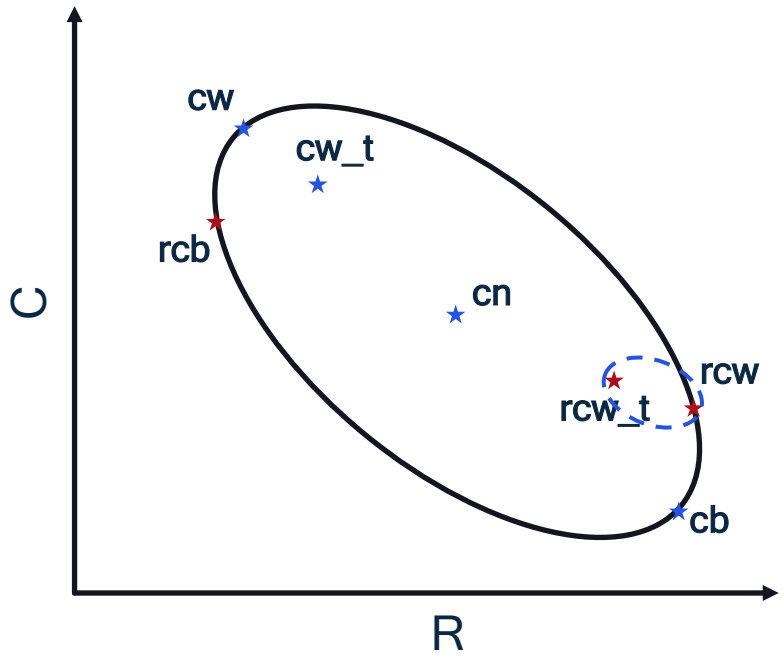
Startpoint: */reg1 (rising edge-triggered flip-flop clocked by XXX)
Endpoint: */reg2 (rising edge-triggered flip-flop clocked by XXX)
Path group: XXX
Path type: max (recalculated)
Slack shift: 0.025665

Layer	Min sensitivity	Max sensitivity	Flag
M0:M0_mask1:M0_mask2			
	0.000000	0.005806	
M1:M1_mask1:M1_mask2			
	0.000000	0.003579	
M2:M2_mask1:M2_mask2			
	0.000000	0.003689	
M3:M3_mask1:M3_mask2			
	0.000000	0.026804	
M4:M4_mask1:M4_mask2			
	0.000000	0.008521	
M5	0.000000	0.007405	
M6	0.000000	0.002024	
M7	0.000000	0.006375	
M8	0.000000	0.008199	
M9	0.000000	0.006525	
M10	0.000000	0.005521	
M11	0.000000	0.000018	
M12	0.000000	0.000000	unused

Interconnect Skew: Parasitic Ranges

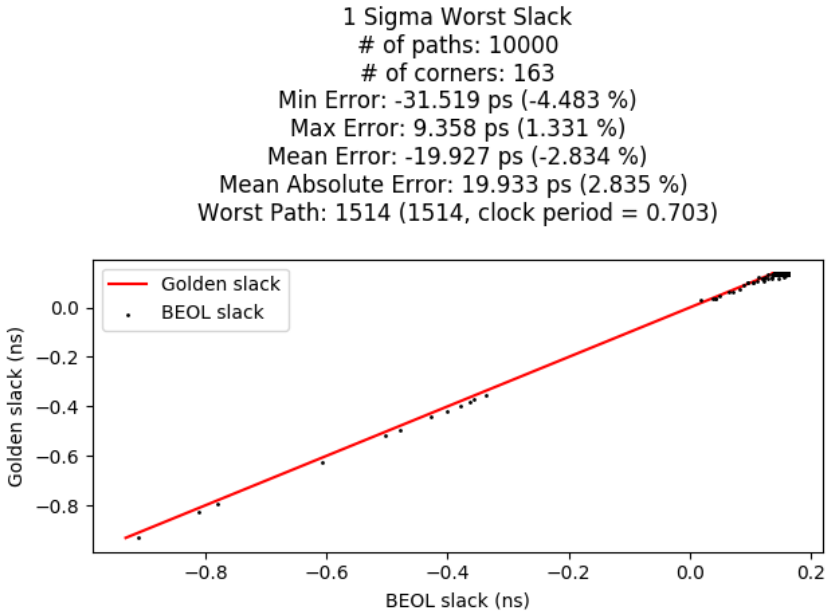
- From foundry

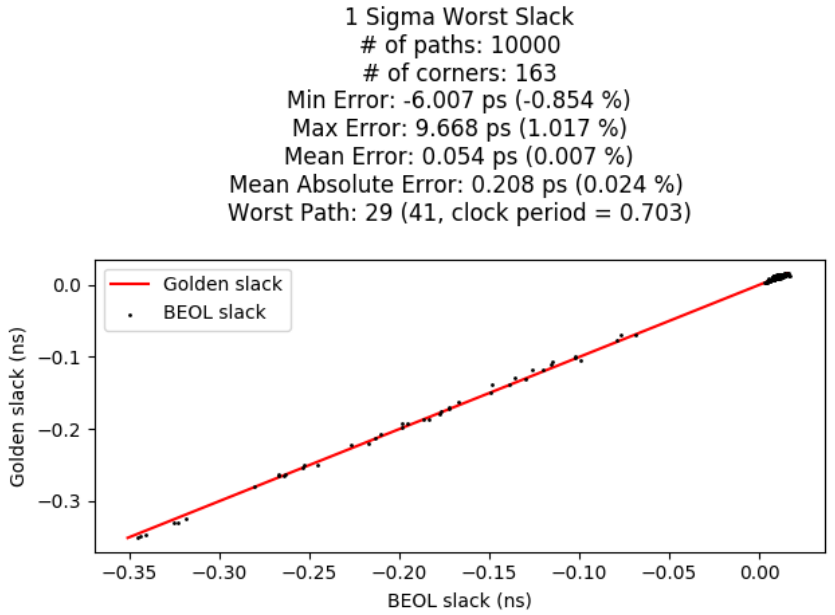
- Using multi-GPD analysis
  - Define reference corner
  - Define -min / -max reference corners, e.g., rcw_t and rcw
  - Run extract_parasitic_range



Interconnect Skew: Validation

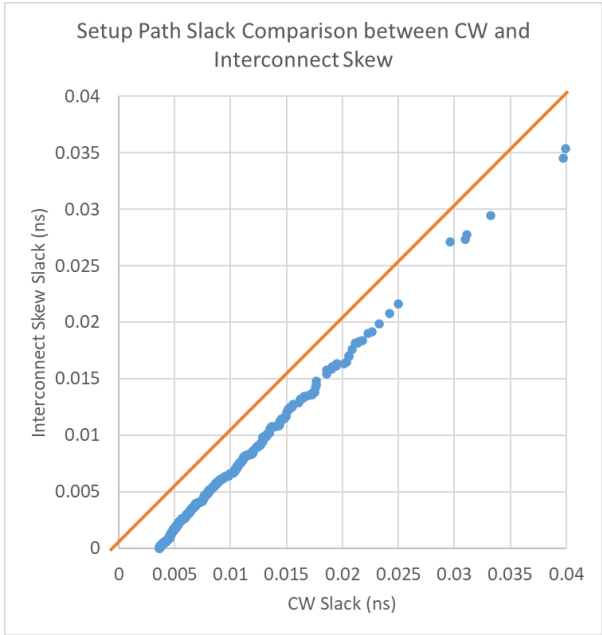
- Validate PS interconnect skew against golden slack
  - Golden slack = scale_parasitics (scaling SPEF directly)
  - Test slack = PS interconnect skew slack

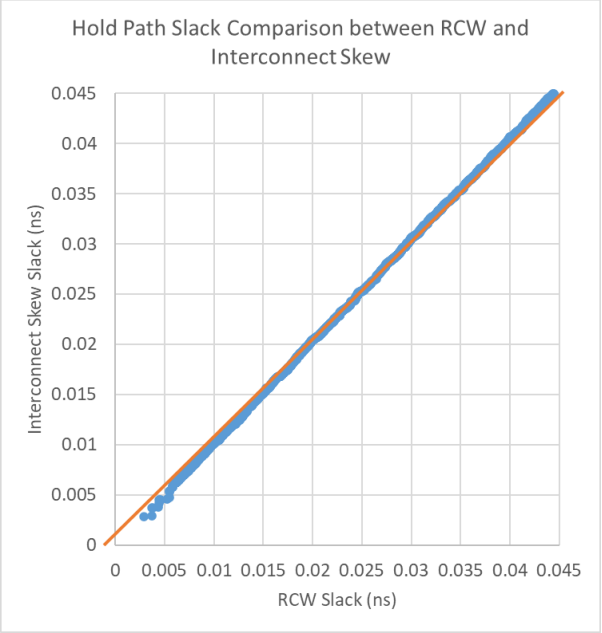




Interconnect Skew: Results

- Interconnect skew can induce slack shifts in paths
  - 5.3ps slack shift in setup
  - 3.4ps slach shift in hold
- Magnitude of the slack shift depends on the design
- Traditional corner-based STA / extraction methodology is not enough to cover timing shifts due to metal mistracking





Interconnect Skew: Summary

- PS Interconnect skew improves design robustness against potential back-end-of-line mistrack
- Derate based methods are simple and pessimistic
- PS Interconnect skew can also provide useful feedback to designers to identify dominating metal layer

Thank you

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