Revolutionizing Advanced Node Processes: Samsung Foundry Embraces Synopsys QuickCap for SF2

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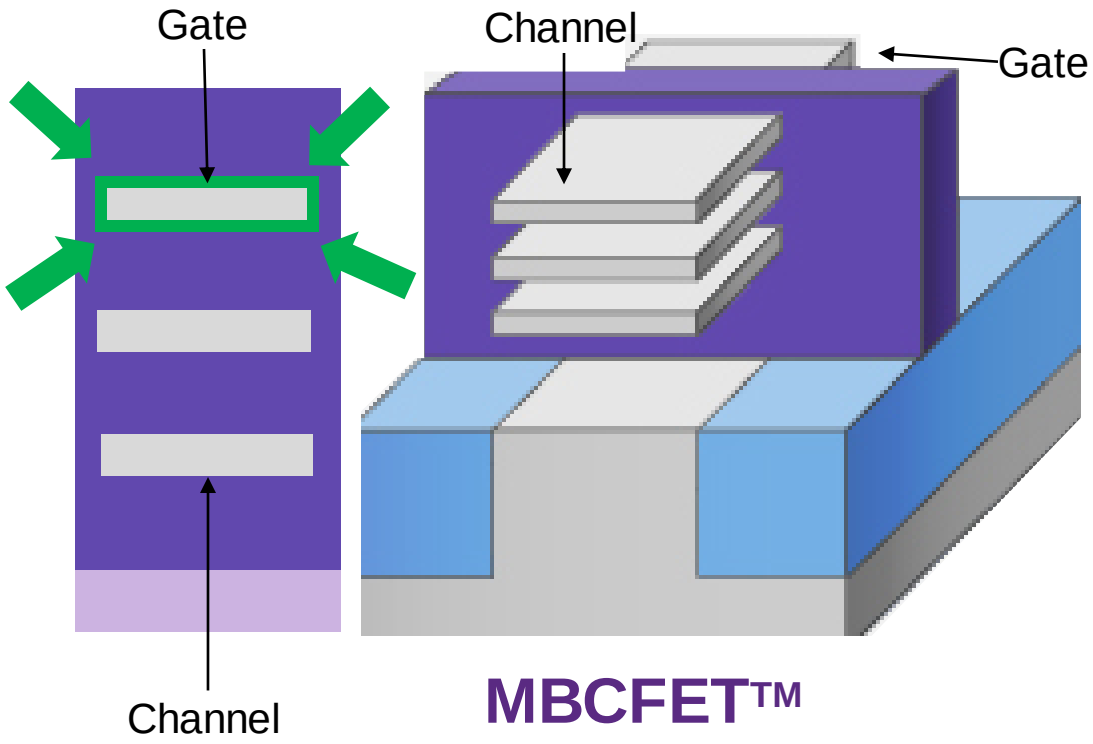
Navigating the Nanoscale

Understanding the Critical Role of RC Parasitics in Adv. Nodes



MBCFET™

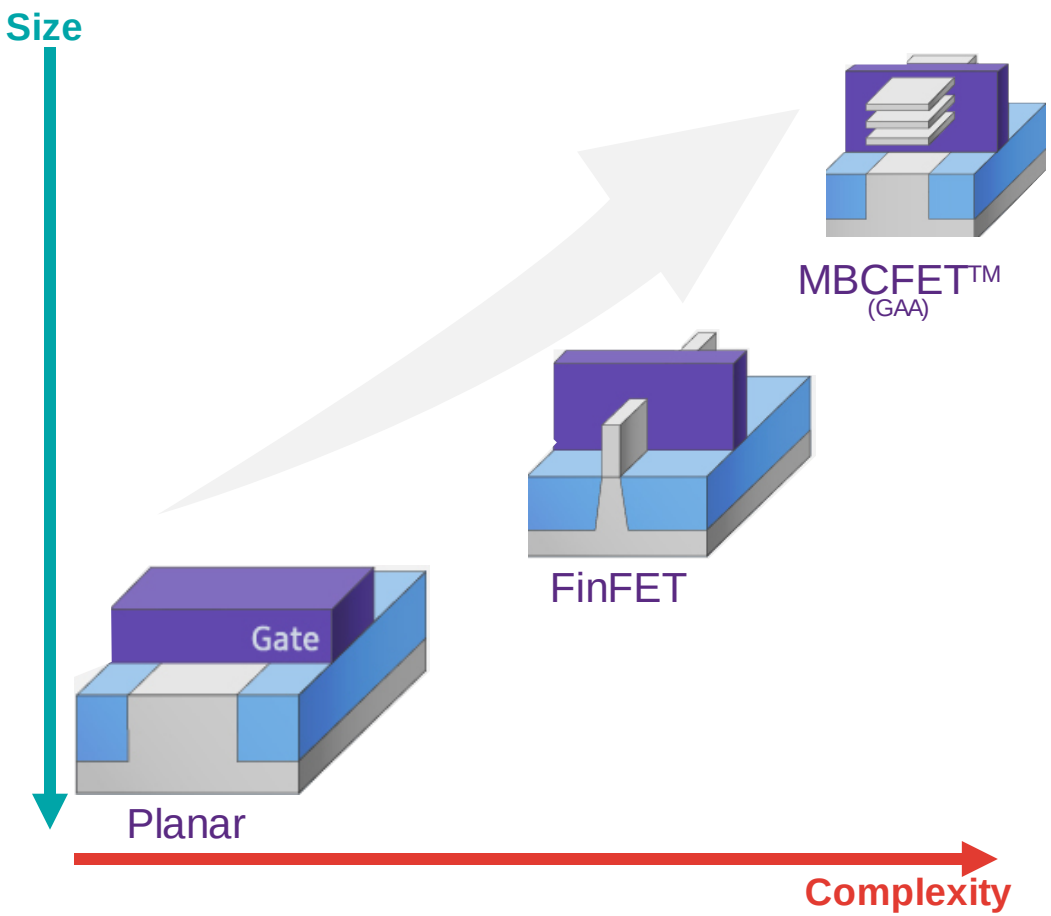
	Power	Perf	Area
SF2 (vs SF3)	-25%	+12%	-5%

*Estimated

Importance of Precise RC Parasitic Extraction

- Parasitic RC effect increases with device scaling.
- Accurate Device modeling is critical for accurate target performance setting and circuit design.
- Failure to accurately model RC parasitics will result in significant delays in design cycle.

Challenges in Developing Advanced Node PDK's for Accurate RC Extraction

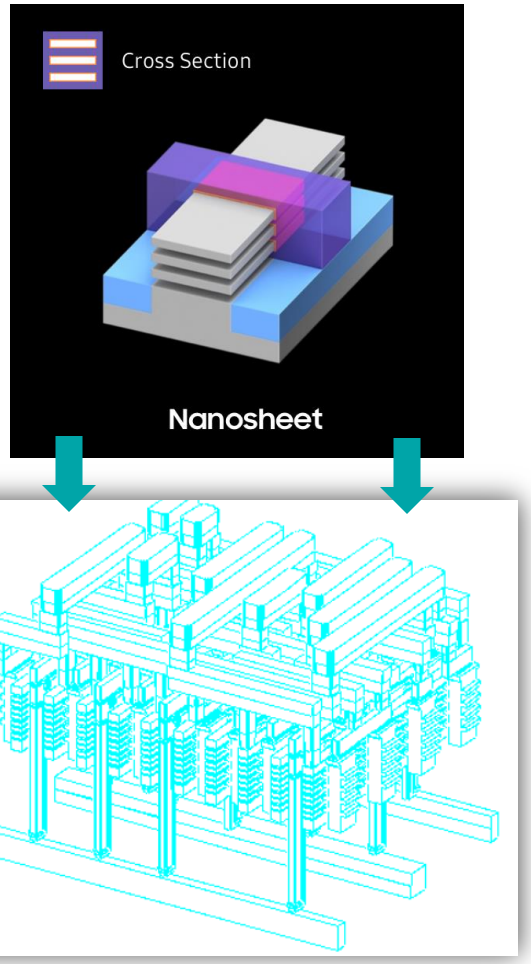


- Exploring Device, Metal and Via layer interactions for Reference Generation.
- Validating Metal and Via patterns against Silicon data.
- Understanding Complex Device Structures.
- Capturing Device Parasitic for Accurate Device Model generation.
- BSPDN process which need extract R and C even with backside connection to device level.

BSPDN : Back Side Power Delivery Network

Enhancing PDK Development

Current limitations impacting the fast, accurate PDK development

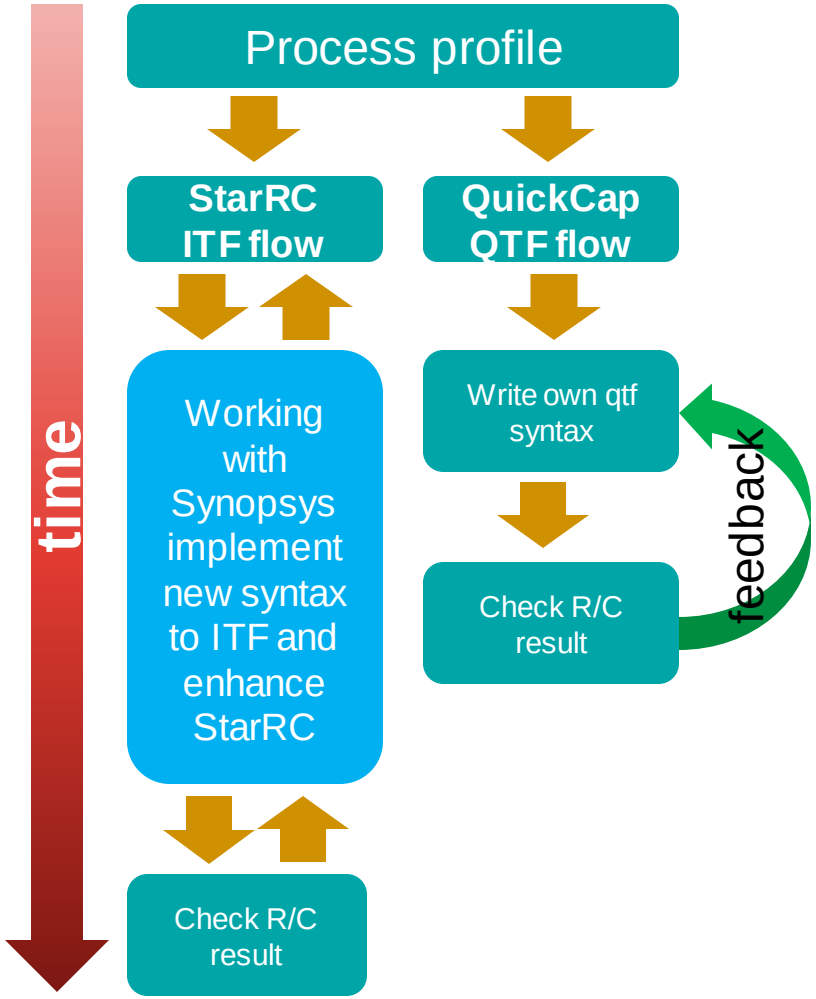


3D representation of Nanosheet device by Quickcap

- Early-Stage Process Development and Structural Testing
  - In the early stages of process development, numerous test versions of structures are required. This is crucial in designing and validating new structures.
  - In advanced nodes, even small changes in shape or material can have a significant impact on device performance. **Therefore, it is important to predict and optimize these changes through accurate PEX modeling.**
- Limitations of Current 2.5D/3D PEX tools
  - Current 2.5D/3D PEX tools face challenges in rapidly creating early stage PDKs with various process structures.
  - Creating a new structure and building a running PDK from it takes significantly more time with modern 3D extraction tools.
- BSPDN Process
  - The BSPDN process requires a different PEX approach from the typical front-side usage, which has been used so far.

Unlocking flexibility with QuickCap QTF

Samsung Foundry QuickCap QTF generation flow



QuickCap QTF flow benefits:

- Significant TAT gain to implement and simulation process profile.
- Simple and easy to write programing syntax.
- Leverage gds format to quickly generate RC information.

QuickCap QTF advantage vs traditional flow.

- Support for Boolean operations allows foundry to experiment, model and analyze layout parasitic effects.
- 3D viewer of quickcap helps a lot when creating new shapes and check if it's really applied as expected.

Unlocking flexibility with QuickCap QTF

Leveraging **QuickCap** for accurate reference PDK development

Current Challenges

#1

- Traditional 3D Solvers have accuracy and performance limitations.

#2

- Limited Flexibility to explore the device and metal profiles

#3

- Requires a lot of effort to model, process and analyze the parasitics.

QuickCap Benefits

#1

- Silicon correlated accuracy with linear scalability across hundreds of cores.

#2

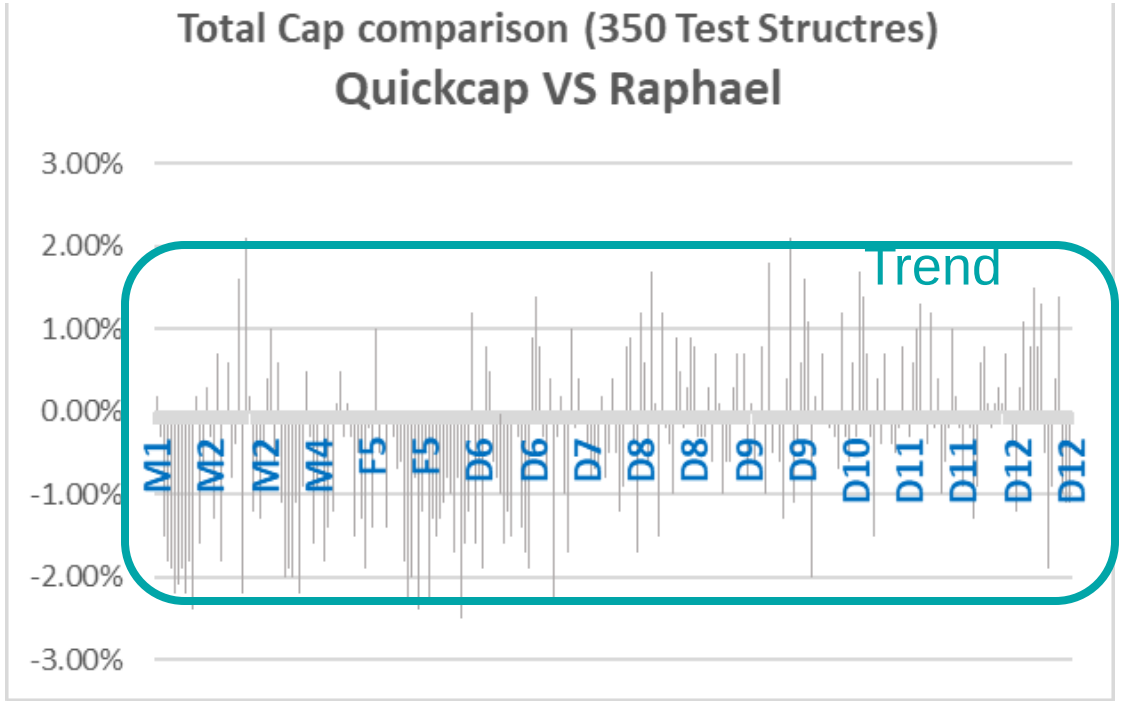
- Offers flexible programming language and 3D profile view for process exploration.

#3

- Allows Boolean operation to quickly analyze various parasitic effects.

2nm : QC vs Raphael BEOL comparison

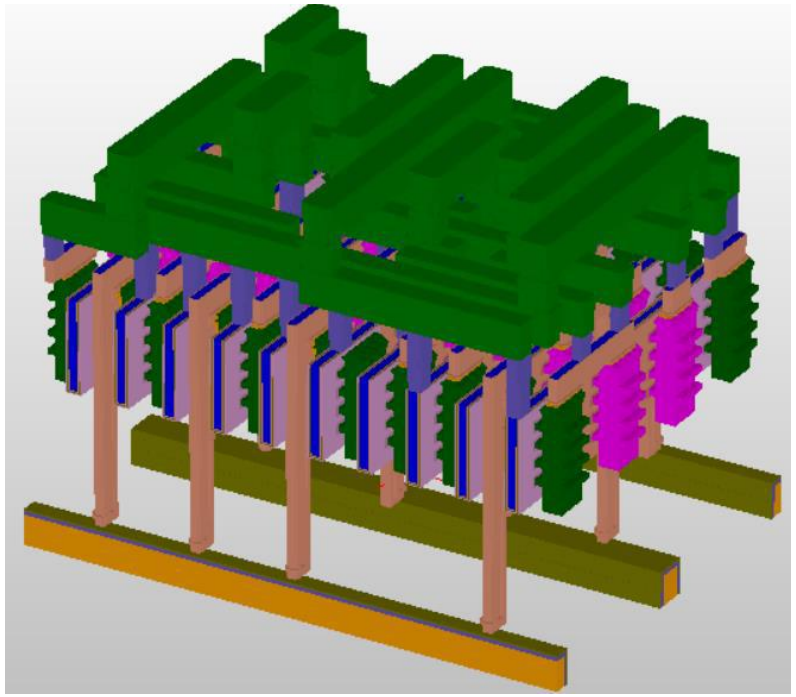
Leveraging Accurate and Efficient Capacitance Modeling



- Samsung uses Raphael as the reference for early test structures.
- QuickCap generated data for 350 structures is compared w/ Raphael.
- QuickCap data is showing tight correlation with Raphael.
- QuickCap ran significantly faster than Raphael

2nm : QC vs Raphael FEOL comparison

Leveraging Accurate and Efficient Capacitance Modeling



3D profile of BSPDN process (not a real caputre)

Total cap comparison

Net	Tcap (QuickCap)	Tcap (Raphael)	Diff (%)
A	1.81E-16	1.80E-16	0.541
Y	1.16E-16	1.16E-16	0.283

Coupling cap comparison

Net Pair	Ccap (QuickCap)	Ccap (Raphael)	Diff (%)
A - VSS	3.71E-17	3.69E-17	0.511
A - VDD	4.05E-17	4.03E-17	0.477
A - Y	1.04E-16	1.03E-16	0.577
VSS - Y	5.97E-18	6.10E-18	-2.209
VDD - Y	6.65E-18	6.78E-18	-1.953

Tight Correlation

2nm : QC vs Raphael FEOL comparison

Tcap and Ccap comparison across various design cells

Total cap comparison

Design	Avg Error (%)	STD (%)
INV_D1	-0.404	0.293
INV_D2	0.412	0.129
NAND2_D1	1.169	0.324
NAND2_D4	-1.942	1.128
NOR2_D1	1.762	0.142
NOR2_D1	-2.077	0.852

- QuickCap generated data for a suite of standard cells is compared against Raphael.
- QuickCap shows tight accuracy correlation with Raphael.
- Both Average Error and Standard Deviations bounds are within limits.

Conclusions & Plans:

Conclusions

- QuickCap results are proven accurate for Samsung 2nm BSPDN process.
- QuickCap will be Samsung Foundry's **Reference** for 2nm BSPDN process and future process nodes.
- As next steps, Samsung Foundry customers will benefit from enhanced StarRC PDK, enabling precise parasitic extraction for Digital, Custom and Multi-Die design.

Future Plans

- Samsung Foundry will leverage QuickCap for 1.4nm and future technologies PDK development.
- Samsung will continue partnership with Synopsys on QuickCap usage.

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THANK YOU

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