Automated Layout and Analysis for Optimization of Power MOSFETs Using PDG and R3D™

Lou Hutter
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Acknowledgements – Co-Authors and Support

- Co-Authors:
  - Mark Harward – Covalar Design LLC
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  - Renaldo Hernandez – Silicon Frontline Technology (now Synopsys)
  - Joe Zhou – Silicon Frontline Technology (now Synopsys)
  - Dermott Lynch – Silicon Frontline Technology (now Synopsys)

Motivation

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- Power Management is essential in most electronic systems.
- Power FET area is a key factor in Power Management IC cost.
- Power FET optimization involves several technology-dependent factors that affect $R_{DS(on)}$ – e.g., # fingers, aspect ratio, # pads and placement, metal buss.
- Manual layout requires too much time and effort to allow full exploration of the layout space.
- The PDG-R3D flow enables the layout design to truly explore the layout space to fully optimize the power FET.

Agenda

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- The PDG-R3D Flow
- Metal Layer / Buss Strategy Exploration
- Power FET Optimization
- Future Work

Acronyms & Terms Used in Presentation

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- FET = Field Effect Transistor
- PMIC = Power Management Integrated Circuit (IC)
- BCD = Bipolar-CMOS-DMOS silicon technology
- $R_{DS(on)}$ = Drain-to-source resistance in “on”-state of Power FET
- R_{SP} = Specific on-resistance (= $R_{DS(on)}$ × Area) of Power FET
- V_{DS} = Drain-to-source voltage. V_{GS} = Gate-to-source voltage
- I_{DS} = Drain-to-source current. $R_{DS(on)} = V_{DS} / I_{DS}$
- DOE = Design of experiments
- BEOL = backend of line (metallization part of the process flow)
- Aspect Ratio = width of structure / height of structure

$R_{DS(on)}$ and R_{SP} – Key Power Figures of Merit

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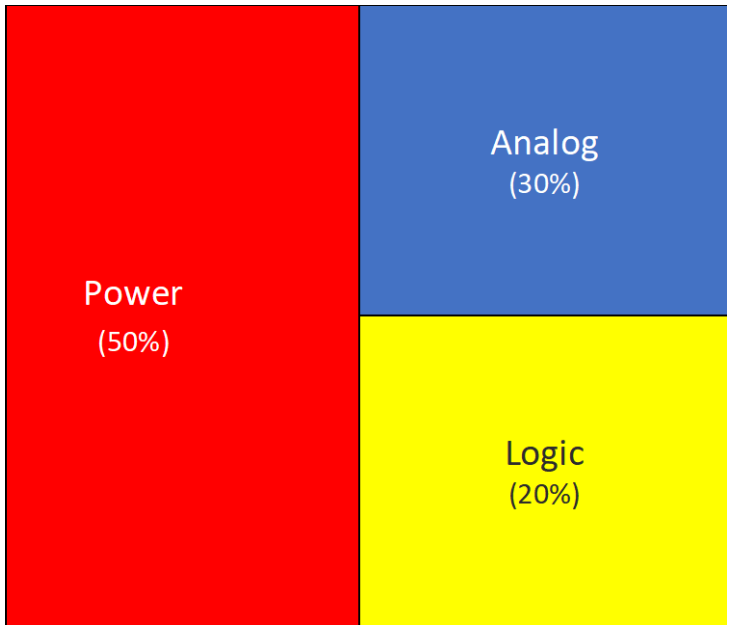
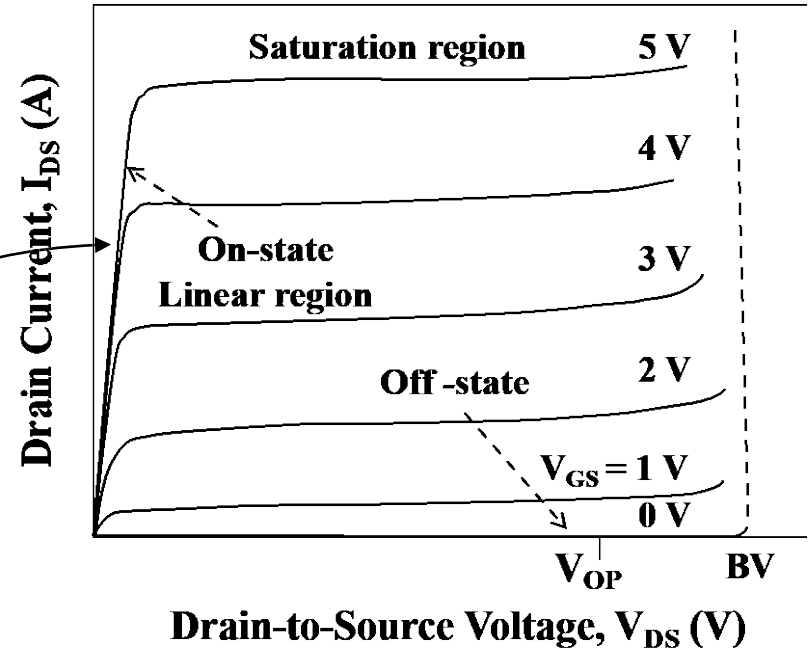
Power FET typically used as switch – “on” and “off”

- Power management ICs (PMICs) merges power, analog, and logic components.
- $R_{DS(on)}$ relates to “on” state. Low $R_{DS(on)}$ → Low IR drop → Higher efficiency.
- For die size, want lowest $R_{DS(on)}$ in smallest Area → R_{SP} (= $R_{DS(on)}$ × Area).



$$\text{Si } R_{DS(on)} \approx \frac{Lt_{ox}}{W\mu\varepsilon_{ox}(V_{GS}-V_T)}$$

$R_{DS(on)} \downarrow \Rightarrow W \uparrow$



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Automated Power FET Generation

PDG-R3D Flow

PDG (Power Device Generator)

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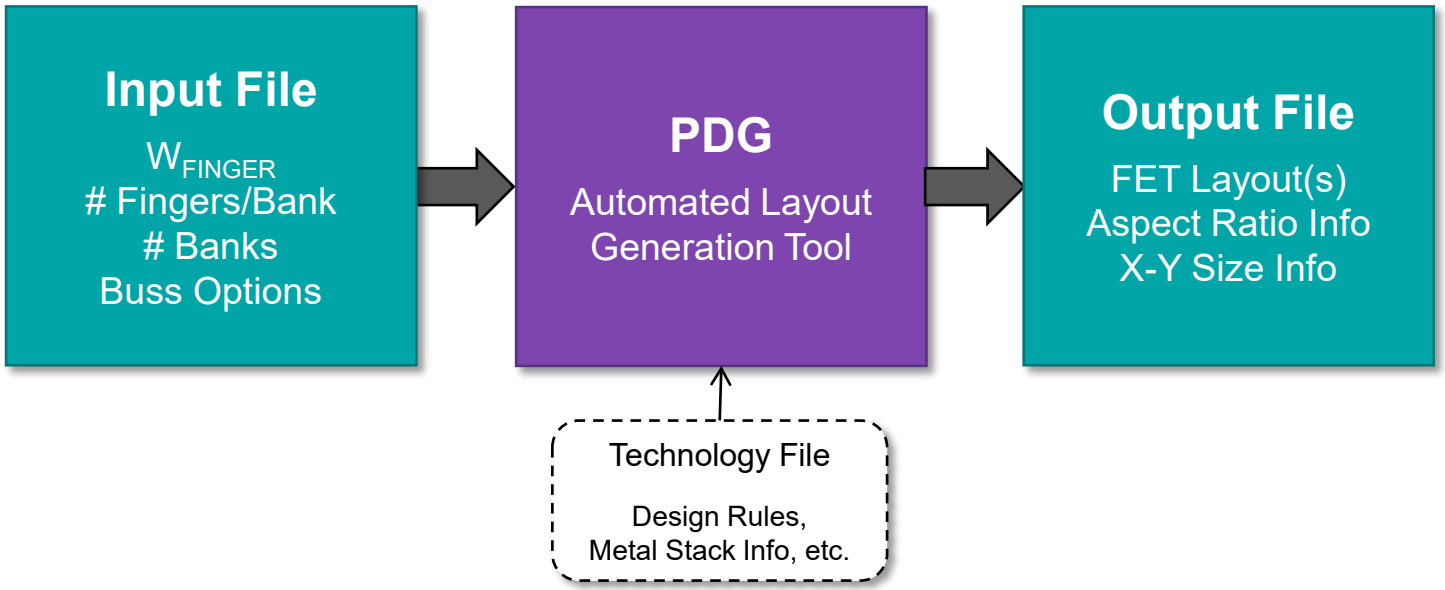
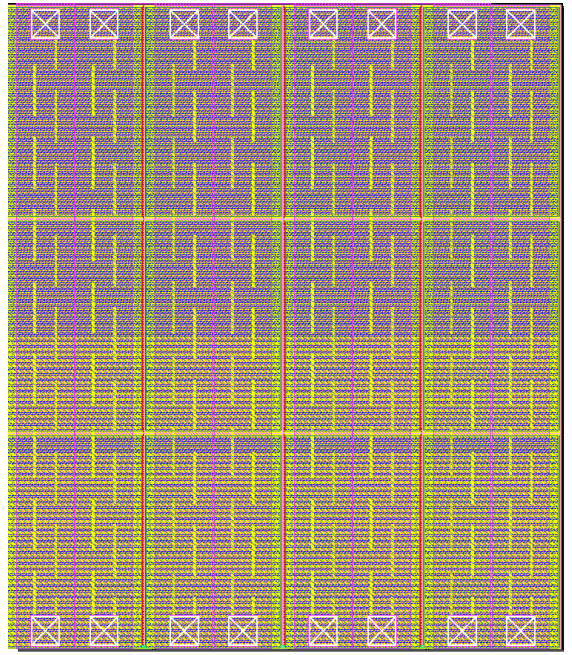
PDG is a software tool that automates the layout of power FETs.

- A set of inputs are provided to describe the desired FET.
- PDG can output a single layout, or it can explore the layout space and provide many layouts to identify the optimum one.





Power FET layouts include source, drain and gate connections, bond pads substrate / isolation rings and sense FET options

R3D (Power Device Analysis)

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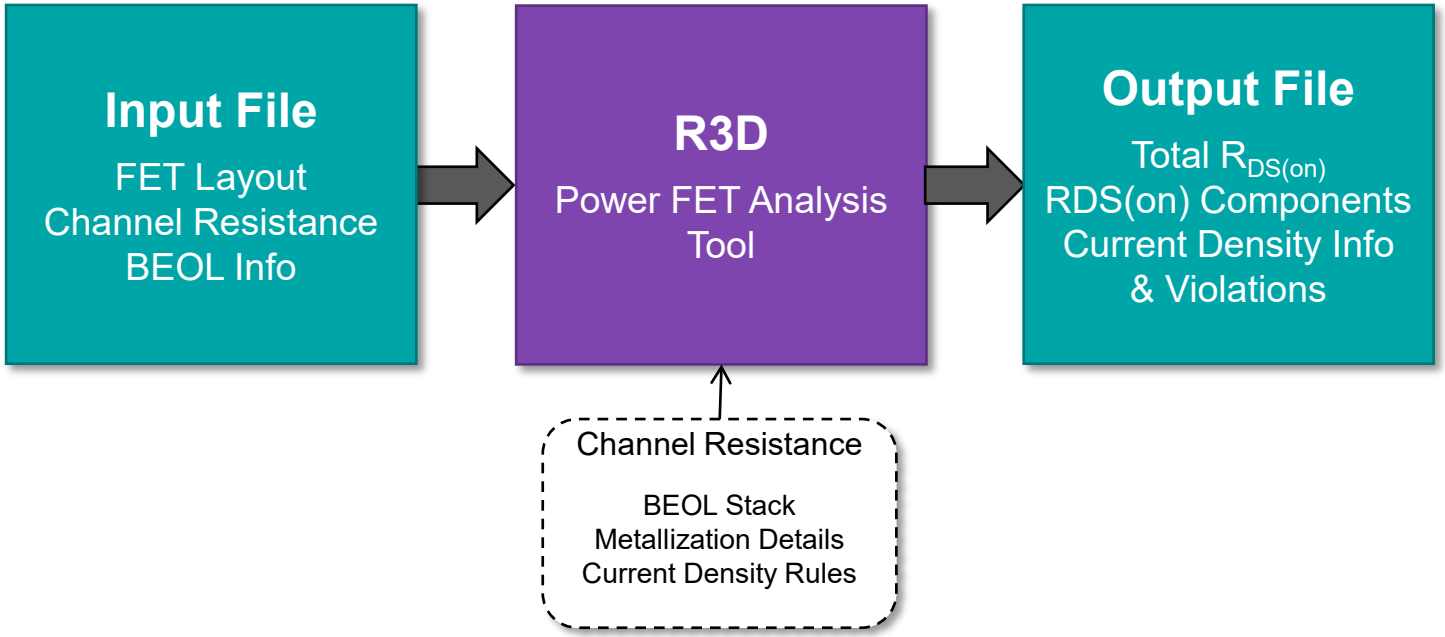
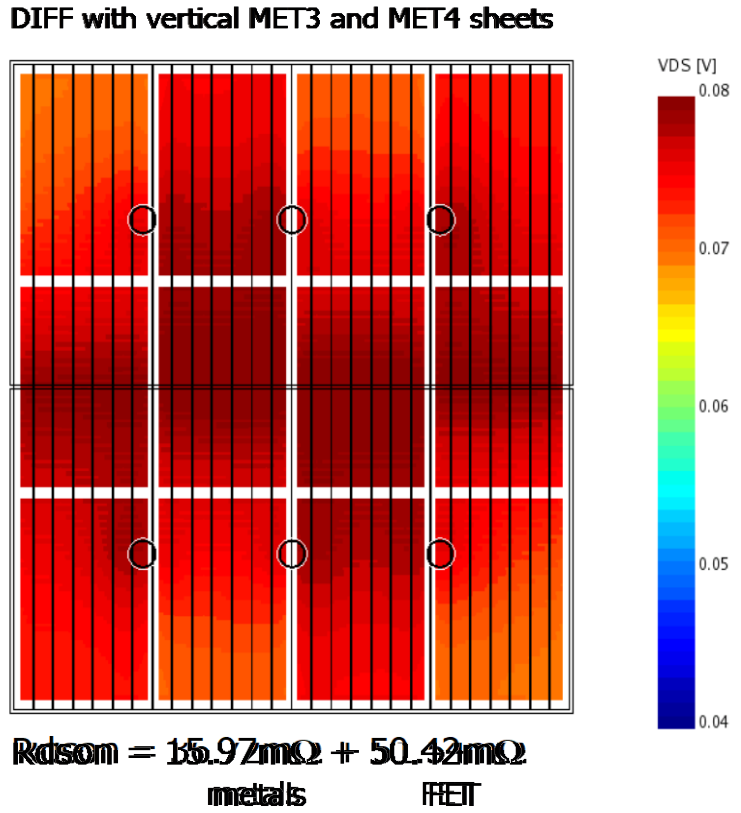
R3D is a software tool that analyzes the metal interconnects of power FETs.

- A complete power FET layout is provided to R3D as an input.
- R3D analyzes the layout and calculates the total $R_{DS(on)}$ and contributions from all parts of the Power FET metal bussing system.





Power FET Exploration

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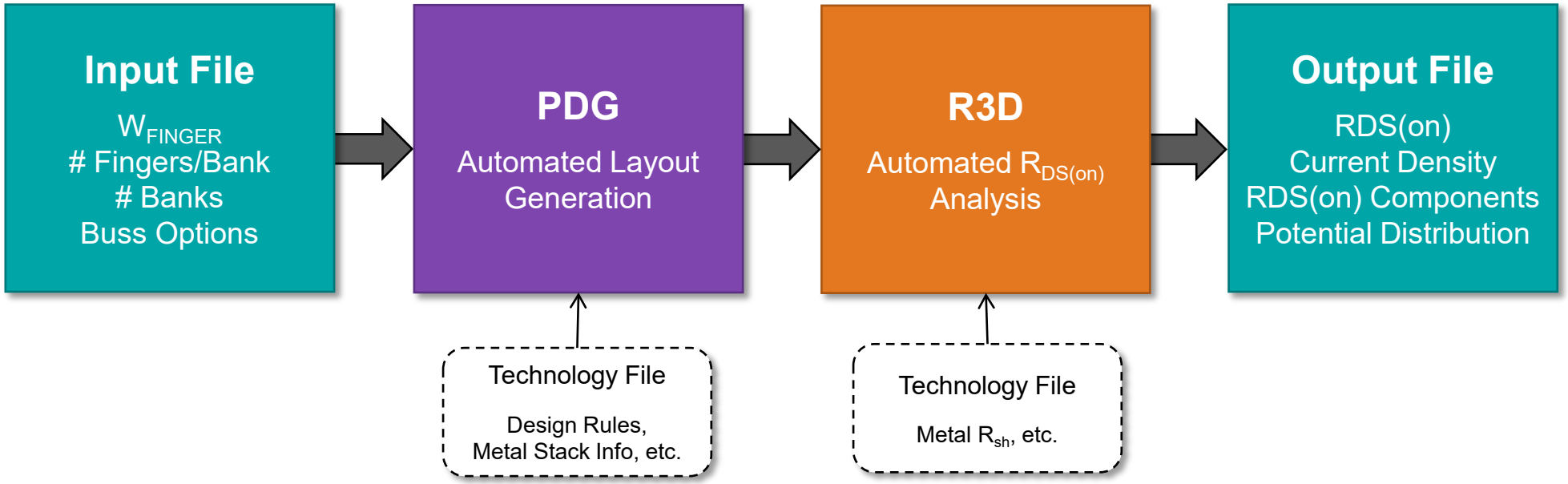
Automated Layout & Analysis in Seamless Flow – Single or Batch



Go from concept to complete layouts and RDS(on) estimates in minutes.

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Automated Power FET Generation

Metal Layer / Buss Strategy Exploration

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180nm BCD Process with Aluminum BEOL

- 3LM-5LM Options.
- Top metal is always thick.

Layer	Resistance
$R_{channel}$	3842 Ω•µm
CONT	14.5 Ω/cont
M1	125 mΩ/□
VIA1	5.5 Ω/via
M2	88 mΩ/□
VIA2	5.5 Ω/via
M3	88 mΩ/□
VIA3	5.5 Ω/via
M4	88 mΩ/□
VIA4	4.0 Ω/via
M5	10 mΩ/□

Metal Layer / Buss Strategy Exploration

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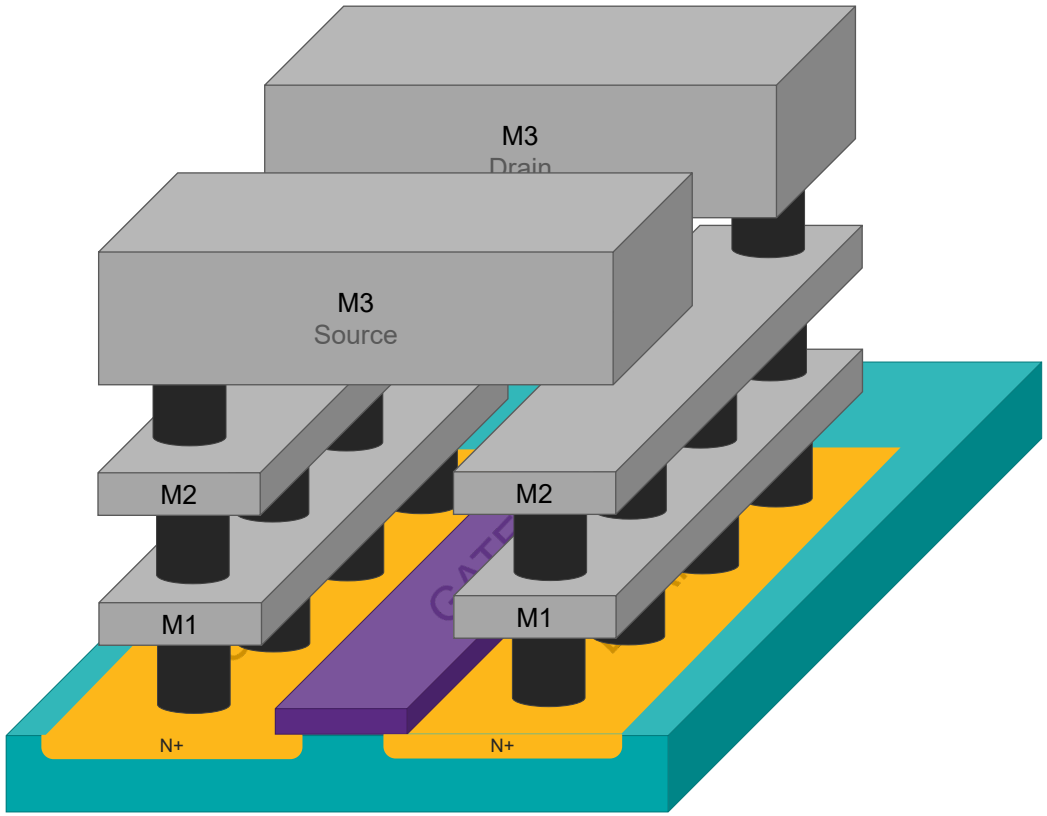
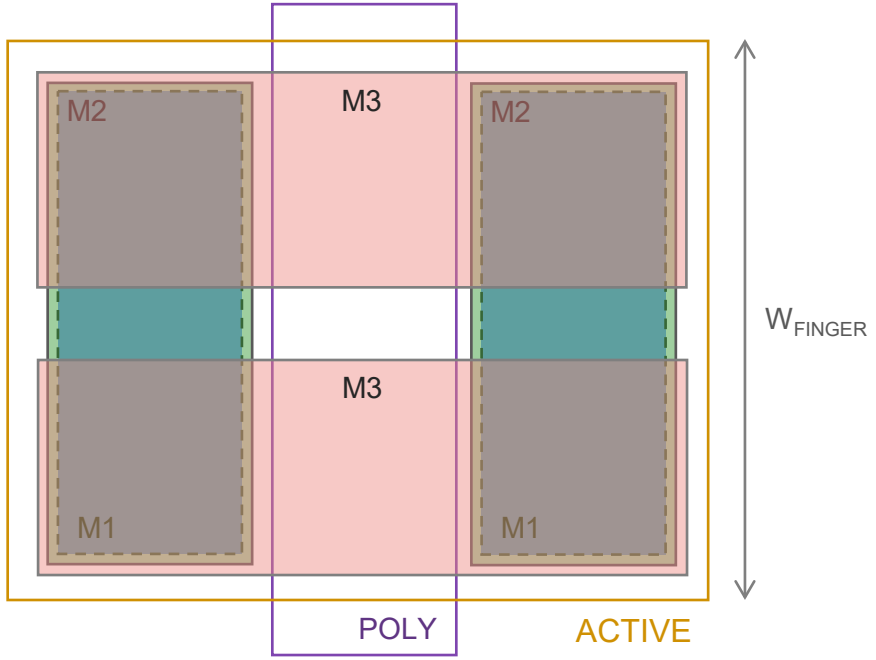
3LM Thick Metal: M1 || M2 ⊥ M3 (A-Style)

Physical View



Layout View



CONTACT and VIA not shown

Metal Layer / Buss Strategy Exploration

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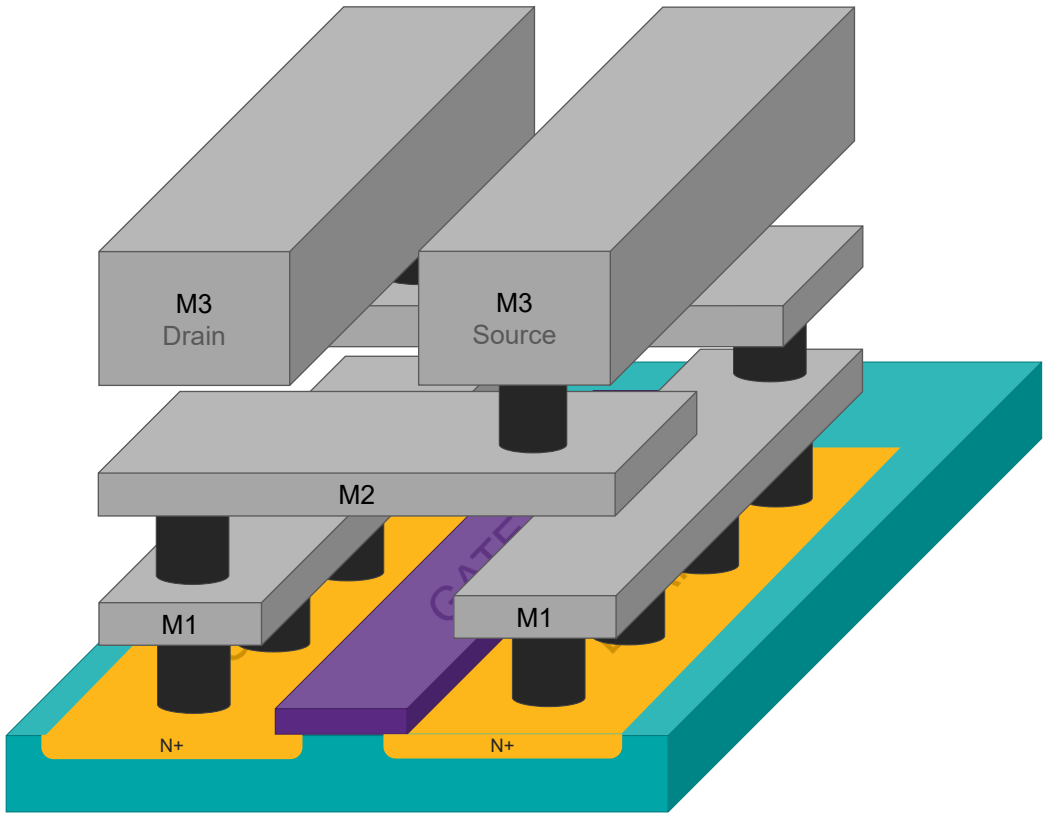
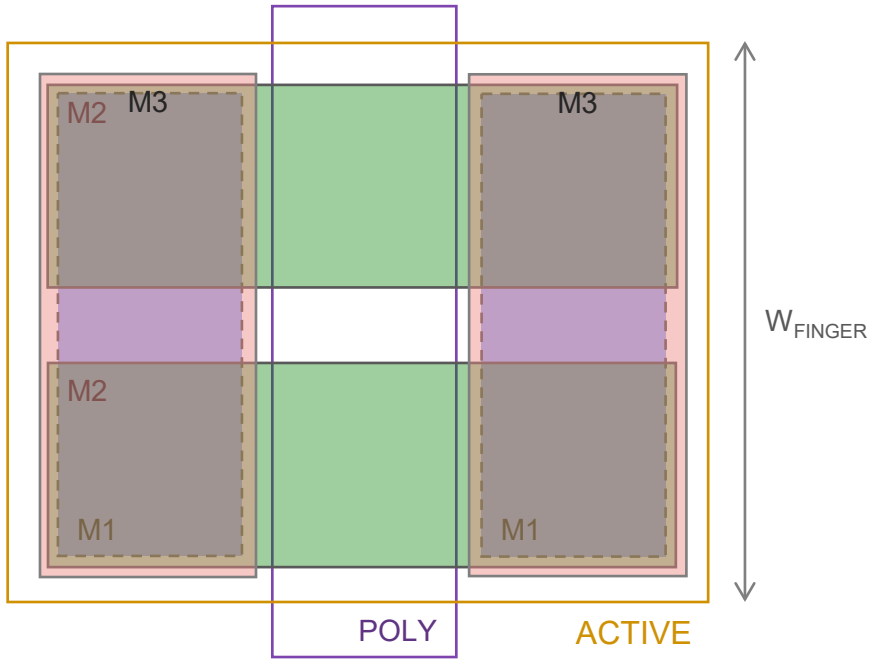
3LM Thick Metal: M1 ⊥ M2 ⊥ M3 (B-Style)

Physical View



Layout View



CONTACT and VIA not shown

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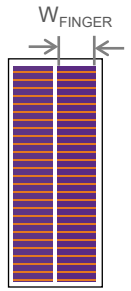
Metal Buss Options Explored in 3LM, 4LM and 5LM:

3LM	4LM	5LM
M1 ⊥ M2 ⊥ M3	M1 ⊥ M2 || M3 ⊥ M4	M1 ⊥ M2 || M3 || M4 ⊥ M5
M1 || M2 ⊥ M3	M1 || M2 || M3 ⊥ M4	M1 || M2 ⊥ M3 || M4 ⊥ M5
		M1 || M2 || M3 || M4 ⊥ M5

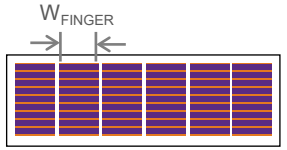
Transistor Options:

W_{FINGER} = 200µm
# of Fingers / Bank
Transistor Banks
Aspect Ratio

Example #1:
Aspect Ratio = 0.4
224 Fingers/Bank
2 Banks
Total Width = 89,600 µm
Area = 498,517 µm^2



Example #2:
Aspect Ratio = 3.46
74 Fingers/Bank
6 Banks
Total Width = 88,800 µm
Area = 510,554 µm^2



Power FET Exploration

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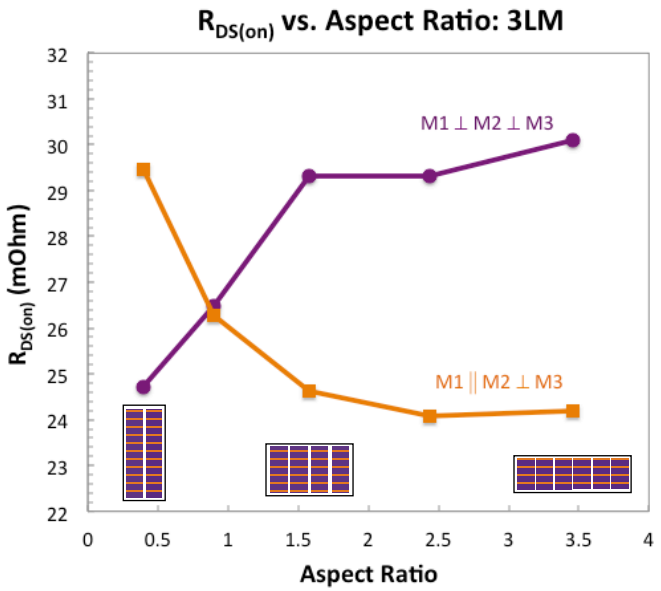
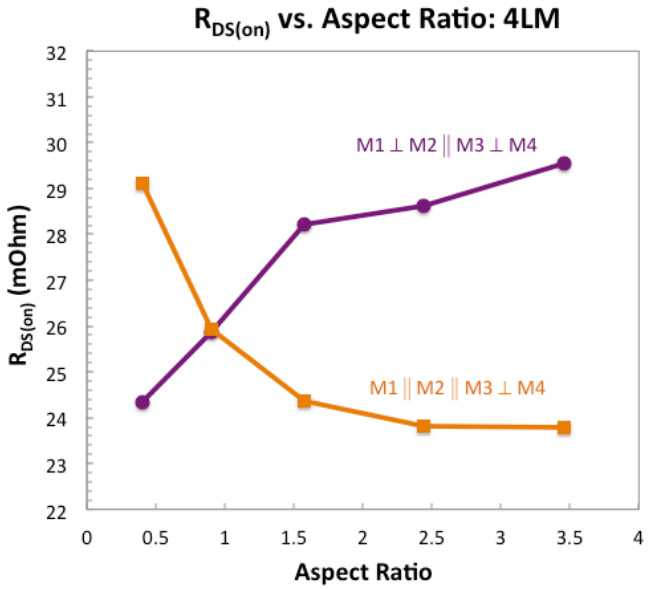
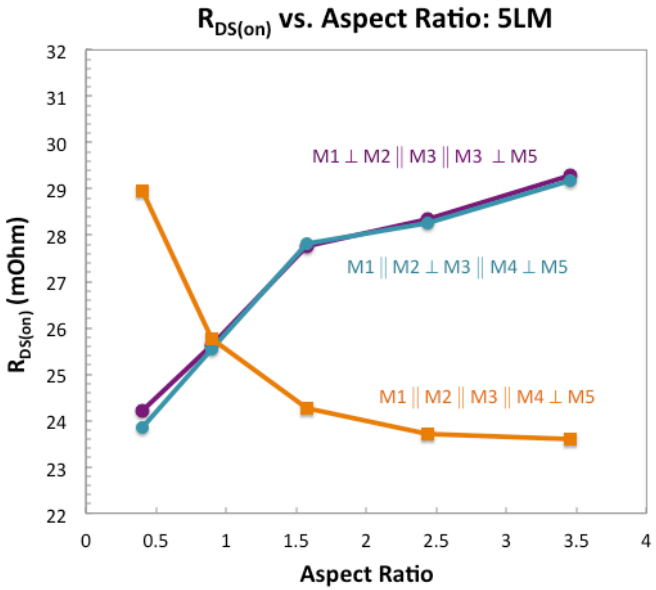
$R_{DS(on)}$ Analysis from Auto-Generated Layouts







35 layouts auto-Generated and analyzed with a run time of about 4 hours

Power FET Exploration

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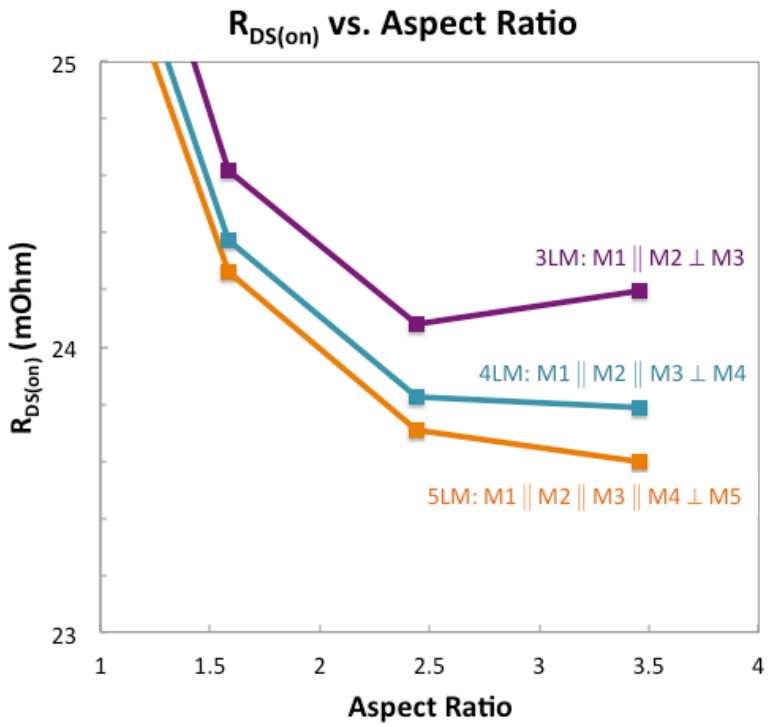
$R_{DS(on)}$ Analysis from Auto-Generated Layouts



4LM and 5LM deliver a marginal reduction in $R_{DS(on)}$ for these devices which may not offset the additional wafer cost.

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Automated Power FET Generation

Power FET Optimization

Optimization Approach

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Ran a Series of DOEs to Study Various Design/Process Sensitivities

DOE #	Purpose
1	Study impact of number of bond pads on $R_{DS(on)}$.
2	Study the B-style bussing options using 4LM on $R_{DS(on)}$.
3	Study the impact of M2 || M3 width on $R_{DS(on)}$.
4	Study the impact of the # of M4 busses on $R_{DS(on)}$ and J_{max}.
5	Study the impact of source bond pad placement on $R_{DS(on)}$.

Silicon Technology

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180nm BCD Process with Aluminum BEOL

- Key Electrical Parameters for 4LM Flow:

Layer	Resistance
$R_{channel}$	3842 Ω•µm
CONT	14.5 Ω/cont
M1	125 mΩ/□
VIA1	5.5 Ω/via
M2	88 mΩ/□
VIA2	5.5 Ω/via
M3	88 mΩ/□
VIA3	4.0 Ω/via
M4	10 mΩ/□

Structures Used for Optimization Studies

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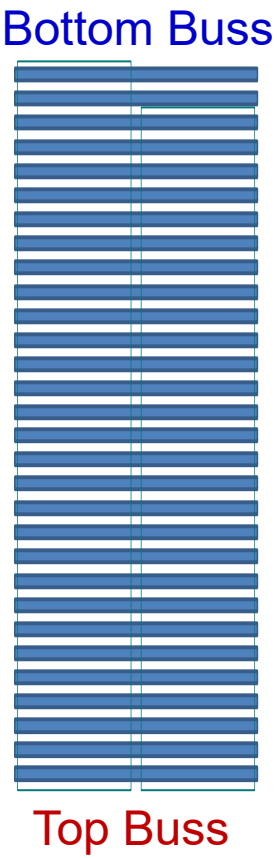
Two Primary Device Structures Used

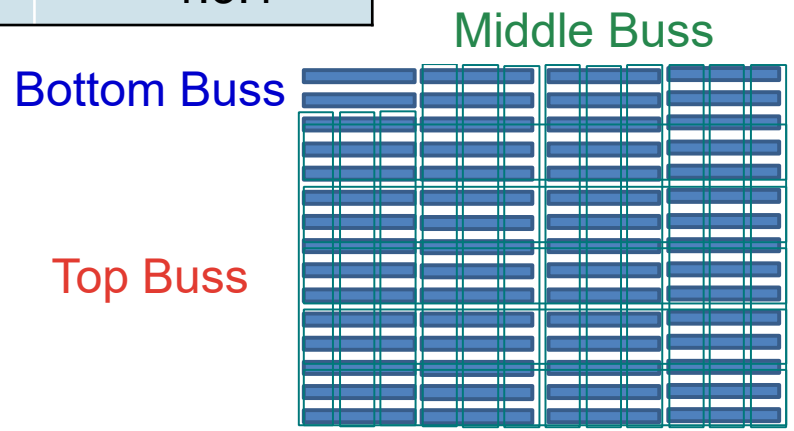
- A-style = (M1 || M2 || M3) ⊥ M4

Parameter	Value
Finger Width	200 µm
Finger Number	986
Area	~ 1 mm^2
Aspect Ratio	~ 0.25:1



- B2-style = M1 ⊥ (M2 || M3) ⊥ M4

Parameter	Value
Finger Width	200 µm
Finger Number	1028
Area	~ 1 mm^2
Aspect Ratio	~ 1.3:1



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DOE 1

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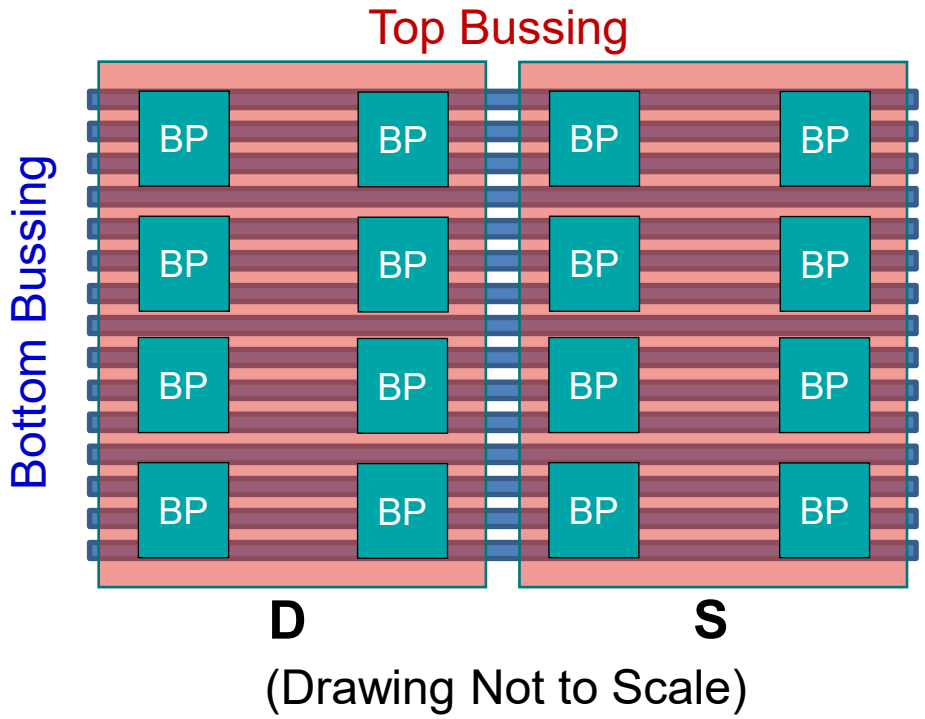
Study Impact of Bond Pad Count, Validate Tools

- DOE Purpose: Study impact of bond pad number on $R_{DS(on)}$
- A-style Buss Option: (M1 || M2 || M3) ⊥ M4

Pads	Pad Arrangement
20	20 S, 20 D
12	12 S, 12 D
6	6 S, 6 D
4	4 S, 4 D



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DOE 1 (cont)

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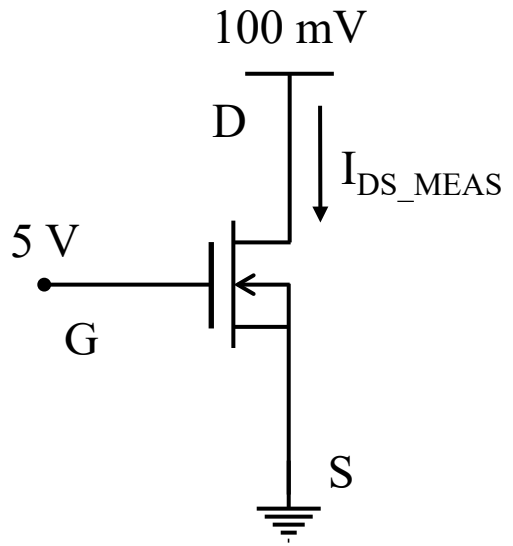
Study Impact of Bond Pad Count, Validate Tools

- PDG/R3D Results:

Bond Pads	I_{DS_MEAS}	$R_{DS(on)}$
20 S, 20 D	7.65 A	13.08 mΩ
12 S, 12 D	6.53 A	15.31 mΩ
6 S, 6 D	4.43 A	22.60 mΩ
4S, 4 D	3.12 A	32.10 mΩ

- Simulation Results: $R_{DS(on)}$ (4+4) / $R_{DS(on)}$ (20+20) ≈ 2.4
- Silicon Results: $R_{DS(on)}$ (4+4) / $R_{DS(on)}$ (20+20) ≈ 2.1



$R_{DS(on)} = 100\ mV / I_{DS\_MEAS}$

DOE 1 (cont)

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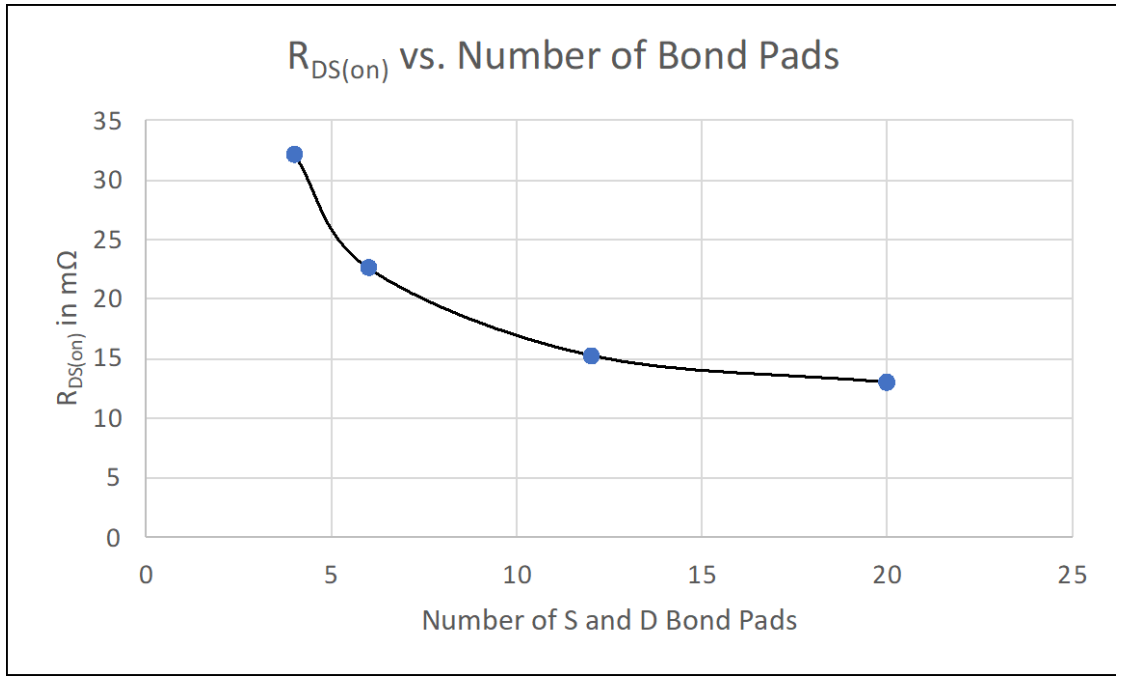
Study Impact of Bond Pad Count, Validate Tools

- DOE Conclusions:
  - Major impact of bond pad number on $R_{DS(on)}$ (~50%).
  - Good correlation between PDG/R3D simulations and silicon results.



DOE 2

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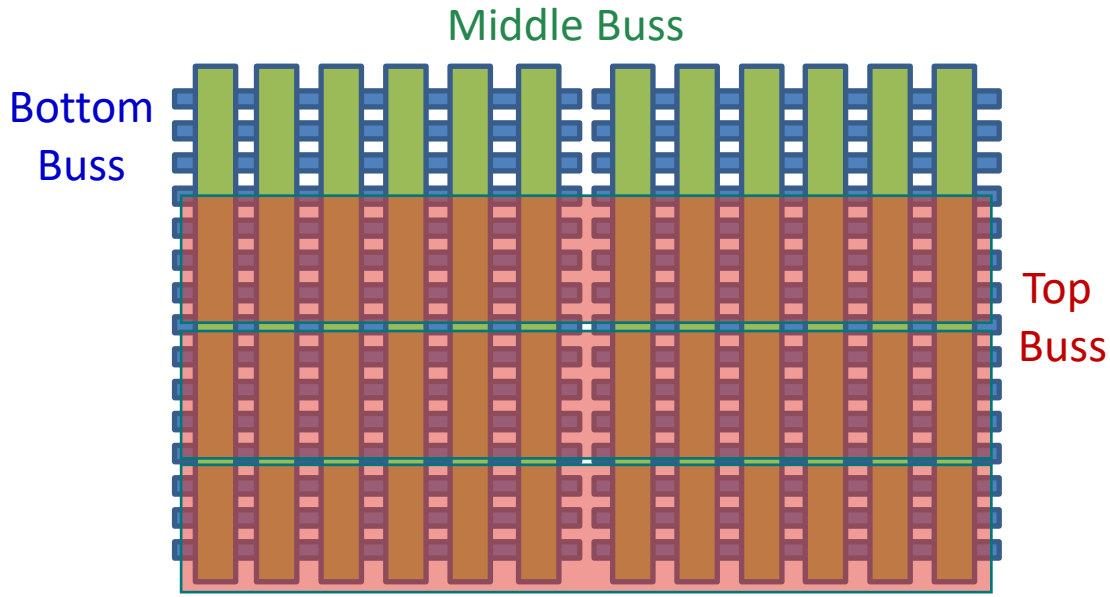
Study 4LM B-style Buss Options

- DOE Purpose: Study the B-style bussing options using 4LM on $R_{DS(on)}$
- B-style Buss Options:

Buss Option	Buss Strategy
B-Style	Bottom ⊥ Middle ⊥ Top
B1	(M1 || M2) ⊥ M3 ⊥ M4
B2	M1 ⊥ (M2 || M3) ⊥ M4
B3	M1 ⊥ M2 ⊥ (M3 || M4)



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DOE 2 (cont)

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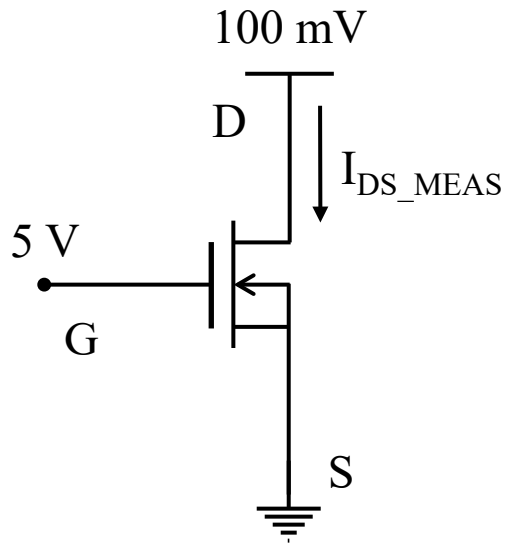
Study 4LM B-style Buss Options

- PDG/R3D Results:

Buss Style	I_{DS_MEAS}	$R_{DS(on)}$
B1	10.31 A	9.70 mΩ
B2	10.41 A	9.61 mΩ
B3	10.33 A	9.68 mΩ

- B2 Silicon Results: 9.64 mΩ



$R_{DS(on)} = 100\ mV / I_{DS\_MEAS}$

DOE 2 (cont)

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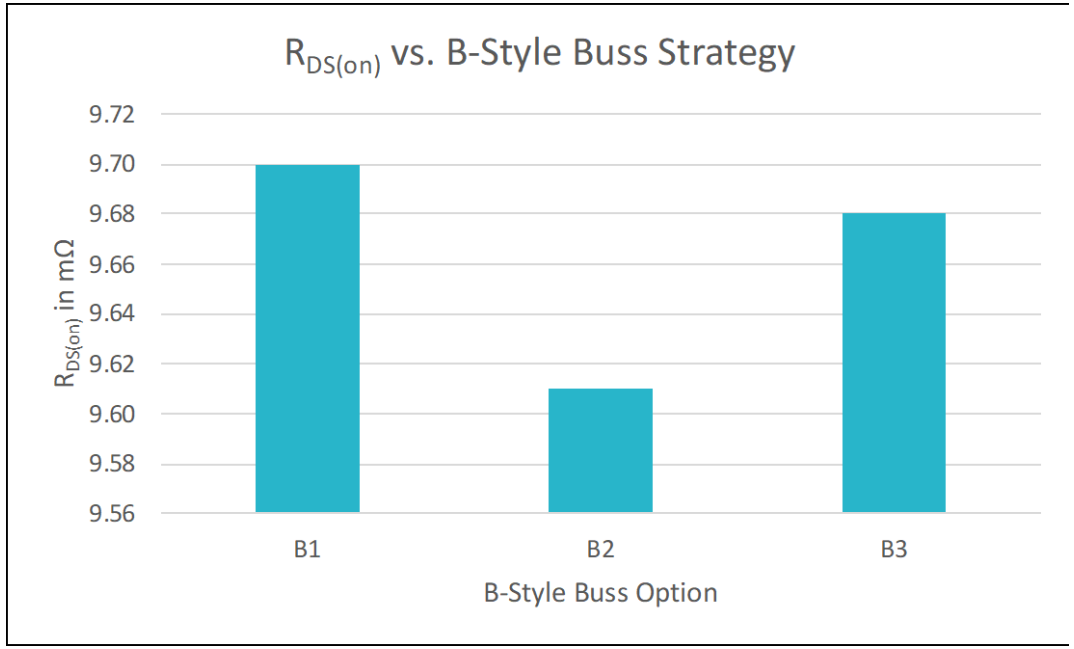
Study 4LM B-style Buss Options

- DOE Conclusions:
  - Minor impact of B-style bussing approach on $R_{DS(on)}$ (~1%)
  - B2-style bussing gives best result, albeit small effect
  - Very good correlation between PDG/R3D simulations and silicon results



DOE 3

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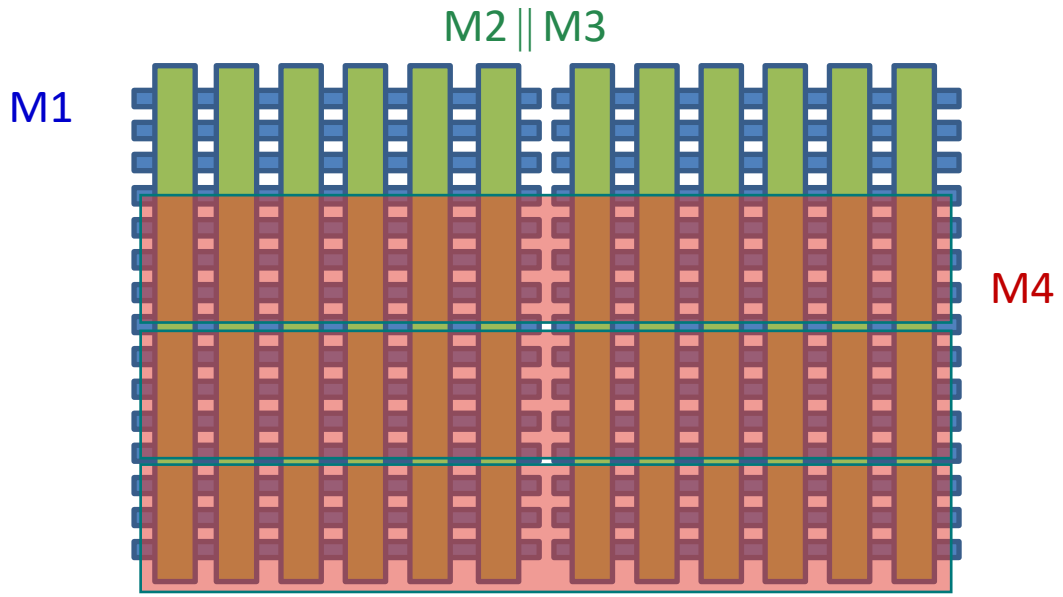
M2 || M3 Width Sensitivity in 4LM B2-style Buss Strategy

- DOE Purpose: Study the impact of M2 || M3 width on $R_{DS(on)}$
- B2-style buss strategy: M1 ⊥ (M2 || M3) ⊥ M4

M2 Width	M3 Width
2 µm	2 µm
10 µm	10 µm
18 µm	18 µm
22 µm	22 µm
26 µm	26 µm
34 µm	34 µm
42 µm	42 µm



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DOE 3 (cont)

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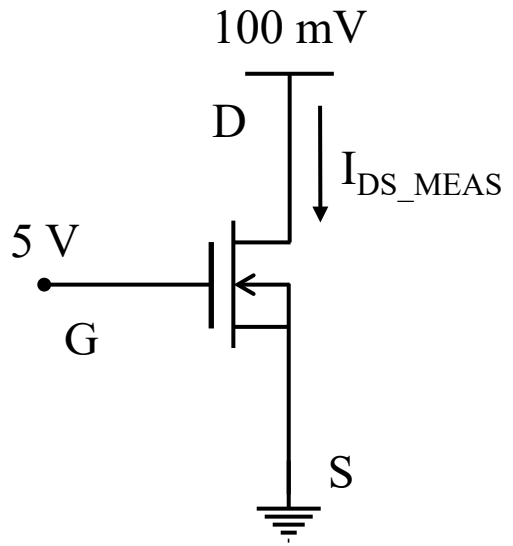
M2 || M3 Width Sensitivity in 4LM B2-style Buss Strategy

- PDG/R3D Results:

M2 %M3 Width	I_{DS_MEAS}	$R_{DS(on)}$
2 µm	10.33 A	9.69 mΩ
10 µm	10.39 A	9.63 mΩ
18 µm	10.40 A	9.62 mΩ
22 µm	10.40 A	9.62 mΩ
26 µm	10.39 A	9.63 mΩ
34 µm	10.38 A	9.64 mΩ
42 µm	10.35 A	9.66 mΩ



$R_{DS(on)} = 100\ mV / I_{DS\_MEAS}$

- Silicon Results: 9.64 mΩ

DOE 3 (cont)

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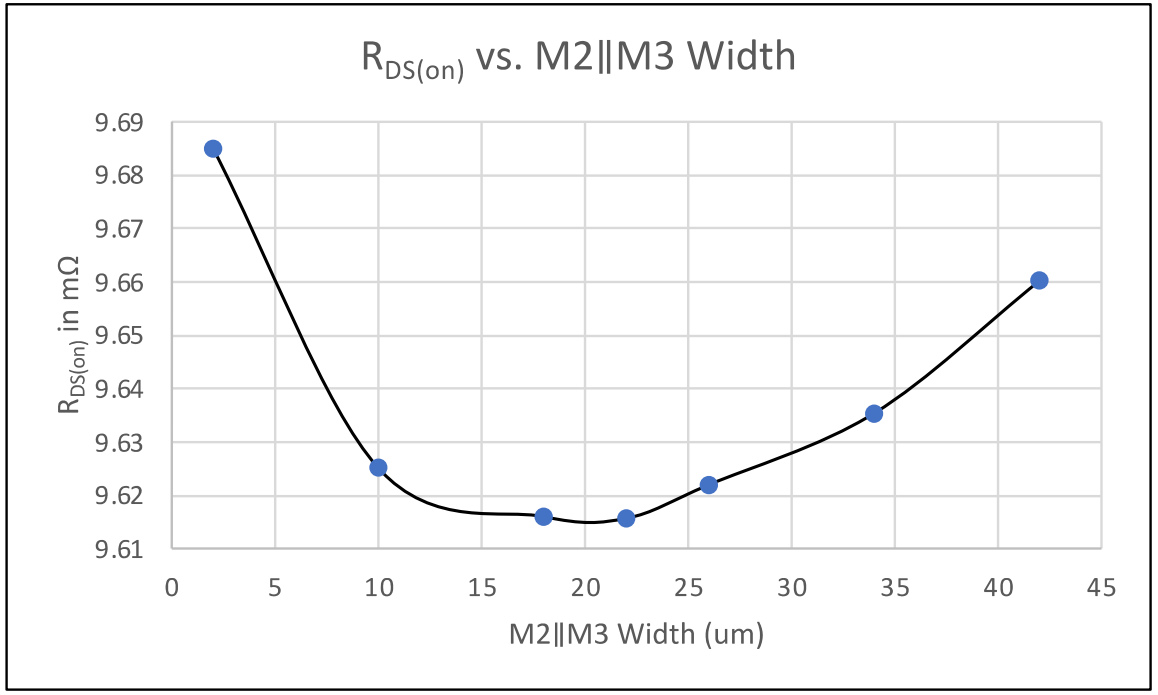
M2 || M3 Width Sensitivity in 4LM B2-style Buss Strategy

- DOE Conclusions:
  - Minor impact of M2 || M3 width on $R_{DS(on)}$ (~1%)
  - Middle buss width ~20 µm gives best result
  - Very close matching to silicon results



DOE 4

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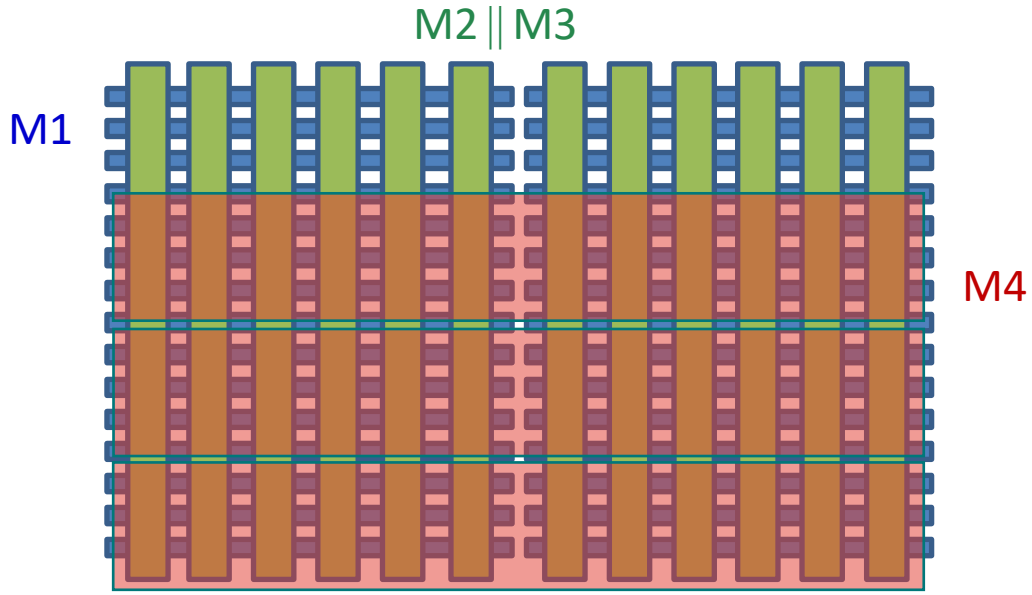
Impact of M4 Buss Number/Width in 4LM Buss Strategy

- DOE Purpose: Study the impact of the number of M4 busses, and their width, on $R_{DS(on)}$ and J_{max} violations.
- B2-style buss strategy: M1 ⊥ (M2 || M3) ⊥ M4

M4 Buss #	M4 Buss Width	S & D Pads
2	655 µm	6S , 6D
2	655 µm	8S , 8D
4	323 µm	8S , 8D
8	155 µm	8S , 8D
12	107 µm	12S , 12D



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DOE 4 (cont)

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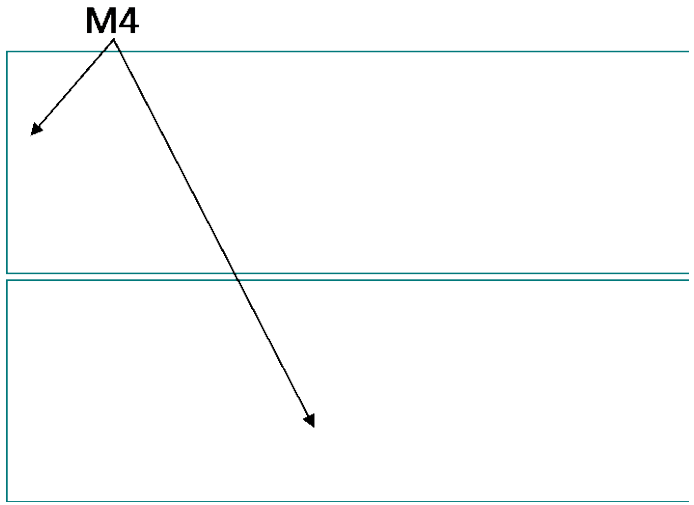
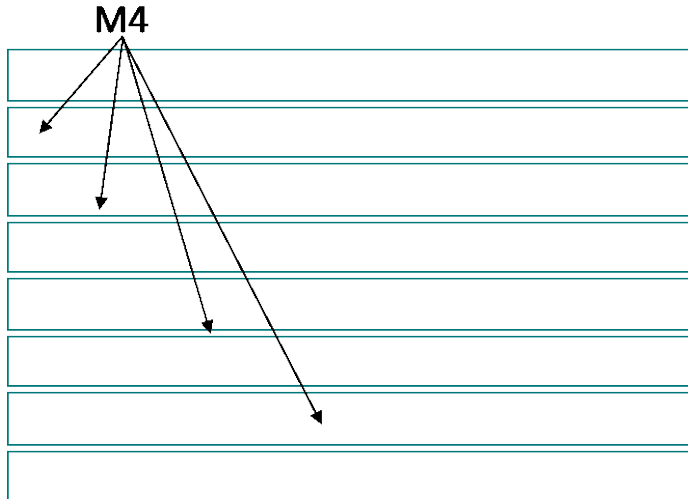
Impact of M4 Buss Number/Width in 4LM Buss Strategy

- M4 Buss Options:

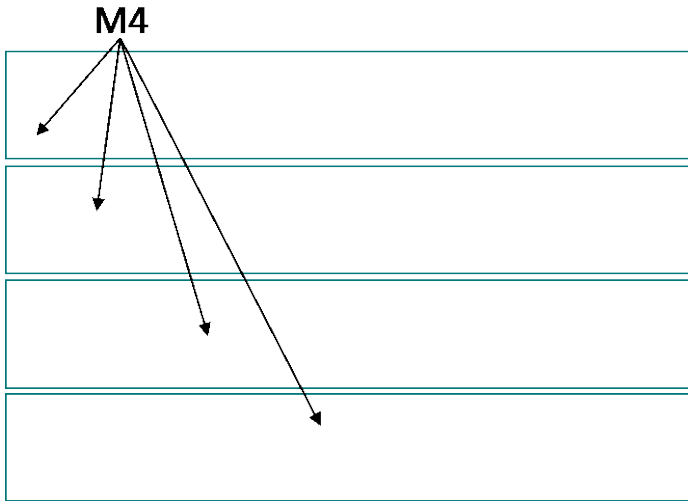
2 M4 Busses

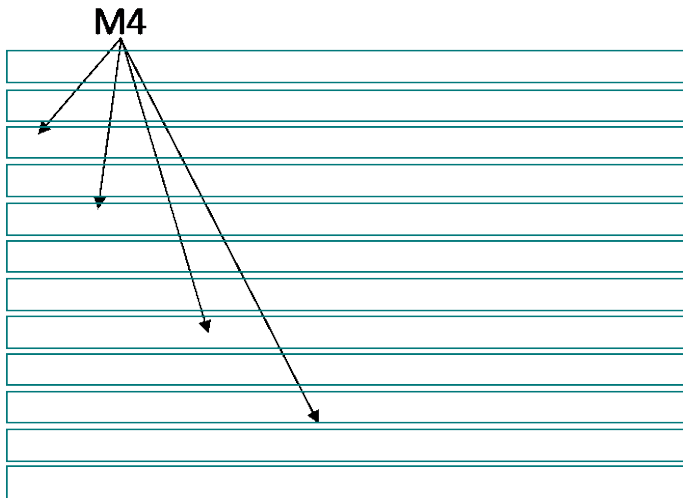




8 M4 Busses

4 M4 Busses





12 M4 Busses

DOE 4 (cont)

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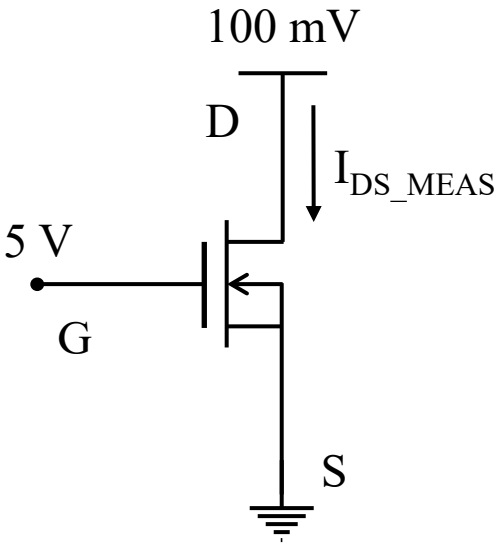
Impact of M4 Buss Number/Width in 4LM Buss Strategy

- PDG/R3D Results:

M4 Buss #	M4 Buss Width	S & D Pads	I_{DS_MEAS}	$R_{DS(on)}$	# J_{max} Violations
2	655 µm	6S, 6D	4.92 A	20.3 mΩ	1039
2	655 µm	8S, 8D	4.96 A	20.2 mΩ	1036
4	323 µm	8S, 8D	8.69 A	11.5 mΩ	245
8	155 µm	8S, 8D	10.0 A	9.98 mΩ	77
12	107 µm	12S, 12D	10.4 A	9.65 mΩ	17



– Analysis focused on red section since all had constant 8S + 8D pads.

$R_{DS(on)} = 100\ mV / I_{DS\_MEAS}$

DOE 4 (cont)

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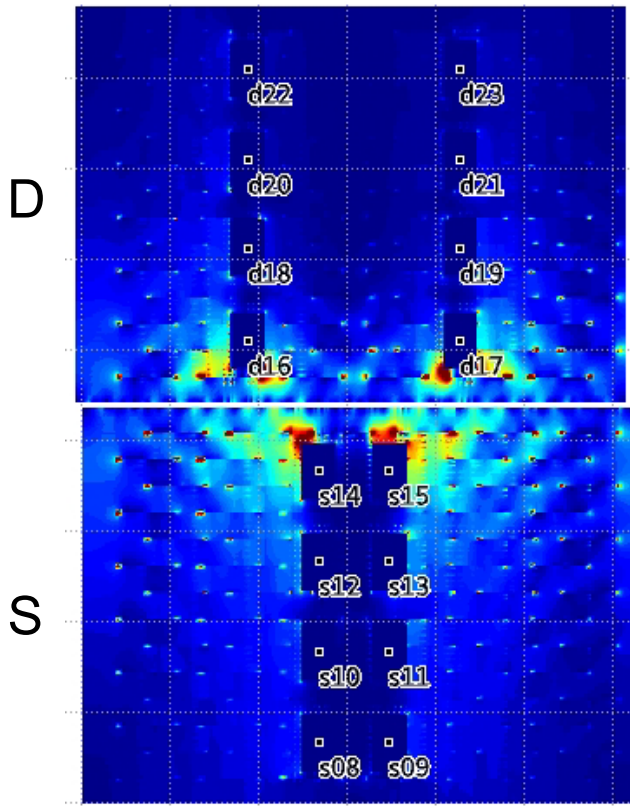
Impact of M4 Buss Number/Width in 4LM Buss Strategy

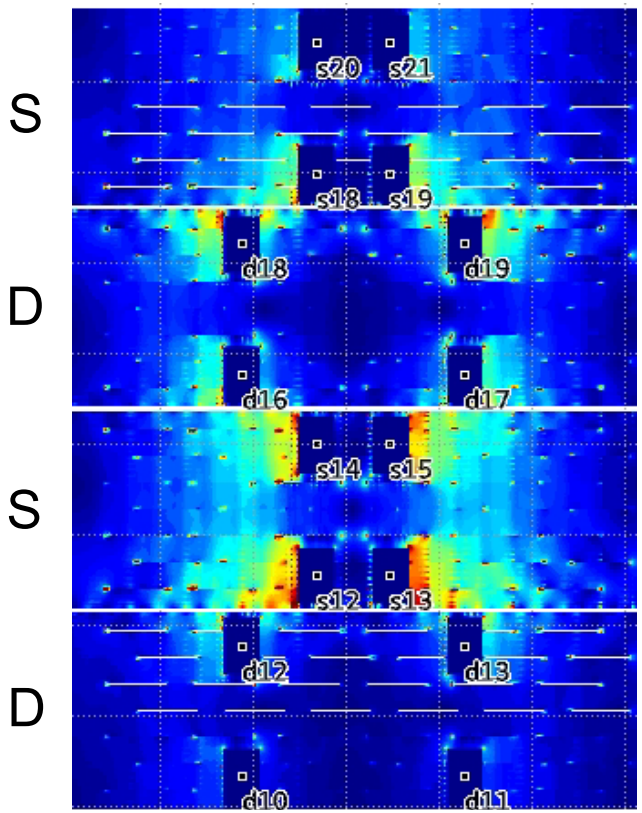
- Visual Look at J_{max} Violations (all with 8S + 8D pads):

2-Buss M4



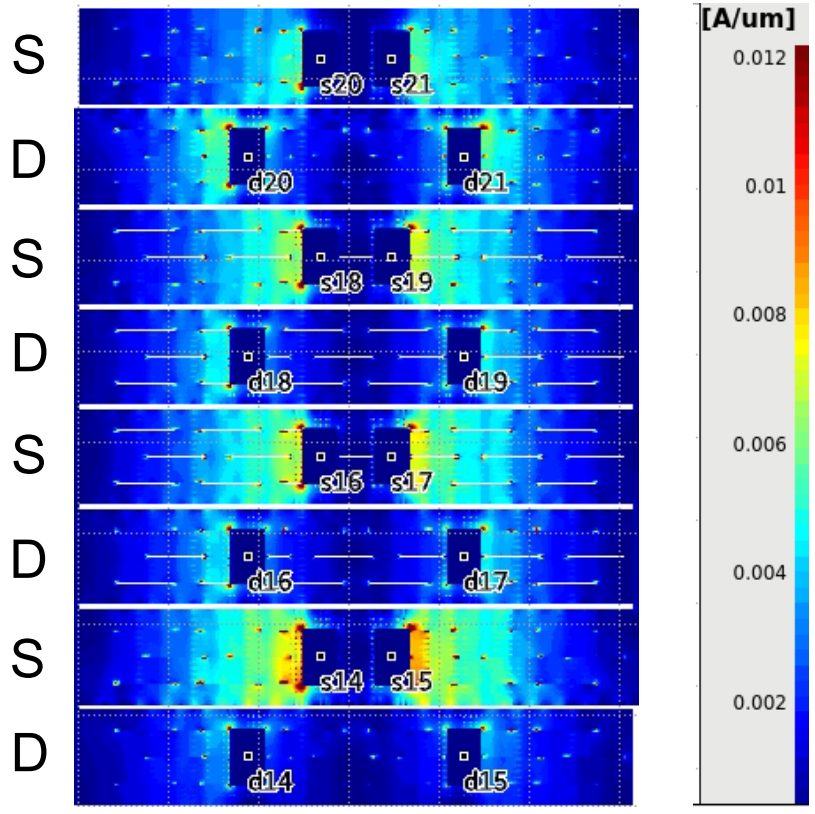
1036 Violations

4-Buss M4



245 Violations

8-Buss M4



77 Violations

DOE 4 (cont)

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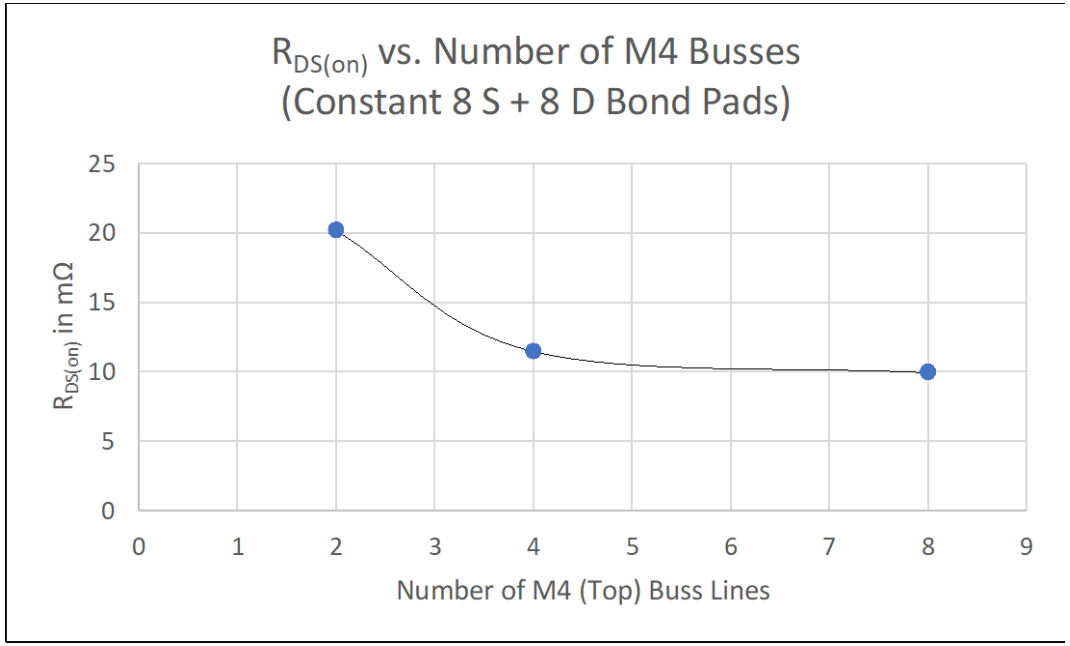
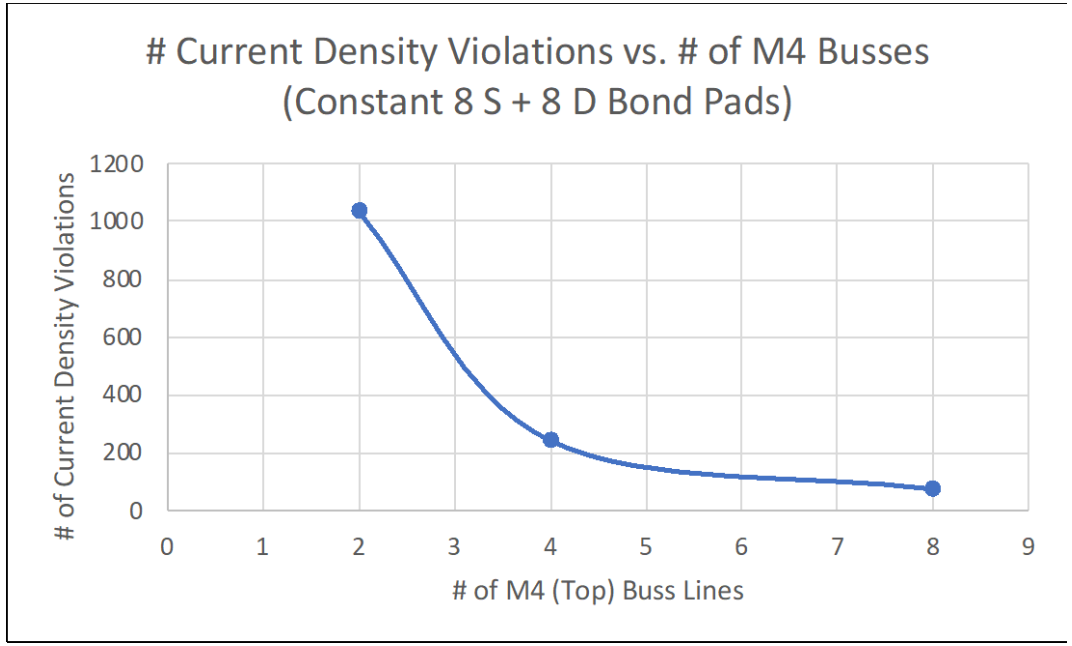
Impact of M4 Buss Number/Width in 4LM Buss Strategy

- DOE Conclusions:
  - Major impact from M4 buss number on $R_{DS(on)}$ (~50%).
  - Significant impact from more M4 busses on current density violations (~90%).
    - Note: The goal of this DOE was not to get to zero violations, but to show sensitivity to design/process factors.





DOE 5

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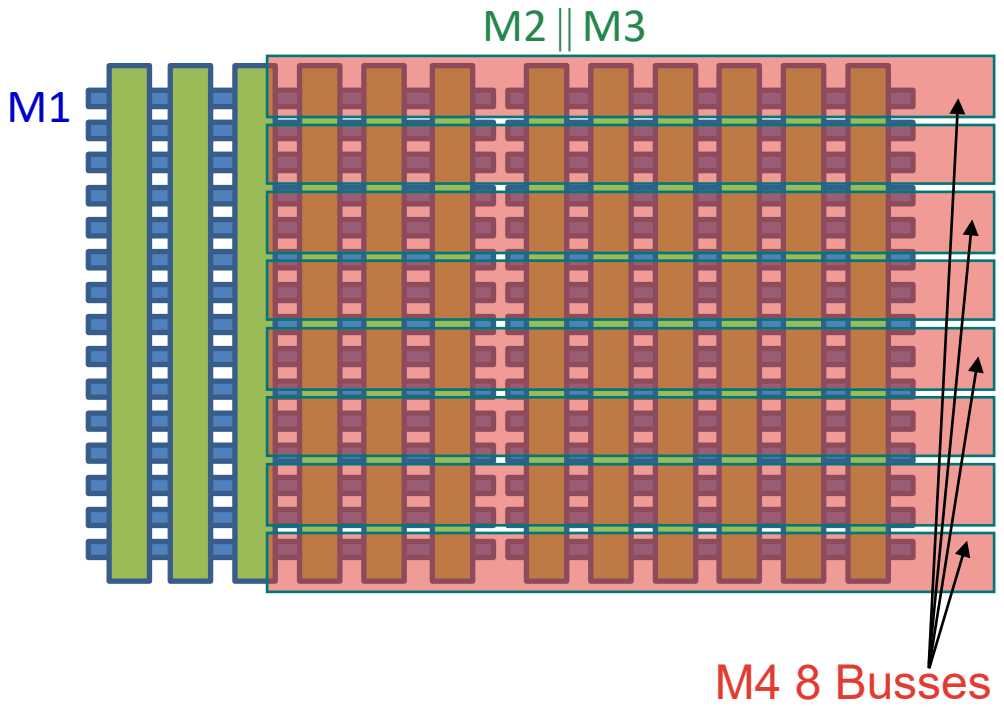
Bond Pad Displacement Study

- DOE Purpose: Study the impact of source bond pad displacement on $R_{DS(on)}$.
- B2-style buss strategy: M1 ⊥ (M2 || M3) ⊥ M4 (8 busses)

Pad Displacement Distance	Direction of Displacement
10 µm	Toward Center
30 µm	Toward Center
70 µm	Toward Center
130 µm	Toward Center

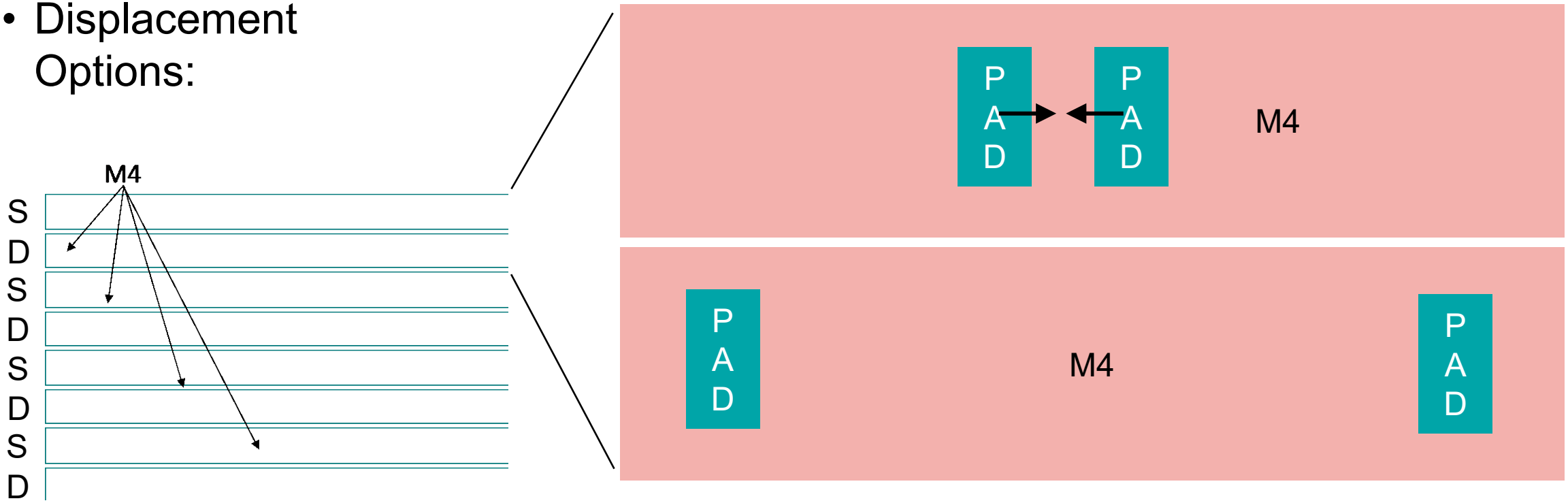


Note: M4 busses shifted to right to enable better viewing.

DOE 5 (cont)

Bond Pad Displacement Study

- Displacement Options:



DOE 5 (cont)

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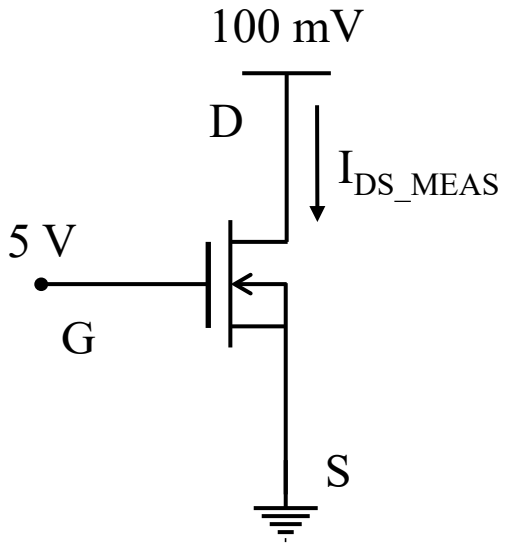
Bond Pad Displacement Study

- PDG/R3D Results:

Source Pad Displacement Distance	I_{DS_MEAS}	$R_{DS(on)}$
10 µm	9.90 A	10.1 mΩ
30 µm	9.95 A	10.0 mΩ
70 µm	10.1 A	9.95 mΩ
130 µm	10.2 A	9.82 mΩ



$R_{DS(on)} = 100\ mV / I_{DS\_MEAS}$

DOE 5 (cont)

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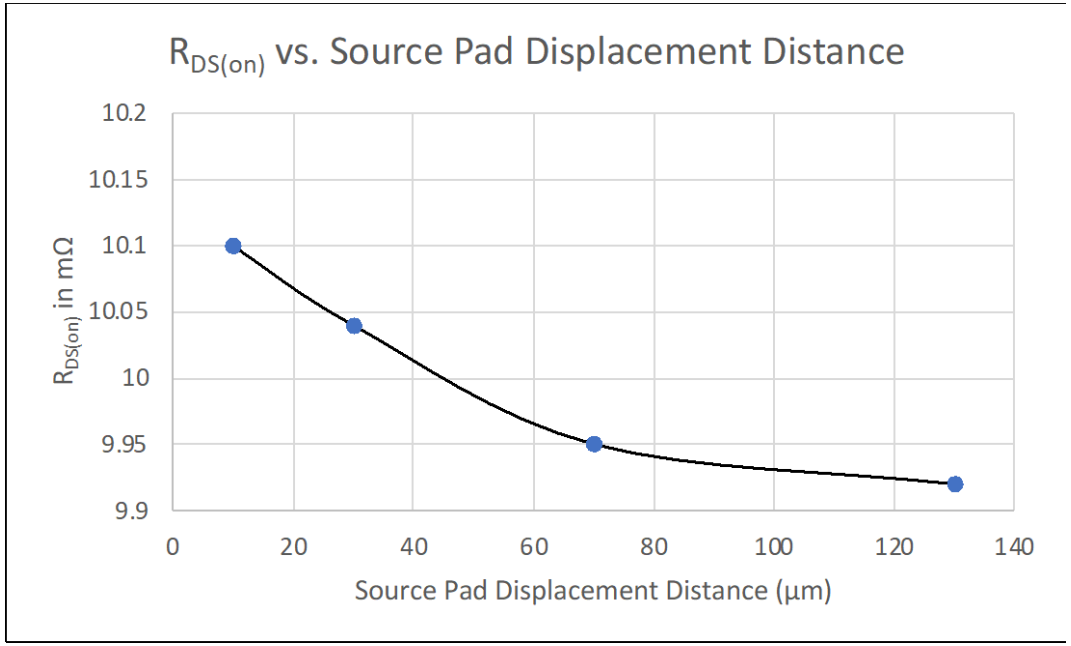
Bond Pad Displacement Study

- DOE Conclusions:
  - Meaningful impact from source pad placement (3% impact).
  - PDG/R3D enables bond pad placement optimization around pre-set positions (either a single pad moved independently, or all pads moved in tandem).



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Automated Power FET Generation

Conclusions and Future Work

Conclusions

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- Demonstrated a flow to auto-generate layouts and analyze $R_{DS(on)}$ of Power FET devices.
  - Fast: 35 large ($W_{Total} \approx 89{,}000$ µm) device layouts created and analyzed in 4 run hours
  - Easy: Can be run in batch mode to minimize user intervention
- Explored 3LM/4LM/5LM BEOL and Metal Bussing Strategy with Detailed DOEs.
- Identified layout parameters with improved $R_{DS(on)}$ and current uniformity.
  - Increased number of top metal busses improved both $R_{DS(on)}$ and current density violations.
  - Increased number of bond pads improved $R_{DS(on)}$.
- PDG/R3D flow enables the layout engineer to explore and optimize to squeeze performance and die size.

Future Work

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- Broaden optimization space beyond area and $R_{DS(on)}$. Envision weighted optimization objective functions that incorporate factors such as:
  - Current uniformity
  - Capacitance
  - Reliability e.g. electromigration (new feature!)
  - Thermal – absolute and uniformity
- Systematically explore buss tapering
- Expand to important new power device technologies GaN and SiC


THANK YOU
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