PV Signoff and productivity feature for sub nm nodes

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Meta

Agenda

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- Overview of Meta
- ICV flow at Meta
- ICV Productivity flows and use models
  - Layer Debugger
  - LVS short finder
  - ICV Explorer

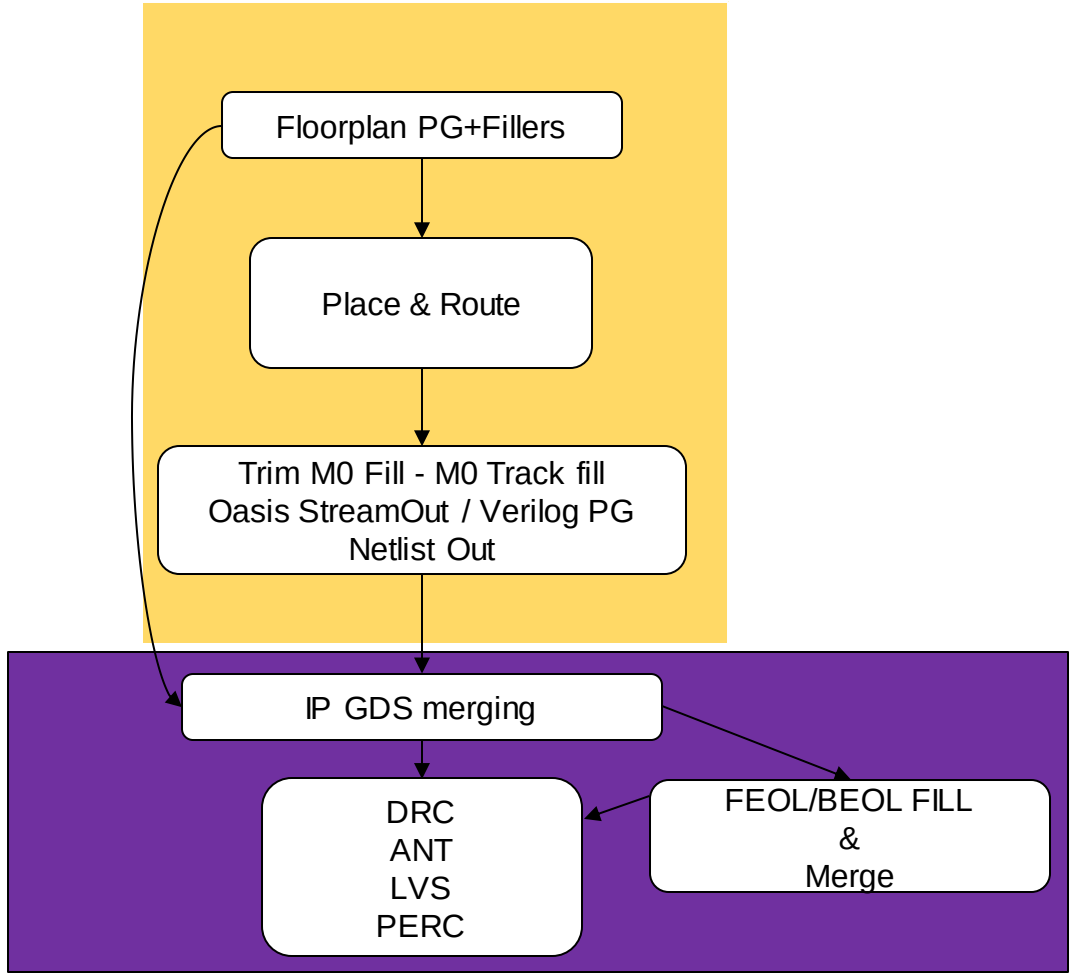
Meta Overview

- Meta Platforms, Inc. builds technology that helps people connect and share and grow business.

- Meta Infra silicon team
  - Designs and develop ASICs to Supports AI workloads and infrastructure demands.

PV Signoff Flow

PDV Flow at Meta



ICV Flows

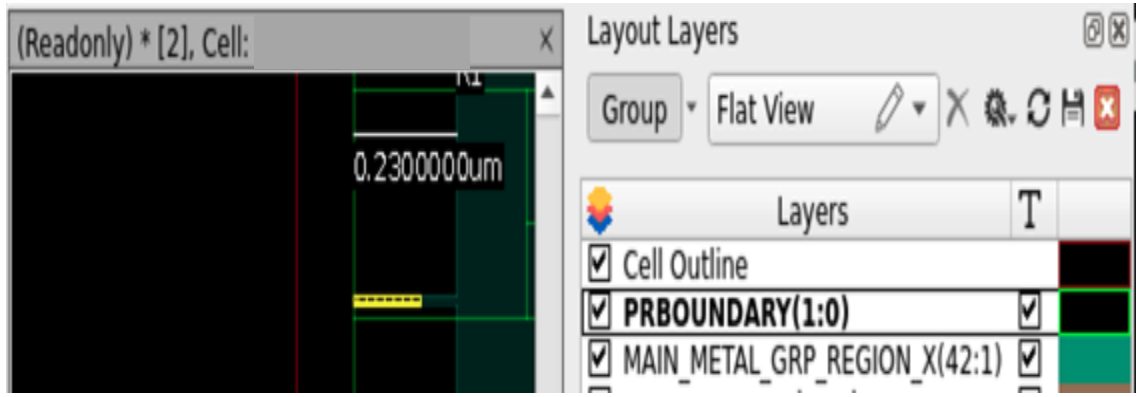
ICV Productivity Flows

Layer Debugger

ICV Productivity flows and use models

Layer debugger

- The Layer Debugger is a utility that provides a simple graphical method to debug layer creation in a runset.
- Use models: Debug complex DRC rules by generating intermediate layers.
- add -layer_debugger option in cmd file
- add -svc "M*.EN.2 *" option for particular drc debug in cmd file



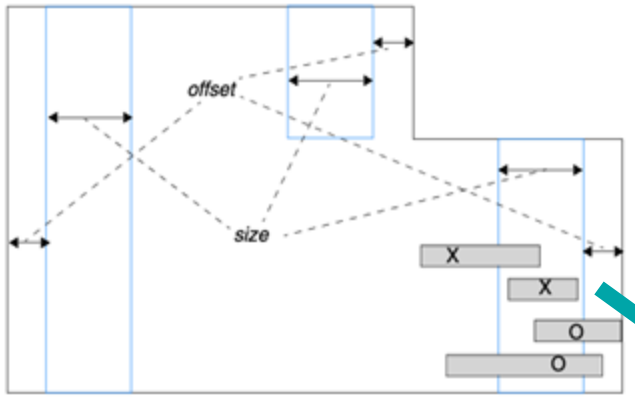
Layer debugger : Metal enclosure violations flagged by ICV ruleset but not by PnR tool

```
PROPERTY LEF58_BOUNDARYEOLBLOCKAGE "BOUNDARYEOLBLOCKAGE 0.1055 OFFSET 0.1485 PARALLEL 0.2505 WITHIN 0.2295 SPACING 0.2505 ; " ;
```

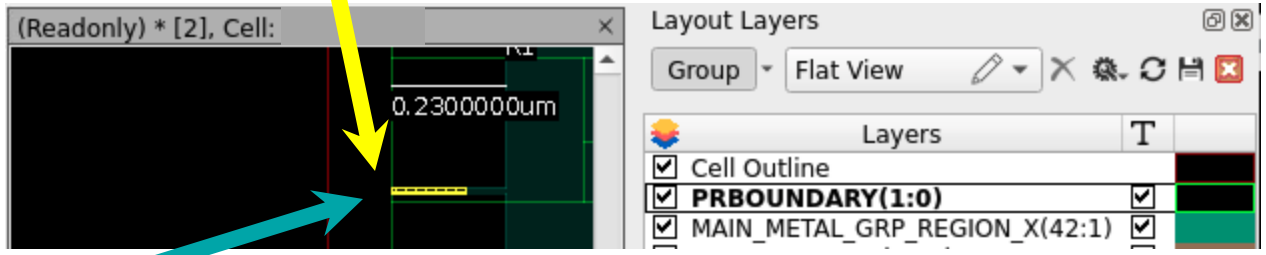
Root-cause: TECHLEF increase of BoundaryEOLBlockage OFFSET by 24nm

LEF/DEF 5.8 Language Reference
LEF Syntax - Layer (Routing)

Figure 5-25 Illustration of the Boundary EOL Blockage Rule



BoundaryEOLBlockage SIZE (0.1055) + OFFSET (0.1485) != M2_EN_19_2_SZ1

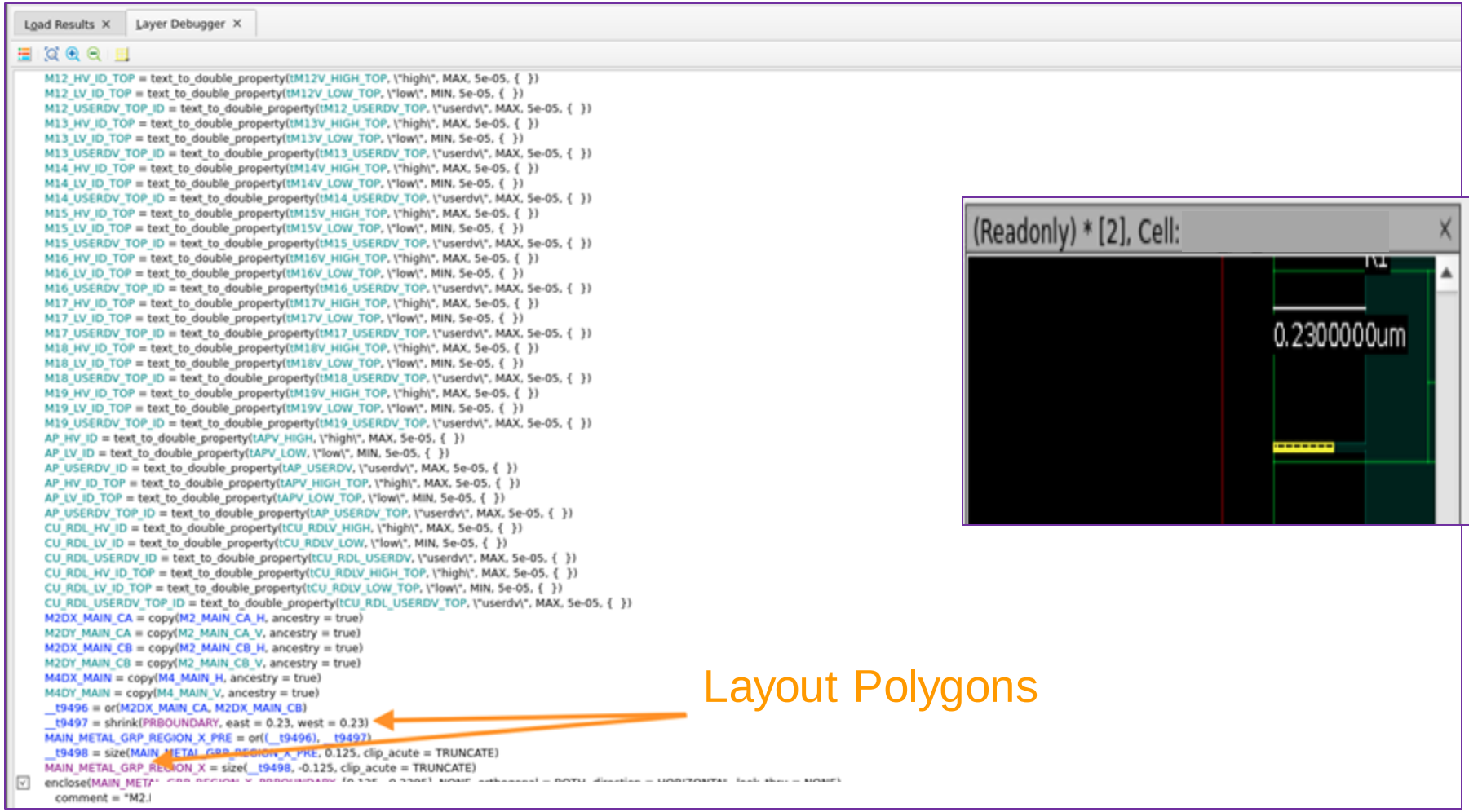


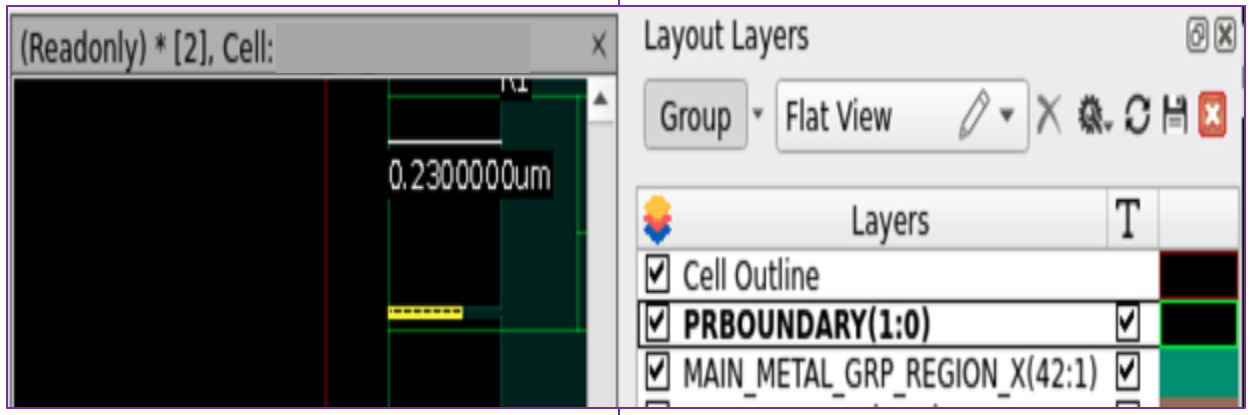
Layout polygons & violation marker

```
VARIABLE M2_EN_19_2_SZ1 0.2300
VARIABLE M2_EN_19_2_SZ2 0.1250
VARIABLE                0.1250
VARIABLE                0.2295

Main_M2_NMINP_GRP_Region_pre_x = OR M2dx_main ( SHRINK prBoundary RIGHT BY M2_EN_19_2_SZ1 LEFT BY M2_EN_19_2_SZ1 )
```

Layer debugger





Layout Polygons

ICV Productivity Flows

LVS Short Finder

Short Finder

- The short finder allows you to walkthrough the individual polygons of the shorted path for the given violations.

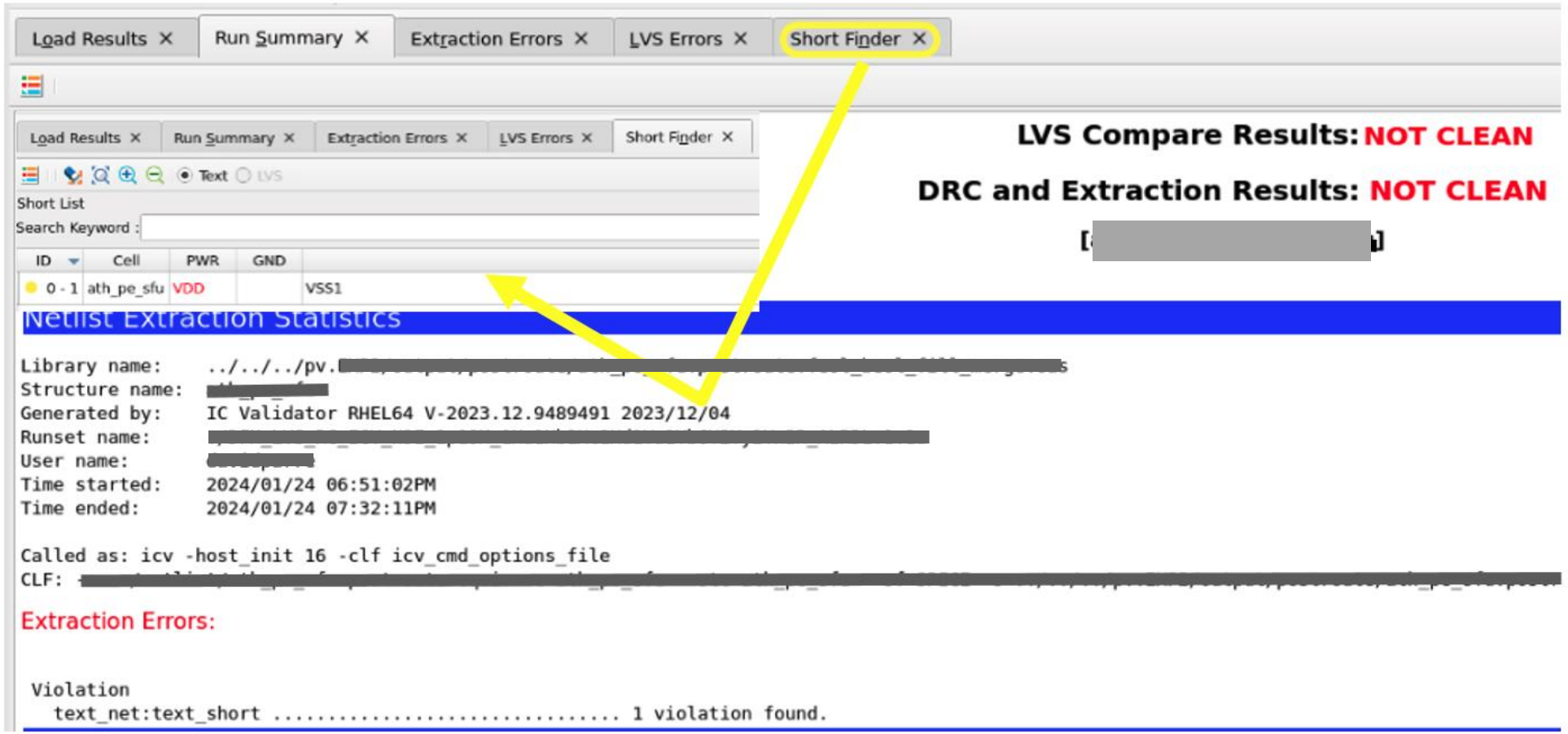
- Isolation difficulties

Short isolation requires time, patience, and the ability to analyze large portions of layout area.

  - ***Power / ground nets***: nets span entire chip
  - ***Shorts through well layers***: wells span large sections of chip
  - ***Hierarchy shorts***: require understanding of multiple levels of hierarchy at the same time

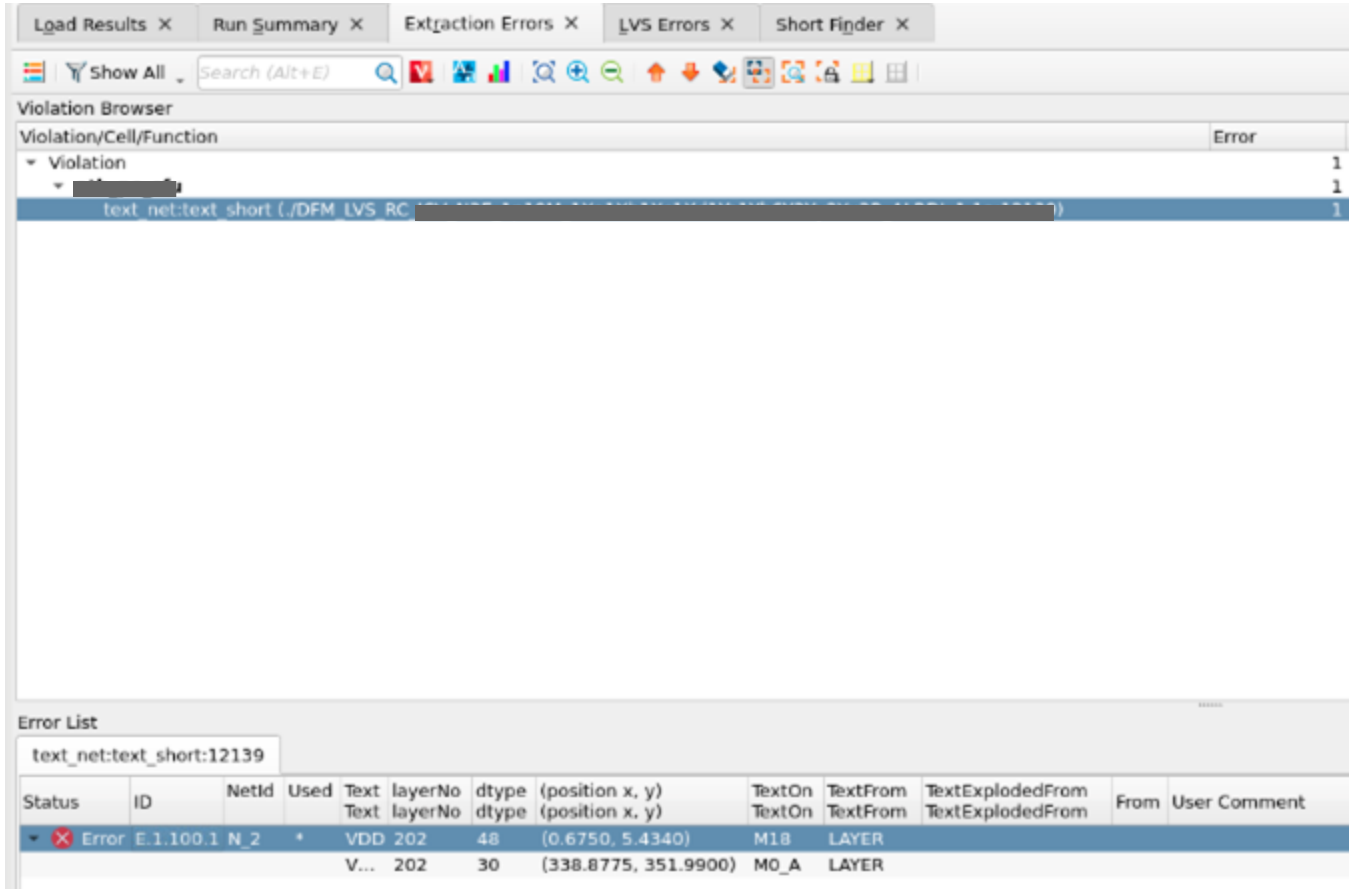
- Add –vueshort for Textshort and –create_lvs_short_output for compare short in cmdfile

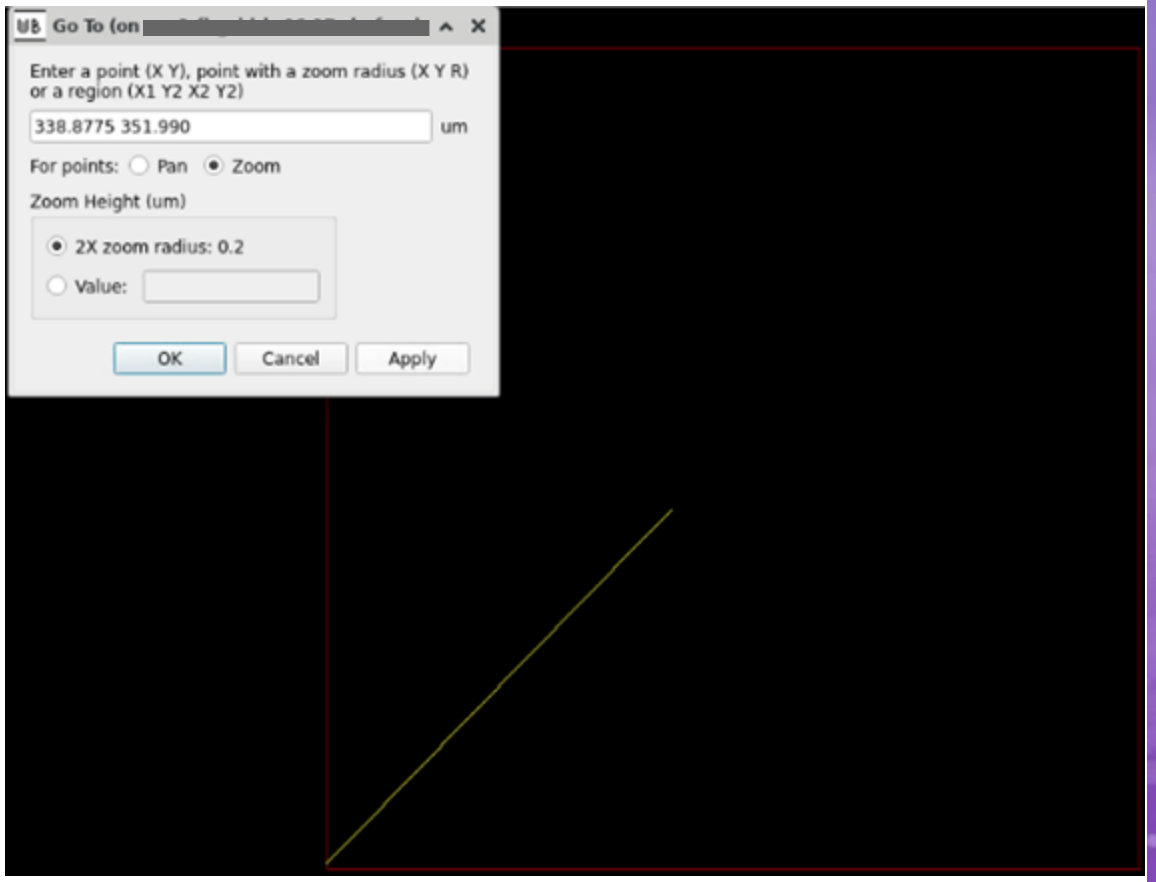
LVS short finder



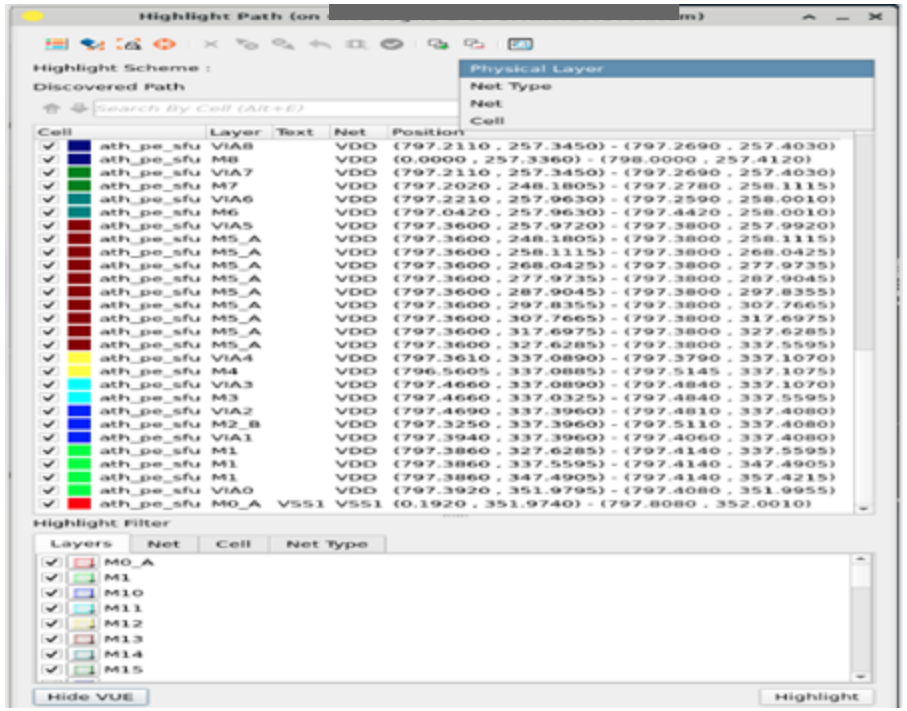
LVS short finder

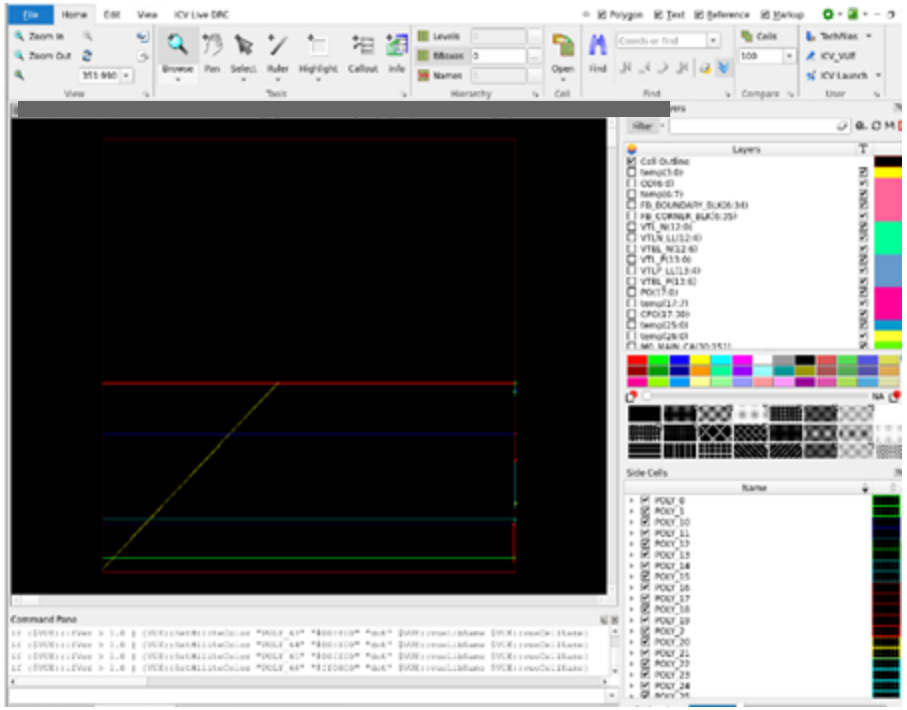
Display of full error path between M18 VDD startpt and M0_A VSS1 endpt





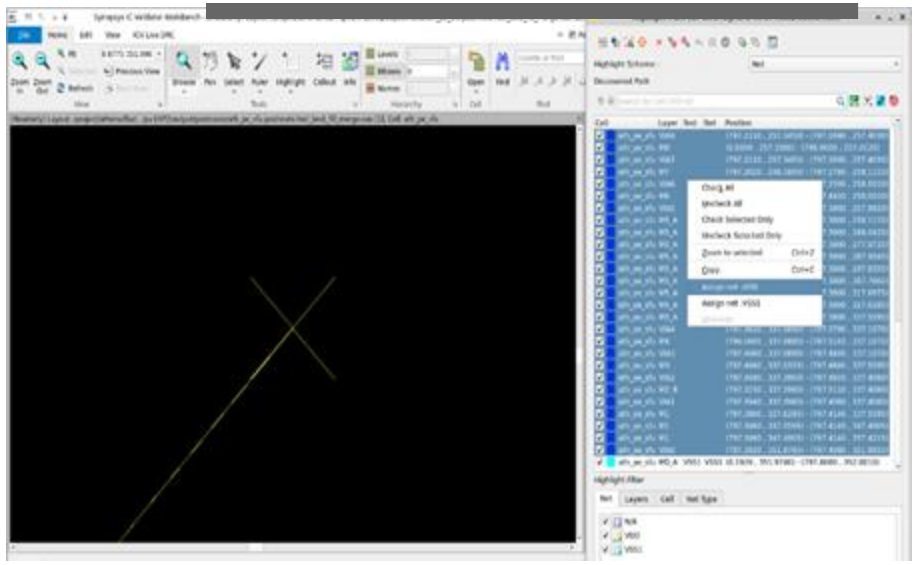
Designer zooms to endpt coordinate suspecting issue with incorrectly labelled net during manual editing of M0 Mask 1 ground wire

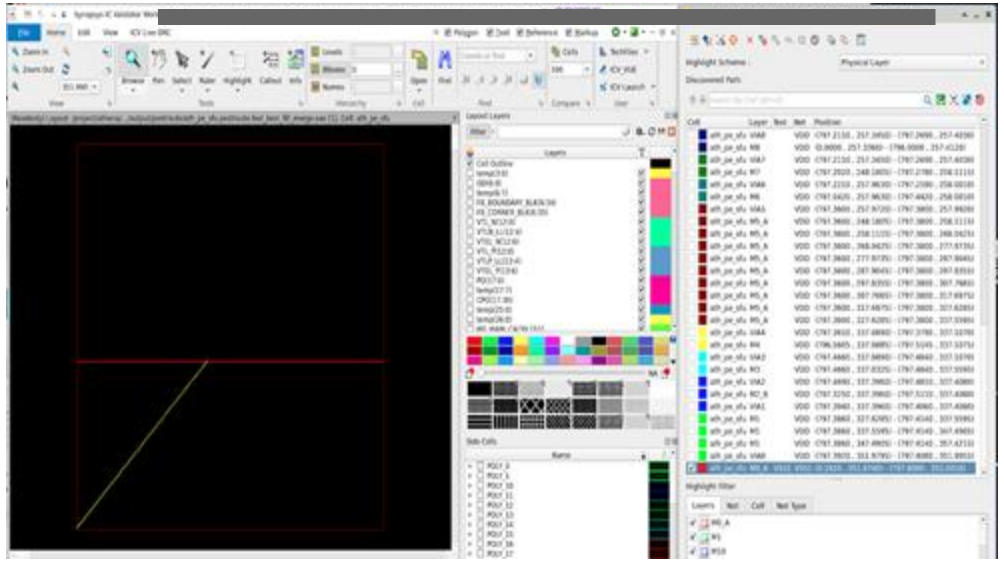




LVS short finder

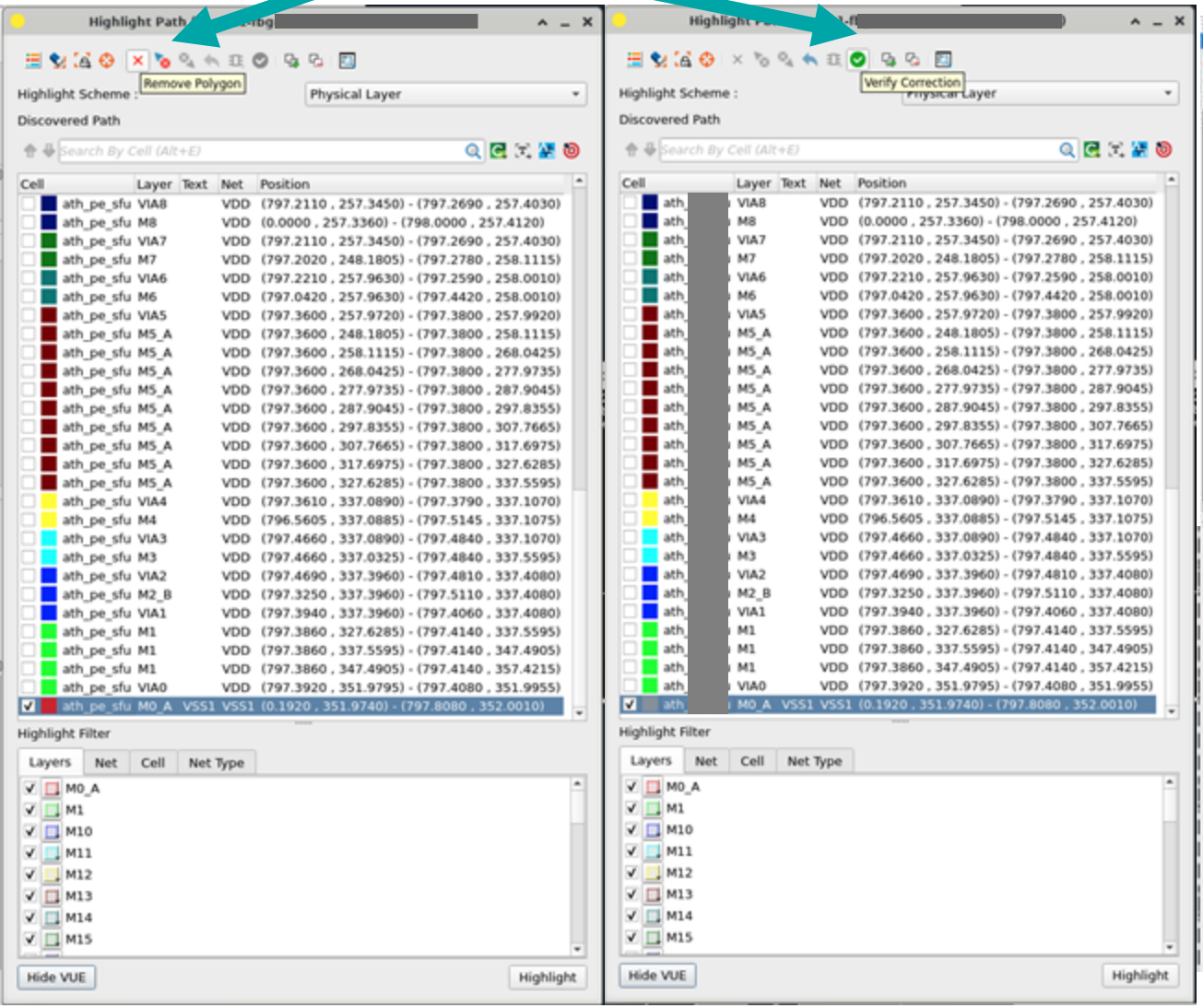
User assigned VDD net to polygons in all layers except selected VSS1 polygon to prune debug

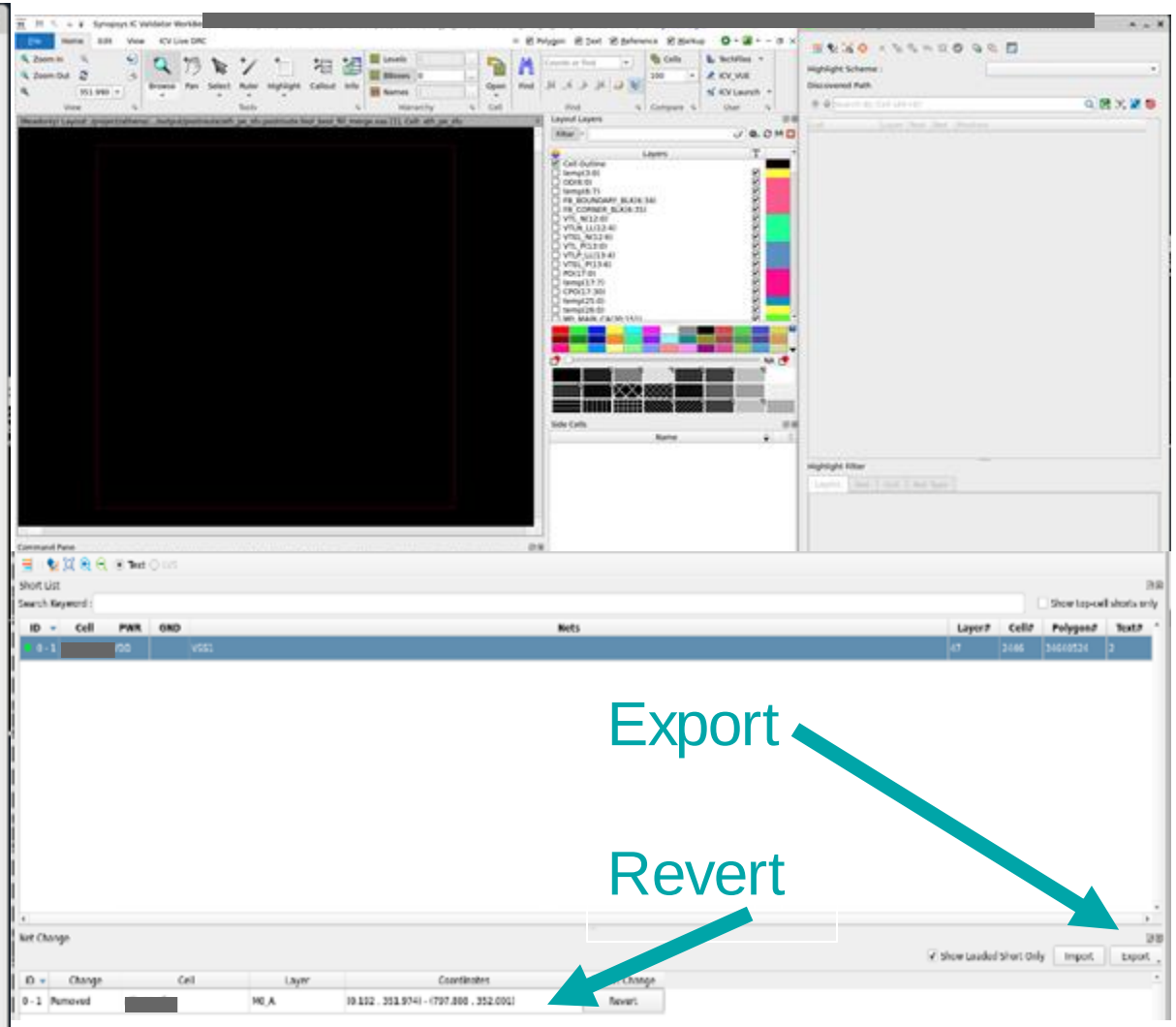




LVS short finder

User **found offending VSS1 polygon:**
Remove Polygon / Verify Correction / Export fix info for designer



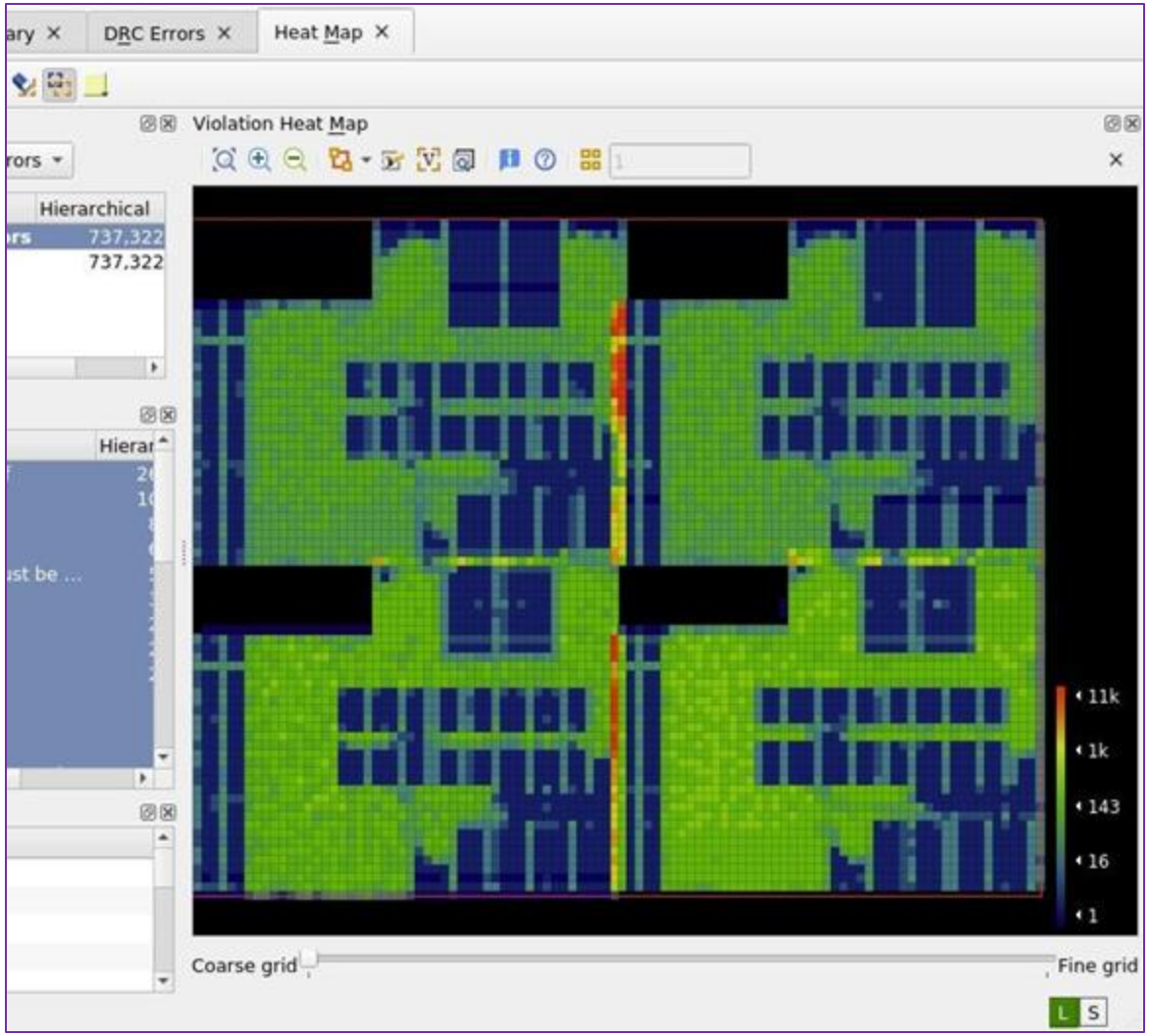


ICV Productivity Flows

ICV Explorer

DRC Explorer

- Feature to debug dirty and gross problems in the design.
- Less hardware resources and time.
- Add “-explorer standalone” in the cmdfile



DRC Explorer

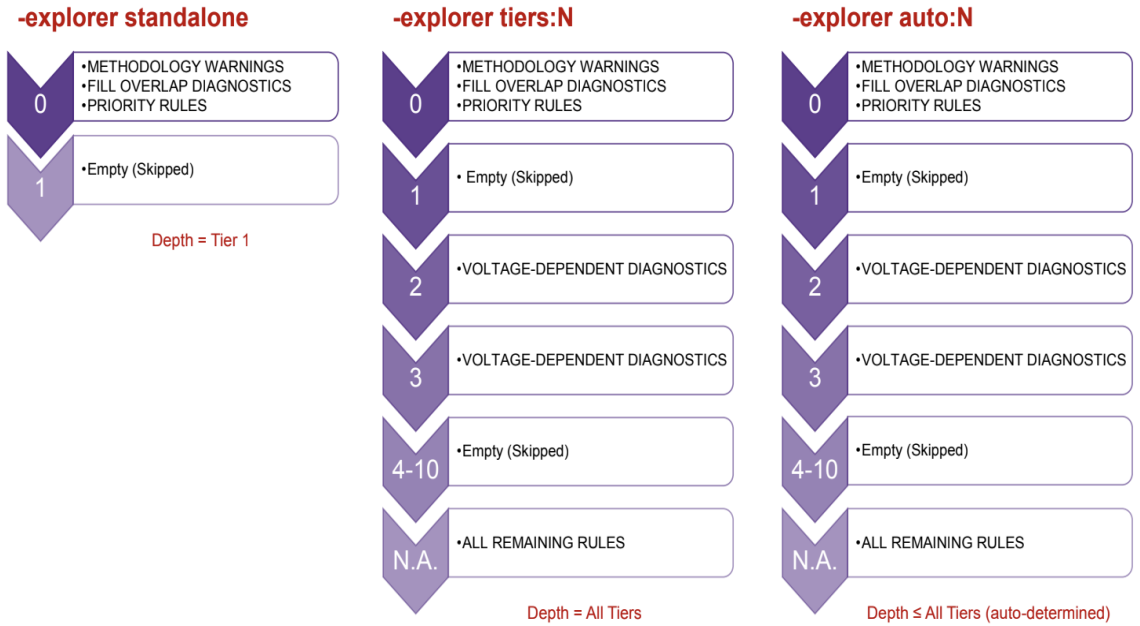
- **DRC Explorer Tiers**

-explorer standalone → Tiers 0 to 1 always run

-explorer auto:N → Tiers 0 to N are eligible to run; run may terminate early if any tier is excessively dirty.

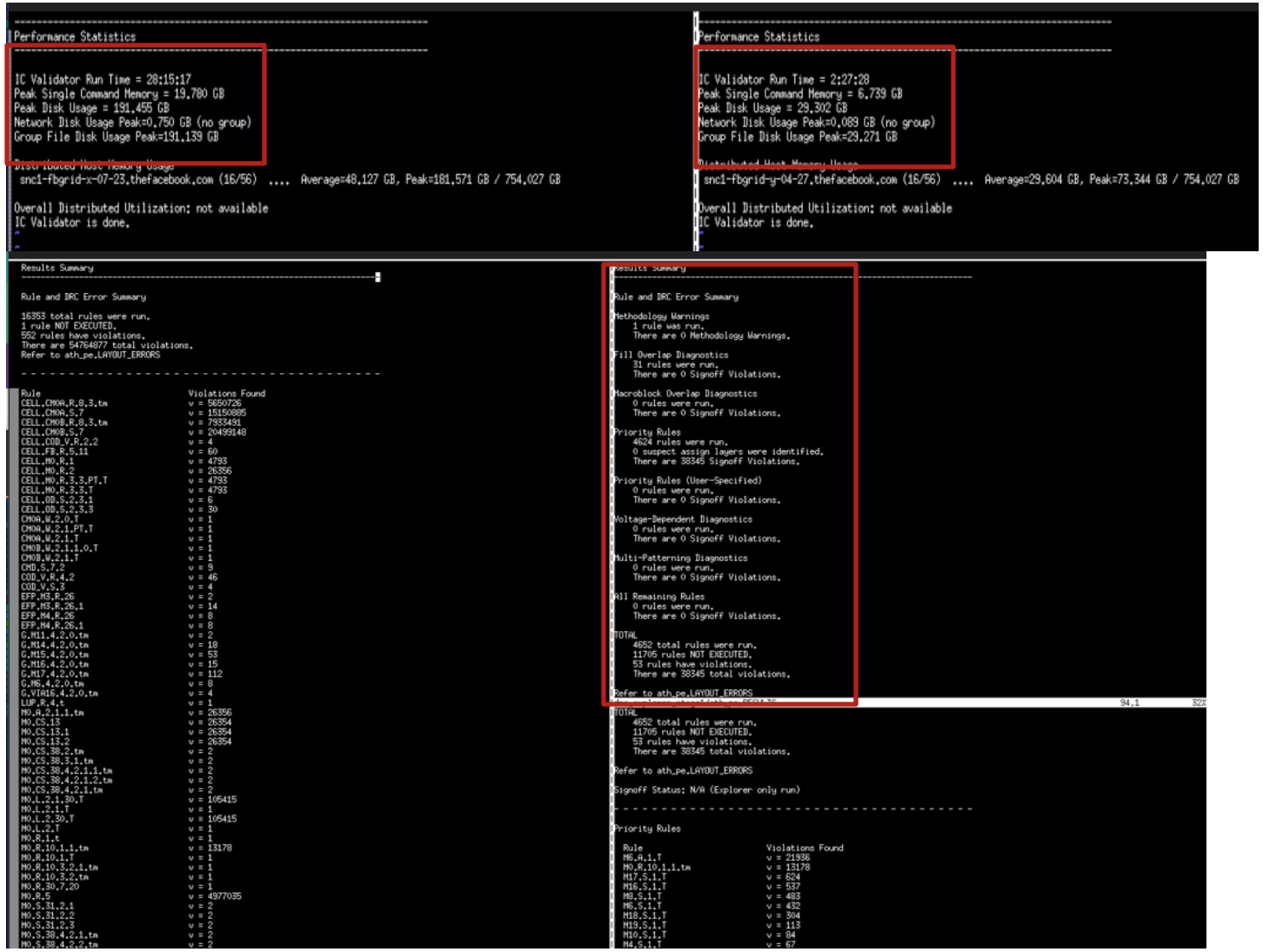
-explorer tiers:N → Tiers 0 to N always run

-explorer_tiers_file <file> → optional user defined Explorer tiers file



DRC Explorer

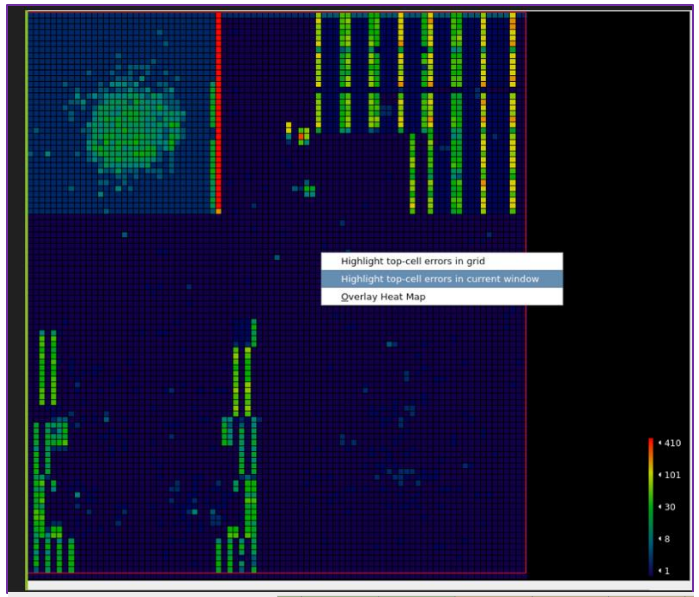
- DRC explorer helps to quickly detect the fundamental design issues.
- Running a subset of rules to flag gross problem
- Signoff and Explorer run results match.
- **10x faster** run time compared to full-signoff runs.

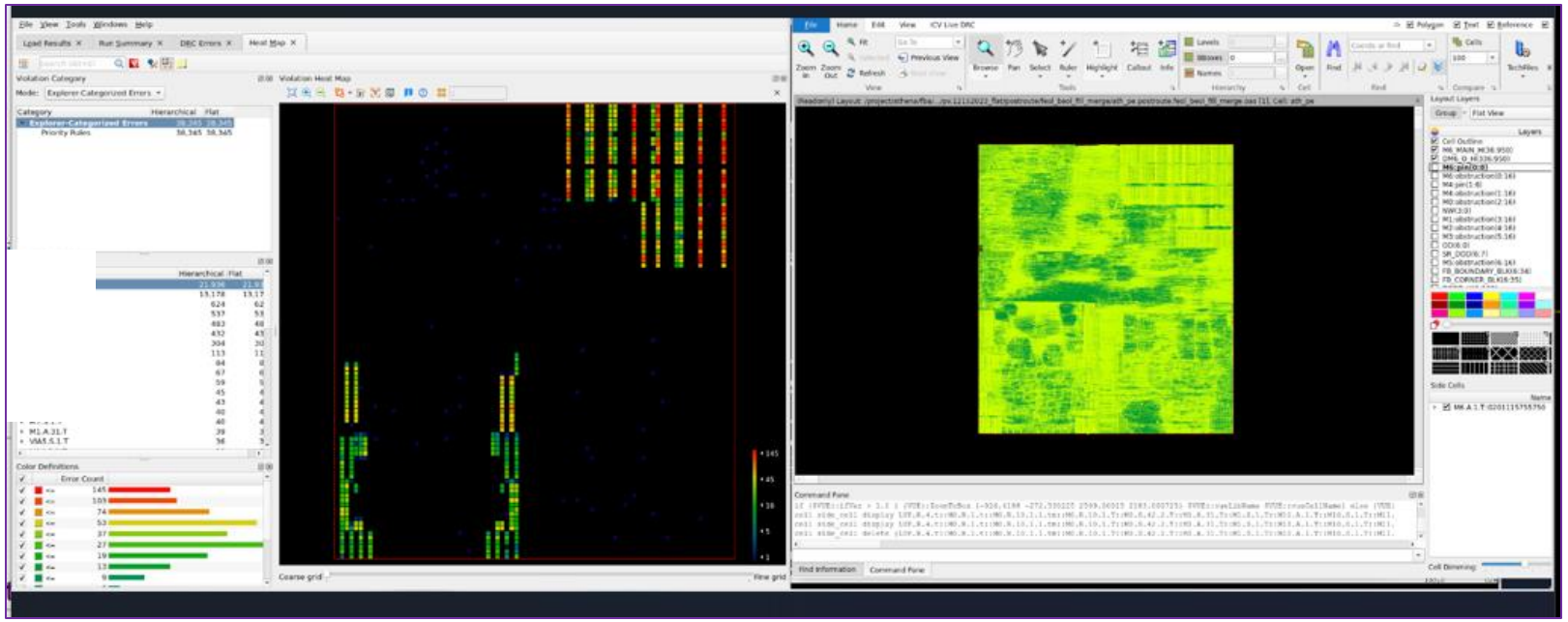


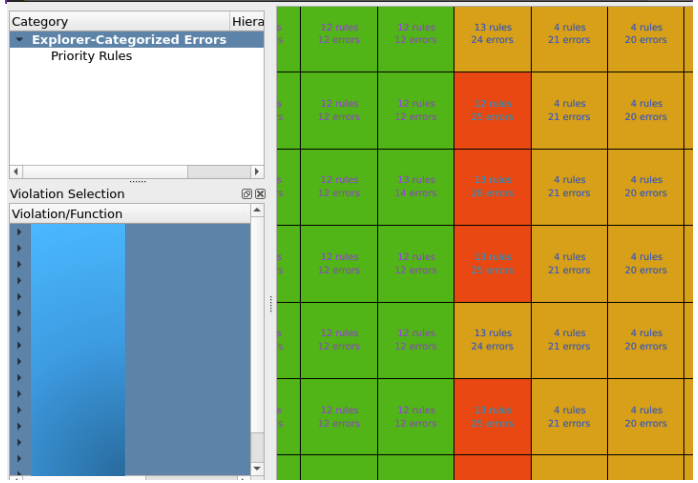
DRC Explorer

Heatmap

- DRC heat-map to find problematic areas.
- Controls to highlight all rules heatmap or single rule heatmap.
- Controls to overlay heatmap to the actual layout.

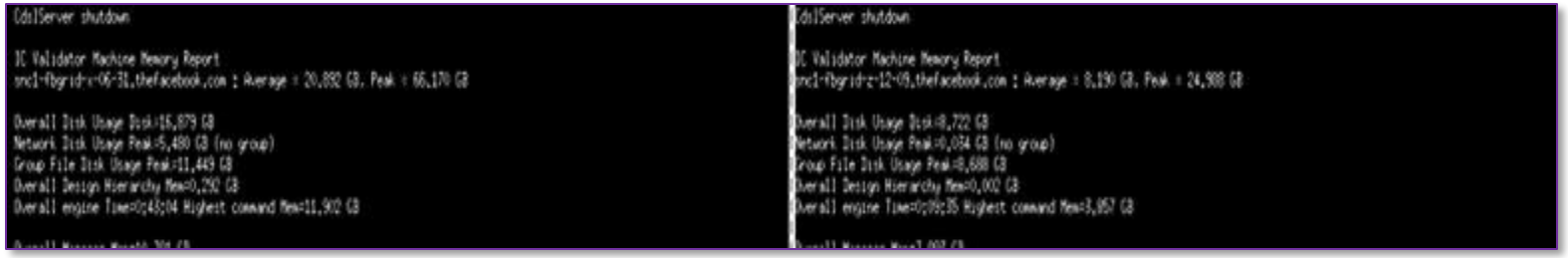


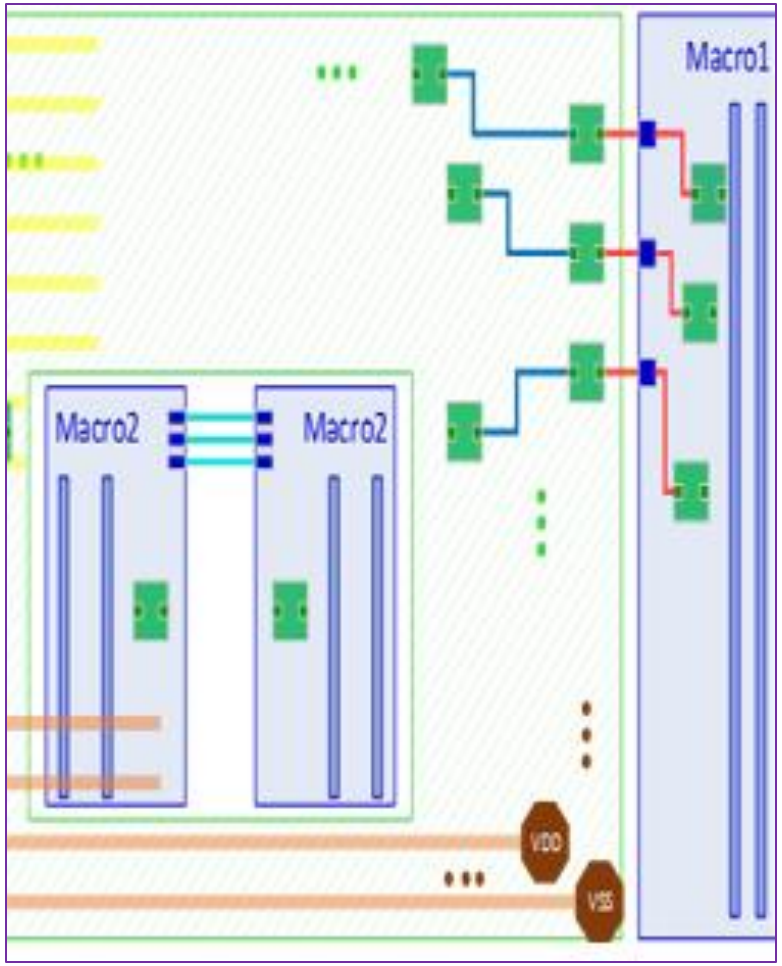




LVS Explorer

- The LVS Explorer feature helps to quickly find top-level shorts and other connectivity issues without running full LVS.
- 5x Faster run time to find the same short.
- Debug and short isolation is same as regular LVS
- Add “-explorer lvs:1” option in cmdfile



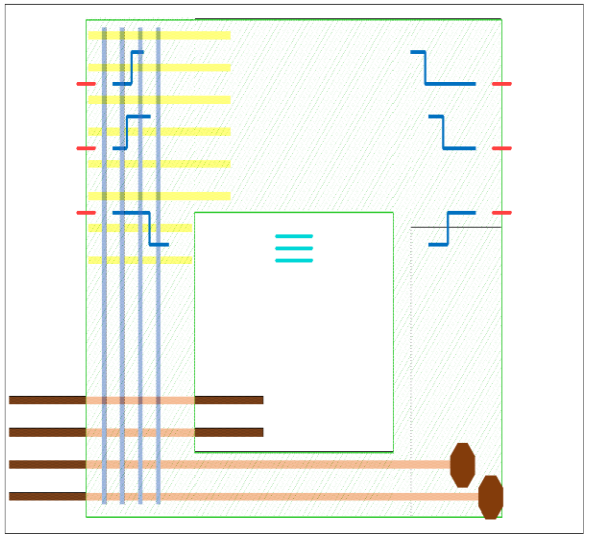


LVS Explorer

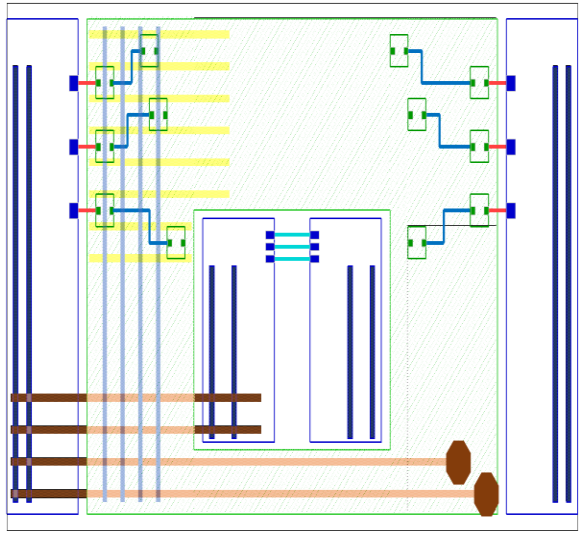
Stages of LVS explorer

	Extract	Compare	Description
Stage 1	Metal only; Delete equiv cells	None	Metal only, text based short check
Stage 2	Metal only; only pins for equiv cells	Black box only	Top level interconnectivity check
Stage 3	Full; all layers, all data	Full	Full LVS check

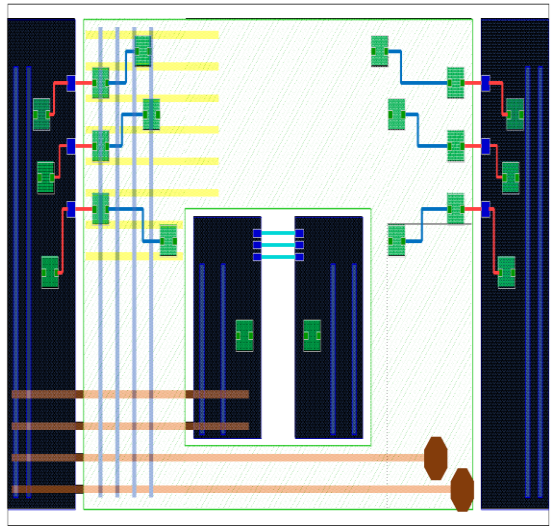
Stage 1



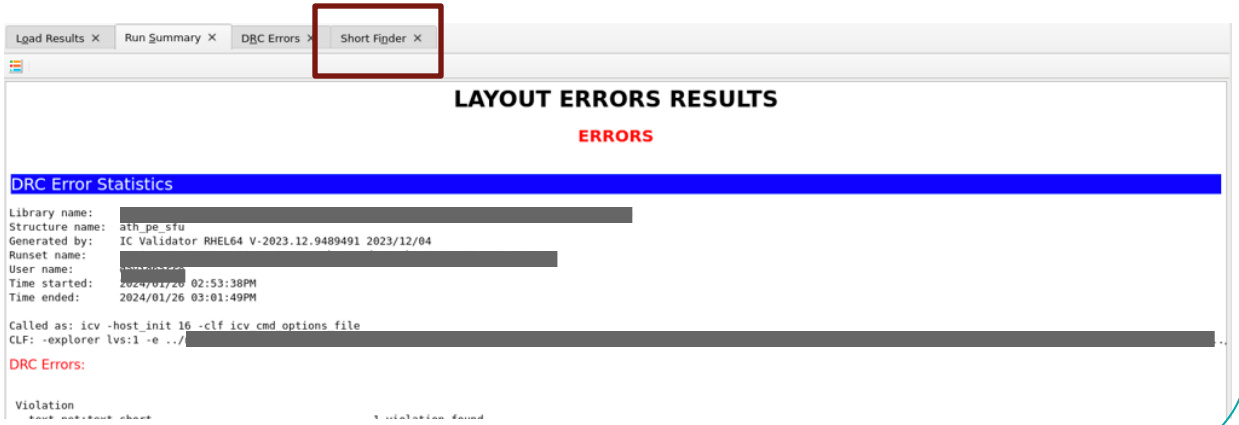
Stage 2

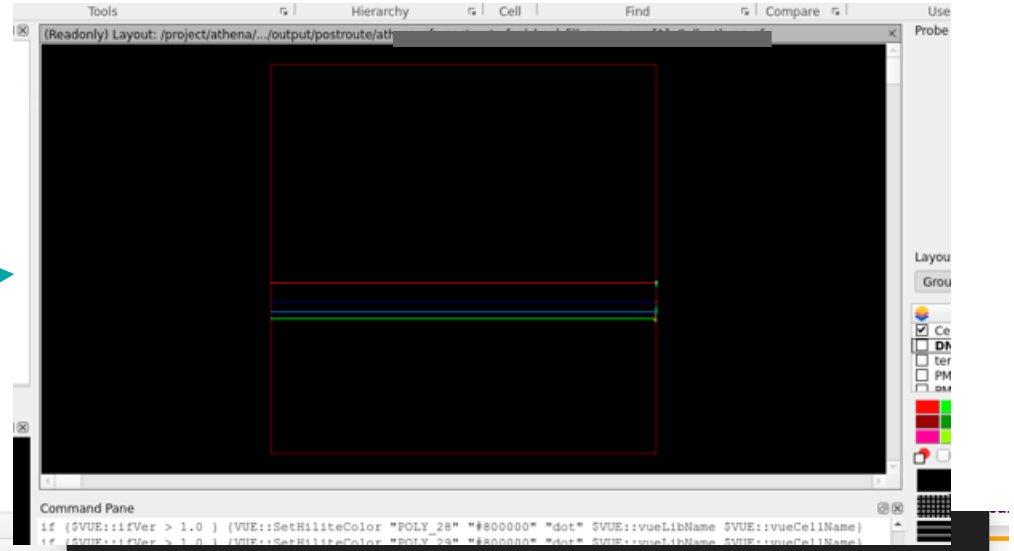


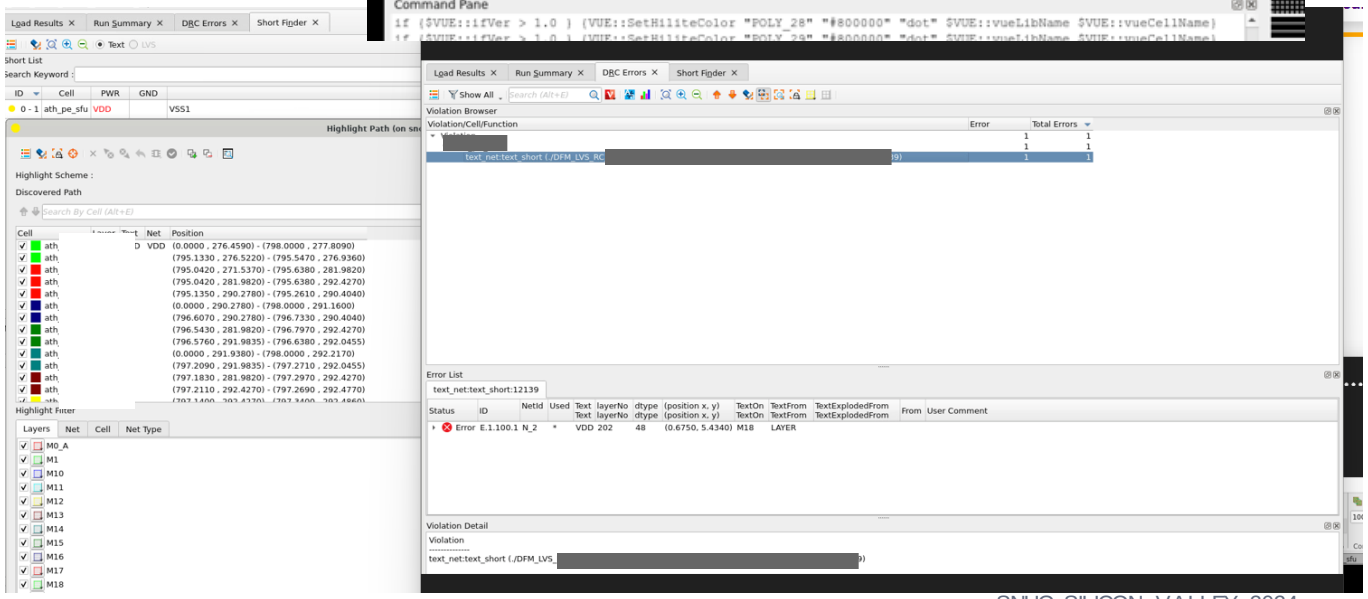
Stage 3



LVS Explorer







- Using Short finder to debug that short.
- Highlight controls to highlight each layer on the shorted path. Highlight by net or by cells.

Summary

- Meta is using IC Validator for PV signoff runs.
- Features like Layer_debugger and Short finder help to debug design issues faster and efficiently.
- Features like Explorer providing faster results with less resources and runtime.

THANK YOU

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