



# PV Signoff and productivity feature for sub nm nodes

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Meta



# Agenda

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- Overview of Meta
- ICV flow at Meta
- ICV Productivity flows and use models
  - Layer Debugger
  - LVS short finder
  - ICV Explorer

# Meta Overview



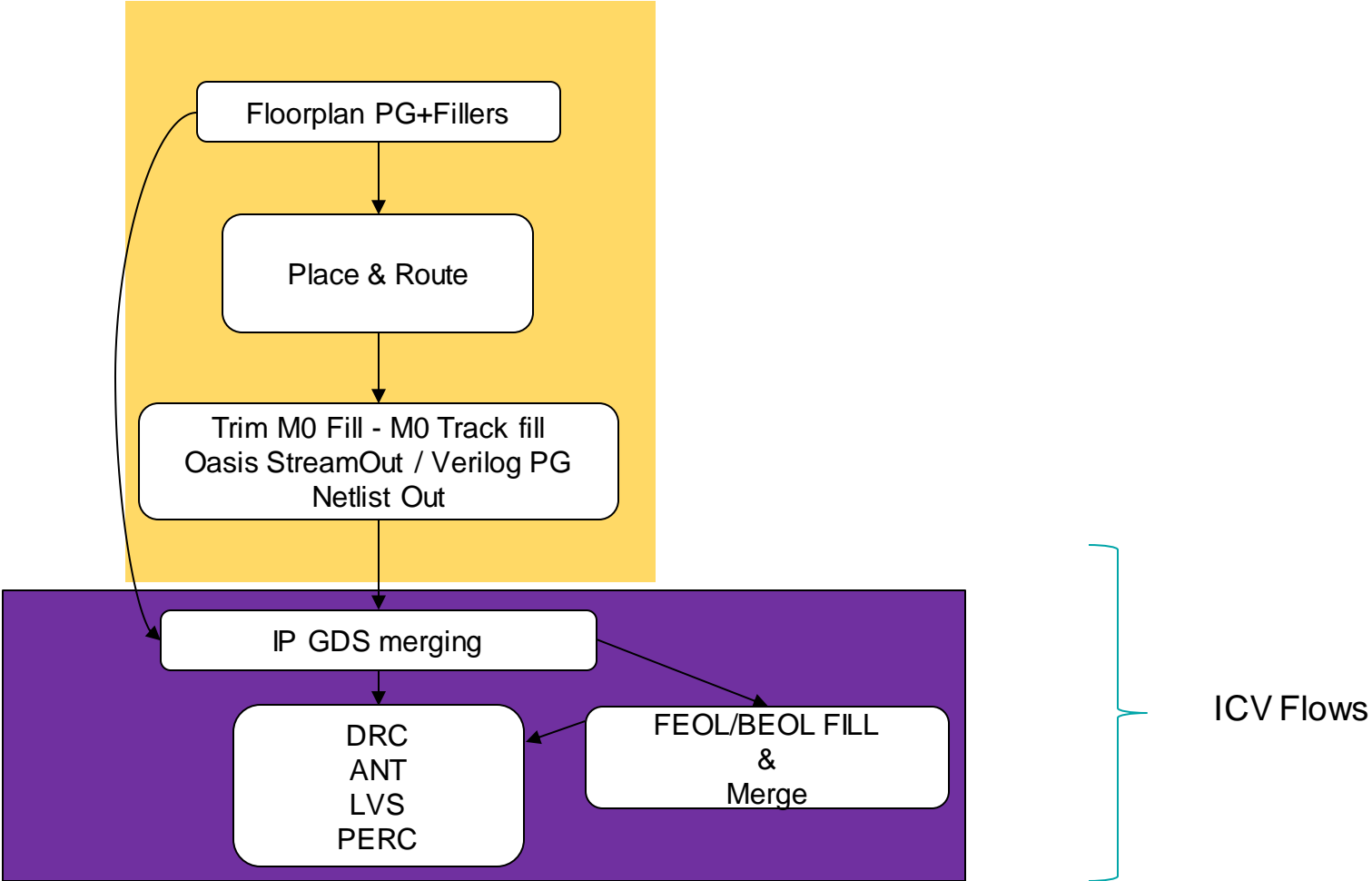
- Meta Platforms, Inc. builds technology that helps people connect and share and grow business.
- Meta Infra silicon team
  - Designs and develop ASICs to Supports AI workloads and infrastructure demands.





# PV Signoff Flow

# PDV Flow at Meta





# ICV Productivity Flows

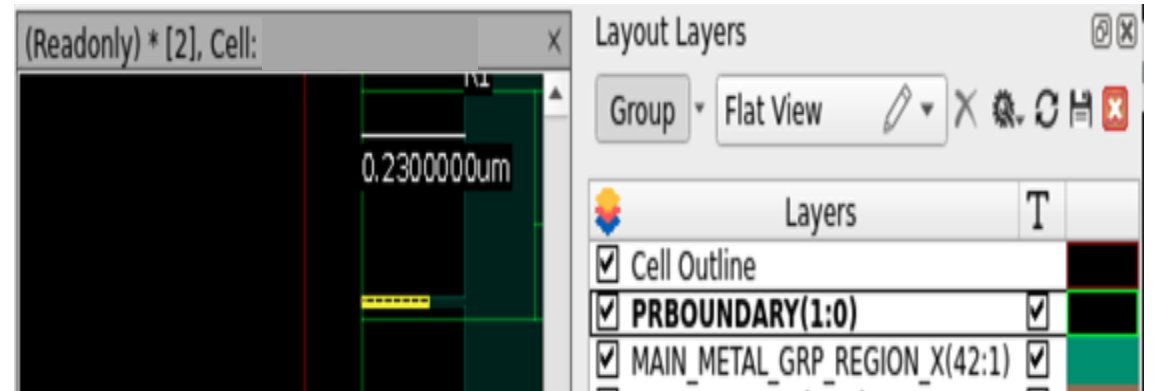
## Layer Debugger

# ICV Productivity flows and use models



## Layer debugger

- The Layer Debugger is a utility that provides a simple graphical method to debug layer creation in a runset.
- Use models: Debug complex DRC rules by generating intermediate layers.
- add `-layer_debugger` option in cmd file
- add `-svc "M*.EN.2 *"` option for particular drc debug in cmd file





# Layer debugger : Metal enclosure violations flagged by ICV ruleset but not by PnR tool

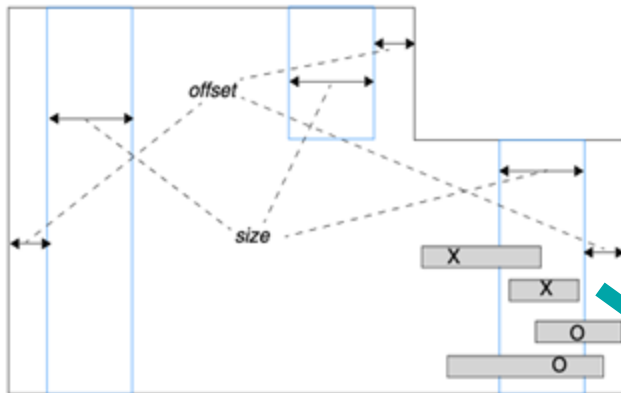


```
PROPERTY LEF58_BOUNDARYEOLBLOCKAGE "BOUNDARYEOLBLOCKAGE 0.1055 OFFSET 0.1485 PARALLEL 0.2505 WITHIN 0.2295 SPACING 0.2505 ; "
```

Root-cause: TECHLEF increase of BoundaryEOLBlockage OFFSET by 24nm

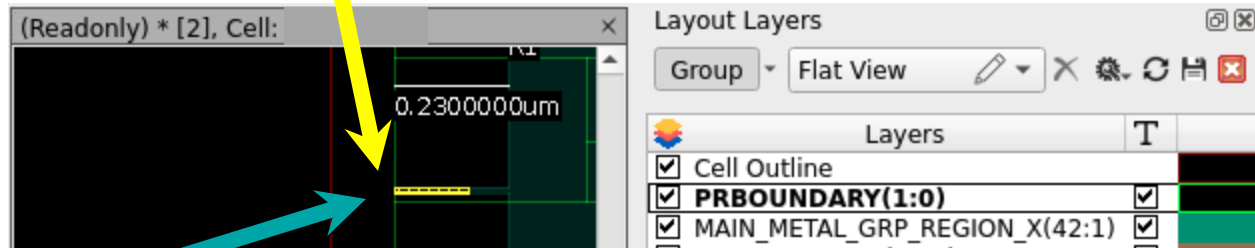
LEF/DEF 5.8 Language Reference  
LEF Syntax - Layer (Routing)

Figure 5-25 Illustration of the Boundary EOL Blockage Rule



Preferred routing direction is horizontal

BoundaryEOLBlockage SIZE (0.1055) + OFFSET (0.1485) !=  
M2\_EN\_19\_2\_SZ1



Layout polygons & violation marker

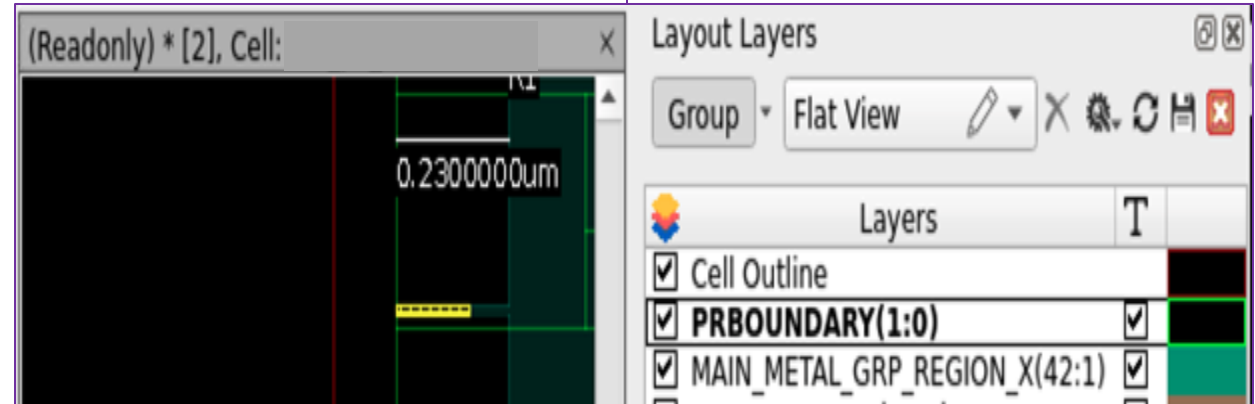
```
VARIABLE M2_EN_19_2_SZ1 0.2300
VARIABLE M2_EN_19_2_SZ1 0.1250
VARIABLE M2_EN_19_2_SZ1 0.1250
VARIABLE M2_EN_19_2_SZ1 0.2295
```

```
Main_M2_NMIMP_GRP_Region_pre_x = OR M2dx_main ( SHRINK prBoundary RIGHT BY M2_EN_19_2_SZ1 LEFT BY M2_EN_19_2_SZ1 )
```

# Layer debugger



```
Lgadm Results X Layer Debugger X
M12_HV_ID_TOP = text_to_double_property(tM12V_HIGH_TOP, 'high', MAX, 5e-05, { })
M12_LV_ID_TOP = text_to_double_property(tM12V_LOW_TOP, 'low', MIN, 5e-05, { })
M12_USERDV_TOP_ID = text_to_double_property(tM12_USERDV_TOP, 'userdv', MAX, 5e-05, { })
M13_HV_ID_TOP = text_to_double_property(tM13V_HIGH_TOP, 'high', MAX, 5e-05, { })
M13_LV_ID_TOP = text_to_double_property(tM13V_LOW_TOP, 'low', MIN, 5e-05, { })
M13_USERDV_TOP_ID = text_to_double_property(tM13_USERDV_TOP, 'userdv', MAX, 5e-05, { })
M14_HV_ID_TOP = text_to_double_property(tM14V_HIGH_TOP, 'high', MAX, 5e-05, { })
M14_LV_ID_TOP = text_to_double_property(tM14V_LOW_TOP, 'low', MIN, 5e-05, { })
M14_USERDV_TOP_ID = text_to_double_property(tM14_USERDV_TOP, 'userdv', MAX, 5e-05, { })
M15_HV_ID_TOP = text_to_double_property(tM15V_HIGH_TOP, 'high', MAX, 5e-05, { })
M15_LV_ID_TOP = text_to_double_property(tM15V_LOW_TOP, 'low', MIN, 5e-05, { })
M15_USERDV_TOP_ID = text_to_double_property(tM15_USERDV_TOP, 'userdv', MAX, 5e-05, { })
M16_HV_ID_TOP = text_to_double_property(tM16V_HIGH_TOP, 'high', MAX, 5e-05, { })
M16_LV_ID_TOP = text_to_double_property(tM16V_LOW_TOP, 'low', MIN, 5e-05, { })
M16_USERDV_TOP_ID = text_to_double_property(tM16_USERDV_TOP, 'userdv', MAX, 5e-05, { })
M17_HV_ID_TOP = text_to_double_property(tM17V_HIGH_TOP, 'high', MAX, 5e-05, { })
M17_LV_ID_TOP = text_to_double_property(tM17V_LOW_TOP, 'low', MIN, 5e-05, { })
M17_USERDV_TOP_ID = text_to_double_property(tM17_USERDV_TOP, 'userdv', MAX, 5e-05, { })
M18_HV_ID_TOP = text_to_double_property(tM18V_HIGH_TOP, 'high', MAX, 5e-05, { })
M18_LV_ID_TOP = text_to_double_property(tM18V_LOW_TOP, 'low', MIN, 5e-05, { })
M18_USERDV_TOP_ID = text_to_double_property(tM18_USERDV_TOP, 'userdv', MAX, 5e-05, { })
M19_HV_ID_TOP = text_to_double_property(tM19V_HIGH_TOP, 'high', MAX, 5e-05, { })
M19_LV_ID_TOP = text_to_double_property(tM19V_LOW_TOP, 'low', MIN, 5e-05, { })
M19_USERDV_TOP_ID = text_to_double_property(tM19_USERDV_TOP, 'userdv', MAX, 5e-05, { })
AP_HV_ID = text_to_double_property(tAPV_HIGH, 'high', MAX, 5e-05, { })
AP_LV_ID = text_to_double_property(tAPV_LOW, 'low', MIN, 5e-05, { })
AP_USERDV_ID = text_to_double_property(tAP_USERDV, 'userdv', MAX, 5e-05, { })
AP_HV_ID_TOP = text_to_double_property(tAPV_HIGH_TOP, 'high', MAX, 5e-05, { })
AP_LV_ID_TOP = text_to_double_property(tAPV_LOW_TOP, 'low', MIN, 5e-05, { })
AP_USERDV_TOP_ID = text_to_double_property(tAP_USERDV_TOP, 'userdv', MAX, 5e-05, { })
CU_RDL_HV_ID = text_to_double_property(tCU_RDLV_HIGH, 'high', MAX, 5e-05, { })
CU_RDL_LV_ID = text_to_double_property(tCU_RDLV_LOW, 'low', MIN, 5e-05, { })
CU_RDL_USERDV_ID = text_to_double_property(tCU_RDL_USERDV, 'userdv', MAX, 5e-05, { })
CU_RDL_HV_ID_TOP = text_to_double_property(tCU_RDLV_HIGH_TOP, 'high', MAX, 5e-05, { })
CU_RDL_LV_ID_TOP = text_to_double_property(tCU_RDLV_LOW_TOP, 'low', MIN, 5e-05, { })
CU_RDL_USERDV_TOP_ID = text_to_double_property(tCU_RDL_USERDV_TOP, 'userdv', MAX, 5e-05, { })
M2DX_MAIN_CA = copy(M2_MAIN_CA_H, ancestry = true)
M2DY_MAIN_CA = copy(M2_MAIN_CA_V, ancestry = true)
M2DX_MAIN_CB = copy(M2_MAIN_CB_H, ancestry = true)
M2DY_MAIN_CB = copy(M2_MAIN_CB_V, ancestry = true)
M4DX_MAIN = copy(M4_MAIN_H, ancestry = true)
M4DY_MAIN = copy(M4_MAIN_V, ancestry = true)
__t9496 = or(M2DX_MAIN_CA, M2DY_MAIN_CB)
__t9497 = shrink(PRBOUNDARY, east = 0.23, west = 0.23)
MAIN_METAL_GRP_REGION_X_PRE = or(__t9496, __t9497)
__t9498 = size(MAIN_METAL_GRP_REGION_X_PRE, 0.125, clip_acute = TRUNCATE)
MAIN_METAL_GRP_REGION_X = size(__t9498, -0.125, clip_acute = TRUNCATE)
enclose(MAIN_METAL_GRP_REGION_X, PRBOUNDARY, east = 0.23, west = 0.23)
comment = "M2!"
```



Layout Polygons



# ICV Productivity Flows

## LVS Short Finder

# Short Finder



- The short finder allows you to walkthrough the individual polygons of the shorted path for the given violations.
- Isolation difficulties
  - Short isolation requires time, patience, and the ability to analyze large portions of layout area.
  - **Power / ground nets:** nets span entire chip
  - **Shorts through well layers:** wells span large sections of chip
  - **Hierarchy shorts:** require understanding of multiple levels of hierarchy at the same time
- Add `-vueshort` for Textshort and `-create_lvs_short_output` for compare short in cmdfile

# LVS short finder



The screenshot shows the 'Short Finder' tab in a software application. The interface includes a 'Short List' table with columns for ID, Cell, PWR, and GND. A yellow arrow points from the 'Short Finder' tab to the first row of the table, which contains a violation.

| ID    | Cell       | PWR | GND  |
|-------|------------|-----|------|
| 0 - 1 | ath_pe_sfu | VDD | VSS1 |

Below the table, the 'Netlist Extraction Statistics' section provides details about the extraction process, including the library name, structure name, and generation date. The 'Extraction Errors' section shows a single violation: 'text\_net:text\_short ..... 1 violation found.'

**LVS Compare Results: NOT CLEAN**  
**DRC and Extraction Results: NOT CLEAN**

[REDACTED]

Library name: ../../../../pv.[REDACTED]  
Structure name: [REDACTED]  
Generated by: IC Validator RHEL64 V-2023.12.9489491 2023/12/04  
Runset name: [REDACTED]  
User name: [REDACTED]  
Time started: 2024/01/24 06:51:02PM  
Time ended: 2024/01/24 07:32:11PM

Called as: icv -host\_init 16 -clf icv\_cmd\_options\_file  
CLF: [REDACTED]

**Extraction Errors:**

Violation  
text\_net:text\_short ..... 1 violation found.

# LVS short finder



Display of full error path between M18 VDD startpt and M0\_A VSS1 endpt

The screenshot shows the LVS Short Finder tool interface. At the top, there are tabs for 'Load Results', 'Run Summary', 'Extraction Errors', 'LVS Errors', and 'Short Finder'. Below the tabs is a search bar and a toolbar. The 'Violation Browser' section shows a tree view with 'Violation' expanded, and a single entry 'text\_net:text short (/DFM LVS RC ...)' is selected. At the bottom, the 'Error List' table is visible, showing the error details.

| Status | ID                  | NetId | Used | Text | layerNo | dtype                | (position x, y) | TextOn | TextFrom | TextExplodedFrom | From | User Comment |  |
|--------|---------------------|-------|------|------|---------|----------------------|-----------------|--------|----------|------------------|------|--------------|--|
| ✖      | Error E.1.100.1 N_2 | *     | VDD  | 202  | 48      | (0.6750, 5.4340)     | M18             | LAYER  |          |                  |      |              |  |
|        |                     |       | V... | 202  | 30      | (338.8775, 351.9900) | M0_A            | LAYER  |          |                  |      |              |  |

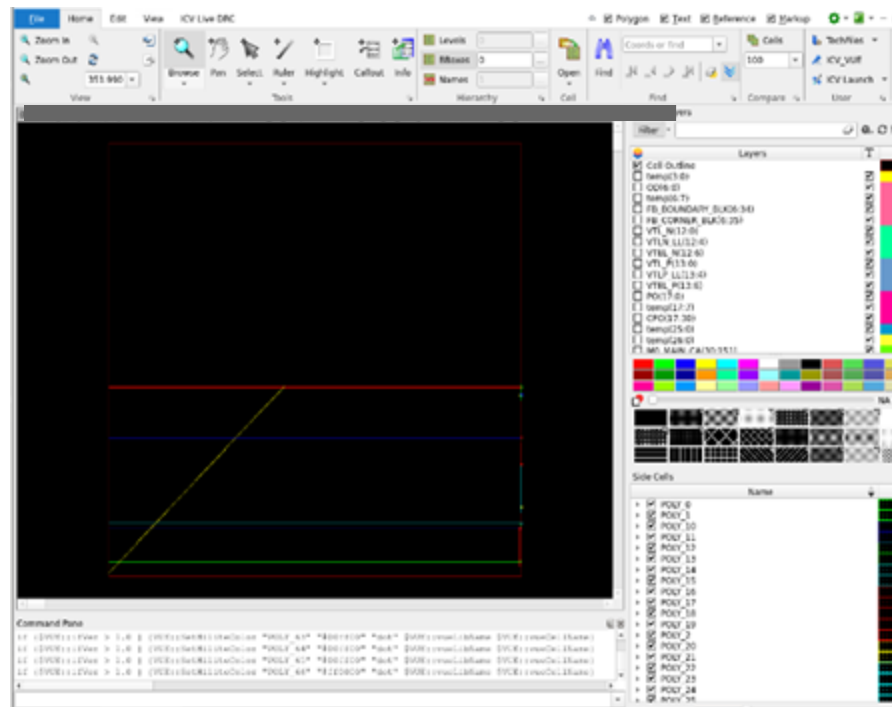
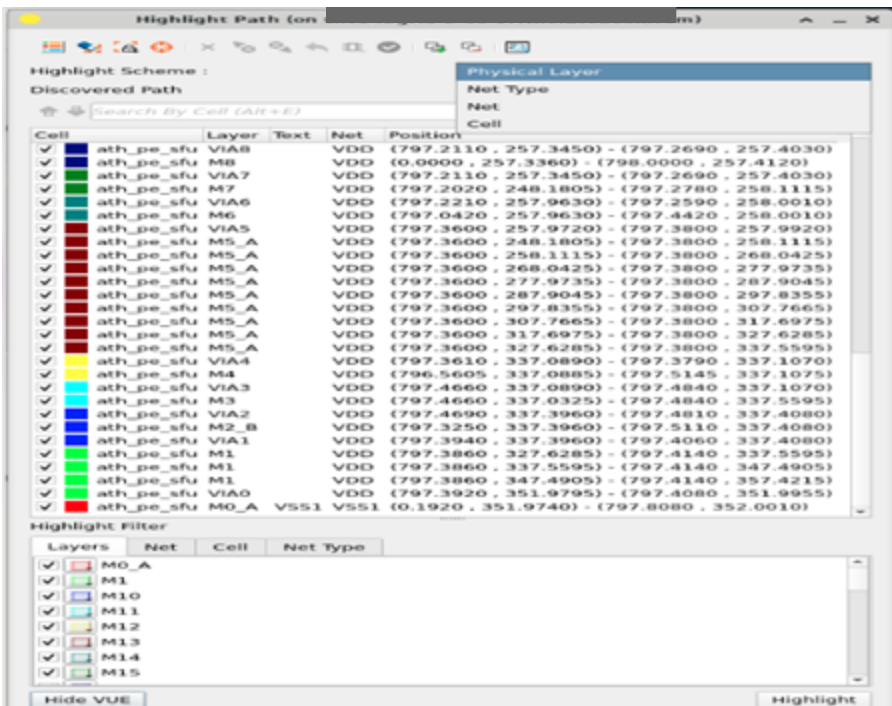
The screenshot shows the 'Go To' dialog box in the design tool. The dialog has a title bar 'Go To (on ...)' and a search bar. Below the search bar, there are input fields for 'Enter a point (X Y), point with a zoom radius (X Y R) or a region (X1 Y2 X2 Y2)'. The first input field contains '338.8775 351.990' and the unit is 'um'. Below the input fields, there are radio buttons for 'For points: Pan' and 'Zoom', with 'Zoom' selected. There is also a 'Zoom Height (um)' section with a radio button for '2X zoom radius: 0.2' and a 'Value:' input field. At the bottom, there are 'OK', 'Cancel', and 'Apply' buttons.

Designer zooms to endpt coordinate suspecting issue with incorrectly labelled net during manual editing of M0 Mask 1 ground wire

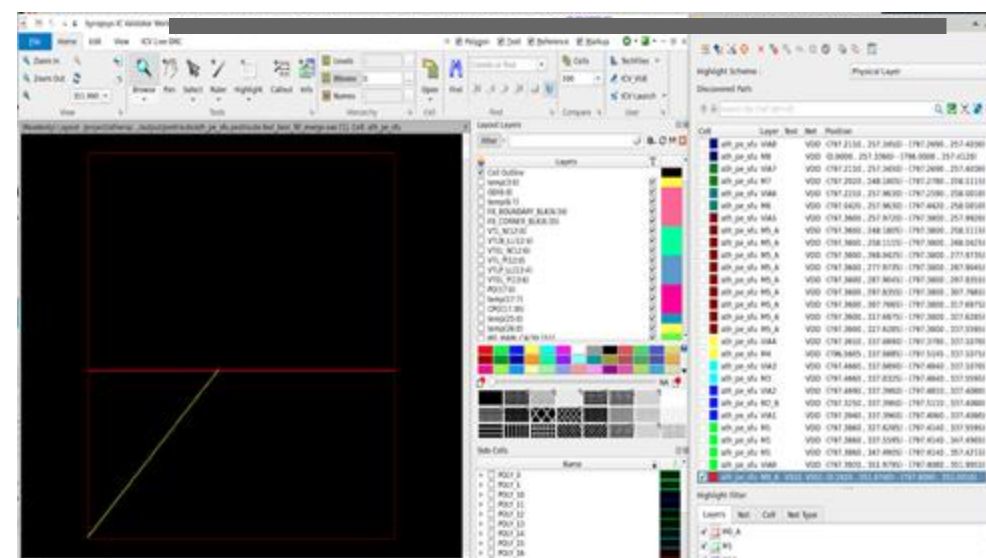
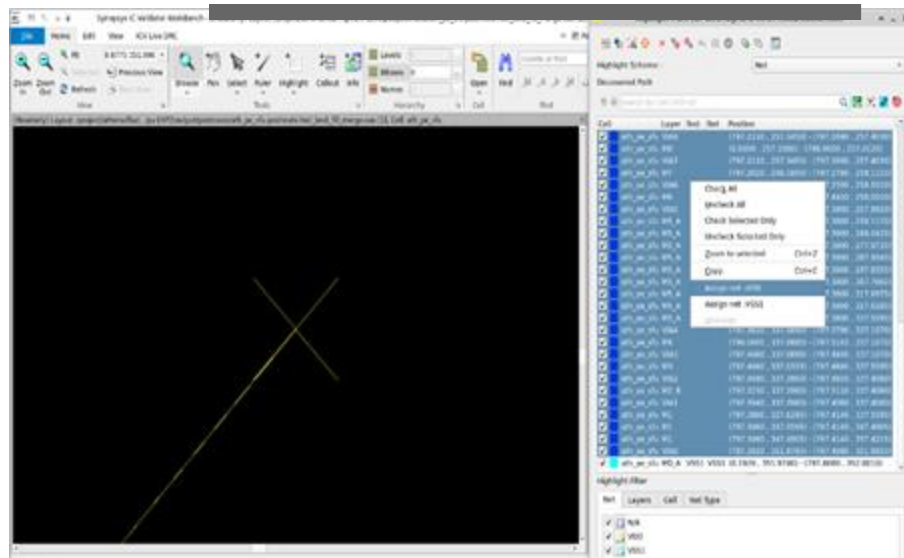




# LVS short finder



User assigned VDD net to polygons in all layers except selected VSS1 polygon to prune debug



# LVS short finder



User found offending VSS1 polygon:

Remove Polygon / Verify Correction / Export fix info for designer

| Cell            | Layer | Text  | Net | Position |
|-----------------|-------|---|-----|----------|
| ath_pe_sf1 VIA8 | VDD   | (797.2110, 257.3450) - (797.2690, 257.4030) |     |          |
| ath_pe_sf1 M8   | VDD   | (0.0000, 257.3360) - (798.0000, 257.4120)   |     |          |
| ath_pe_sf1 VIA7 | VDD   | (797.2110, 257.3450) - (797.2690, 257.4030) |     |          |
| ath_pe_sf1 M7   | VDD   | (797.2020, 248.1805) - (797.2780, 258.1115) |     |          |
| ath_pe_sf1 VIA6 | VDD   | (797.2210, 257.9630) - (797.2590, 258.0010) |     |          |
| ath_pe_sf1 M6   | VDD   | (797.0420, 257.9630) - (797.4420, 258.0010) |     |          |
| ath_pe_sf1 VIA5 | VDD   | (797.3600, 257.9720) - (797.3800, 257.9920) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 248.1805) - (797.3800, 258.1115) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 258.1115) - (797.3800, 268.0425) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 268.0425) - (797.3800, 277.9735) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 277.9735) - (797.3800, 287.9045) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 287.9045) - (797.3800, 297.8355) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 297.8355) - (797.3800, 307.7665) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 307.7665) - (797.3800, 317.6975) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 317.6975) - (797.3800, 327.6285) |     |          |
| ath_pe_sf1 M5_A | VDD   | (797.3600, 327.6285) - (797.3800, 337.5595) |     |          |
| ath_pe_sf1 VIA4 | VDD   | (797.3610, 337.0890) - (797.3790, 337.1070) |     |          |
| ath_pe_sf1 M4   | VDD   | (796.5605, 337.0885) - (797.5145, 337.1075) |     |          |
| ath_pe_sf1 VIA3 | VDD   | (797.4660, 337.0890) - (797.4840, 337.1070) |     |          |
| ath_pe_sf1 M3   | VDD   | (797.4660, 337.0325) - (797.4840, 337.5595) |     |          |
| ath_pe_sf1 VIA2 | VDD   | (797.4690, 337.3960) - (797.4810, 337.4080) |     |          |
| ath_pe_sf1 M2_B | VDD   | (797.3250, 337.3960) - (797.5110, 337.4080) |     |          |
| ath_pe_sf1 VIA1 | VDD   | (797.3940, 337.3960) - (797.4060, 337.4080) |     |          |
| ath_pe_sf1 M1   | VDD   | (797.3860, 327.6285) - (797.4140, 337.5595) |     |          |
| ath_pe_sf1 M1   | VDD   | (797.3860, 337.5595) - (797.4140, 347.4905) |     |          |
| ath_pe_sf1 M1   | VDD   | (797.3860, 347.4905) - (797.4140, 357.4215) |     |          |
| ath_pe_sf1 VIA0 | VDD   | (797.3920, 351.9795) - (797.4080, 351.9955) |     |          |
| ath_pe_sf1 M0_A | VSS1  | (0.1920, 351.9740) - (797.8080, 352.0010)   |     |          |

| ID  | Cell | PWK | OND | Nets | Layer? | Cells | Polygon? | Text? |
|-----|------|-----|-----|------|--------|-------|----------|-------|
| 0-1 |      | DD  |     | VSS1 | at     | 2046  | 3160224  | 2     |





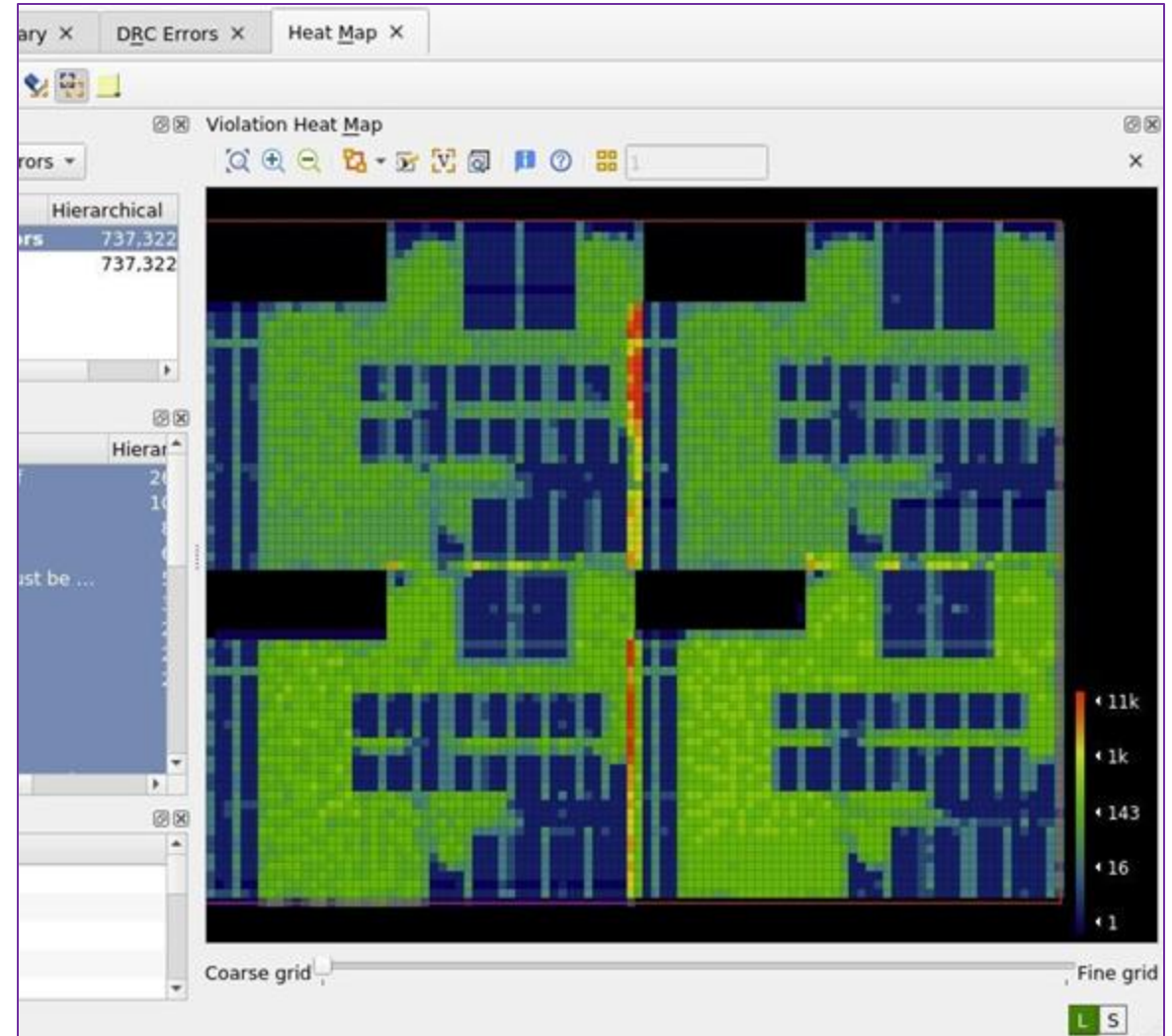
# ICV Productivity Flows

## ICV Explorer

# DRC Explorer



- Feature to debug dirty and gross problems in the design.
- Less hardware resources and time.
- Add “-explorer standalone” in the cmdfile



# DRC Explorer



## • DRC Explorer Tiers

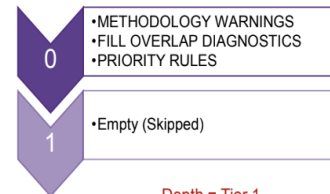
-explorer standalone → Tiers 0 to 1 always run

-explorer auto:N → Tiers 0 to N are eligible to run; run may terminate early if any tier is excessively dirty.

-explorer tiers:N → Tiers 0 to N always run

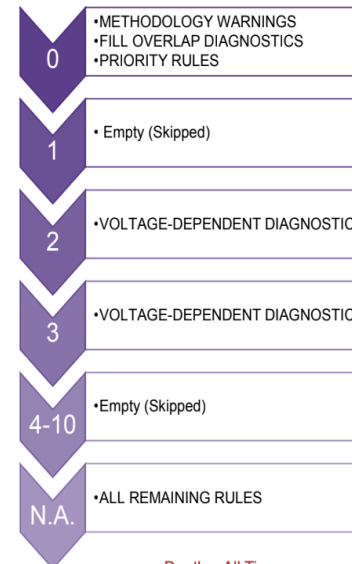
-explorer\_tiers\_file <file> → optional user defined Explorer tiers file

-explorer standalone



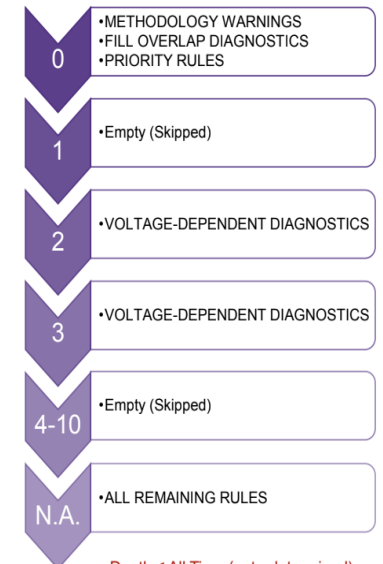
Depth = Tier 1

-explorer tiers:N



Depth = All Tiers

-explorer auto:N



Depth ≤ All Tiers (auto-determined)

# DRC Explorer



- DRC explorer helps to quickly detect the fundamental design issues.
- Running a subset of rules to flag gross problem
- Signoff and Explorer run results match.
- **10x faster** run time compared to full-signoff runs.

**Performance Statistics**

IC Validator Run Time = 28:15:17  
Peak Single Command Memory = 191,455 GB  
Peak Disk Usage = 191,455 GB  
Network Disk Usage Peak=0,750 GB (no group)  
Group File Disk Usage Peak=191,139 GB

Distributed Host Memory Usage  
snc1-fbgrid-x-07-23,thefacebook.com (16/56) .... Average=48,127 GB, Peak=181,571 GB / 754,027 GB

Overall Distributed Utilization: not available  
IC Validator is done.

**Results Summary**

Rule and DRC Error Summary

46363 total rules were run.  
1 rule NOT EXECUTED.  
552 rules have violations.  
There are 54764877 total violations.  
Refer to ath\_pe\_LAYOUT\_ERRORS

| Rule                | Violations Found |
|---------------------|------------------|
| CELL_CWR_R_8_3.ta   | v = 5650726      |
| CELL_CWR_P_7        | v = 15150895     |
| CELL_CWR_R_8_3.ta   | v = 7833481      |
| CELL_CWR_S_7        | v = 20499148     |
| CELL_COP_V_P_2_2    | v = 4            |
| CELL_F8_R_5_11      | v = 60           |
| CELL_M0_R_1         | v = 4793         |
| CELL_M0_R_2         | v = 26356        |
| CELL_M0_R_3_3_PT.T  | v = 4793         |
| CELL_M0_R_3_3.T     | v = 4793         |
| CELL_OB_S_2_3_1     | v = 6            |
| CELL_OB_S_2_3_3     | v = 30           |
| CHOR_U_2_0_1        | v = 1            |
| CHOR_U_2_1_PT.T     | v = 1            |
| CHOR_U_2_1_1.T      | v = 1            |
| CHOR_U_2_1_1_0.T    | v = 1            |
| CHOR_U_2_1_1.T      | v = 1            |
| CHD_S_7_2           | v = 9            |
| COO_V_R_4_2         | v = 46           |
| COO_V_S_3           | v = 4            |
| EFP_M3_R_26         | v = 2            |
| EFP_M3_R_26_1       | v = 14           |
| EFP_M4_R_26         | v = 8            |
| EFP_M4_R_26_1       | v = 8            |
| G_M11_4_2_0.ta      | v = 2            |
| G_M14_4_2_0.ta      | v = 18           |
| G_M15_4_2_0.ta      | v = 53           |
| G_M16_4_2_0.ta      | v = 15           |
| G_M17_4_2_0.ta      | v = 112          |
| G_M6_4_2_0.ta       | v = 8            |
| G_VIAB_4_2_0.ta     | v = 4            |
| LIF_P_4_1           | v = 1            |
| MO_A_2_1_1.ta       | v = 26356        |
| MO_CS_13            | v = 26354        |
| MO_CS_13_1          | v = 26354        |
| MO_CS_13_2          | v = 26354        |
| MO_CS_38_2.ta       | v = 2            |
| MO_CS_38_3_1.ta     | v = 2            |
| MO_CS_38_4_2_1_1.ta | v = 2            |
| MO_CS_38_4_2_1_2.ta | v = 2            |
| MO_CS_38_4_2_1.ta   | v = 2            |
| MO_A_2_1_30.T       | v = 105415       |
| MO_L_2_1.T          | v = 1            |
| MO_L_2_30.T         | v = 105415       |
| MO_L_2.T            | v = 1            |
| MO_R_1.T            | v = 1            |
| MO_R_10_1_1.ta      | v = 13178        |
| MO_R_10_1_1.T       | v = 1            |
| MO_R_10_3_2_1.ta    | v = 1            |
| MO_R_10_3_2.ta      | v = 1            |
| MO_R_20_7_20        | v = 1            |
| MO_R_5              | v = 977035       |
| MO_S_31_2_1         | v = 2            |
| MO_S_31_2_2         | v = 2            |
| MO_S_31_2_3         | v = 2            |
| MO_S_38_4_2_1.ta    | v = 2            |
| MO_S_38_4_2_2.ta    | v = 2            |

**Performance Statistics**

IC Validator Run Time = 2:27:28  
Peak Single Command Memory = 6,739 GB  
Peak Disk Usage = 29,302 GB  
Network Disk Usage Peak=0,083 GB (no group)  
Group File Disk Usage Peak=29,271 GB

Distributed Host Memory Usage  
snc1-fbgrid-y-04-27,thefacebook.com (16/56) .... Average=29,604 GB, Peak=73,344 GB / 754,027 GB

Overall Distributed Utilization: not available  
IC Validator is done.

**Results Summary**

Rule and DRC Error Summary

Methodology Warnings  
1 rule was run.  
There are 0 Methodology Warnings.

Fill Overlap Diagnostics  
31 rules were run.  
There are 0 Signoff Violations.

Macroblock Overlap Diagnostics  
0 rules were run.  
There are 0 Signoff Violations.

Priority Rules  
4524 rules were run.  
0 suspect assign layers were identified.  
There are 38345 Signoff Violations.

Priority Rules (User-Specified)  
0 rules were run.  
There are 0 Signoff Violations.

Voltage-Dependent Diagnostics  
0 rules were run.  
There are 0 Signoff Violations.

Multi-Patterning Diagnostics  
0 rules were run.  
There are 0 Signoff Violations.

All Remaining Rules  
0 rules were run.  
There are 0 Signoff Violations.

TOTAL  
4652 total rules were run.  
11705 rules NOT EXECUTED.  
53 rules have violations.  
There are 38345 total violations.  
Refer to ath\_pe\_LAYOUT\_ERRORS

Signoff Status: N/A (Explorer only run)

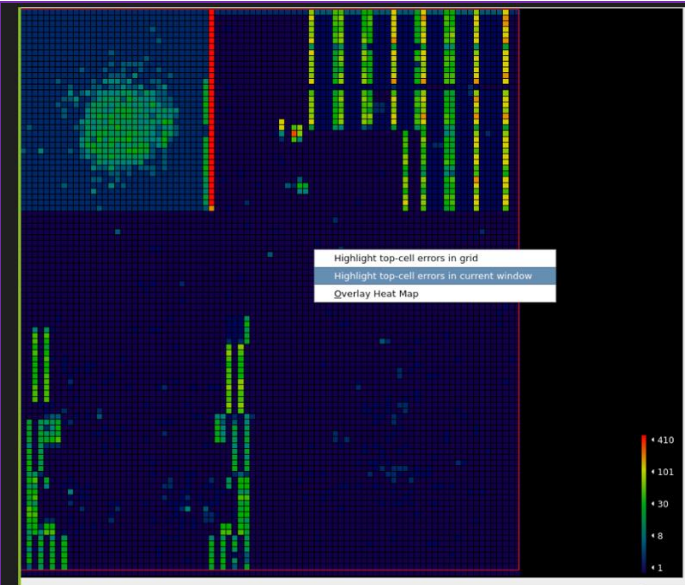
**Priority Rules**

| Rule           | Violations Found |
|----------------|------------------|
| M5_R_1_1.T     | v = 21836        |
| M0_R_10_1_1.ta | v = 13178        |
| M17_S_1_1.T    | v = 624          |
| M16_S_1_1.T    | v = 537          |
| M5_S_1_1.T     | v = 483          |
| M6_S_1_1.T     | v = 432          |
| M18_S_1_1.T    | v = 304          |
| M15_S_1_1.T    | v = 113          |
| M10_S_1_1.T    | v = 84           |
| M4_S_1_1.T     | v = 67           |

# DRC Explorer

## Heatmap

- DRC heat-map to find problematic areas.
- Controls to highlight all rules heatmap or single rule heatmap.
- Controls to overlay heatmap to the actual layout.



| Category                    | Hiera | 12 rules<br>24 errors | 12 rules<br>12 errors | 13 rules<br>24 errors | 4 rules<br>21 errors | 4 rules<br>20 errors |
|-----------------------------|-------|-----------------------|-----------------------|-----------------------|----------------------|----------------------|
| Explorer-Categorized Errors |       |                       |                       |                       |                      |                      |
| Priority Rules              |       |                       |                       |                       |                      |                      |
|                             |       | 12 rules<br>22 errors | 12 rules<br>12 errors | 12 rules<br>25 errors | 4 rules<br>21 errors | 4 rules<br>20 errors |
| Violation Selection         |       | 12 rules<br>22 errors | 13 rules<br>14 errors | 13 rules<br>24 errors | 4 rules<br>21 errors | 4 rules<br>20 errors |
| Violation/Function          |       | 12 rules<br>22 errors | 12 rules<br>12 errors | 13 rules<br>25 errors | 4 rules<br>21 errors | 4 rules<br>20 errors |
|                             |       | 12 rules<br>22 errors | 12 rules<br>12 errors | 13 rules<br>24 errors | 4 rules<br>21 errors | 4 rules<br>20 errors |
|                             |       | 12 rules<br>22 errors | 12 rules<br>12 errors | 13 rules<br>25 errors | 4 rules<br>21 errors | 4 rules<br>20 errors |



# LVS Explorer



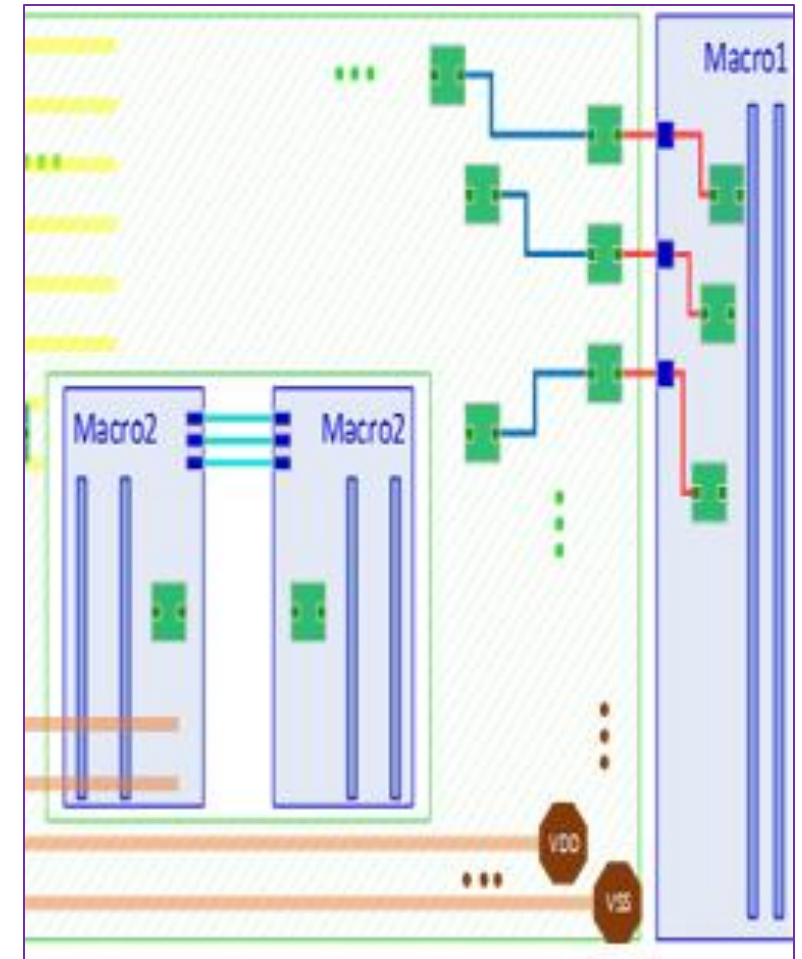
- The LVS Explorer feature helps to quickly find top-level shorts and other connectivity issues without running full LVS.
- 5x Faster run time to find the same short.
- Debug and short isolation is same as regular LVS
- Add “-explorer lvs:1” option in cmdfile

```
lvsServer shutdown
IC Validator Machine Memory Report
src1-fbgridz-05-31,thefacebook.com : Average = 20,892 GB, Peak = 66,170 GB

Overall Disk Usage Disk=15,879 GB
Network Disk Usage Peak=5,480 GB (no group)
Group File Disk Usage Peak=11,443 GB
Overall Design Hierarchy Mem=0,292 GB
Overall engine Time=0:45:04 Highest command Mem=11,902 GB
Overall Memory Peak=16,704 GB

lvsServer shutdown
IC Validator Machine Memory Report
src1-fbgridz-12-09,thefacebook.com : Average = 8,130 GB, Peak = 24,908 GB

Overall Disk Usage Disk=8,722 GB
Network Disk Usage Peak=0,034 GB (no group)
Group File Disk Usage Peak=8,688 GB
Overall Design Hierarchy Mem=0,002 GB
Overall engine Time=0:09:25 Highest command Mem=3,857 GB
Overall Memory Peak=1,007 GB
```

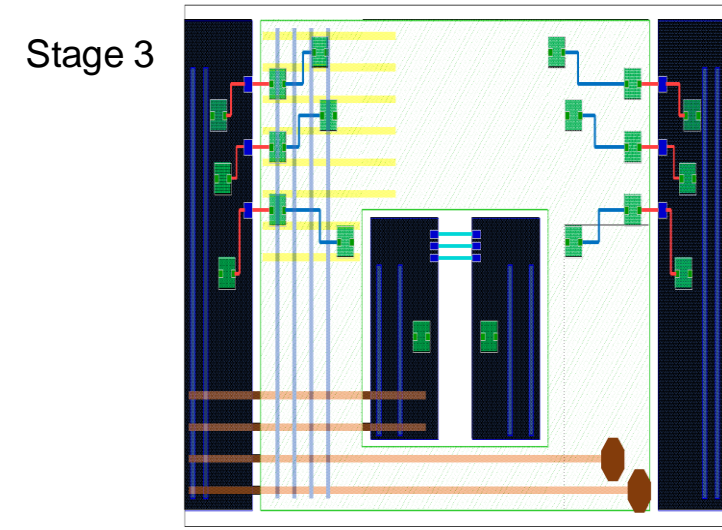
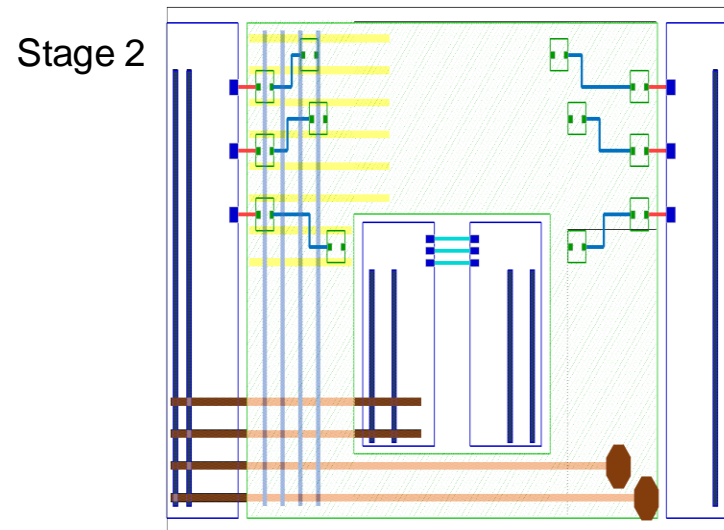
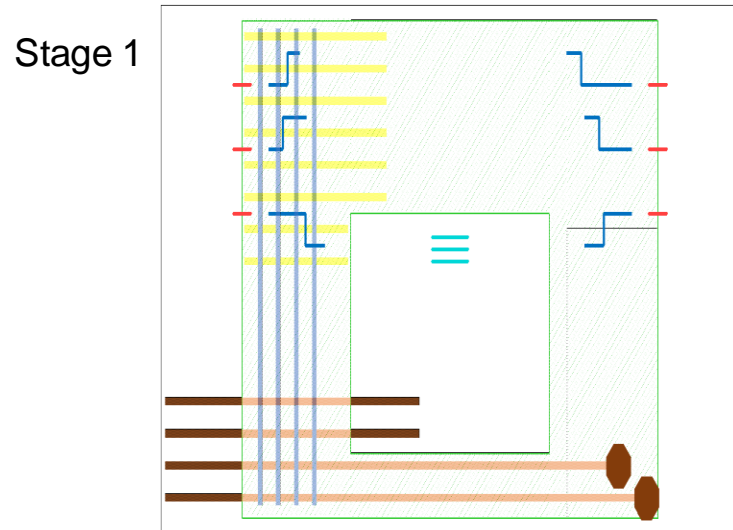


# LVS Explorer



## Stages of LVS explorer

|         | Extract                               | Compare        | Description                        |
|---------|---------------------------------------|----------------|------------------------------------|
| Stage 1 | Metal only; Delete equiv cells        | None           | Metal only, text based short check |
| Stage 2 | Metal only; only pins for equiv cells | Black box only | Top level interconnectivity check  |
| Stage 3 | Full; all layers, all data            | Full           | Full LVS check                     |



# LVS Explorer



The screenshot shows the 'Short Finder' tab in LVS Explorer. The main window displays 'LAYOUT ERRORS RESULTS' with a red 'ERRORS' header. Below this is a blue bar for 'DRC Error Statistics' containing the following information:

- Library name: [redacted]
- Structure name: ath\_pe\_sfu
- Generated by: IC Validator RHEL64 V-2023.12.9489491 2023/12/04
- Runset name: [redacted]
- User name: [redacted]
- Time started: 2024/01/26 02:53:38PM
- Time ended: 2024/01/26 03:01:49PM

Below the statistics, it shows the command used: `Called as: icv -host_init 16 -clf icv cmd options file` and `CLF: -explorer lvs:1 -e ../`. A red box highlights the 'Short Finder' tab, and a red box highlights the 'DRC Errors' section.

This screenshot shows a layout viewer window with a dark background. A red rectangular box highlights a specific path on the layout. A blue arrow points from the 'Short Finder' tab in the previous screenshot to this layout viewer, indicating the transition from error identification to visual inspection.

- Using Short finder to debug that short.
- Highlight controls to highlight each layer on the shorted path. Highlight by net or by cells.

This screenshot shows the 'Short Finder' tab with a detailed error list and violation details. The 'Violation Browser' shows a table with the following data:

| Violation/Cell/Function           | Error | Total Errors |
|-----------------------------------|-------|--------------|
| text_net:text_short (/DFM LVS RC) | 1     | 1            |
|                                   | 1     | 1            |

The 'Error List' shows a single error: `Error E.1.100.1 N_2` with details: `VDD 202 48 (0.6750, 5.4340) M18 LAYER`. The 'Violation Detail' section shows the violation path: `text_net:text_short (/DFM LVS`.



# Summary



- Meta is using IC Validator for PV signoff runs.
- Features like Layer\_debugger and Short finder help to debug design issues faster and efficiently.
- Features like Explorer providing faster results with less resources and runtime.



***THANK YOU***

***YOUR  
INNOVATION  
YOUR  
COMMUNITY***