Unleashing Efficiency: Cloud-Powered Advancements in Physical Verification for Advanced Semiconductor Nodes

Vilesh Shah, Shantanu Divekar, Vikash Tyagi, Evan Chen
Astera Labs

Agenda

- About Astera Labs
- PV Challenges for Connectivity and Ultra-High Bandwidth Designs
- PV Signoff flow in Astera Labs
  - Cloud and ICV
- Synopsys IC Validator(TM) Methodology
  - Explorer, Heat-map and DV diagnostics
  - Short Debugging
  - PERC

Astera Labs

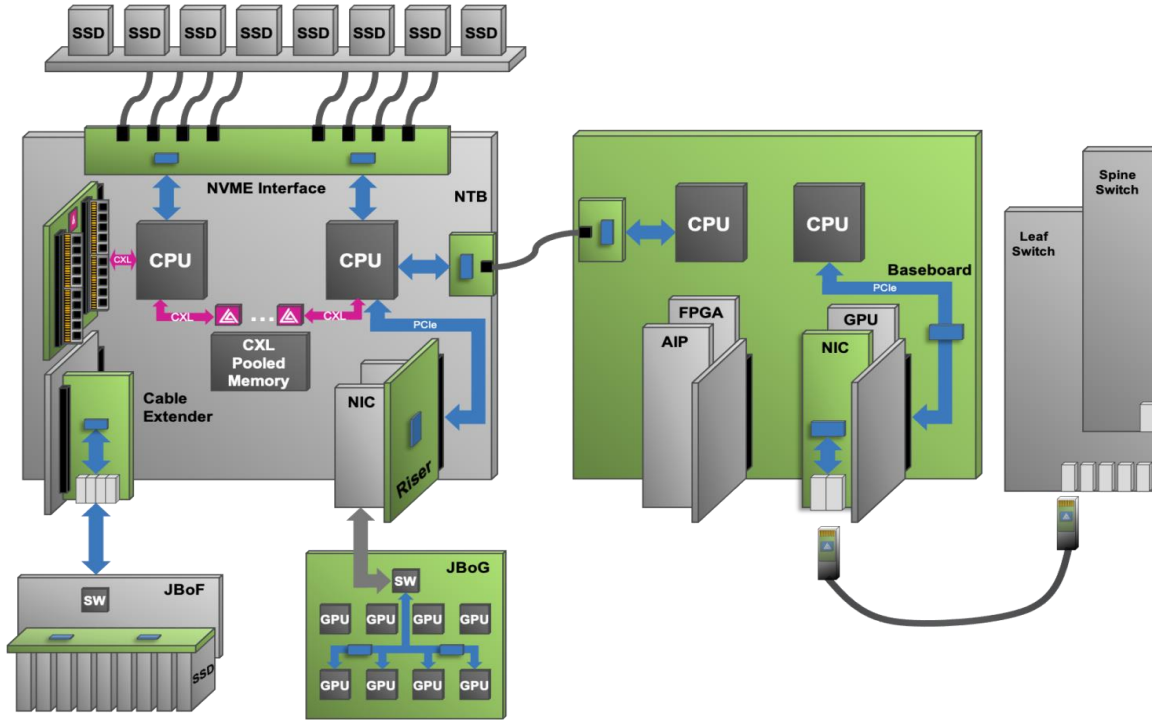
Products and Technology

Silicon and System Products to Address Performance Bottlenecks

Aries Platform
PCIe/CXL Smart DSP Retimers

Taurus Platform
200G/400G/800G Smart Cable Modules

Leo Platform
CXL memory controller acceleration



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Physical Verification Requirements

Challenges for high-bandwidth designs

- Fast performance is a key requirement
  - Early design verification with dirty block/chip level data is usually time-consuming
  - Long runtimes due to PG shorts across complex power domains
- DRC closure in 5nm/7nm is challenging
  - Aligning FIN and PO across the blocks
  - Analog/Digital IP from different companies needs to follow different placement grid
- Base density issues near IP edge
  - IP base layers where Foundry fill deck is not friendly
- The LUP violations closer to high voltage IP requires a lot of up-front planning since they must meet very strict LUP density and spacing rules from Foundry
- DRC runs scale very linearly with number of CPUs available – we used from 4 cpu to 384 cpu jobs spread over multiple servers

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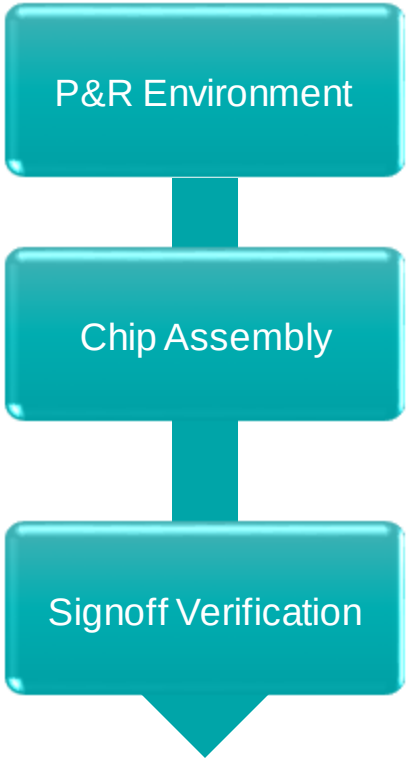
Astera Labs Physical Verification Flow



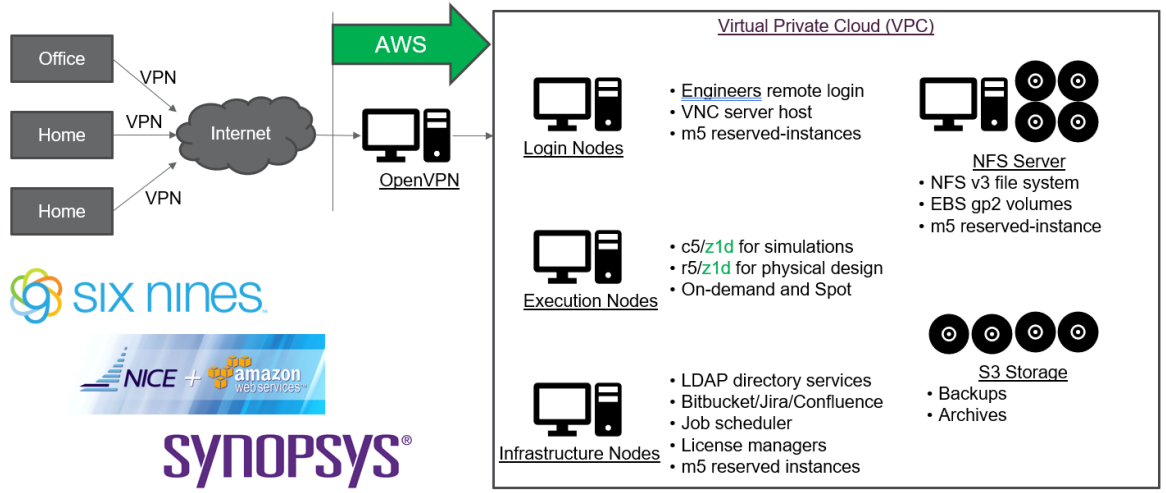
- Place & Route (Synopsys Fusion Compiler(TM))
  - Floorplan to chip finish
  - Tech file-based DRC
- Chip assembly
  - merged in Synopsys FC
- Full chip Verification (Synopsys IC Validator)
  - DRC (FEOL, BEOL, VDR)
  - LVS
  - Antenna
  - FILL
  - PERC

15+ PV signoff with ICV for N16/N7/N5 Nodes.

AWS Cloud for Physical Verification

On-Demand scaling for fast performance

- AWS Cloud resources used for all design flow, including physical verification
- On-Demand resource access enables to scale physical verification jobs for faster runtime
- Synopsys IC Validator is cloud friendly, easy to setup and great scalability



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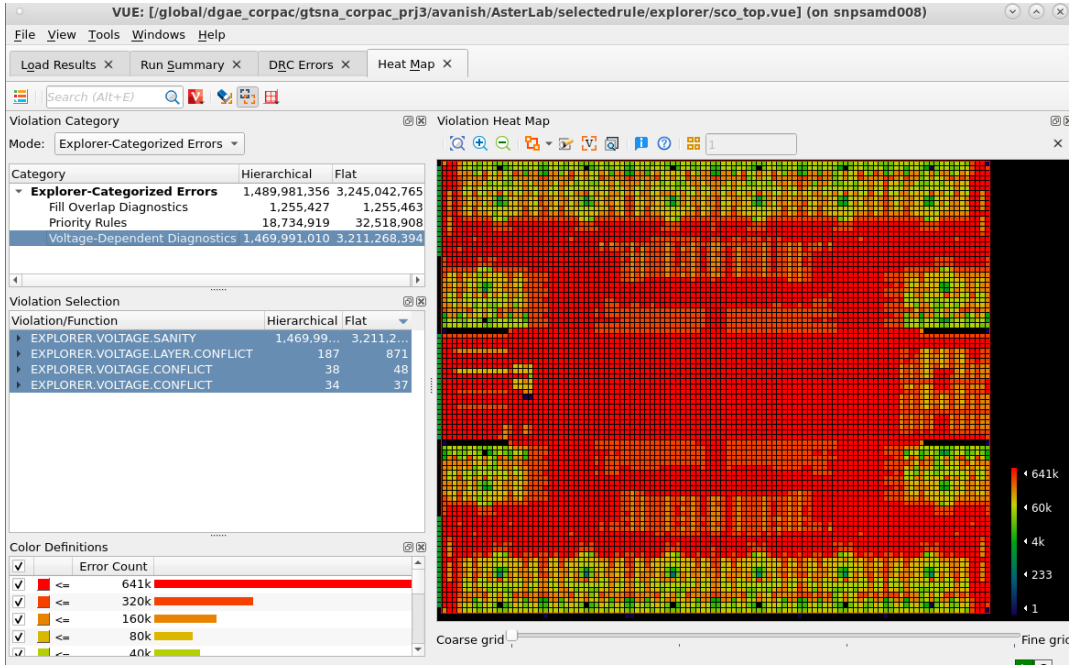
Quick Verification During Early Design Stage

- Synopsys IC Validator Explorer DRC enables fast DRC for early design verification
  - Quickly checks fundamental design issues
  - Fix large design issues before signoff
- Easy debugging with DRC heatmap
- Voltage dependent diagnostics for VDR rule

Run Time		
No of CPUs	DRC Explorer Runtime (Hrs.)	DRC Run time
32	3:00:50	18+ Hrs.

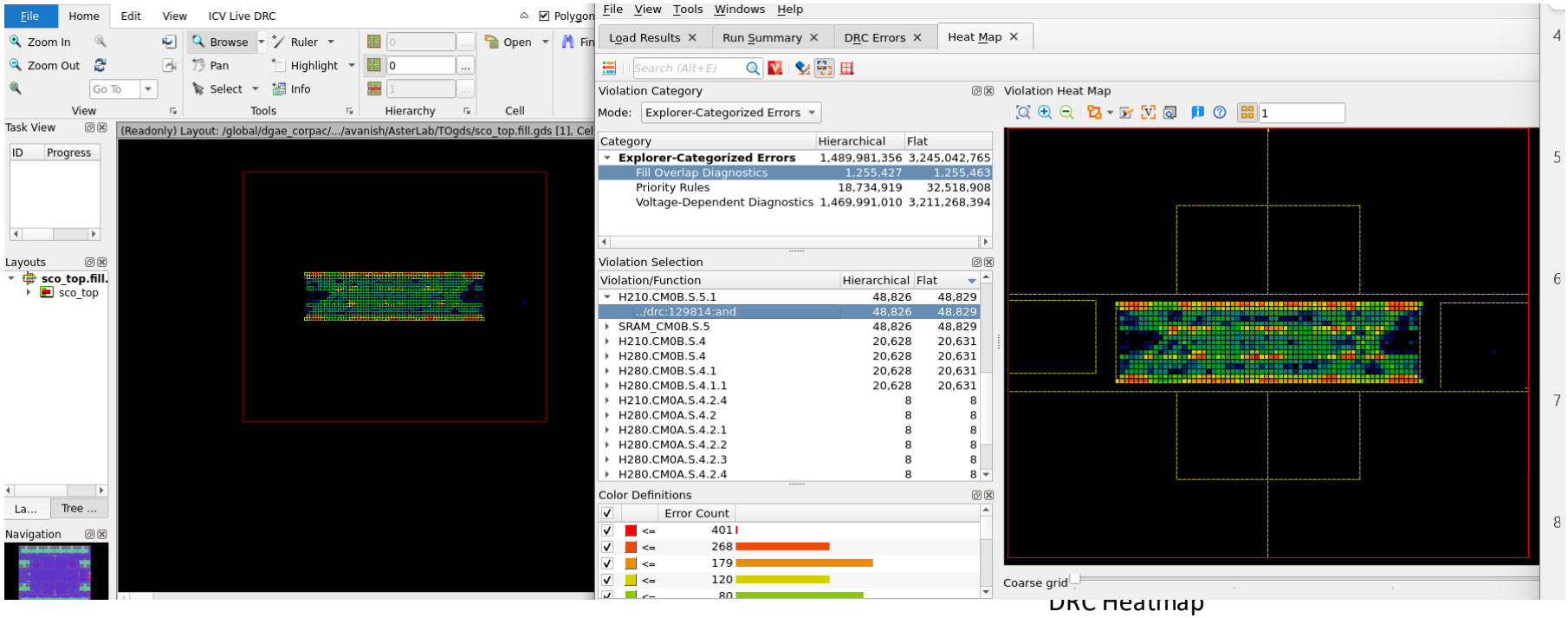


DRC Heatmap

Faster dirty design verifications

Quick Verification During Early Design Stage

- **Fill Overlap Diagnostics**
  - Heatmap helped to identify the region and the cells causing these violations
  - HDBELT* cells placed in the center have issues.

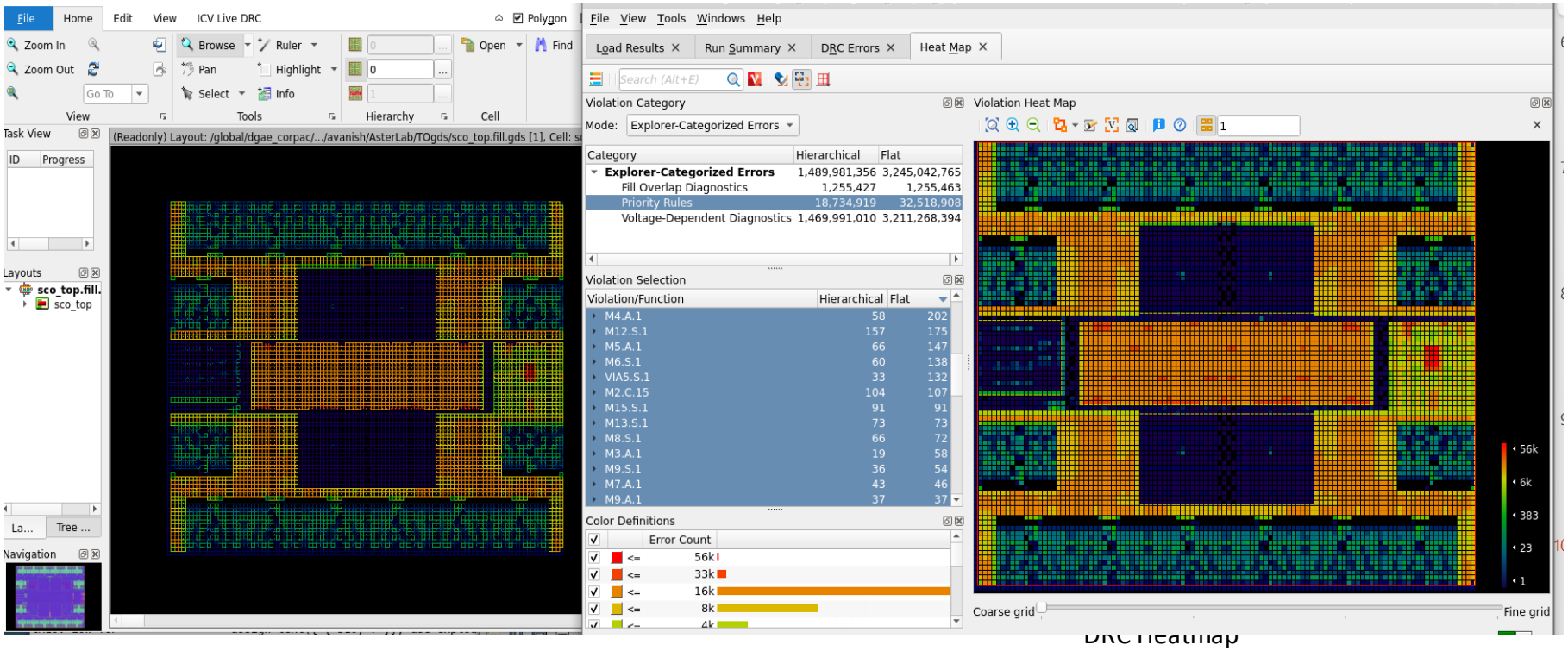


DRC Heatmap

Faster dirty design verifications

Quick Verification During Early Design Stage

- **Priority Rules**
  - ~18 million signoff rules violations were flagged by DRC explorer.
  - Heatmap for all these rule helped to debug these issues faster.

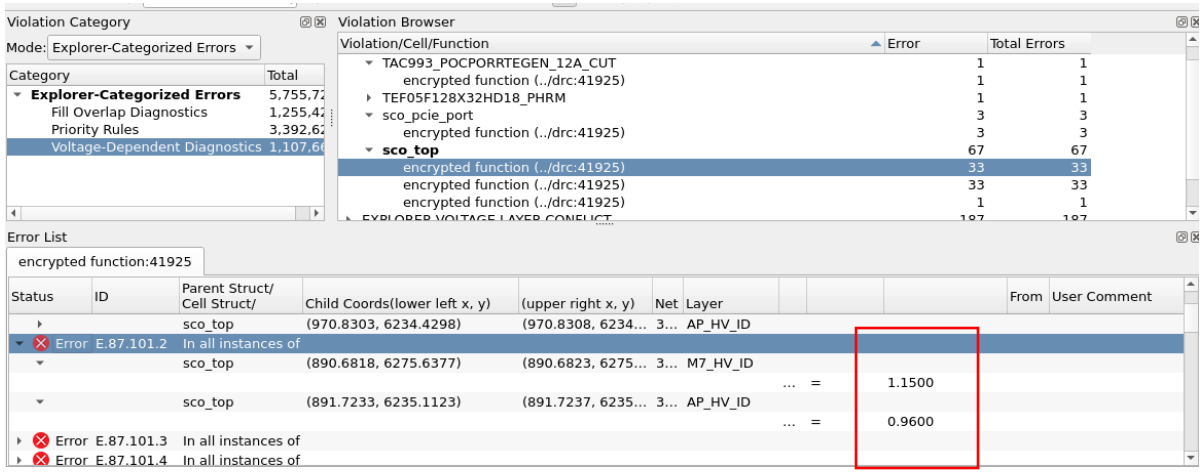


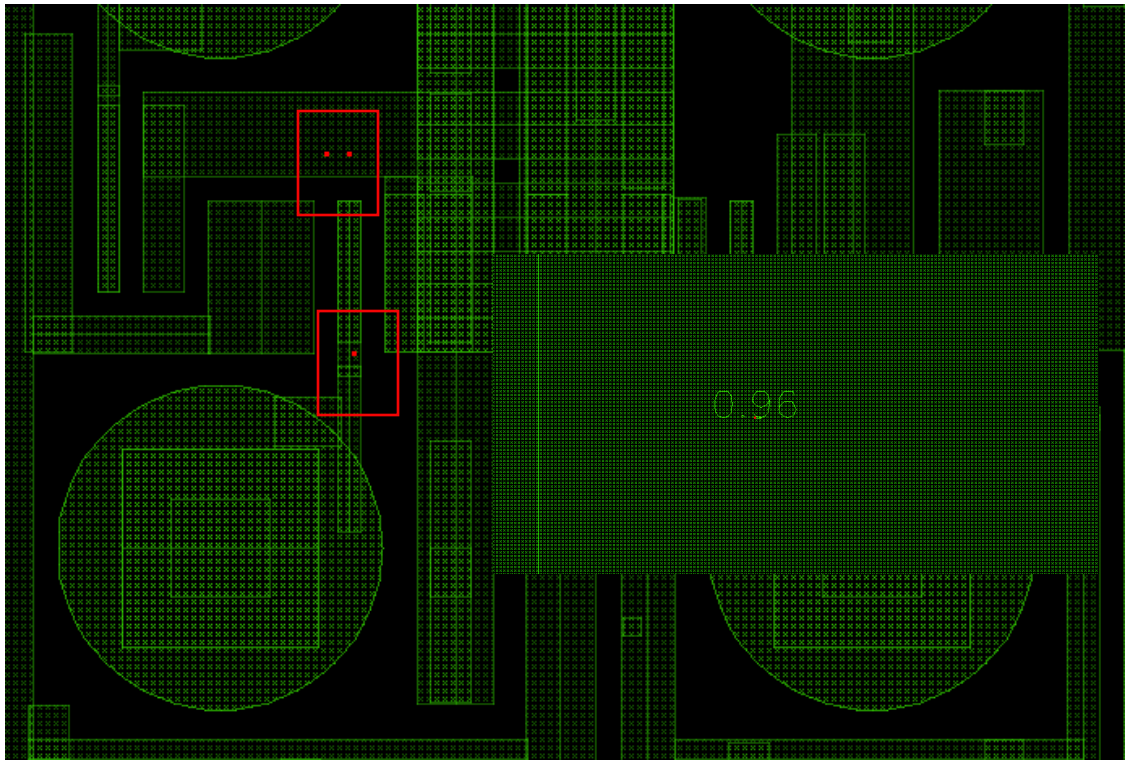
DRC Heatmap

Faster dirty design verifications

Quick Verification During Early Design Stage

- **Voltage-dependent diagnostic**
  - **EXPLORER.VOLTAGE.CONFLICT**
  - EXPLORER.VOLTAGE.LAYER.CONFLICT
  - EXPLORER.VOLTAGE.SANITY





Faster dirty design verifications

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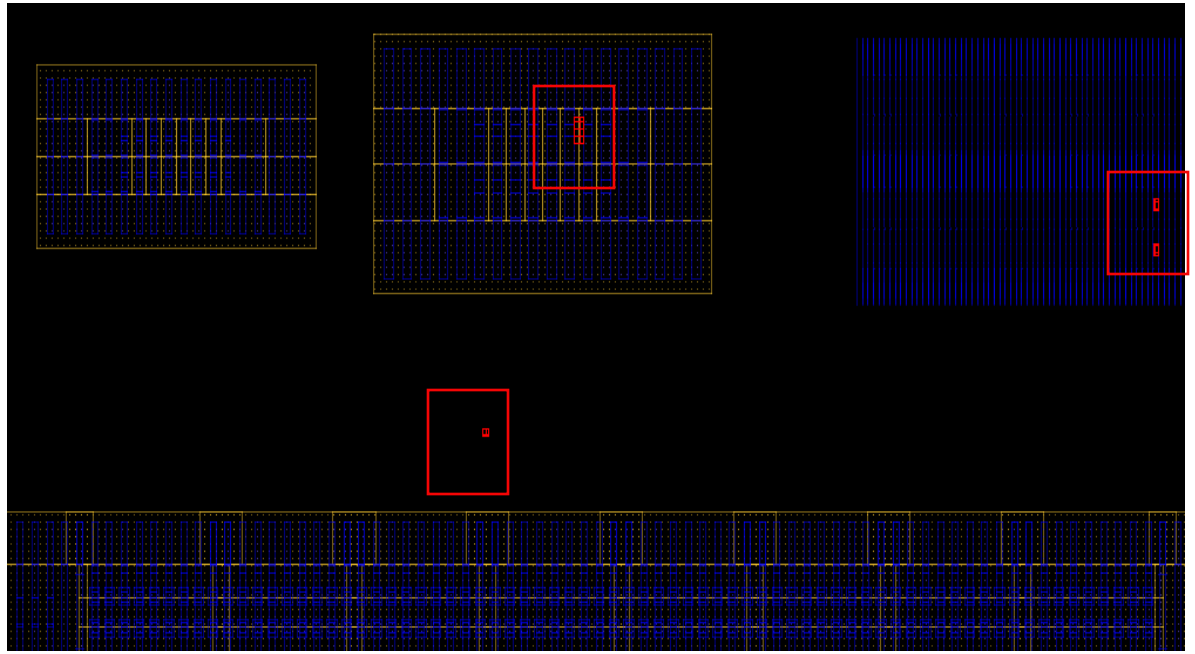
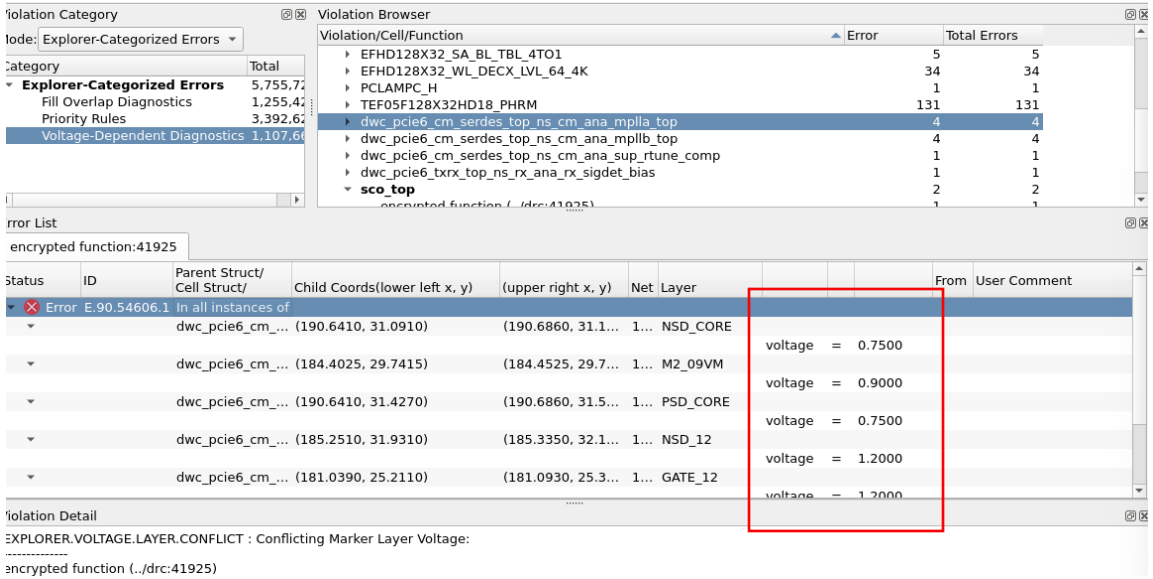
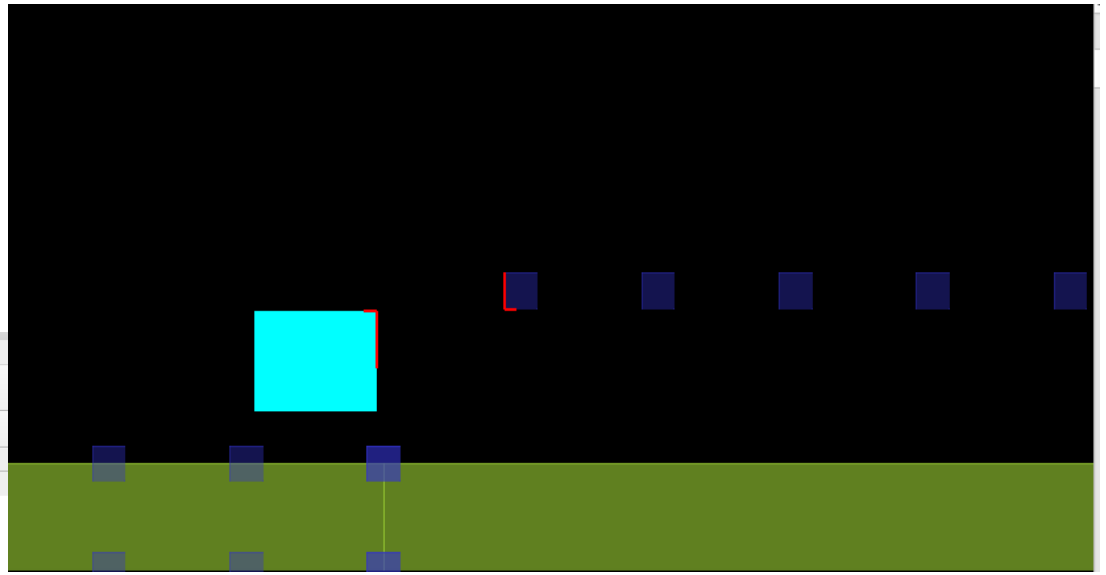




Faster dirty design verifications

Delta Voltage Rule debugging

- Delta voltage debug features helped to debug DV rule faster
- Traditionally we just see error markers



File View Tools Classification Windows Help

Load Results × | Run Summary × | DRC Errors ×

Custom Filter | Search (Alt+E)

Violation Browser

Violation/Cell/Function	Error	Total Errors
layout_drawn_errors:missing_cell	1	1
VC.S.6.1:VC	10,628	10,628
sco_top	10,628	10,628
dv_error_voltage_source_error_nets (./drc:217912)	10,000	10,000
dv_error_voltage_source_error_nets (./drc:217928)	628	628

Error List

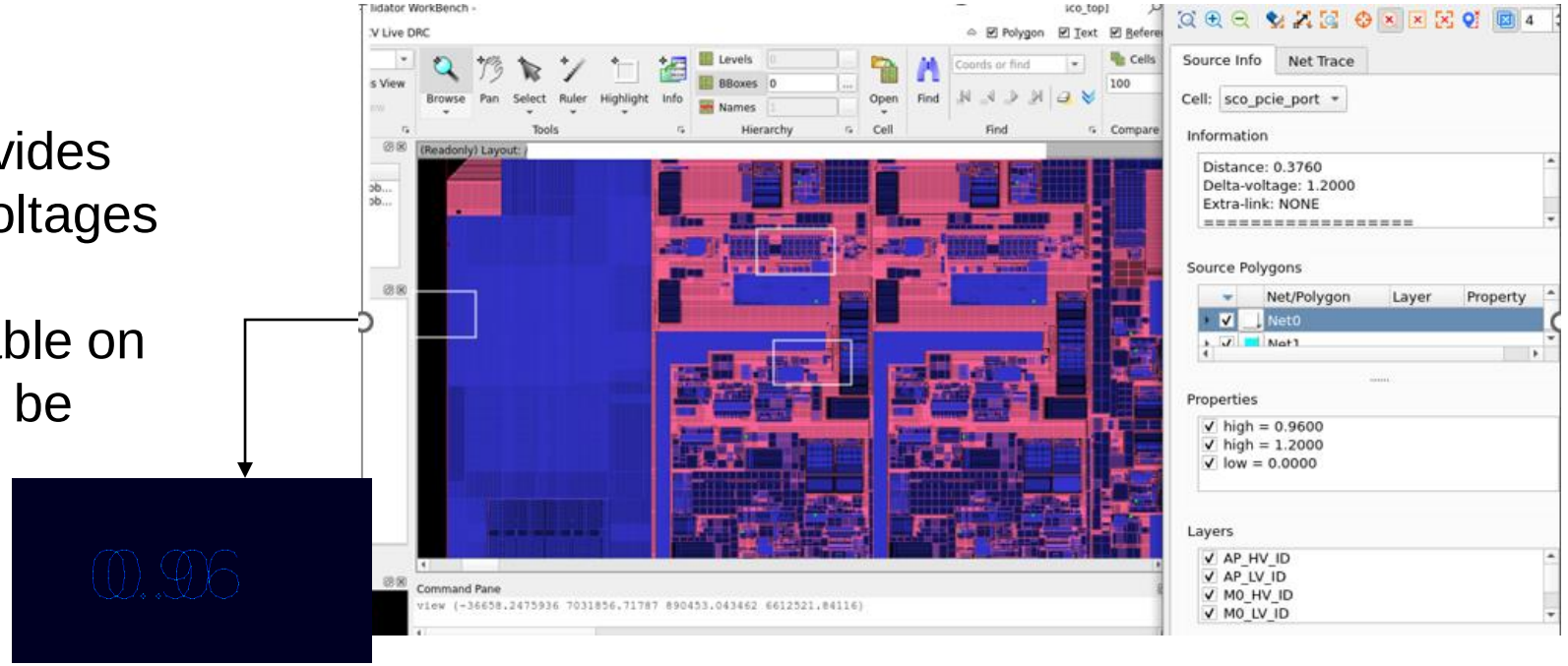
dv_error_voltage_source_error_nets:217912

Status	ID	(lower left x, y)	(upper right x, y)	Distance	Delta-voltage	Extra-link	Property1	Property1 source	Property2	Property2 source
Error	E.10.101.1	(0.7070, 6963.6700)	(0.7630, 6963.6710)	0.0480	1.9800	NONE	high = 1.9800	(group = MVH, property = high)	low = 0.0...	(group = MVL, property ...
							high = 0.7500	(group = NSD_CORE, property = high)	low = 0.0...	(hard-coded)

Faster Delta Voltage Rule Debugging

Delta Voltage Rule debugging

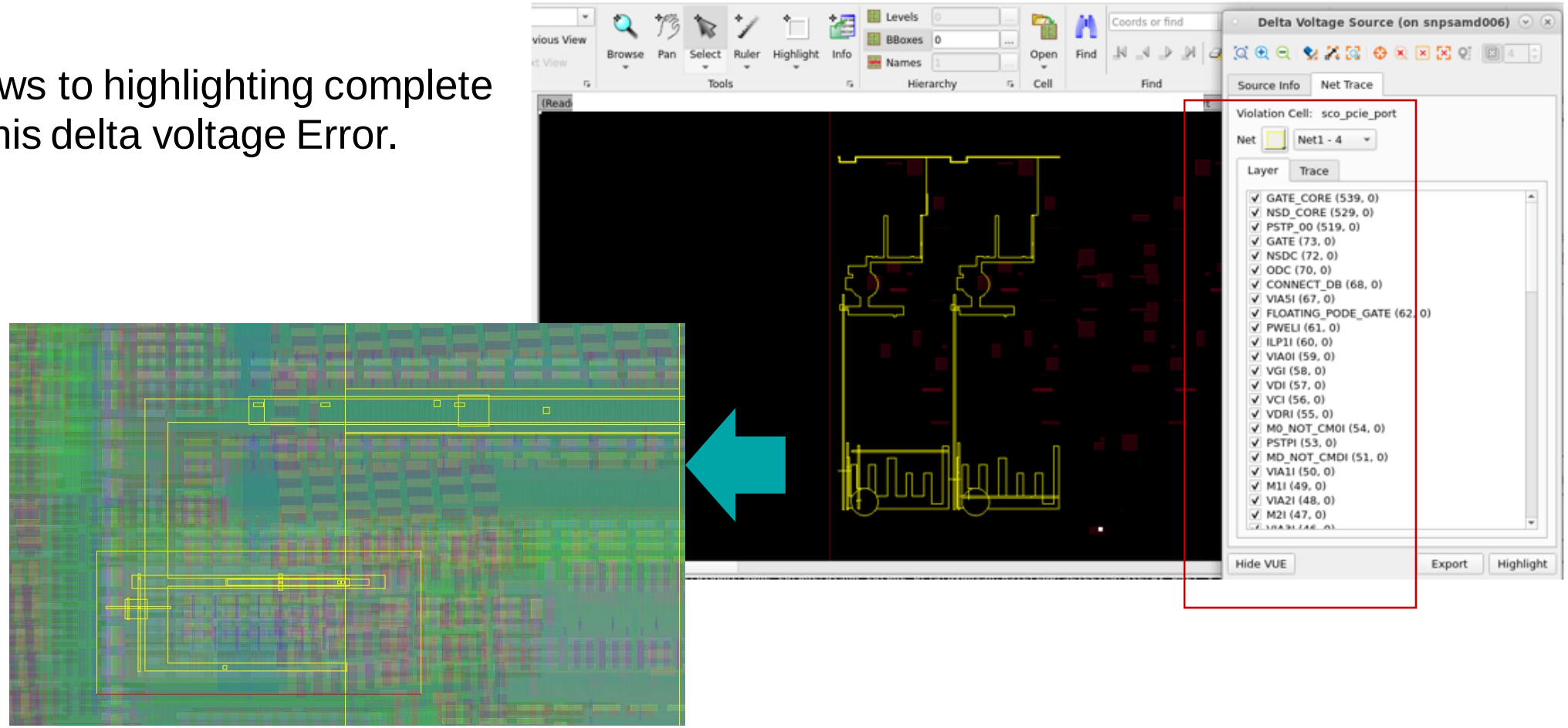
- Delta voltage debug GUI provides controls to highlight source voltages
- All the source voltages available on the net causing this error can be highlighted.



Faster Delta Voltage Rule Debugging

Delta Voltage Rule debugging

- Net trace allows to highlighting complete net causing this delta voltage Error.



Faster Delta Voltage Rule Debugging

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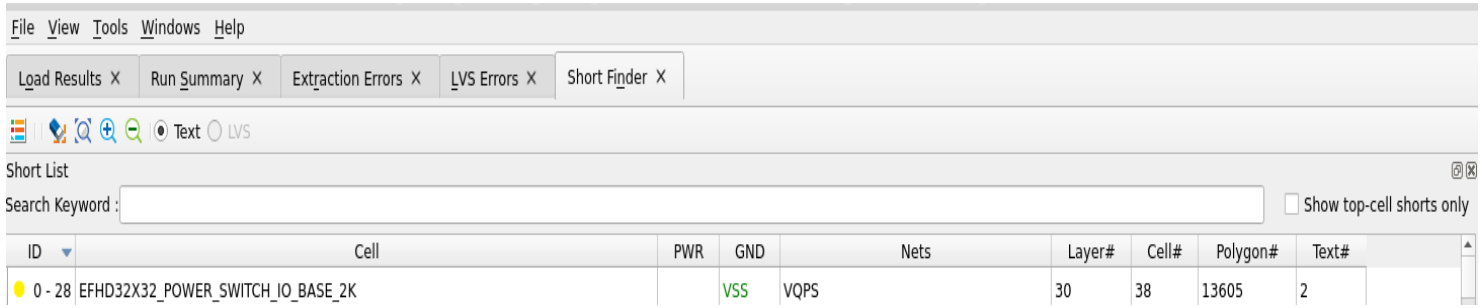
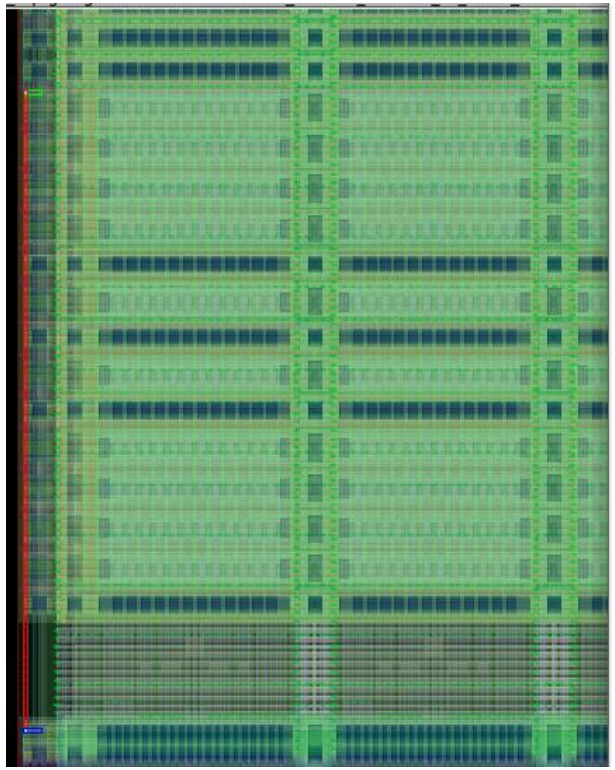
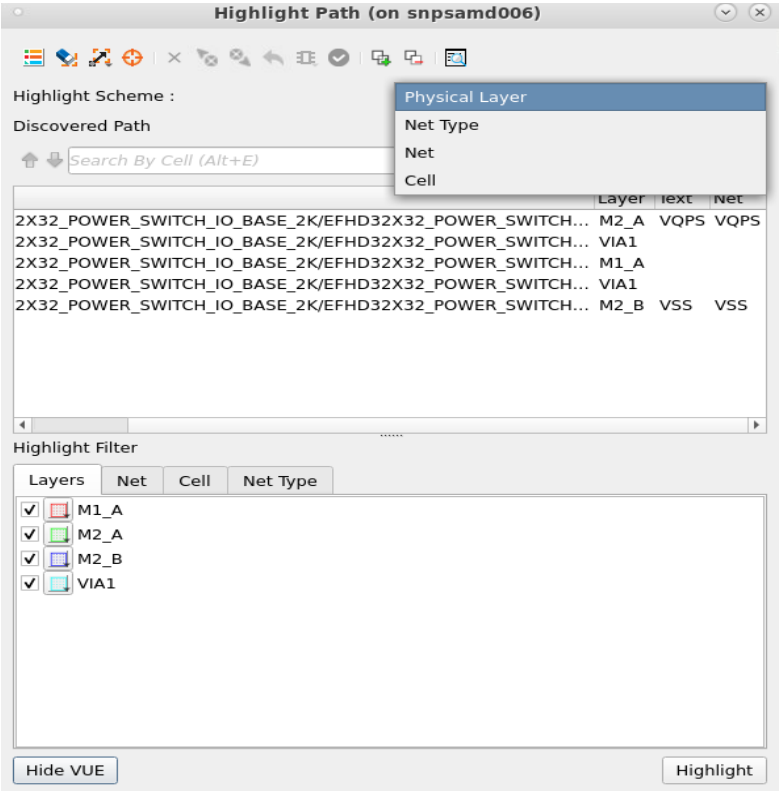
LVS Short-Finder

- Interactive short debugging using short finder utility.
- The shorted path of the short is highlighted with the option to emulate the fixes without re-running LVS again

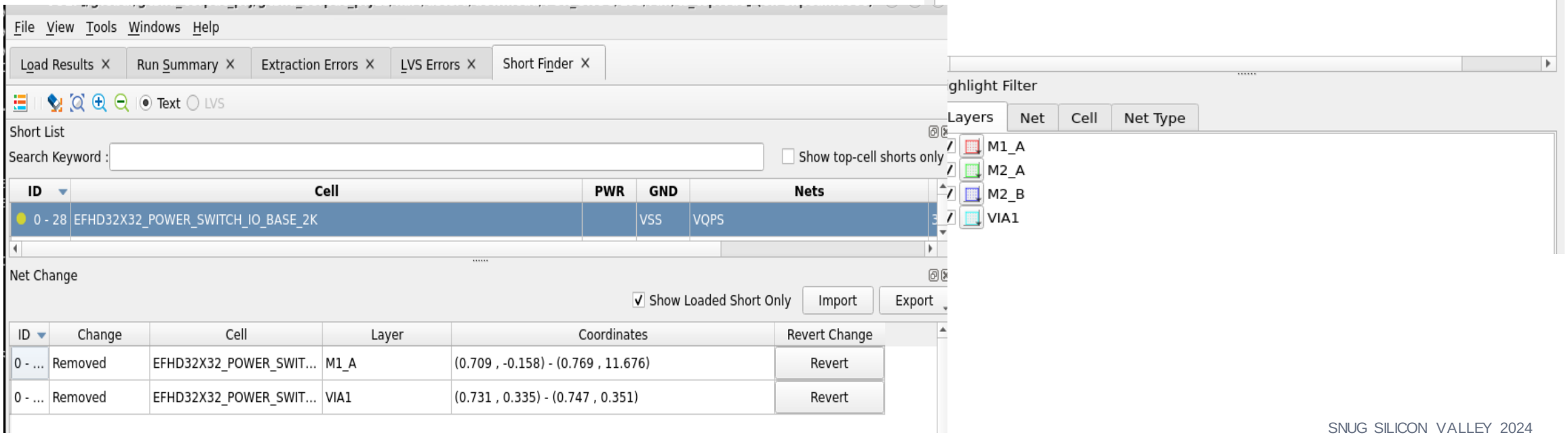






LVS Short-Finder

- Emulate the possible fixes by analyzing the short
- Once the short is clean do those fixes in the layout. All required information are available in VUE.



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Synopsys IC Validator PERC Results

ICV PERC Results on N5 Design		
PERC Flow	**No of CPUs**	**Runtime (Hrs.)**
Netlist/Topological checks	32	1:54:13
Point to Point (P2P) Resistance check	32	11:11:07
Current Density (CD) checks	32	10:18:20

- Running all rules form foundry provided PERC deck
- Synopsys StarRC(TM) bases extraction for P2P and CD checks

Full Chip PERC verification

Synopsys ICV PERC Flow Run Result Reports

Summary of Clamp Network

Power	Ground	Clamp Type	nfin
VDD	VSS	Single	4923840.00
VDDIO	VSS	Single	1168128.00
VP	GD	Single	3878400.00
VPDIG	GD	Single	775680.00
VPH	GD	Single	5564928.00
VPOD	GD	Single	7425024.00
VQPS	VSS	Cascoded (2-stage)	85078.00

ESD Network File

Summary of I/O ESD Network

I/O	Power	Ground	Primary Up (Type)	Primary Down (Type)	Secondary Up (Type)	Secondary Down (Type)	Clamp Type	nfin
A_PERN0	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN1	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN10	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN11	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN12	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN13	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN14	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN15	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN2	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN3	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN4	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN5	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN6	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN7	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00
A_PERN8	VPH	GD	PRIMARYUPDIO (Single)	PRIMARYDOWNDIO (Single)	SECONDARYUPDIO (Single)	SECONDARYDOWNDIO (Single)	Single	5564928.00

ESD Path Resistance Information

P2P measurements by rule check / path

Multiple lines with the same colors indicate a group of segments on the same path

Source Pin : Secondary down anode -> Sink Pins : Closest clamp group

Path ID	Source	Sink	Segment	Net	Segment Res (Ohms)	Total Path Res (Ohms)	Rule Limit (Ohms)	Rule Name	Pass / Fail
01213_0_01213_00000	I_7194D1FA372805___I_7194D1FA2135819___I_7194D1FA3680736___I_7194D1FA2774518___N_2564235 (IO: A_PETP5)	GD	1 of 1	GD	2.7265	2.7265	10.0	ESD.14.5.1gU	☑
01214_0_01214_00000	I_7194D1FA372805___I_7194D1FA2135819___I_7194D1FA3680736___I_7194D1FA2774518___N_2564236 (IO: A_PETN5)	GD	1 of 1	GD	2.7167	2.7167	10.0	ESD.14.5.1gU	☑
01142_0_01142_00000	I_7194D1FA372805___I_7194D1FA2135819___I_7194D1FA3680736___I_7194D1FA2783956___N_1662209 (IO: A_PERP5)	GD_VPH	1 of 1	GD	4.3672	4.3672	10.0	ESD.14.5.1gU	☑
01217_0_01217_00000	I_7194D1FA372805___I_7194D1FA2135819___I_7194D1FA3680736___I_7194D1FA2783956___N_3443183 (IO: A_PERN5)	GD_VPH	1 of 1	GD	4.3369	4.3369	10.0	ESD.14.5.1gU	☑

Summary

- Synopsys IC Validator delivered full flow performance and productivity for physical signoff of leading Astera Labs design
  - DRC Explorer provided a quick and efficient method for early analysis and finding and debugging hot spots
  - Complete reliability and ESD verification with Synopsys ICV PERC

- 15+ successful tapeouts with Synopsys ICV for N16/N7/N5 designs.


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