

Silicon.da

Silicon Insights and Data Analytics from Design
to Manufacturing

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Yield Explorer + Silicondash = Silicon.da



Product Manufacturing ... from NPI through HVM



- New Product / Process
- Design Centric Analytics
- Interactive Test Analytics

- For systematic failure mechanisms
- For design – process interactions
- Logic and Memory diagnostics
- New Product Introduction and Process characterization
- Interactive data preparation and data analysis
- Custom analytics flows and reporting
- Failure Analysis link



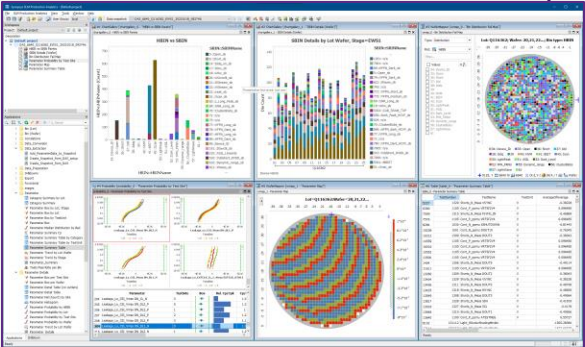
- Yield Management System
- Production / Quality Control
- Volume Test Analytics Automation

- For random and systematic yield and performance issues
- For operational issues and excursions on manufacturing flow
- Automated data mining on large volumes
- All incoming material analyzed automatically
- Web-browser high-speed analytics and reporting
- Automated production control strategies

Silicon.da Platform

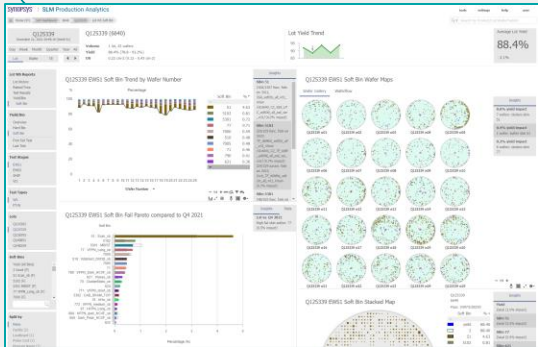


Yield Explorer
=> Local client

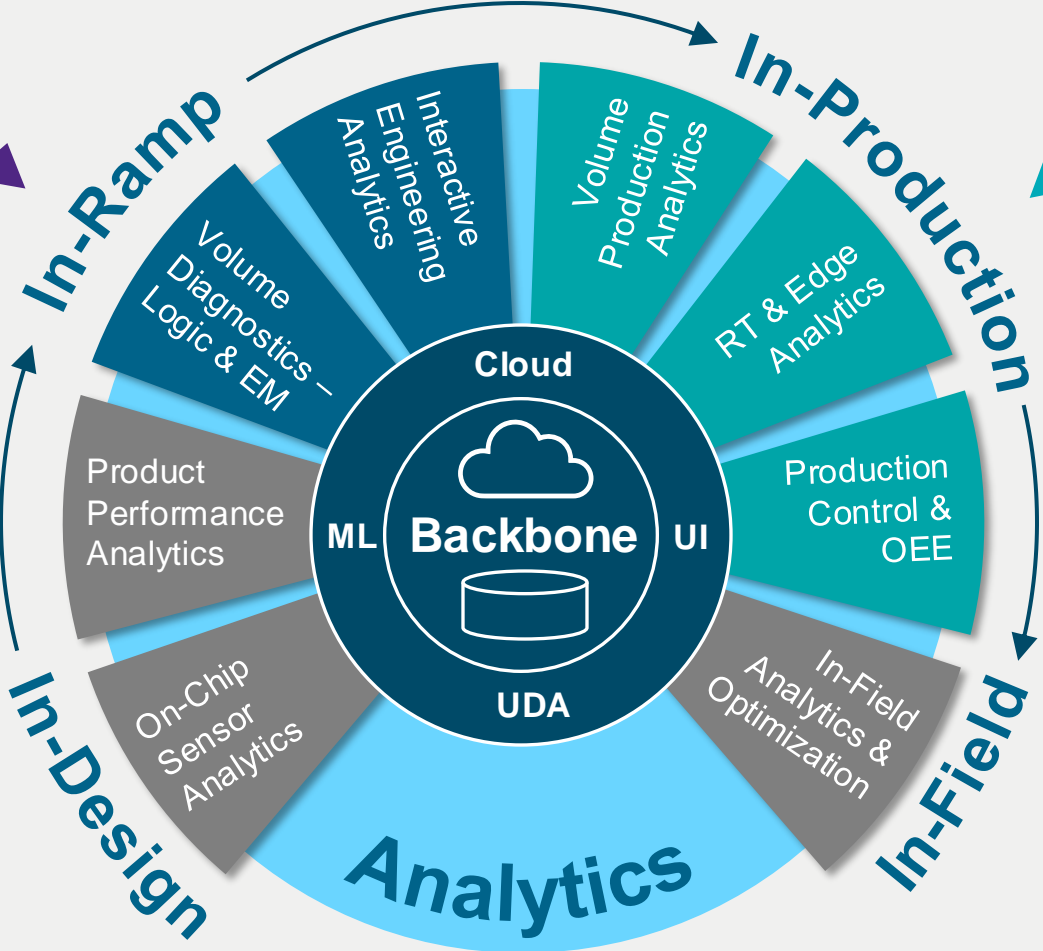


Test data (2023.03)
Diagnostics (2024.03)

Silicondash
=> Web client



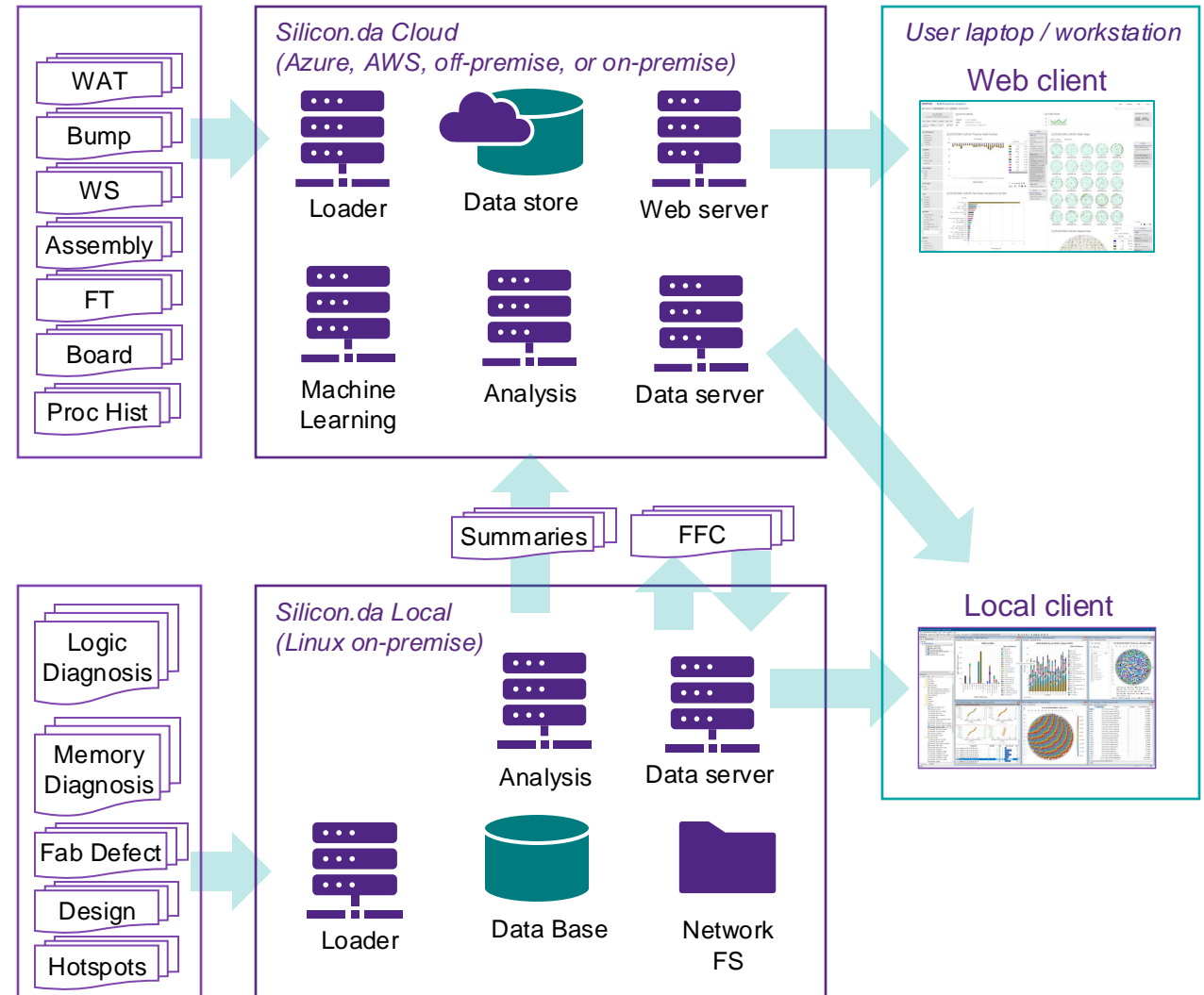
Test data (2023.03)
Diagnostics (2024.03)
ML platform (2024.03)



Platform architecture

Engineering and production data analytics

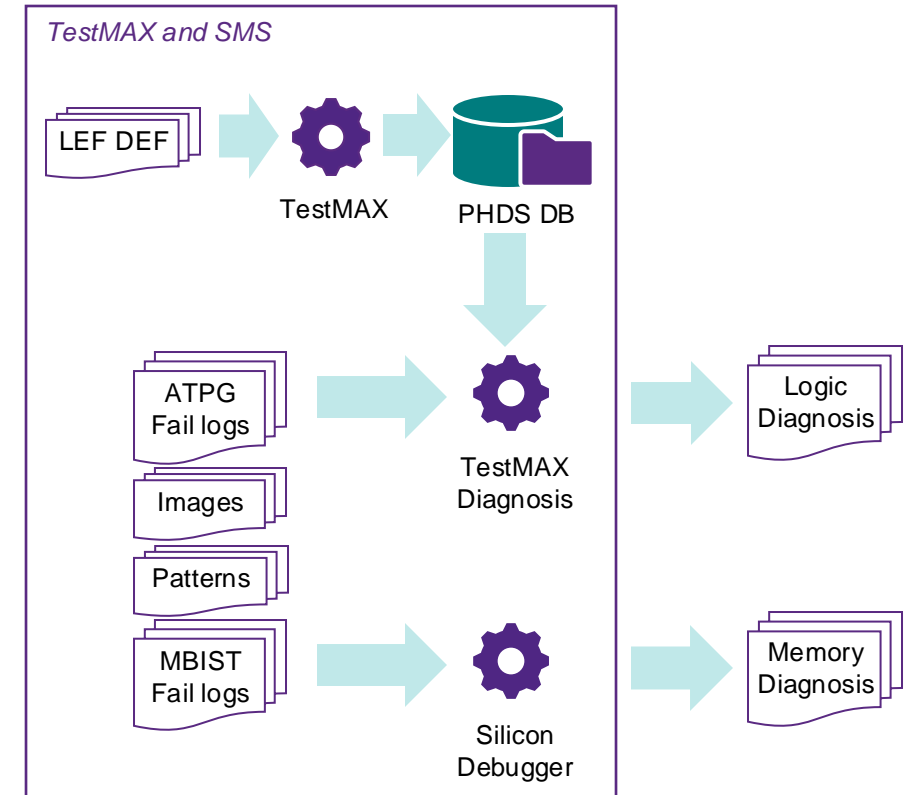
- Test results and diagnosis summaries are loaded to cloud (or local) data servers
- Design and diagnosis details are loaded to local data servers
- Machine Learning runs in cloud servers
- Additional test and fab data (if available) are loaded to cloud or local servers
- Web client for cloud data
- Local client for any data



Diagnosis flow

Test fail diagnosis

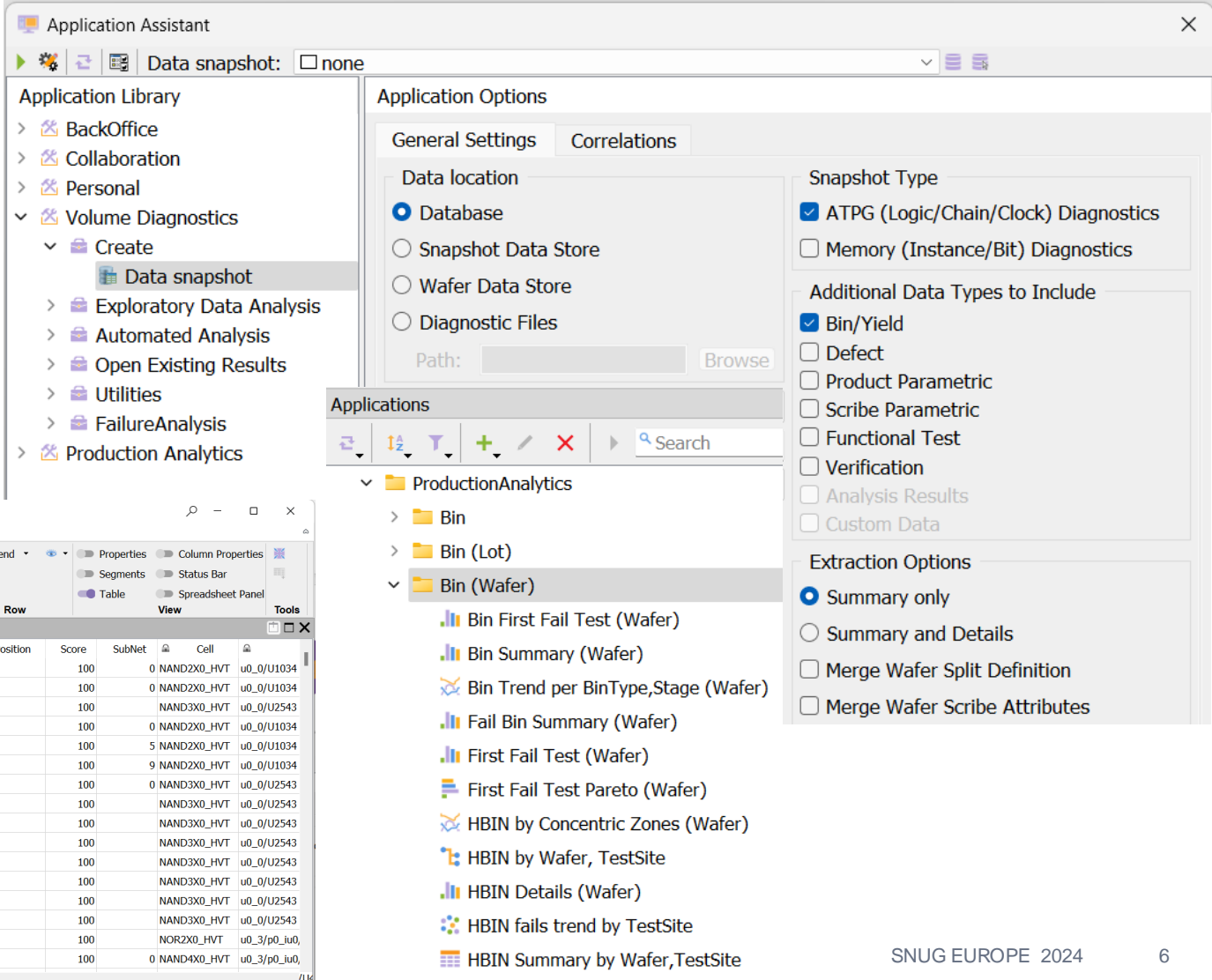
- LEF DEF is converted to PHDS Data Base
- ATPG fail logs are diagnosed with TestMAX Diagnosis (or 3rd party tools) to identify fail logic and chain candidates with probability scores
- MBIST fail logs are diagnosed with SMS Yield Accelerator Silicon Debugger (or 3rd party tools) to identify failed memories and bits
- Design images and test patterns are used during diagnosis process
- Logic and Memory diagnosis results are loaded to Silicon.da



Start the analysis with Local client

Using Local (Diagnostics) or Cloud (Test) data

- Open the local app (windows or linux)
- Login to the Local or Cloud database
- Use Application Assistant to create a local snapshot
- Use predefined Application Tasks and Flows for analytics
- Continue with custom analysis if needed



The screenshot shows the 'Application Assistant' window. On the left is the 'Application Library' with a tree view including 'BackOffice', 'Collaboration', 'Personal', 'Volume Diagnostics', 'Create', 'Data snapshot', 'Exploratory Data Analysis', 'Automated Analysis', 'Open Existing Results', 'Utilities', 'FailureAnalysis', and 'Production Analytics'. The 'Data snapshot' option is selected. The main area is titled 'Application Options' and has two tabs: 'General Settings' and 'Correlations'. Under 'General Settings', 'Data location' is set to 'Database'. 'Snapshot Type' has 'ATPG (Logic/Chain/Clock) Diagnostics' checked. Under 'Additional Data Types to Include', 'Bin/Yield' is checked. The 'Applications' section shows a tree view with 'ProductionAnalytics' expanded to show 'Bin', 'Bin (Lot)', and 'Bin (Wafer)'. Under 'Bin (Wafer)', several analysis tasks are listed, including 'Bin First Fail Test (Wafer)', 'Bin Summary (Wafer)', 'Bin Trend per BinType,Stage (Wafer)', 'Fail Bin Summary (Wafer)', 'First Fail Test (Wafer)', 'First Fail Test Pareto (Wafer)', 'HBIN by Concentric Zones (Wafer)', 'HBIN by Wafer, TestSite', 'HBIN Details (Wafer)', 'HBIN fails trend by TestSite', and 'HBIN Summary by Wafer, TestSite'.

Synopsys Silicon.da Client - [Default project]

CellFault	DiagClass	FaultModel	FaultNum	FaultType	InternalFault	NumCandidatesInDefect	NumDefects	NumFailures	ScanCellPosition	Score	SubNet	Cell
23	Y	CellAware	CTM	23 sa0	D83	36	1	12		100	0	NAND2X0_HVT u0_0/U1034
24	Y	CellAware	CTM	24 sa0	D88	36	1	12		100	0	NAND2X0_HVT u0_0/U1034
25	Y	CellAware	CTM	25 sa0	D101	36	1	12		100	0	NAND3X0_HVT u0_0/U2543
26		Driver	Stuck-at	26 sa1		36	1	12		100	0	NAND2X0_HVT u0_0/U1034
27		Receiver	Stuck-at	27 sa0		36	1	12		100	5	NAND2X0_HVT u0_0/U1034
28		Receiver	Stuck-at	28 sa0		36	1	12		100	9	NAND2X0_HVT u0_0/U1034
29		Receiver	Stuck-at	29 sa1		36	1	12		100	0	NAND3X0_HVT u0_0/U2543
30	Y	CellAware	CTM	30 sa0	D1	36	1	12		100		NAND3X0_HVT u0_0/U2543
31	Y	CellAware	CTM	31 sa0	D11	36	1	12		100		NAND3X0_HVT u0_0/U2543
32	Y	CellAware	CTM	32 sa0	D13	36	1	12		100		NAND3X0_HVT u0_0/U2543
33	Y	CellAware	CTM	33 sa0	D24	36	1	12		100		NAND3X0_HVT u0_0/U2543
34	Y	CellAware	CTM	34 sa0	D27	36	1	12		100		NAND3X0_HVT u0_0/U2543
35	Y	CellAware	CTM	35 sa0	D105	36	1	12		100		NAND3X0_HVT u0_0/U2543
36	Y	CellAware	CTM	36 sa0	D126	36	1	12		100		NAND3X0_HVT u0_0/U2543
37	Y	CellAware	CTM	1 sa0	D45	26	1	18		100		NOR2X0_HVT u0_3/p0_u0,
38		Driver	Stuck-at	2 sa0		26	1	18		100	0	NAND4X0_HVT u0_3/p0_u0,

Automated Volume Diagnostics



Using Logic / Chain diagnosis results

- Automated analysis identifies statistical outliers for multiple control factors
- Design statistics and critical area are used to normalize results and determine expected fail ratios
- Review fails by standard cell, cell internal, instance, net, via, design block, fault model, layers, etc.
- Strength of each outlier and the Yield impact is calculated
- Review trends, select outliers and drilldown to maps and failure analysis selection

Control Factor	Distribution	P-value	Gap %	Count	Strength	YL %
Category + Cell		0.0001	29.1	90	6.3	37.5
Category + CTMLayers		0.1297	-	-	-	-
Category + Layers		0.1297	-	-	-	-
Cell		0.0001	30.7	94	6.5	39.2
Cell + Component		0.0001	9.1	115	4.4	47.9
Cell + InternalFault		0.0001	25.0	79	6.9	32.9
Cell + InternalFaultElement		0.0001	26.5	150	7.3	62.5
Cell + Layers		0.0528	4.0	96	5.4	40.0
Cell + Placement		0.0001	11.2	88	5.3	36.7
Cell + Transistors		0.0001	26.3	147	6.7	61.3
CellGroup		0.9692	-	-	-	-
Component		0.0379	18.1	86	2.0	35.8

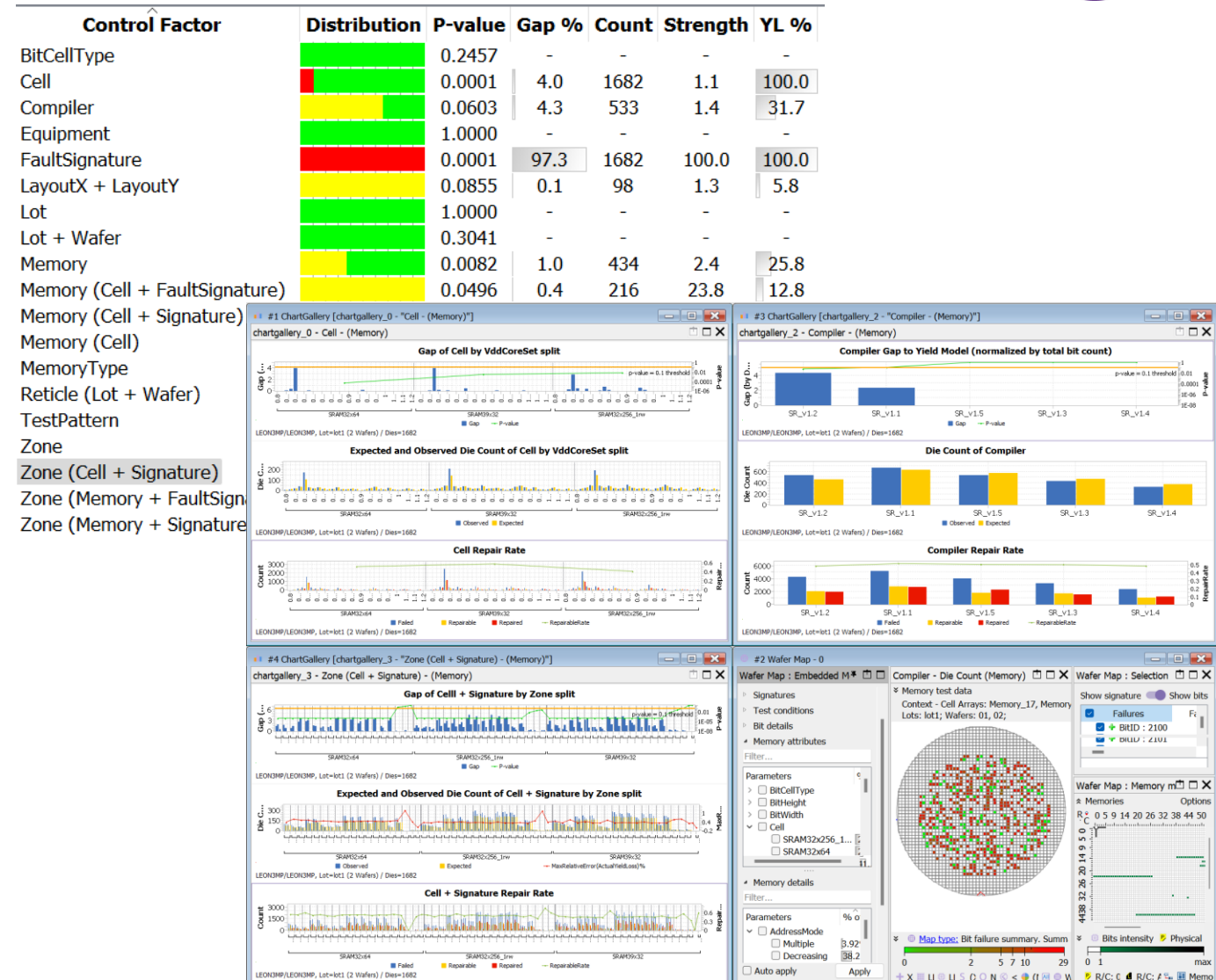


Automated Volume Diagnostics



Using Memory diagnosis results

- Automated analysis identifies statistical outliers for multiple control factors
- Memory design attributes are used to normalize results and determine expected fail ratios
- Review fails by memory design, bit cell type, compiler, topological and electrical fault signature, zone, etc.
- Strength of each outlier and the Yield impact is calculated
- Review trends, select outliers and drilldown to maps and failure analysis selection

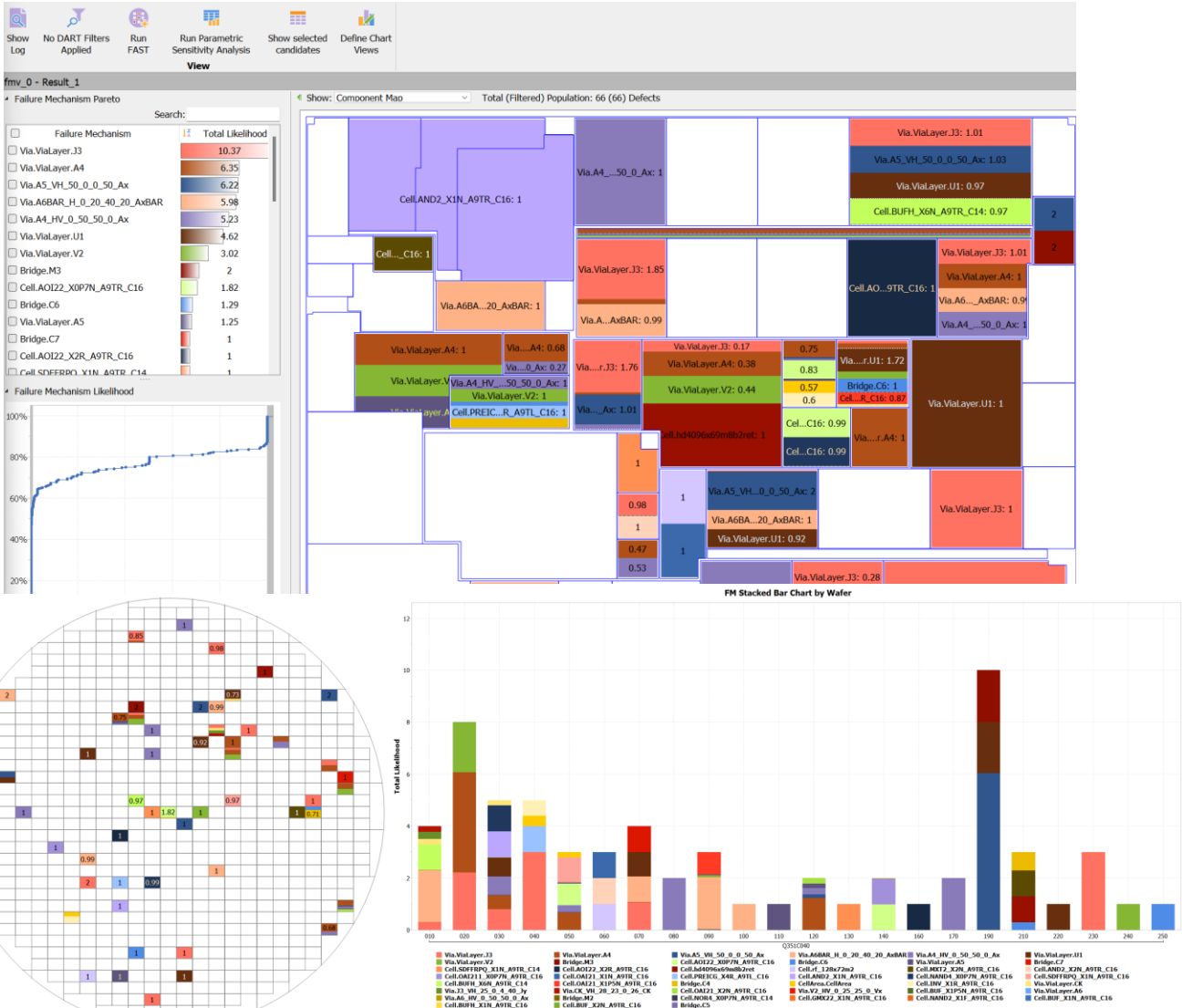


Failure Mode Analysis



Using Logic diagnosis results

- Bayesian inference identifies the most important failure modes
- Design statistics and critical area and cell test models are used to improve results
- Results are analyzed by component design block
- Likelihood of each failure is estimated and aggregated
- Review trends, select outliers and drilldown to maps and failure analysis selection



© Map type: FM Stacked bar chart. Stretch

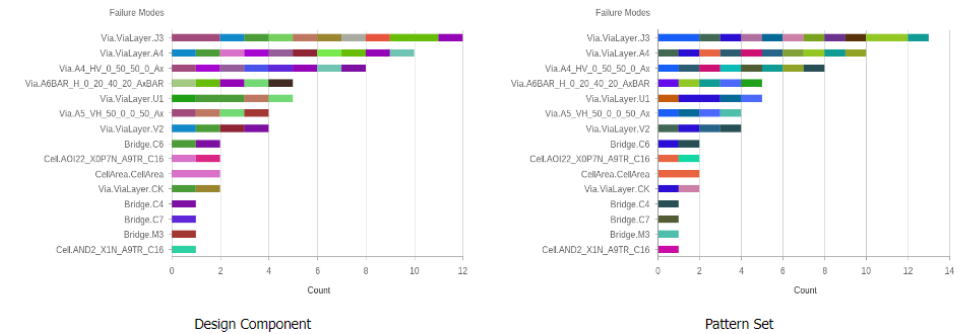
Diagnostics trends

Using all diagnosis results

- Diagnostics summaries are shown in the web client
- Paretos and trends by wafer / lot or time-scope
- Single and stacked wafer maps
- Results using failure modes, design components, memories, bit signatures, etc.

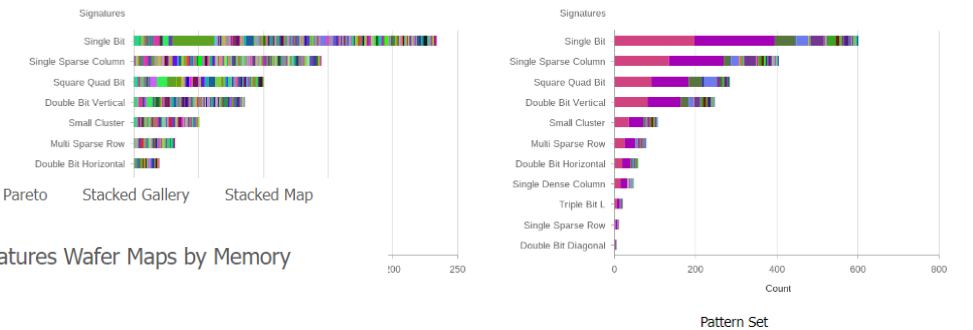
Logic Failure Modes Trend Gallery **Paretos** Stacked Gallery Stacked Map Distributions

S11P Logic Failure Modes Paretos



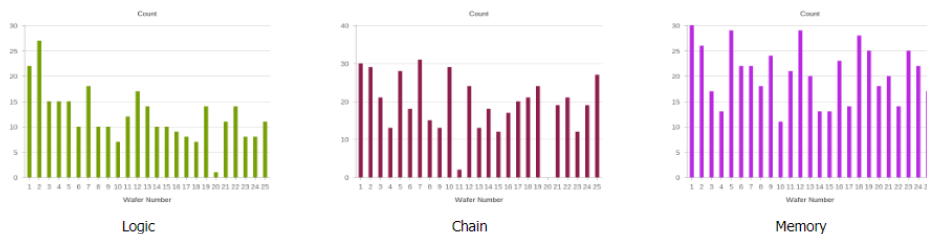
Memory Signatures Trend Gallery **Paretos** Stacked Gallery Stacked Map Distributions

S11P Memory Signatures Paretos

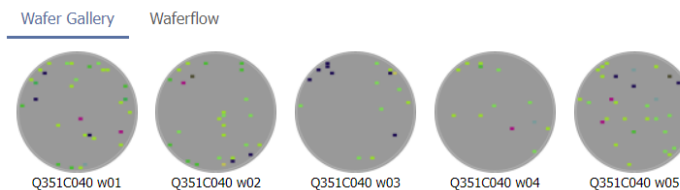


Diagnosis Results Failure Modes
Trends Pareto Stacked Maps Distributions

S11P Diagnosis Trends



S11P Memory Signatures Wafer Maps by Memory



Failure Analysis Selection

Using Logic / Chain diagnosis results

- Fail candidates identified as main Yield problems are reviewed and selected for failure analysis
- Filter by attributes, AVD and FMA results, overlay with GDS/OASIS, etc.
- Selected candidates are saved in a cart, and exported to Avalon or 3rd party format



The screenshot displays the Synopsys failure analysis software interface. It is divided into several panels:

- Candidate Table:** A table with columns: Include, rhumbnai, rfer Locati, ie Locatio, Lot, Wafer, CellFau. Row 1 is highlighted in blue.
- Selection (FML cannot show multiple result):** A tree view showing 'DefectNum 1' expanded to 'C-001' (Driver).
- Analysis View:** Two tables. The top table shows FMA results for Candidate C-001. The bottom table shows AVD results for Candidate C-001.
- Wafer map:** A circular grid representing the wafer layout.
- Physical Connectivity Viewer:** A detailed view of the circuit board layout with a red box highlighting a specific area.
- Layers:** A list of layers including Physical Details (Outline, Cells, M1, M2, M3, VIA1, VIA2), Nets and Cells (Outline, Cells, M1, M2, M3, VIA1, VIA2), and Pins (Outline, QN, VDD, VSS).

Failed Memory and Bit Signatures

Using Memory diagnosis results

- Interactive UI to review failed memories and bit signatures
- Filter fails by test conditions, memory attributes, and algorithm or bit-level details
- Wafer, reticle or die stacks
- View fail bits with physical or logical maps
- Selected bits and signatures are saved in a cart, and exported to Avalon or 3rd party format

The screenshot displays the Synopsys memory diagnosis tool interface. It features a top toolbar with various actions like 'Toggle Gallery View', 'Toggle Die Grid Editor', and 'Toggle Lens View'. The main workspace is divided into several panels:

- Left Panel:** A navigation tree with 'Context', 'Test patterns', 'Signatures', and 'Test conditions'. Below it are filter sections for 'Parameters' (Frequency, Temp, VddCore) and 'Bit details' (AddressMode, BackGround, Counter, etc.).
- Top Center Panel:** 'Memory - Die Count (Memory) : Viewer Gallery' showing two circular die maps for 'lot1:01' and 'lot1:02'.
- Top Right Panel:** 'Wafer Map : Selection' showing a table of failures.
- Bottom Center Panel:** 'Memory - Die Count (Memory) : Die map' showing a grid of memory cells with some highlighted in red and green.
- Bottom Right Panel:** 'Wafer Map : Memory map' showing a heatmap of memory intensity across a grid of rows and columns.

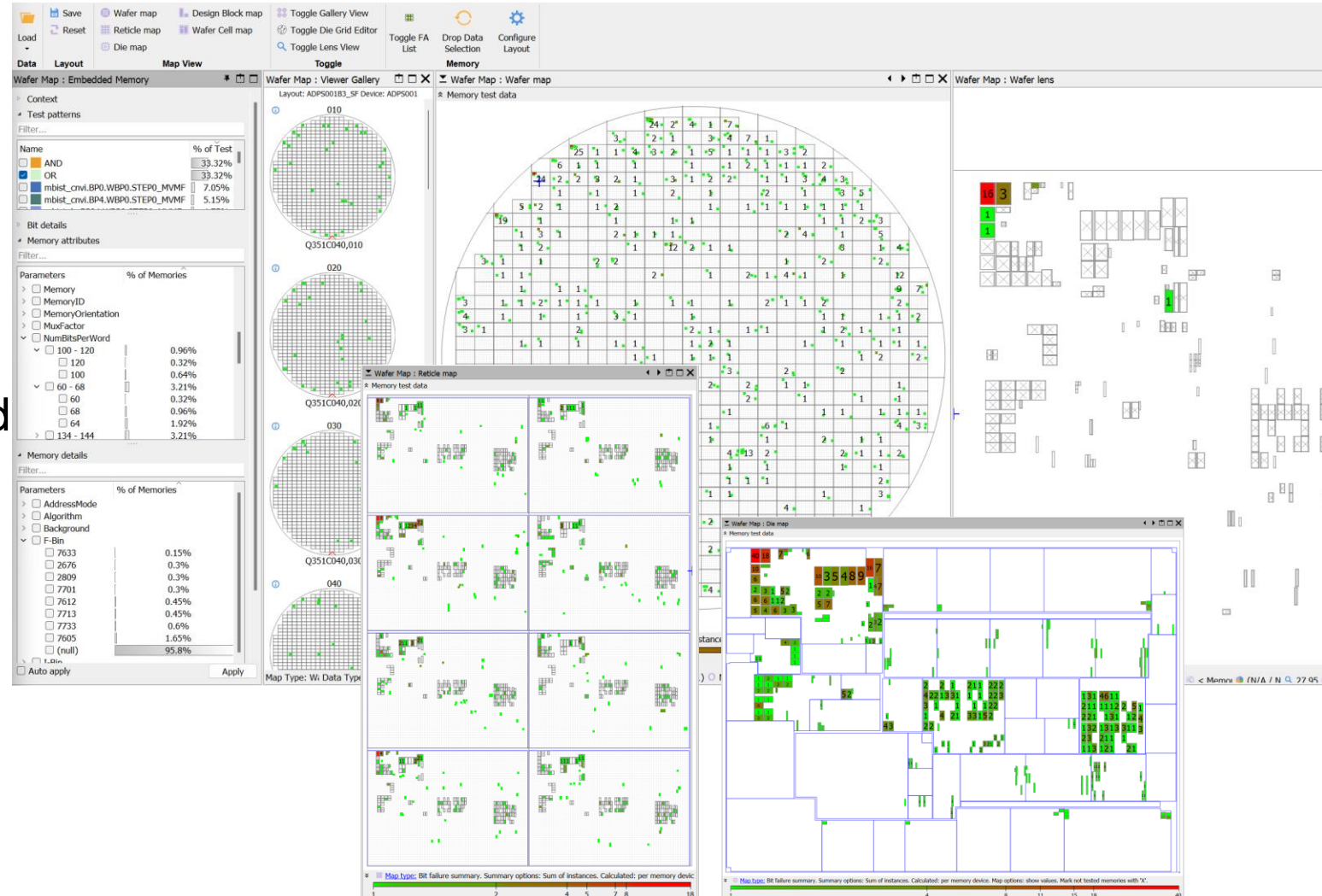
Failures	FailureID	Memory	Bank	Signature	StartPRow	Star
Double Bit Horizontal : 20	40	Memory_66	None	Double Bit Ho...	28	
Multi Sparse Column : 15	43	Memory_66	None	Multi Sparse ...	0	
Single Bit : 25	41	Memory_66	None	Single Bit	20	
Single Bit : 28	44	Memory_66	None	Single Bit	23	
Single Bit : 26	42	Memory_66	None	Single Bit	24	
Single Sparse Column : 61	36	Memory_66	None	Single Sparse ...	0	
Single Sparse Row : 96	37	Memory_66	None	Single Sparse ...	27	
Small Cluster : 14	38	Memory_66	None	Small Cluster	5	

Failures	FailureID	Signature	OtherSignature	VddCore	Left	Right
BITID : 209	12	Small Cluster		1.2	3897900	3900990
BITID : 249	13	Small Cluster		1.2	3900990	3903990
BITID : 289	14	Small Cluster		1.2	3903990	3906990
BITID : 329	15	Small Cluster		1.2	3906990	3909990

Failed Memories

Using MBIST production test results

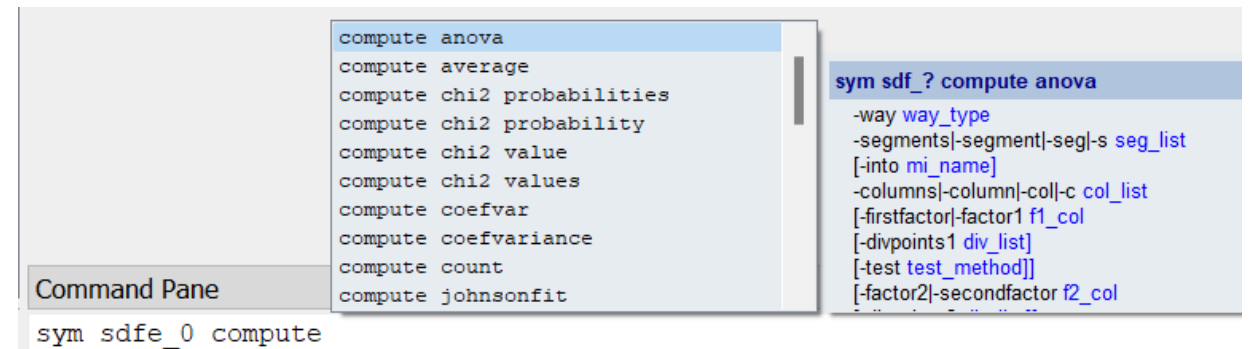
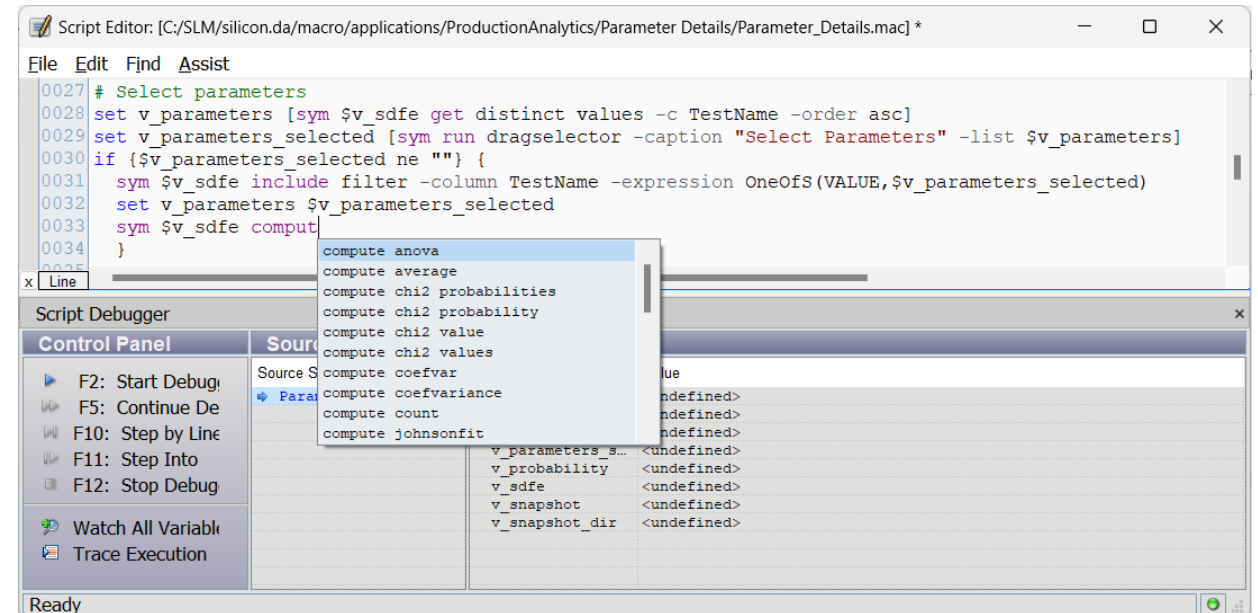
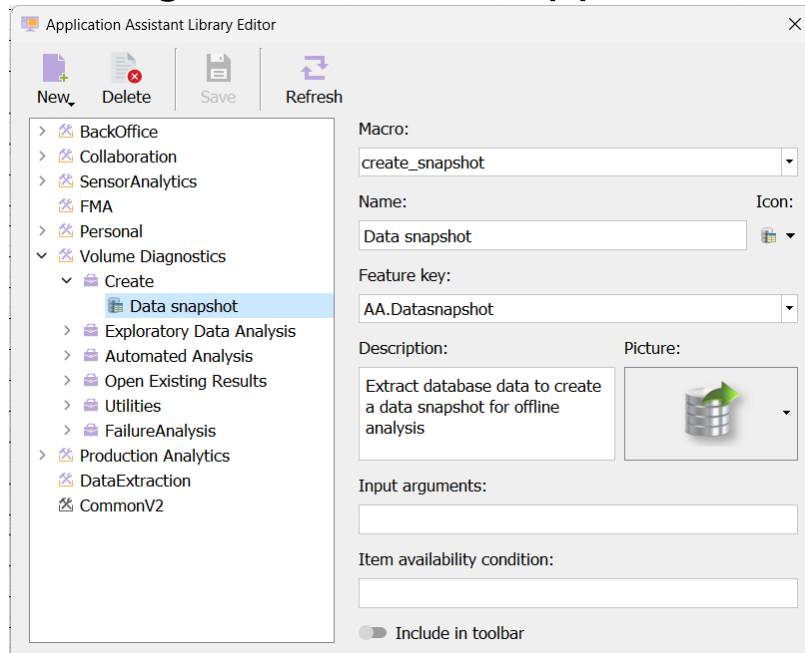
- Failed or repaired MBIST results are converted to memories using test pattern definitions
- Applies to high volume test, no additional data logging required
- Fails are filtered by test conditions, memory attributes, and algorithm details
- Wafer, reticle or die stacks
- Trends and paretos available by memory attributes
- Compatible with automated volume diagnostics analysis



Commands and macros

Automation for the local application

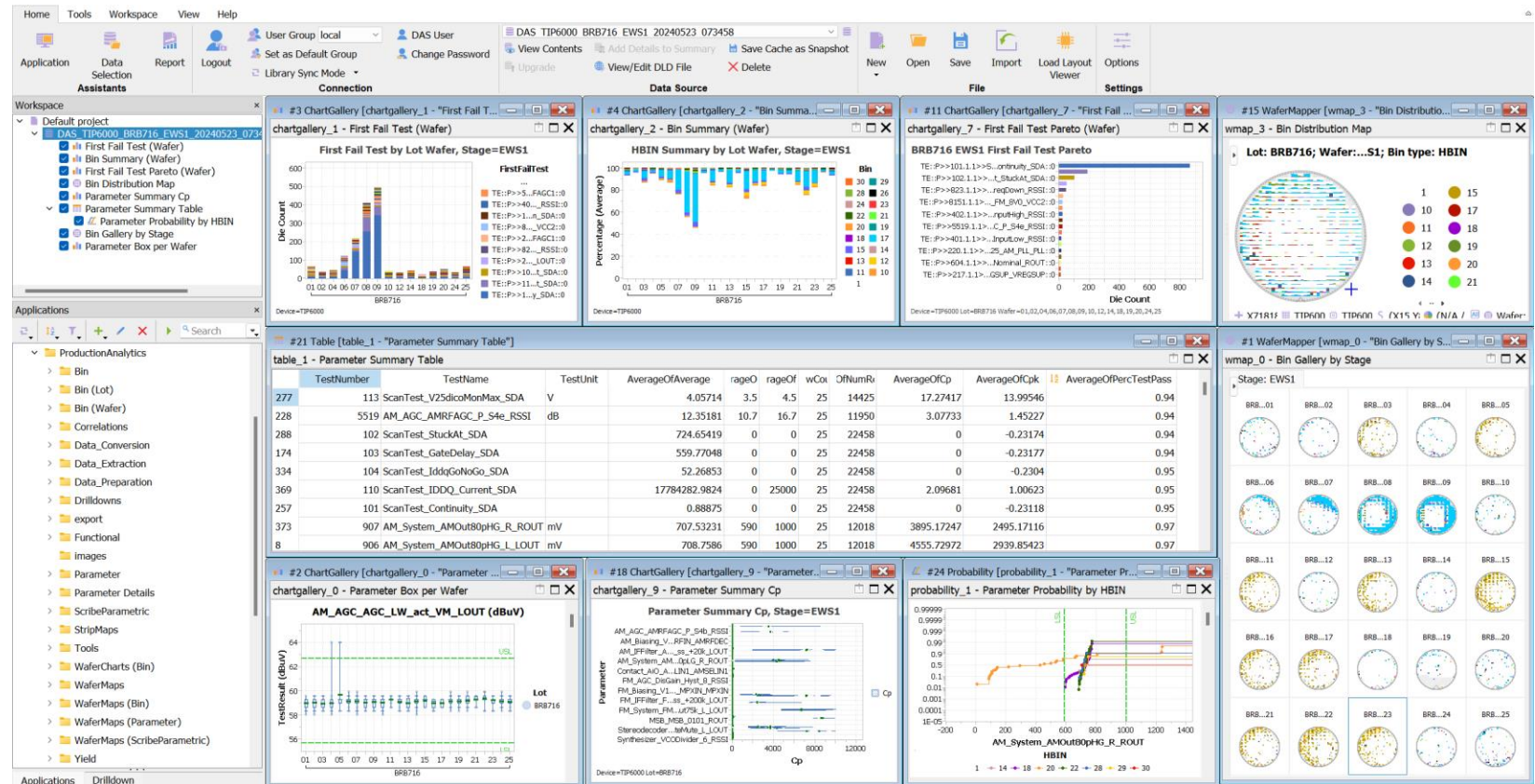
- Use GUI or commands for any analytics
- Use predefined or custom macros
- Build macros using TCL or Python or R
- Script Designer includes lookahead help
- Package macros into applications



Custom analysis with Local client

Using any test results

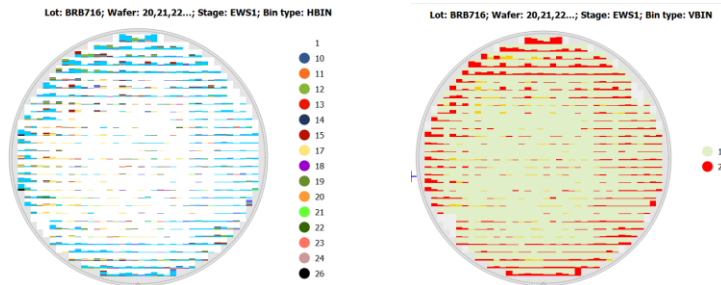
- Download data from cloud, and/or import local files
- Create a local data snapshot with any data types required
- Use existing tasks and flows, or create your own
- Use analysis tools: charts, spreadsheet functions, statistics, maps, correlations
- Use TCL / Python / R macros
- Save, reuse and share tasks, macros and data snapshots



Virtual test limits analysis

Using production test results

- Review results with existing limits
- Set new virtual limits as desired
- Recalculate virtual fails and virtual bins
- Compare existing and virtual results

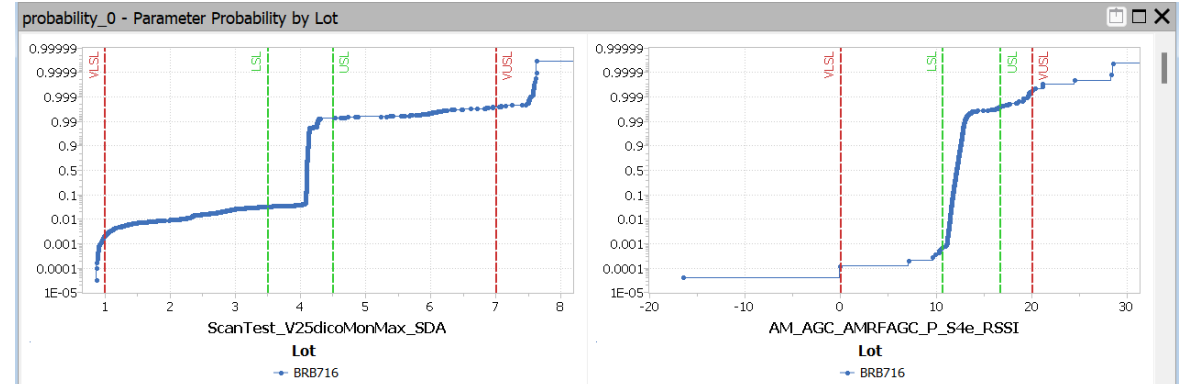


table_1 - Lot Wafer Yield ORIGINAL

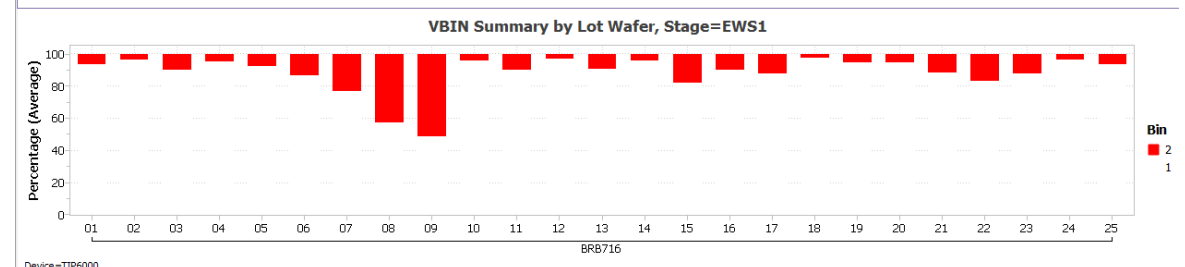
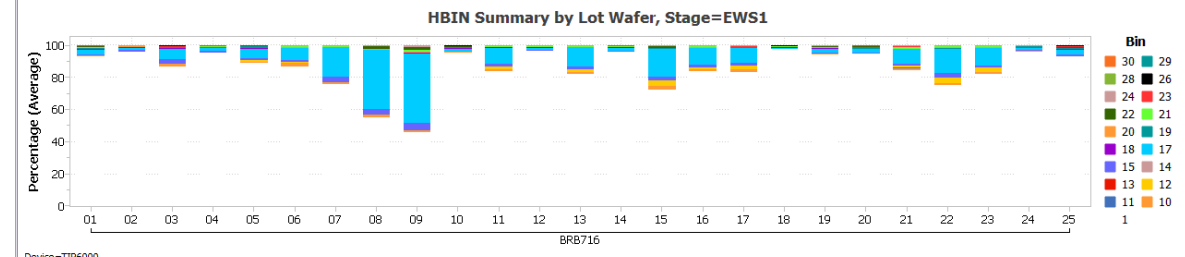
	Month	Week	Stage	Lot	Device	TestSequence	01	02	03	04	05	06	07	08
1	M2014/01	W2014/02	EWS1	BRB716	TIP6000	0	0.929	0.958		0.950		0.865	0.759	0.552
2	M2014/02	W2014/06	EWS1	BRB716	TIP6000	0			0.868		0.889			

table_0 - Lot Wafer Yield VIRTUAL

	Month	Week	Stage	Lot	Device	TestSequence	01	02	03	04	05	06	07	08
1	M2014/01	W2014/02	EWS1	BRB716	TIP6000	0	0.942	0.967		0.962		0.875	0.791	0.608
2	M2014/02	W2014/06	EWS1	BRB716	TIP6000	0			0.911		0.931			



	Parameter	Lot	Box	Rel. Cp/Cpk	Cp/Cpk	Cp	Cpk	K-Factor	LSL	USL	Total Points
8	AM_System_AMOut80pHG_R_ROUT	BRB716			1.56719	2.53726	1.61899	0.36192	590	1000	12018
9	AM_System_AMOut80pHG_L_LOUT	BRB716			1.55161	2.67173	1.72191	0.35551	590	1000	12018
10	AM_System_AMOut80pLG_L_LOUT	BRB716			1.34081	2.74262	2.04549	0.25418	240	413	12018
11	AM_System_AMOut80pLG_R_ROUT	BRB716			1.35306	2.68415	1.98376	0.26094	240	413	12018
12	EM_System_EMMoanLICND235_L_LOUT	BRB716			2.62005	2.06274	1.00245	0.72007	50	00	12102



Start the analysis with Web client



Using Cloud data

- Open the web browser and login
- Start the analysis from a Dashboard
- Browse recent test results by product / lot (filtered by user permissions)
- Find data by product / stage / lot / file / any of the chip IDs / etc.
- Review insights and drilldown to details

Products Lots Wafer Maps

Most Recently Updated Products

Product	Volume (lots)	Volume (wafers)	Most recently updated lot			
			Loading Time	Lot	Type	Insights (top 2)
M	439	10279	21/05/2024 - 14:03:54	Q	WS	
M	679	16522	21/05/2024 - 14:03:22	C	WS	2 wafers: clusters hbin 93 (31.0%) Lot vs. W21 2024 (up to 71.2%), Outlier yie
M	2488	-	21/05/2024 - 14:02:33	8	FT	
M	3352	82568	21/05/2024 - 14:02:31	C	WS	Zonal yield loss (3.7%)
M	833	5269	21/05/2024 - 14:01:49	C	WS	Zonal yield loss (1.9%)

Filters: Yield not is greater than 20

Product	Stage Type	Stage	Mode	Scope	Volume (lots)	Volume (wafers/sublots)	Total Quantity (dies/parts)	Last update time	D0	Yield
<input type="checkbox"/> FTR6002	FT	FT1	P	ALL	10	245	254638	15/11/2023 - 10:43:33	N/A	93.05
<input type="checkbox"/> P1216	WS	EWS2	P	ALL	177	4223	5135167	15/11/2023 - 10:38:11	0.21	89.66
<input type="checkbox"/> P1216	WS	PAT1	P	ALL	177	4238	5153407	15/11/2023 - 10:38:03	0.21	89.78
<input type="checkbox"/> P17486	WS	EWS1	P	ALL	18	155	2190577	15/11/2023 - 10:46:03	2.77	90.02
<input type="checkbox"/> PF0500	WS	EWS2	P	ALL	10	199	279794	15/11/2023 - 10:17:50	0.13	97.39
<input type="checkbox"/> PF0531	WS	EWS2	P	ALL	12	228	320568	15/11/2023 - 10:44:24	0.21	95.95
<input type="checkbox"/> PF0632	WS	EWS2	P	ALL	8	181	254486	15/11/2023 - 10:45:03	0.13	97.39
<input type="checkbox"/> PROD204693	WS	XXX	P	ALL	1	1	204693	14/11/2023 - 19:35:23	73.14	89.98
<input type="checkbox"/> TIP0065	WS	ROOM2	P	ALL	32	381	394178	21/11/2023 - 02:39:09	1.65	82.57

Parts

Search for 1K parts

Any tag begins with S146

- Any tag
- CLASSTAG
- FABLLOT
- MAC
- OTPVIRGIN
- QRTAG
- Serial
- ULTTAG
- VISUAL_ID

Product	Lot	Wafer/Sublot	X	Y	CLASSTAG	QRTAG
EAK	C135Y0S0	C135Y0S0 w11	26	-30	S146JICV_11182228_019088	S146JICV02504
EAK	S146JICW	S146JICW			S146JICW_11171724_001532	S146JICW03747
EAK	C135Y0S0	C135Y0S0 w24	32	-55		S146JICV10192

Product Families

28 nm FD SOI

Finders

- Products
- Lots
- Wafers/Sublots
- Test Events
- Parts
- Files
- Events
- Testers

Production Traffic Light Dashboards



Using production test results

- Browse Yield and D0 trends, review insights, click to continue the analysis

Traffic Light Dashboard

WS ASSY ASSY_W FT FT_W

Showing 1-20 of 173 Page 1 of 9 Show 20 Items

Product	Stage	Trend	Rolling Quarter										Current Quarter				Last Quarter					
			WAT Insight	Test Insight	Volume (wafers)	Weq +/-	Fin. \$	Fin. +/-	D0	Target D0	Yield	Target Yield	Volume (wafers)	D0	Target D0	Yield	Target Yield	Volume (wafers)	D0	Target D0	Yield	Target Yield
AI	S1	↗	3	0.11	13185	-157.25			0.15	0.13	87.44	88.50	7390	0.14	0.13	87.56	88.50	17732	0.15	0.13	87.10	88.50
AI	S1	-	0	0.30	20			N/A		89.52			18	N/A	89.69			4	N/A		89.65	
AI	OQA-FAB	-	0	0	24			0.00		99.78								24	0.00		99.78	
AI	OQA-FAB																					
AI	OQA-FAB	-	0	0	75			0.000		99.83			75	0.000		99.83						
AI	S1	-	0	0	100			0.041		85.70			75	0.041		85.70		25	0.041		85.72	
AI	OQA-FAB	-	0	0	178			0.003		99.71			150	0.002		99.73		136	0.004		99.58	

S1 Insights Last 90 Days

Yield Insights (up to 3.1%)

- ▶ Zonal (up to 3.1%)
- ▶ Outlier wafers (up to 0.4%)
- ▶ Clusters (up to 0.2%)
- ▶ Periodic effects
- ▶ WAT correlation

Test Hardware Insights (up to 0.1%)

- ▶ Probe card dependence (up to 0.1%)
- ▶ Tester dependence (< 0.1%)
- ▶ Test site dependence (< 0.1%)
- ▶ Partial wafer

Retest Insights

- ▶ Facility dependence
- ▶ Outlier wafers
- ▶ Outlier lots
- ▶ Probe card dependence
- ▶ Tester dependence

Integrity Insights (5 parts)

- ▶ High retest count on pass parts (5 parts)

Product Insights

- ▶ Wide test limits

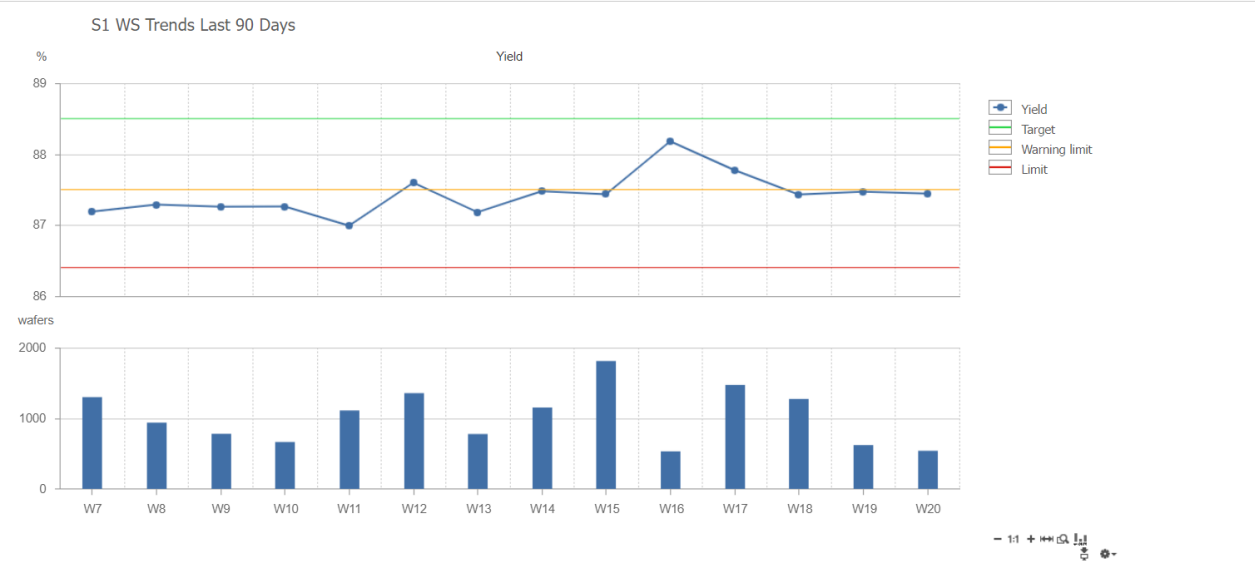
Pattern Analysis (< 0.1%)

- ▶ Yield patterns (< 0.1%)

Wafer Labels

- ▶ Manual classification

Last 90 Days vs. Q1 2024
Average yield improvement (+0.3%)



Product Families



Using production test results

- Create groups of similar products
- Compare trends and results within each group, by product or by lot
- Use Dashboards to compare summaries
- Click on any row in the table to go to the full analysis for the selected data

Product Families

- A Family
- L Family
- N

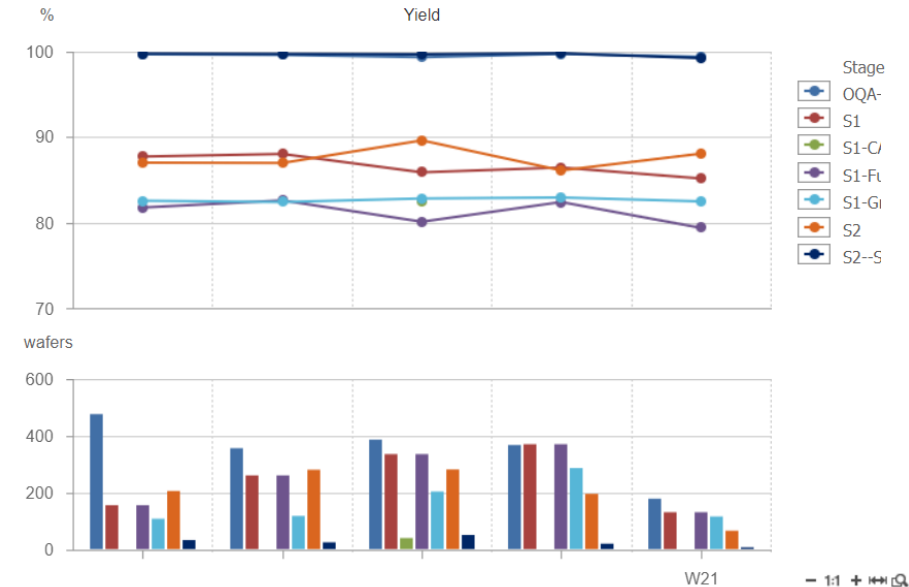
Products in Family

- A S81
- A SOC
- A H68
- A GPU
- A SOC
- A IOE
- A GPU

Overview Products (9) Lots (576) WS ASSY ASSY_W FT FT_W

Family Product Family WS Last 30 Days

Trends OQA-FAB S1 S1-CALC S1-Fully Featured S1-GroupBin S2 S2--Skip Untested



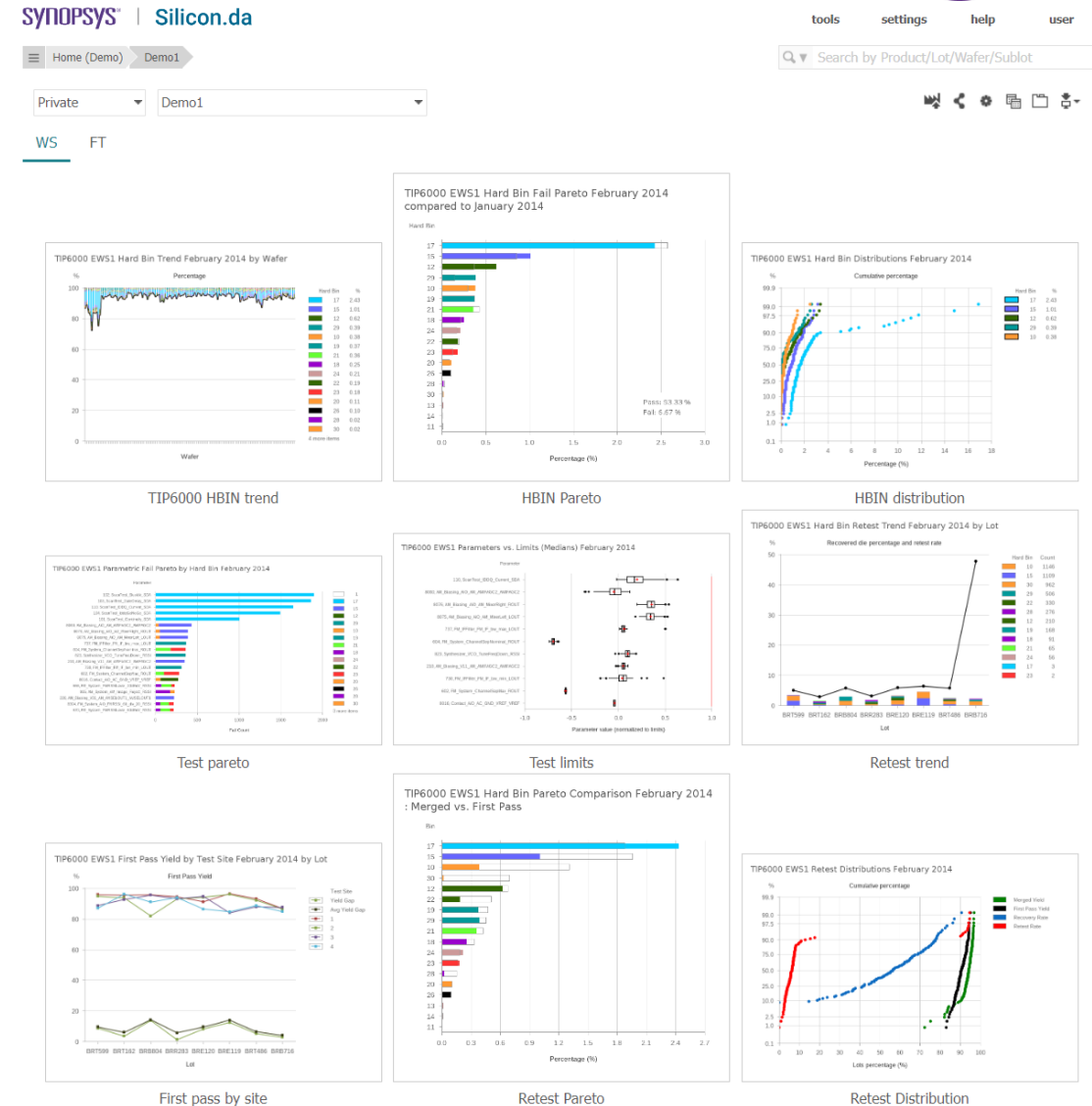
Family Product Family Reports Last 7 Days

Product Family	Wafer Acceptance			Wafer Sort				Assembly				Assembly - Wafer			Final Test			Final Test - Wafer						
	Stage	Volume (lots)	Volume (wafers)	Stage	Volume (lots)	Volume (wafers)	Yield (%)	D0	Stage	Volume (lots)	Volume (sublots)	Yield (%)	Stage	Volume (lots)	Volume (wafers)	Yield (%)	Stage	Volume (lots)	Volume (wafers)	Yield (%)				
Family	PCM	13	247	S2--S...	7	25	99.7	N/A	EOL	65	65	100.0	EOL	33	94	100.0	B6	24	24	62.3	B6	23	53	96.7
	PCM-C	11	225	S2	49	203	88.1	N/A									B6	13	13	68.1	B6	20	39	82.8
	PCM-FI	1	5	S1-Gr...	55	294	82.4	N/A									B6	1	1	100.0	B6	1	3	76.4
	PCM-FI	1	5	S1-F...	73	366	81.6	N/A									B6	47	47	66.4	B6	38	69	74.5
	PCM-O	13	247	S1	73	366	86.0	N/A									B6	7	7	15.8	B6	13	17	20.7

Personal Dashboards

Using production test results

- Create a personal dashboard for each project
- It is refreshed automatically every time
- Add any chart to the personal dashboard
- Click on any chart to go to the full analysis
- Share dashboards between colleagues



Dashboards

- Home
- My Dashboard
- Silicon.da Dashboard
- File Dashboard

My shared Dashboards

- My Product Set Dashboard

Shared Dashboards

- AI shboard (rami...)
- AI A PCM (jeff.ch...)
- AI M HVQK Analy...
- AI -P_Performanc...
- AI PCM (jeff.che...)
- AI B PCM (jeff.c...)
- AI B Performanc...

Add chart to a dashboard

Select dashboard

- Demo1
- My Dashboard

Select tab

- WS
- FT

Create new dashboard

Create new tab

Image caption

Image positioning

First Last

Automated Insights



Using production test results

- Data is analyzed for typical Yield and test problems
- Additional metrics are checked and reported when significant
- Insights are calculated at lot and wafer level, and aggregated to day, week, month, quarter, year, all scope
- Mouse hover shows mini charts for each insight, and click opens the report
- Start from the insights to identify the most important problems for each product on any time scope

TIP6000 EWS1 Insights Week 06 2014

Yield Insights (up to 2.2%)

- ▶ Outlier lots (up to 2.2%)
- ▶ Zonal (up to 1.7%)
- ▶ Periodic effects
- ▶ Clusters (up to 0.5%)
- ▶ Outlier wafers (up to 0.3%)
- ▶ Reticle/repetitive effect (< 0.1%)

Test Hardware Insights (up to 0.3%)

- ▶ Test site dependence (up to 0.3%)
- ▶ Loadboard dependence (up to 0.2%)
- ▶ Probe card dependence (up to 0.2%)
- ▶ Tester dependence (up to 0.2%)
- ▶ Gap in testing

Retest Insights

- ▶ Outlier wafers
- ▶ Outlier lots
- ▶ Loadboard dependence
- ▶ Probe card dependence
- ▶ Program name dependence
- more...

Process Insights (< 0.1%)

- ▼ Distribution tails (< 0.1%)
 - 3 wafers: tails on 730, FM_IFFilter_FM_IF_bw_min_LOUT (< 0.1%)

Integrity Insights (2 parts)

- ▶ High retest count on pass parts (2 parts)

Product Insights (up to 0.8%)

- ▶ Test limit sensitivity (up to 0.8%)
- ▶ Wide test limits
- ▶ Program name dependence (< 0.1%)
- ▶ Program version dependence (< 0.1%)

Test

- ▶ Test

W06 2014 vs. W05 2014

- Average yield drop (-2.6%)
- Baseline degradation for hbin 15 (+0.6%)
- Baseline yield stable

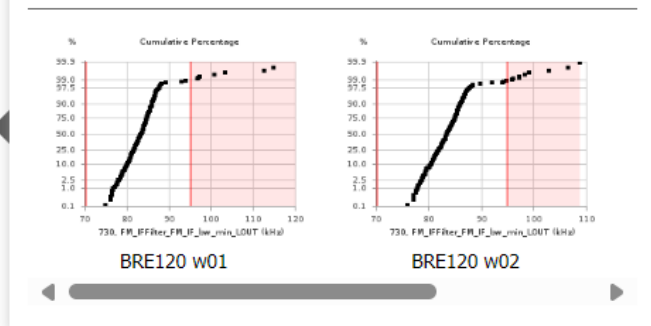
Degradation (up to 0.8%)

- ▶ Test (wafers)
- ▶ Outlier wafers (0.3%)
- ▶ Test limit sensitivity (wafers) (0.8%)
- ▶ Clusters (wafers) (up to 0.2%)
- ▶ Wide test limits (wafers)
- more...

Improvement (up to 0.4%)

- ▶ Probe card dependence (up to 0.4%)
- ▶ Loadboard dependence (up to 0.3%)
- ▶ Tester dependence (up to 0.3%)
- ▶ Zonal (up to 0.2%)

3 wafers: tails on 730, FM_IFFilter_FM_IF_bw_min_LOUT (< 0.1%)



Yield and Bin analysis

Using production test results

- Review hard, soft and custom bin trends and maps and insights
- Navigate between wafer, lot, day, week, month, quarter, year, all scope
- Separate reports available for retests and merged results

Week 03 2014
January 13, 2014 - January 19, 2014

Day Week Month Quarter Year All

Rolling Latest Lot

Product WS Reports
Retest/Time
Test Results
Yield/Bin

Yield/Bin
Overview
Hard Bin
Soft Bin

Stages
EWS1
EWS2
PAT

Stage Types
WS

Products
TIP0251
TIP6000

Hard Bins
Yield (All Bins)
1 (P)
17 (F)
15 (F)
12 (F)
10 (F)
21 (F)

Split by
None
Loadboard (2)
Probe Card (3)
Program Name (2)
Program Version (2)
Test Site (4)
Tester (2)
Facility (1)
Process (1)
ROM Code (1)
Tester Type (1)
Manual Split ...
Manual Grouping ...

Correlation
Correlate with ...
R² Analysis ...

Workspace Management
My Workspace
Integration Flows
Analysis Flows
Recipes
Scripts

HL Workspace
Models

TIP6000

Volume 31 lots, 485 wafers

Yield 92.9%

DO 0.25 cm-2

Insights
Lot BR8716
Low yield outlier (8.9% impact)
High fail bin outlier: 17 (7.5% impact)

Lot BR8120
High fail bin outlier: 29 (0.4% impact)

Yield 91.48
Zonal (1.7% impact)

HBin 17
Zonal (0.7% impact)

HBin 12
Zonal (0.4% impact)

HBin 15
Zonal (0.2% impact)

Product Yield Trend

Average Yield
92.9%
- 1.5%

TIP6000 EWS1 Hard Bin Fail Pareto Week 06 2014 compared to Week 05 2014

TIP6000 EWS1 Hard Bin Trend Week 06 2014 by Wafer

TIP6000 EWS1 Hard Bin Stacked Map Week 06 2014

TIP6000 EWS1 Hard Bin Maps Week 06 2014

Wafer Gallery Waferflow Stacked Maps

TIP6000 EWS1 Hard Bin Distributions Week 06 2014

TIP6000 EWS1 Insights Week 06 2014

Yield Insights (up to 2.2%)

- Outlier lots (up to 2.2%)
- Zonal (up to 1.7%)
- Periodic effects
- Clusters (up to 0.5%)
- Outlier wafers (up to 0.3%)
- Residue/repetitive effect (< 0.1%)

Test Hardware Insights (up to 0.3%)

- Test site dependence (up to 0.3%)
- Loadboard dependence (up to 0.2%)
- Probe card dependence (up to 0.2%)
- Tester dependence (up to 0.2%)
- Gap in testing

Retest Insights

- Outlier wafers
- Loadboard dependence
- Probe card dependence
- Program name dependence

Process Insights (< 0.1%)

- Distribution tails (< 0.1%)

Integrity Insights (2 parts)

- High retest count on pass parts (2 parts)

Product Insights (up to 0.8%)

- Test limit sensitivity (up to 0.8%)
- Wide test limits
- Program name dependence (< 0.1%)
- Program version dependence (< 0.1%)

Test

- Test

W06 2014 vs. W05 2014

- Average yield drop (-2.6%)
- Baseline degradation for hbin 15 (-0.6%)
- Baseline yield stable

Degradation (up to 0.8%)

- Test (wafers)
- Outlier wafers (0.3%)
- Test limit sensitivity (wafers) (0.6%)
- Clusters (wafers) (up to 0.2%)
- Wide test limits (wafers)

Improvement (up to 0.4%)

- Probe card dependence (up to 0.4%)
- Loadboard dependence (up to 0.3%)
- Tester dependence (up to 0.3%)
- Zonal (up to 0.2%)

Wafer Gallery **Waferflow** **Hard Bin Table**

16/01/2014 03:32 16/01/2014 03:32 (ONLINE_R... Merged Map

Parametric Result analysis



Using production test results

- Review parametric results, statistics, trends, maps and insights
- Review bins associated to each failed test
- Navigate between tests, wafer, lot, day, week, month, quarter, year, all scope
- Sort tables and galleries by typical statistics and Cp Cpk

BRE120
February 03, 2024 15:21:08 (Week 6)

BRE120 (TIP6000)
Volume: 1 lot, 25 wafers
Yield: 94.8%

Lot Yield Trend
Average Lot Yield: 94.8%
+1.5%

BRE120 EWS1 Parametric Fail Pareto by Hard Bin

Parameter	Fail count
102_ScanTest_StackM_SDA	322
103_ScanTest_GasDelay_SDA	314
104_ScanTest_N89OutputOp_SDA	243
110_ScanTest_IDDQ_Current_SDA	202
101_ScanTest_Construty_SDA	150
823_Synthesizer_VCO_TuneFreq_V	103
737_FM_Filter_FM_IF_bar_mhz	99
604_FM_System_ChannelSepNominal_R	88
602_FM_System_ChannelSepMeas_R	88
600_Synthesizer_AIO_Synth_VCO_Bur	88
601_Synthesizer_AIO_Synth_VCO_Bur	88
670_FM_System_FMRSSLevel_000B_V	88
830_Synthesizer_VCO_Gear_0000_RSSI	88

BRE120 EWS1 Parametric Cp/Cpk Pareto

Parameter	Cpk
102_ScanTest_StackM_SDA	1.08
103_ScanTest_GasDelay_SDA	0.96
104_ScanTest_N89OutputOp_SDA	0.95
110_ScanTest_IDDQ_Current_SDA	0.91
101_ScanTest_Construty_SDA	0.93
823_Synthesizer_VCO_TuneFreq_V	0.96
737_FM_Filter_FM_IF_bar_mhz	0.99
604_FM_System_ChannelSepNominal_R	0.97
602_FM_System_ChannelSepMeas_R	0.97
600_Synthesizer_AIO_Synth_VCO_Bur	0.97
601_Synthesizer_AIO_Synth_VCO_Bur	0.97
670_FM_System_FMRSSLevel_000B_V	0.97
830_Synthesizer_VCO_Gear_0000_RSSI	0.97

BRE120 EWS1 Parameters vs. Limits

BRE120 EWS1 Parameter Charts

BRE120 EWS1 Parametric Statistics Table

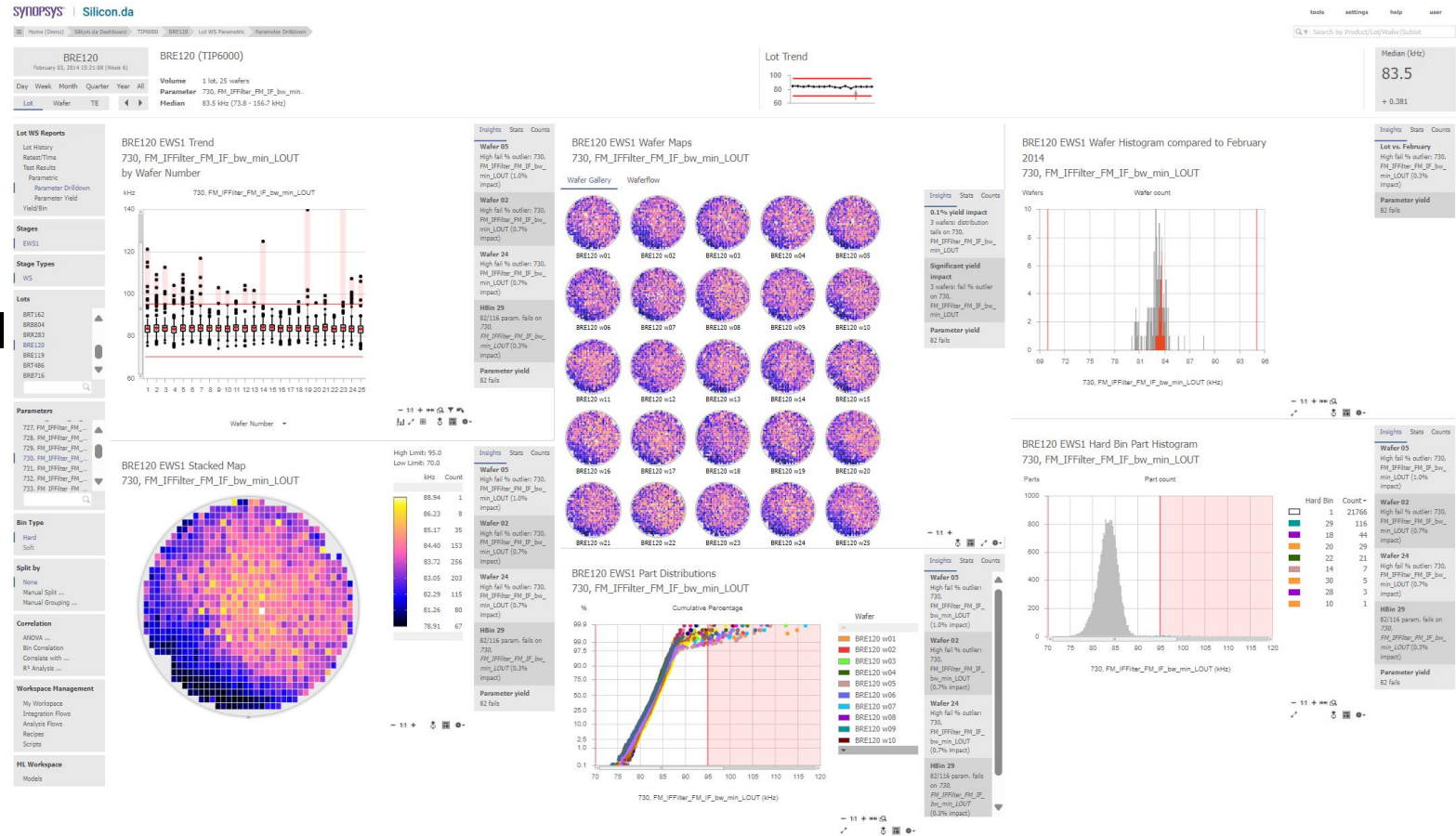
Test number	Test name	Unit	Low limit	High limit	PSD	Mean	Stdev	Cp	Cpk	Result count	Fail count	Yield (%)
102	ScanTest_StackM_SDA		0	0	0	262.7	5108.0			22888	322	98.6
103	ScanTest_GasDelay_SDA		0	0	0	264.8	5847.7			22888	314	98.6
104	ScanTest_N89OutputOp_SDA		0	0	0	48.838	1019.2			22888	243	98.9
110	ScanTest_IDDQ_Current_SDA		0	25000.0	4541.2	95112.0	1.18e+7	3.79	1.401	22888	202	99.1
101	ScanTest_Construty_SDA		0	0	0	0.229	13.747			22888	150	99.3
823	Synthesizer_VCO_TuneFreq_V	V	-0.8	0.6	-0.691	-0.699	0.212	1.758	1.596	22262	103	95.5
737	FM_Filter_FM_IF_bar_mhz	kHz	100.0	130.0	115.7	115.9	4.216	6.237	5.949	21962	102	99.5
604	FM_System_ChannelSepNominal_R		45	90	59.030	70.415	1508.4	1.022	0.885	21870	53	90.0
602	FM_System_ChannelSepMeas_R		20	90	41.017	41.506	2.045	14.158	0.075	21411	51	90.0
600	Synthesizer_AIO_Synth_VCO_Bur		4.55	5.10	4.63	4.82	2.51	3.834	3.812	22262	50	90.0
601	Synthesizer_AIO_Synth_VCO_Bur		1.40	1.54	1.499	1.482	0.70	3.205	3.180	22262	50	90.0
670	FM_System_FMRSSLevel_000B_V		3.2	3.8	3.415	3.417	0.075	2.180	1.905	22141	48	90.0
830	Synthesizer_VCO_Gear_0000_RSSI		0.8	1	0.96	0.99	0.0403	40.229	3.885	22262	48	90.0
830	Synthesizer_VCO_Gear_0000_RSSI		0.8	1	0.943	0.944	0.0401	35.917	20.363	22262	48	90.0
830	Synthesizer_VCO_Gear_0000_RSSI		0.8	1	0.944	0.945	0.0031	40.816	23.068	22262	48	90.0
830	Synthesizer_VCO_Gear_0000_RSSI		0.8	1	0.937	0.938	0.0404	35.162	22.054	22262	48	90.0
830	Synthesizer_VCO_Gear_0000_RSSI		0.8	1	0.968	0.969	0.0521	32.156	3.959	22262	47	90.0
830	Synthesizer_VCO_Gear_0000_RSSI		0.8	1	0.948	0.949	0.0521	29.053	8.838	22262	47	90.0
830	Synthesizer_VCO_Gear_0000_RSSI		0.8	1	0.961	0.961	0.0208	38.061	14.567	22262	47	90.0

Parametric Result Drilldown analysis



Using selected production test results

- Review trends, maps, statistics for any selected parameter
- Compare results of current lot / wafer to larger population
- Adjust test limits to evaluate yield impact



Parametric Yield Drilldown analysis



Using selected production test fail results

- Review trends, maps, statistics of failures for any selected parameter
- Failures are based on test limits and/or test fail flags
- Limits can be adjusted to estimate impact of changes

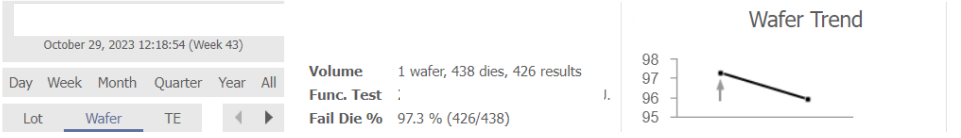
The screenshot displays the Synopsys SiliconDNA interface for a parametric yield drilldown analysis. The main dashboard shows the following components:

- Navigation Sidebar:** Includes sections for Lot WS Reports, Stages, Stage Types, Lots, Parameters, Split by, Correlation, and Workspace Management.
- Dashboard Summary:**
 - Lot:** BRE120 (TIP6000)
 - Volume:** 1 lot, 25 wafers
 - Parameter:** 730, FM_IFFilter_FM_IF_bw_min_LOUT
 - Fail Die %:** 0.4 % (82/22950)
- Lot Trend:** A line graph showing the trend of failures over time.
- BRE120 EWS1 Fail Trend:** A bar chart showing the fail count by wafer number.
- BRE120 EWS1 Wafer Maps:** A grid of 25 wafer maps (w01 to w25) showing the distribution of failures on each wafer.
- BRE120 EWS1 Stacked Fail Map:** A large circular map showing the cumulative distribution of failures across all wafers.
- BRE120 EWS1 Wafer Distributions:** A scatter plot showing the cumulative percentage of failures versus the fail die percentage.
- Statistics Panel:**
 - 0.4% yield impact:** 3 wafers distribution, 3 wafers fail % outlier on 730.
 - Significant yield impact:** 3 wafers fail % outlier on 730.
 - Parameter yield:** 82 fails.
- Right Panel:** A table showing the distribution of failures across different stages and parameters.

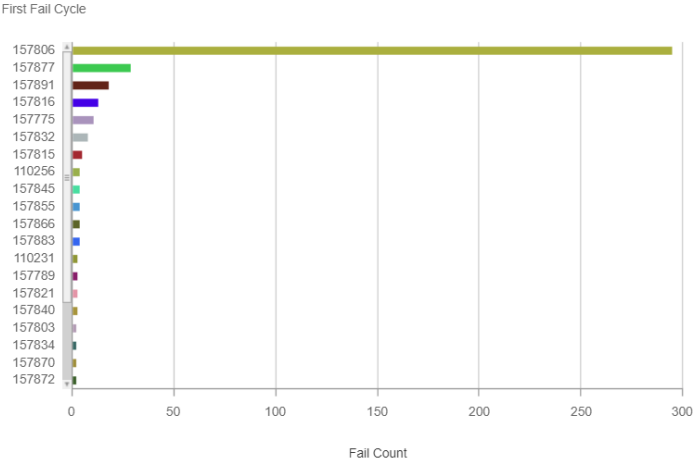
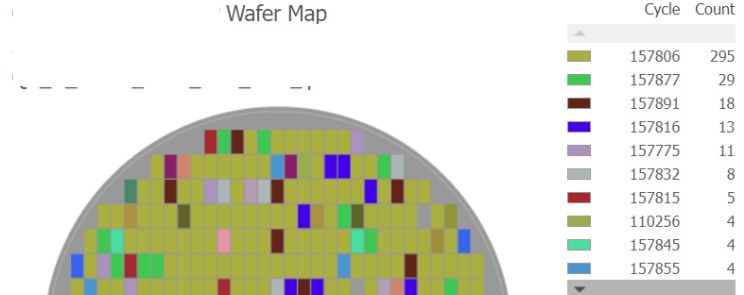
Functional Test analysis

Using production test results

- Review pareto, trends, and maps of failures of tests
- Review pareto and maps of failed cycles and patterns of tests
- Correlate functional fails and parametric test results
- Typically used for ATPG scan, MBIST, Vmin search, etc.



- Retest/Time
 - Test Results
 - Functional
 - Functional Drilldown
 - Wafer/Sublot History
 - Yield/Bin
- Stages
- S11P
- Stage Types
- WS



Die Traceability in packages

Using production test results

- Chip ID (ECID, 2DID, etc.) are combined with assembly data to link all test results
- Package test results are viewed as reconstructed wafer maps
- Failed and pass die history is available across all tests
- Multi Chip Modules are recreated as wafers for all included dies

BZ9857 w19 (TIP0065)
 May 17, 2010 14:02:26 (Week 20)
 Volume: 1 wafer, 2236 dies
 Yield: 95.6%
 Test Events: 2 (17/05/2010 04:02 - 14:02)

Wafer Yield Trend
 Wafer Yield: 95.6% (+1.6%)

Hard Bin Map
 BZ9857 w19 ROOM1 Hard Bin Map

Hard Bin	Count	%
1	1	95.62
6	6	4.16
13	13	0.09
20	20	0.09
18	18	0.04

Insights

- HBin 6**: 93/93 param. fails on 77048, pos 25 Uth > 4V (4.1% impact) Clusters (1.9% impact)
- HBin 1**: FT_W pass from WS POSTINK fail (2 parts)

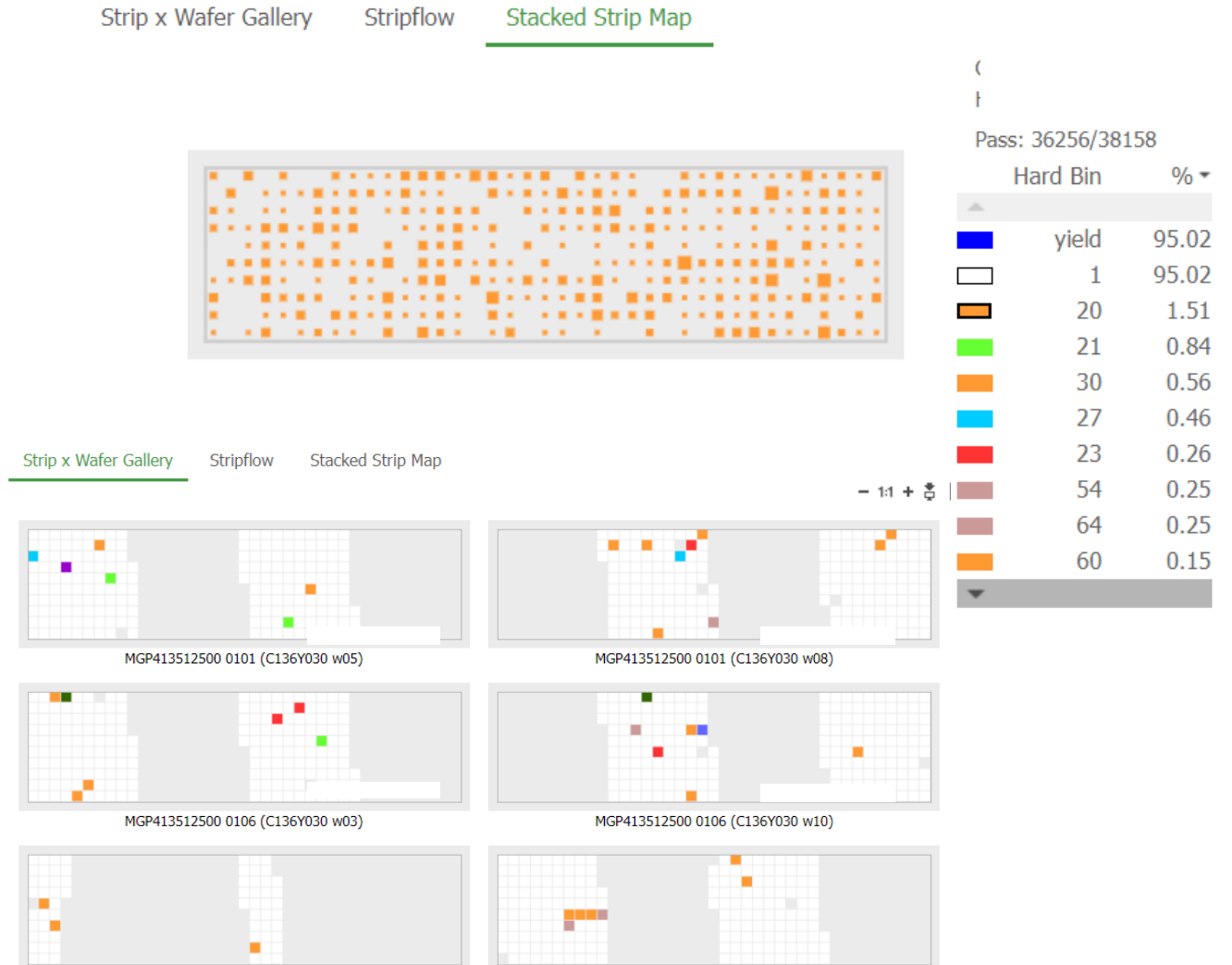
Die History

<input type="checkbox"/>	Lot	Wafer/Sublot	X	Y	Orig. S	TE Date/Time	Type	Stage	Hard Bin	Test Site
<input type="checkbox"/>	BZ9857	BZ9857 w19	28	19	28, 31	30/03/2010 - 18:18:17	WS	HOT1	2	0
<input type="checkbox"/>	BZ9857	BZ9857 w19	28	19	28, 31	14/04/2010 - 17:45:02	WS	POSTINK	1	0
<input type="checkbox"/>	BZ9857	524463104				17/05/2010 - 04:02:18	FT	ROOM1	6	0
<input type="checkbox"/>	BZ9857	BZ9857 w19	28	19	28, 31	17/05/2010 - 04:02:18	FT_W	ROOM1	6	0

Strip analysis from assembly

Using production test results

- Chip ID (ECID, 2DID, etc.) are combined with strip assembly data
- Package test results are viewed as reconstructed strip maps
- Stacked strip maps can show dominant fail bin problems
- Individual strip maps can show assembly problems



Gage Reliability and Reproduceability

Using production test results

- Compare test measurements and identify test instability or quality problems
- Applies for wafer-to-wafer and packaged parts

Gage R&R Statistics - ANOVA (Crossed)
80001, vddshort_400mV_TM:VDDIO_33@VDDIO_33[1]

Two-Way ANOVA Table With Interaction

Source	DF	SS	MS	F	P
Part	982.0	8.89e-4	9.05e-7	1.01	0.428
Split	0.0	0.0	0.0	0.0	1.00
Part*Split	0.0	0.0	0.0	0.0	1.00
Repeatability	1966.0	0.00176	8.97e-7		
Total	2948.0	0.00265			

Two-Way ANOVA Table Without Interaction

Gage R&R With Interaction

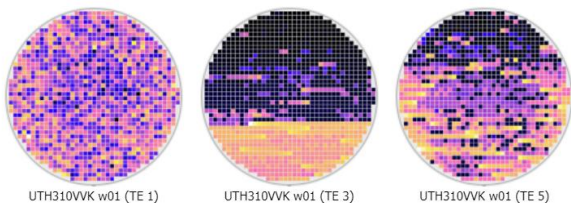
Source	VarComp	%VarComp	StdDev	Study Var (6*SD)	SV/Tolerance (%)	%Study Var
Total Gage R&R	8.97e-7	74.83	9.47e-4	0.00568	63.15	86.50
Repeatability	8.97e-7	74.83	9.47e-4	0.00568	63.15	86.50
Reproducibility	0.0	0.00	0.0	0.0	0.00	0.00
Split	0.0	0.00	0.0	0.0	0.00	0.00
Part*Split	0.0	0.00	0.0	0.0	0.00	0.00
Part-To-Part	3.02e-7	25.17	5.49e-4	0.00330	36.62	50.17
Total Variation	1.20e-6	100.00	0.00110	0.00657	73.00	100.00

Number of distinct categories: 0

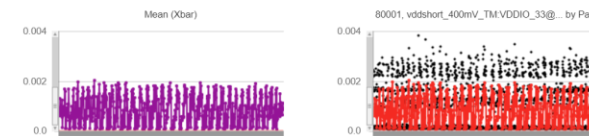
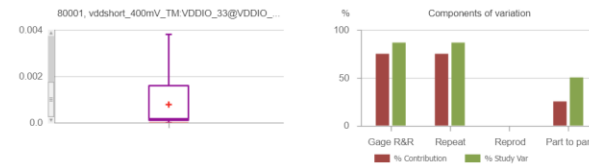
Gage R&R Test Events - ANOVA (Crossed)

80001, vddshort_400mV_TM:VDDIO_33@VDDIO_33[1]

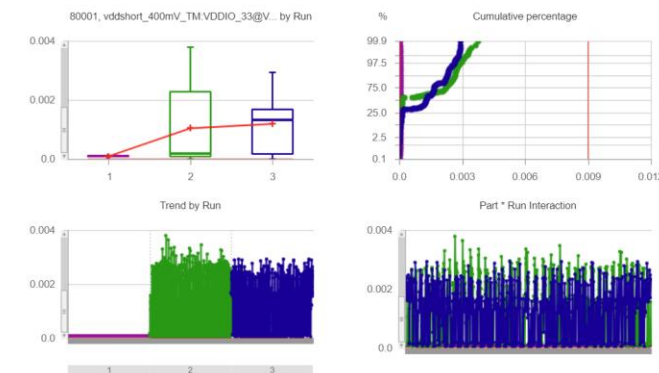
Gallery Waferflow



Gage R&R Charts - ANOVA (Crossed)
80001, vddshort_400mV_TM:VDDIO_33@VDDIO_33[1]



Per Run Charts - ANOVA (Crossed)
80001, vddshort_400mV_TM:VDDIO_33@VDDIO_33[1]

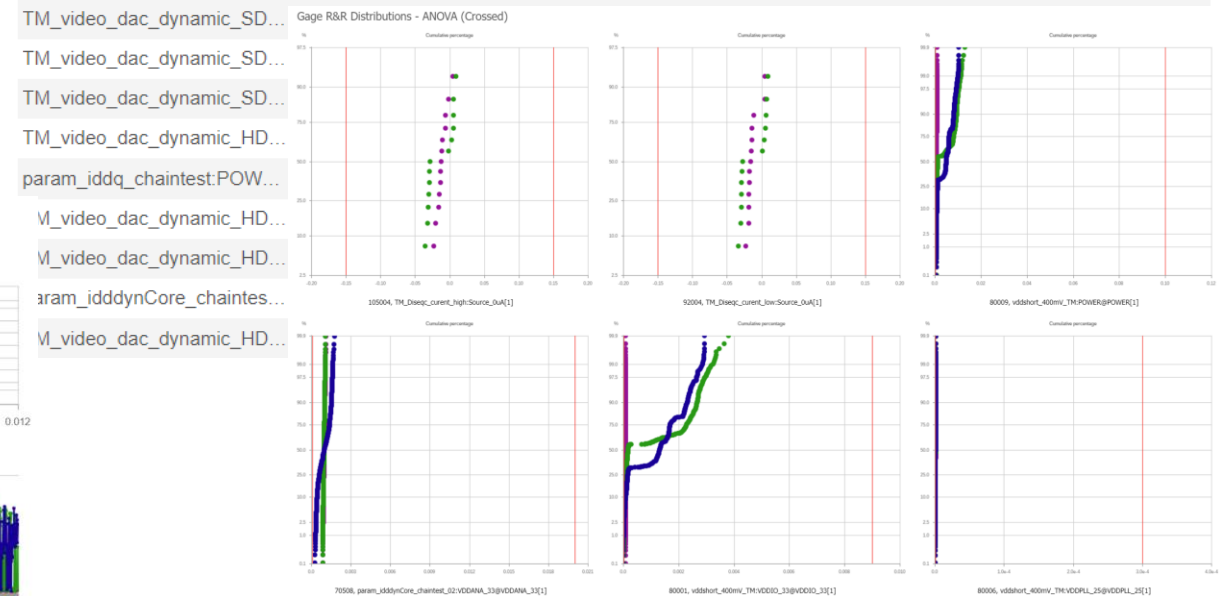


Gage R&R Analysis - ANOVA (Crossed)

Filters: Repeat. (EV) not is missing

Showing 1-50 of 153 Page 1 of 4 Show 50 Items

Parametric test	Unit	%Study var		Dist. cat.	%Tot (6 * stdev / tolerance)				Matrix		
		Gage R&R	Part-Part		Reprod. (AV)	Repeat. (EV)	Total R&R	Part-Part	Parts	Splits	Runs
vddshort_400mV_TM:VDDL...		99.89	4.59	0	0	1.30	1.30	0.06	970	1	3
vddshort_400mV_TM:VDDA...		98.18	18.97	0	0	1.12	1.12	0.22	967	1	3
param_iddq_chaintest:VDDI...		97.96	20.07	0	0	11.73	11.73	2.40	960	1	3
TM_video_dac_dynamic_HD...		95.04	31.11	0	0	4.67	4.67	1.53	14	1	2
TM_audio_dac_dyn_sin_LH...		94.99	31.25	0	0	39.07	39.07	12.85	14	1	2



Scripts and recipes

Automation for the cloud system

- Use predefined system scripts, or build your own scripts using JS
- Scripts are version controlled
- Use recipes to schedule or trigger the scripts based on any type of event
- Run from a list of applicable tools



Description | Script | Scope Validator | Ports / Parameters | Audit History | **Trigger type : Wafer/Sublot**

Script Name : Initialize ink map

Version Comment:

Description: Copies bin data to a new map. A source stage can be specified if a different stage from the current is to be used.

Labels: INKING

Config Controls: ON_WAFER, INKING, MAP_EDIT

Max Test Events:

Editors: Users, besides the owner, allowed to edit this script

Access Level: ROLE_ADMIN, ROLE_INTEGRATION, ROLE_PRODUCTION, **ROLE_USER**

Hide content

Output to user data set

Scope

Facility *i* *

Product Family *i* *

Product *i* *

ROM Code *i* *

Stage *i* *

Stage Type *i* *

Mode Code *i* *

Test Equipment Name *i* *

Program Version *i* *

Package *i* *

Sanity Status *i* PASSED, QUARANTINE, WARNING, REJECTED

Reason *i* *

Scripts | Libraries | Macros | Run History

Filters: Name not contains ink

Showing 1-11 of 11

<input type="checkbox"/>	Name	Description	Owner	Created by	Sharing	Ver.	Last update	State	Actions
<input type="checkbox"/>	Initialize ink map	Copies bin data to a new map. A source stage can be specified if ...	system	system	SYSTEM	1.0	12/10/2022 - 00:00:00	Production	
<input type="checkbox"/>	Ink between two selected dies	Ink all pass dies between two selected dies (e.g. scratch).	system	system	SYSTEM	2.0	08/04/2019 - 00:00:00	Production	
<input type="checkbox"/>	Ink bins	Inks dies of specified hard and/or soft bins.	system	system	SYSTEM	1.0	12/08/2022 - 00:00:00	Production	
<input type="checkbox"/>	Ink by manual limit	Ink dies using manually defined limit on parameters values.	system	system	SYSTEM	2.0	08/04/2019 - 00:00:00	Production	
<input type="checkbox"/>	Ink clusters	Ink around clusters of fail dies. In case of die selection, only ink a...	system	system	SYSTEM	3.0	08/04/2019 - 00:00:00	Production	
<input type="checkbox"/>	Ink enclosed area	Ink all pass dies in area enclosed by convex hull of selected dies.	system	system	SYSTEM	2.0	08/04/2019 - 00:00:00	Production	

Development | Qualification | **Production** | Phase Out | Obsolete

All Tools

Tools available on current scope

CORRELATION ANALYSIS

Correlate with ... | Gage R&R Analysis | R² Analysis ...

LOCAL CLIENT ANALYSIS

Export Parquet files | Export data (SDF)

SYNOPSYS TOOLS

Check Event Integrity | Create Custom Insight | DPAT

Delete Custom Insights | Export Assembly Maps | Export Lot Summary File

Failing Test on Pass Bin | Initialize ink map | Ink bins

Ink by manual limit | Ink clusters | Ink holes

Ink insights | Ink wafer edge | Ink wafer edge

Judgement Check Data Integrit... | Judgement Check SBL Multi-Wa... | Judgement Action

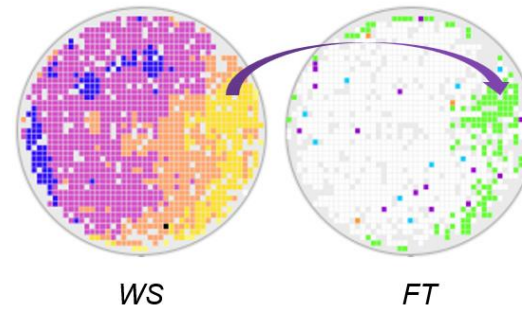
Parametric Prediction | Parametric Prediction Training | Part level Parameters Statistics

Machine Learning

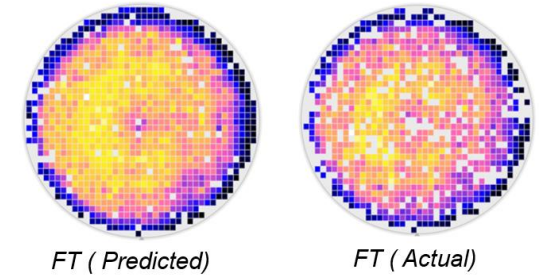
Using production test results

- Train and use predefined ML apps
 - Predict Parametric result at any future test stage from wafer sort results
 - Predict Yield and Bin at any future test stage from wafer sort results
 - Predict Vmin at SLT from monitor results
- Develop custom ML apps

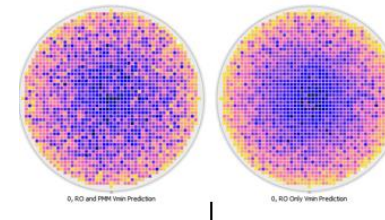
Bin Prediction



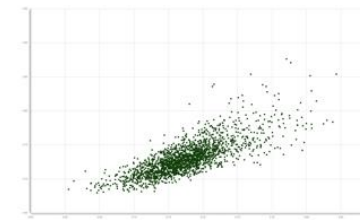
Parametric Prediction



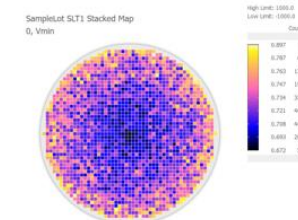
Vmin Predictions



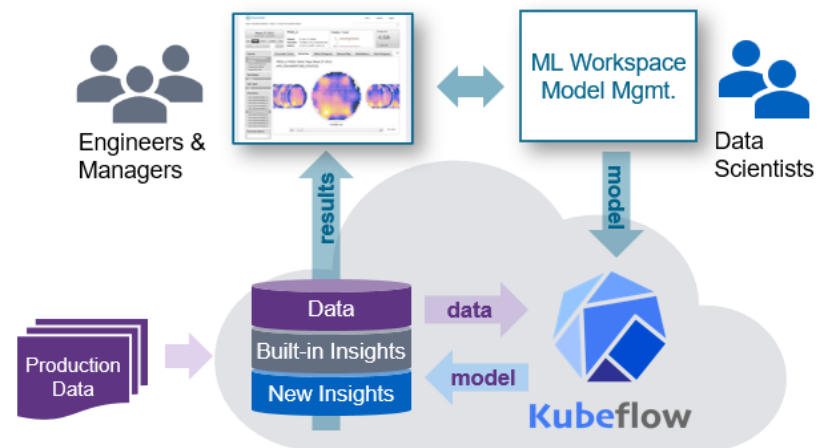
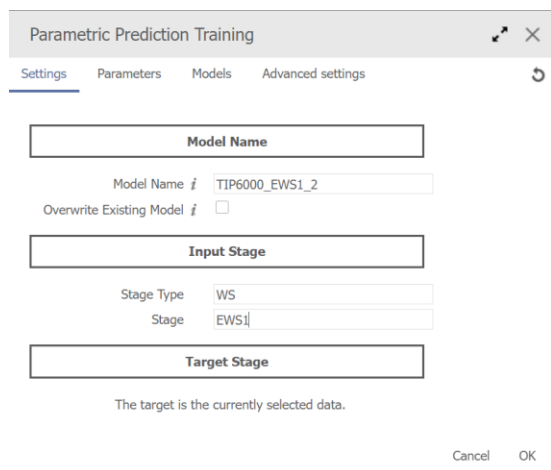
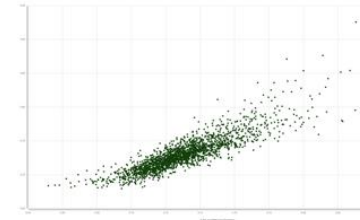
RO Prediction Vs Vmin



Measured Vmin at SLT



RO+PMM Prediction Vs Vmin

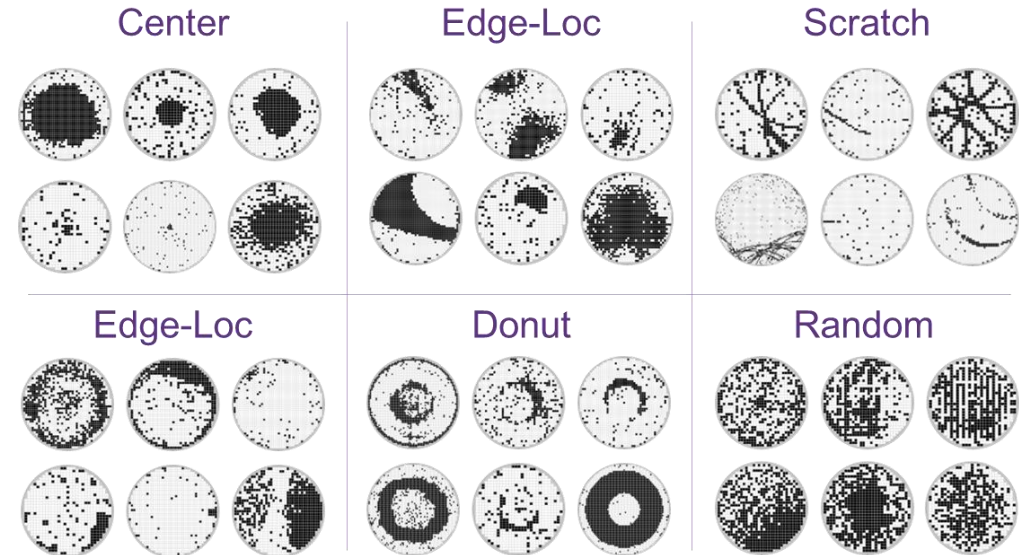


Spatial Patterns and Inking

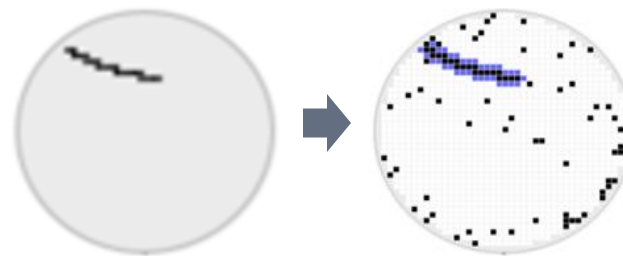
Using production bin results

- Spatial wafer pattern classification for typical patterns
- Scratch detection for multiple types of scratches
- Cluster and Good Die Bad Neighbor (GDBN) detection
- Automated inking for the die around problem areas to improve reliability

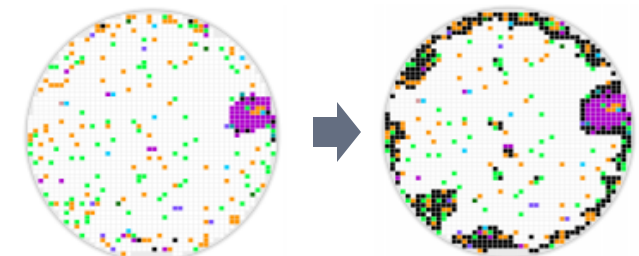
Pattern Classification



Scratch Detection and Inking



Clusters and Inking

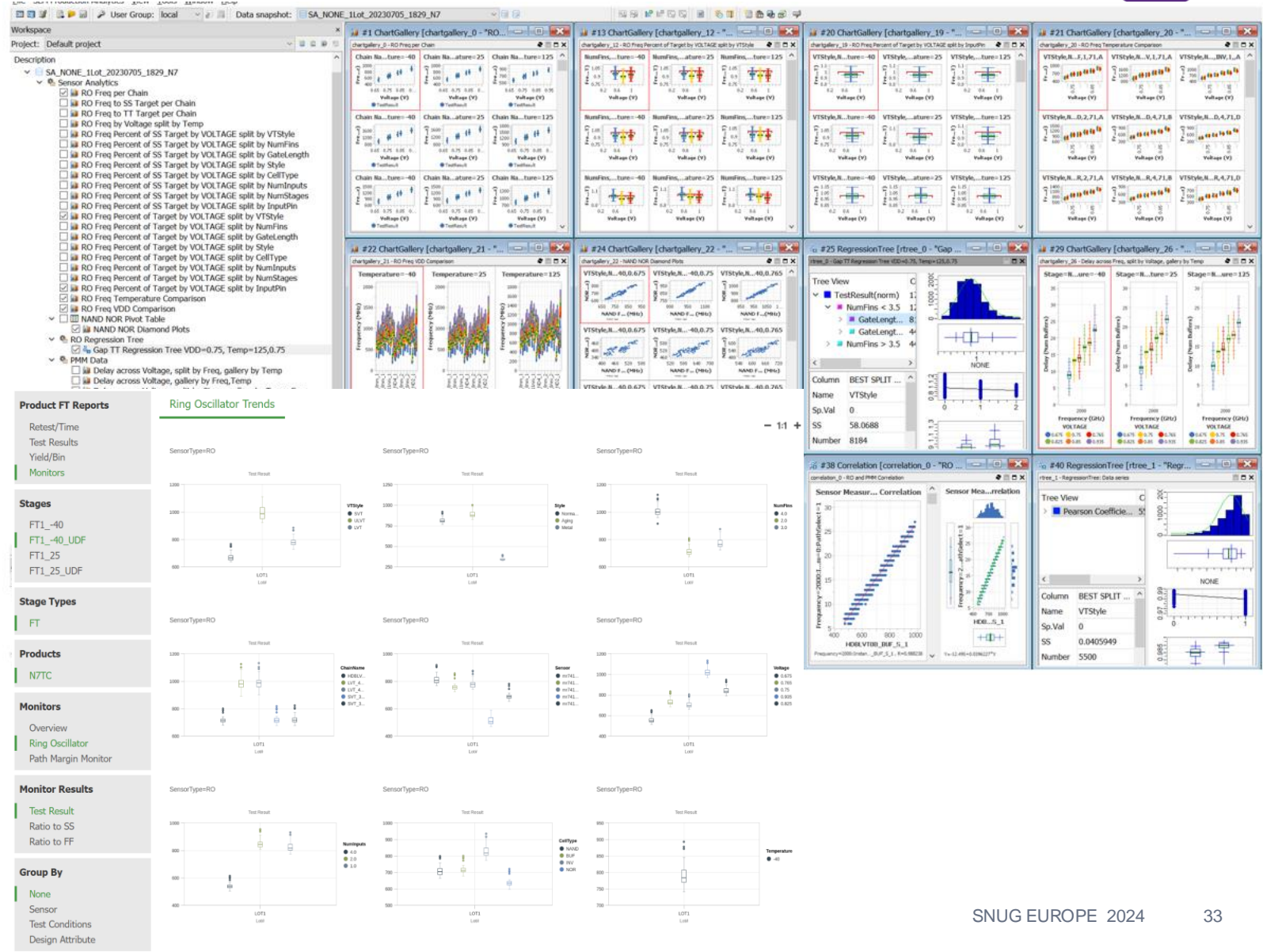


Monitor Analytics



Using embedded monitors

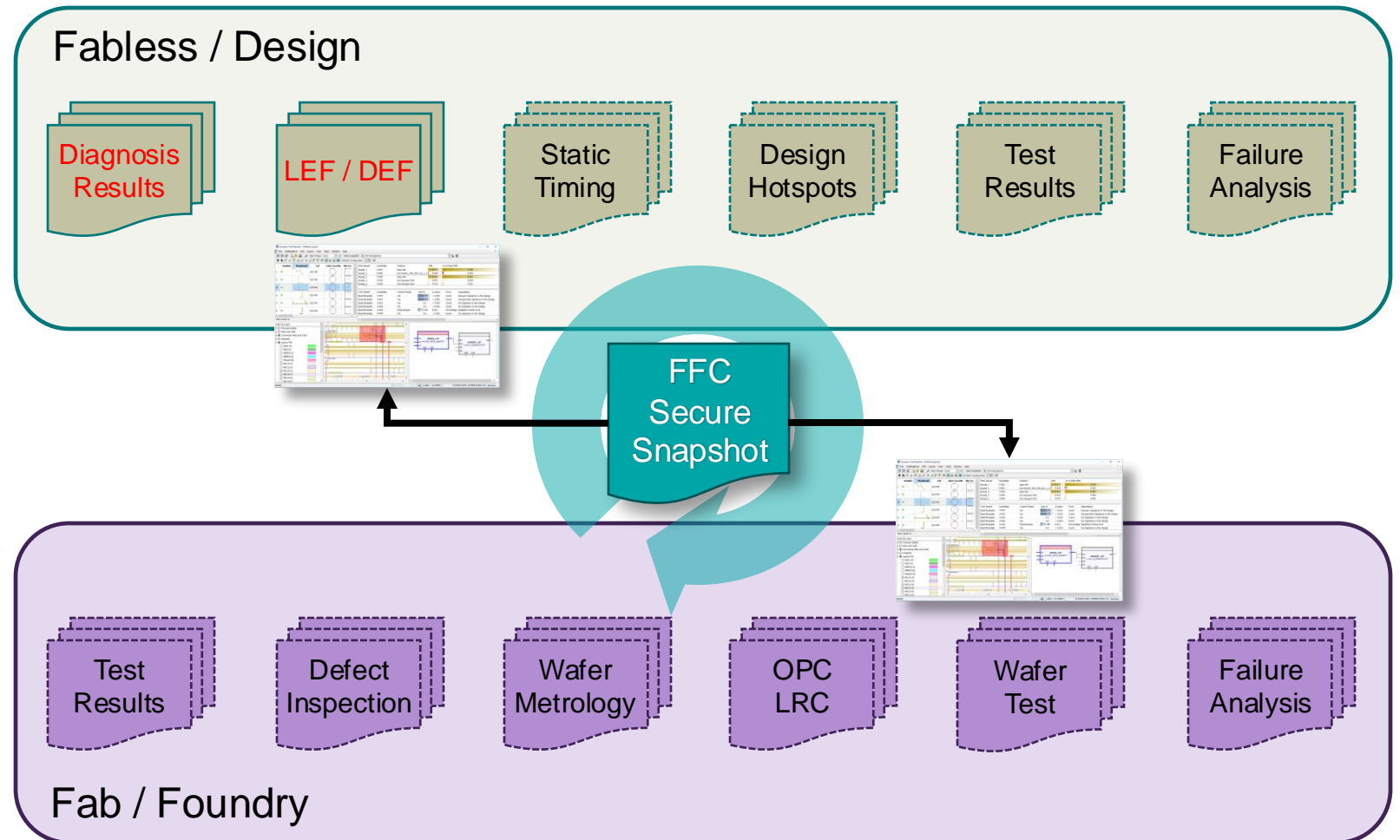
- Synopsys SLM IP and 3rd party monitors are embedded inside chips, including Voltage, Temperature, Ring Oscillator, Path delay, Clock delay, etc.
- Test results at multiple test conditions identifies process, design, simulation, and reliability problems
- Performance and reliability of chips is monitored through whole product lifecycle
- Local and web apps available



Fab Fabless Collaboration

Using manufacturing and diagnosis results

- FFC flow allows to securely share diagnosis results between Fabless/Design and Fab/Foundry
- Design data is protected
- Automated for each wafer
- Each partner sends only what they want to share
- Each partner can continue the analysis with their local data, and share again if needed
- Currently used by all major foundries (with Yield Explorer)



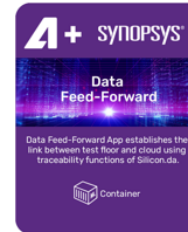
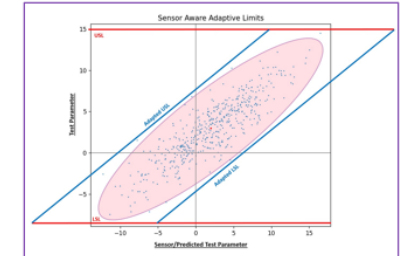
Tester Edge Applications

Using production test results on test floor

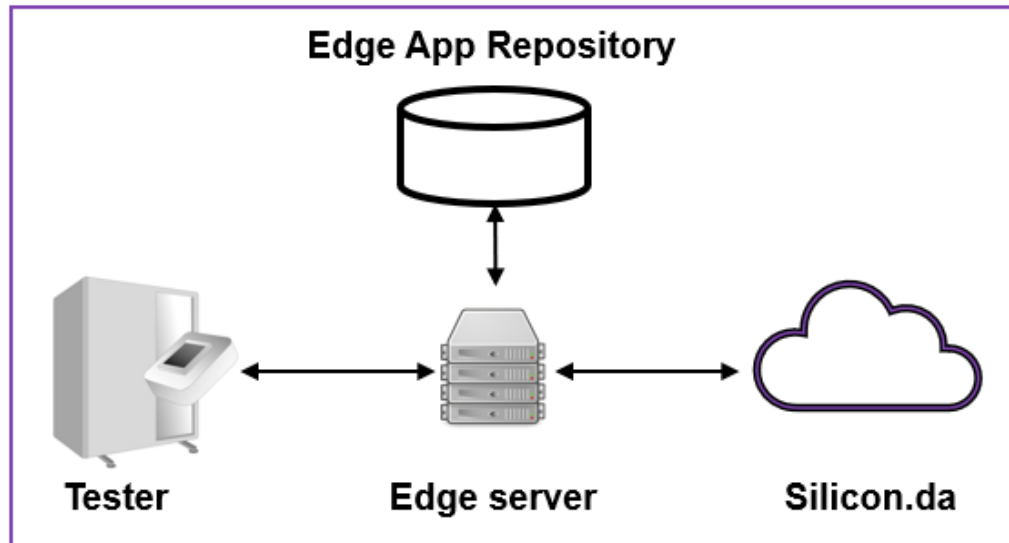
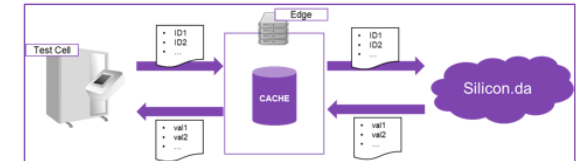
- Synopsys provides Silicon.da applications for the Advantest ACS Edge platforms
- The applications connect to the Silicon.da system (local or cloud)
- Further collaborations planned with other tester companies



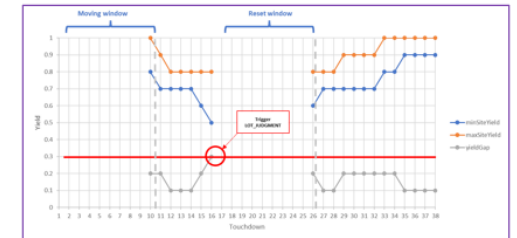
“Improve silicon quality by adjusting test limits using on-chip sensors in real-time”



“Link between test floor and Silicon.da cloud system using traceability functions”



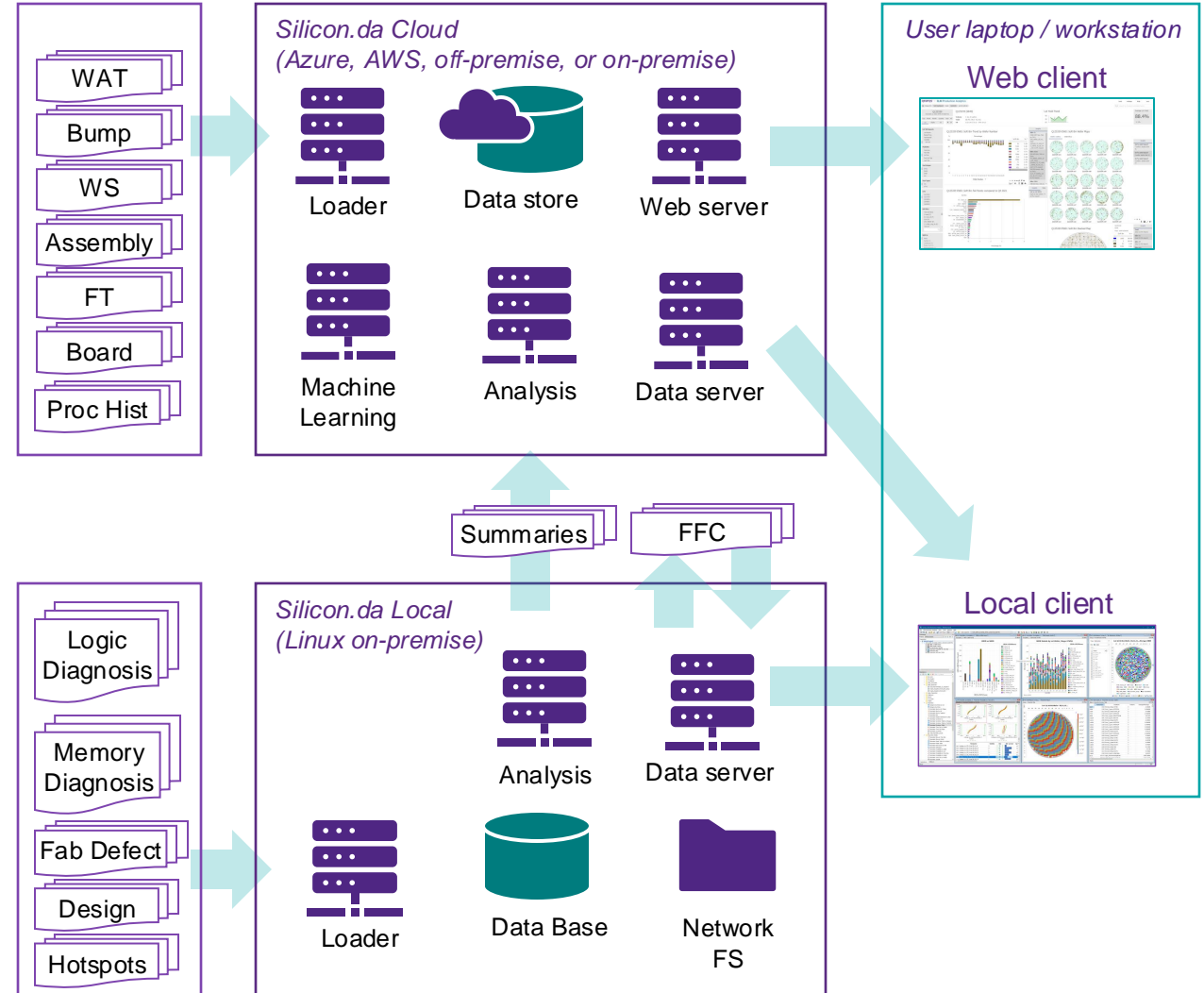
“Detection of yield gap during testing across sites”



Silicon.da Summary

Engineering and production data analytics

- A complete solution for Yield ramp
- Analytics for design-centric diagnosis, test program results, packaging and fab data
- Web and local client applications, with machine learning and built-in applications
- Scalable from a few wafers to millions
- Secure data exchange with foundries



THANK YOU

Our
Technology,
Your
Innovation™