Silicon.da

Silicon Insights and Data Analytics from Design to Manufacturing

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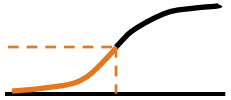
June 2024

Yield Explorer + Silicondash = Silicon.da

Product Manufacturing … from NPI through HVM

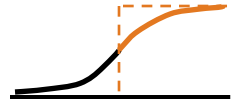


Yield Explorer

- New Product / Process
- Design Centric Analytics
- Interactive Test Analytics

- For systematic failure mechanisms
- For design – process interactions
- Logic and Memory diagnostics
- New Product Introduction and Process characterization
- Interactive data preparation and data analysis
- Custom analytics flows and reporting
- Failure Analysis link

silicondash

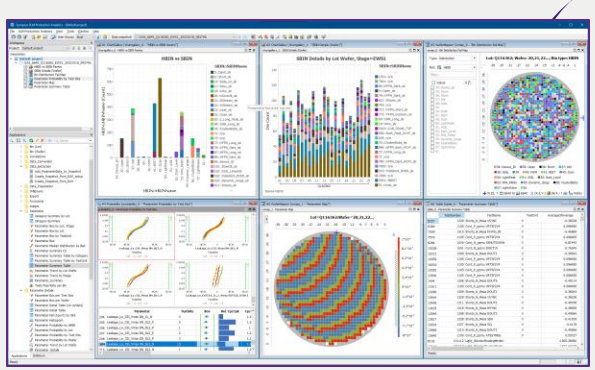


- Yield Management System
- Production / Quality Control
- Volume Test Analytics Automation

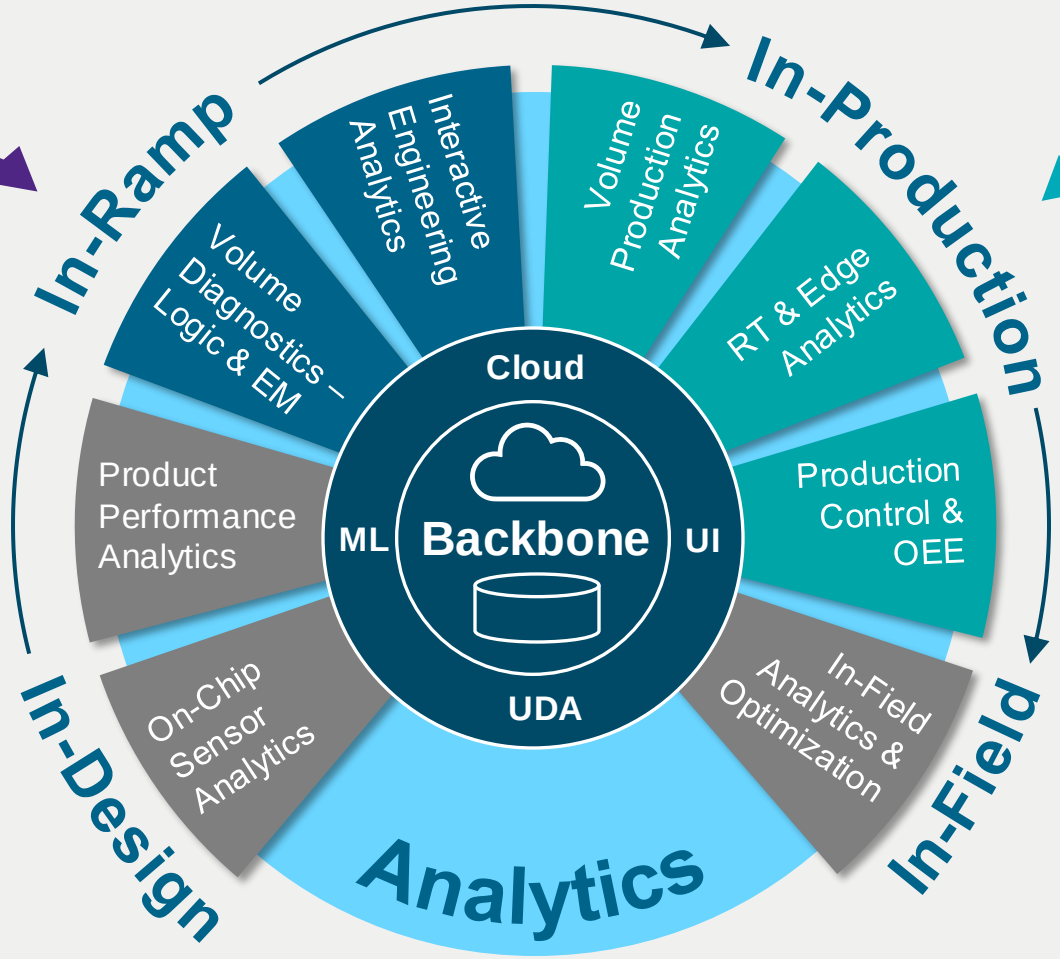
- For random and systematic yield and performance issues
- For operational issues and excursions on manufacturing flow
- Automated data mining on large volumes
- All incoming material analyzed automatically
- Web-browser high-speed analytics and reporting
- Automated production control strategies

Silicon.da Platform

Yield Explorer
=> Local client



Test data (2023.03)
Diagnostics (2024.03)



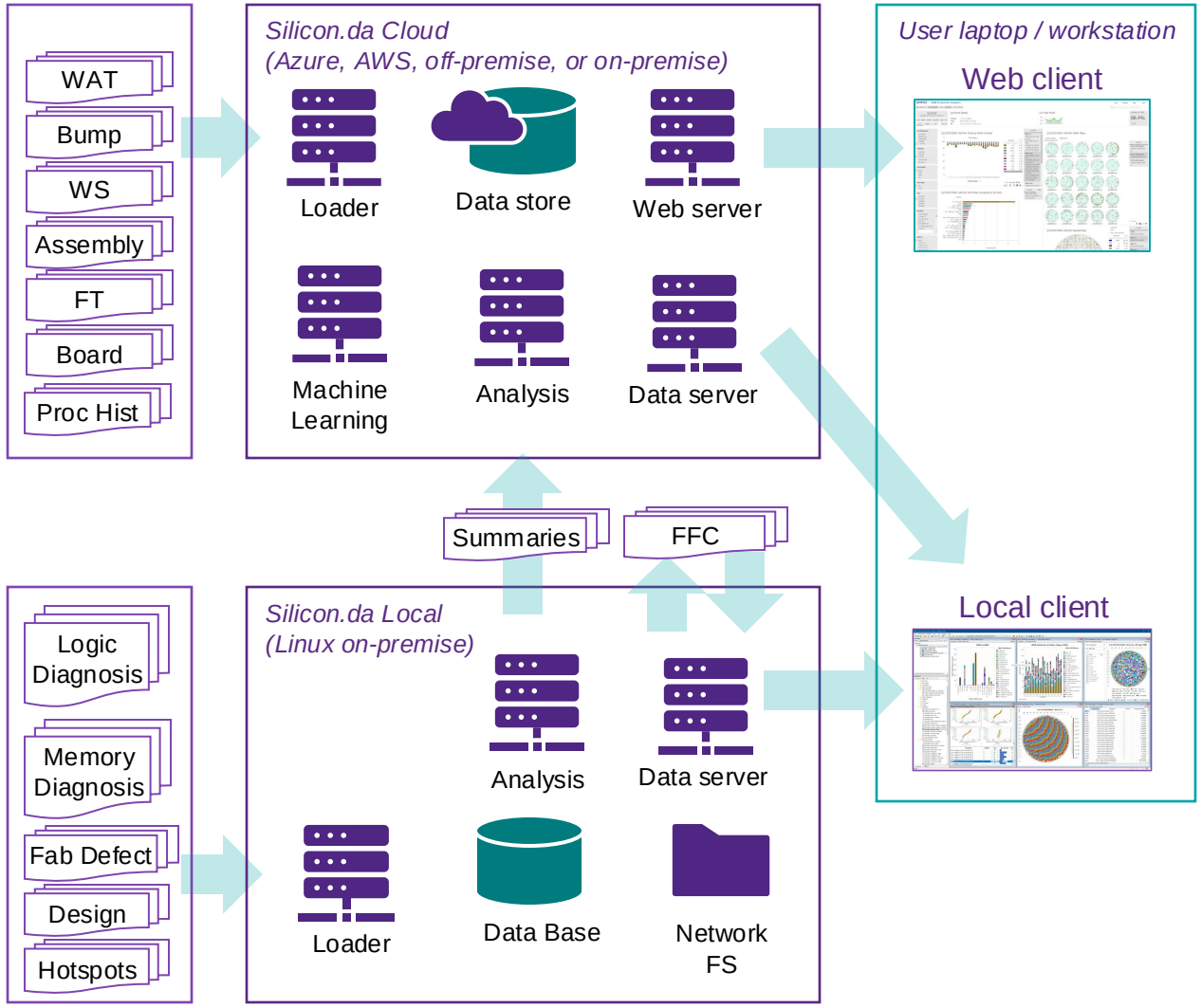
Silicondash
=> Web client

Test data (2023.03)
Diagnostics (2024.03)
ML platform (2024.03)

Platform architecture

Engineering and production data analytics

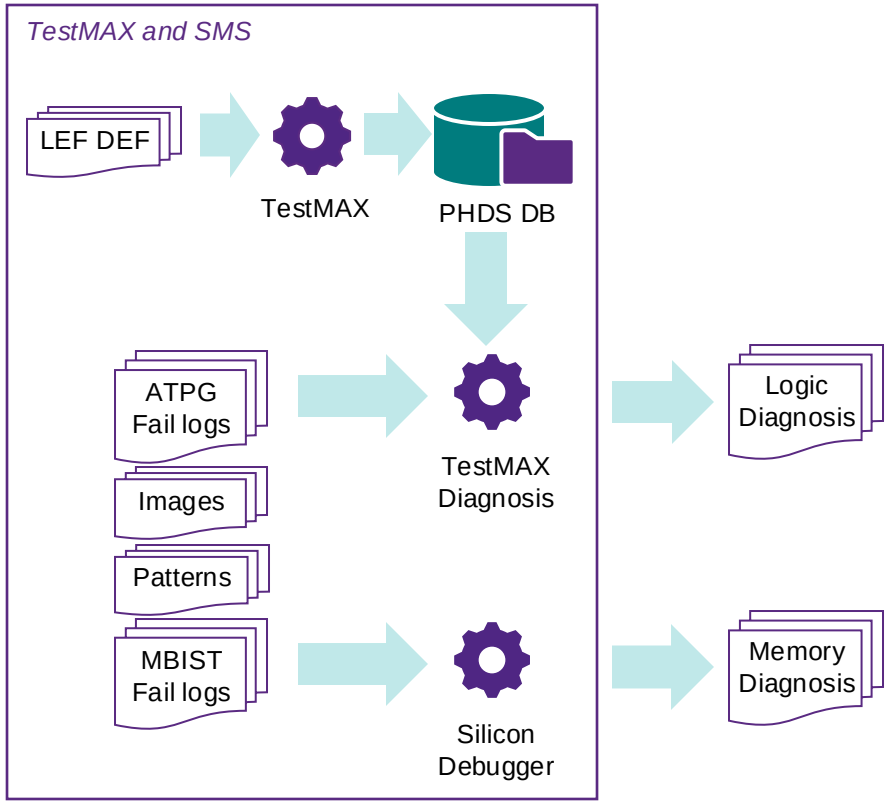
- Test results and diagnosis summaries are loaded to cloud (or local) data servers
- Design and diagnosis details are loaded to local data servers
- Machine Learning runs in cloud servers
- Additional test and fab data (if available) are loaded to cloud or local servers
- Web client for cloud data
- Local client for any data



Diagnosis flow

Test fail diagnosis

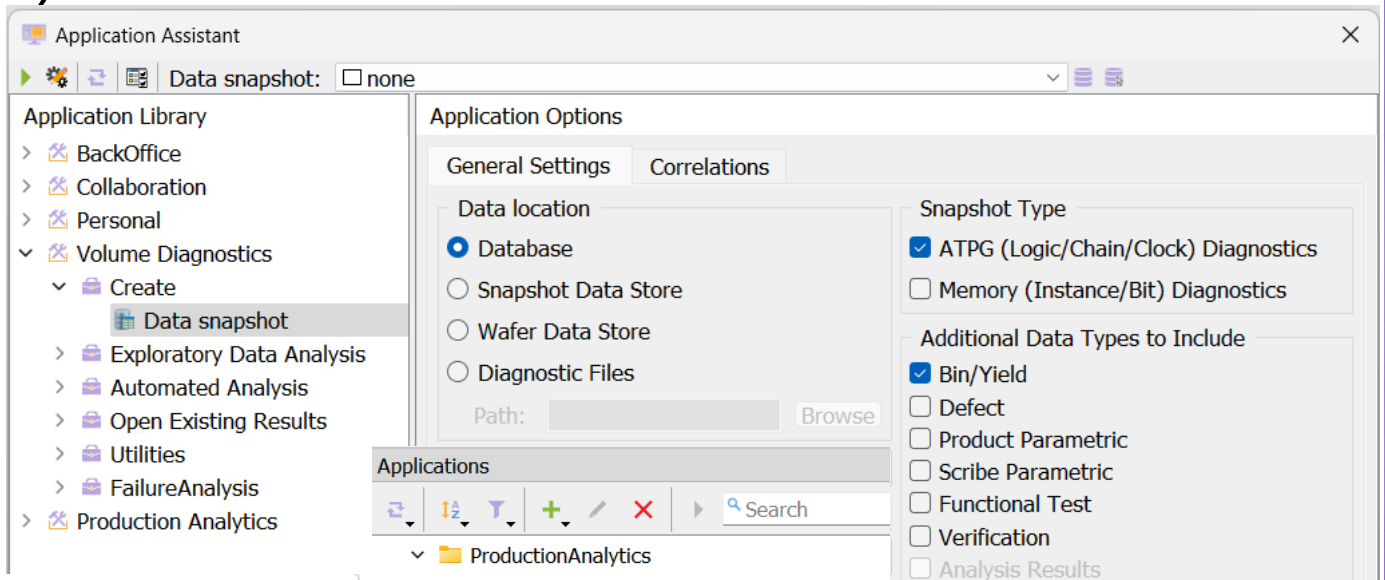
- LEF DEF is converted to PHDS Data Base
- ATPG fail logs are diagnosed with TestMAX Diagnosis (or 3rd party tools) to identify fail logic and chain candidates with probability scores
- MBIST fail logs are diagnosed with SMS Yield Accelerator Silicon Debugger (or 3rd party tools) to identify failed memories and bits
- Design images and test patterns are used during diagnosis process
- Logic and Memory diagnosis results are loaded to Silicon.da

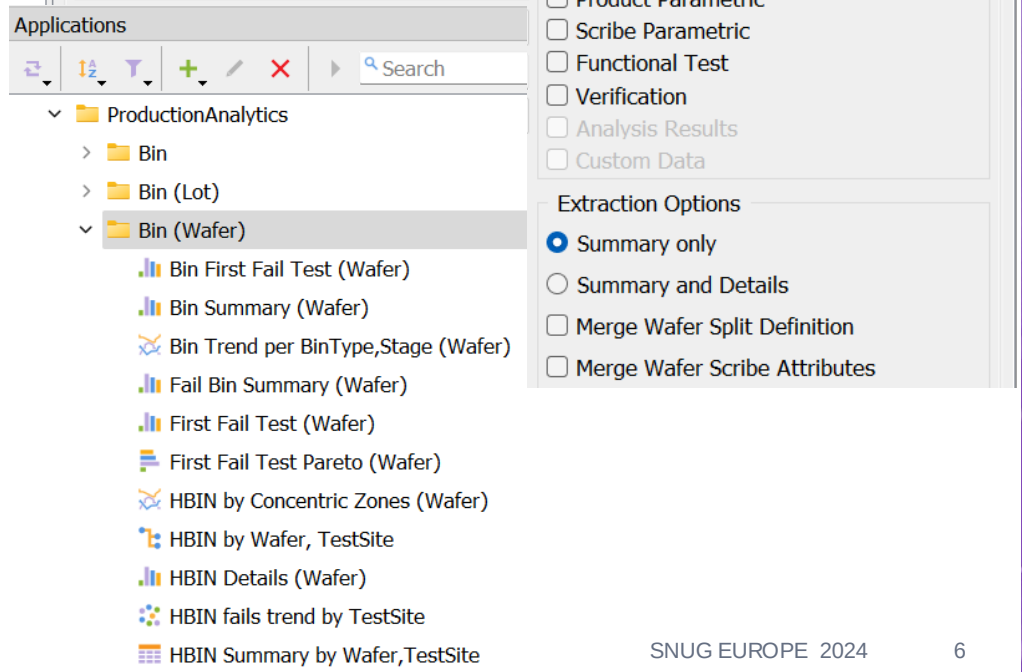


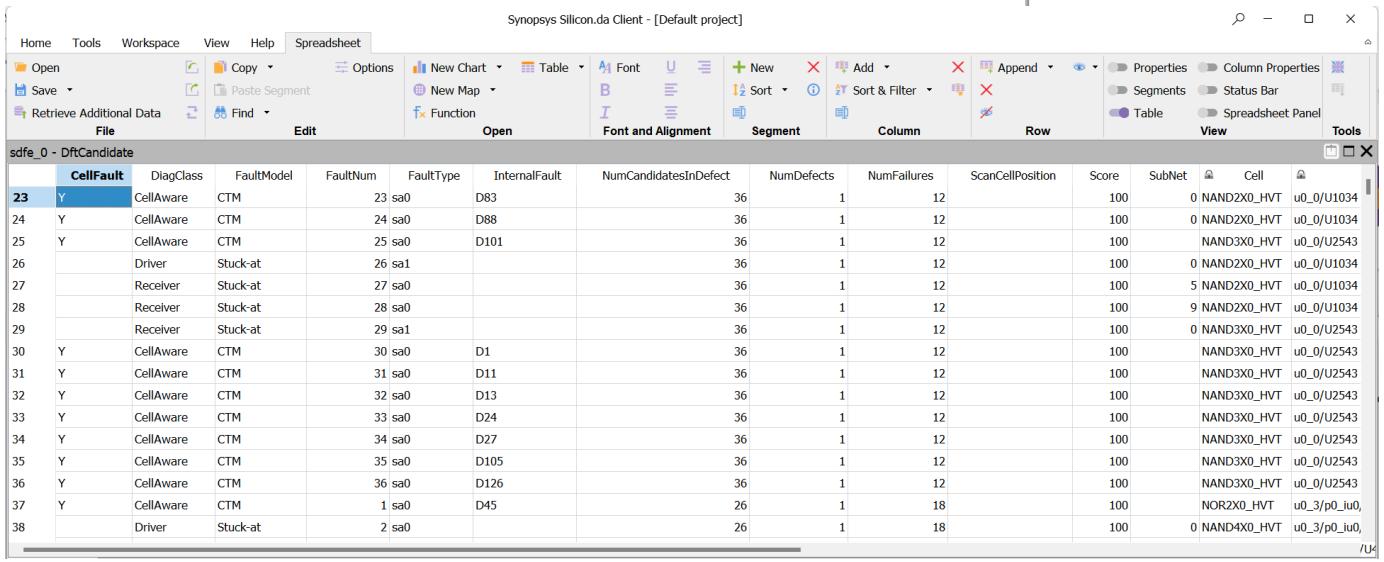
Start the analysis with Local client

Using Local (Diagnostics) or Cloud (Test) data

- Open the local app (windows or linux)
- Login to the Local or Cloud database
- Use Application Assistant to create a local snapshot
- Use predefined Application Tasks and Flows for analytics
- Continue with custom analysis if needed







	CellFault	DiagClass	FaultModel	FaultNum	FaultType	InternalFault	NumCandidatesInDefect	NumDefects	NumFailures	ScanCellPosition	Score	SubNet	Cell	
23	Y	CellAware	CTM	23	sa0	D83	36	1	12		100	0	NAND2X0_HVT	u0_0/U1034
24	Y	CellAware	CTM	24	sa0	D88	36	1	12		100	0	NAND2X0_HVT	u0_0/U1034
25	Y	CellAware	CTM	25	sa0	D101	36	1	12		100		NAND3X0_HVT	u0_0/U2543
26		Driver	Stuck-at	26	sa1		36	1	12		100	0	NAND2X0_HVT	u0_0/U1034
27		Receiver	Stuck-at	27	sa0		36	1	12		100	5	NAND2X0_HVT	u0_0/U1034
28		Receiver	Stuck-at	28	sa0		36	1	12		100	9	NAND2X0_HVT	u0_0/U1034
29		Receiver	Stuck-at	29	sa1		36	1	12		100	0	NAND3X0_HVT	u0_0/U2543
30	Y	CellAware	CTM	30	sa0	D1	36	1	12		100		NAND3X0_HVT	u0_0/U2543
31	Y	CellAware	CTM	31	sa0	D11	36	1	12		100		NAND3X0_HVT	u0_0/U2543
32	Y	CellAware	CTM	32	sa0	D13	36	1	12		100		NAND3X0_HVT	u0_0/U2543
33	Y	CellAware	CTM	33	sa0	D24	36	1	12		100		NAND3X0_HVT	u0_0/U2543
34	Y	CellAware	CTM	34	sa0	D27	36	1	12		100		NAND3X0_HVT	u0_0/U2543
35	Y	CellAware	CTM	35	sa0	D105	36	1	12		100		NAND3X0_HVT	u0_0/U2543
36	Y	CellAware	CTM	36	sa0	D126	36	1	12		100		NAND3X0_HVT	u0_0/U2543
37	Y	CellAware	CTM	1	sa0	D45	26	1	18		100		NOR2X0_HVT	u0_3/p0_iu0,
38		Driver	Stuck-at	2	sa0		26	1	18		100	0	NAND4X0_HVT	u0_3/p0_iu0,

Automated Volume Diagnostics

Using Logic / Chain diagnosis results

- Automated analysis identifies statistical outliers for multiple control factors
- Design statistics and critical area are used to normalize results and determine expected fail ratios
- Review fails by standard cell, cell internal, instance, net, via, design block, fault model, layers, etc.
- Strength of each outlier and the Yield impact is calculated
- Review trends, select outliers and drilldown to maps and failure analysis selection

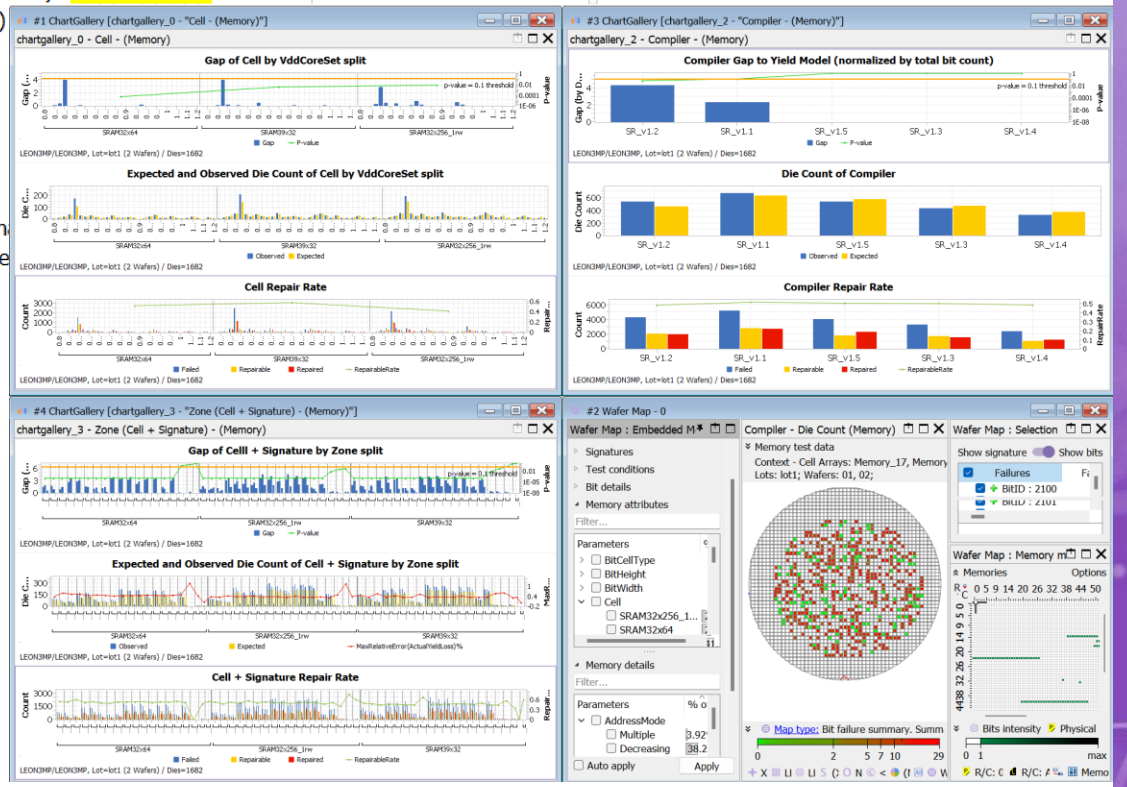
Control Factor	Distribution	P-value	Gap %	Count	Strength	YL %
Category + Cell		0.0001	29.1	90	6.3	37.5
Category + CTMLayers		0.1297	-	-	-	-
Category + Layers		0.1297	-	-	-	-
Cell		0.0001	30.7	94	6.5	39.2
Cell + Component		0.0001	9.1	115	4.4	47.9
Cell + InternalFault		0.0001	25.0	79	6.9	32.9
Cell + InternalFaultElement		0.0001	26.5	150	7.3	62.5
Cell + Layers		0.0528	4.0	96	5.4	40.0
Cell + Placement		0.0001	11.2	88	5.3	36.7
Cell + Transistors		0.0001	26.3	147	6.7	61.3
CellGroup		0.9692	-	-	-	-
Component		0.0379	18.1	86	2.0	35.8
Component (Cell)						
Component (ComponentType)						
DesignBlock						
DiagClass						
Diagnosable						
Equipment						
FaultModel						
FaultType						
Instance						
Instance + InternalFault						
Net						
Net + Subnet						
PhysicalLayer						
Placement (Cell)						
Via						
ViaLayer						

Automated Volume Diagnostics

Using Memory diagnosis results

- Automated analysis identifies statistical outliers for multiple control factors
- Memory design attributes are used to normalize results and determine expected fail ratios
- Review fails by memory design, bit cell type, compiler, topological and electrical fault signature, zone, etc.
- Strength of each outlier and the Yield impact is calculated
- Review trends, select outliers and drilldown to maps and failure analysis selection

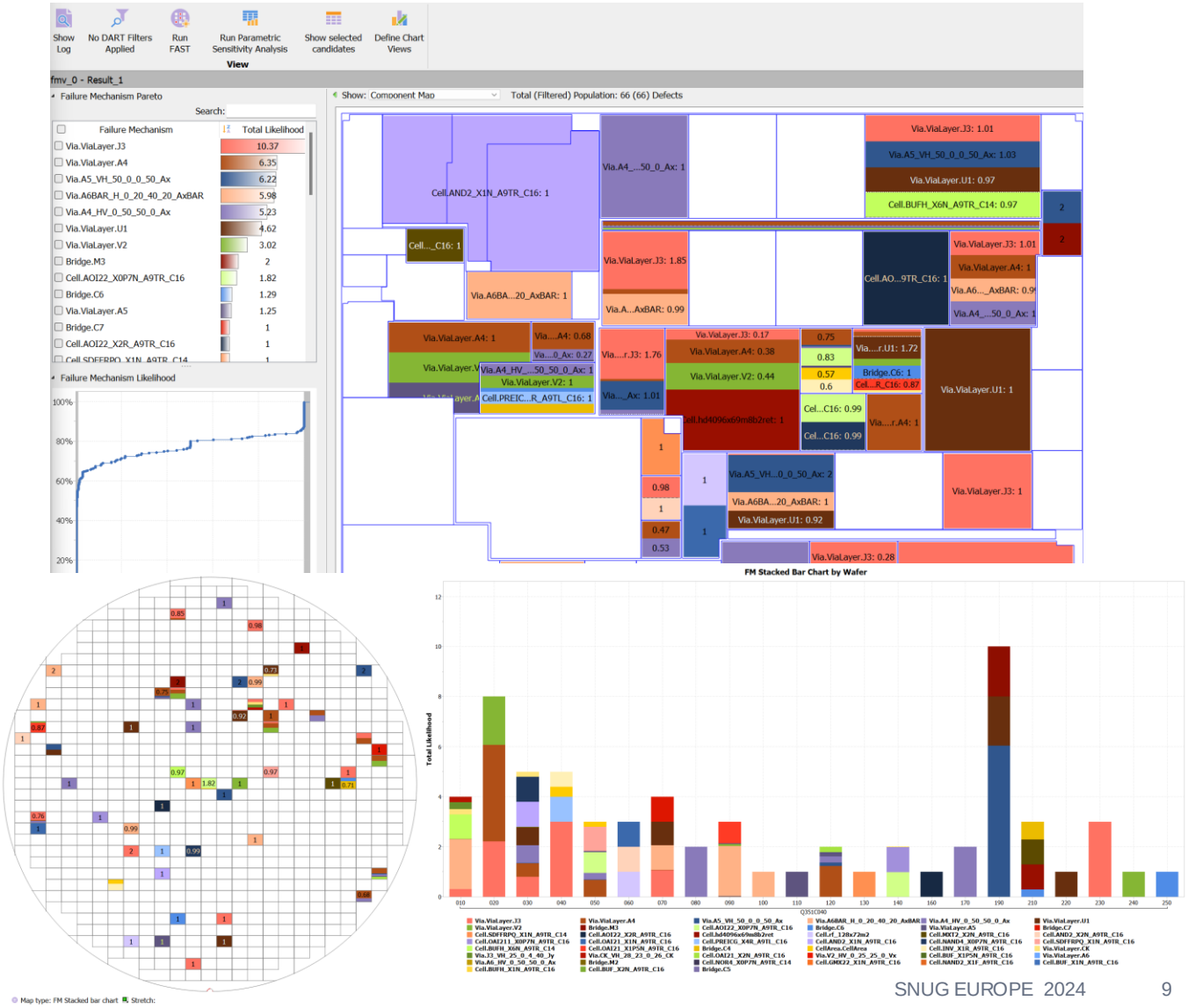
Control Factor	Distribution	P-value	Gap %	Count	Strength	YL %
BitCellType		0.2457	-	-	-	-
Cell		0.0001	4.0	1682	1.1	100.0
Compiler		0.0603	4.3	533	1.4	31.7
Equipment		1.0000	-	-	-	-
FaultSignature		0.0001	97.3	1682	100.0	100.0
LayoutX + LayoutY		0.0855	0.1	98	1.3	5.8
Lot		1.0000	-	-	-	-
Lot + Wafer		0.3041	-	-	-	-
Memory		0.0082	1.0	434	2.4	25.8
Memory (Cell + FaultSignature)		0.0496	0.4	216	23.8	12.8
Memory (Cell + Signature)						
Memory (Cell)						
MemoryType						
Reticle (Lot + Wafer)						
TestPattern						
Zone						
Zone (Cell + Signature)						
Zone (Memory + FaultSign						
Zone (Memory + Signature						



Failure Mode Analysis

Using Logic diagnosis results

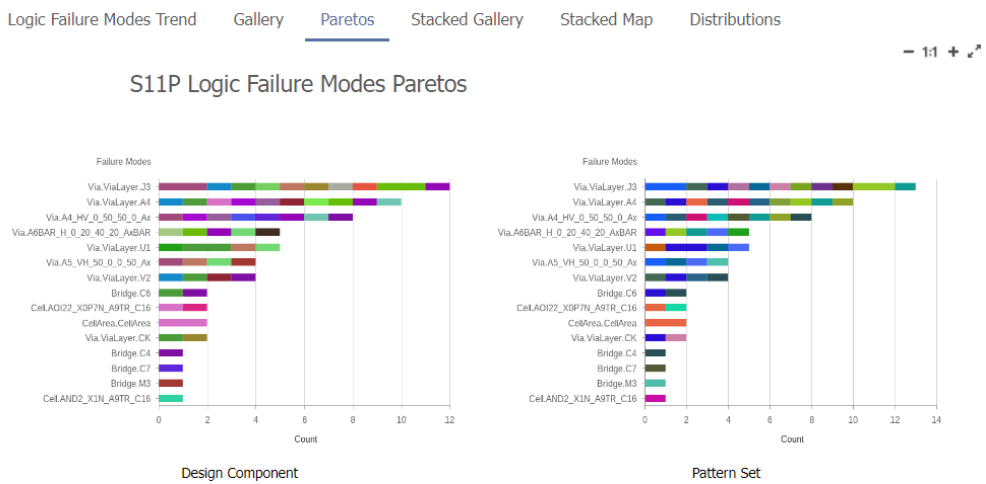
- Bayesian inference identifies the most important failure modes
- Design statistics and critical area and cell test models are used to improve results
- Results are analyzed by component design block
- Likelihood of each failure is estimated and aggregated
- Review trends, select outliers and drilldown to maps and failure analysis selection

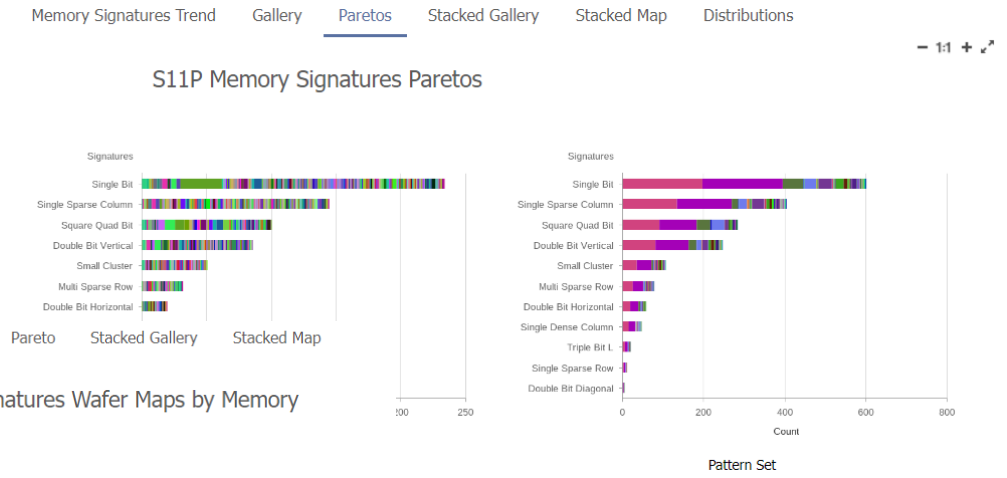


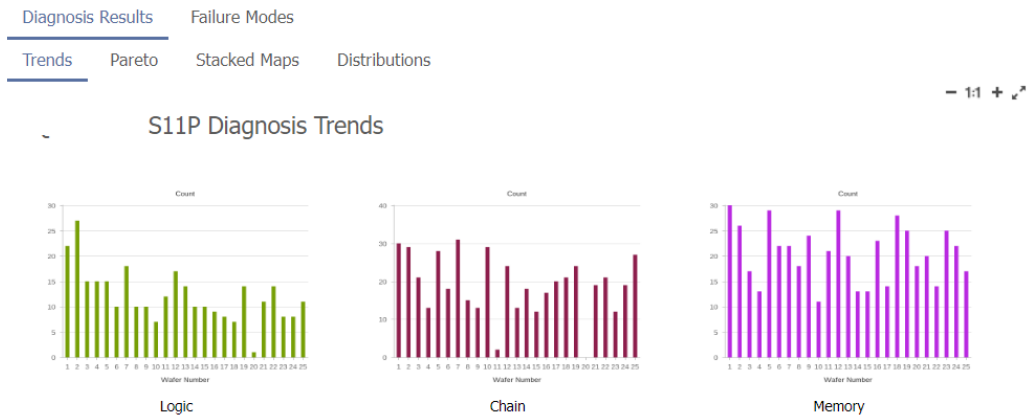
Diagnostics trends

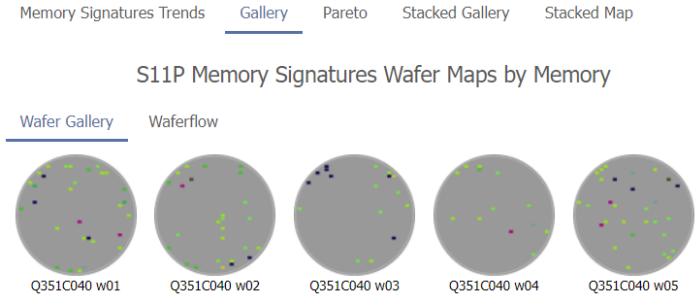
Using all diagnosis results

- Diagnostics summaries are shown in the web client
- Paretos and trends by wafer / lot or time-scope
- Single and stacked wafer maps
- Results using failure modes, design components, memories, bit signatures, etc.





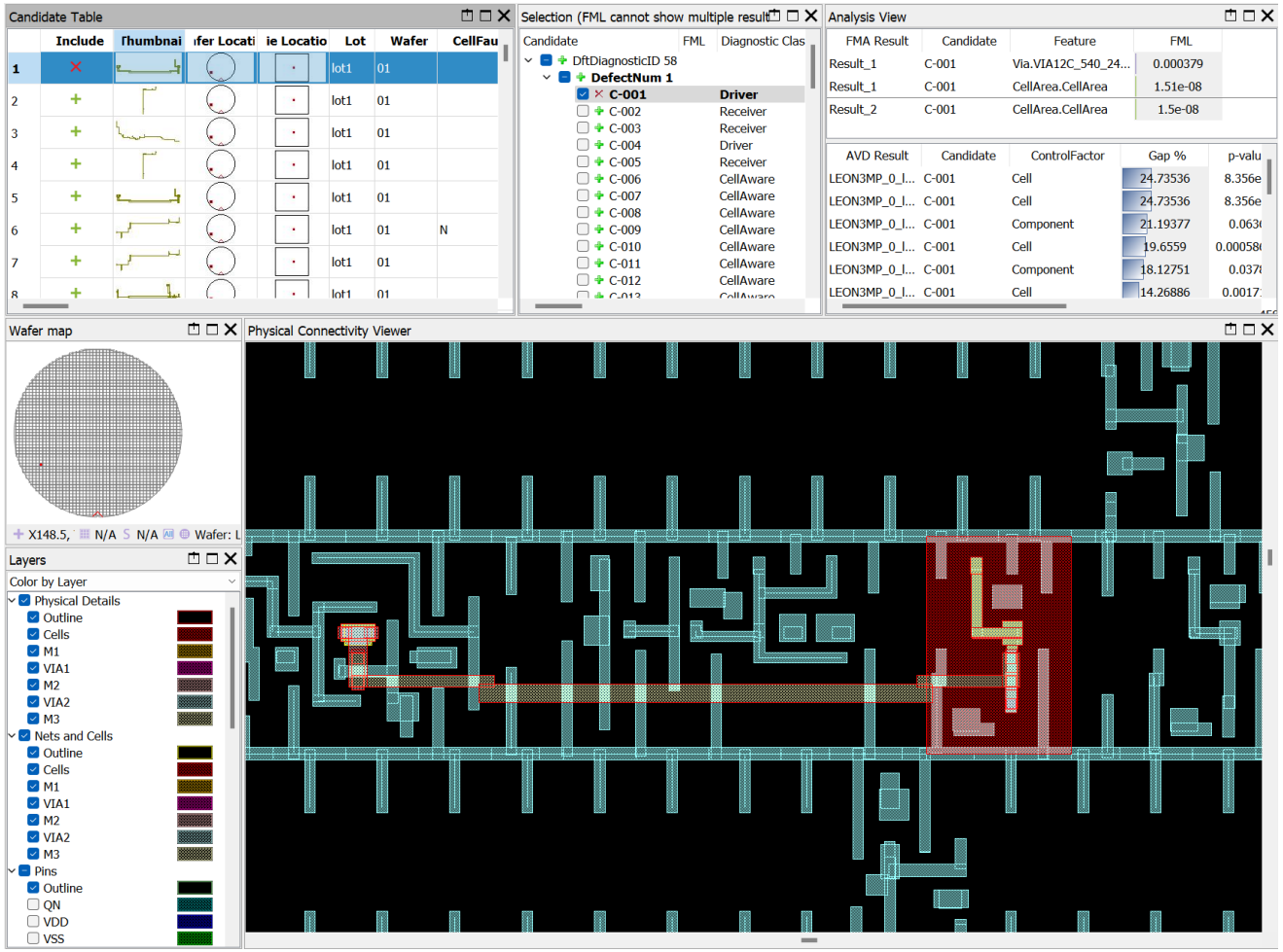




Failure Analysis Selection

Using Logic / Chain diagnosis results

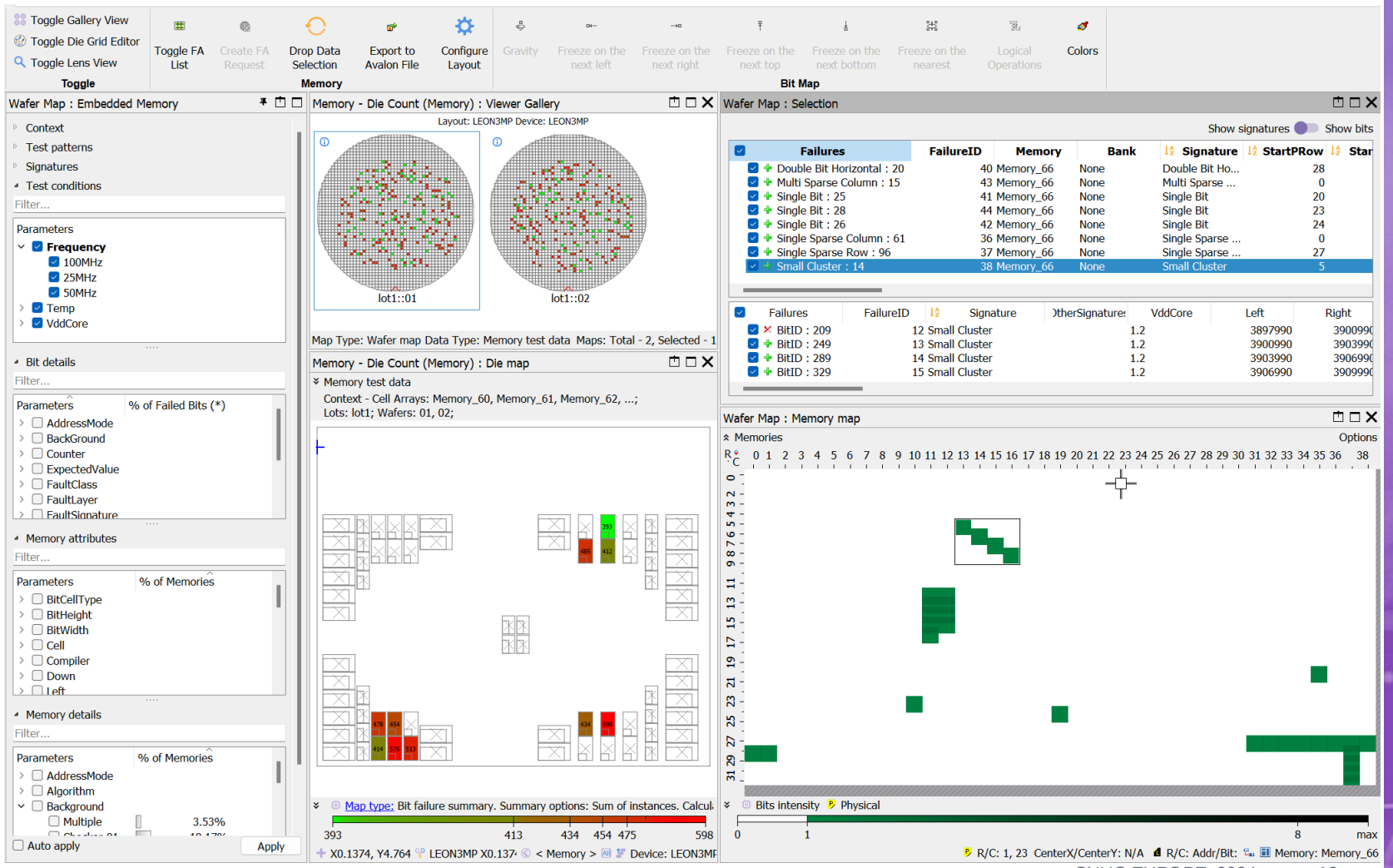
- Fail candidates identified as main Yield problems are reviewed and selected for failure analysis
- Filter by attributes, AVD and FMA results, overlay with GDS/OASIS, etc.
- Selected candidates are saved in a cart, and exported to Avalon or 3rd party format



Failed Memory and Bit Signatures

Using Memory diagnosis results

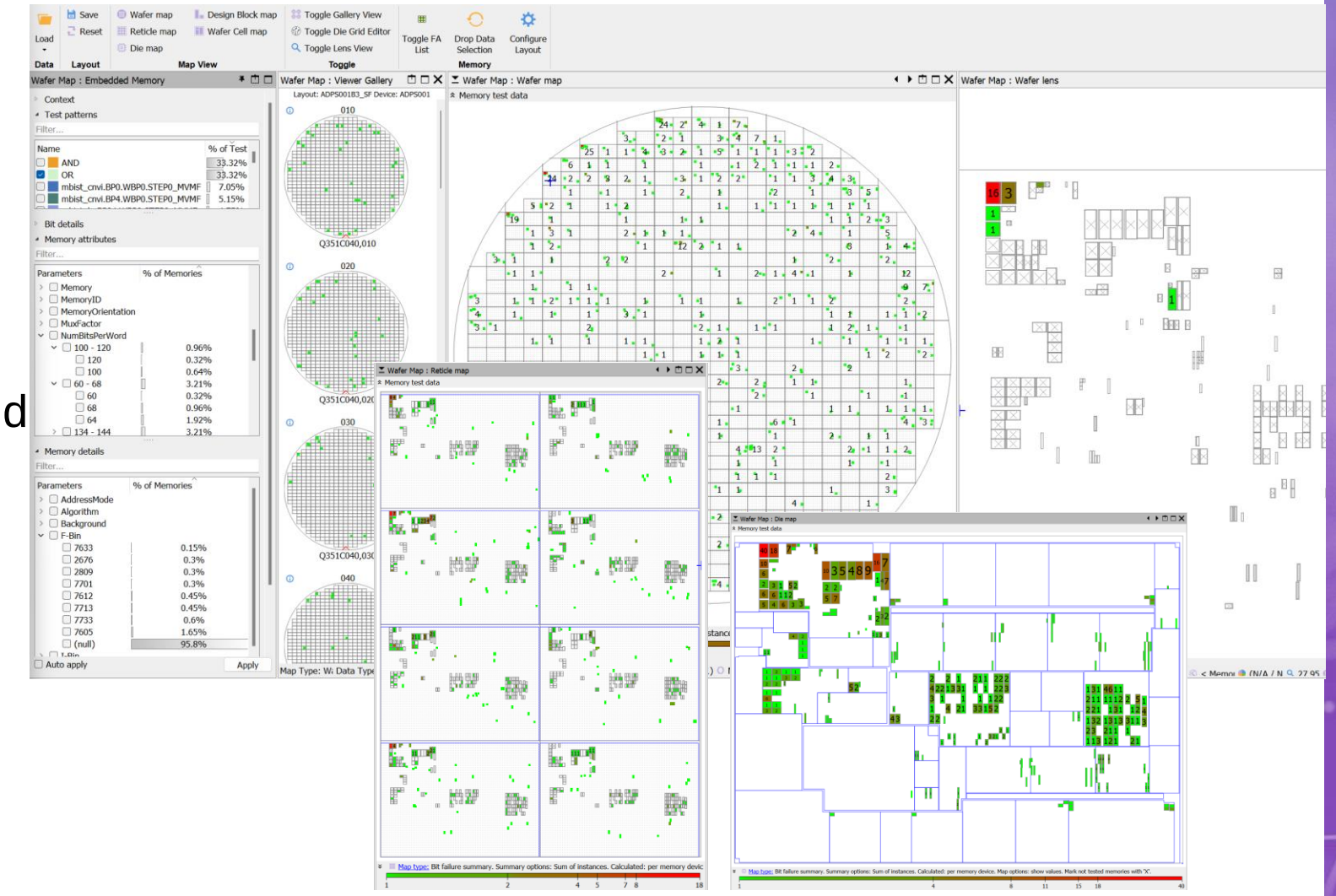
- Interactive UI to review failed memories and bit signatures
- Filter fails by test conditions, memory attributes, and algorithm or bit-level details
- Wafer, reticle or die stacks
- View fail bits with physical or logical maps
- Selected bits and signatures are saved in a cart, and exported to Avalon or 3rd party format



Failed Memories

Using MBIST production test results

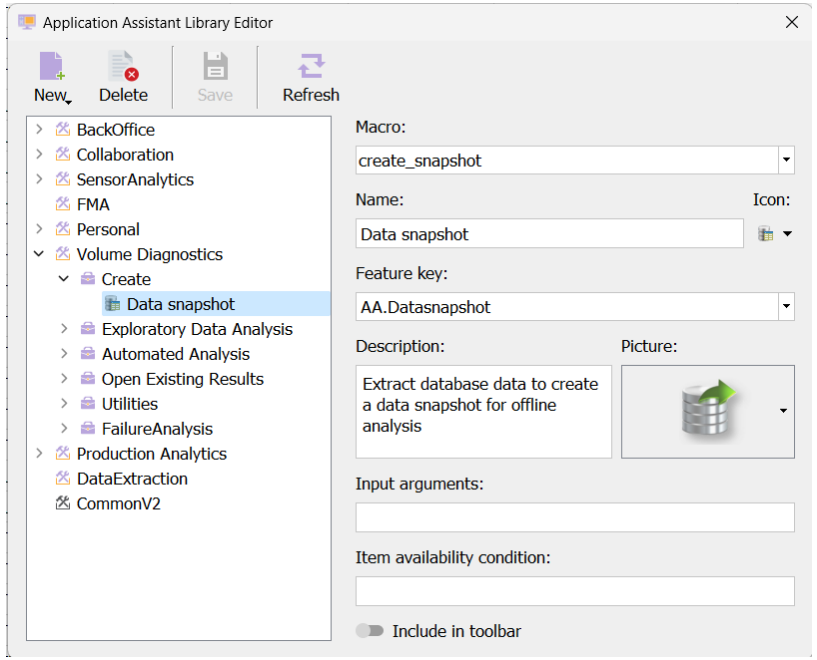
- Failed or repaired MBIST results are converted to memories using test pattern definitions
- Applies to high volume test, no additional data logging required
- Fails are filtered by test conditions, memory attributes, and algorithm details
- Wafer, reticle or die stacks
- Trends and paretos available by memory attributes
- Compatible with automated volume diagnostics analysis

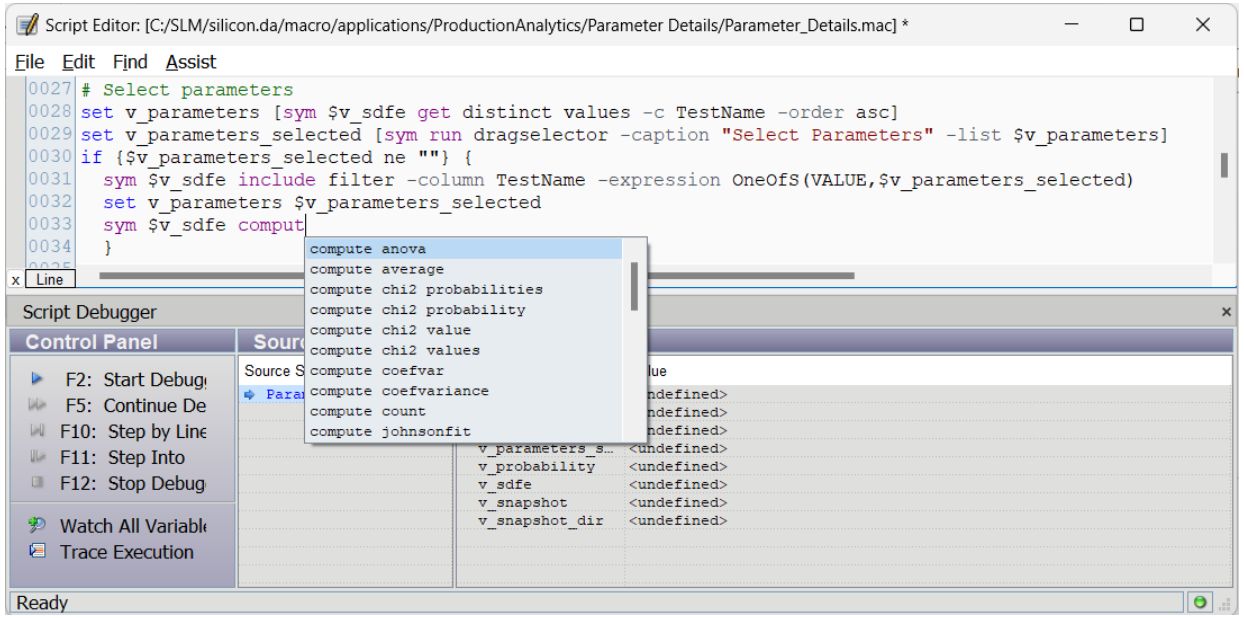


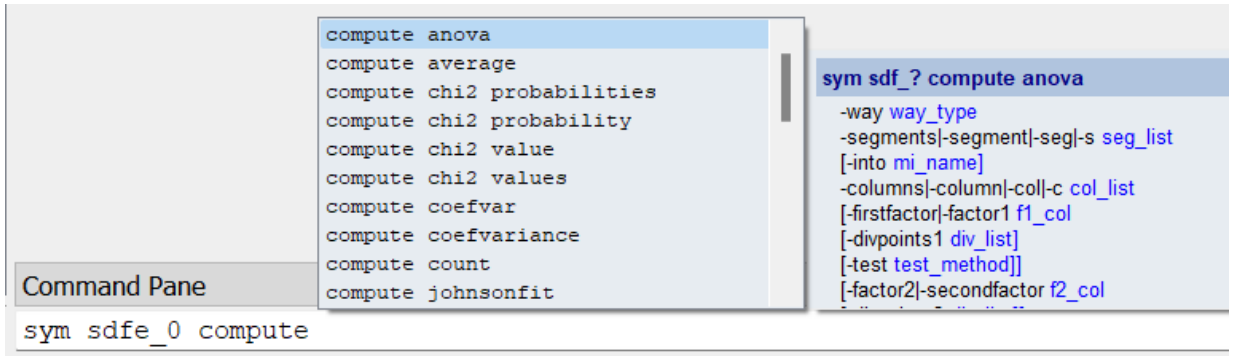
Commands and macros

Automation for the local application

- Use GUI or commands for any analytics
- Use predefined or custom macros
- Build macros using TCL or Python or R
- Script Designer includes lookahead help
- Package macros into applications



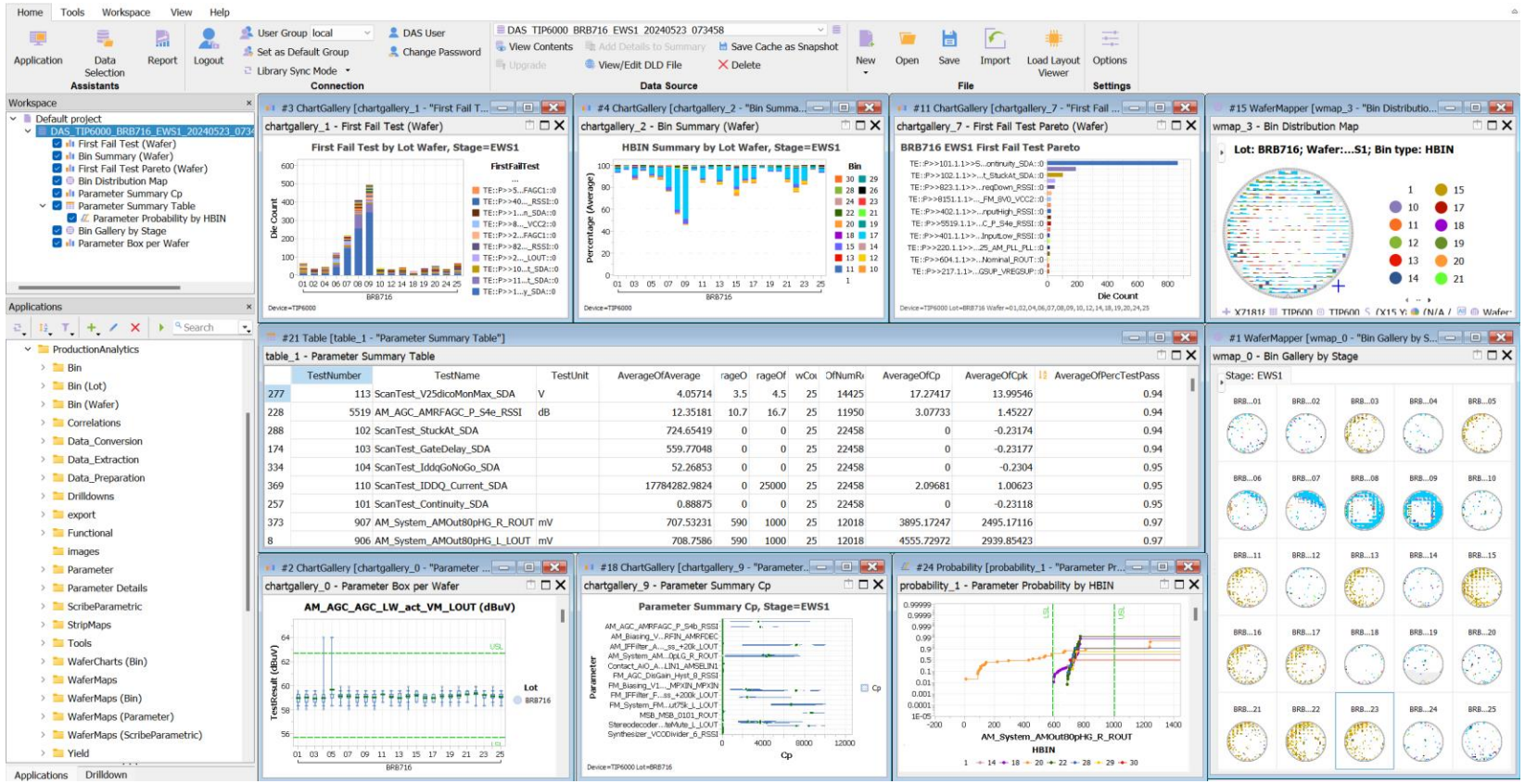




Custom analysis with Local client

Using any test results

- Download data from cloud, and/or import local files
- Create a local data snapshot with any data types required
- Use existing tasks and flows, or create your own
- Use analysis tools: charts, spreadsheet functions, statistics, maps, correlations
- Use TCL / Python / R macros
- Save, reuse and share tasks, macros and data snapshots



Virtual test limits analysis

Using production test results

- Review results with existing limits
- Set new virtual limits as desired
- Recalculate virtual fails and virtual bins
- Compare existing and virtual results

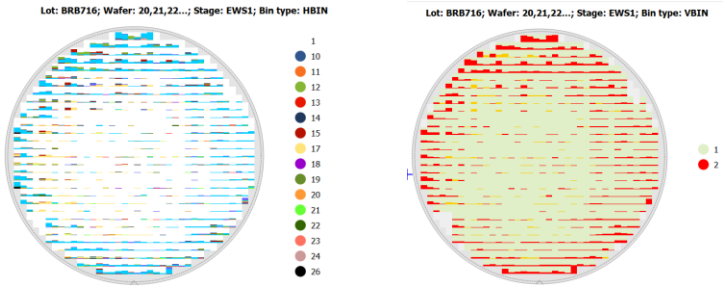
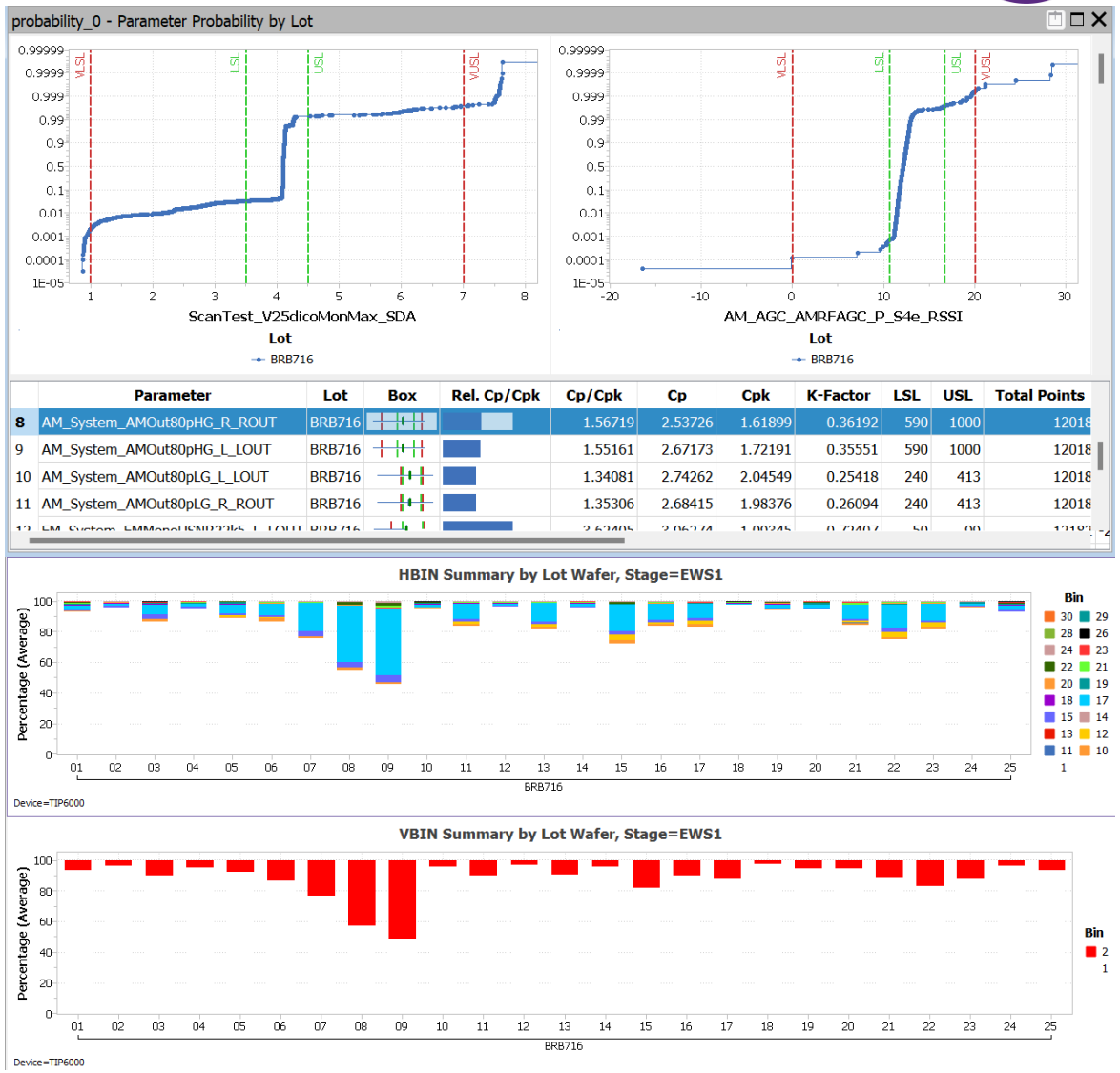


table_1 - Lot Wafer Yield ORIGINAL

	Month	Week	Stage	Lot	Device	TestSequence	01	02	03	04	05	06	07	08
1	M2014/01	W2014/02	EWS1	BRB716	TIP6000	0	0.929	0.958		0.950		0.865	0.759	0.552
2	M2014/02	W2014/06	EWS1	BRB716	TIP6000	0			0.868		0.889			

table_0 - Lot Wafer Yield VIRTUAL

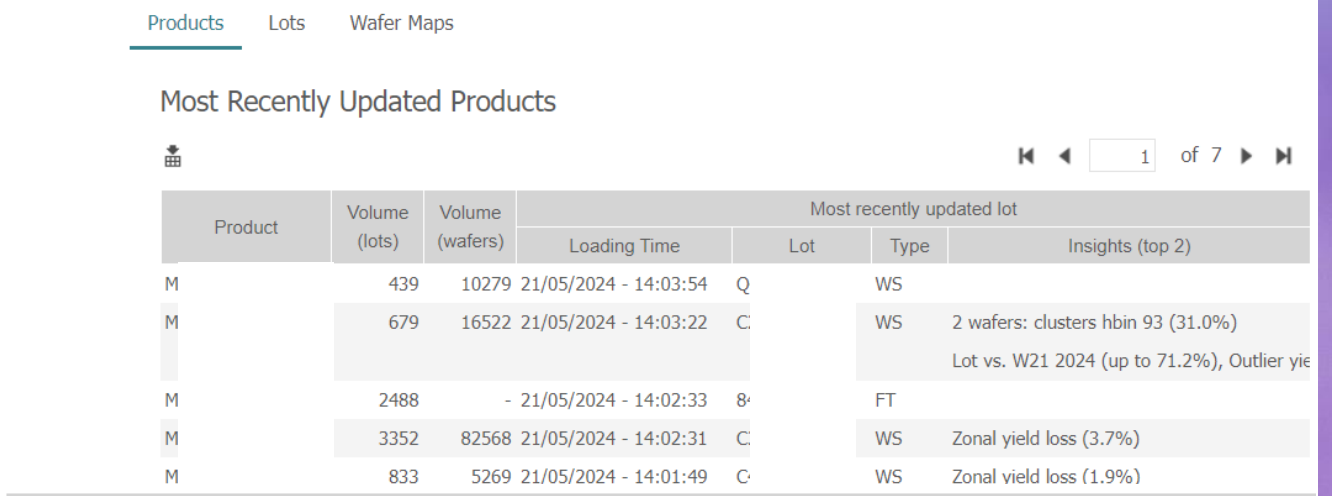
	Month	Week	Stage	Lot	Device	TestSequence	01	02	03	04	05	06	07	08
1	M2014/01	W2014/02	EWS1	BRB716	TIP6000	0	0.942	0.967		0.962		0.875	0.791	0.608
2	M2014/02	W2014/06	EWS1	BRB716	TIP6000	0			0.911		0.931			

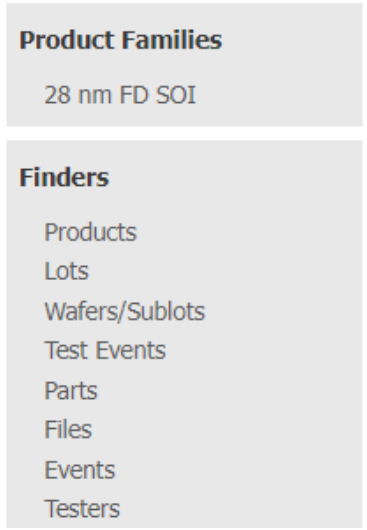


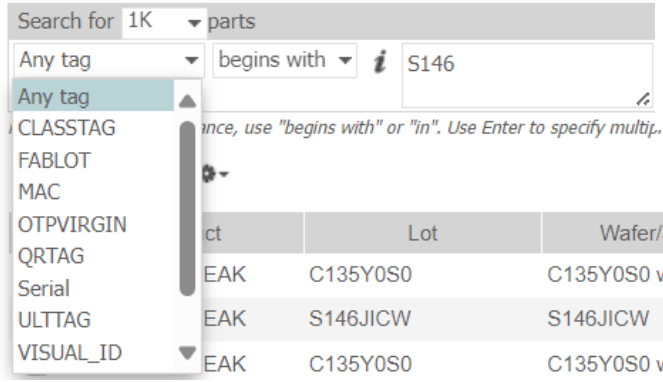
Start the analysis with Web client

Using Cloud data

- Open the web browser and login
- Start the analysis from a Dashboard
- Browse recent test results by product / lot (filtered by user permissions)
- Find data by product / stage / lot / file / any of the chip IDs / etc.
- Review insights and drilldown to details





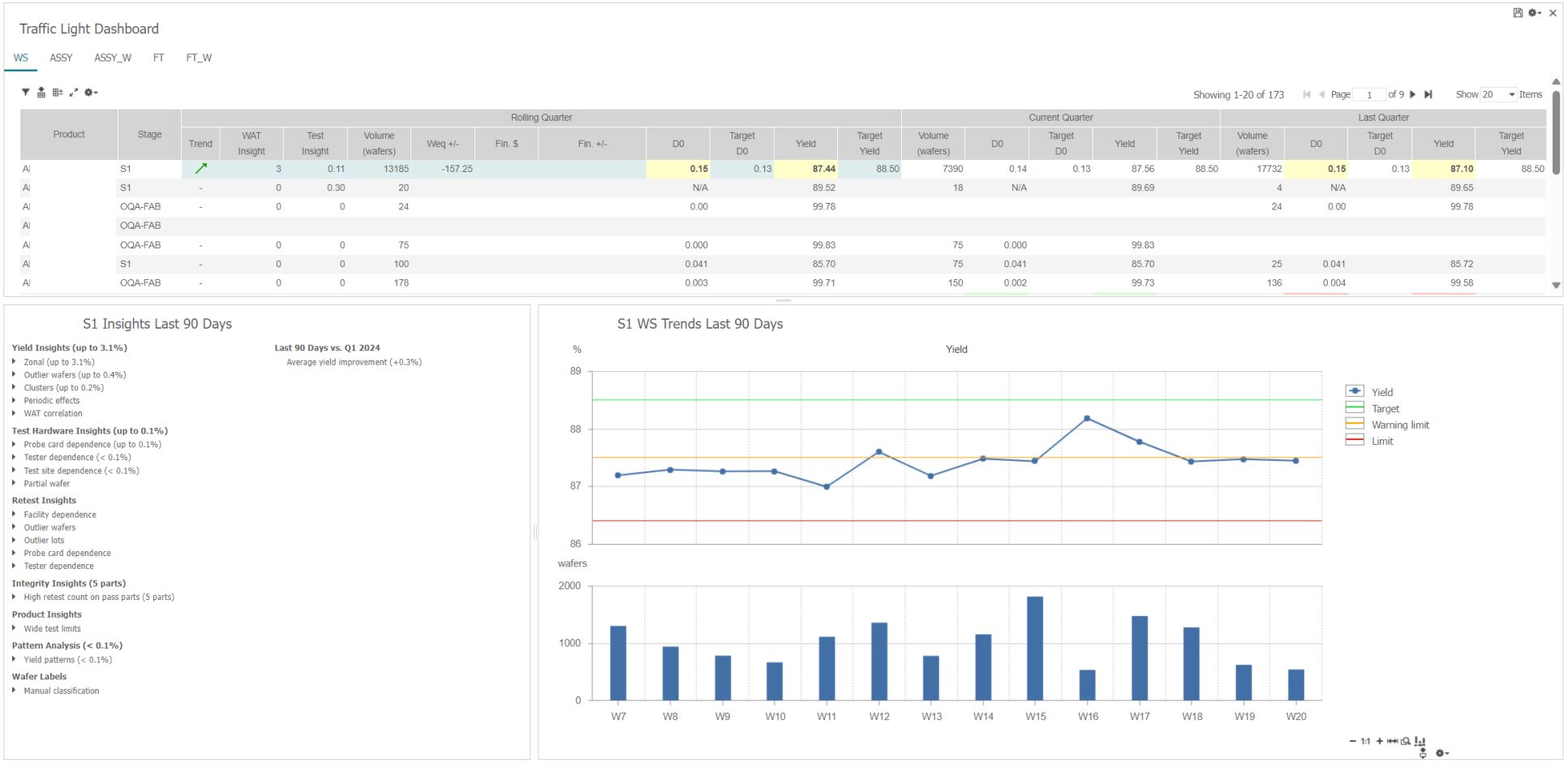


ct	Lot	Wafer/Sublot	X	Y	CLASSTAG	QRTAG
EAK	C135Y0S0	C135Y0S0 w11	26	-30	S146JICV_11182228_019088	S146JICV02504
EAK	S146JICW	S146JICW			S146JICW_11171724_001532	S146JICW03747
EAK	C135Y0S0	C135Y0S0 w24	32	-55		S146JICV10192

Production Traffic Light Dashboards

Using production test results

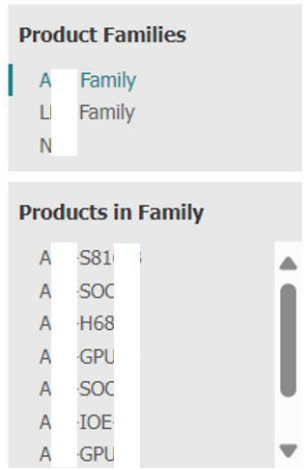
- Browse Yield and D0 trends, review insights, click to continue the analysis

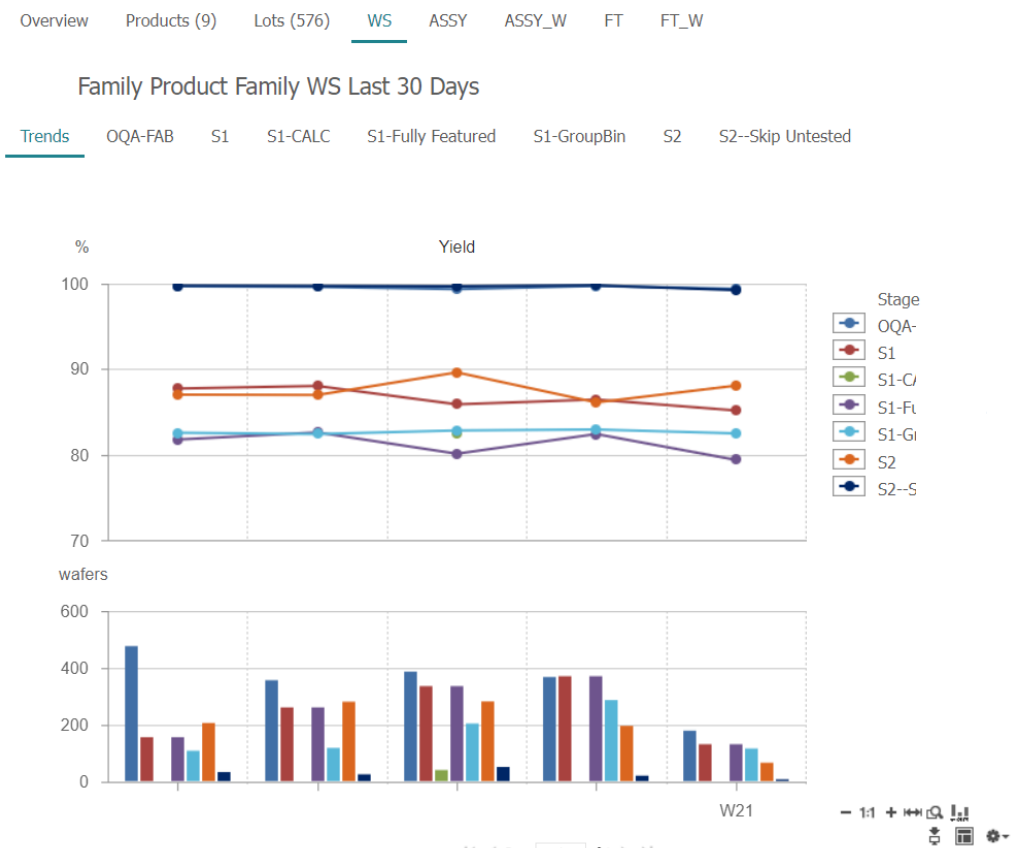


Product Families

Using production test results

- Create groups of similar products
- Compare trends and results within each group, by product or by lot
- Use Dashboards to compare summaries
- Click on any row in the table to go to the full analysis for the selected data





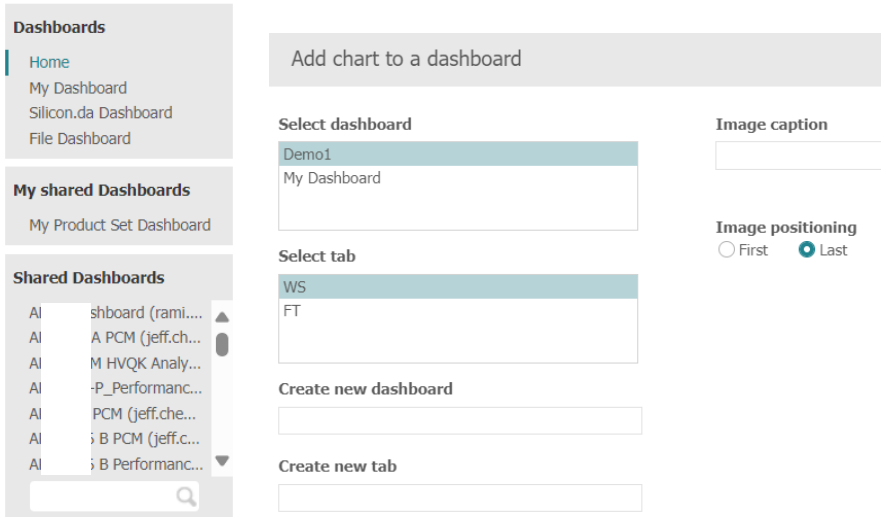
Family Product Family Reports Last 7 Days

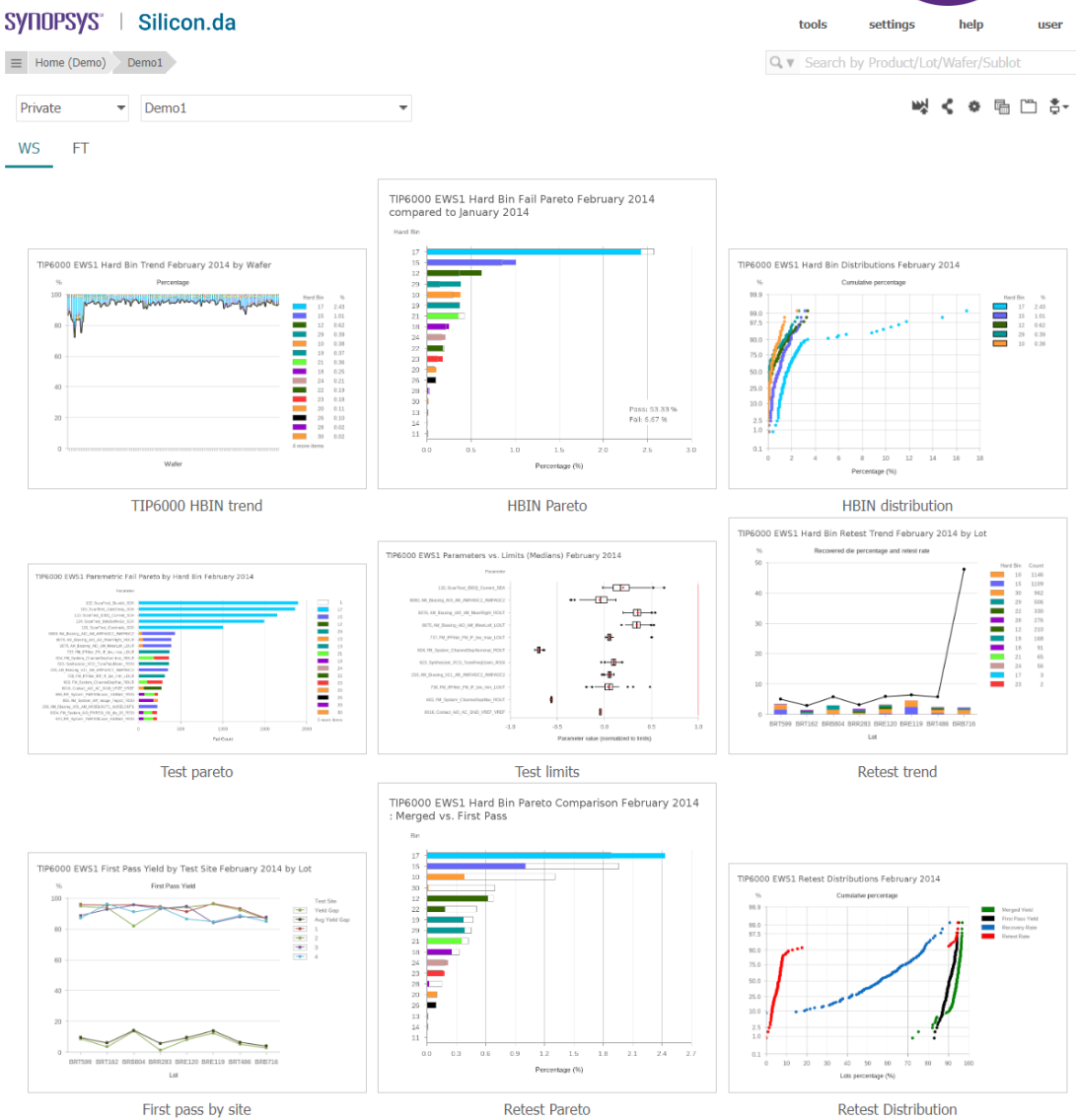
Product Family	Wafer Acceptance			Wafer Sort					Assembly				Assembly - Wafer				Final Test				Final Test - Wafer			
	Stage	Volume (lots)	Volume (wafers)	Stage	Volume (lots)	Volume (wafers)	Yield (%)	D0	Stage	Volume (lots)	Volume (sublots)	Yield (%)	Stage	Volume (lots)	Volume (wafers)	Yield (%)	Stage	Volume (lots)	Volume (sublots)	Yield (%)	Stage	Volume (lots)	Volume (wafers)	Yield (%)
Family	PCM	13	247	S2--S...	7	25	99.7	N/A	EOL	65	65	100.0	EOL	33	94	100.0	B6	24	24	62.3	B6	23	53	96.7
	PCM-C	11	225	S2	49	203	88.1	N/A									B6	13	13	68.1	B6	20	39	82.8
	PCM-Fl	1	5	S1-Gr...	55	294	82.4	N/A									B6	1	1	100.0	B6	1	3	76.4
	PCM-Fl	1	5	S1-F...	73	366	81.6	N/A									B6	47	47	66.4	B6	38	69	74.5
	PCM-O	13	247	S1	73	366	86.0	N/A									B6	7	7	15.8	B6	13	17	20.7

Personal Dashboards

Using production test results

- Create a personal dashboard for each project
- It is refreshed automatically every time
- Add any chart to the personal dashboard
- Click on any chart to go to the full analysis
- Share dashboards between colleagues





Automated Insights

Using production test results

- Data is analyzed for typical Yield and test problems
- Additional metrics are checked and reported when significant
- Insights are calculated at lot and wafer level, and aggregated to day, week, month, quarter, year, all scope
- Mouse hover shows mini charts for each insight, and click opens the report
- Start from the insights to identify the most important problems for each product on any time scope

TIP6000 EWS1 Insights Week 06 2014

Yield Insights (up to 2.2%)
- Outlier lots (up to 2.2%)
- Zonal (up to 1.7%)
- Periodic effects
- Clusters (up to 0.5%)
- Outlier wafers (up to 0.3%)
- Reticle/repetitive effect (< 0.1%)

Test Hardware Insights (up to 0.3%)
- Test site dependence (up to 0.3%)
- Loadboard dependence (up to 0.2%)
- Probe card dependence (up to 0.2%)
- Tester dependence (up to 0.2%)
- Gap in testing

Retest Insights
- Outlier wafers
- Outlier lots
- Loadboard dependence
- Probe card dependence
- Program name dependence

more...

Process Insights (< 0.1%)
- Distribution tails (< 0.1%)
  - 3 wafers: tails on 730, FM_IFFilter_FM_IF_bw_min_LOUT (< 0.1%)

Integrity Insights (2 parts)
- High retest count on pass parts (2 parts)

Product Insights (up to 0.8%)
- Test limit sensitivity (up to 0.8%)
- Wide test limits
- Program name dependence (< 0.1%)
- Program version dependence (< 0.1%)

Test
- Test

W06 2014 vs. W05 2014

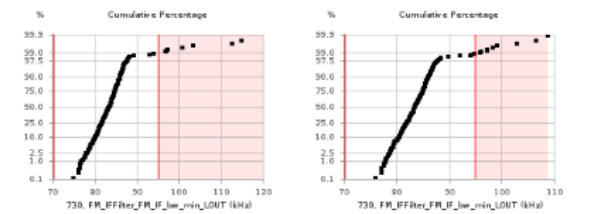
Average yield drop (-2.6%)
Baseline degradation for hbin 15 (+0.6%)
Baseline yield stable

Degradation (up to 0.8%)
- Test (wafers)
- Outlier wafers (0.3%)
- Test limit sensitivity (wafers) (0.8%)
- Clusters (wafers) (up to 0.2%)
- Wide test limits (wafers)

more...

Improvement (up to 0.4%)
- Probe card dependence (up to 0.4%)
- Loadboard dependence (up to 0.3%)
- Tester dependence (up to 0.3%)
- Zonal (up to 0.2%)

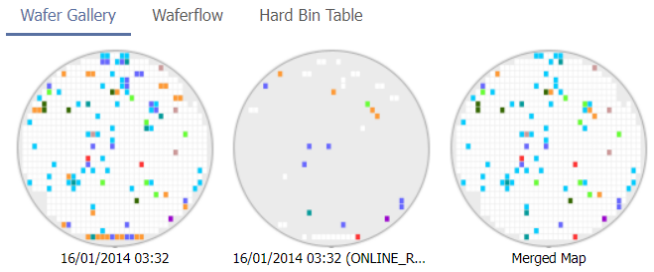
3 wafers: tails on 730, FM_IFFilter_FM_IF_bw_min_LOUT (< 0.1%)

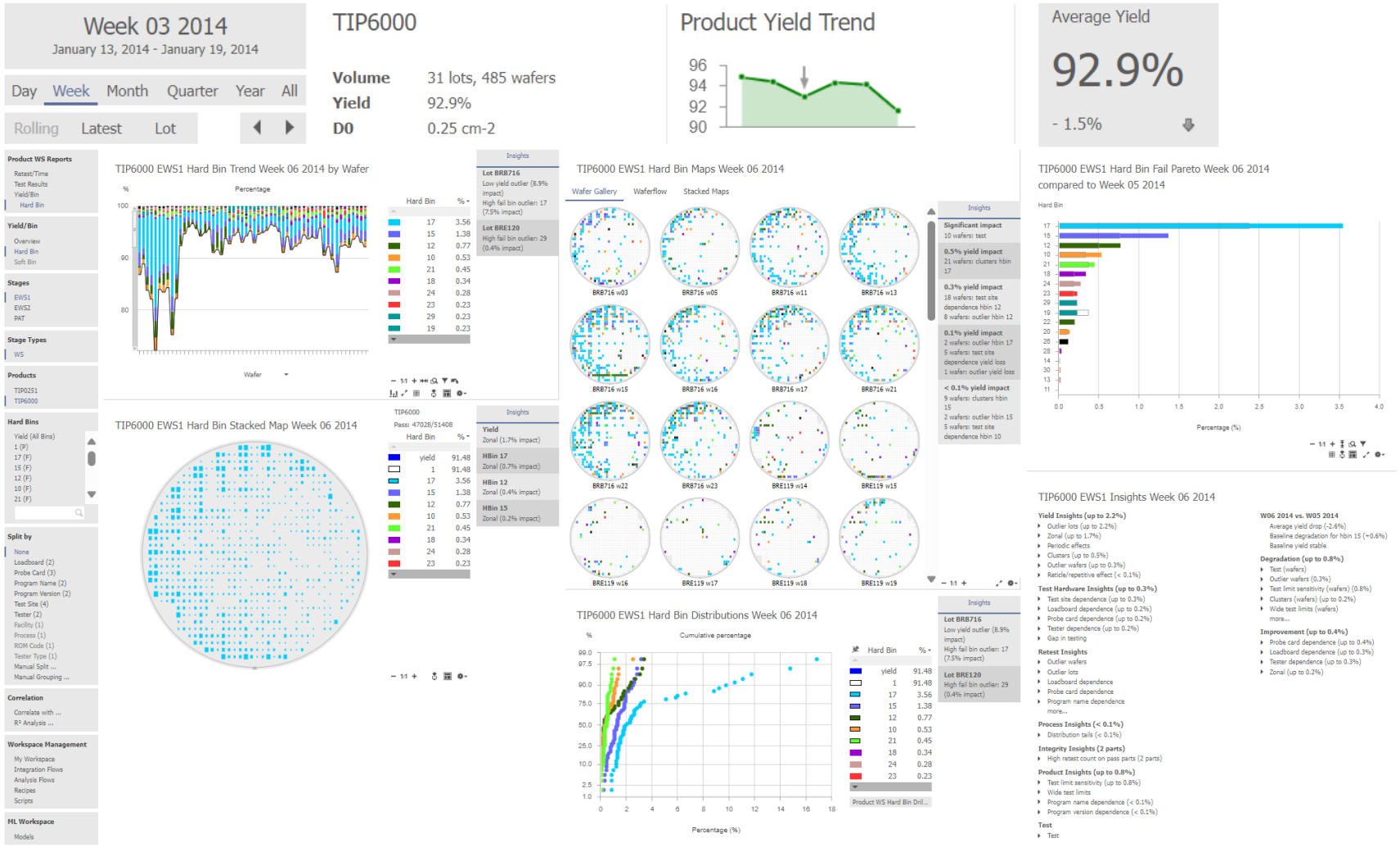


Yield and Bin analysis

Using production test results

- Review hard, soft and custom bin trends and maps and insights
- Navigate between wafer, lot, day, week, month, quarter, year, all scope
- Separate reports available for retests and merged results





Parametric Result analysis

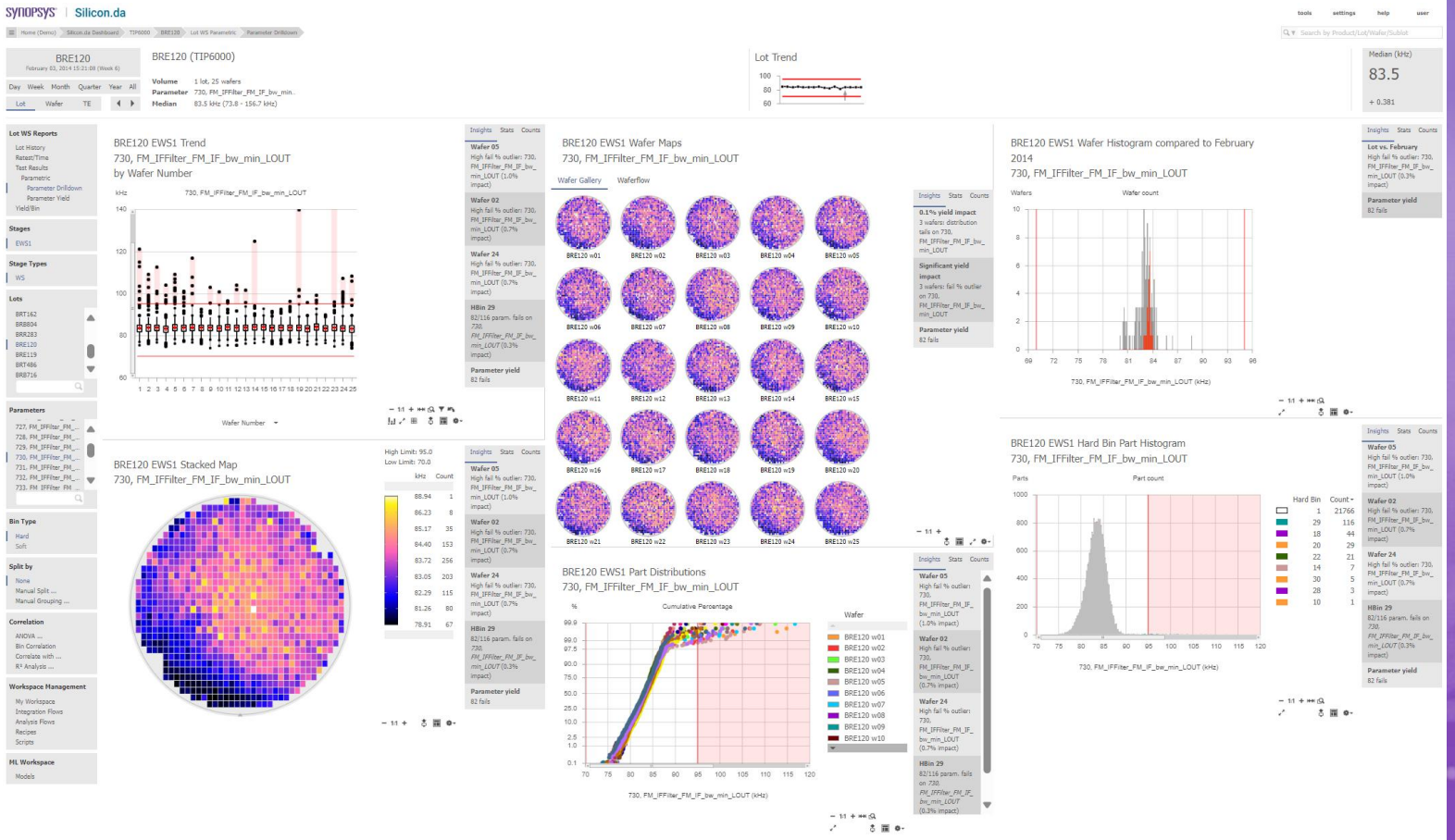
Using production test results

- Review parametric results, statistics, trends, maps and insights
- Review bins associated to each failed test
- Navigate between tests, wafer, lot, day, week, month, quarter, year, all scope
- Sort tables and galleries by typical statistics and Cp Cpk

Parametric Result Drilldown analysis

Using selected production test results

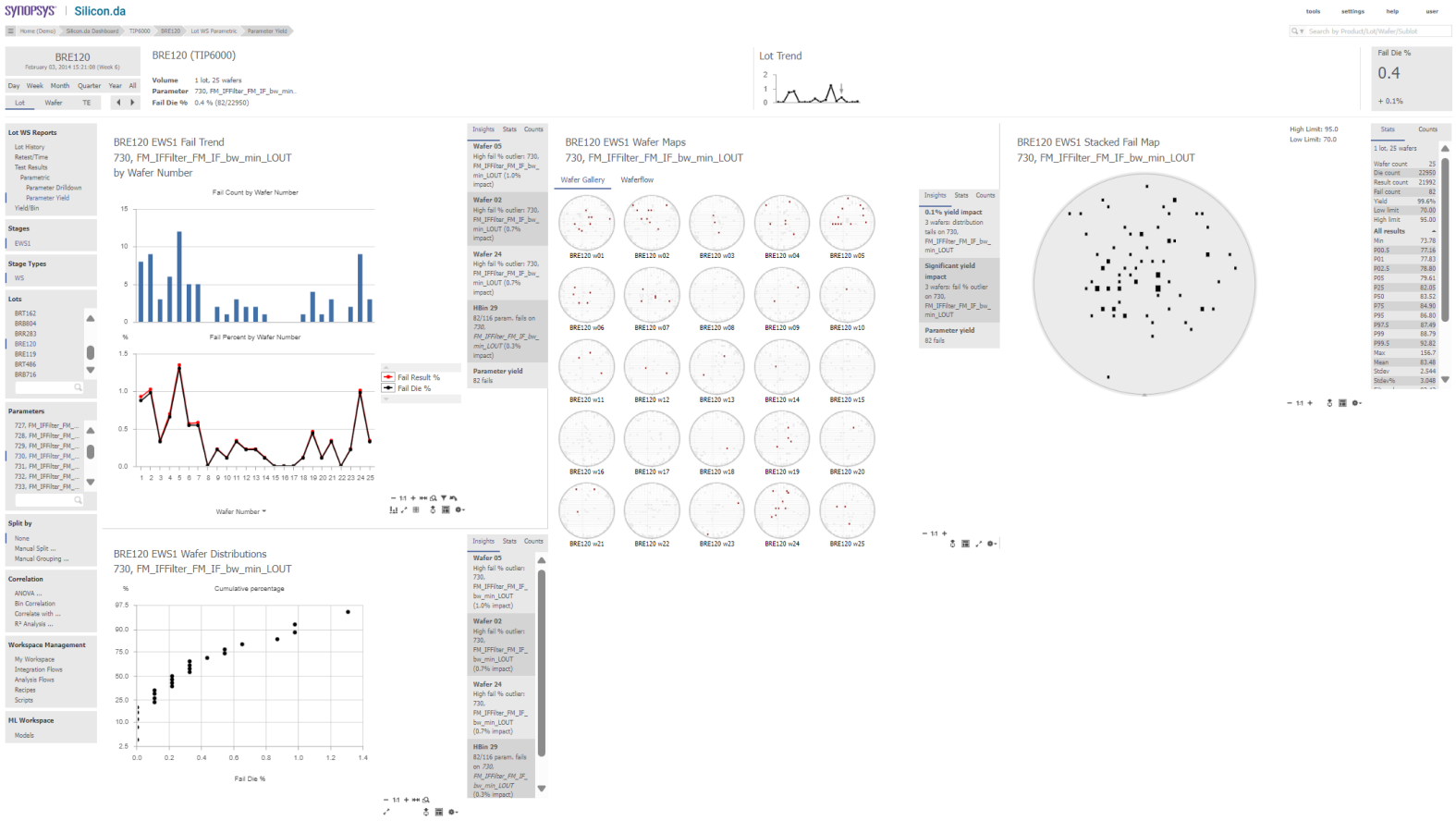
- Review trends, maps, statistics for any selected parameter
- Compare results of current lot / wafer to larger population
- Adjust test limits to evaluate yield impact



Parametric Yield Drilldown analysis

Using selected production test fail results

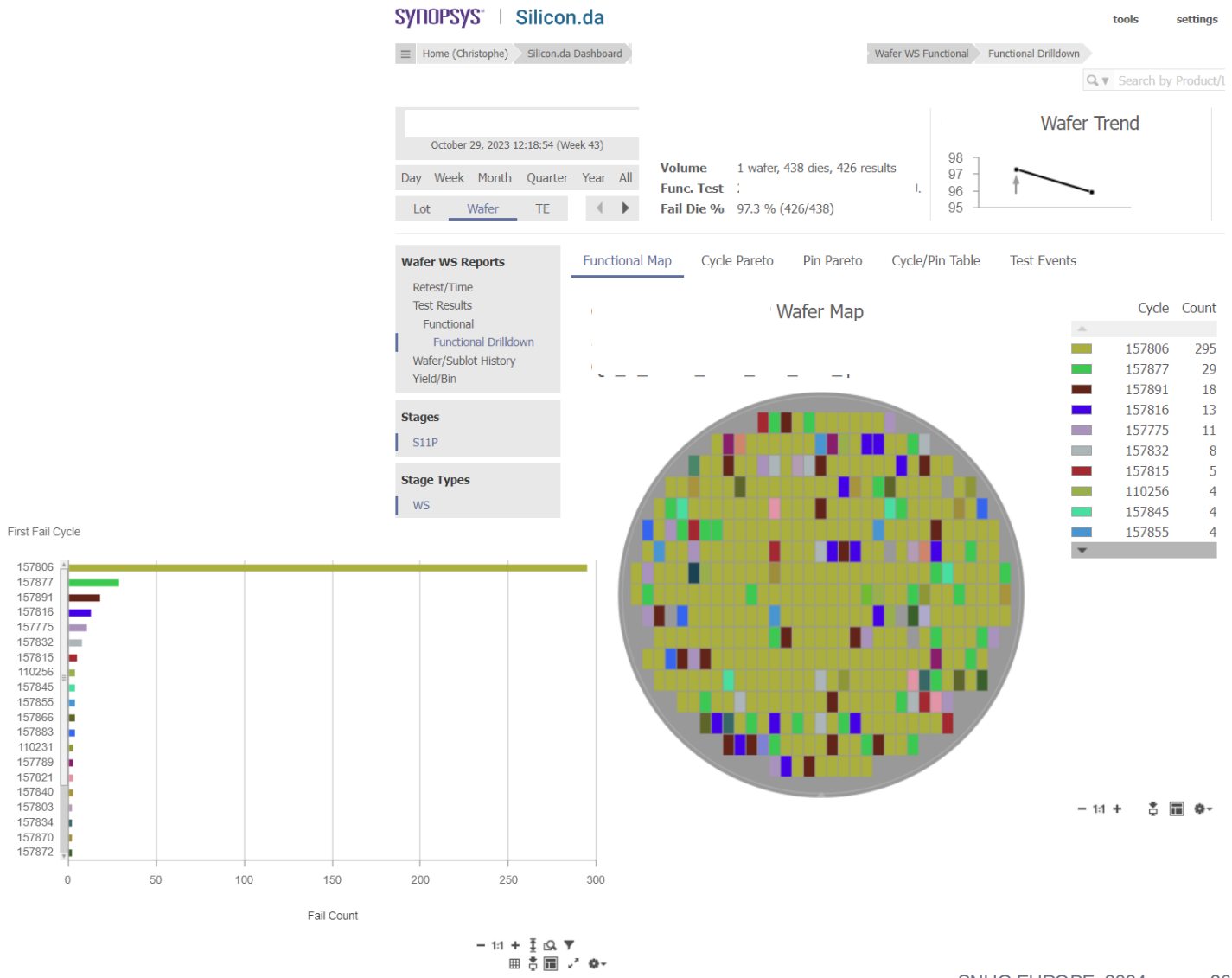
- Review trends, maps, statistics of failures for any selected parameter
- Failures are based on test limits and/or test fail flags
- Limits can be adjusted to estimate impact of changes



Functional Test analysis

Using production test results

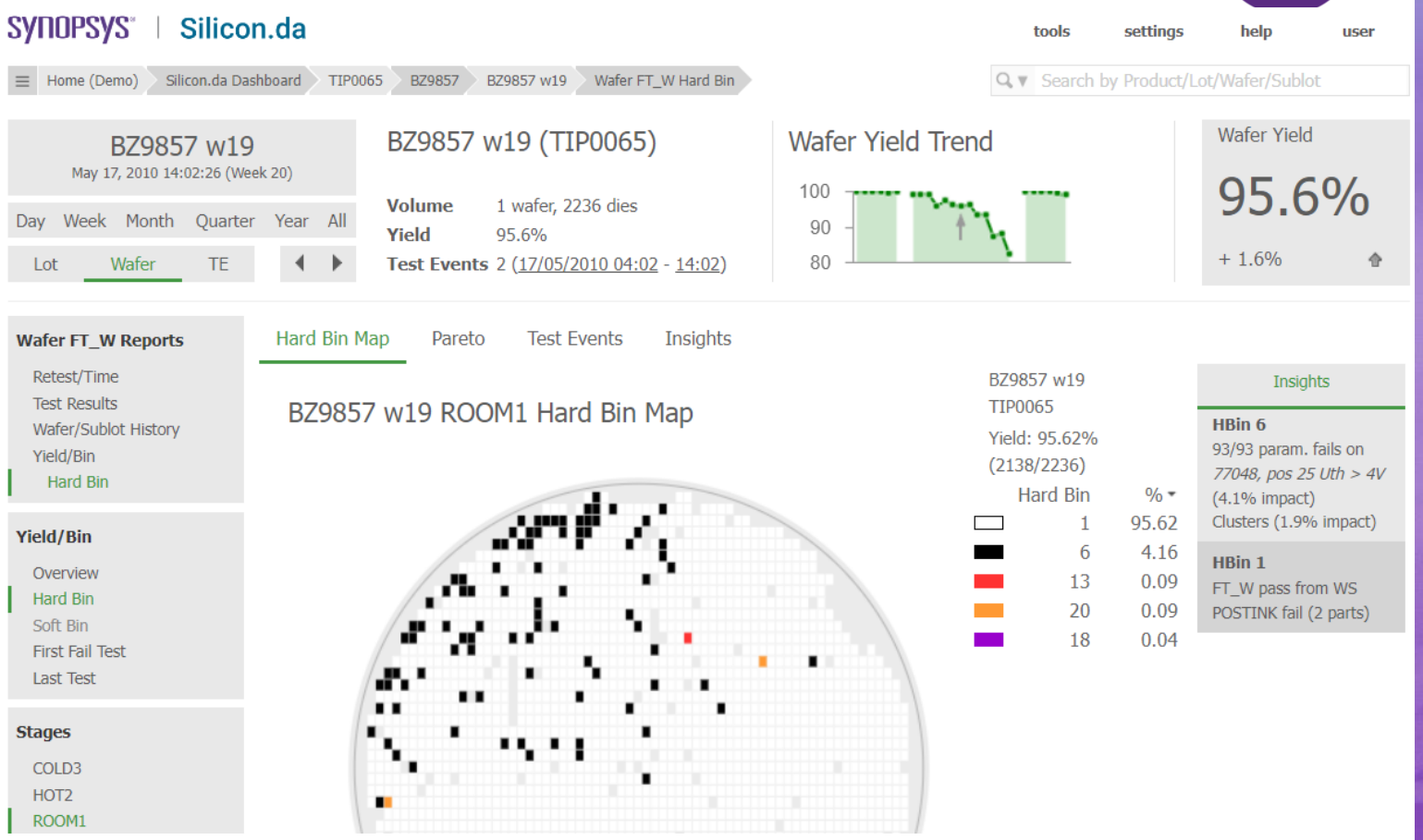
- Review pareto, trends, and maps of failures of tests
- Review pareto and maps of failed cycles and patterns of tests
- Correlate functional fails and parametric test results
- Typically used for ATPG scan, MBIST, Vmin search, etc.



Die Traceability in packages

Using production test results

- Chip ID (ECID, 2DID, etc.) are combined with assembly data to link all test results
- Package test results are viewed as reconstructed wafer maps
- Failed and pass die history is available across all tests
- Multi Chip Modules are recreated as wafers for all included dies



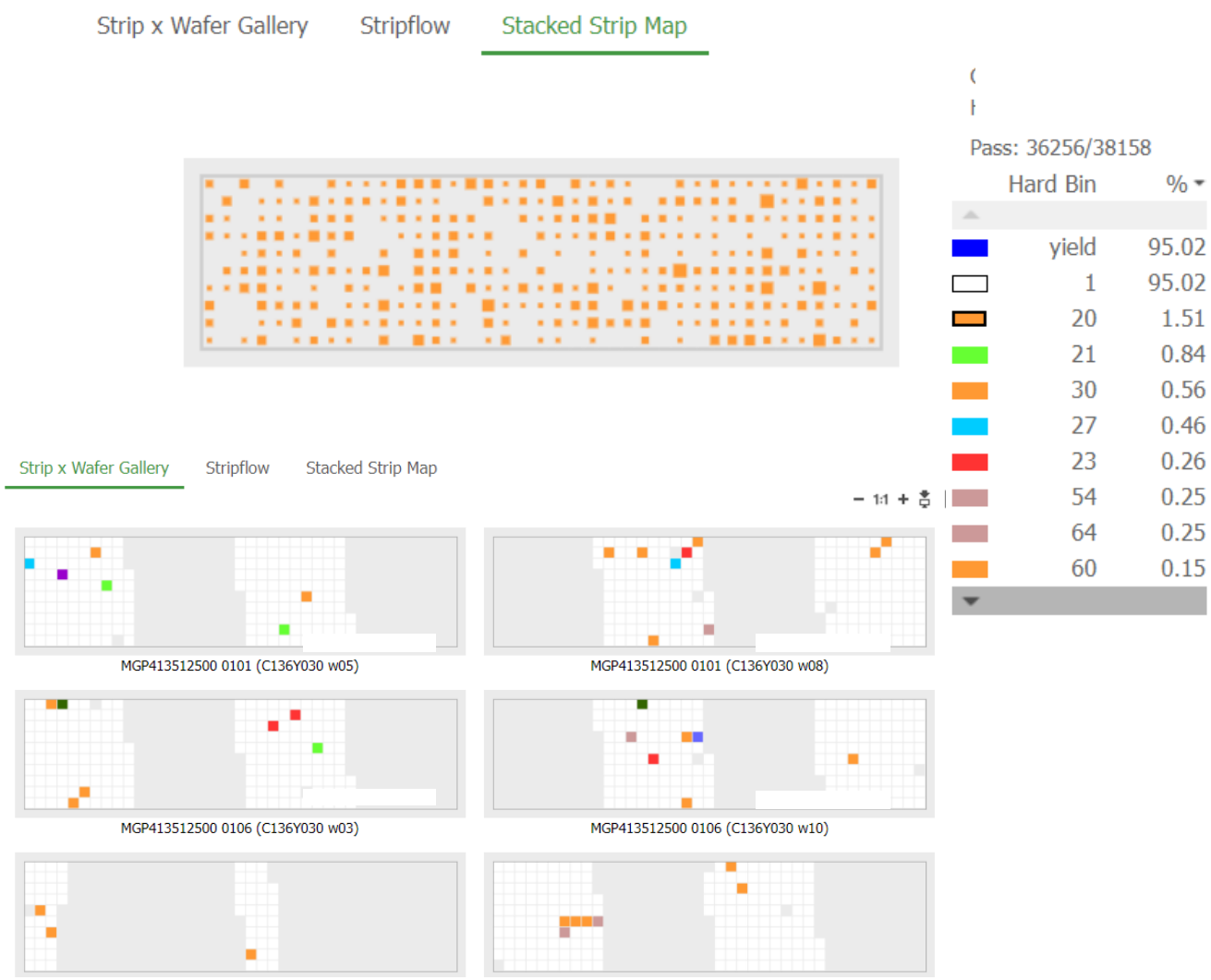
Die History

Lot	Wafer/Sublot	X	Y	Orig.	S	TE Date/Time	Type	Stage	Hard Bin	S	Test Site
BZ9857	BZ9857 w19	28	19	28, 31		30/03/2010 - 18:18:17	WS	HOT1	2		0
BZ9857	BZ9857 w19	28	19	28, 31		14/04/2010 - 17:45:02	WS	POSTINK	1		0
BZ9857	524463104					17/05/2010 - 04:02:18	FT	ROOM1	6		0
BZ9857	BZ9857 w19	28	19	28, 31		17/05/2010 - 04:02:18	FT_W	ROOM1	6		0

Strip analysis from assembly

Using production test results

- Chip ID (ECID, 2DID, etc.) are combined with strip assembly data
- Package test results are viewed as reconstructed strip maps
- Stacked strip maps can show dominant fail bin problems
- Individual strip maps can show assembly problems



Gage Reliability and Reproduceability

Using production test results

- Compare test measurements and identify test instability or quality problems
- Applies for wafer-to-wafer and packaged parts

Gage R&R Statistics - ANOVA (Crossed)
80001, vddshort_400mV_TM:VDDIO_33@VDDIO_33[1]

Two-Way ANOVA Table With Interaction

Source	DF	SS	MS	F	P
Part	982.0	8.89e-4	9.05e-7	1.01	0.428
Split	0.0	0.0	0.0	0.0	1.00
Part*Split	0.0	0.0	0.0	0.0	1.00
Repeatability	1966.0	0.00176	8.97e-7		
Total	2948.0	0.00265			

Two-Way ANOVA Table Without Interaction

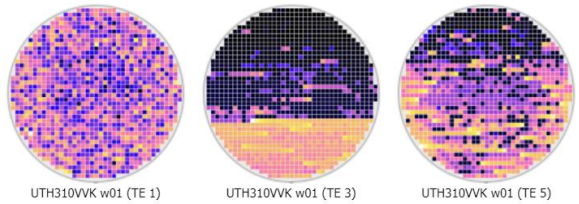
Gage R&R With Interaction

Source	VarComp	%VarComp	StdDev	Study Var (6*SD)	SV/Tolerance (%)	%Study Var
Total Gage R&R	8.97e-7	74.83	9.47e-4	0.00568	63.15	86.50
Repeatability	8.97e-7	74.83	9.47e-4	0.00568	63.15	86.50
Reproducibility	0.0	0.00	0.0	0.0	0.00	0.00
Split	0.0	0.00	0.0	0.0	0.00	0.00
Part*Split	0.0	0.00	0.0	0.0	0.00	0.00
Part-To-Part	3.02e-7	25.17	5.49e-4	0.00330	36.62	50.17
Total Variation	1.20e-6	100.00	0.00110	0.00657	73.00	100.00

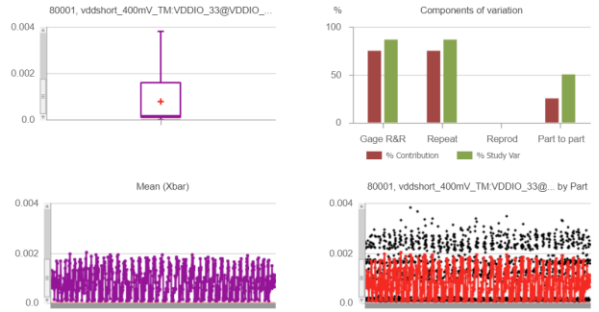
Number of distinct categories: 0

Gage R&R Test Events - ANOVA (Crossed)
80001, vddshort_400mV_TM:VDDIO_33@VDDIO_33[1]

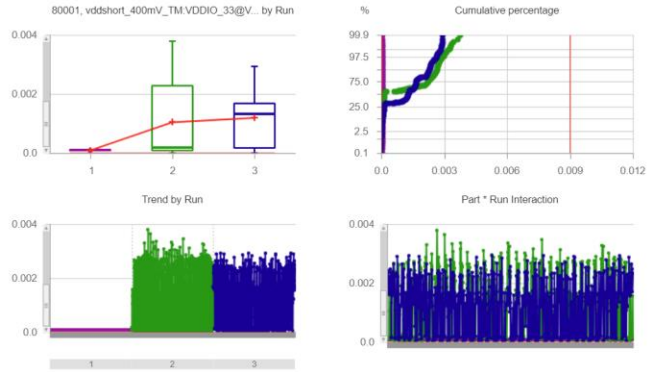
Gallery Waferflow



Gage R&R Charts - ANOVA (Crossed)
80001, vddshort_400mV_TM:VDDIO_33@VDDIO_33[1]



Per Run Charts - ANOVA (Crossed)
80001, vddshort_400mV_TM:VDDIO_33@VDDIO_33[1]



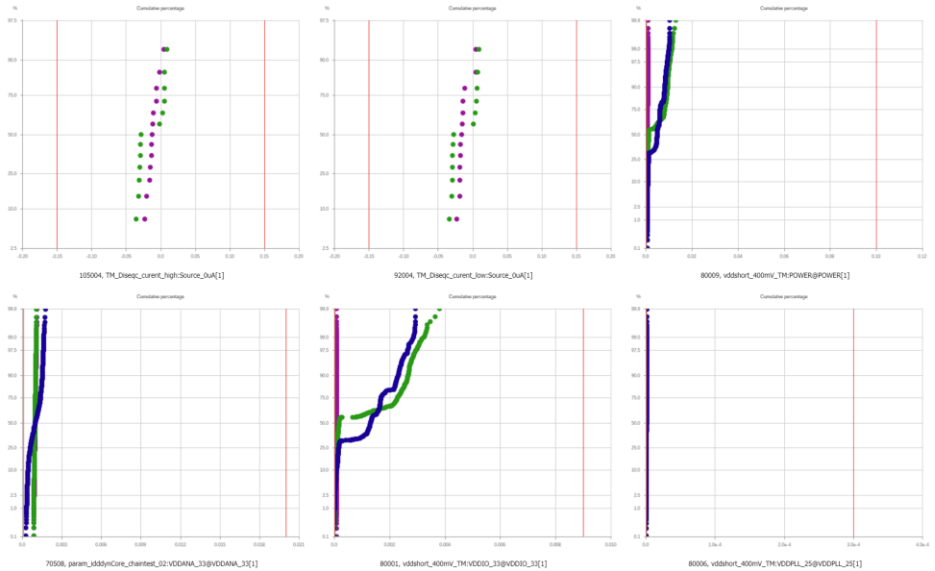
Gage R&R Analysis - ANOVA (Crossed)

Filters:
Repeat. (EV) not is missing

Showing 1-50 of 153 Page 1 of 4 Show 50 Items

Parametric test		%Study var		Dist. cat.	%Tol (6 * stdev / tolerance)				Matrix		
Test name	Unit	Gage R&R	Part-Part		Reprod. (AV)	Repeat. (EV)	Total R&R	Part-Part	Parts	Splits	Runs
vddshort_400mV_TM:VDDL...		99.89	4.59	0	0	1.30	1.30	0.06	970	1	3
vddshort_400mV_TM:VDDA...		98.18	18.97	0	0	1.12	1.12	0.22	967	1	3
param_iddq_chaintest:VDDI...		97.96	20.07	0	0	11.73	11.73	2.40	960	1	3
TM_video_dac_dynamic_HD...		95.04	31.11	0	0	4.67	4.67	1.53	14	1	2
TM_audio_dac_dyn_sin_LH:...		94.99	31.25	0	0	39.07	39.07	12.85	14	1	2
TM_video_dac_dynamic_SD...											
TM_video_dac_dynamic_SD...											
TM_video_dac_dynamic_SD...											
TM_video_dac_dynamic_HD...											
param_iddq_chaintest:POW...											
M_video_dac_dynamic_HD...											
M_video_dac_dynamic_HD...											
aram_idddynCore_chaintes...											
M_video_dac_dynamic_HD...											

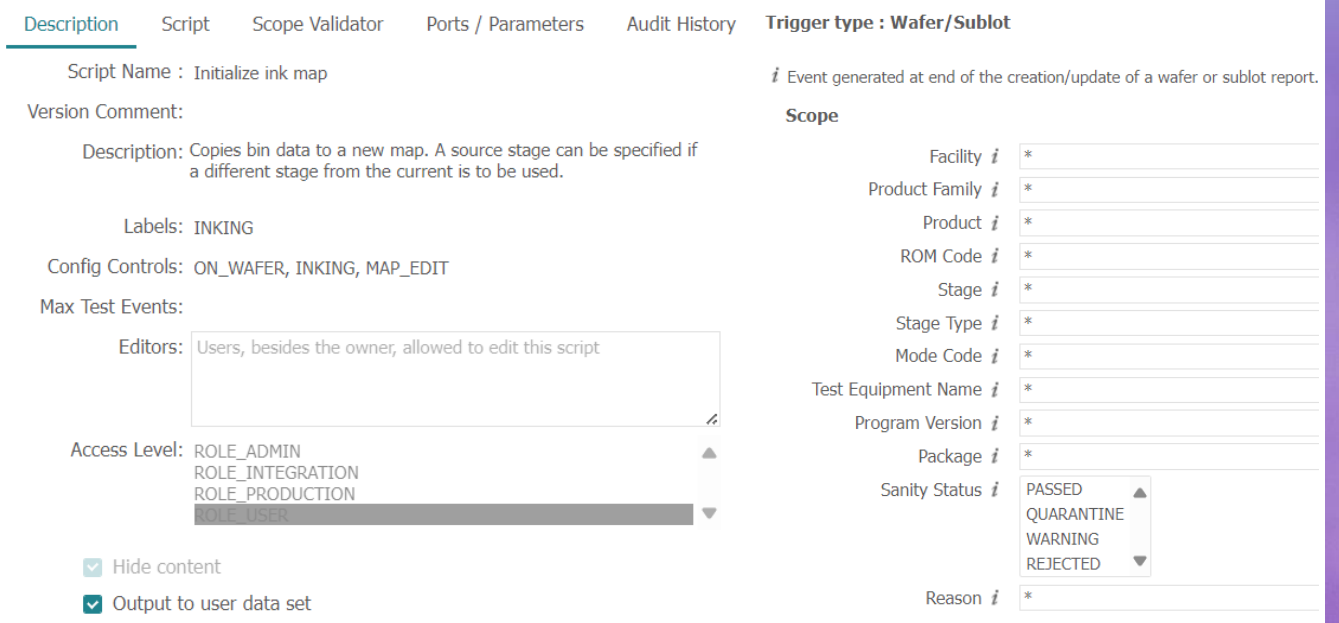
Gage R&R Distributions - ANOVA (Crossed)

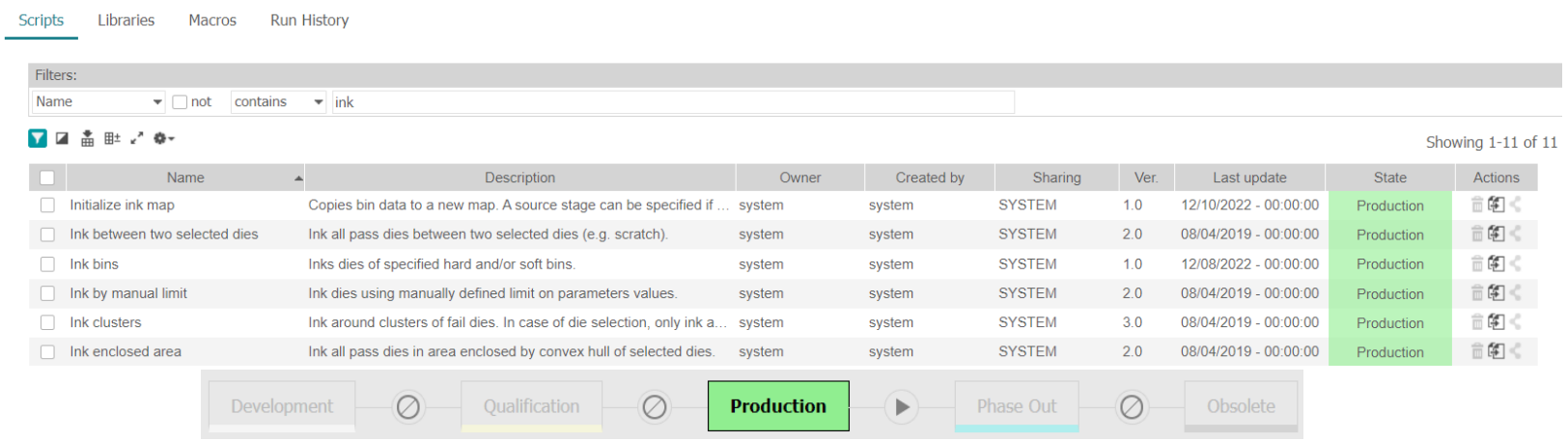


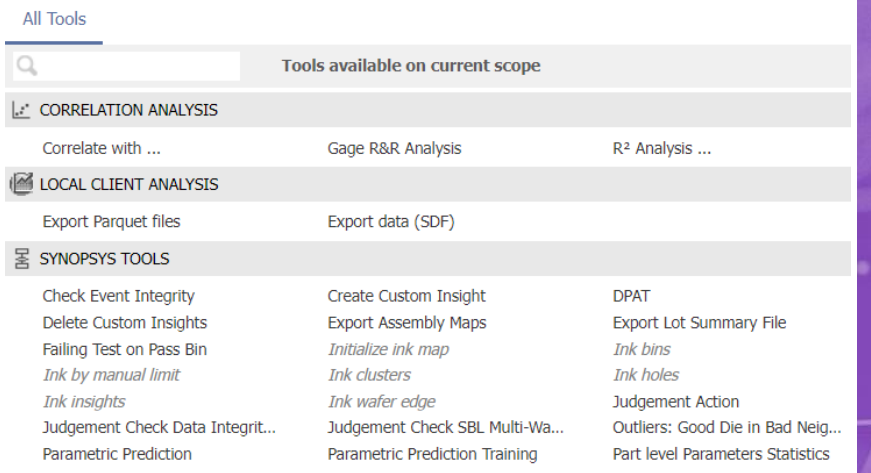
Scripts and recipes

Automation for the cloud system

- Use predefined system scripts, or build your own scripts using JS
- Scripts are version controlled
- Use recipes to schedule or trigger the scripts based on any type of event
- Run from a list of applicable tools



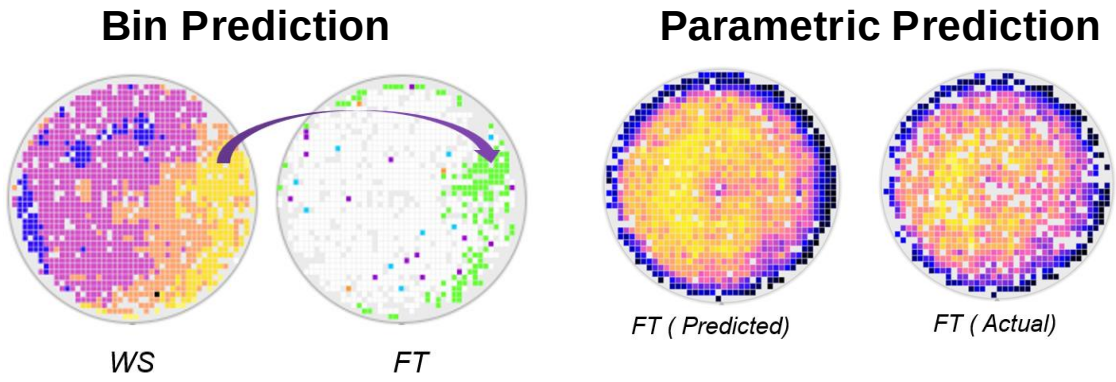


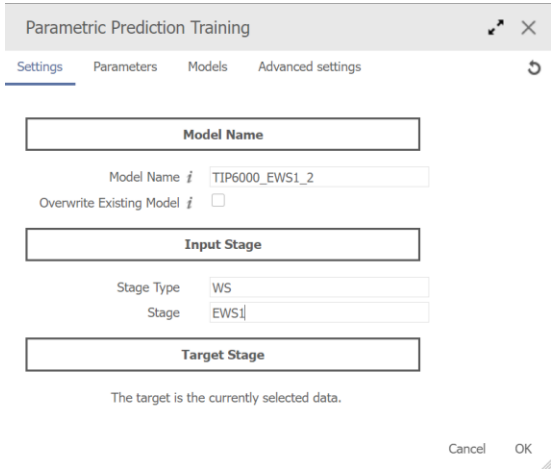


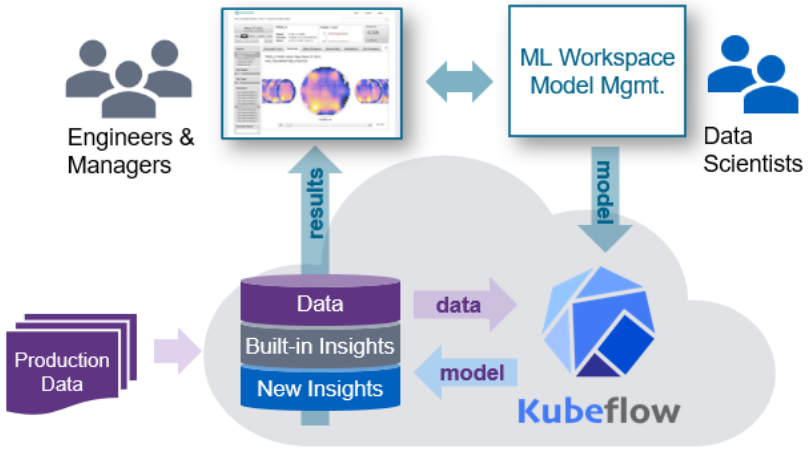
Machine Learning

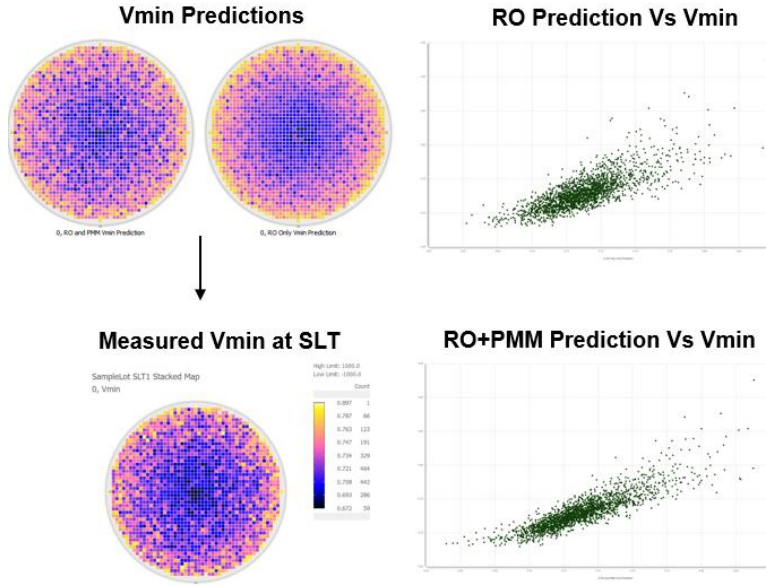
Using production test results

- Train and use predefined ML apps
  - Predict Parametric result at any future test stage from wafer sort results
  - Predict Yield and Bin at any future test stage from wafer sort results
  - Predict Vmin at SLT from monitor results
- Develop custom ML apps







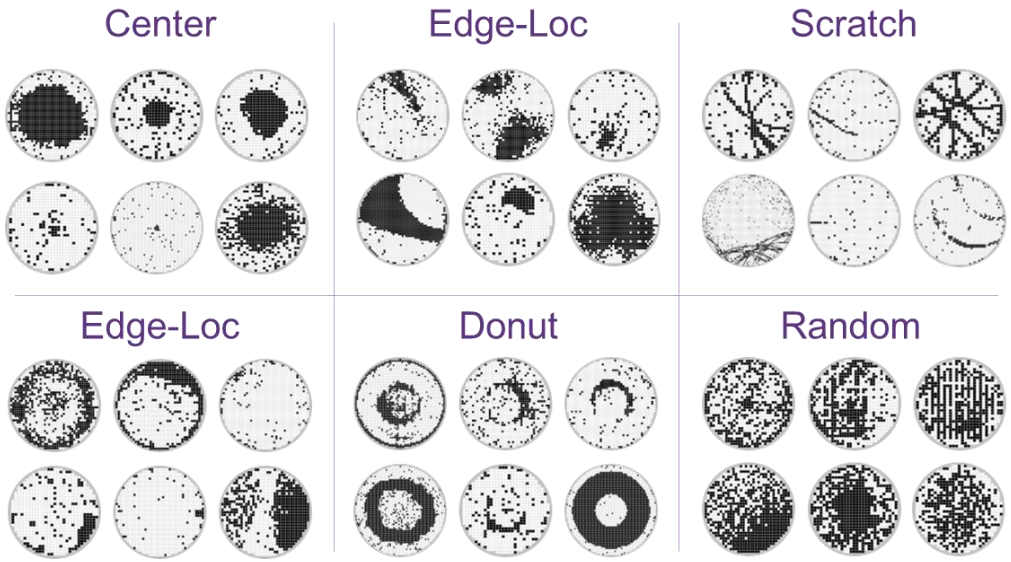


Spatial Patterns and Inking

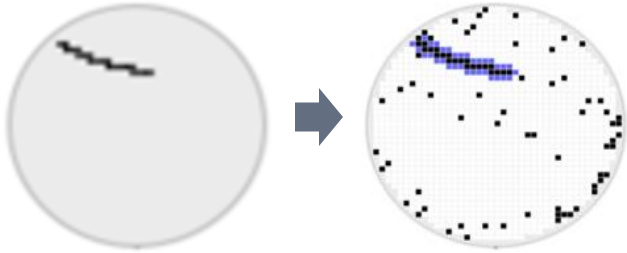
Using production bin results

- Spatial wafer pattern classification for typical patterns
- Scratch detection for multiple types of scratches
- Cluster and Good Die Bad Neighbor (GDBN) detection
- Automated inking for the die around problem areas to improve reliability

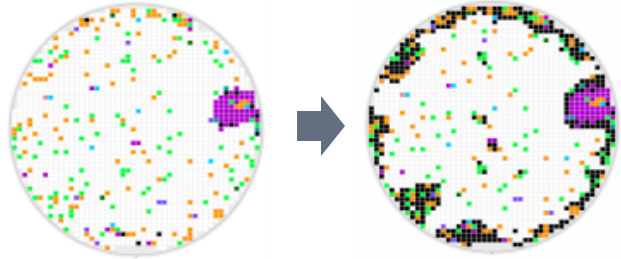
Pattern Classification



Scratch Detection and Inking



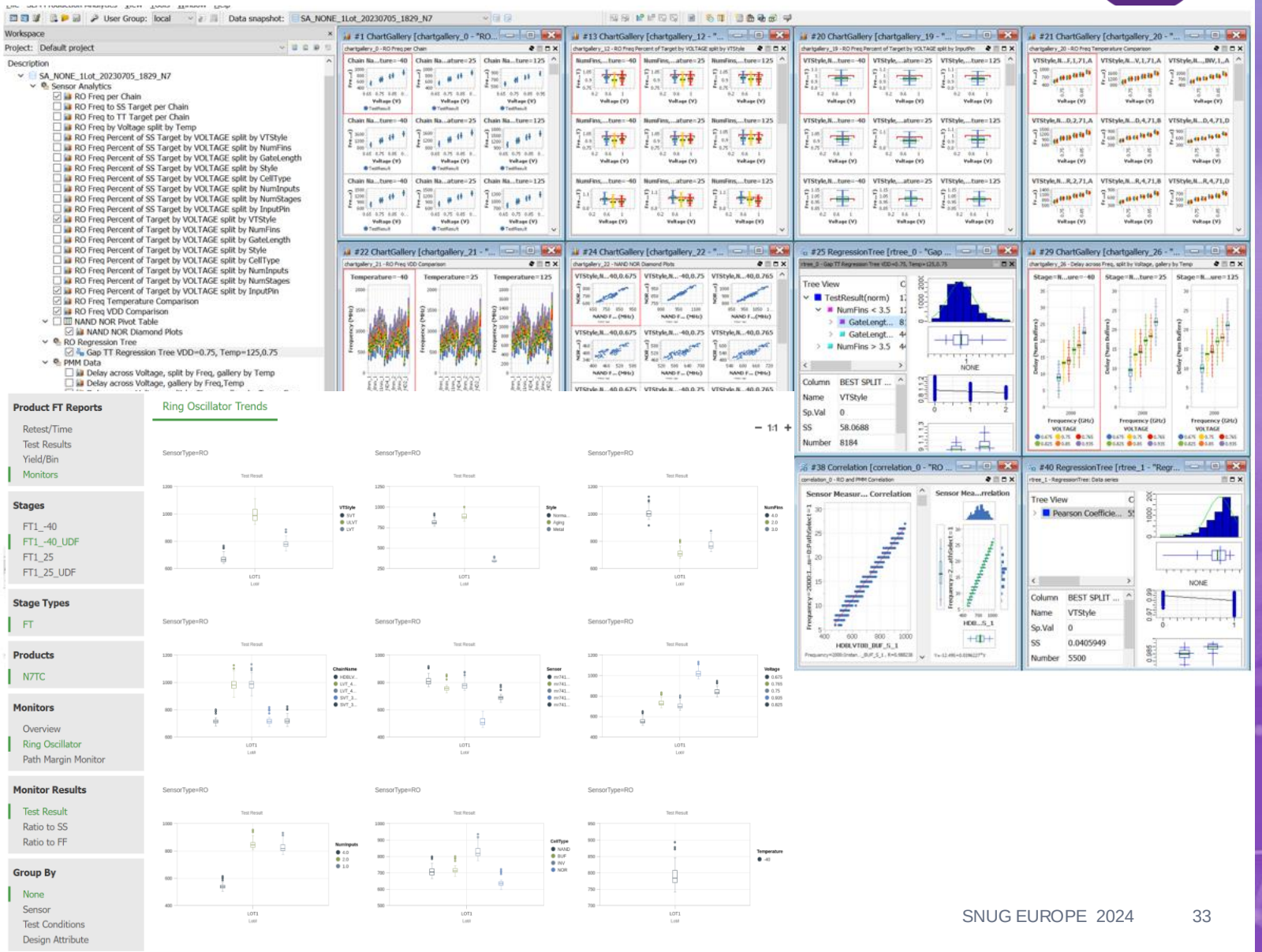
Clusters and Inking



Monitor Analytics

Using embedded monitors

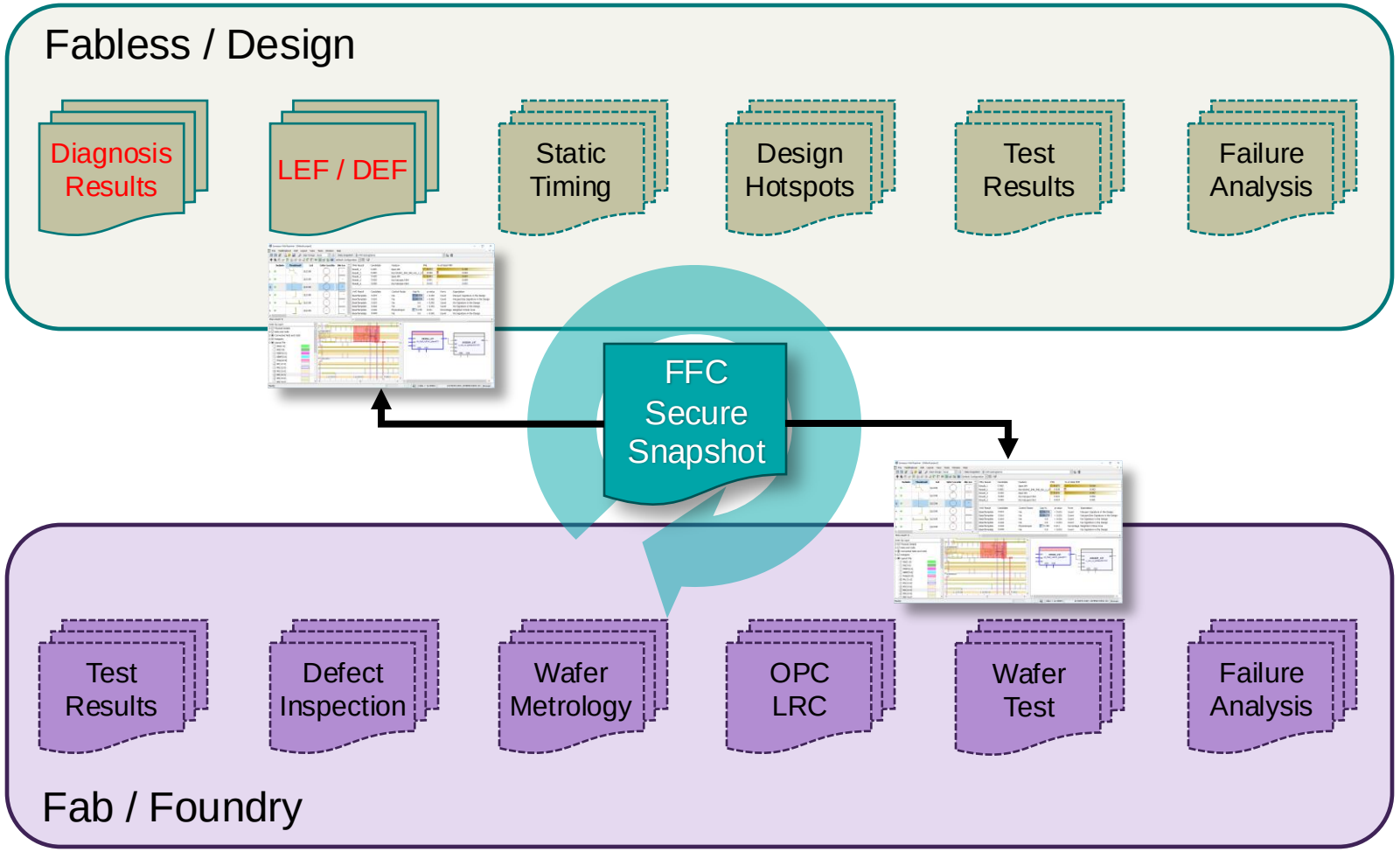
- Synopsys SLM IP and 3rd party monitors are embedded inside chips, including Voltage, Temperature, Ring Oscillator, Path delay, Clock delay, etc.
- Test results at multiple test conditions identifies process, design, simulation, and reliability problems
- Performance and reliability of chips is monitored through whole product lifecycle
- Local and web apps available



Fab Fabless Collaboration

Using manufacturing and diagnosis results

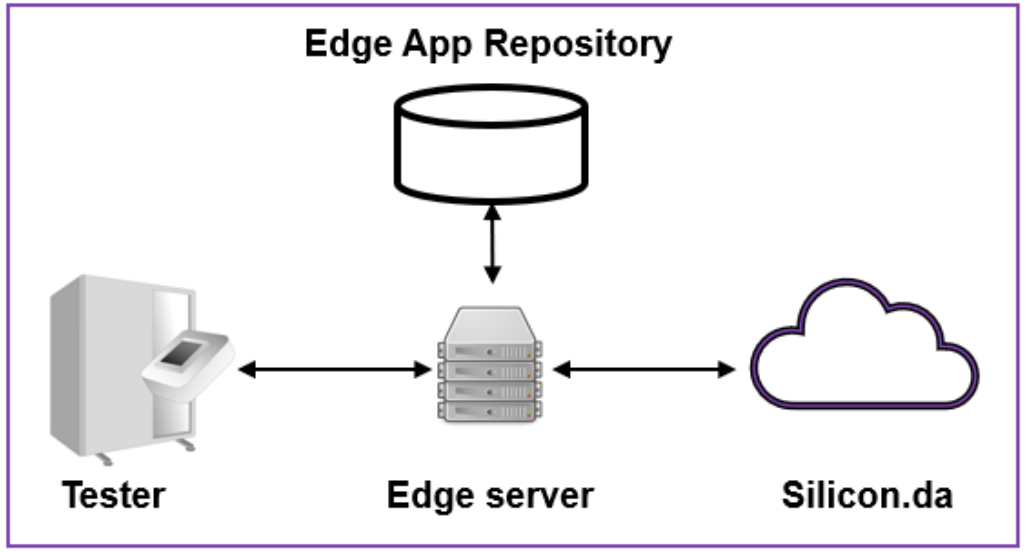
- FFC flow allows to securely share diagnosis results between Fabless/Design and Fab/Foundry
- Design data is protected
- Automated for each wafer
- Each partner sends only what they want to share
- Each partner can continue the analysis with their local data, and share again if needed
- Currently used by all major foundries (with Yield Explorer)

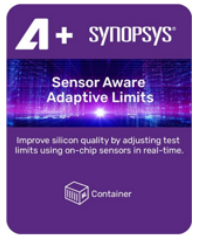


Tester Edge Applications

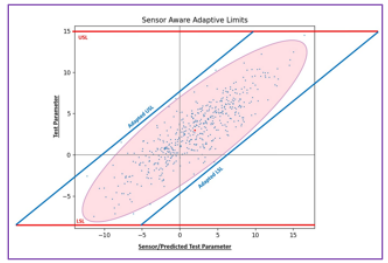
Using production test results on test floor

- Synopsys provides Silicon.da applications for the Advantest ACS Edge platforms
- The applications connect to the Silicon.da system (local or cloud)
- Further collaborations planned with other tester companies

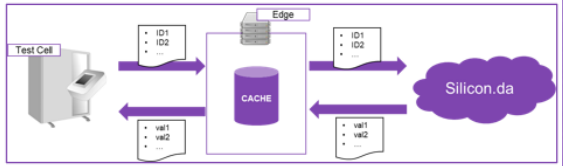


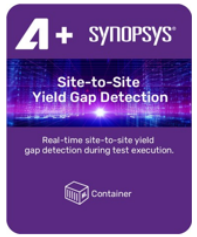


"Improve silicon quality by adjusting test limits using on-chip sensors in real-time"

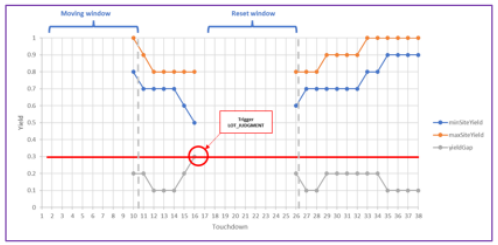


"Link between test floor and Silicon.da cloud system using traceability functions"





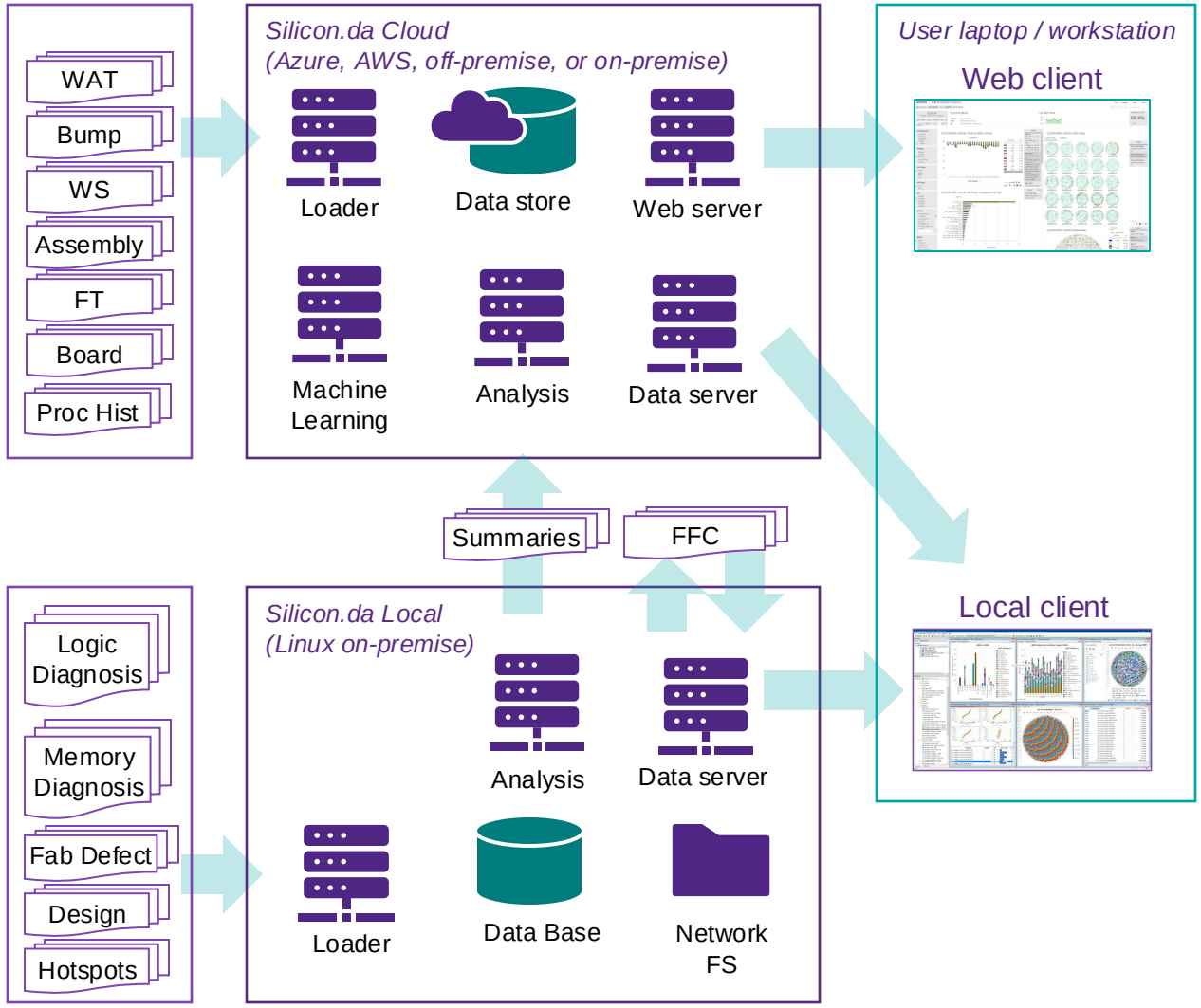
"Detection of yield gap during testing across sites"



Silicon.da Summary

Engineering and production data analytics

- A complete solution for Yield ramp
- Analytics for design-centric diagnosis, test program results, packaging and fab data
- Web and local client applications, with machine learning and built-in applications
- Scalable from a few wafers to millions
- Secure data exchange with foundries




THANK YOU
Our Technology, Your Innovation™