# Multiphysics Integrity

## over Physical Implementation Cycles

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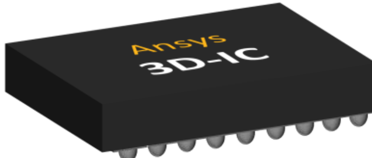
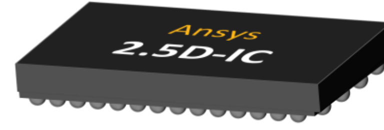
Ansys

# From Multiple Physics to Multiphysics

## Coupling between Physics

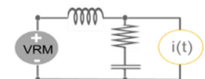


**Signal** Integrity

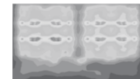
Interconnects
vs. High-Speed Performance

**Power** Integrity



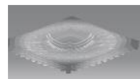
Power Delivery Network
vs. Performance

**Thermal** Integrity

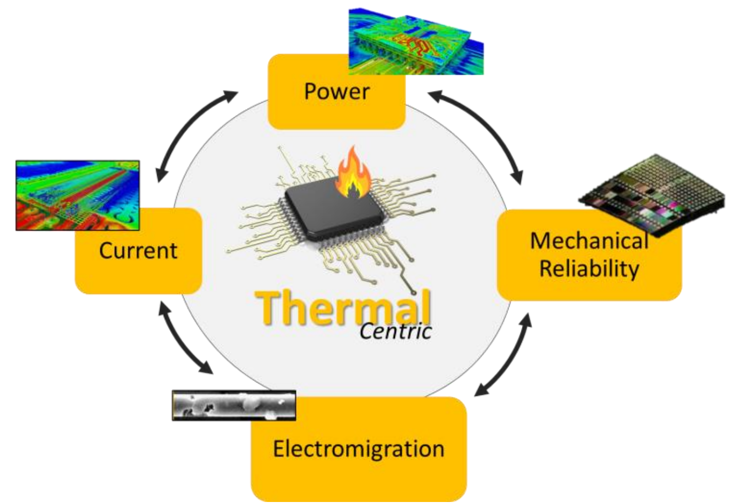


Power / Heat Dissipation
vs. Reliability

**Mechanical** Integrity

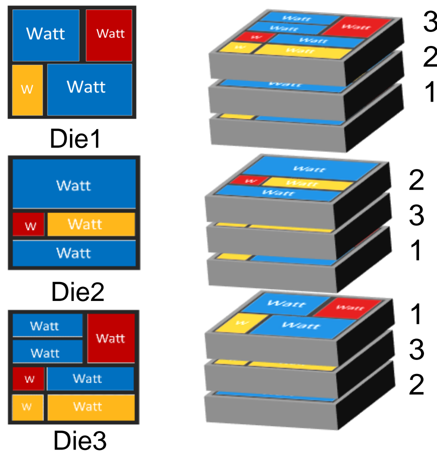


Fatigue / Warpage
vs. Reliability

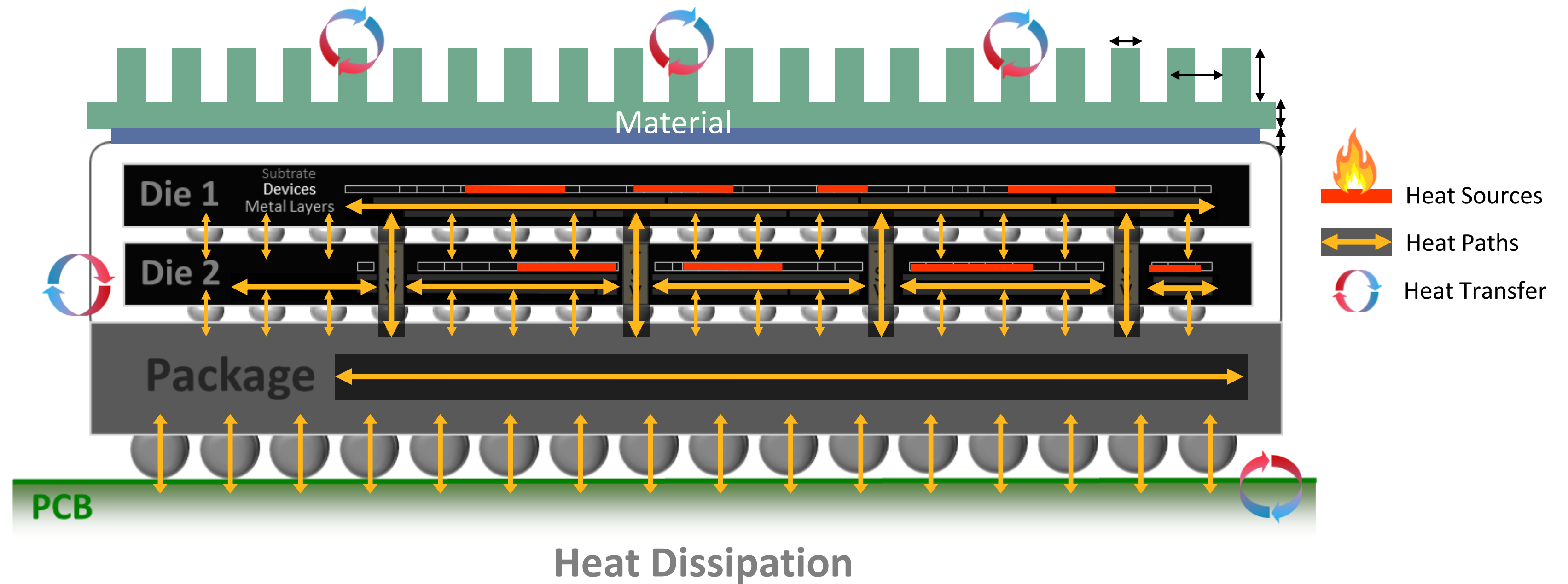


# Why so hot?

## More than T°




3DIC Power Stack-Up




Heat Dissipation

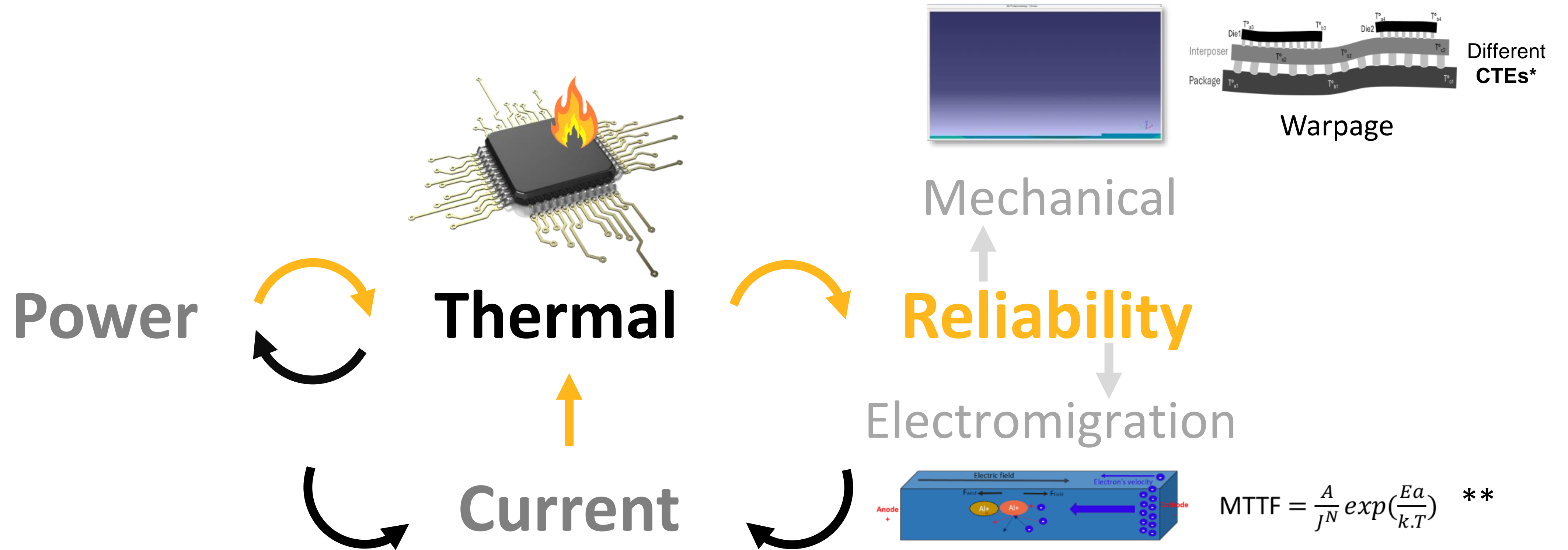
**Heat Dissipation** (conduction, coupling, transfer) relies on many design parameters

**Temperatures** and **Gradients** impact performances (power, frequences) and reliability (lifetime, warpage, fatigue)

Need to simulate, to understand and to validate **Thermal Integrity**, from **pre-Layout** to **SignOff**

# Thermal Integrity?

## Definition and scope of analysis




* Coefficient of thermal expansion

** Black's equation, Mean Time To Failure function of: J = Current Density, Ea = Activation Energy, R = Boltzmann's constant, T = Kelvin temperature

# Multi-die Integrity & Reliability Solution

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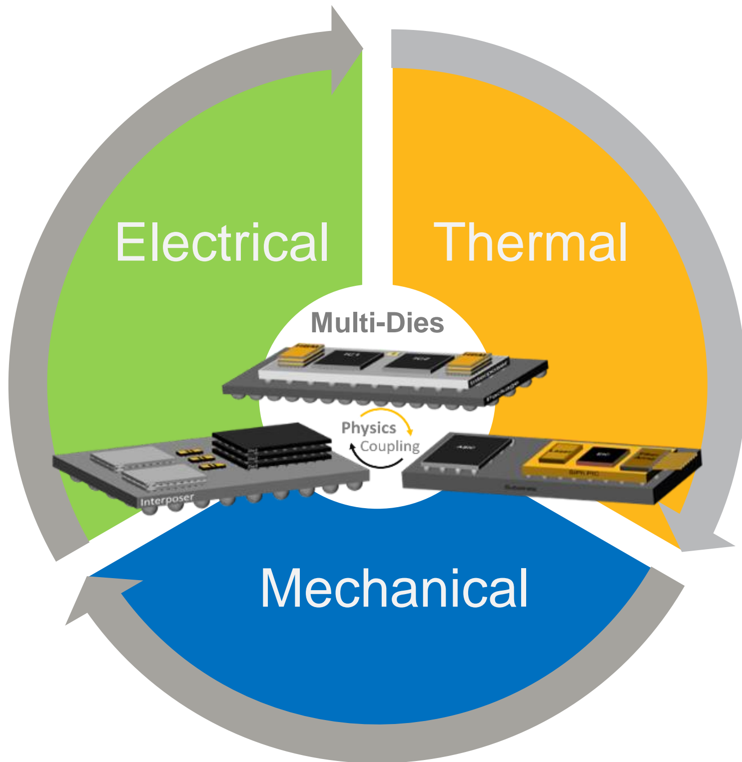
## RedHawk-SC Electrothermal, single purpose build platform

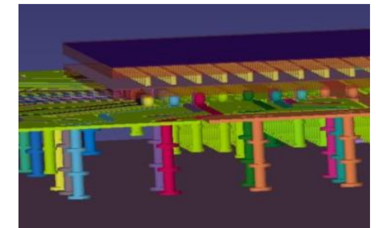



### Multiphysics simulation platform for Multi-Die Chiplets

**1. Multi-die Setup**
- ✓ Assembly of chip-package-system
- ✓ Advanced 3D-IC packaging with million+ connections
- ✓ Provide configuration for die level EMIR (/RedHawk-SC, /Totem-SC) and ESD (/Pathfinder-SC)

**2.Thermal/Structural integrity**
- ✓ Static/Transient Thermal Analysis
- ✓ Static/Transient Electrothermal Analysis
- ✓ Thermal-induced Stress-strain analysis
- ✓ Multiphysics electro-thermal-mechanical analysis

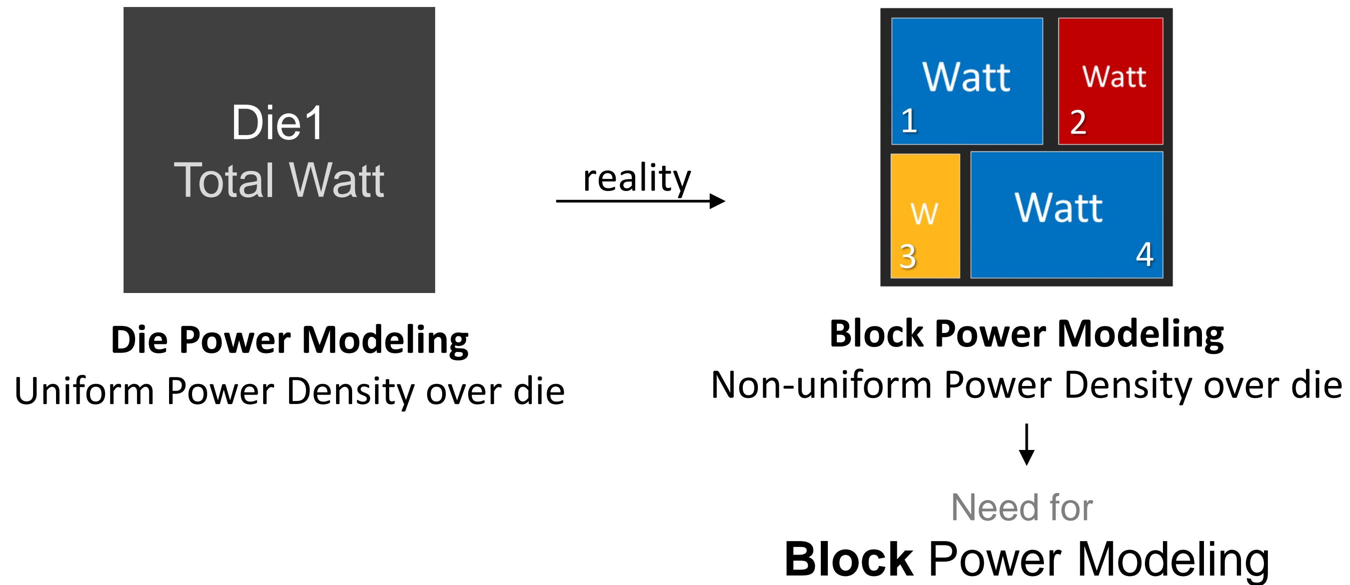
**3. Signal/Power integrity**
- ✓ Interposer/Package/PCB extraction and co-simulation
- ✓ Chip Model Analyzer
- ✓ High-speed signal integrity analysis with power-noise impacts


Assembly-Model-Simulation

*It is about bringing Thermal (/Icepak) & Structural (/Mechanical) expertise to the chip designers, for* ***Pre-Layout*** *to* ***Signoff*** *Analysis*

# Die Thermal Modeling

From expected to final implemented power density



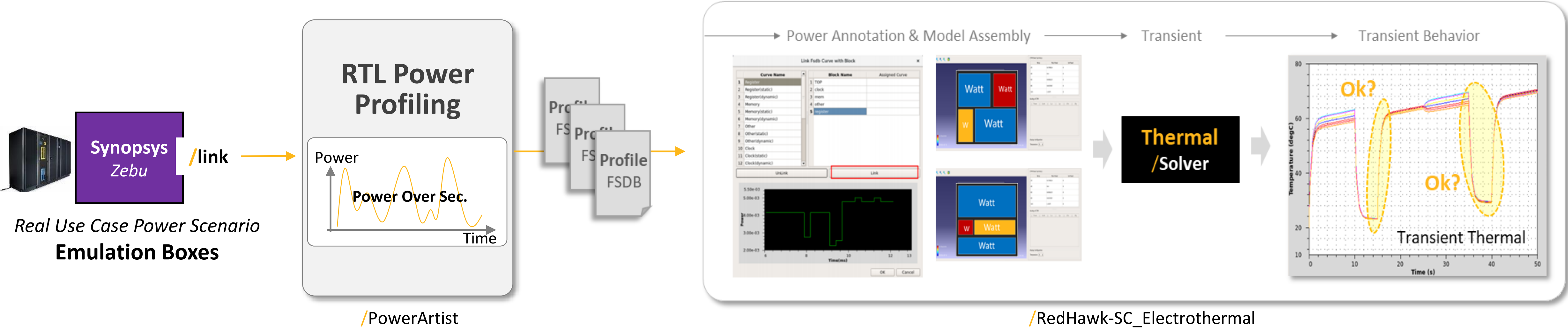

**Die Power Modeling**
Uniform Power Density over die

**Block Power Modeling**
Non-uniform Power Density over die

Need for
**Block** Power Modeling

# Block Level Modeling Application 1/2

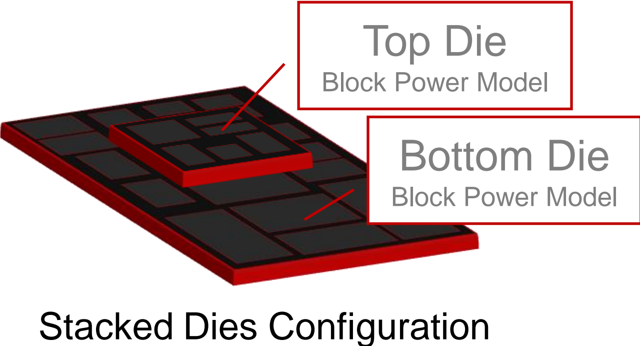
## Transient Power-Thermal Management use case simulation



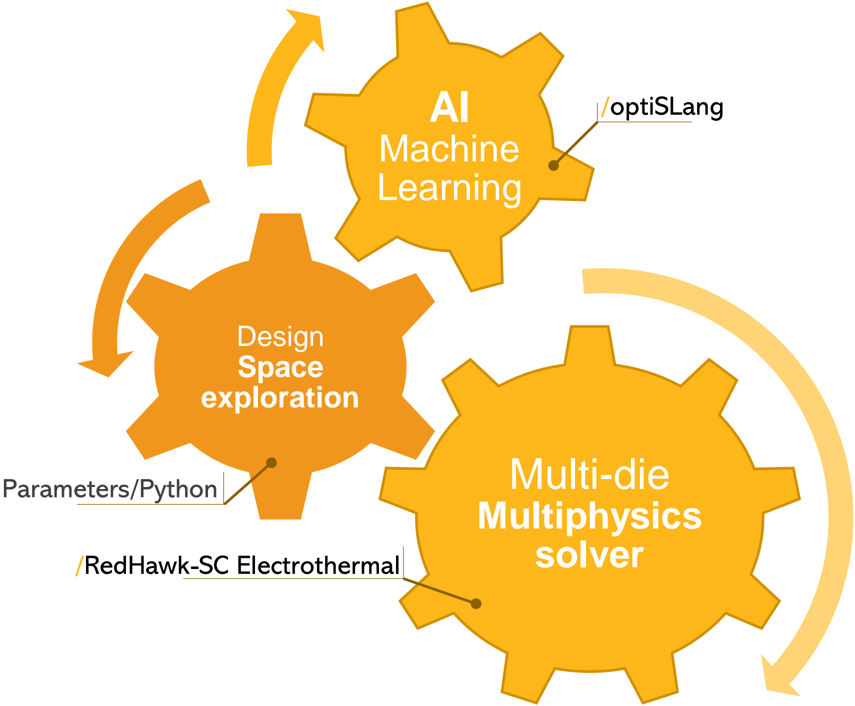

**Thermal-Aware** transient Power Management & Optimization

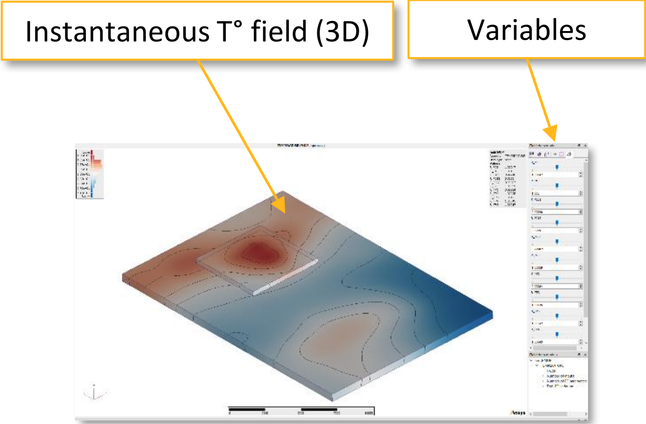
# Block Level Modeling Application 2/2

## Thermal Field Metamodeling for interactive Power-Thermal exploration




Stacked Dies Configuration




Power-Thermal Management interactive exploration

Multi-Die Power Assembly

Building Thermal Training data

Thermal Field Metamodel

# Die Thermal Modeling

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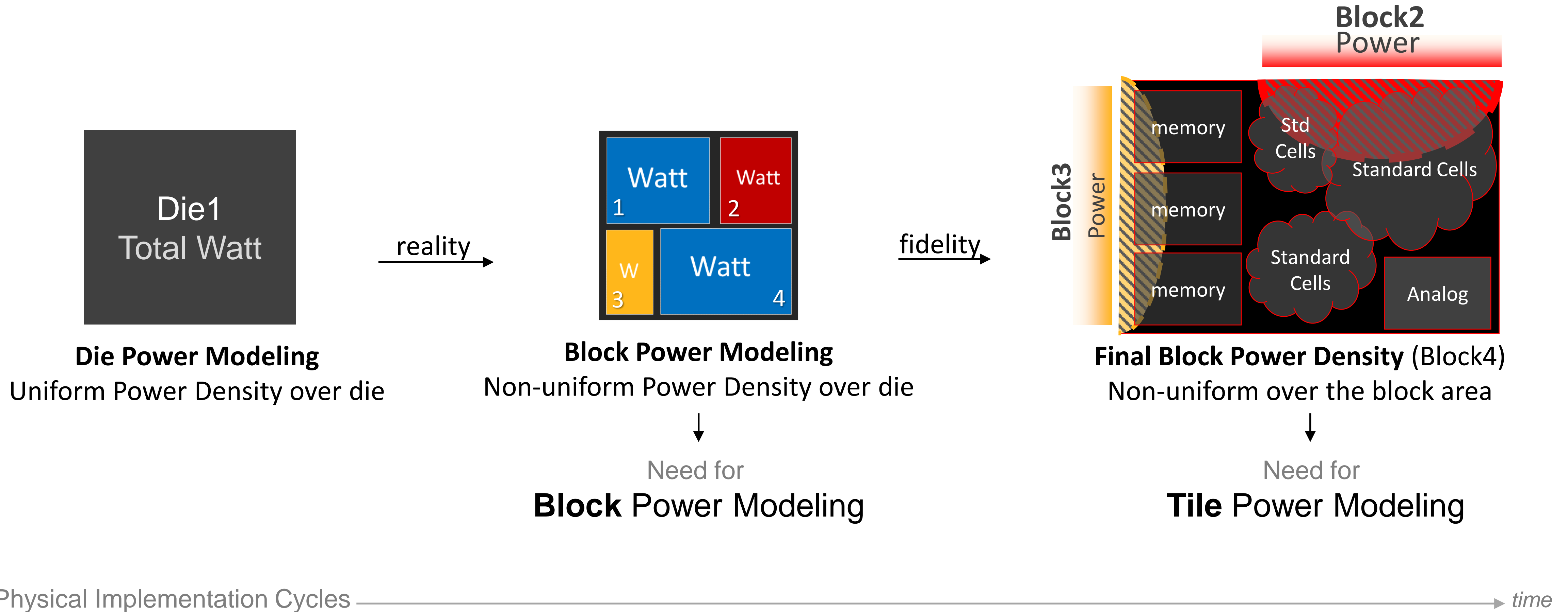
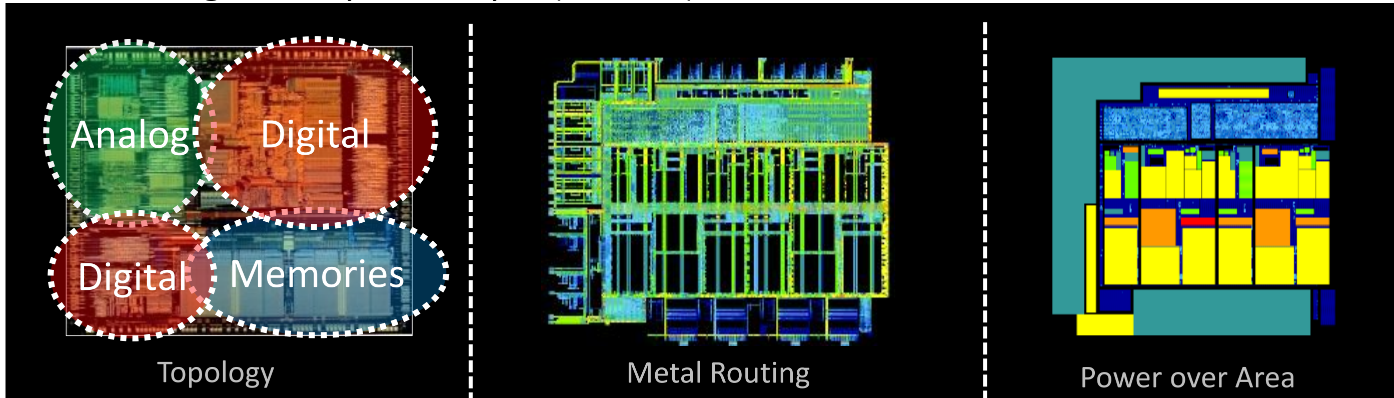
## From expected to final implemented power density



# Chip Thermal Model (CTM)

## High Fidelity Die Modeling

**Die Modeling** from Layout Analysis (LEF/DEF)




/RedHawk-SC

### Tile-Based Die Modeling

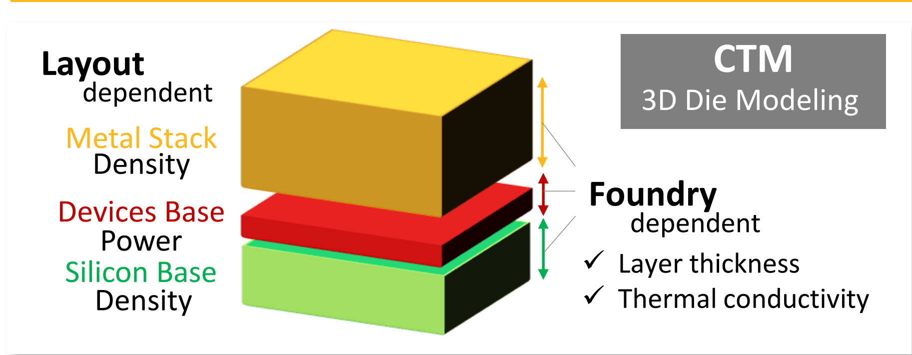
- ✓ T° aware Power Density
- ✓ Metal Density Modeling

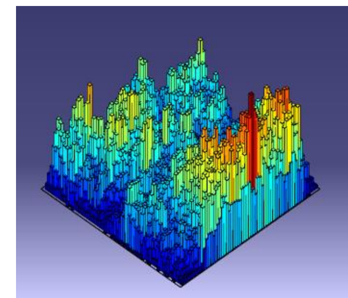
Power
T°

*Model supported within:*

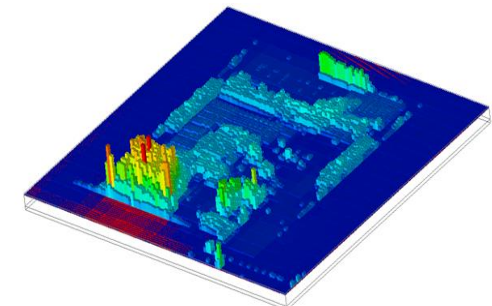
- ✓ /RedHawk-SC Electrothermal
- ✓ /Icepak

Support **encrypted technology** files from foundry



CTM - Metal density

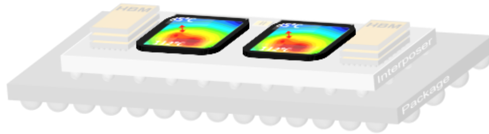


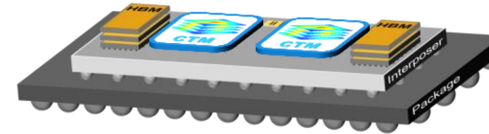
CTM – Heat flux map

# Die Reliability Signoff

## Thermal aware Electromigration analysis

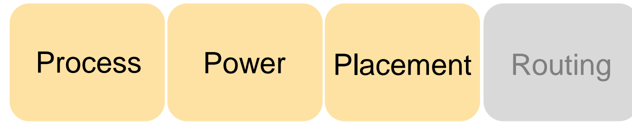
**Dies Level**
/RedHawk-SC

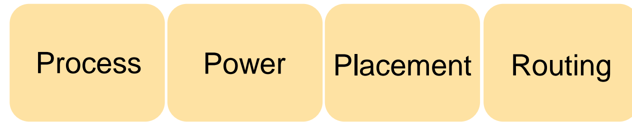




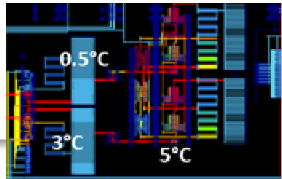
**Multi-Die Level**
/RedHawk-SC Electrothermal

P&R cycles

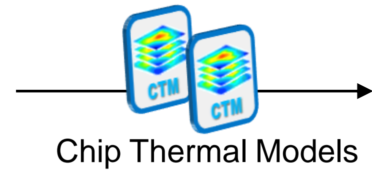


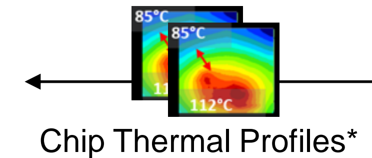

Self Heat Analysis



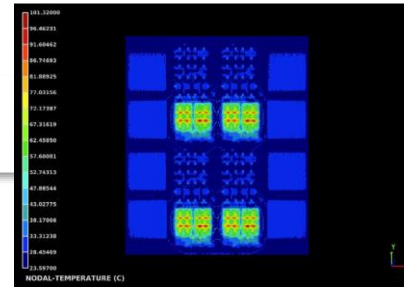

$T°_{Final} = T°_j + \Delta T°$




Chip Thermal Models




Chip Thermal Profiles*



Multi-Die Thermal Analysis

✓ High fidelity Thermal Analysis

✓ Thermal-aware Electromigration Signoff
*with /Totem-SC for Analog Layouts*

* Temperature Profile ($T°_j$) = Per-layer per-Tile Temperature

# 3DIC Compiler

## Thermal Integrity from the physical implementation platform

**3DIC Compiler Platform**

**RedHawk-SC Electrothermal Platform**

| Power Integrity | Thermal Integrity | Signal Integrity |
| --- | --- | --- |
| **Hierarchical EM/IR** w. Chip Power Model Reduced Order Model | **Thermal Analysis** Conducted heat Die-to-die coupling | **Multi-Domain Analysis** Time, Frequency |
| **Thermal-aware EM/IR** | **Electro-Thermal** Self Heating Joule heating, melting | **Signal Transmission** Reflections, crosstalk, impedance mismatches |
| **Electrostatic Discharge Analysis (ESD)** | **Thermal Stress** Stress, Warpage | **Unexpected coupling** Signal-to-PG, Die-to-Die TSV-To-TSV |

Physics Coupling

Physics Coupling

VRM

i(t)

**Synopsys 3DIC Compiler ↔ Ansys RedHawk-SC Electrothermal**

**3DIC Compiler**

NDM

Top-level

settings

Synopsys

<3dic_shell>

analyze_3d_thermal

Load Thermal Results

Thermal Maps

**RedHawk-SC Electrothermal**

- Extract Data from NDM
- Setup 3DIC Analysis
- Run Thermal Analysis
- Collect 3DIC Thermal Results

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**Productivity, Accuracy & Convergence** over the physical implementation cycles of the Multi-die system

# Thermal Integrity Optimization

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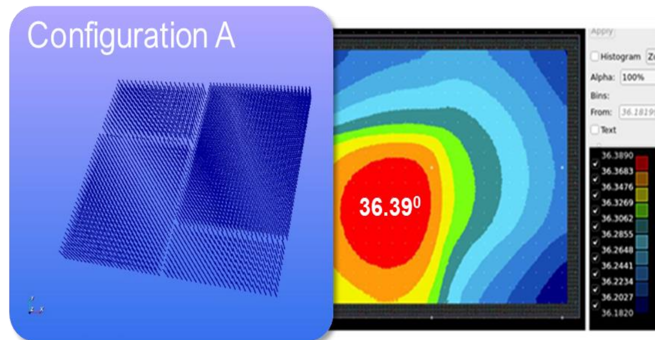
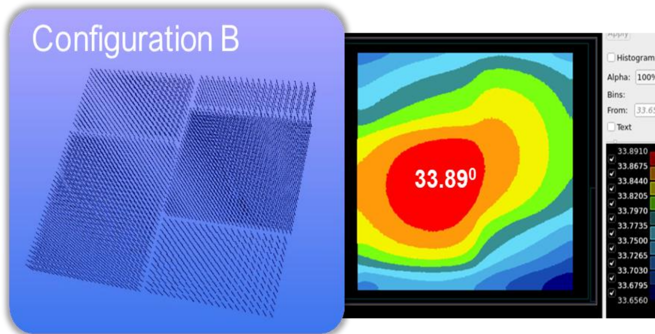
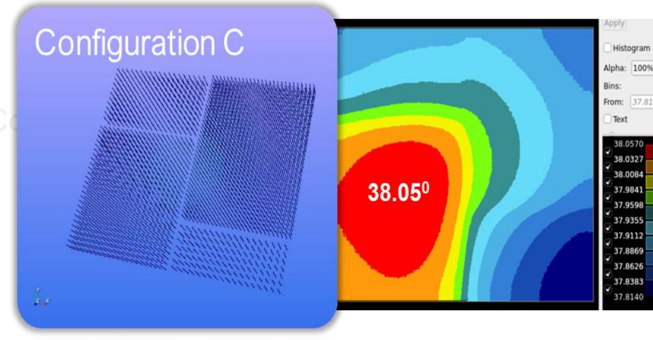
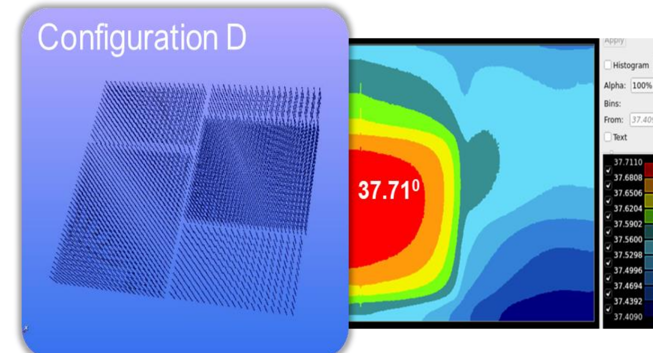
Synopsys 3DIC Compiler & Ansys RedHawk-SC Electrothermal




**Thermal Floorplanning optimization**

- 4x Different TSV Floorplan strategies
- 4x Different Thermal behavior

✓ Configuration B gives the best thermal results
- 12% difference in max peak temperatures
- Superior isotherm distribution across the whole die

Thermal Assessment of TSV Floorplan in **< 2 Hours**

# Thermal Integrity over Design Stages

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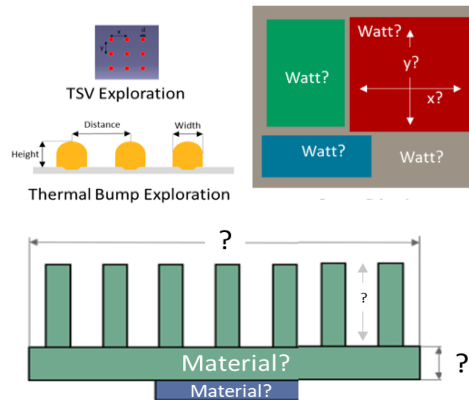
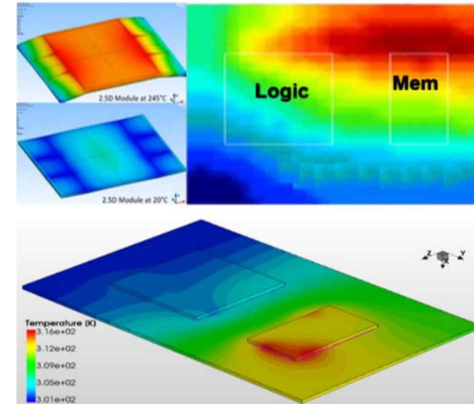
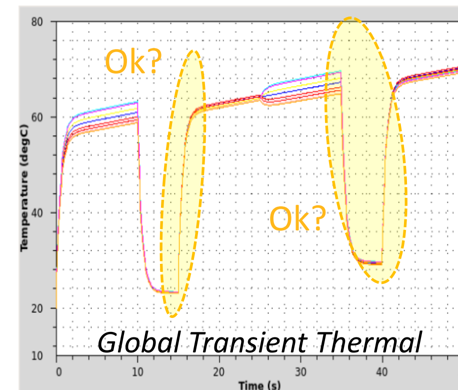
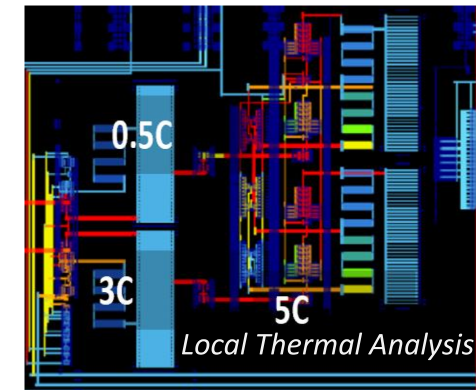
## Convergence from early Optimization to final Signoffs




### Thermal Floorplanning

- Heat Sources / Power floorplanning
- Bump/TSV exploration
- Heatsink, boundary model

### Thermal-Stress Reliability

- Golden standard
- Mature, proven
- Full system integrity

### Power-Thermal Management

- Power-Thermal Scenario Profiling
- Thermal Field Metamodel
- Transient Thermal Analysis

### Thermal-Aware Design Closure

- ElectroMigration SignOff
- Root cause Analysis
- Net based Visual debug

Multi-dies System Pre-Layout SignOff ⟵ Individual IPs' RTL Power SignOff ⟶ Individual Die Post Layout SignOff

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# THANK YOU

*Merci*

Our Technology,
**Your Innovation**™