Flexible Hardware-assisted Verification

Synopsys ZeBu EP platforms

Johannes Stahl, Executive Director, Product Marketing
Synopsys

Your Typical Zoom Day…

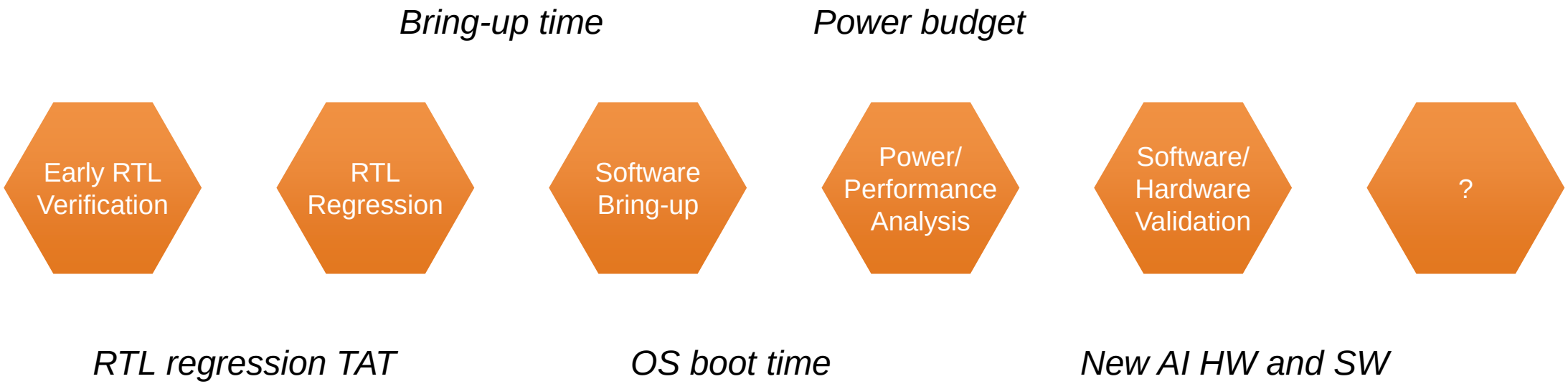
HDMI™
HIGH DEFINITION MULTIMEDIA INTERFACE

Incomplete System Validation

Topics for today

- HAV use case journey
- ZeBu EP overview
- ZeBu EP demo intro

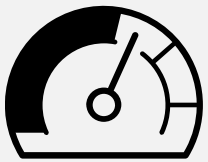
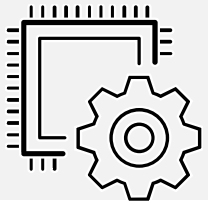
Synopsys HAV Use Case Journey



Software Bring-up

Challenges	• SW integration only in silicon • Risk of silicon re-spin • Cost, schedule overrun and lost revenue
Goals	• Pre-silicon SW validation • SW and HW bugs removed pre-silicon • Reduced project cost and schedule
Requirements	• Full, early SoC model executing SW fast • Support of critical SW (boot, app, training) • OS boot in 30 min
Risks	• Lack of experience with hybrid technologies • Lack of IP models • HAV platform stability
Solutions	• Fastest hybrid platform ZeBu / Virtualizer • Experience and broadest model portfolio • 30+ users: Samsung, Google, ….

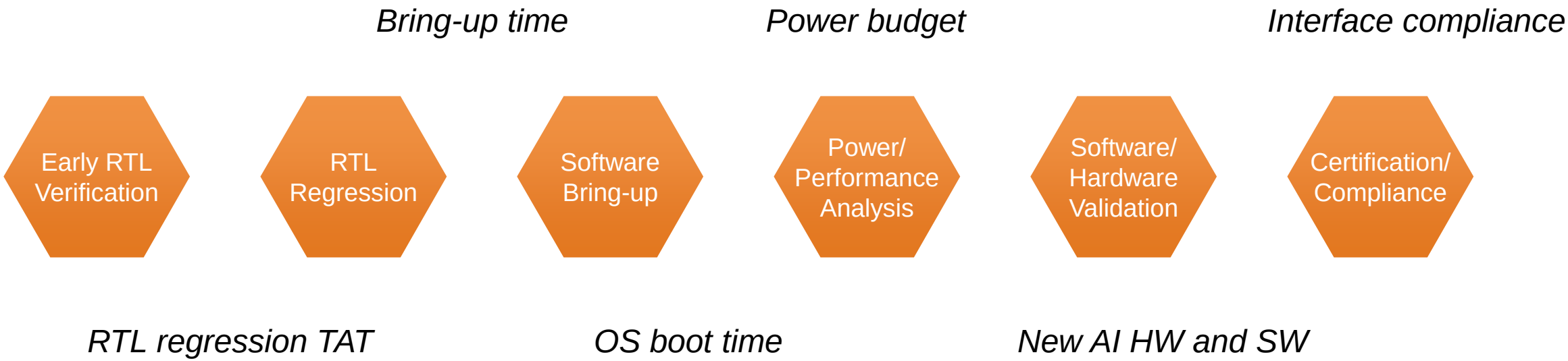
Power/ Performance Analysis

 Challenges	• Silicon power budget exceeded • Software fix insufficient • Lost customers and revenue opportunity
 Goals	• Silicon power within expected budget • Optimization of architecture for SW workload • Winning design sockets
 Requirements	• Analyze power for long workloads • Scalable, fast TAT power calculation • Analyze performance bottlenecks
 Risks	• Using sign-off power tools is too slow • Synthetic workloads do not represent reality • Analysis too late for making RTL changes
 Solutions	• Leverage fastest emulation engines • Full power analysis flow • Deployed at AMD, Samsung,…

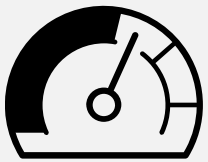
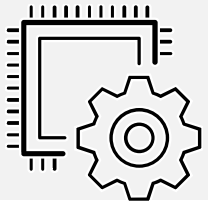
SW/HW Validation

Challenges	• Validating a new processor architecture • New AI SW stack on new AI architecture • Running enough application tests pre-silicon
Goals	• Processor RTL compliance with ISA • Run long AI workloads on final architecture • Execute complex networking traffic
Requirements	• ISA reference model and compliance test • Fast and reliable execution engine • Interfaces to real or virtual traffic generation
Risks	• Reliability of HAV platform for long SW runs • RTL debug using multiple HAV platforms • HAV compile for complex designs
Solutions	• Leverage fastest emulation engines • Arm or RISC-V reference models • Arm compliance test suite (SBSA)

Synopsys HAV Use Case Journey



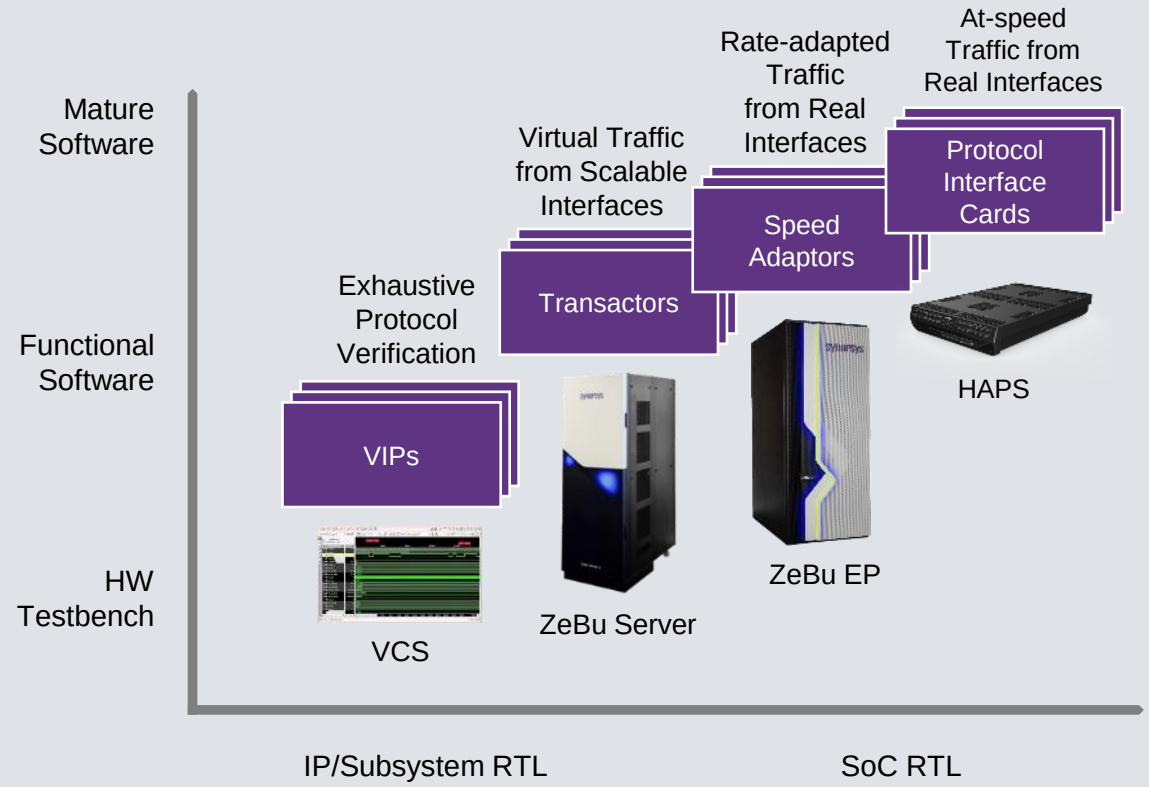
Compliance Certification

 Challenges	• DUT Interface may not be compliant w/ spec • DUT Interface may not work w/other devices • Chip respin maybe required
 Goals	• Run compliance tests at-speed • Run interoperability tests at-speed • Verify interop. between Controller and PHY
 Requirements	• PHY board w/ IP testchip • High-performance FPGA platform for at-speed testing
 Risks	• PHY board w/ IP testchip not available • FPGA Timing closure not possible • DUT Interface SW driver development time
 Solutions	• HAPS = Industry Highest Performance • HAPS IPK = pre-validated SNPS Interface IP Prototype running at-speed w/ SW drivers

Broad Protocol Solution Across Use Cases

PCIe 6.0, CXL 3.0, USB 4, HBM3, UCIe…

Protocol validation using physical and virtual testers



IP Prototyping Kits for HAPS and ZeBu EP

- High Quality & Ease of Use
  - Validated Synopsys IP FPGA Reference Design
  - Ease Synopsys IP Integration into SoC Prototype
- Flexible Configurations
  - Documented supported configurations with automated reconfiguration flow
  - Other configurations supported via SoW
- Soft Only Deliverables
  - Additional hardware required to run reference designs documented in prerequisites

Synopsys IP Prototyping Kit for HAPS and ZeBu EP

IP Core License Required

What we Deliver

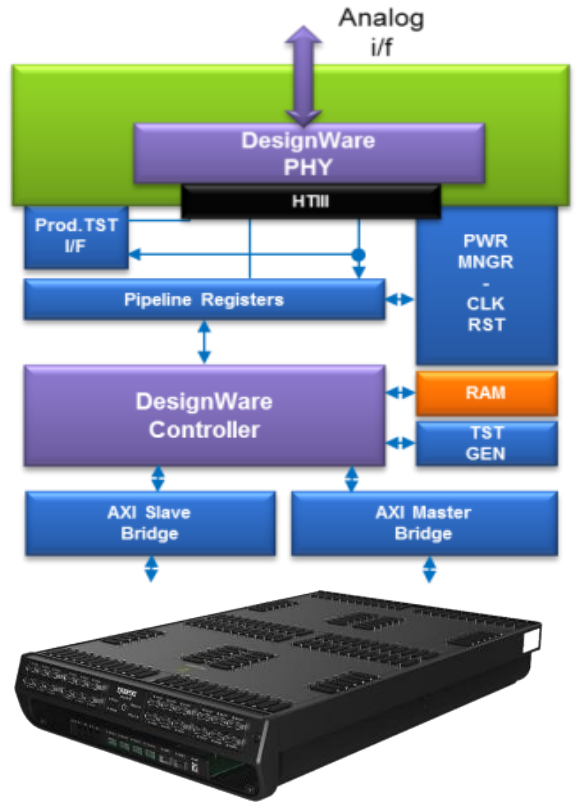
DW-IP FPGA Ref. Design (Verilog Source Code, Simulation Testbench, pre-built image, ProtoCompiler Scripts)

Software (Driver Source Code, Example App. Software, Compilation scripts, Linux Kernel config)

Documentation

Support Channel

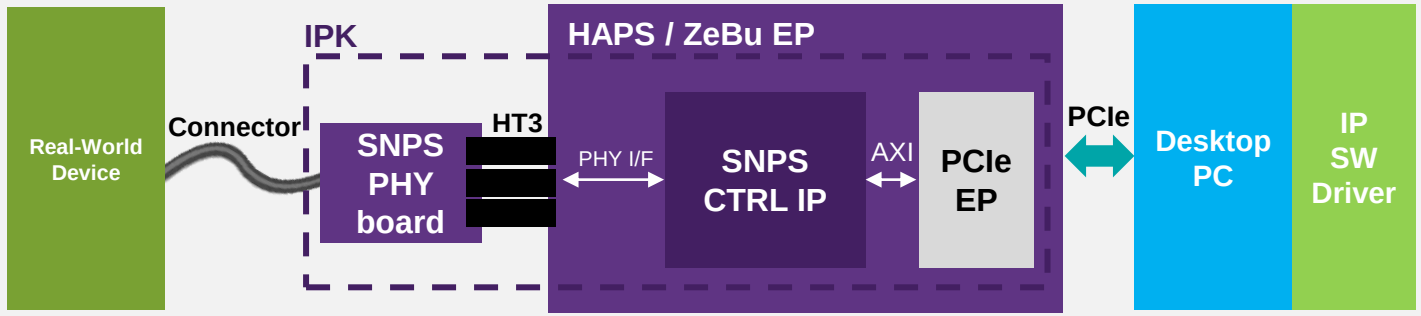
Used with HAPS and ZeBu EP HAV solutions



IPKs enable SW development and Compliance

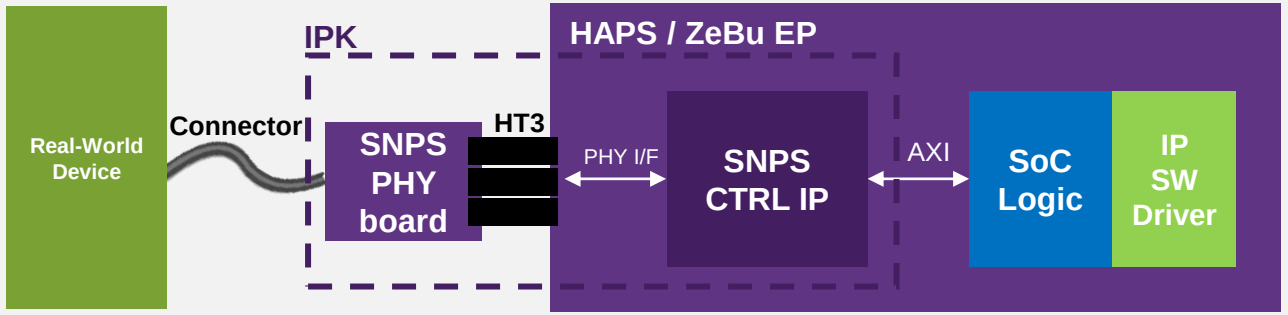
Industry Unique Combination of Synopsys IP and Synopsys HAV

OOB Software
IP Driver Development



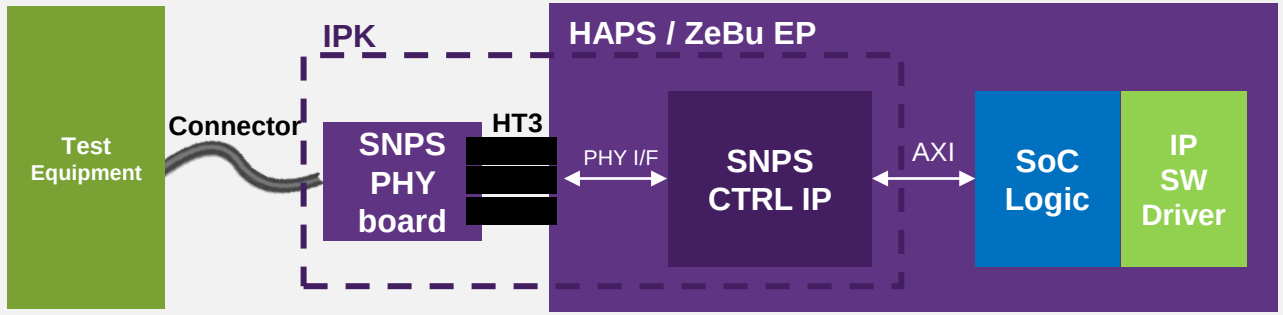
Out of the Box Software Driver Development

Interop Testing / PlugFests



3rd Party Interop Tests

Compliance Tests



Protocol Compliance Tests

Verification & Validation Use Cases

Broad Portfolio of HAV Platforms and Solutions

Verdi & VCS

Early RTL Verification

ZeBu Server 5 ZeBu EP1 ZeBu EP2

Compliance/ Certification

HAPS IP Prototyping Kit

RTL Regression

Software/ Hardware Validation

HAPS Protocol Interface Card

Speed Adaptor

HAPS-100

Virtualizer

Software Bring-up

Power/ Performance Analysis

Platform Architect

ZeBu Empower

Unified Core Technologies: Compile, Debug, Hybrid, Transactors

Synopsys HAV Product Family

Highest-performance HAV and Pre-silicon SW Development Use Case Leader

ZeBu Server

Most Scalable HAV Platform
Lowest TCO, and Most Reliable Emulation

ZeBu EP

Single Hardware Platform – all HAV Use Cases
Lowest TCO for both Emulation and Prototyping

HAPS

Highest performance HAV Platform
At-Speed Protocol Validation with Broadest IP Support for Prototyping

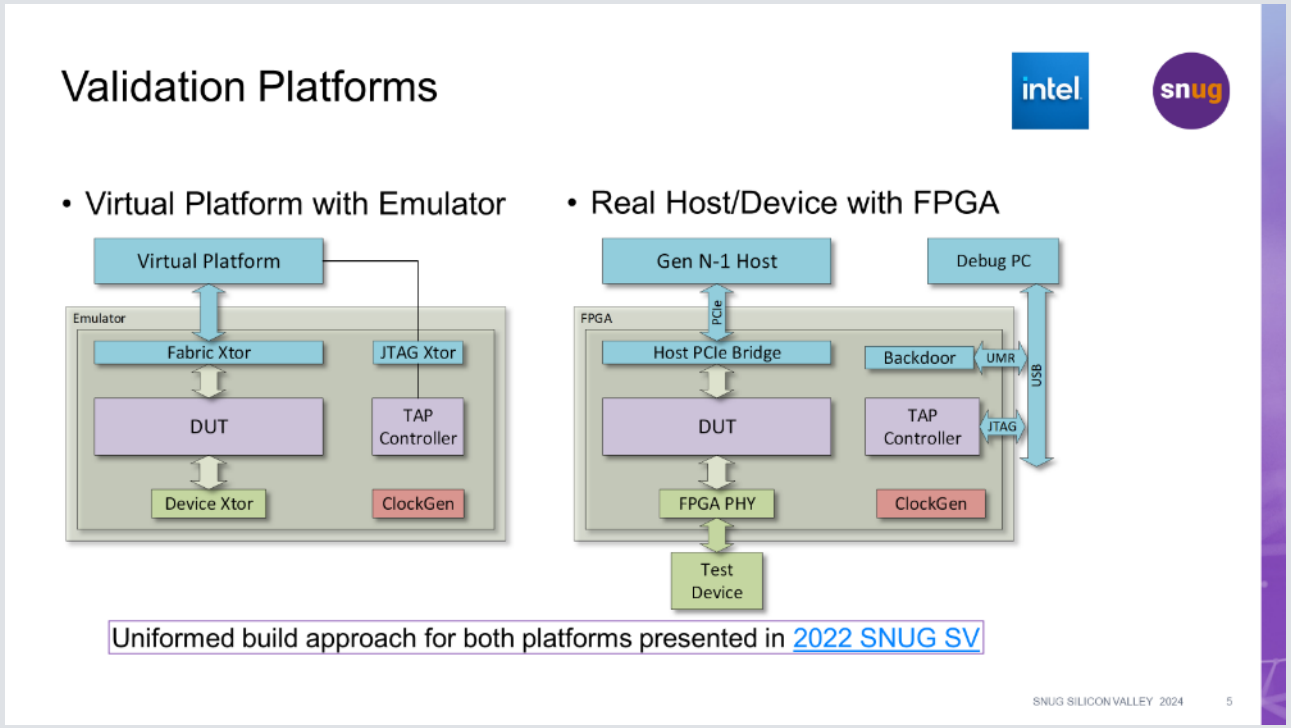
ZeBu EP2

Single Hardware Platform – all HAV Use Cases

- Highest performance for up to 5.8 BG designs
- 1.4 BG capacity per rack
- Proven HAV use cases
- Emulation and Prototyping flexible use
- Direct-connect architecture using HAPS-100 12 FPGA

ZeBu EP Customer Success Example

40k Regressions per week on ZeBu EP platforms

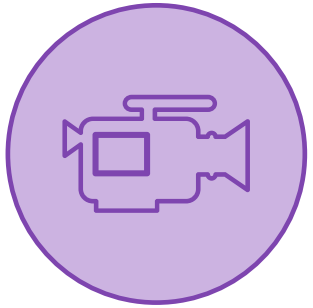


Presented at
SNUG Silicon Valley 2024

Improving Execution Efficiency and Debug Throughput using ZeBu EP1 for Emulation and Prototyping - Jing Zhang - Intel

ZeBu EP Demo: Video Streaming

Using emulation for SW/HW validation with virtual interfaces and real-world interfaces



Input source can be pre-captured video frames or live real device (MIPI camera)

Simultaneous display on video transactor virtual screen and actual display

Video decoder implemented in hardware

SW/HW validation with full visibility and dynamic trigger capability

Validation through visual inspection of video output

Flexibility for Different Interface Technologies

ZeBu EP1 can switch use mode for different runs with one HW setup

ZeBu EP Module

Video decoder

Video RGB 3 x 8bit + H/V sync

Video to AXI Stream

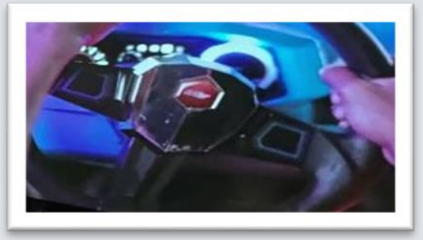
AXI Stream source sel.

Video DMA Adapter

AXI S. to video

Video Xtor

Runtime host display



MIPI DSI Subsystem + D-PHY

HDMI display

Video File DDR (ZRM)

AXI Xtor (IP config)

MIPI CSI Subsystem + D-PHY

Runtime host

MIPI CSI camera

DDR4 (D-ICE)

HT3 MIPI HSIO daughter board

MIPI DSI to HDMI

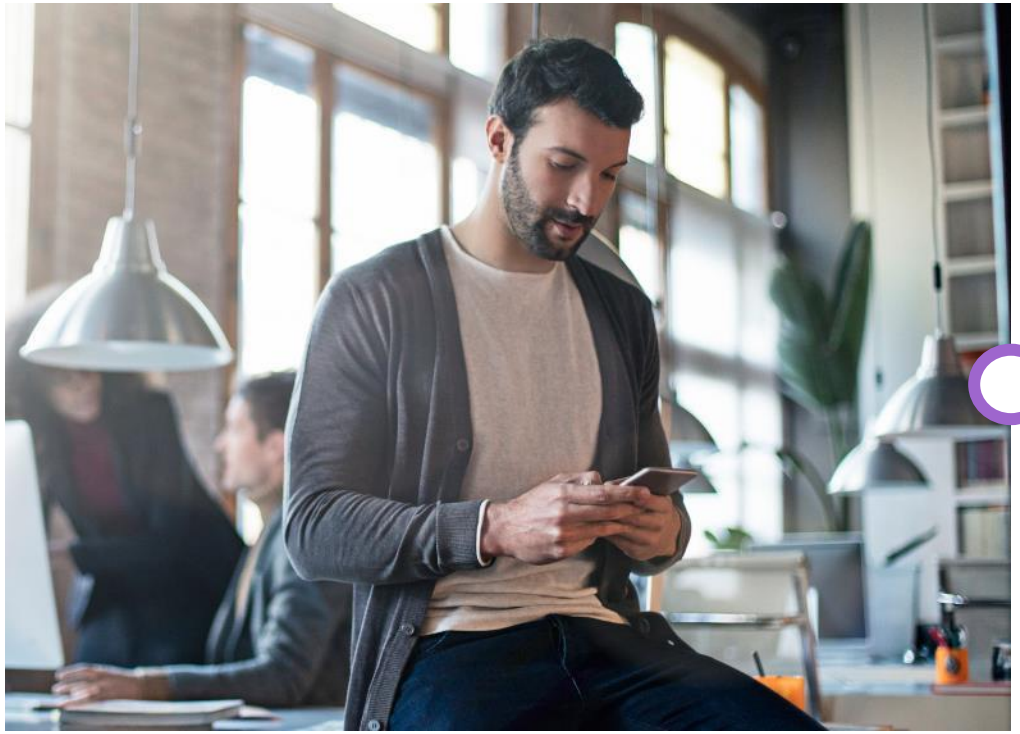
Emu clock domain (25 MHz)

Speed adaptation

Real-world clock domain (200 MHz)

Fastest Clock domain (800 MHz)

A Better Zoom Day…



Certification and Compliance with Synopsys ZeBu EP


THANK YOU
Our Technology, Your Innovation™