3DIC Exploration, Implementation and System Analysis

For Multi-Die Design

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Synopsys

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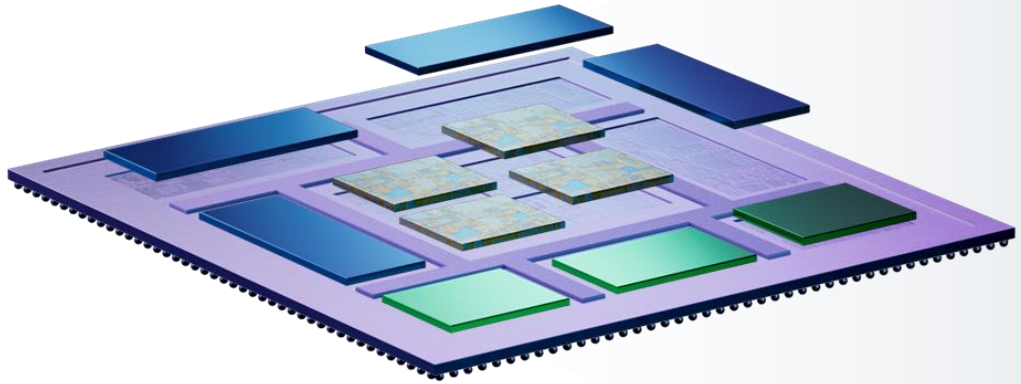
Agenda

- Industry Drivers and Challenges for 3DIC
- Synopsys Multi-Die Solution Overview
- AI Driven 3DIC Design: 3DSO.ai
- 3DIC Compiler: Technology Highlights
  - 3D Prototyping Flow and Thermal Analysis Solution
  - Scalable Solution For Multi-Die Bumps, HBs, TSVs and Fanout RDL Package
  - Multi-Die In-Design and Signoff Analysis
  - 3D Verification / DRC Checks
- Summary

The Drive to Multi-Die Designs



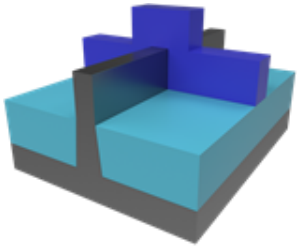
Motivation for Multi-Die

- Accelerated scaling of system functionality at a cost-effective price (>2X reticle limits)
- Reduced risk & time-to-market by re-using proven designs/die
- Lower system power while increasing throughput (up to 30%)
- Rapid creation of new product variants for flexible portfolio management

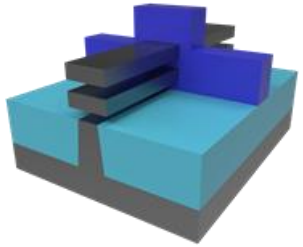
Transition to Multi-Die Design Triggers Profound Changes

ADVANCED NODE DESIGNS

FinFET



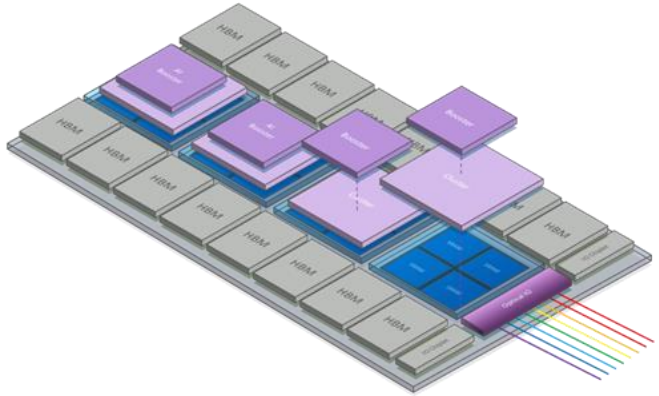
GAA



- Achieving design closure is more difficult
- Voltage drop effects worsen
- Electrothermal power integrity critical

Challenges Intensify with Multi-Die

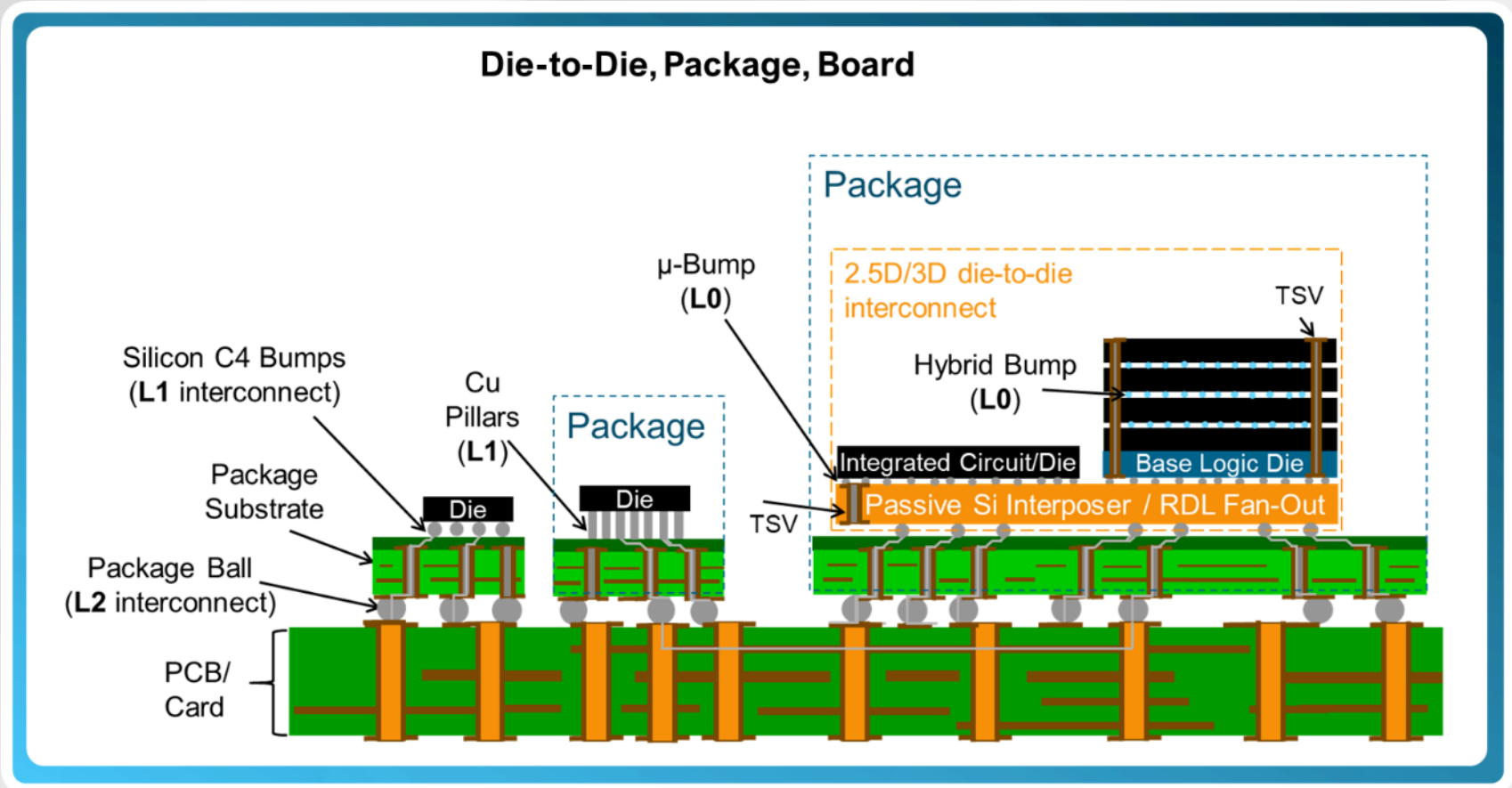
MULTI-DIE DESIGNS

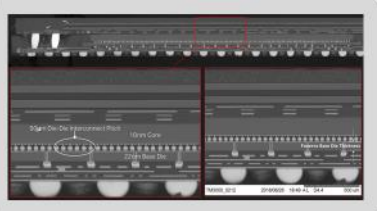


- Complex new failure modes
- Multi-chip power and thermal integrity
- Full-system capacity
- Electro-Thermo-Mechanical reliability
- Electromagnetics

3DIC Design

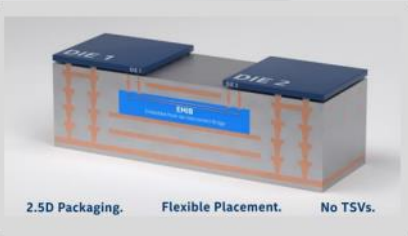
Requires Extensive Multi-die / Packaging Support

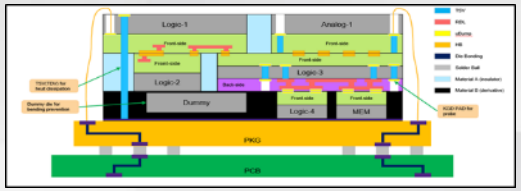




2.5D: 30-50 Chiplets on Base Die

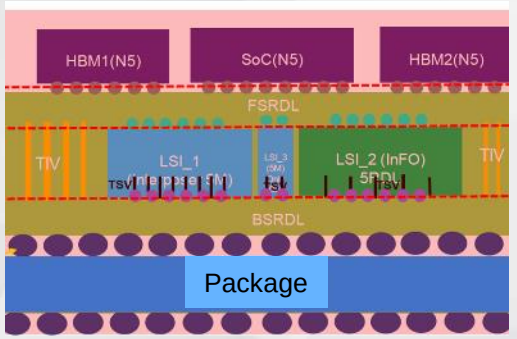
Bridge / Local Silicon Interconnects





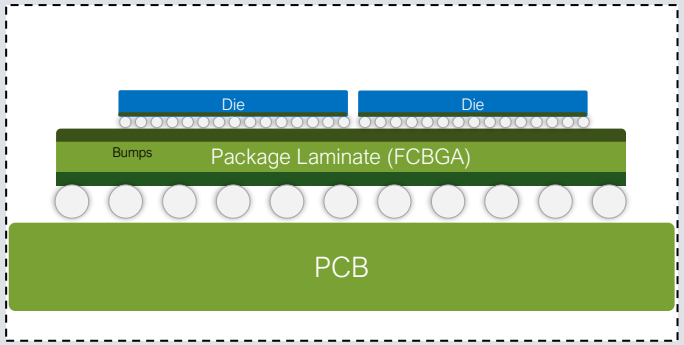
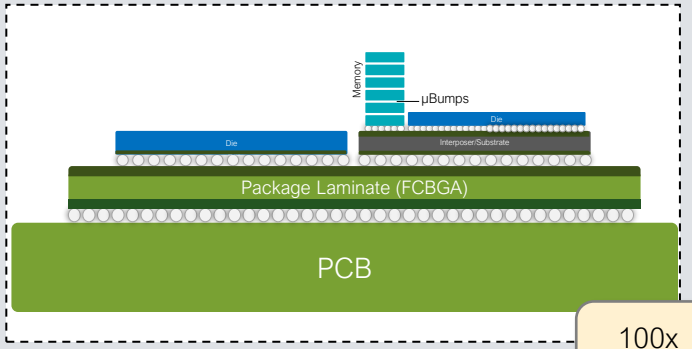
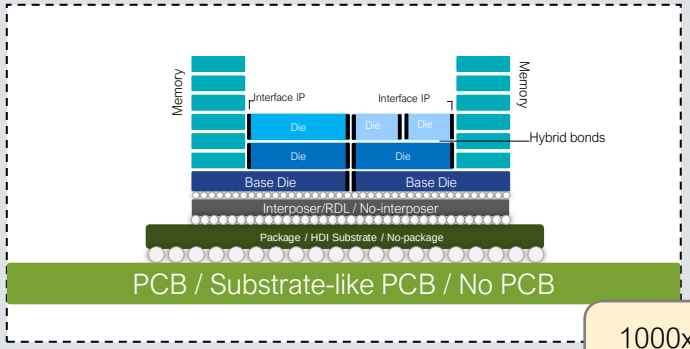
3D Stacking

Combinations + RDL Dies for Fan Out



Trends and Increasing Complexity…

Silicon Disruption!

	Traditional (2D/2.1D)	**Today** (2.5D/3D)	**Emerging** (3D System-Of-Chips)
			
Densities:	Wire-bond 10 IO/mm^2 Power: >10pJ/bit	Bumps (Flip-chip) 100 IO/mm^2 Power: >1.5pJ/bit	µBumps 1,000 IO/mm^2 Power: >0.5pJ/bit	TSV/nTSV 10,000 IO/mm^2 Power: >0.1pJ/bit	Hybrid Arch µBumps+TSV+W2W bonding	Hybrid Bonding 10,000-1M IO/mm^2 Power: <0.05pJ/bit
Challenges:	Integration of 1-2 dies in a laminate package (low density)	Managing high density connectivity/data rate between chip/chip, chip/pkg	**Heterogeneous integration**, increased complexity, order of magnitude higher density/connectivity scaling and data rates	

100x density

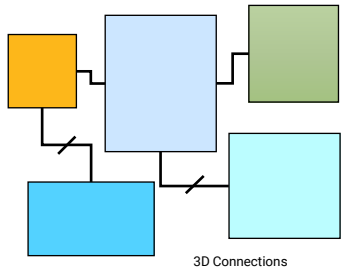
1000x density

3D Heterogeneous Integration Space…

Exacerbating optimization challenge!

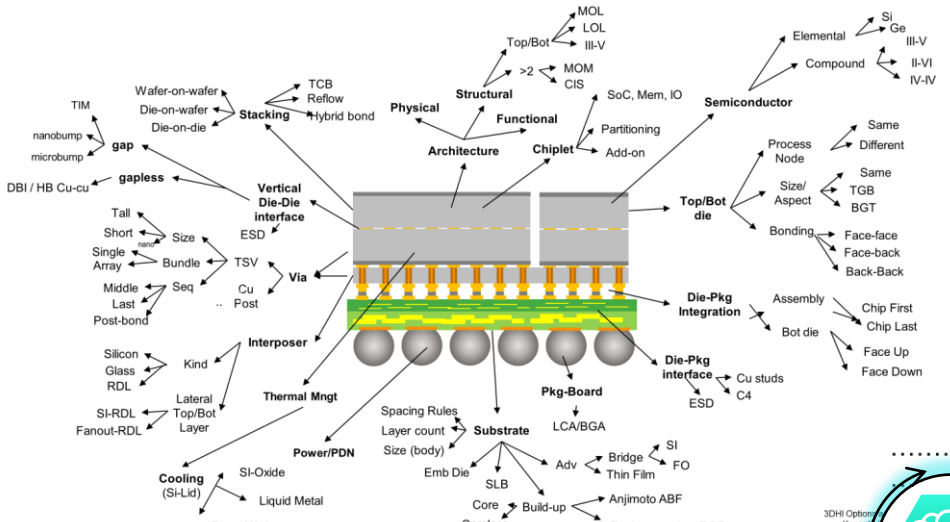
Application Workload

System Definition and Selection

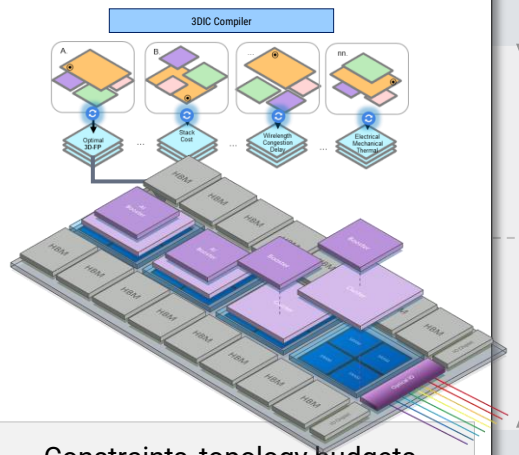


Decomposition, topology, boundary conditions, feasibility

Multi-die Design Knobs (ex)



Architecture and Early Estimation

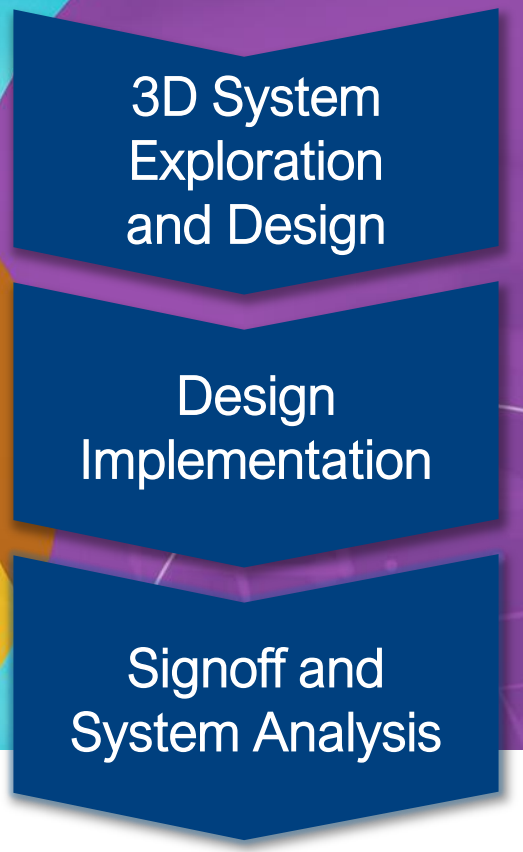


Constraints, topology budgets, connectivity and protocol/IP plans

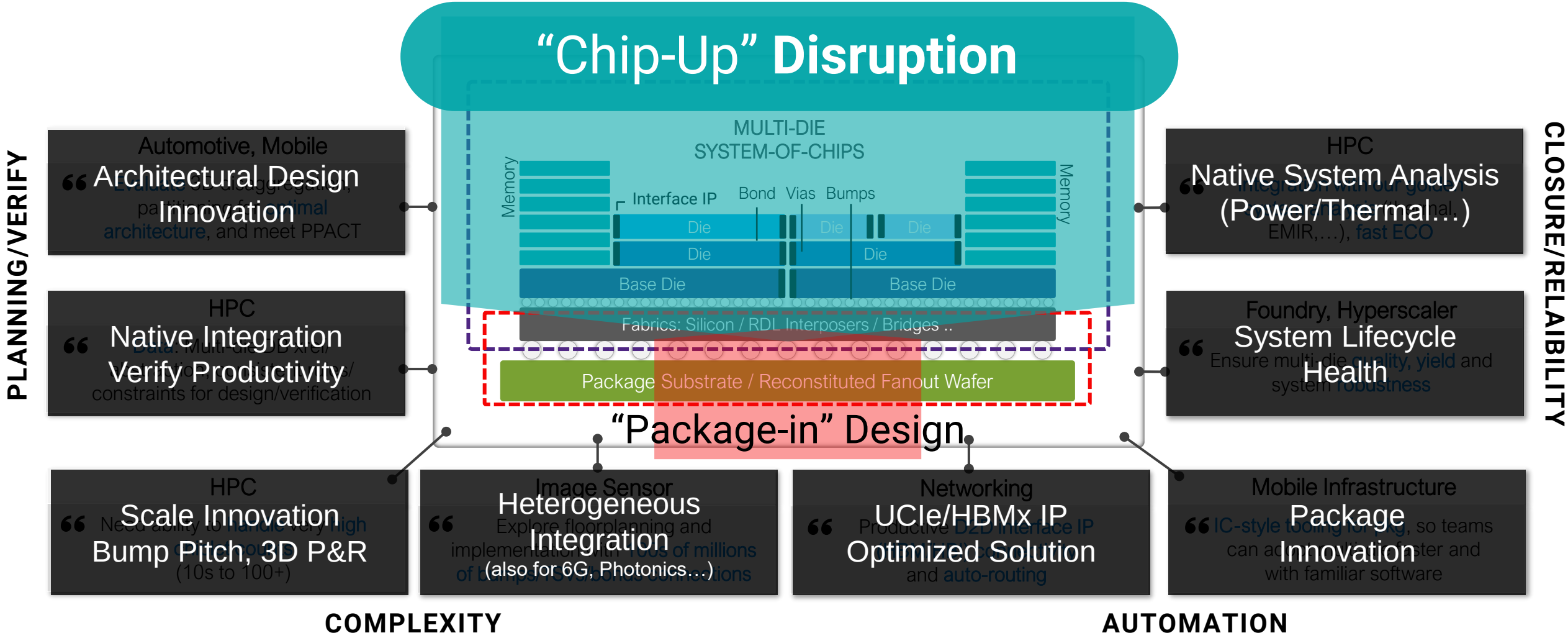
Optimal Architecture

- Huge design space of exploration – multi-dimensional, multi-scale, multi-material, and multi-physics
- Dependency on expert engineers – limited by availability
- Limited reachable solution space – sub-optimal QoR
- Longer time-to-target and convergence

Synopsys Multi-Die Solution Overview

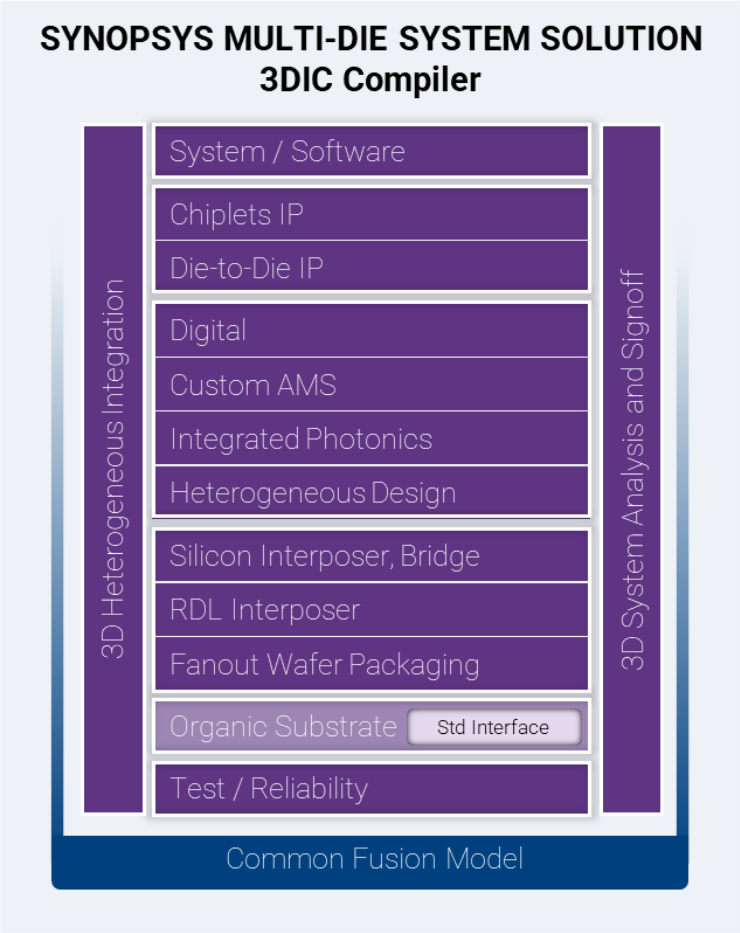


Customers' Feedback/Requirements Shaping Our Solution



Synopsys Comprehensive Multi-Die Solution

Seamless 2D to 3D Design Continuum



Unified Heterogenous Design and Integration platform

Open integrating industry standard solutions for multi-physics, RF/MM analysis, and package design

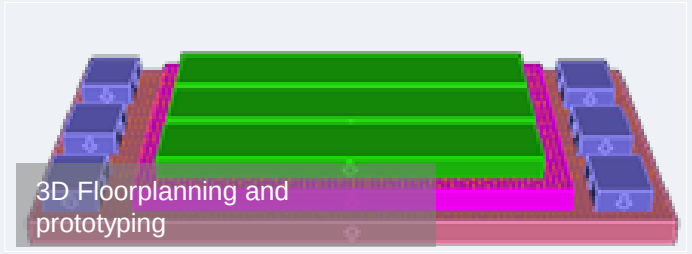
Premier foundry coverage (TSMC, IFS, Samsung)

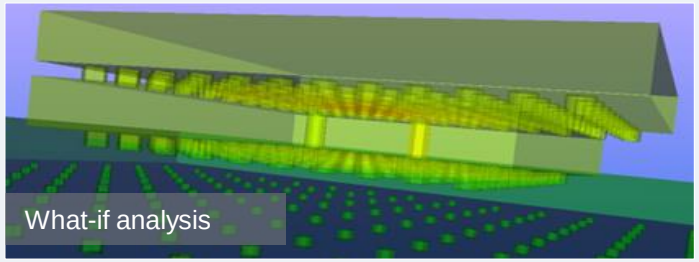
Trusted, Golden Analysis - STA, Power, Thermal, EM/IR, SI/PI, Mechanical Warpage and Stress

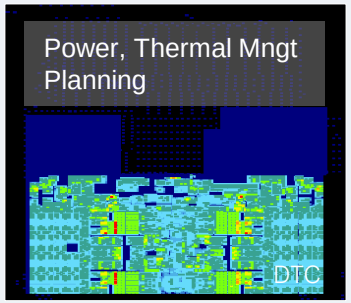
3DIC Compiler

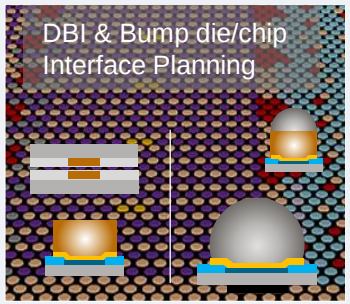
System-Level Exploration-to-Signoff Solution

PLAN & DESIGN

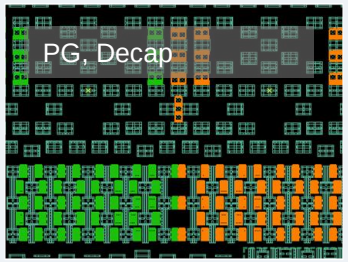


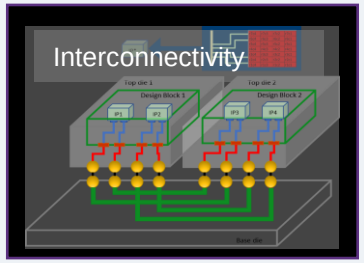


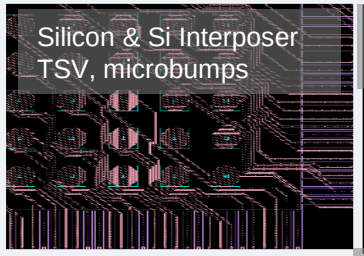


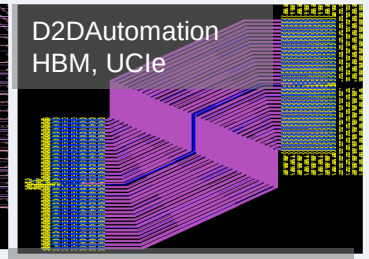


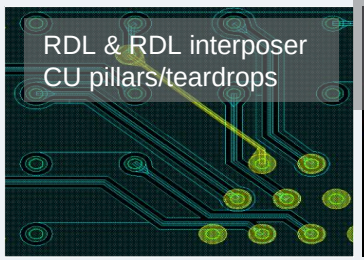
IMPLEMENT & OPTIMIZE

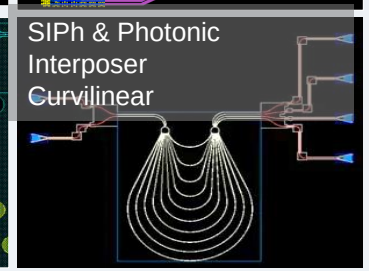




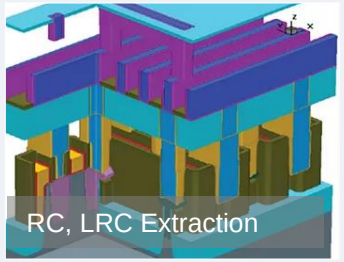


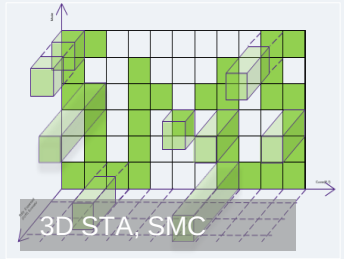


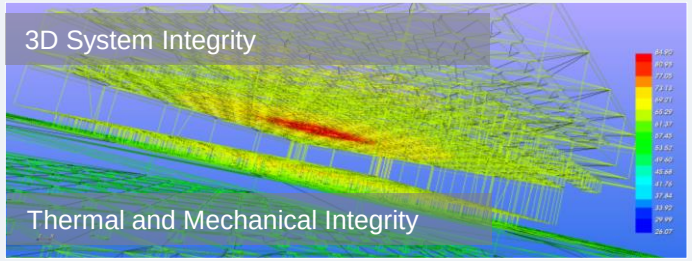


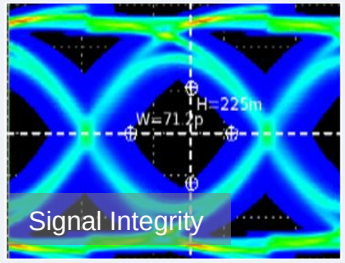


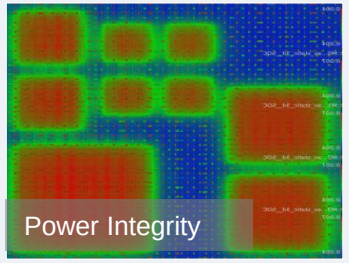
ANALYZE & SIGNOFF







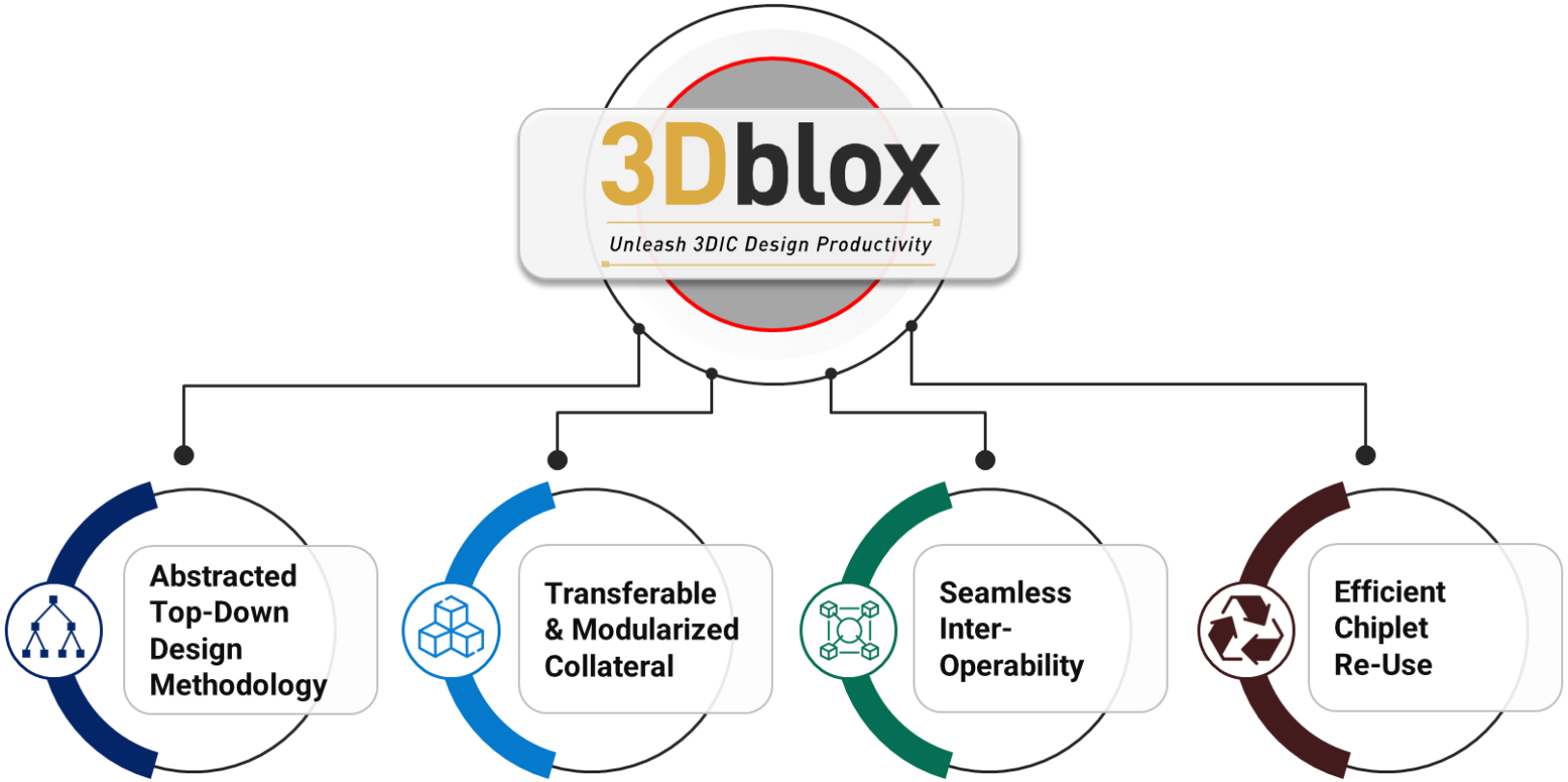




3Dblox: Accelerating the 3DHI Journey

An evolving vision for more efficient exploration and building of multi-die-system solutions

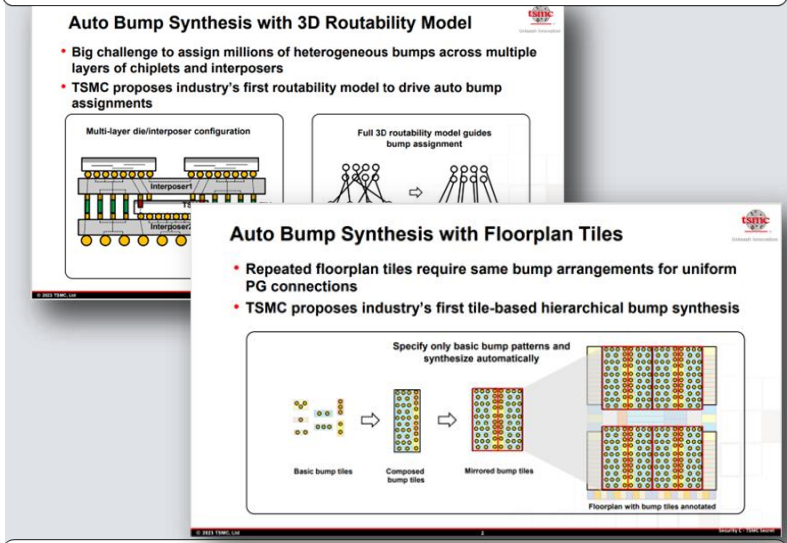
Available in Synopsys 3DIC Compiler today!



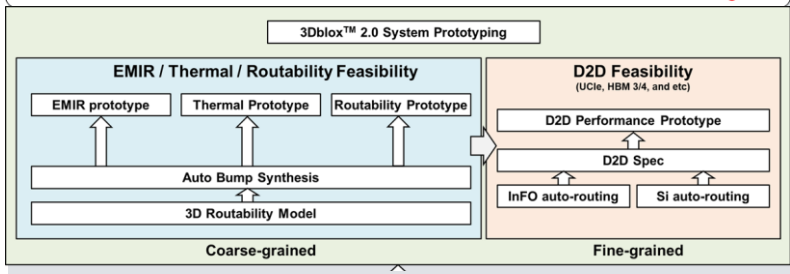
3Dblox Unleash 3DIC Design Productivity **v1.0** Data Formats & Fundamentals

Items	Synopsys
Design Template	V
Assertions	V
Interposer Hierarchy Auto Creation	V
PDN Analysis	(Ansys)
Thermal Analysis	(Ansys)
Physical Verification	V
Interoperability	V

3Dblox Unleash 3DIC Design Productivity **v1.5** Global Bump Optimization



3Dblox Unleash 3DIC Design Productivity **v2.0** Early Feasibility & Prototyping

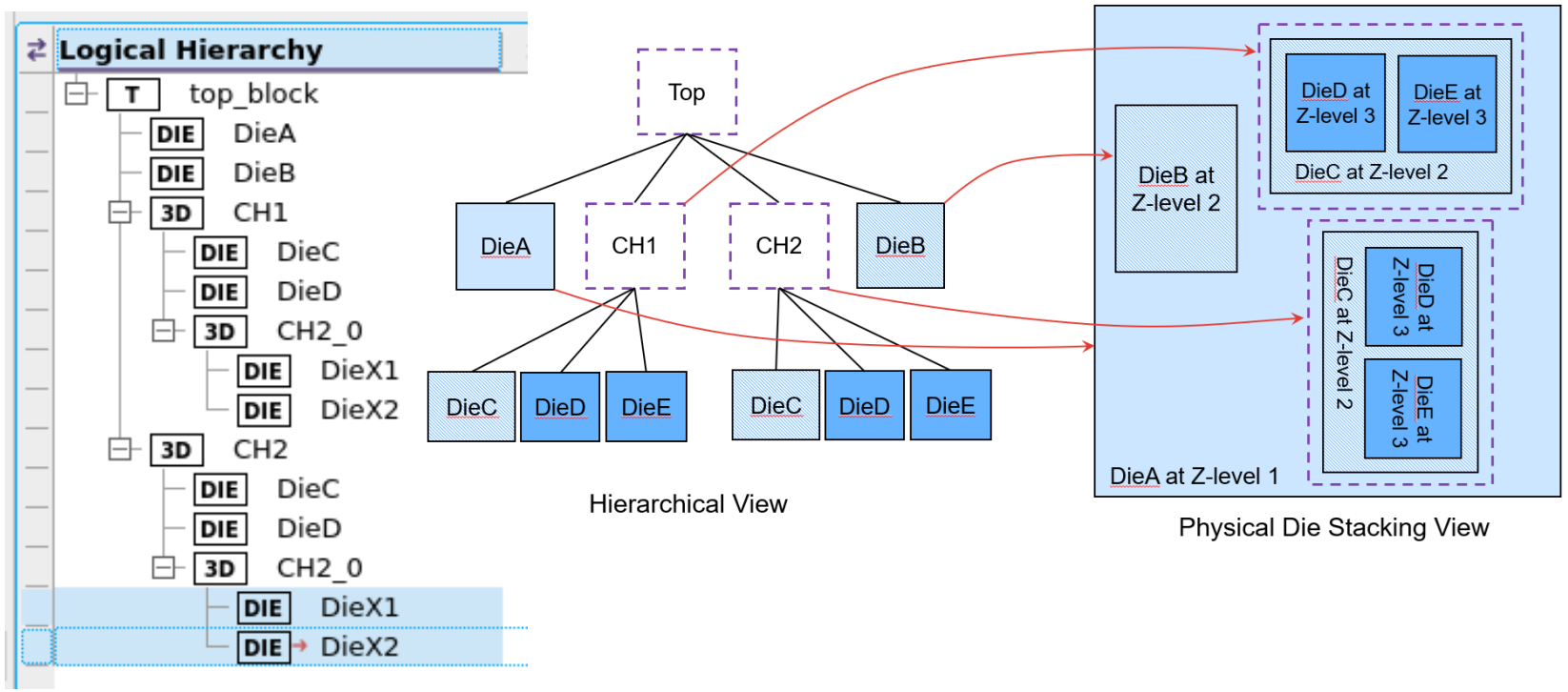


3Dblox: Compliance and Benefits

- Synopsys has been collaborating on 3Dblox from its beginning in 2022.
- Deep collaboration with Foundry and mutual lead customers.
- All Synopsys tools are fully compliant.
- Customers can benefit from
  - Single stack definition
  - Design data exchange between different EDA tools
  - Additional design flows enabled from 3Dblox

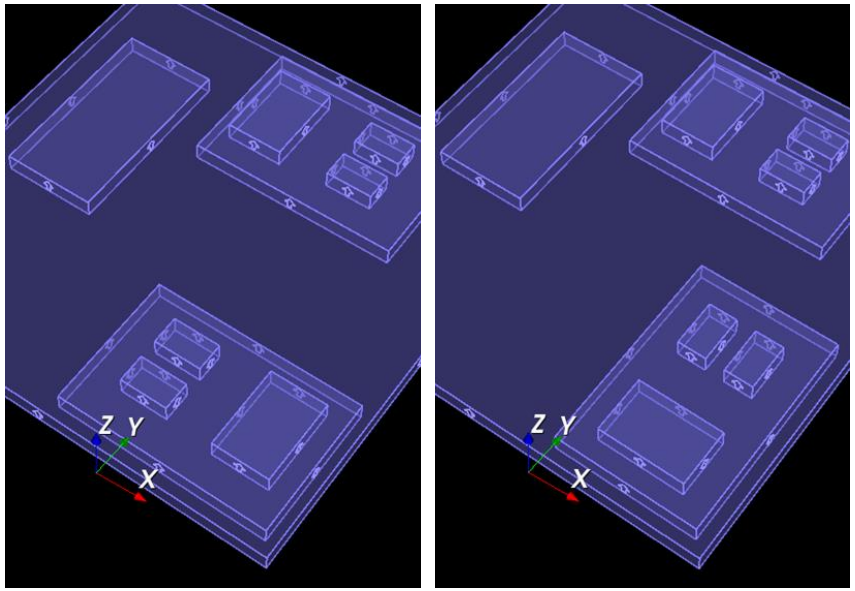
3Dblox Supports 3DIC Design Hierarchy

Extending Single Die design concepts to 3DIC

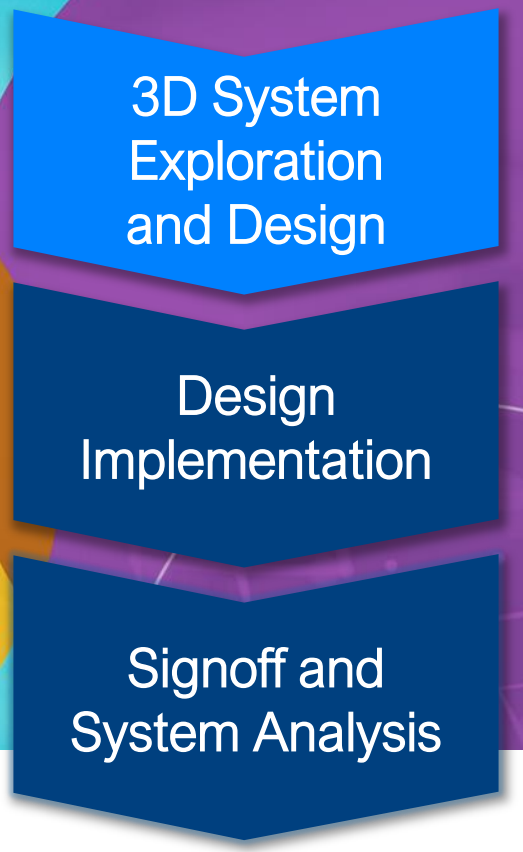


3DIC Compiler allows design hierarchy of chiplets, along with the usual expectations of multiple instantiations, rotation, & mirroring.

Chiplet mirroring: designed once but each mirror is a distinct GDS.



AI Driven 3DIC Design: 3DSO.ai



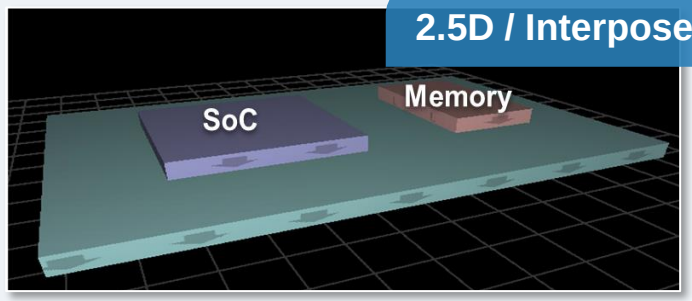
3DIC FP: Efficiently Traverse Solution Space

Early specifications-driven, cost-effective selection of optimal configurations

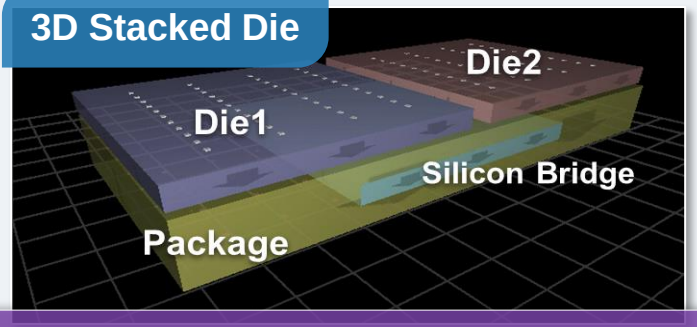
Across Technologies and Processes

Extensive Methodology Support

2.5D / Interposer



3D Stacked Die

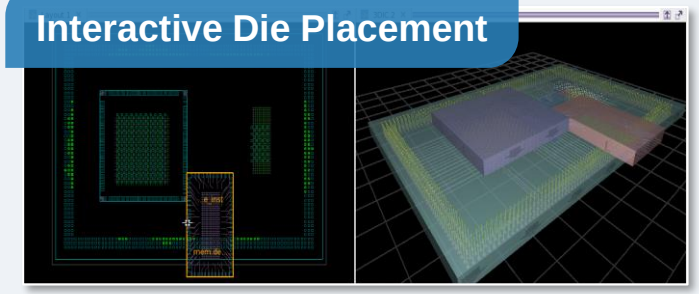


Maximum Solution Freedom

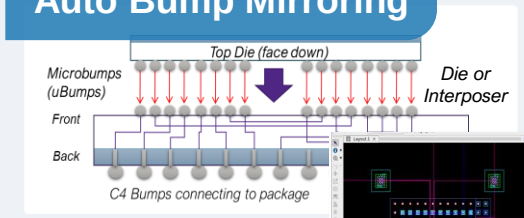
Iterate Fast and Effectively

Intuitive 2D/3D Visualization

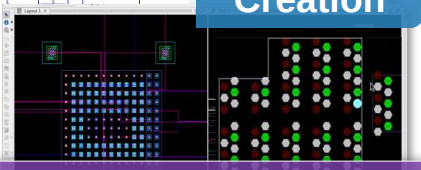
Interactive Die Placement



Auto Bump Mirroring



Interactive Bump Creation

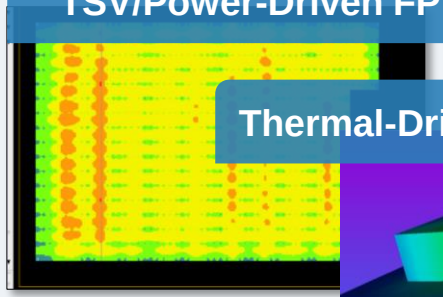


Increased Innovation Potential

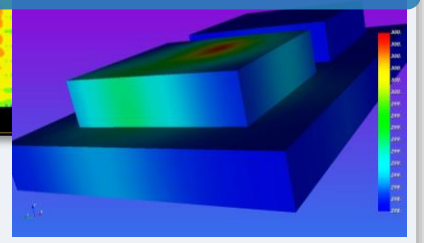
Convergently Refine

Golden-Analysis-Driven Optimization

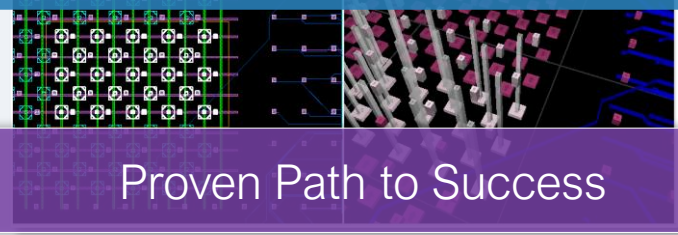
TSV/Power-Driven FP Optimization



Thermal-Driven Refinement



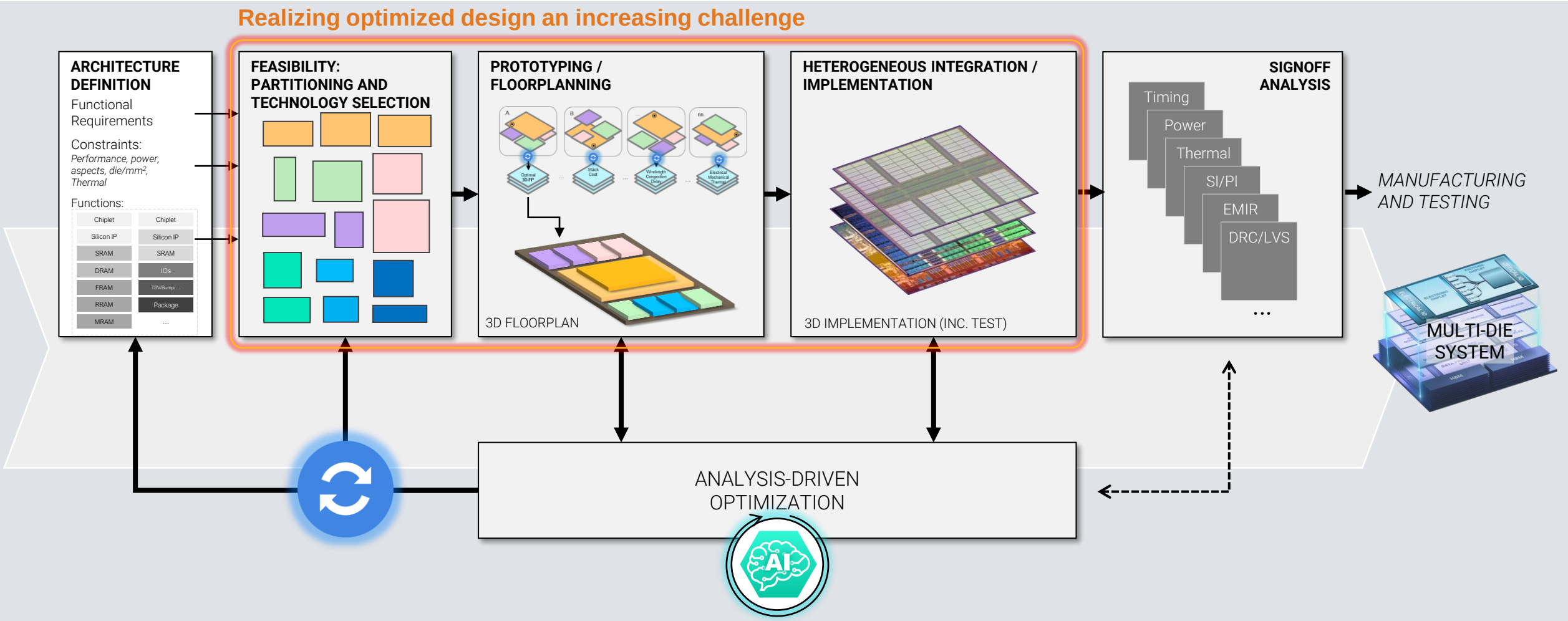
C4 and TSV Selection for Modification



Proven Path to Success

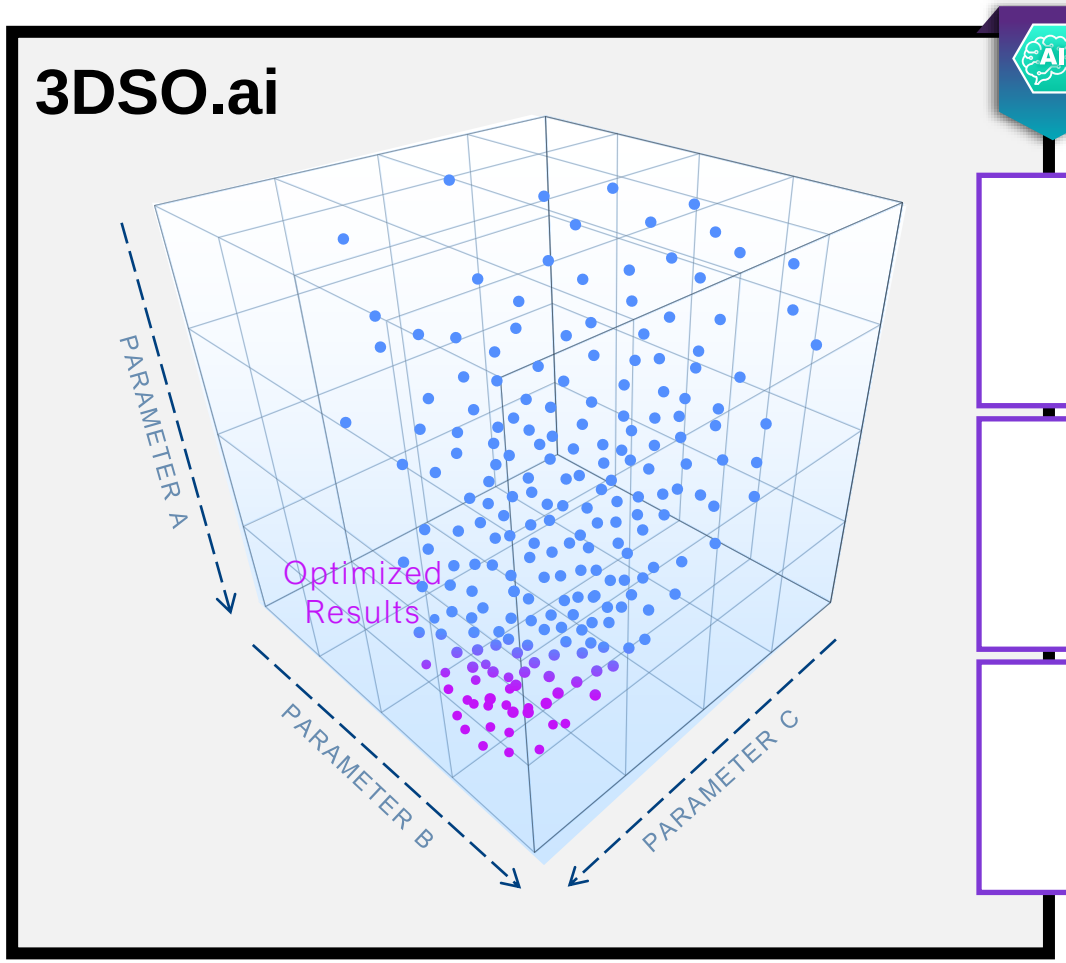
Multi-Die Design Journey…

Architect, create, implement, signoff and manufacture



Introducing **3DSO.ai**

Industry's first autonomous exploration and optimization of 2.5D/3DHI design space



Integrated AI optimization of multi-die designs for signal, thermal and power integrity **in single design platform – 3DIC Compiler**

Fast native analysis for unparalleled system performance and compute efficiency, while maximizing quality-of-results (QoR)

Unprecedented scalability to optimize across massive 3D design space of hundreds of billions of transistors and trillions of design permutations

Extending the Synopsys.ai Leadership

Key enabler for advanced multi-die package design

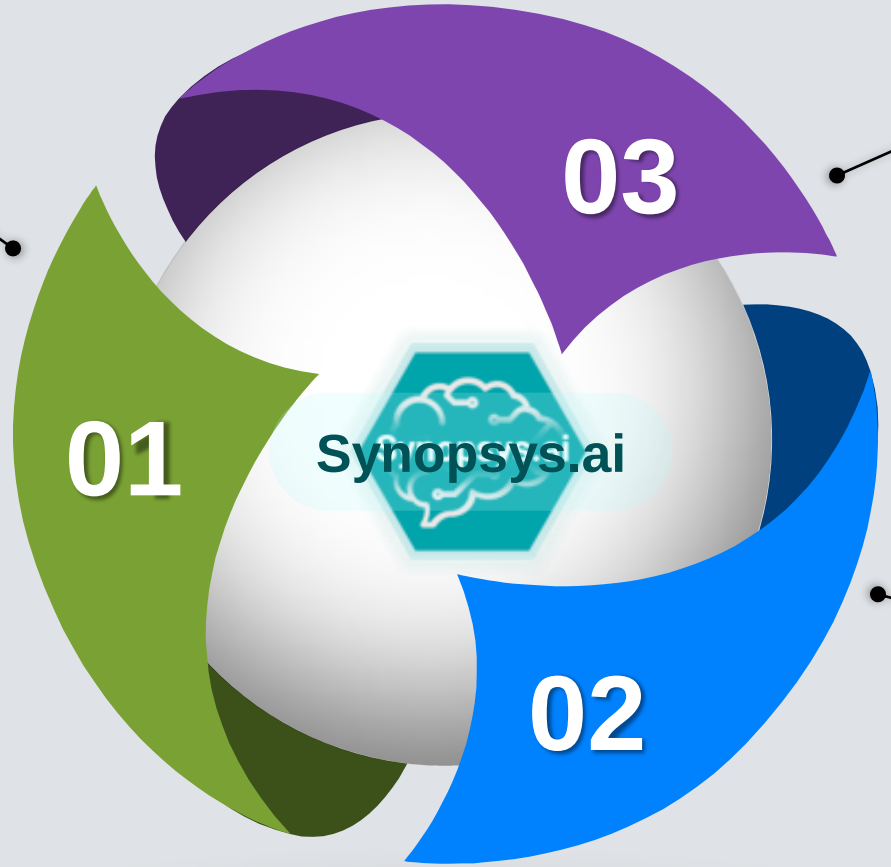
Optimization
(xSO.ai)

DSO.ai
VSO.ai
ASO.ai
TSO.ai

\+

NEW
3DSO.ai

AI-driven Autonomous
Multi-Die Design Space Optimization



Generative AI
(Copilot, ++)

Collaborative
Generative
Knowledge

Data Analytics
(x.da)

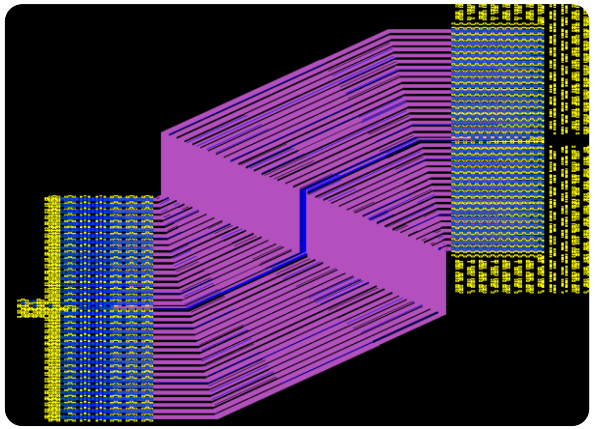
Design.da
Silicon.da
Fab.da

3DSO.ai Automates Expertise-Intensive Design Tasks

Three current areas of focus:

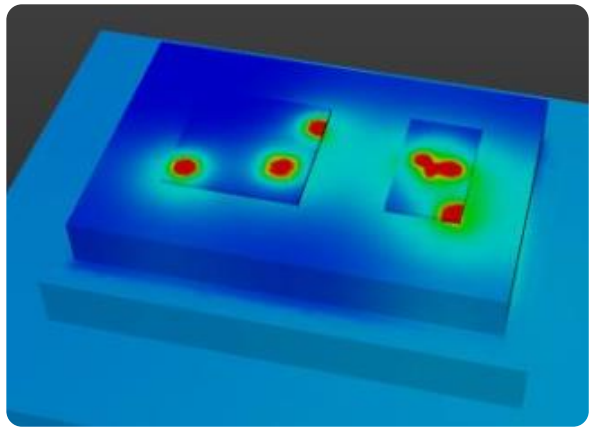
1

Signal Integrity Optimized Routing



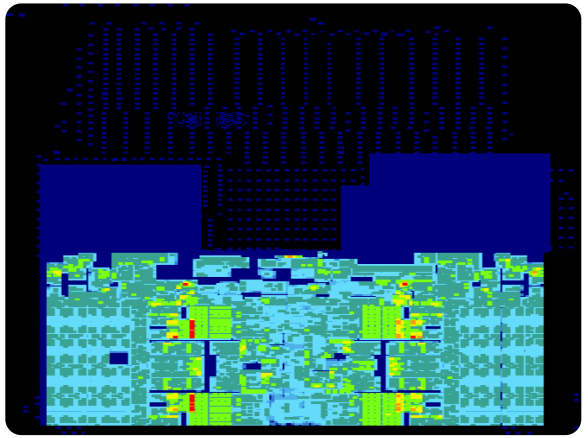
2

Thermal Integrity Optimized Floorplan



3

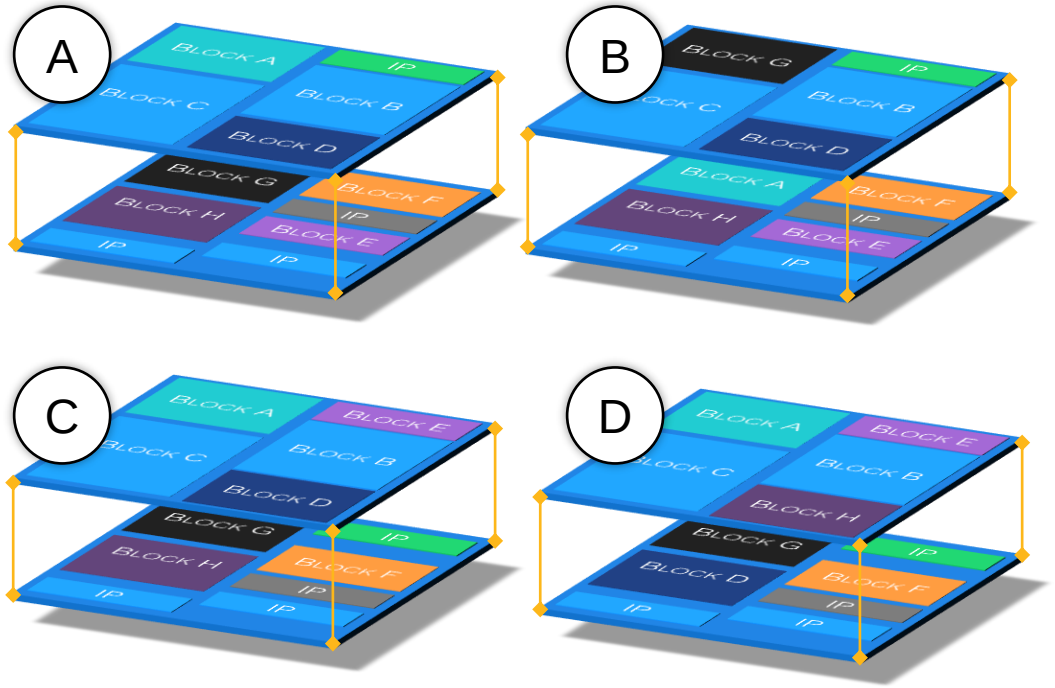
Power Distribution Network Design



2 Floorplan Efficacy Key Careabout for Architects/Designers

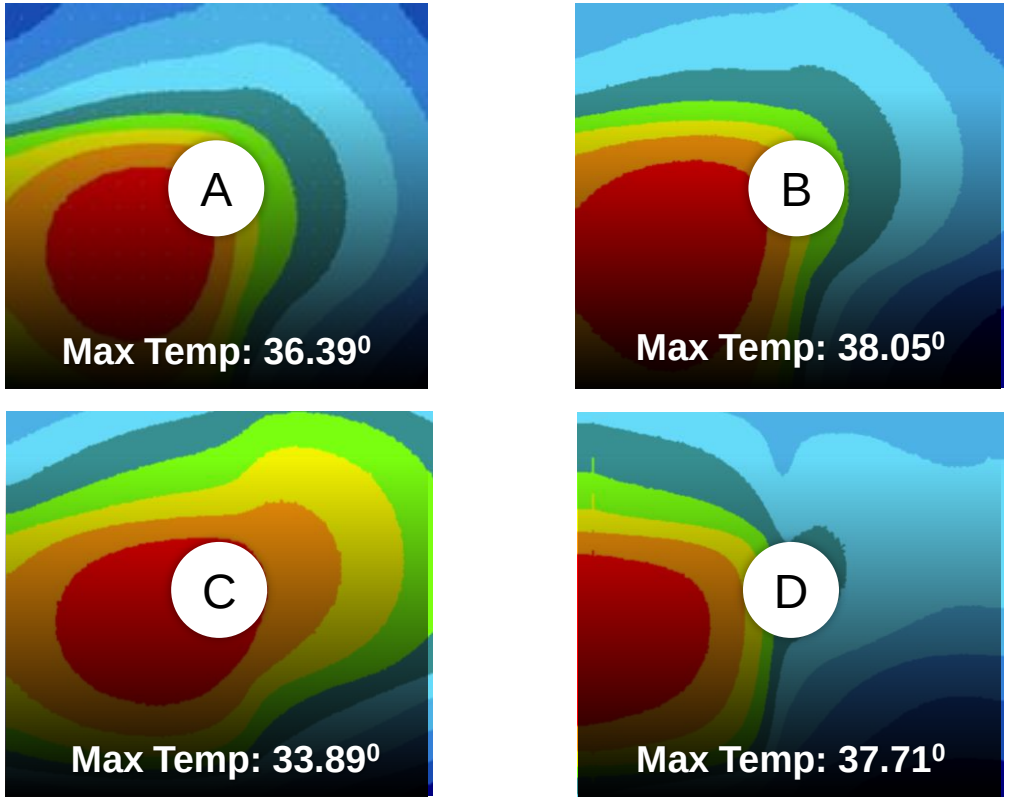
Power/thermal integrity optimization process could be very time-consuming

Configurations



Evaluate physical architectures vs. KPIs (e.g., thermal)

Thermal Evaluation

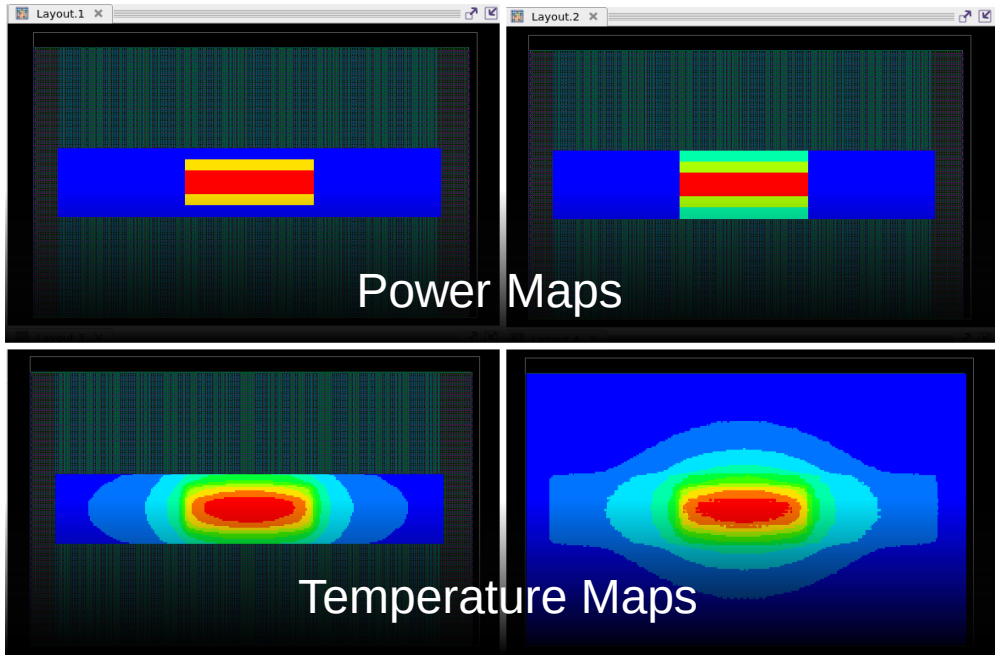


2

Case Study: Fast AI-driven Thermal Integrity Optimization

Accelerated convergence to superior results in ~200 exploration runs

Top Die | Base Die

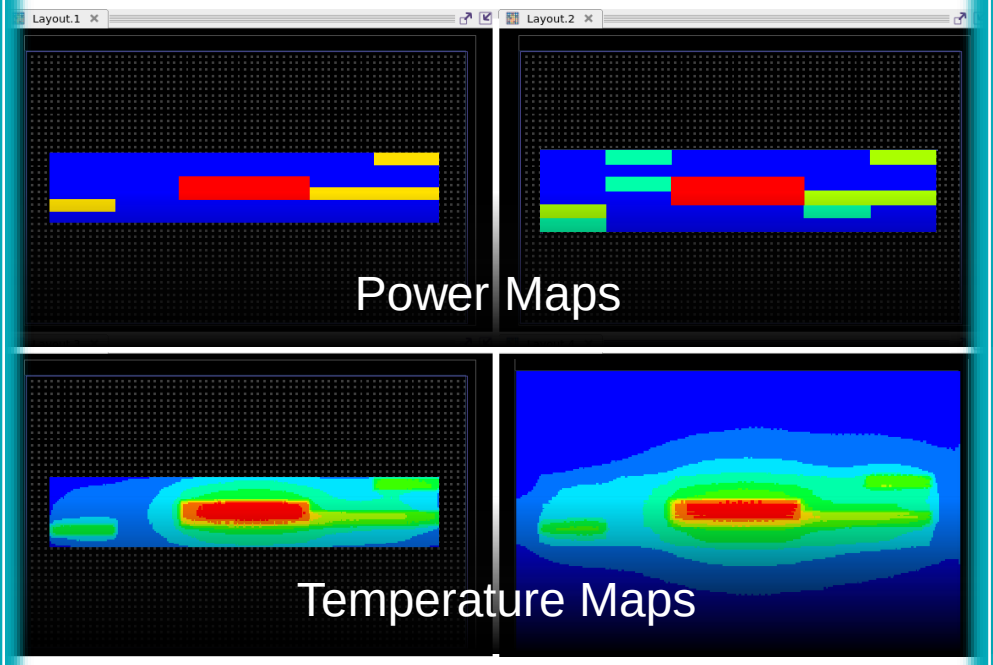


Max Temp =

126.2 ºC (baseline)

3DSO.ai Driven Floorplan

Top Die | Base Die

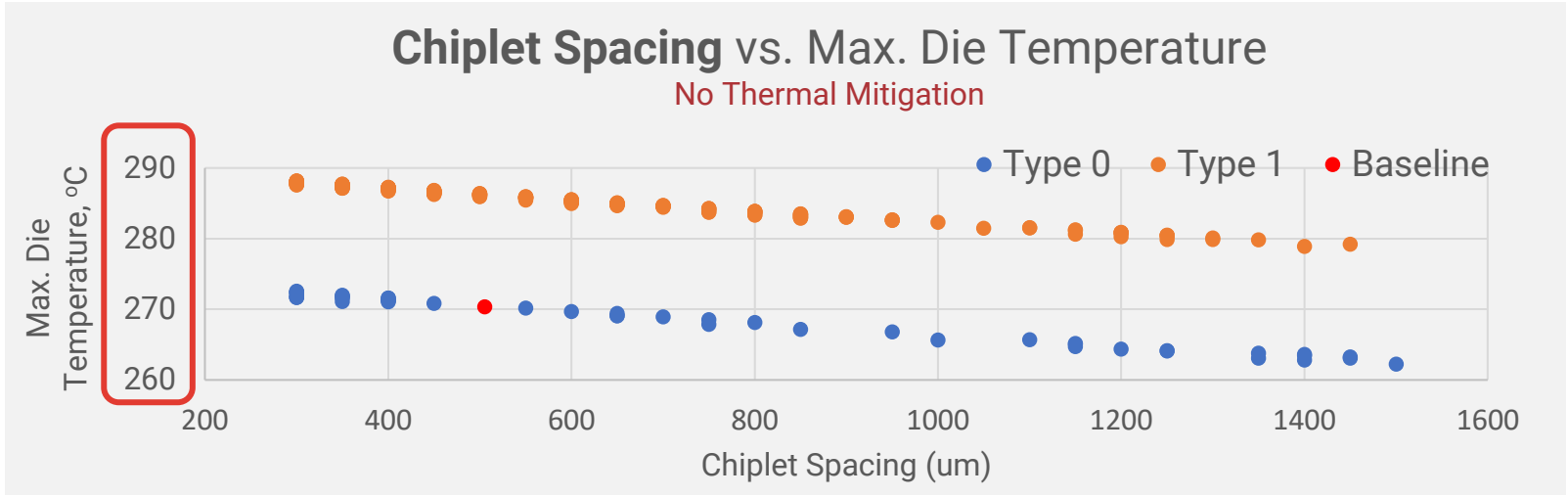


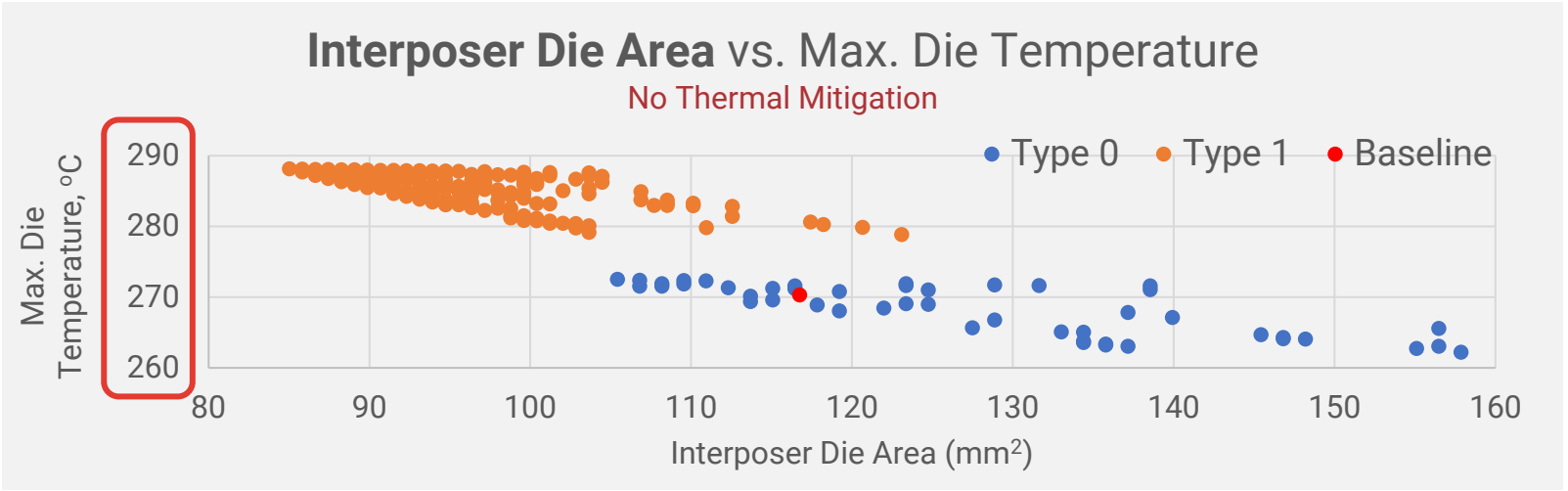
Max Temp =

105.4 ºC (post-3DSO)

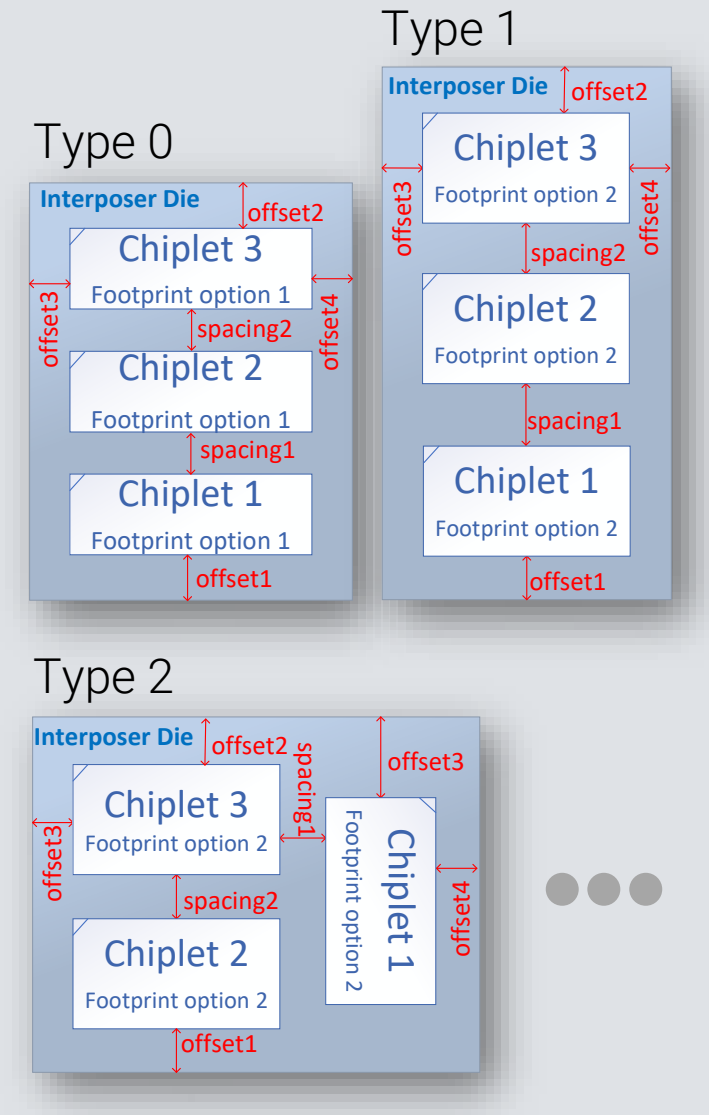
Example: Exploring Floorplan Options

Varying floorplan parameters to identify optimality



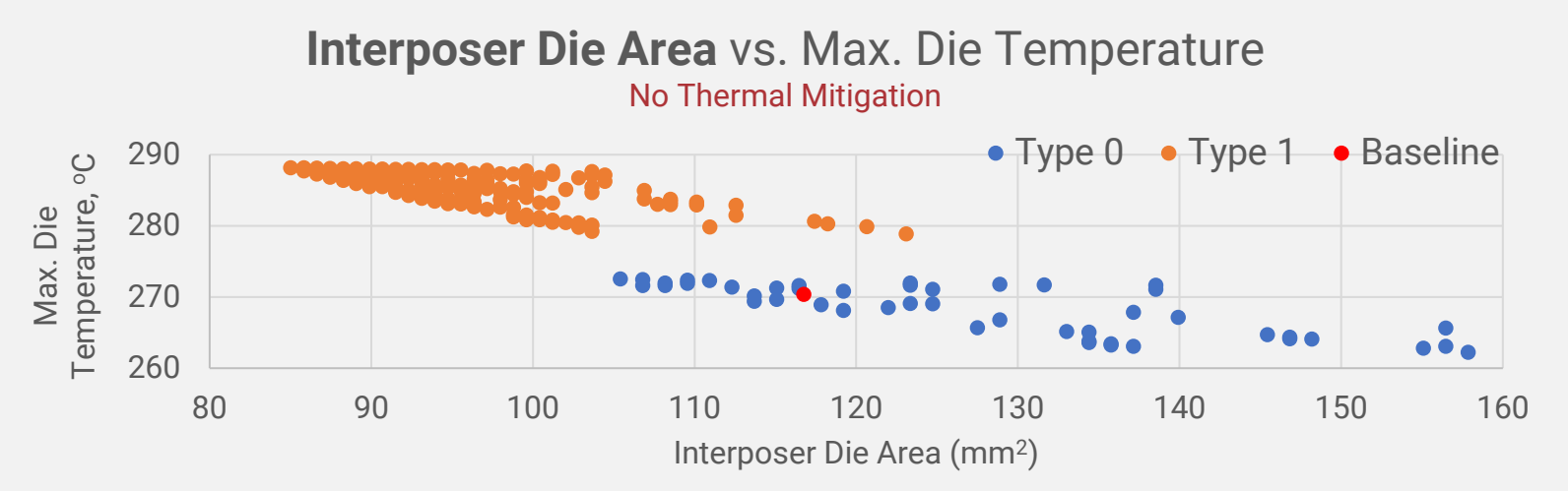


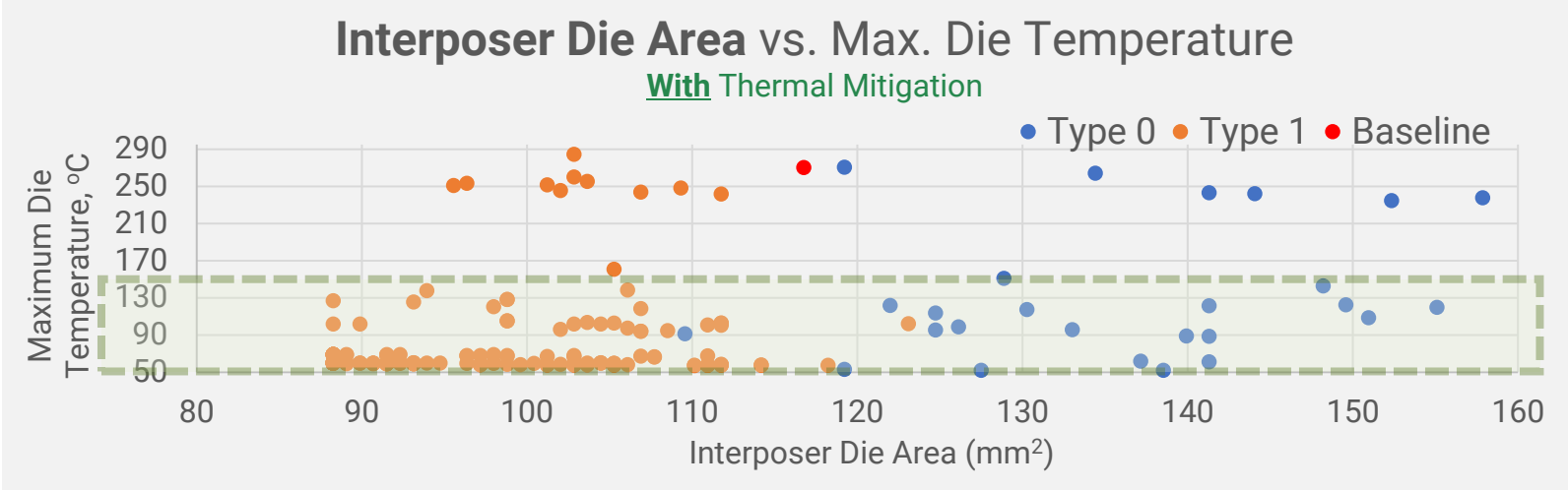
Floorplan Types



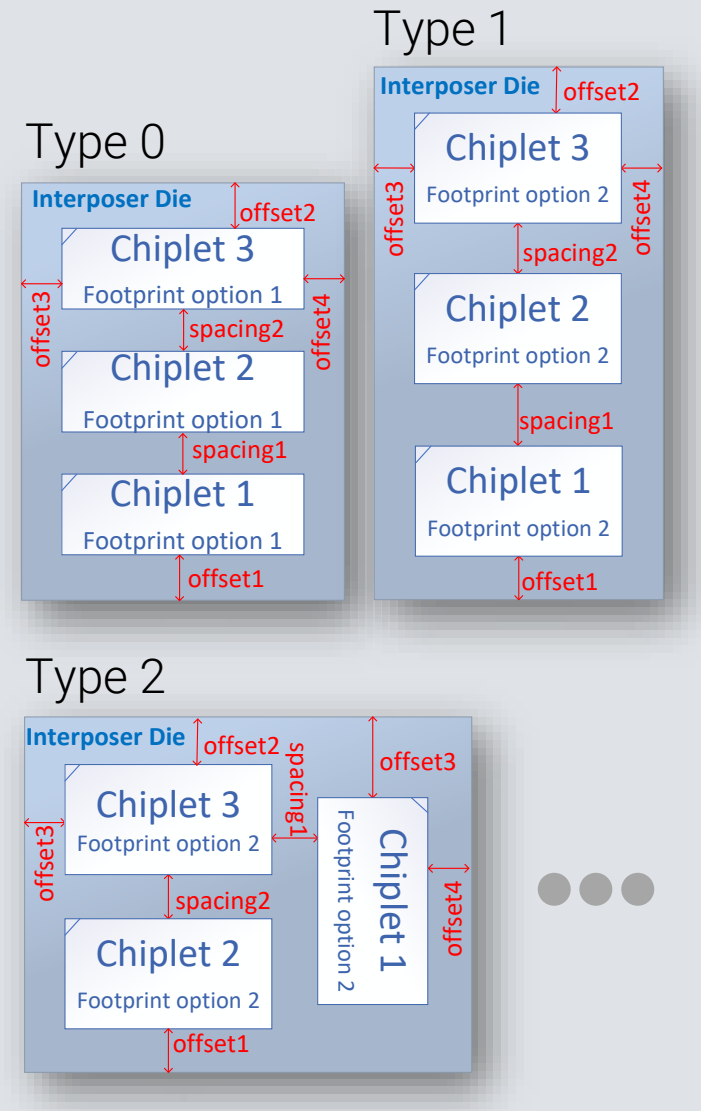
Exploring Thermal-Mitigation Options

TIM k-value, heat-spreader size, passive vs. forced cooling, …



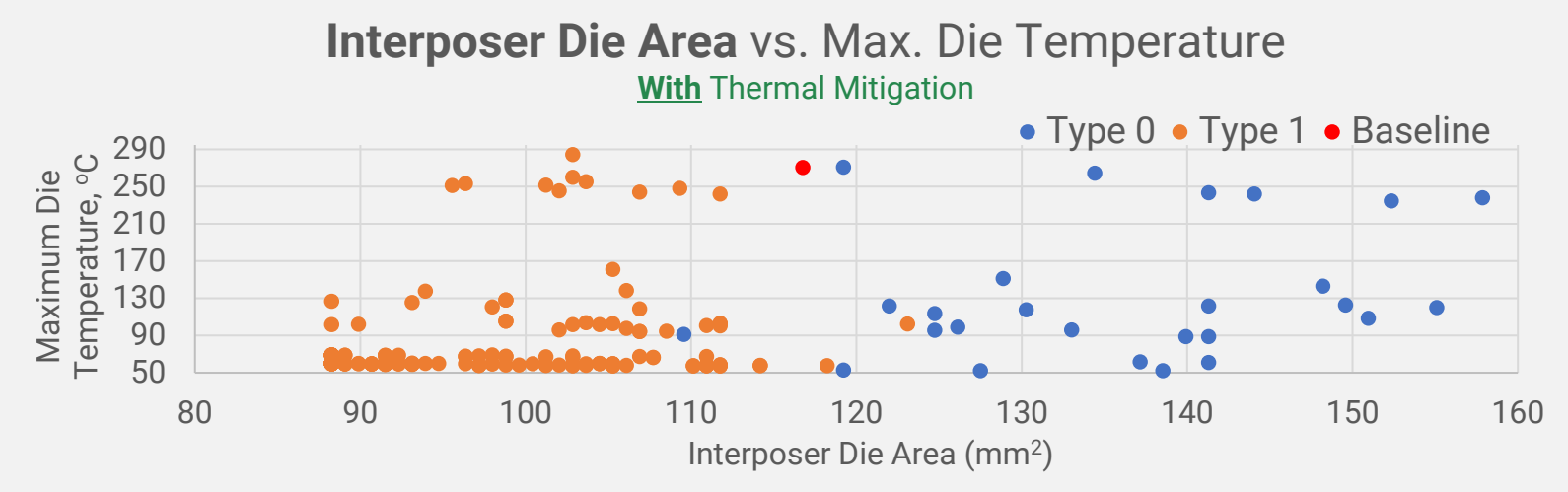


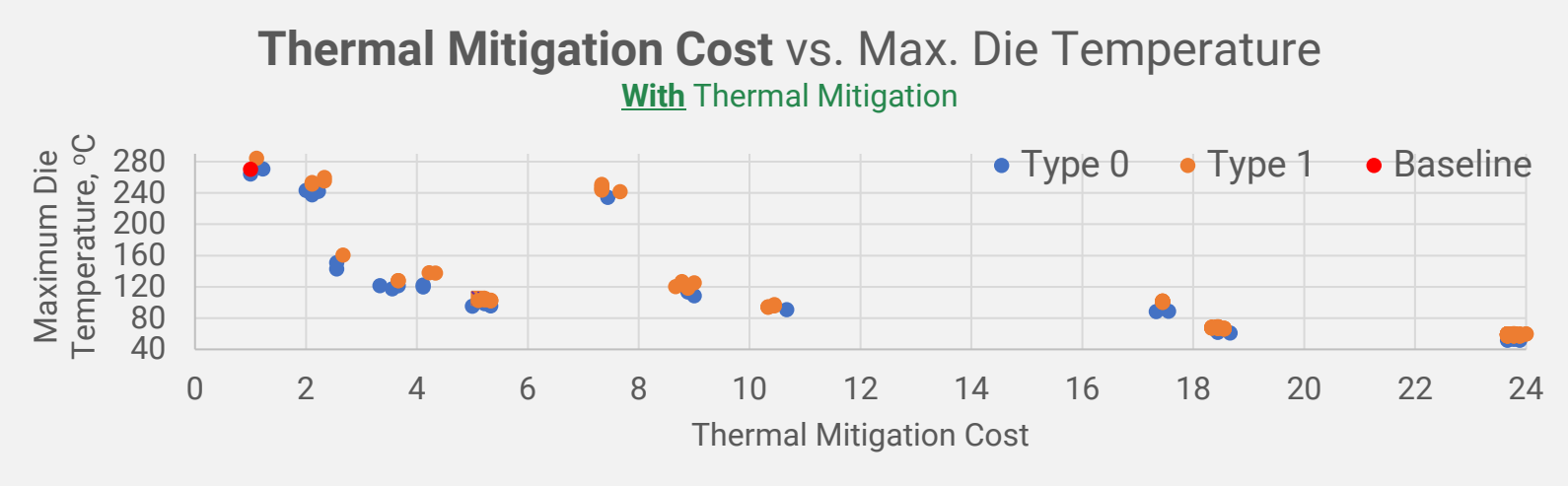
Floorplan Types



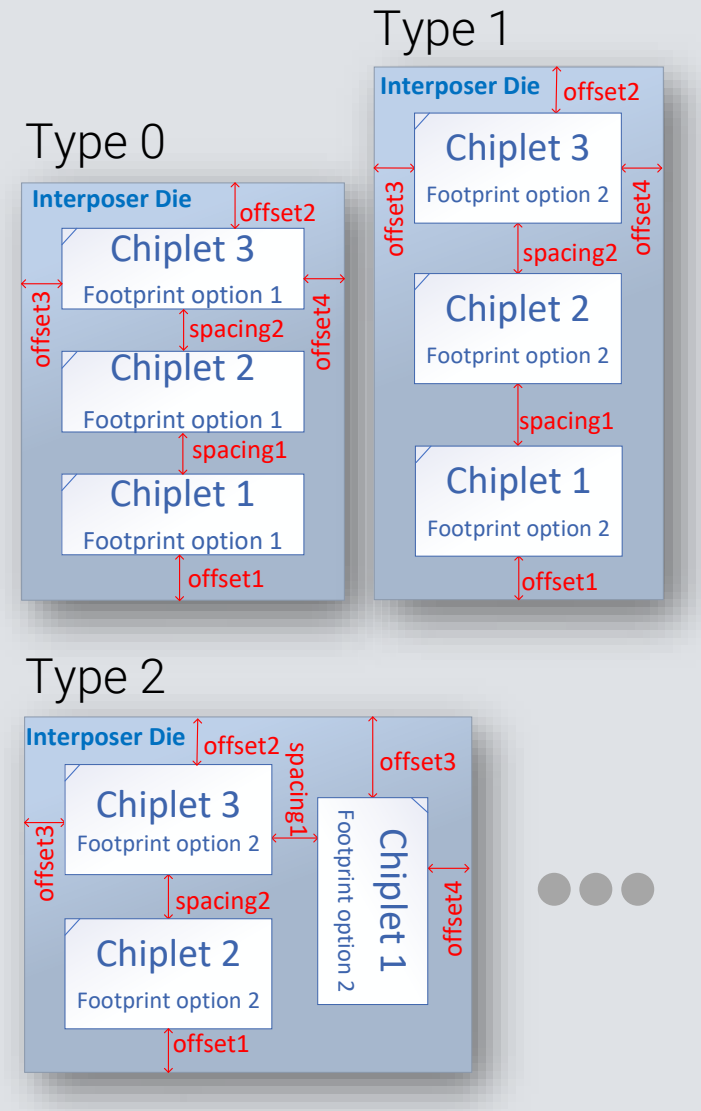
Exploring Thermal-Mitigation Options

TIM k-value, heat-spreader size, passive vs. forced cooling, …

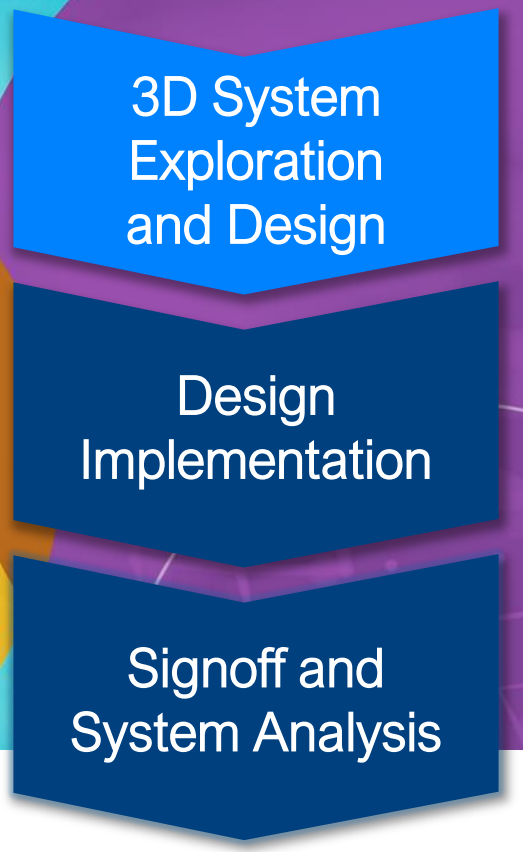




Floorplan Types

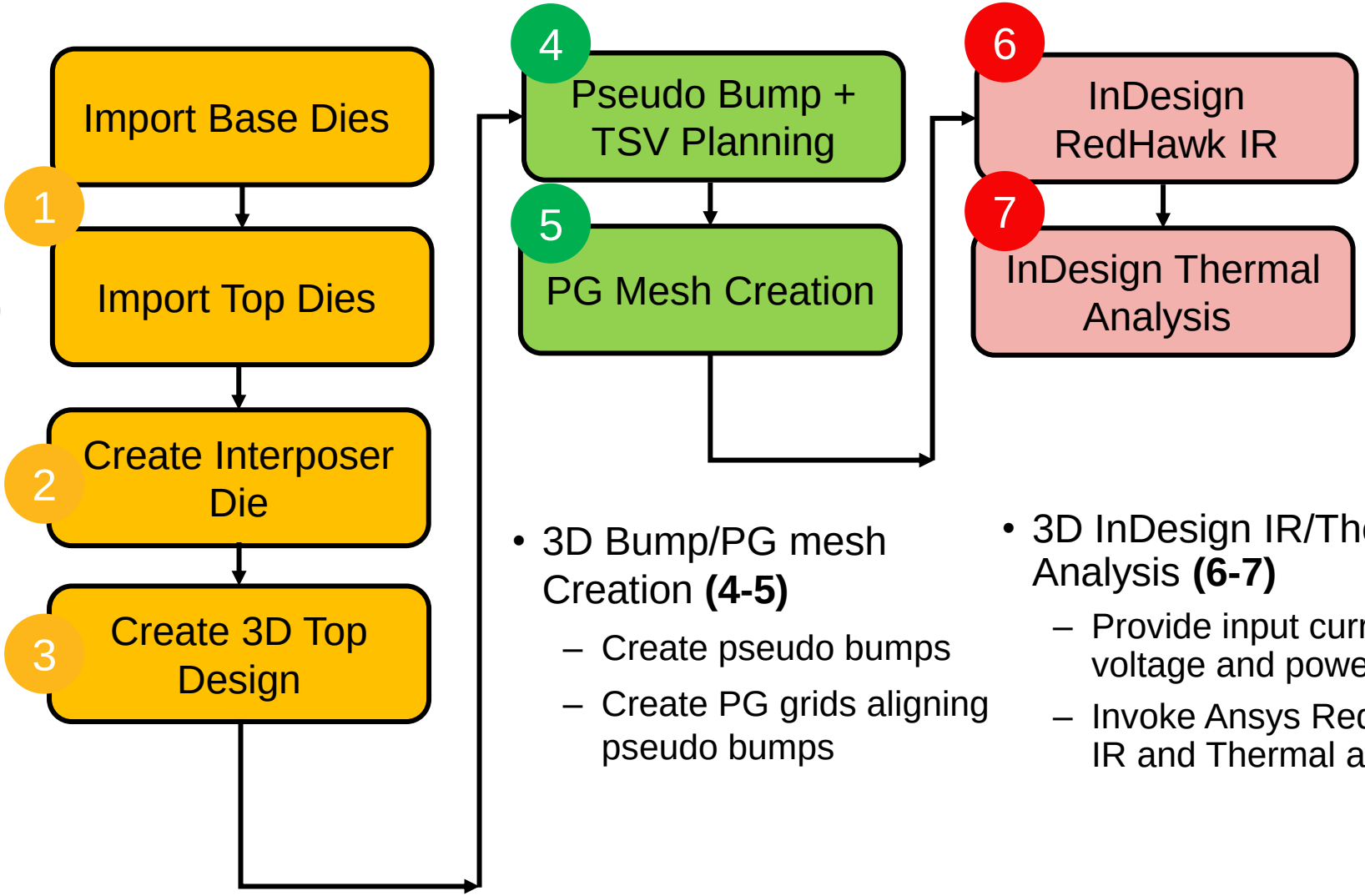


3D Prototyping Flow and Thermal Analysis Solution



3D Prototyping Flow

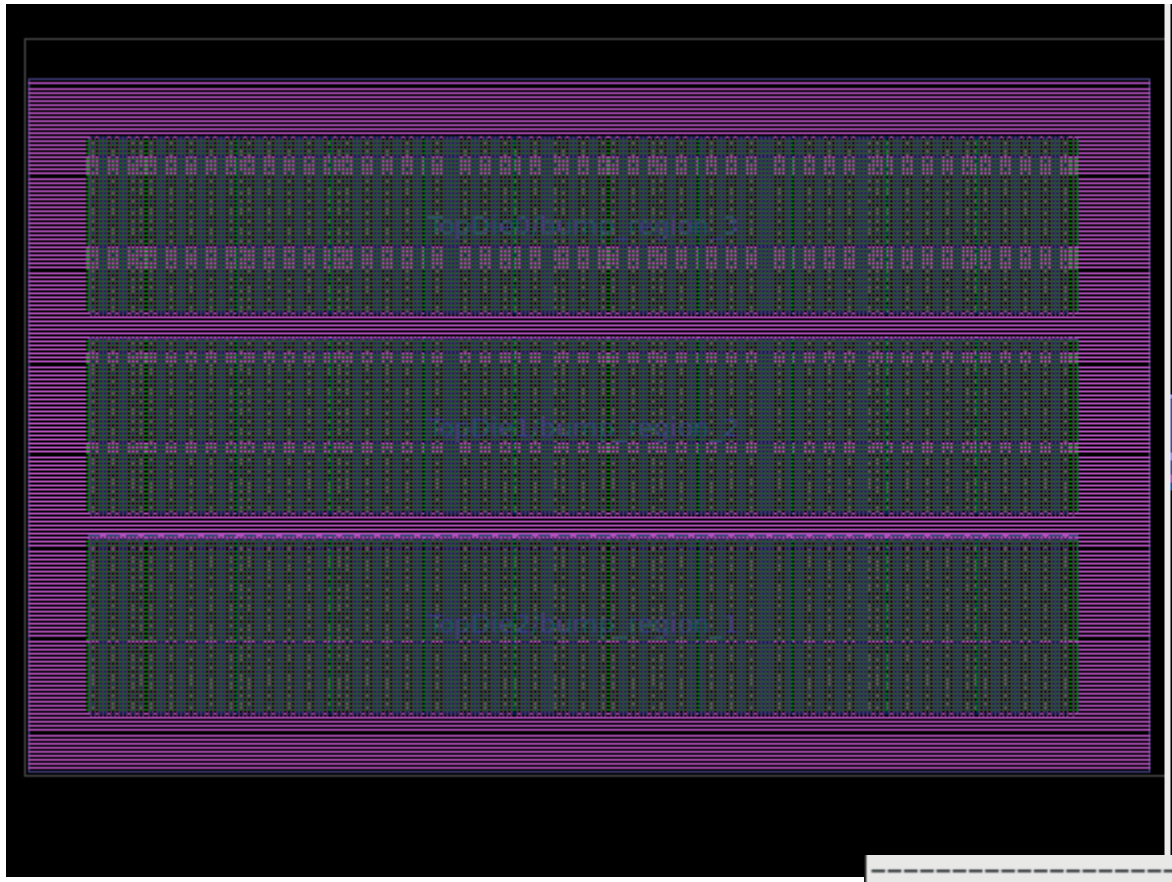
- 3D Design Creation Steps **(1-3)**
  - Base and top die referenced to pre-existing Fusion Compiler NDMs
  - Create Interposer Die
  - Build 3D Top Design with appropriate die Stacking and placement

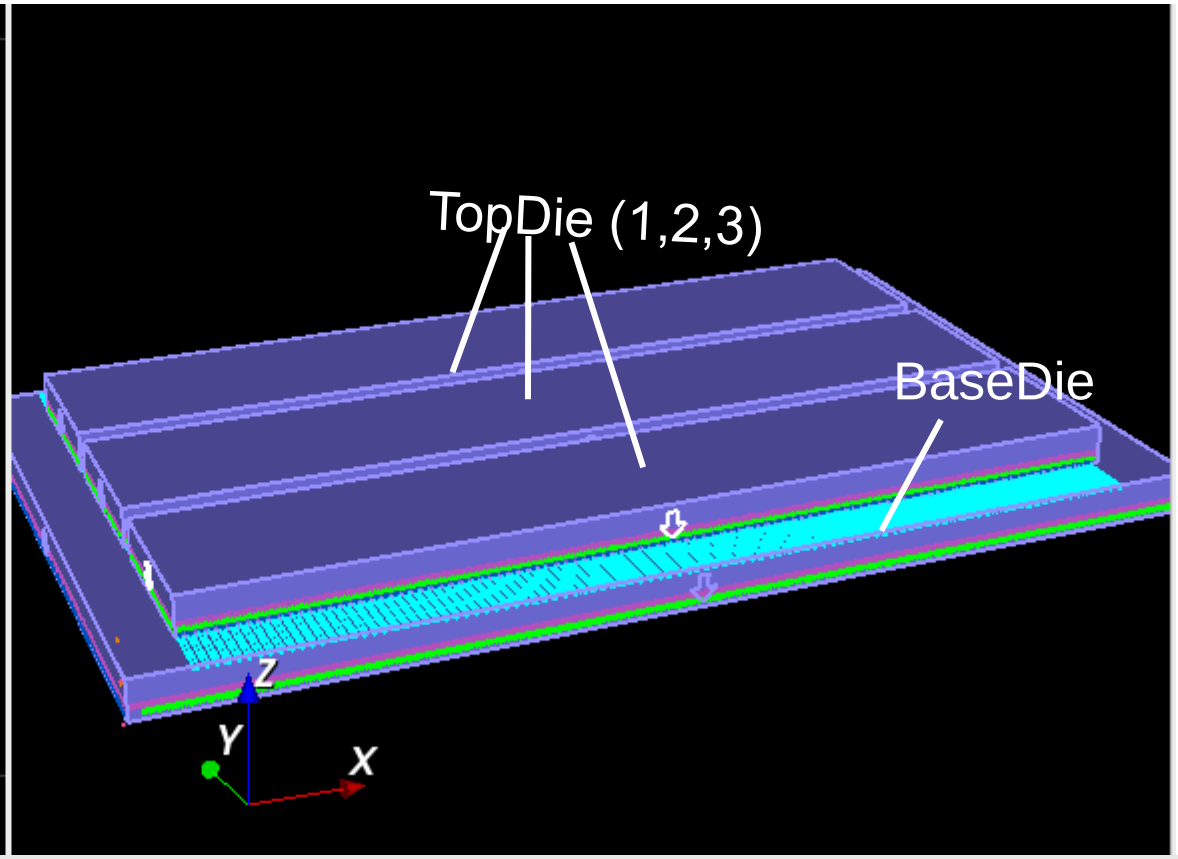


- 3D Bump/PG mesh Creation **(4-5)**
  - Create pseudo bumps
  - Create PG grids aligning pseudo bumps

- 3D InDesign IR/Thermal Analysis **(6-7)**
  - Provide input current, voltage and power info
  - Invoke Ansys Redhawk IR and Thermal analysis

3D Design Planning | 2D / 3D Views



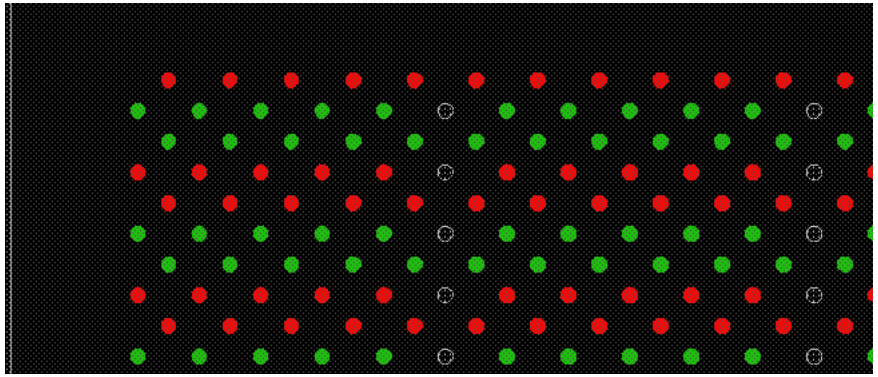


chip_name	stack_z	location	orientation	scaling_factor
TopDie0	1	(779.4540 5644.0040)	MY	1
TopDie1	1	(779.4540 3197.0700)	MY	1
TopDie2	1	(779.4540 750.1360)	MY	1
BaseDie	0	(50.0000 50.0000)	MY	1

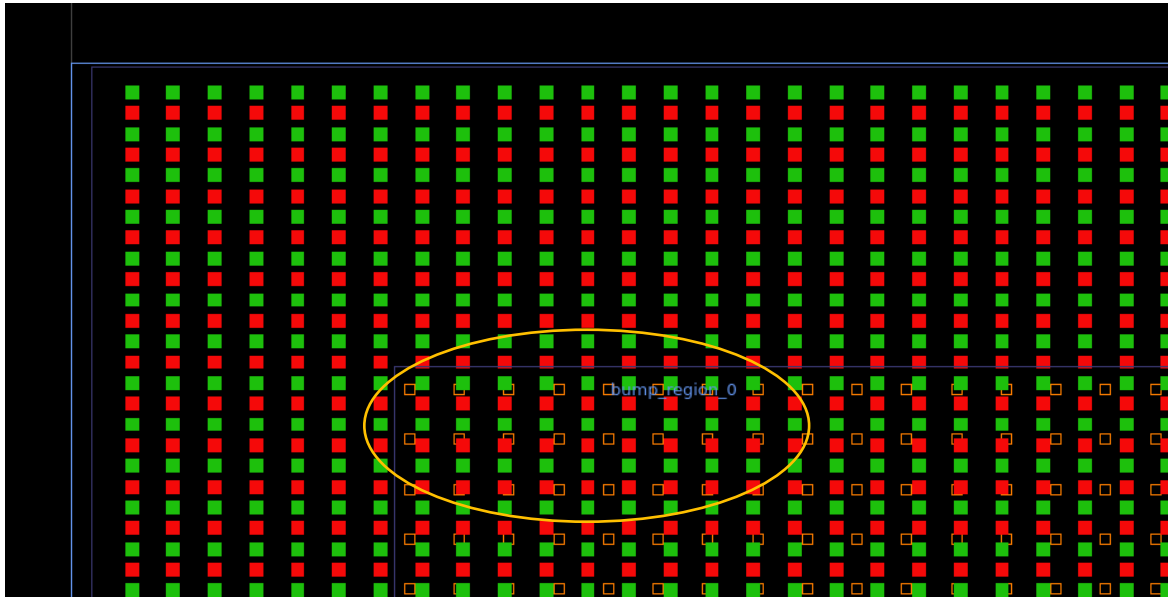
3D Design | Bump Planning Overview

Bump Arrangements

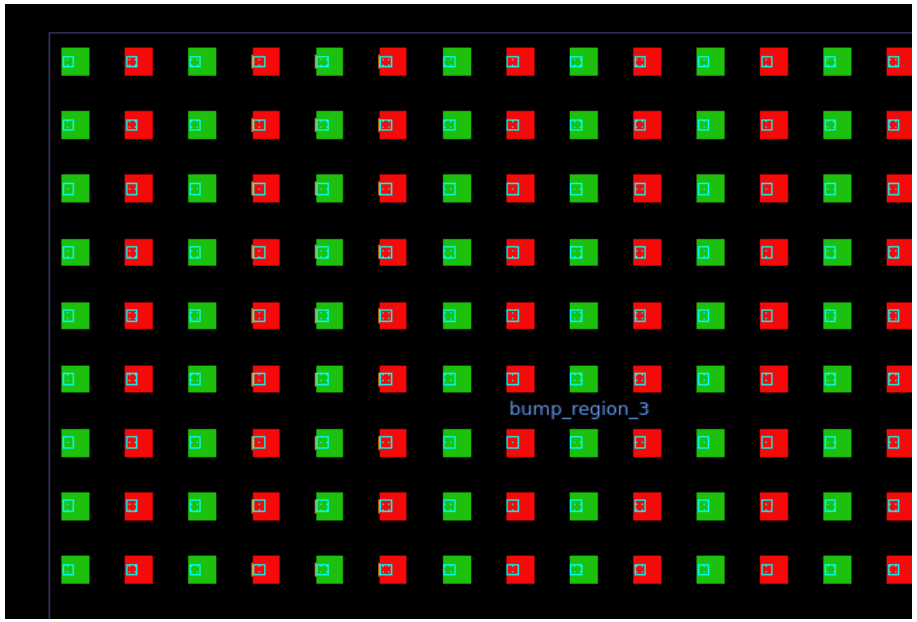
- Front side bumps in Top/Base die
- Bumps mirrored from Base Die to Top dies



Sample of PG and Signal Bumps with different styles



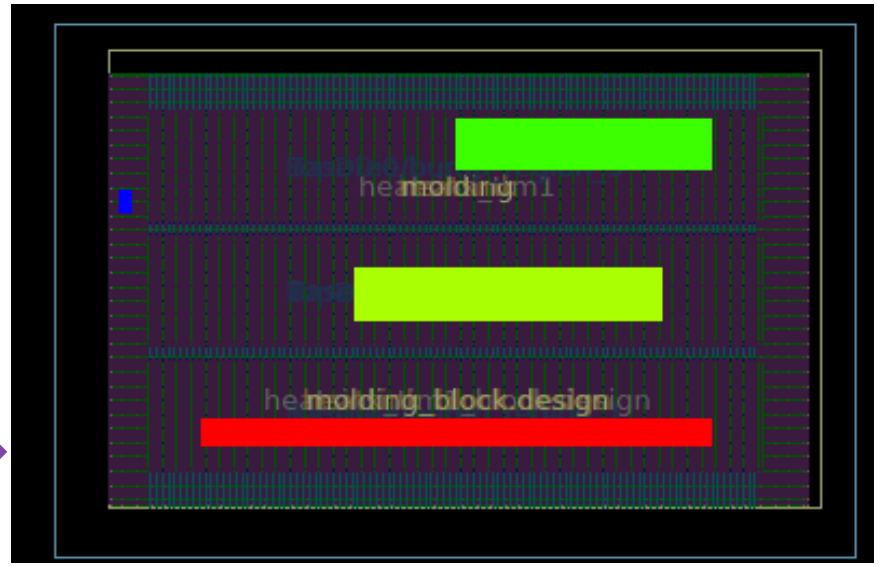
VDD/VSS frontside bumps
Pitch 100,50



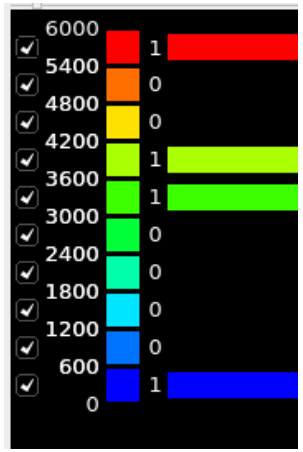
Backside Bumps shown as square shapes
Pitch of 120, 120

In-Design IR / Thermal Analysis

- Run Thermal Analysis within 3DIC shell
- Optionally read Power targets from CSV table

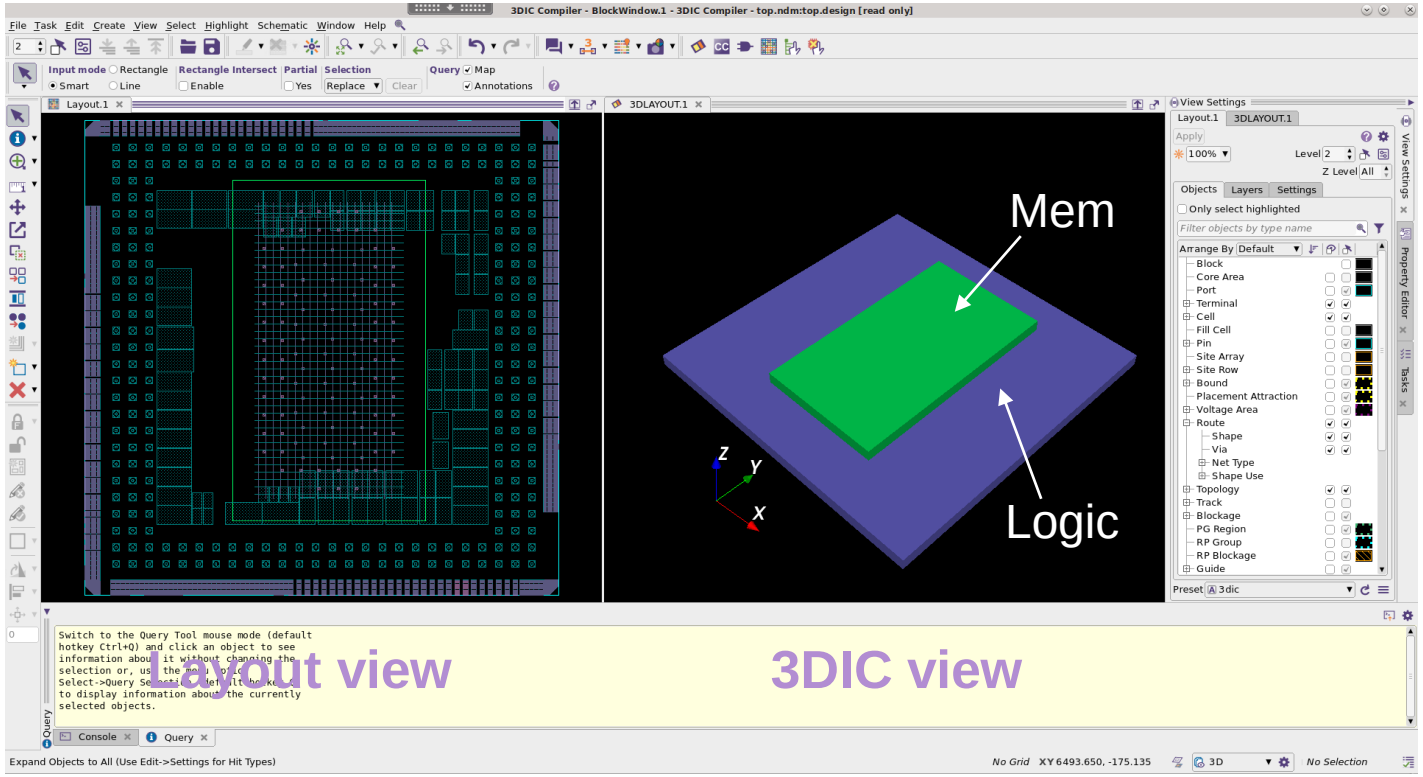


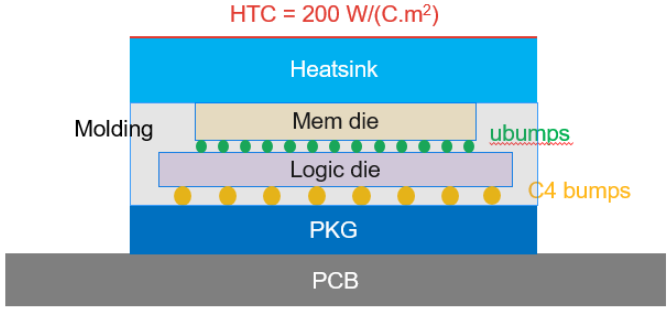
Generated Power Map



Die	Block	#Inst	Width (mm)	Height (mm)	Area (mm^2)	Mem/Phy Area %	Idle Power (W)	Peak Power (W)	Block Peak Power	Block Peak Current
Top Die 1	BLK_B	2	2	4	8	13.5	0.13	2.60	4.9	5.764705882
Top Die 1	BLK_A	1	1	4	4	72	0.08	1.60	1.4	1.647058824
Bottom Die 2	BLK_C	2	2	4	8	72	0.08	1.60	2.9	3.411764706
Bottom Die 2	BLK_D	1	1	4	4	0	0.08	1.50	1.6	1.882352941

3D Stacked Die Thermal Analysis





Side View

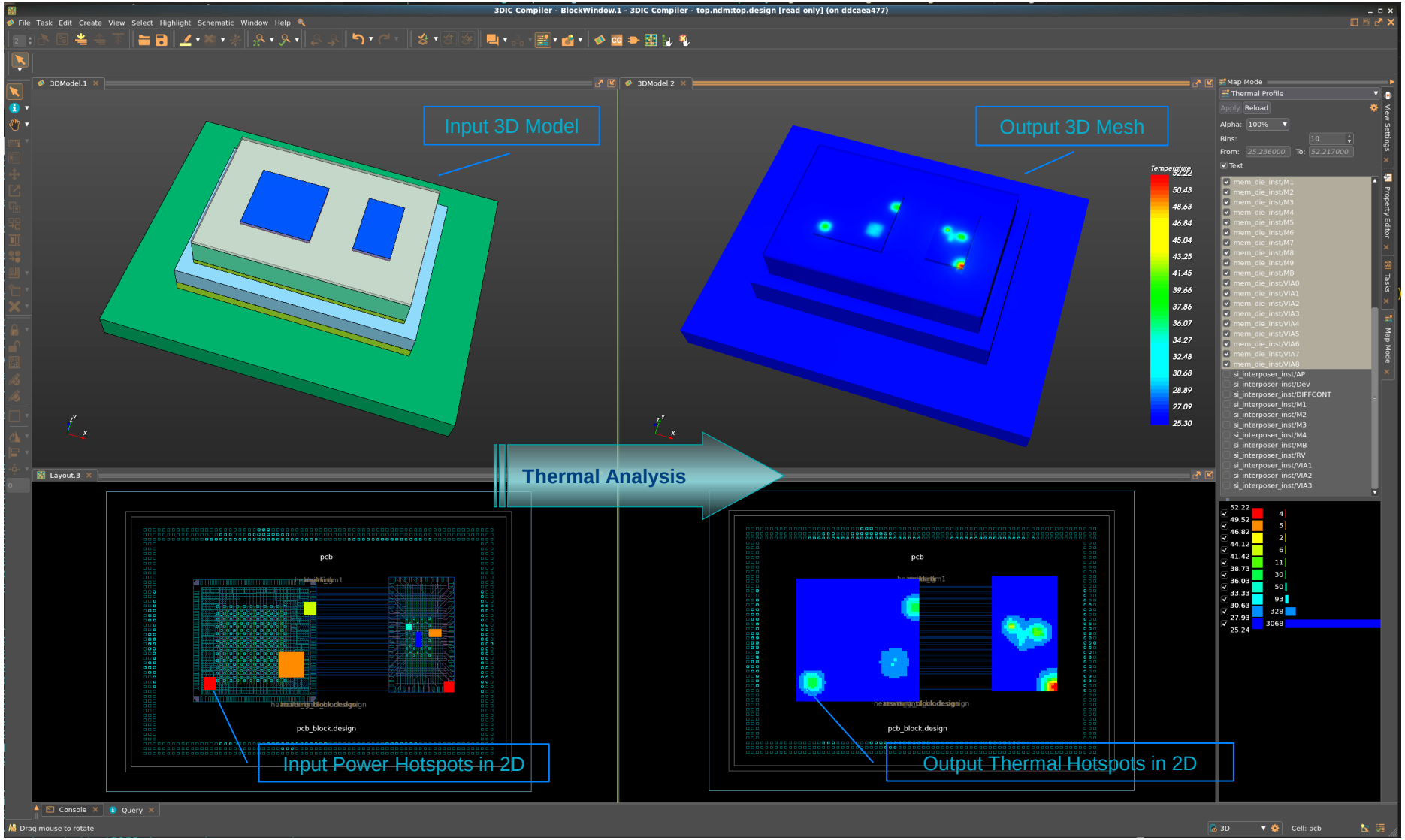
Inputs:

1. TOP.ndm design file
2. Die, C4 bumps, bonding pads thickness's
3. Template Package and PCB design layouts
4. Die power-maps
5. Analysis type: User-defined
6. Airflow: HTC: 200 W/m^{2}K
7. Ambient Temperature: 25 C

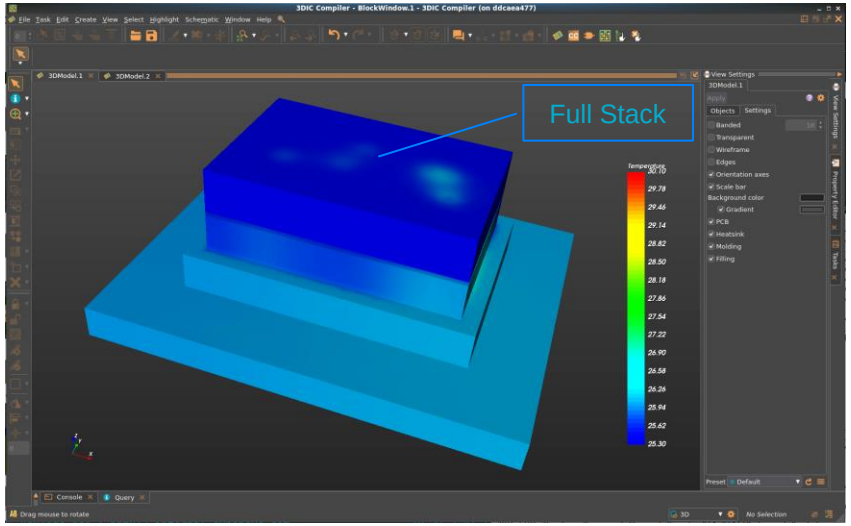
Outputs:

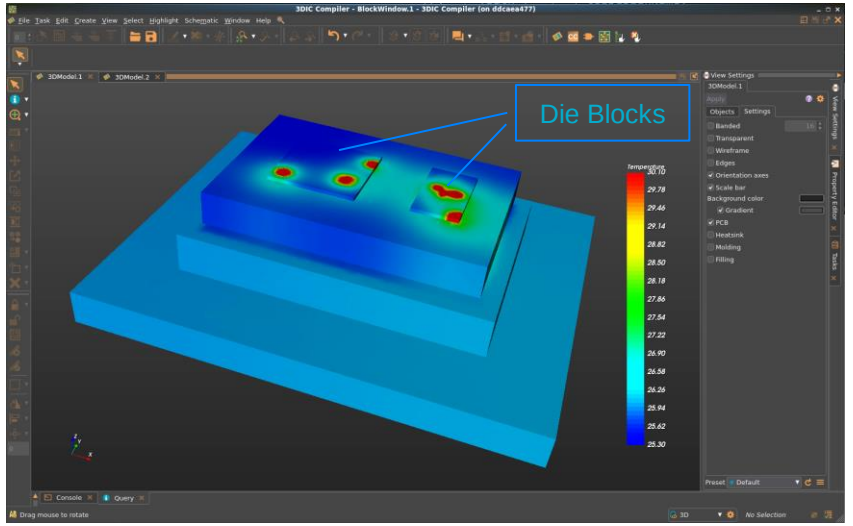
1. Nodal temperatures showing the die hotspot locations

3DIC Compiler Thermal Analysis

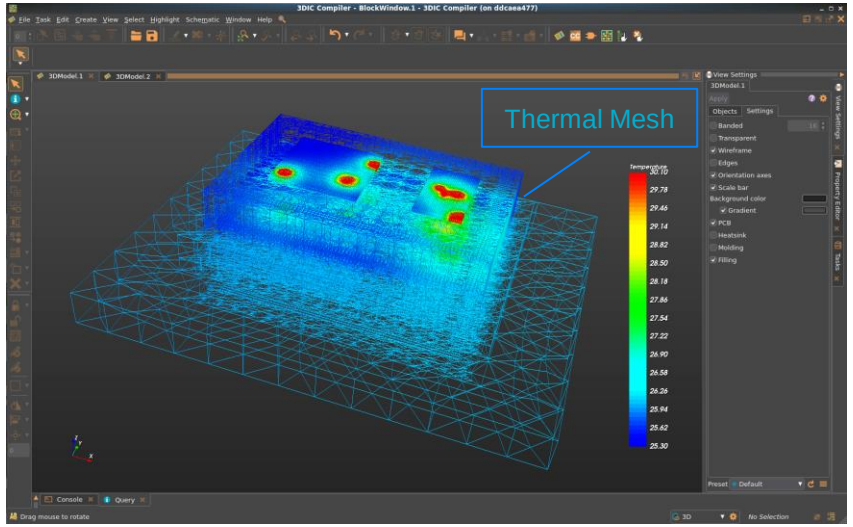


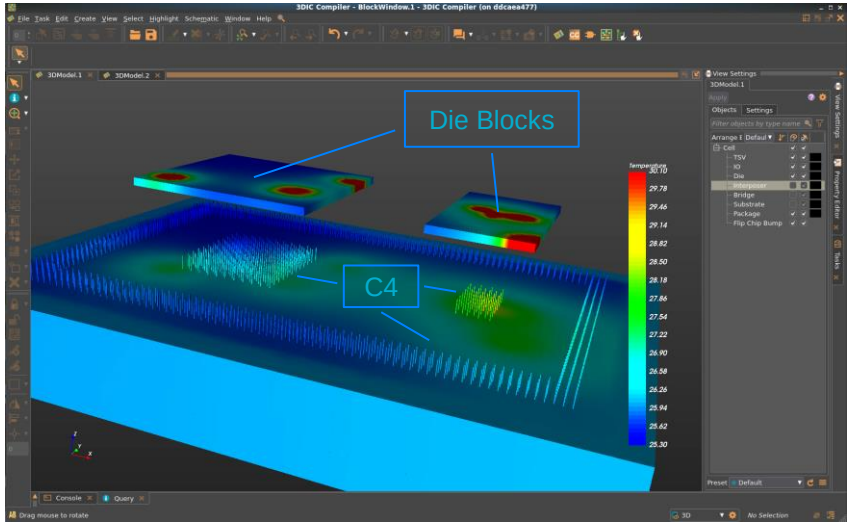
Thermal 3D Stack and Interconnect Exploration



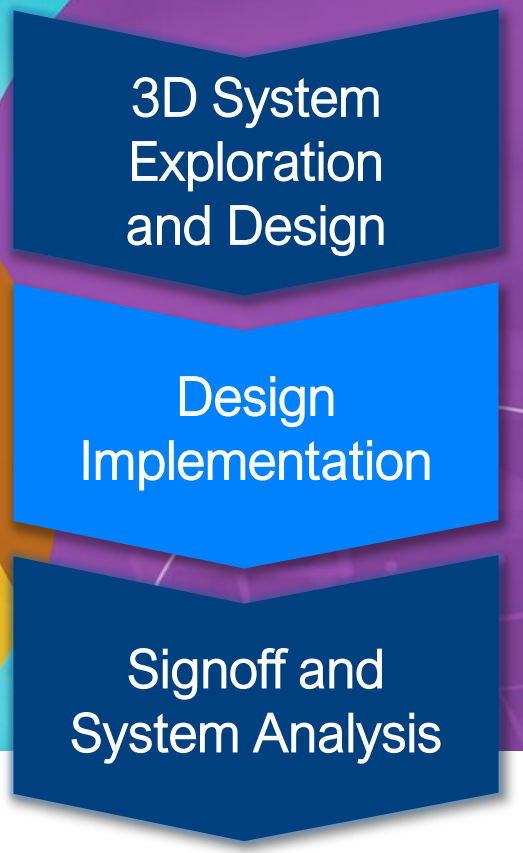


- Explore how heat transfers through the stack, find the hot spots
- Review full stack or turn on/off individual components
- Customize Min and Max Temperatures on the scale
- Inspect details of Thermal fine/coarse meshing





Scalable Solution For Multi-Die Bumps, HBs, TSVs and Fanout RDL Package



Bump / Hybrid Bump Planning Challenges

- Start without bump collateral from Foundry
- Handle wide-ranging bump pitch

	Bump Pitch	Relative Density
Hybrid Bond	10u	**900X**
ubump	40u	**56X**
C4	140u	4.6X
BGA	300u	1X

- Scale up to 50M bumps (100M+ soon)
- Support legacy bump planning flows involving MS Excel and csv
- Create correct-by-construction bump locations using mirroring

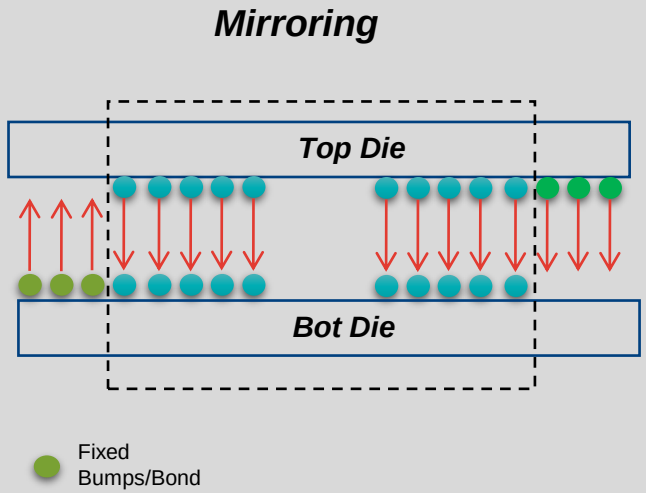
- Auto netlist derivation for interposer
- Automatic bump assignment
- Handle heterogenous optical shrink (different for different Dies) during all operations
- Diff between n and n + 1 bumps and allow accept/reject selective changes

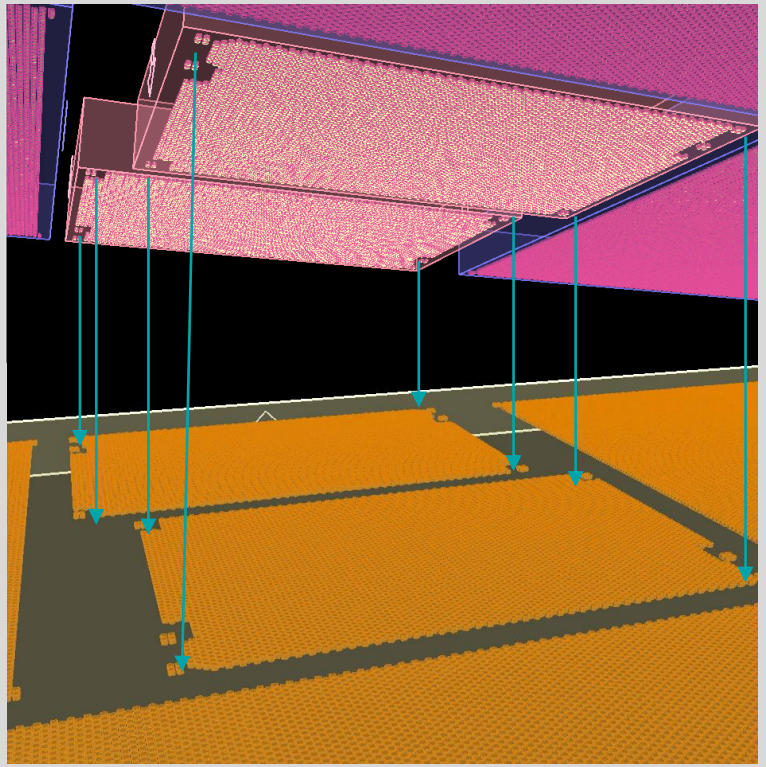
Effectively Managing Inter-Die/Package Connectivity

Bump Mirroring and Assignment

Full and selective mirroring of bumps

Assignment of bumps to port/nets



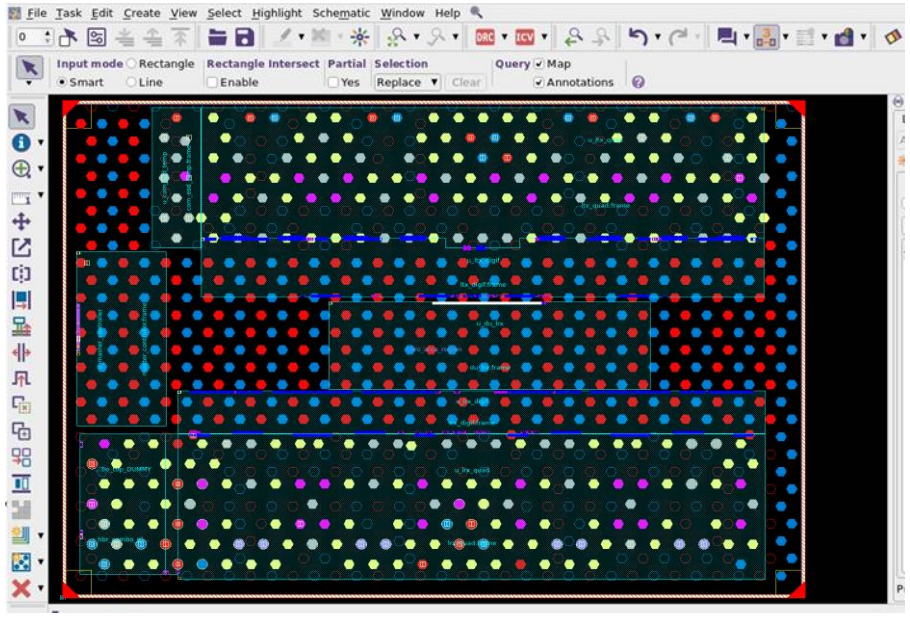


UCIe Bump Mirroring

Bump Planning

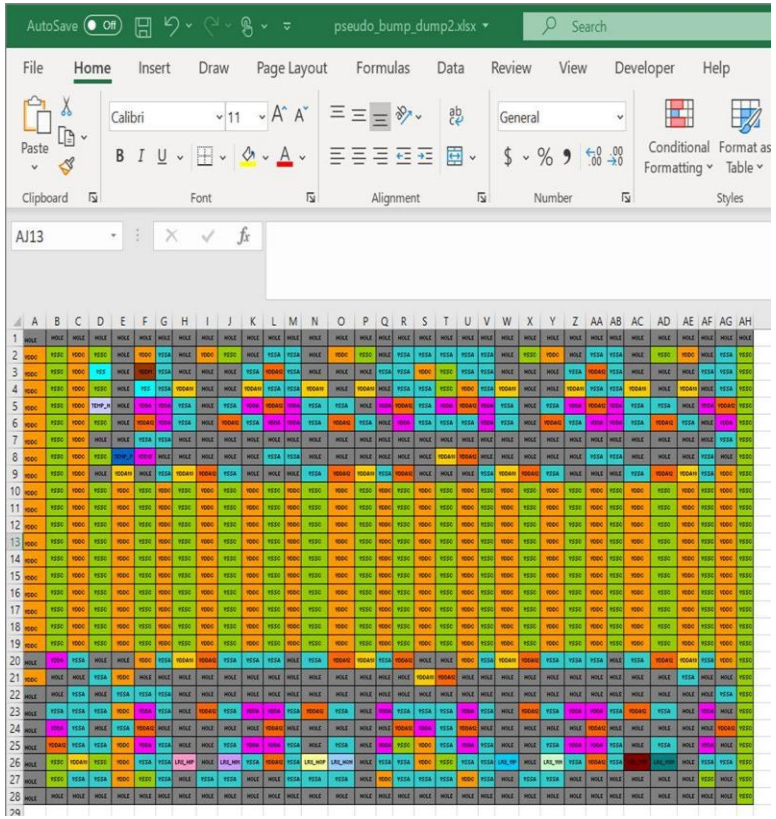
Import/Export From/to Excel and ECO

Pseudo bump creation in 3DIC



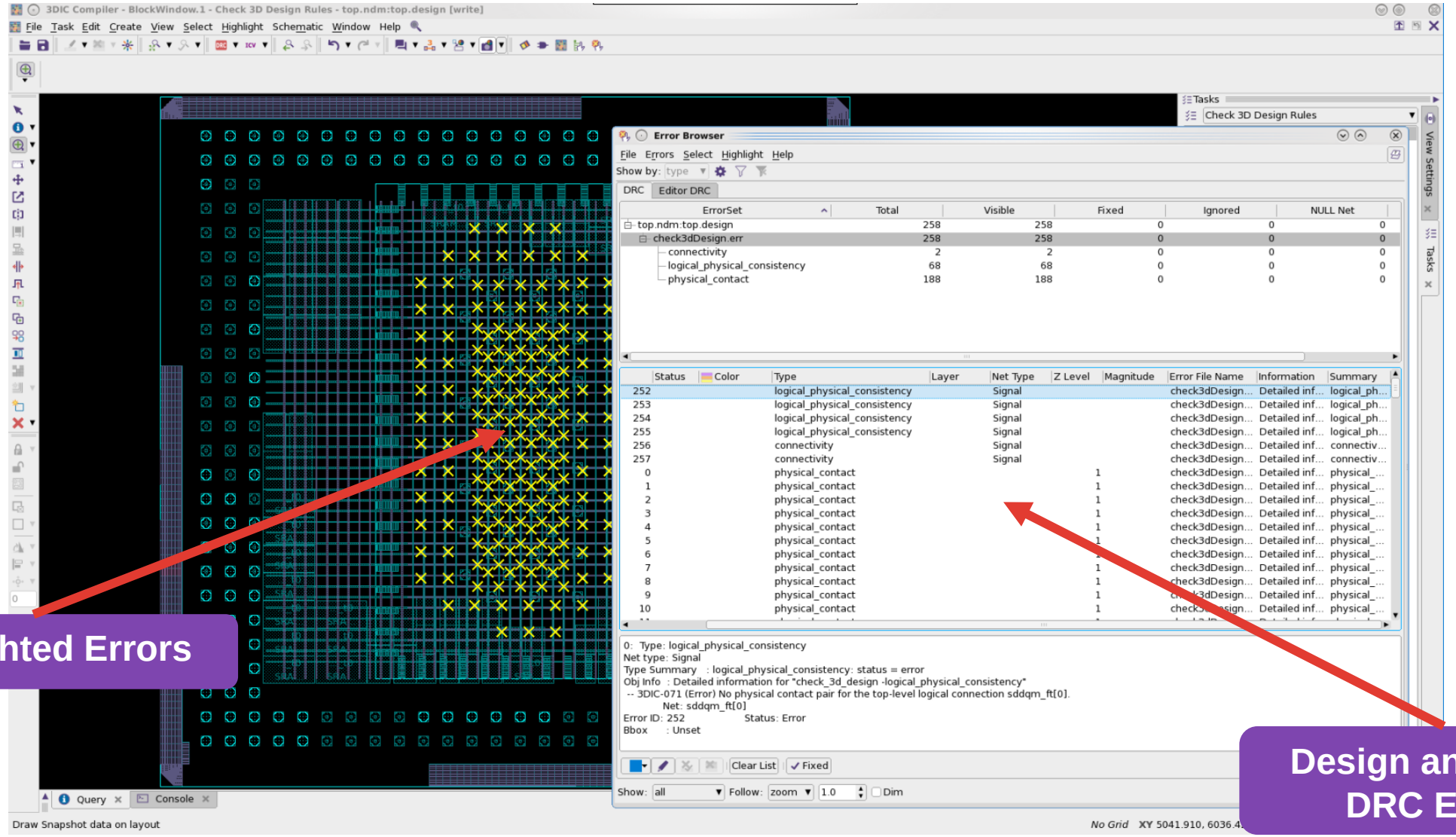
Output Bump CSV/Table

Pseudo_bump_name	is_hole	Net	X	Y	Offset_X	Offset_Y
BRPB0_0_0	TRUE	VDDC	112.797	142.68	0	0
BRPB0_1_0	TRUE	VSSC	242.797	142.68	0	0
BRPB0_2_0	TRUE	VDDC	372.797	142.68	0	0
BRPB0_3_0	TRUE	VSSC	502.797	142.68	0	0
BRPB0_4_0	TRUE	VDDC	632.797	142.68	0	0
BRPB0_5_0	TRUE	VSSC	762.797	142.68	0	0
BRPB0_6_0	TRUE	VDDC	892.797	142.68	0	0
BRPB0_7_0	TRUE	VSSC	1022.797	142.68	0	0
BRPB0_8_0	TRUE	VDDC	1152.797	142.68	0	0
BRPB0_9_0	TRUE	VSSC	1282.797	142.68	0	0
BRPB0_10_0	TRUE	VDDC	1412.797	142.68	0	0
BRPB0_11_0	TRUE	VSSC	1542.797	142.68	0	0
BRPB0_12_0	TRUE	VDDC	1672.797	142.68	0	0
BRPB0_13_0	TRUE	VSSC	1802.797	142.68	0	0
BRPB0_14_0	TRUE	VDDC	1932.797	142.68	0	0
BRPB0_15_0	TRUE	VSSC	2062.797	142.68	0	0
BRPB0_16_0	TRUE	VDDC	2192.797	142.68	0	0
BRPB0_17_0	TRUE	VSSC	2322.797	142.68	0	0
BRPB0_18_0	TRUE	VDDC	2452.797	142.68	0	0
BRPB0_19_0	TRUE	VSSC	2582.797	142.68	0	0
BRPB0_20_0	TRUE	VDDC	2712.797	142.68	0	0
BRPB0_21_0	TRUE	VSSC	2842.797	142.68	0	0
BRPB0_22_0	TRUE	VDDC	2972.797	142.68	0	0
BRPB0_23_0	TRUE	VSSC	3102.797	142.68	0	0
BRPB0_24_0	TRUE	VDDC	3232.797	142.68	0	0
BRPB0_25_0	TRUE	VSSC	3362.797	142.68	0	0
BRPB0_26_0	TRUE	VDDC	3492.797	142.68	0	0
BRPB0_27_0	TRUE	VSSC	3622.797	142.68	0	0
BRPB0_28_0	TRUE	VDDC	3752.797	142.68	0	0
BRPB0_29_0	TRUE	VSSC	3882.797	142.68	0	0
BRPB0_30_0	TRUE	VDDC	4012.797	142.68	0	0
BRPB0_31_0	TRUE	VSSC	4142.797	142.68	0	0
BRPB0_32_0	TRUE	VDDC	4272.797	142.68	0	0
BRPB0_33_0	FALSE	VSSC	4402.797	142.68	0	0
BRPB0_0_1	TRUE	VDDC	112.797	272.68	0	0
BRPB0_1_1	FALSE	VSSC	256.9095	218.047	14.1125	-54.633
BRPB0_2_1	FALSE	VSSA	406.8495	218.047	34.0525	-54.633
BRPB0_3_1	FALSE	VSSA	556.7895	218.047	53.9925	-54.633
BRPB0_4_1	TRUE	VDDC	632.797	272.68	0	0
BRPB0_5_1	FALSE	VSSC	706.7295	218.047	-56.0675	-54.633
BRPB0_6_1	FALSE	VDDC	856.6695	218.047	-36.1275	-54.633
BRPB0_7_1	FALSE	VSSA	1006.61	218.047	-16.1875	-54.633
BRPB0_8_1	FALSE	VSSA	1156.55	218.047	3.7525	-54.633
BRPB0_9_1	FALSE	VSSA	1306.49	218.047	23.6925	-54.633
BRPB0_10_1	TRUE	VDDC	1412.797	272.68	0	0



Graphical Excel Spreadsheet

Design And Bump Checking



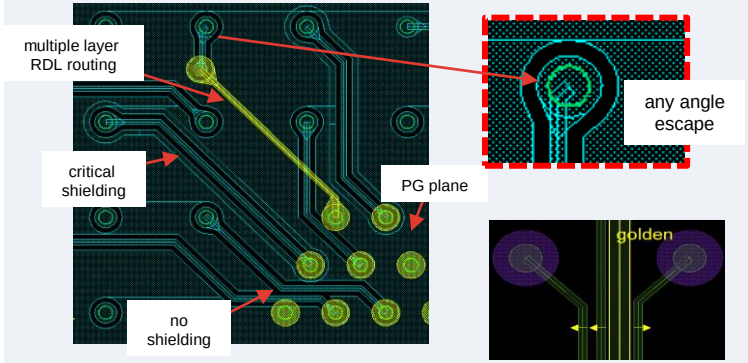
Highlighted Errors

Design and Bump DRC Errors

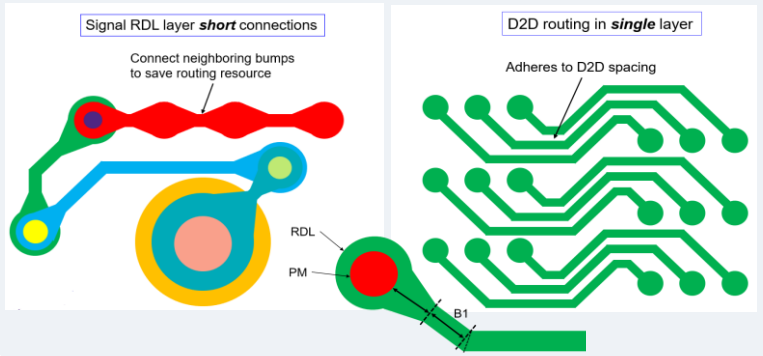
Unique Automated Solution for Fanout RDL

Industry's Fastest Multi-Layer DRC-Aware Wafer Level Packaging Solution

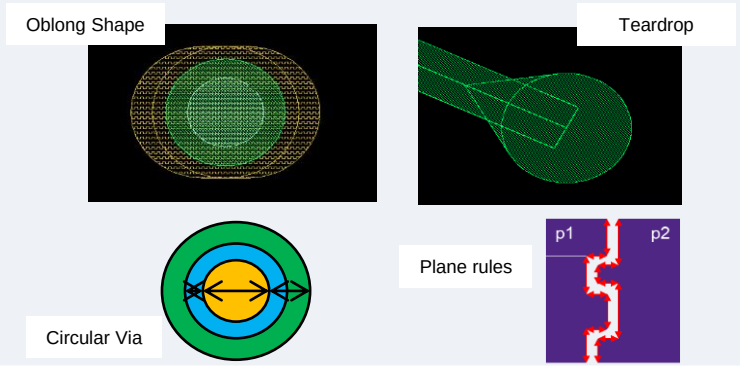
Automated/Interactive Routing



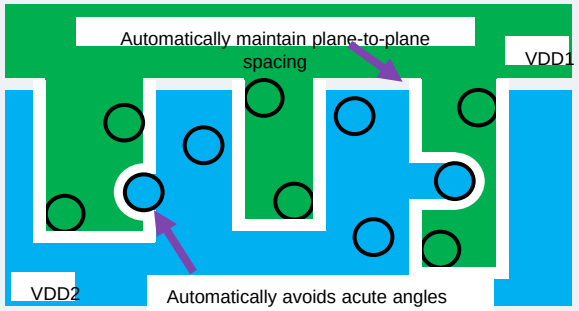
D2D Routing



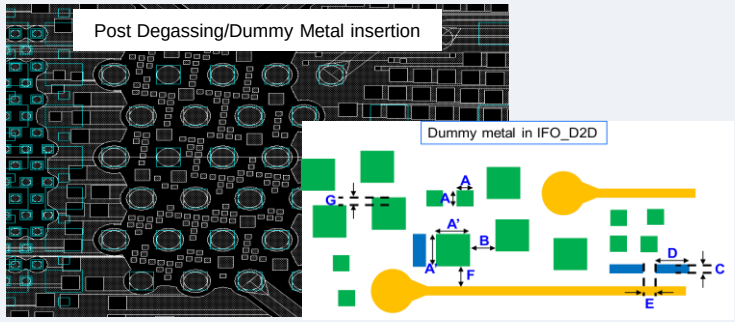
Fanout Shapes



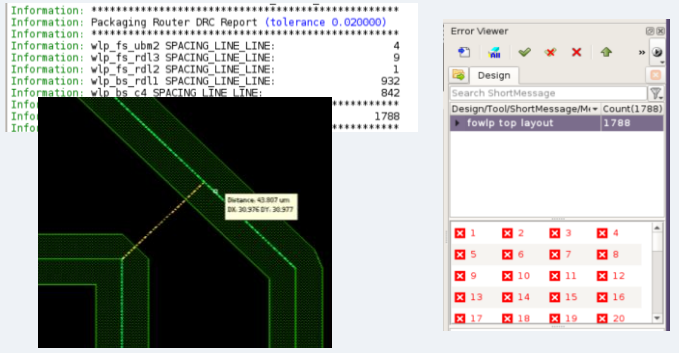
Plane Realization



Substrate Degassing

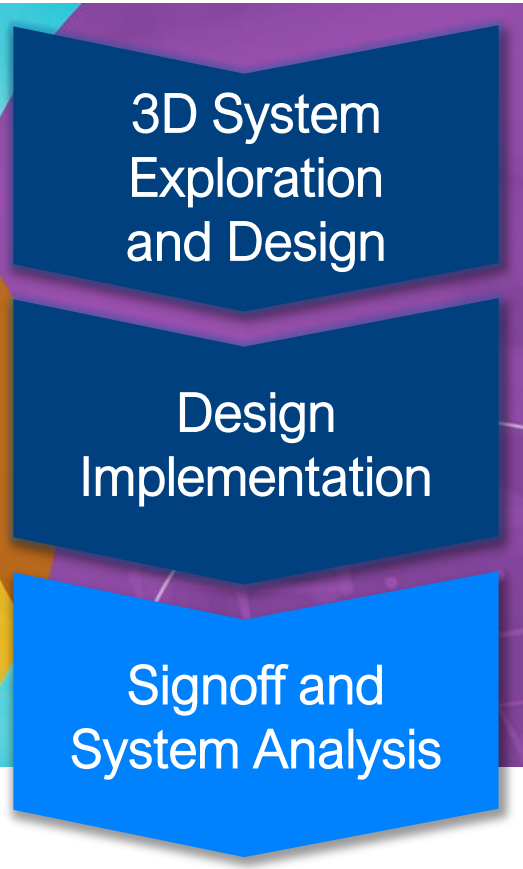


RDL DRC & LVS



Multi-Die In-Design and Signoff Analysis

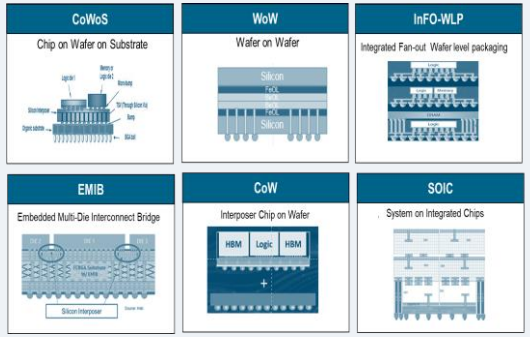
Aided by correct by construction data
from 3DIC Compiler



Full-Spectrum Signoff Analysis

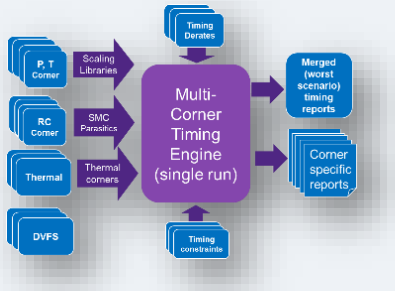
In-Design Multi-Die analysis delivers productivity coupled with full signoff accuracy

Extraction



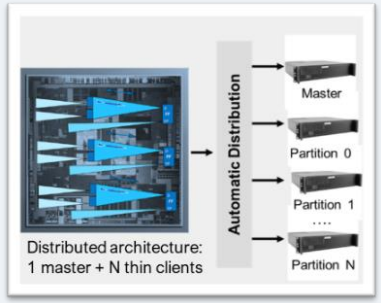
3D Stack/BS, PG and interposer extraction

Static Timing Analysis



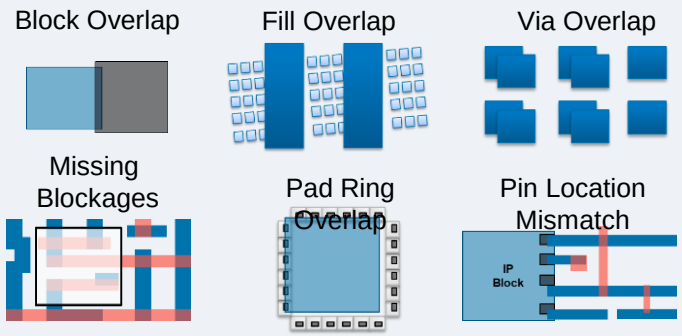
Simultaneous Multi-Corner Analysis

Hypergrid Distributed Analysis

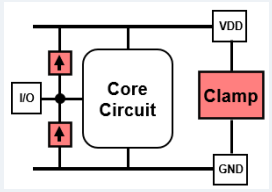


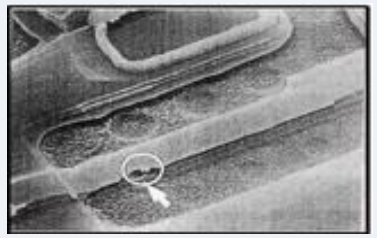
Run 3D STA on billions of instances in hours

DRC/LVS



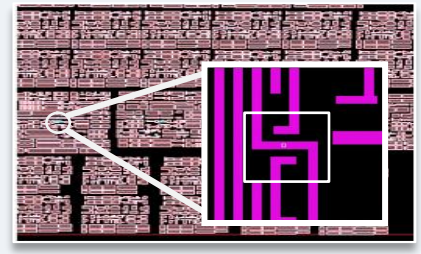
ESD





Topology, CD/P2P Perc, HBM/CDM analysis

ECO



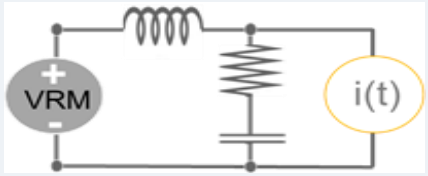
Ultrafast, DRC & Fill ECO within minutes

In-design analysis may require additional product licensing

Multiphysics Analysis together with Ansys

In-Design Multi-Die/Package analysis and modeling

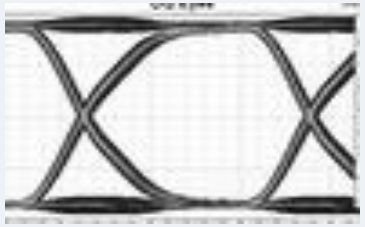
Power Integrity



Power Delivery Network vs. Performance

Physics Coupling

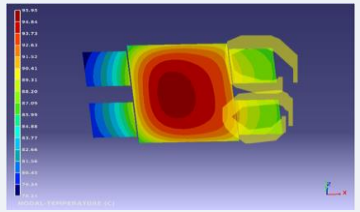
Signal Integrity



Routing Interconnect vs. High-Speed Performance

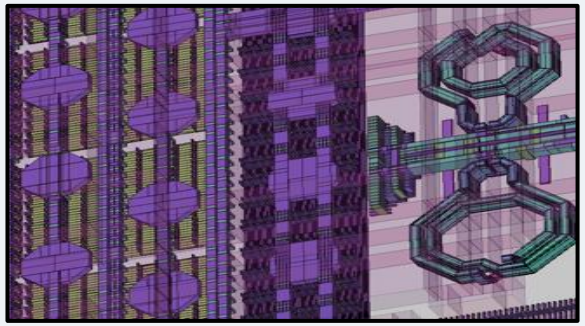
Physics Coupling

Thermal Integrity

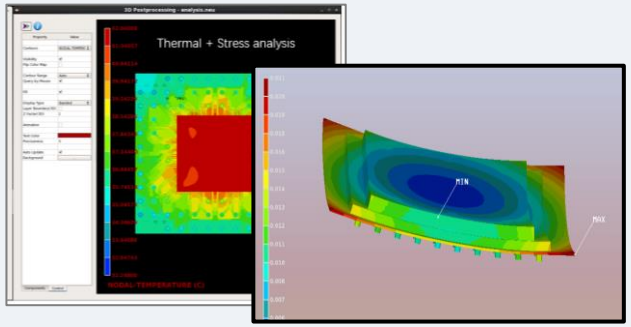


Power/Heat Dissipation vs. Reliability

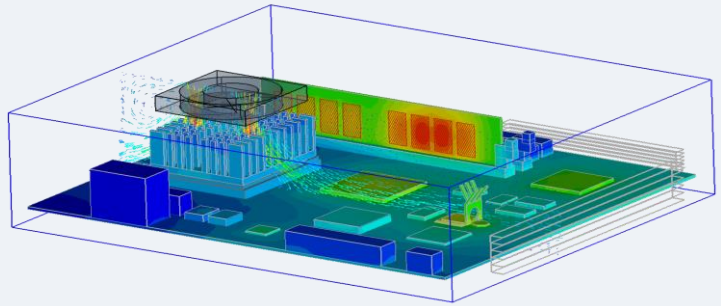
EM Coupling & Interference



Mechanical Stress & Warpage



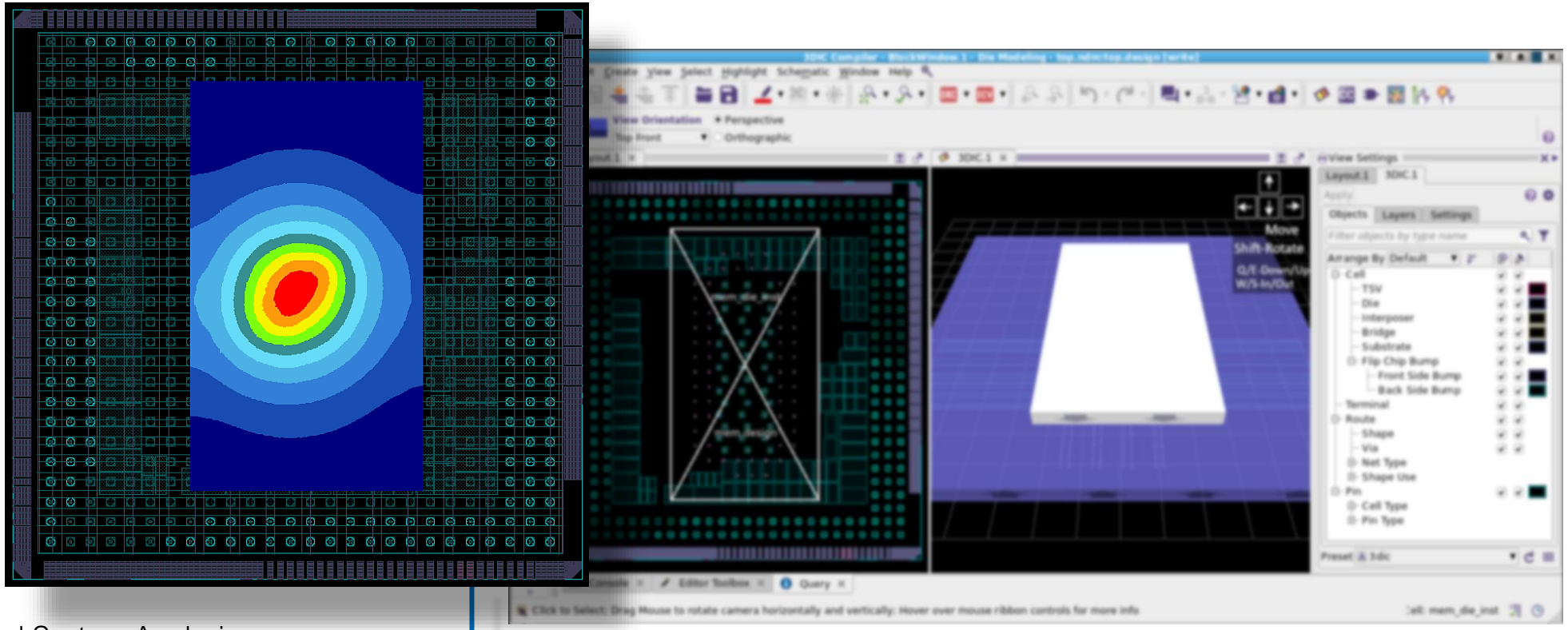
System Thermal



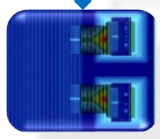
In-design analysis may require additional product licensing

3DIC Compiler System Analysis

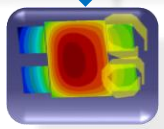
Industry Keystone Analysis Engines From Within The Design Process



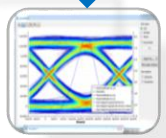
Integrated System Analysis



3DIC EMIR
Ansys Redhawk SC



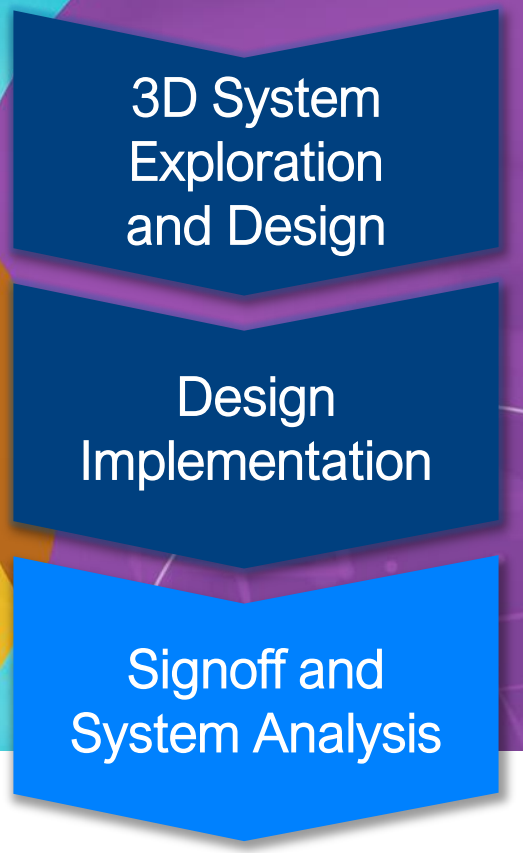
3DIC Thermal
Ansys Redhawk SC-ET



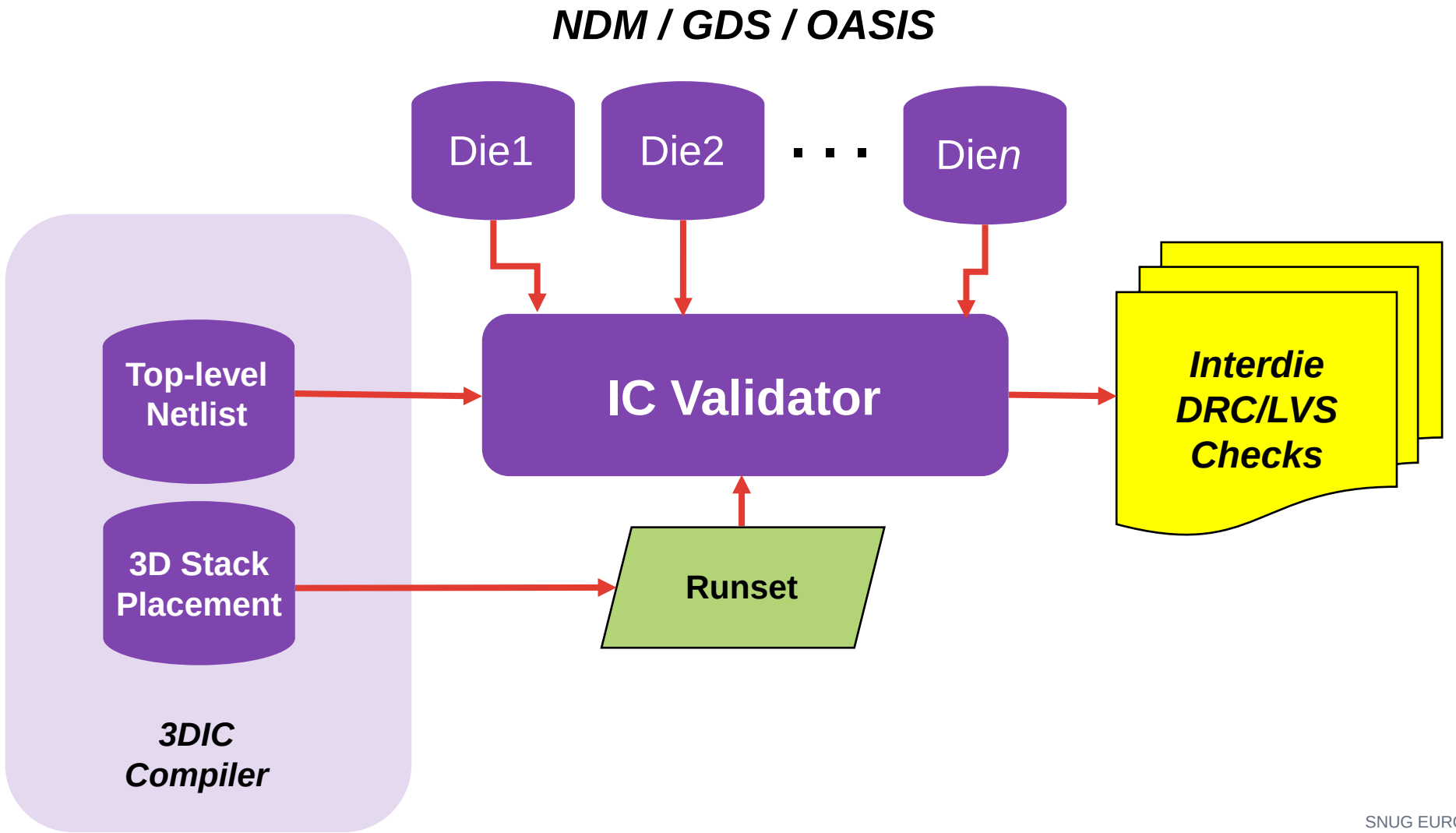
High Frequency EMag Extraction
Ansys HFSS

3D Verification / DRC Checks

In-Design Multi-Die Checking



3DIC Compiler Multi-Die DRC/LVS Verification Flow: Synopsys IC Validator

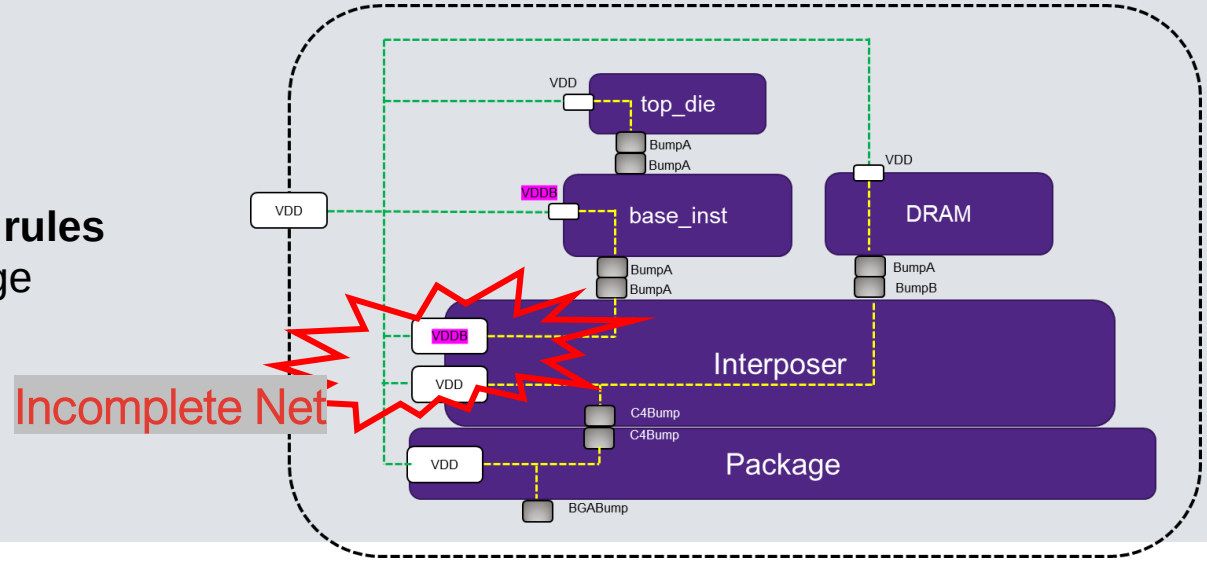


Native 3D Stack Verification

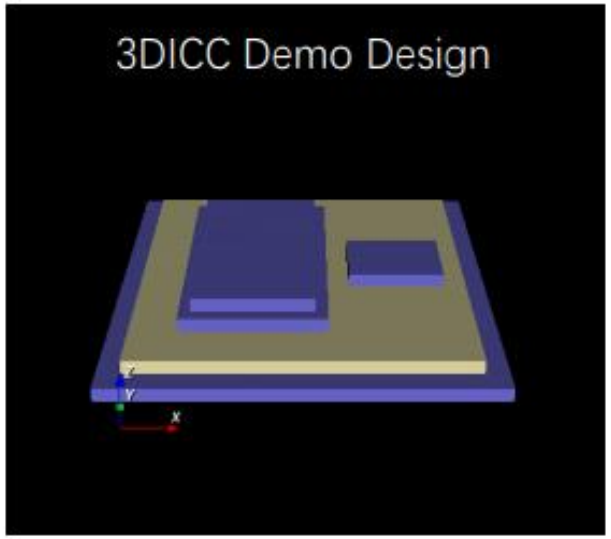
Correct-by-construction Heterogeneous Integration

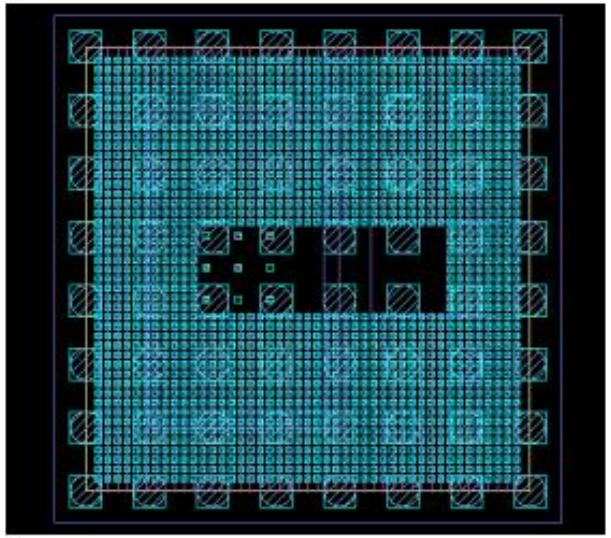
- **Physical DRC for die-die interface and PG**
  - Die/pin/bump overlaps, missing / extra bumps, die alignment,..
  - Bad bump patterns, PG wires,..
  - Placement, spacing, enclosure,..
  - Account for scaling and orientation
- **Logical and physical connectivity LVS**
  - Logical connected/physical disconnected
  - Design open/shorts, text labels mismatches,..
  - PG open/shorts, PG wires,..
  - Support the entire die-die-interposer-package stack,..
- **Over 60 heterogeneous design integration and assembly rules**
  - Extends 2D to 3D with 3DIC Compiler Multi-Die Exchange Format

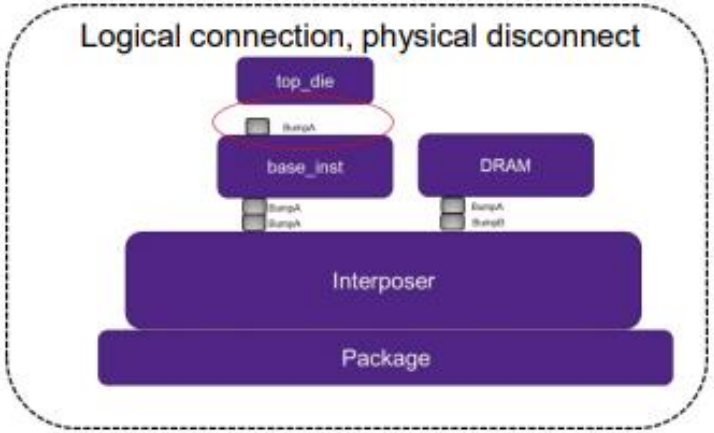
3D Visualization of DRC/LVS violations

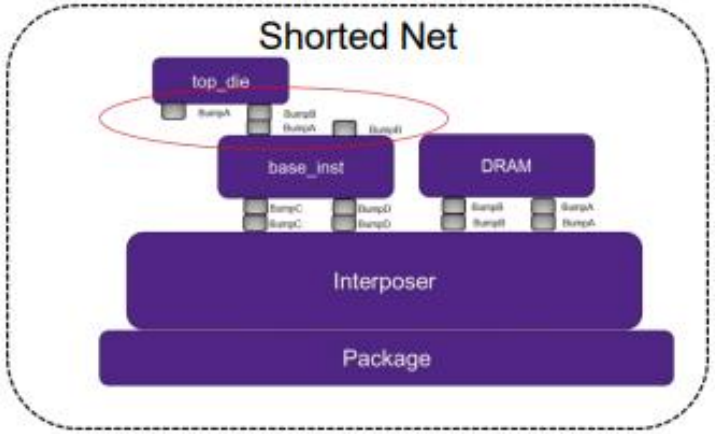


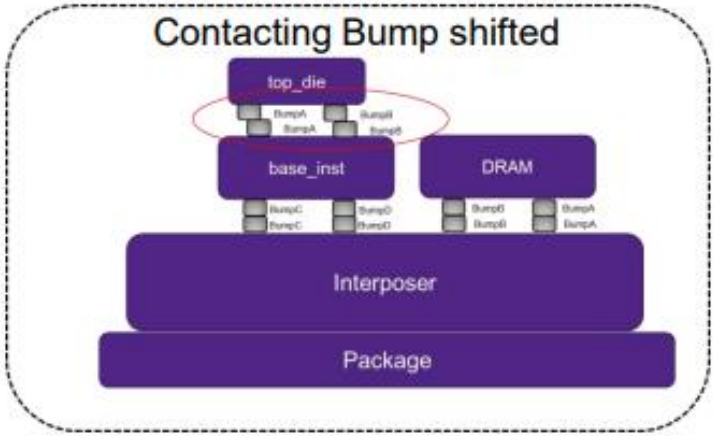
3D Rule Check Examples

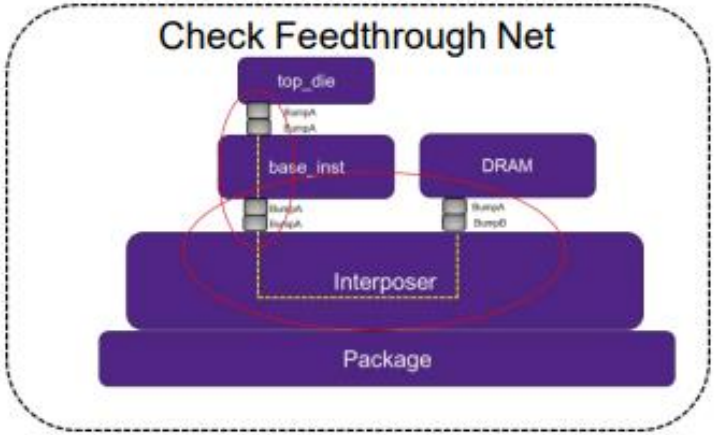


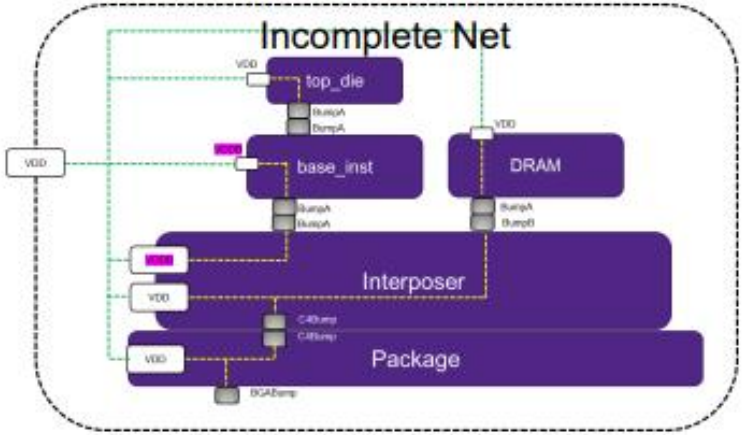






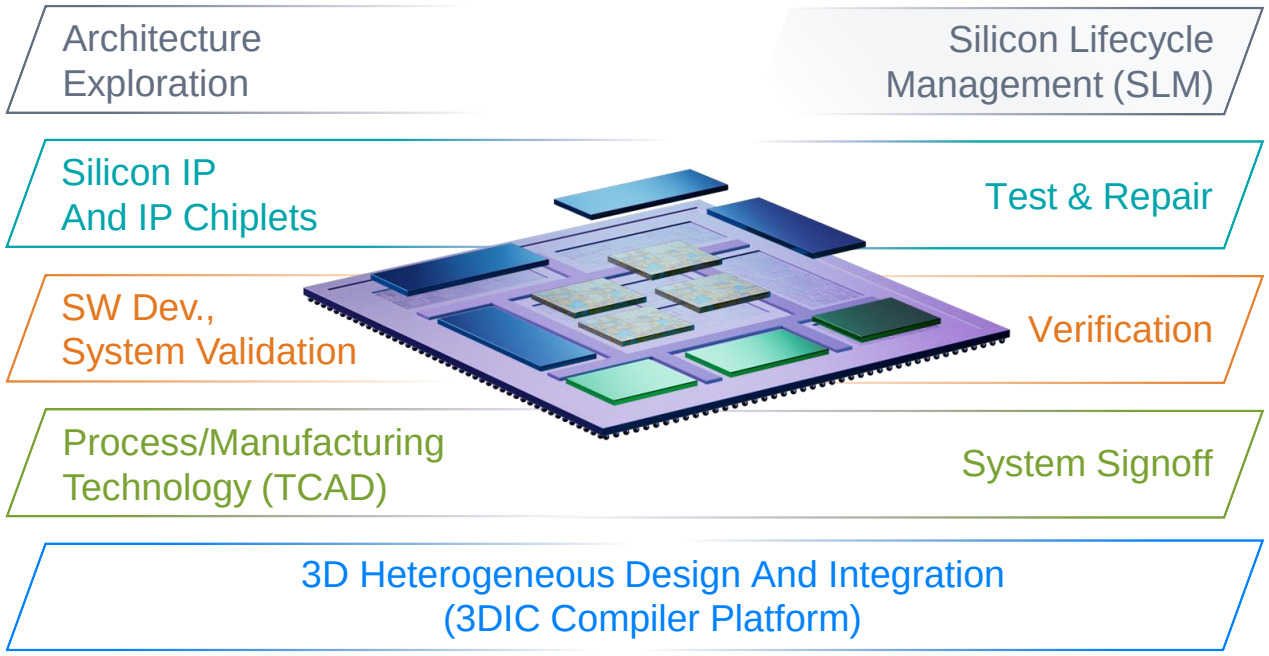






Synopsys Multi-Die Solution

A comprehensive solution for heterogeneous integration



STCO and Design	Co-optimize system thermal, power, and performance with early exploration and partitioning
Software Dev. & Validation	Rapid software development and validation with high-capacity emulation & prototyping
Design Implementation	Efficient die/package co-design with unified exploration-to-signoff platform and robust IP
Manufacturing and Lifecycle Health	Optimized yield, improved health, security and reliability with holistic test and lifecycle management solutions

Summary

Multi-Die Systems Design triggers profound changes which require:

- Automation of power, thermal, stress integrity analysis versus iterative methods
- Automation of signal integrity analysis closure versus manual methods
- A solution that can expand to the full system using AI technology

Synopsys Solutions for solving Multi-Die Challenges

- AI Driven 3DIC Design: 3DSO.ai
- 3D Prototyping Flow and Thermal Analysis Solution
- Scalable Solution For Multi-Die Bumps, HBs, TSVs and Fanout RDL Package
- Multi-Die In-Design and Signoff Analysis
- 3D Verification / DRC Checks

Unified Platform for Analysis-Driven Design and Optimization:

- Synopsys solution for Multi-Die Designs provides seamless 2D to 3D design continuum
- A comprehensive heterogeneous integration solution for System Planning, Automation, Optimization

SYNOPSYS®

snug

THANK YOU

Our
Technology,
Your
Innovation™