Broadening the Horizon – AI-Driven Digital Design Exploration and Implementation

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Industry Trends and Challenges

SYNOPSYS® snug

Design talent is on track to face a shortfall of 35% workers by 2030

- Growing Design Complexity
- March To Angstroms
- 1000x Power Reduction
- Multi-Die Design challenges
- Semi Talent Shortage

Source: BCG analysis

89,000
Demand for US-based design workers in 2030

−

66,000
Supply of US-based design workers in 2030

=

23,000
Shortage of design workers in 2030, growing by 3,000 per year

Demand for workers is expected to rise by ~50% …

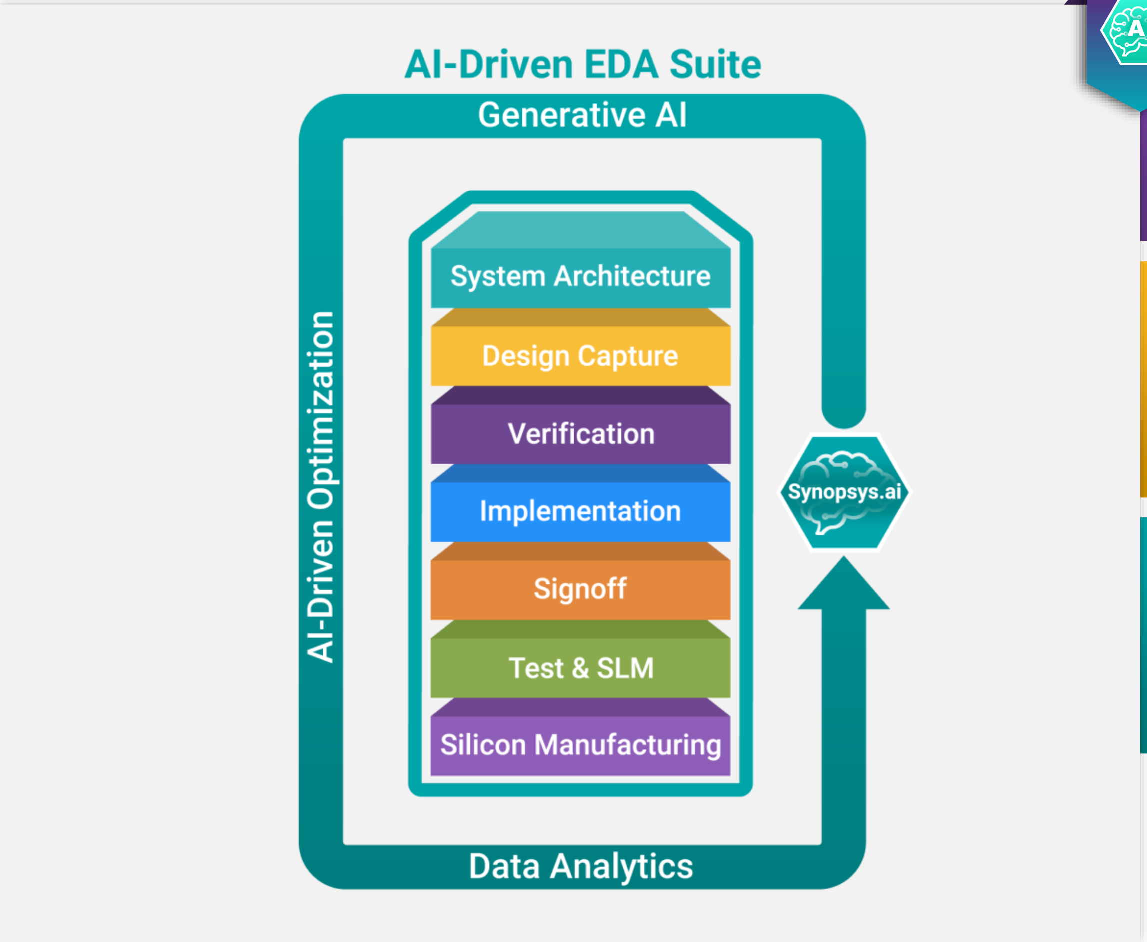
… While supply will grow by less than 1% annually …

… Meaning that demand for design workers will **exceed supply** by nearly 35% in 2030

Demands Significant Increase in Productivity

Synopsys.ai: Industry's First Full-Stack, AI-Driven EDA Suite

Boost productivity for every stage of chip design



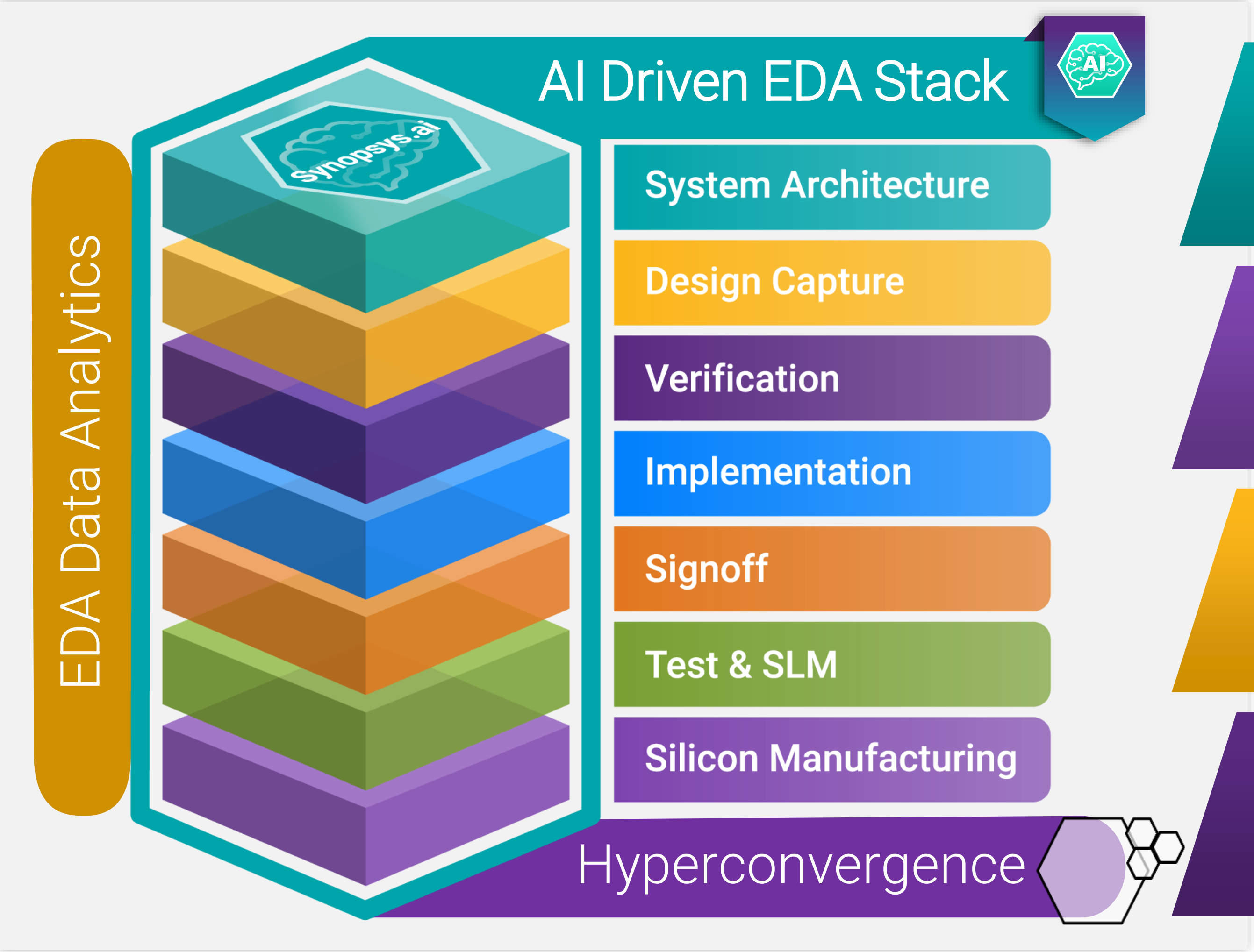
Generative AI
Collaborative, generative, and autonomous design to accelerate innovation

Data Analytics
AI-driven data analytics solution harnesses untapped insights to drive more intelligent decision making

AI-Driven Optimization
AI-driven chip design solutions enhances silicon quality while minimizing costs

Synopsys.ai: Industry's First Full-Stack, AI-Driven EDA Suite

Delivers unmatched productivity & QoR boost



Design Space Optimization
Achieve power, performance and area (PPA) targets, and boost productivity with DSO.ai

Verification Space Optimization
Faster functional testing closure, higher coverage and predictive bug detection with VSO.ai

Test Space Optimization
Automated test generation resulting in fewer, optimized test patterns with TSO.ai

Analog and Manufacturing
Rapid migration of analog designs and development of lithography models

Synopsys.ai Copilot

Key Innovation Areas in Digital Implementation

ADVANCED NODE PPA

- Seamless new node enablement
- Out-of-the-box PPA entitlement and optimized cost efficiency (PPA-C)

HYPERCONVERGENCE

- Fastest design throughput with 100+ core scalabilty
- Global RTL-to-GDSII convergence with expanded shift-left optimization
- Native advanced signoff, test, and verification fusion

AI / ML-BOOSTED PPA & PRODUCTIVITY

- 2nd generation DSO.ai reinforcement learning engine
- AI-guided dynamic implementation flow
- ML-driven predictive flow and big data analytics

HIGH PERFORMANCE CORE INITIATIVE

- Boundary-less development with ecosystem team
- Targeted technology innovation and accelerated feature deployment

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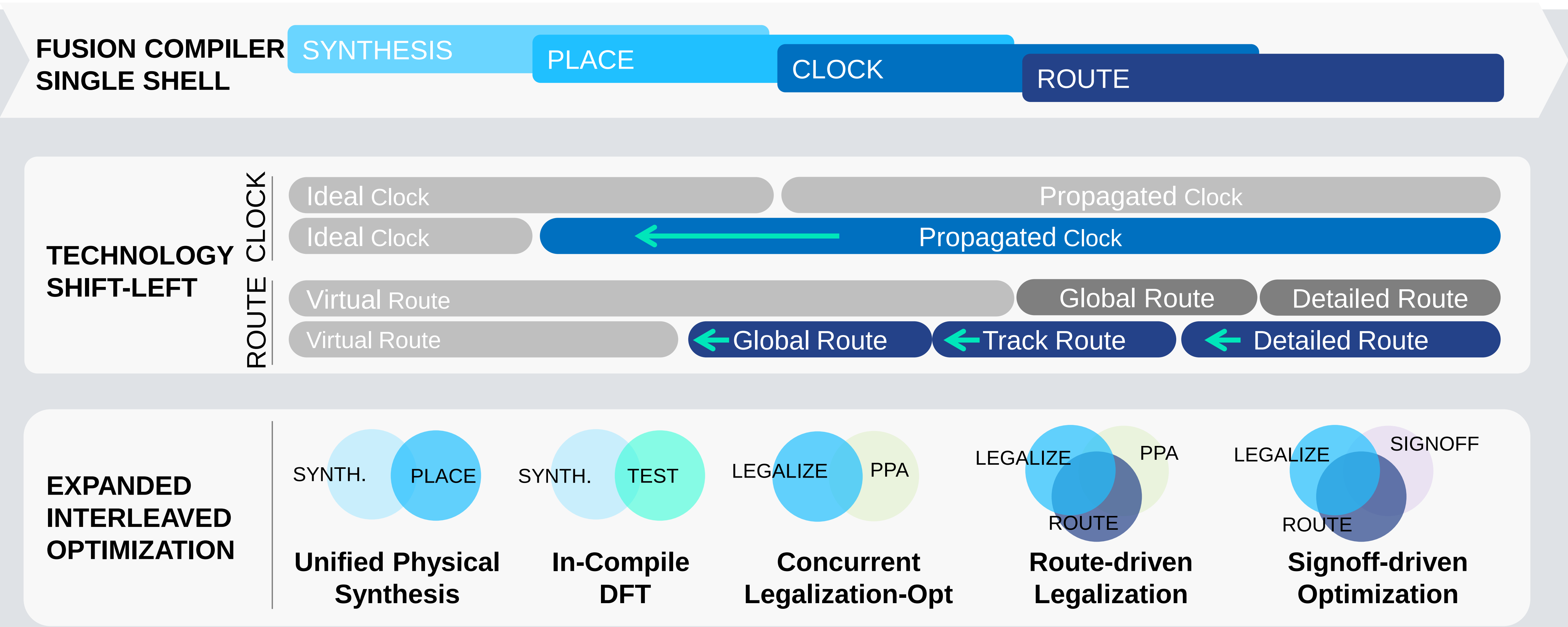
Endless Opportunities for Hyper-Convergent Flow

Single Shell Enabled Technology Movements



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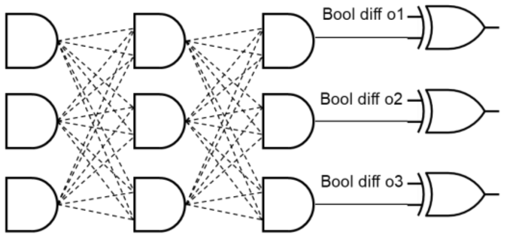
AI/ML-Driven Productivity

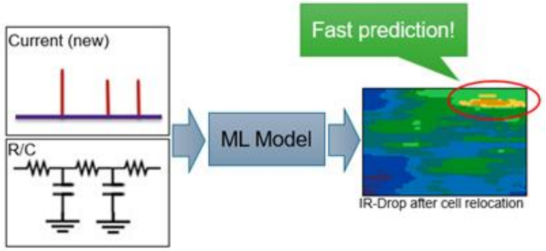
In-Design DSO.ai

ML-Driven Structuring

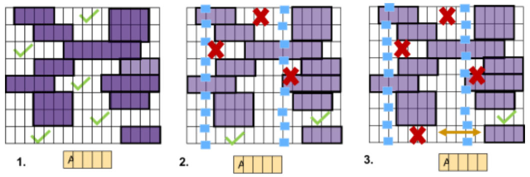


Lean approximate connectivity, edge polarity with AI
Produce exact implementation with BDD/SAT

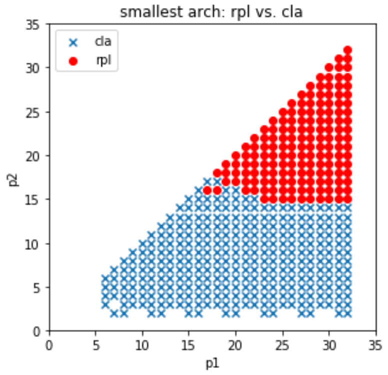
ML IR-drop Prediction



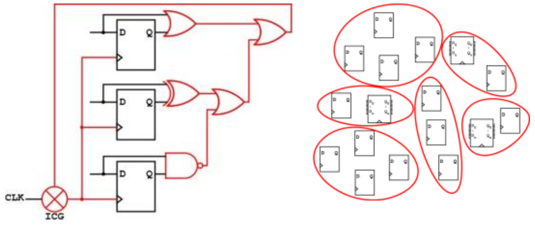
ML Legalization & Opt



ML DW Arch Selection

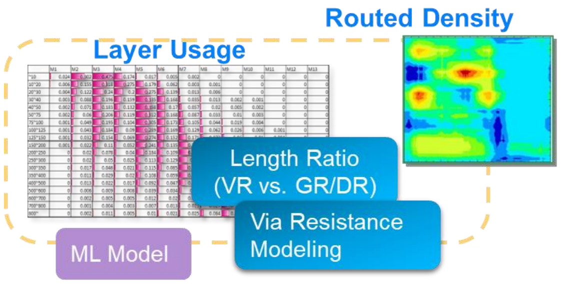


ML Self Gating

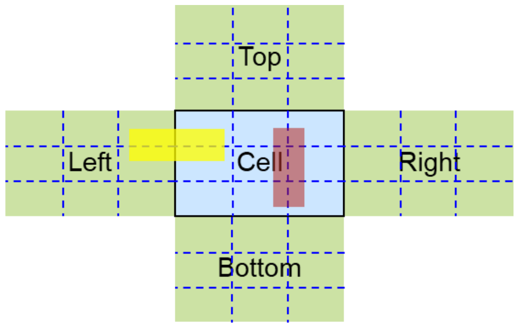


Better PPA and runtime through ML Based candidate identification for self gating

ML Pre-route Extraction



ML Pin Access Check



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Gen AI
DSO.ai
Design.da

AI-driven Implementation Platform

Seamless and scalable AI enablement through Fusion Compiler platform

FUSION COMPILER COCKPIT

- RTL-to-GDSII Implementation
- Common database
- ML technologies
- Signoff Integration

- GenAI Technologies for implementation
  - Design collateral creation
  - Techfile creation
  - RTL PPA opt
  - Knowledge Assistant
  - Floorplan PG creation
  - CTS creation
  - Result Assistant
  - Workflow Assistant

GENAI – Knowledge, Debug, Workflow

DSO.AI – Dynamic flow, Design Space Exploration

DESIGN.DA – Dashboard, Prescriptive Guidance

Direct Launch

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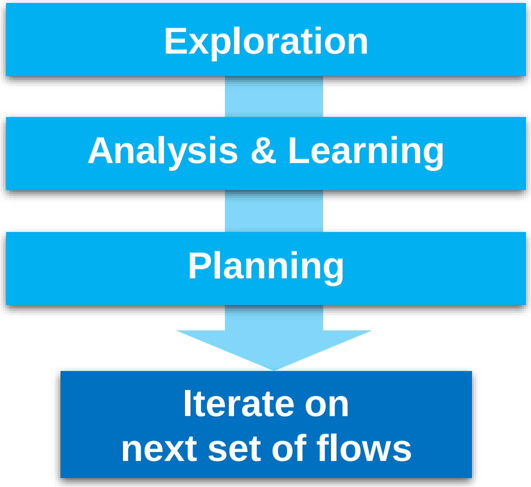
AI / ML Runtime Acceleration Technologies

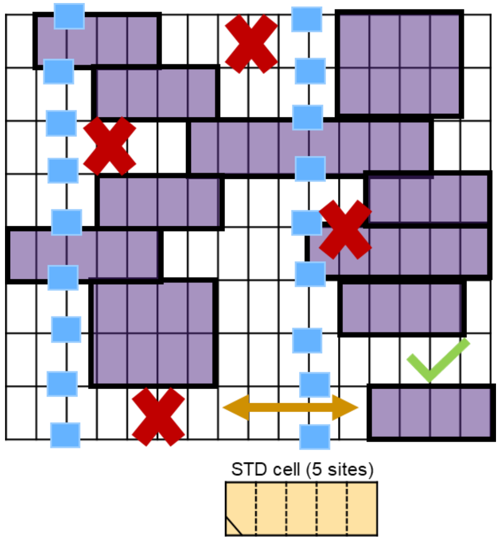
In-Design DSO.ai

- Learns block-specific behavior at each stage to better configure latter stages
- Dynamically configures sub-flows & engines for next runs & stages



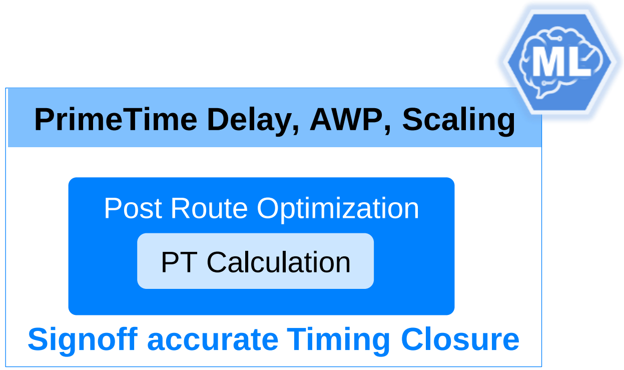
ML-Accelerated Concurrent Legalization and Opt

- ML technique to improve picking candidates or locations for optimization
- Adv rules context-aware probability infrastructure and learning model



ML-Accelerated PrimeTime Delay Calculation

- Machine Learning to reduce delay calculation runtime
  - Leverage pre-defined model to select worst receiver mode
- Same accuracy as standard PrimeTime Delay Calculation



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AI-Driven Acceleration Technologies

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- Flexible multiple objective reinforcement learning (DAC-2022)
- Neural network training inspired coarse placement engine (DAC-2019)
- Netlist clustering to speed up reward calculation

工商時報
COMMERCIAL TIMES

臺大攜手聯發科、至達科技產學研發 超越Google晶片擺置彈性

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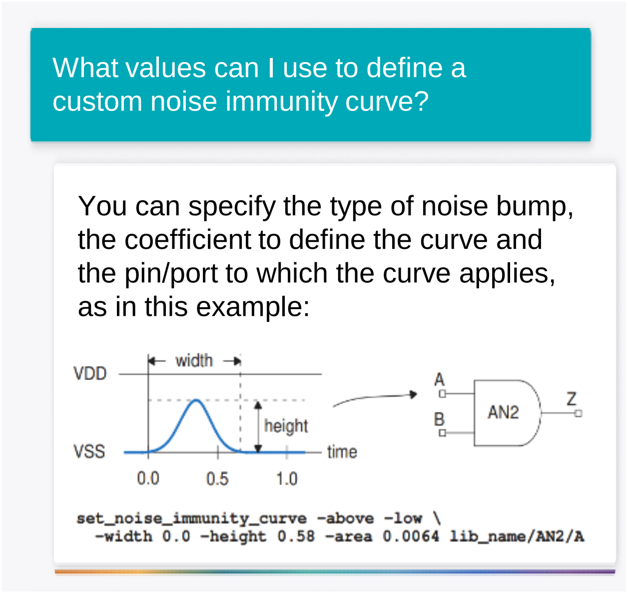
AI-Driven Productivity Enhancement

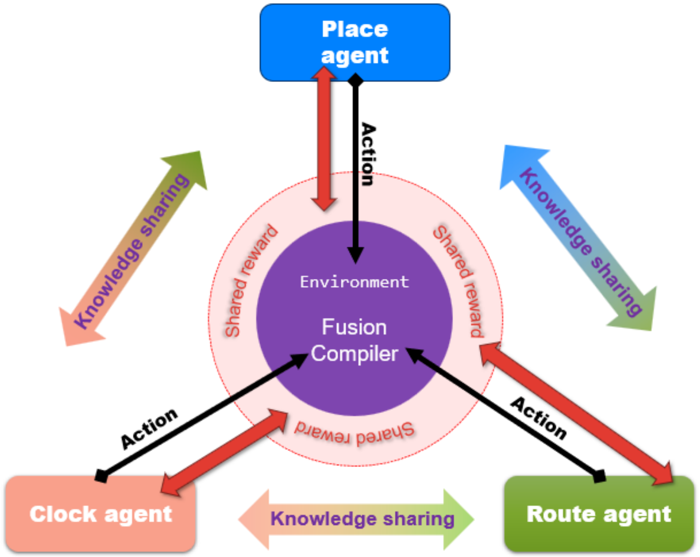
Copilot

- Knowledge assistance to answer expert questions



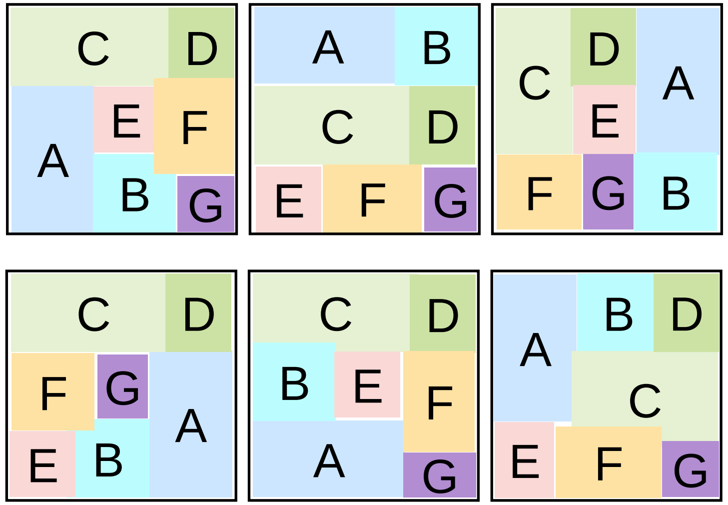
Design Space Exploration

- AI-driven autonomous design optimization



GPU Acceleration

- PPA improvement through placement exploration



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1. Fusion Compiler Copilot

Synopsys.ai Copilot for Next-Level Automation

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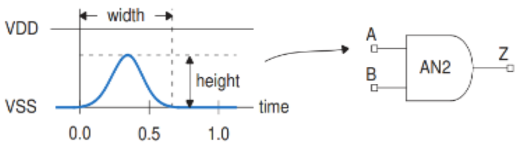
Generative AI (LLM) Based EDA Assistants

1 Knowledge Assistant

What values can I use to define a custom noise immunity curve?

You can specify the type of noise bump, the coefficient to define the curve and the pin/port to which the curve applies, as in this example:




```
set_noise_immunity_curve -above -low \
  -width 0.0 -height 0.58 -area 0.0064 lib_name/AN2/A
```

Answer expert questions

2 Run Assistant

What is the current state of my timing?

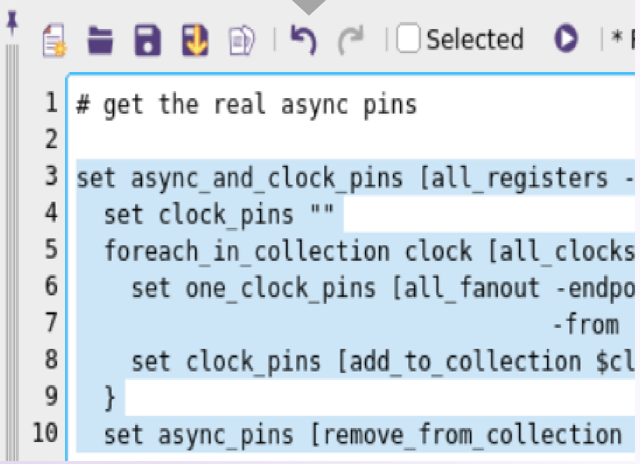
Results from `report_global_timing` show that this design has zero setup violations but 1423 hold violations.

Results from `report_constraints` show that the clock group CLK accounts for 786 violations.

Summarize results, suggest next steps

3 Workflow Assistant

>User presses tab and Tcl is auto-generated based on the comment



Create Tcl workflows

Answer Expert Question: App Options

How to control max density for doing cell placement?

I found the following documents related to your question:

- Controlling the Placement Density ?
- DPP > DPP-417 Message ?
- Resolving and Controlling High Cell Spreading During Congestion Alleviation ?

Show More

Based on these documents, here is my response:

To control the maximum density for cell placement, you can use the `place.coarse.max_density` application option. By setting this option to a specific value between 0 and 1, you can control how densely the tool can place cells in the design.

For example, you can set the maximum density value using the following command:

```
fc_shell> set_app_options -name place.coarse.max_density -value 0.6
```

This command will set the maximum density to 0.6, allowing you to control the density of cell placement in the design. Remember that setting a higher value allows cells to clump together more densely, while setting a lower value helps avoid cell clumping.

List all app options related to placement density control

I found the following documents related to your question:

- place.common.pnet_aware_density Application Option > Examples ?
- place.common.pnet_aware_density Application Option > Examples ?
- place.coarse.max_density Application Option ?

Show More

Based on these documents, here is my response:

- `place.coarse.auto_density_control`
- `place.coarse.max_density`
- `place.coarse.congestion_driven_max_util`
- `plan.place.auto_max_density`
- `place.floorplan.density_aware_hard_movebounds`

Tcl Script Assistance

How to change color of register cells?

I found the following documents related to your question:

- remove_colors Command > Options and Arguments ?
- remove_colors Command > Options and Arguments ?
- place.legalize.libcell_based_color_shifting Application Option ?

Show More

Based on these documents, here is my response:

To change the color of register cells, you can use the following script:

```
gui_change_highlight -remove -all_colors
gui_change_highlight -add -color blue -collection [all_registers]
```

This script will remove all existing colors and then highlight all register cells in blue.

How to write tcl to traverse all cells?

I found the following documents related to your question:

- How Do I Get All the Cells in a Specific Site Row? ?
- rpt_cell Overview ?
- rpt_cell Listing and Output Example ?

Show More

Based on these documents, here is my response:

To traverse all cells in a design using Tcl, you can use the following script:

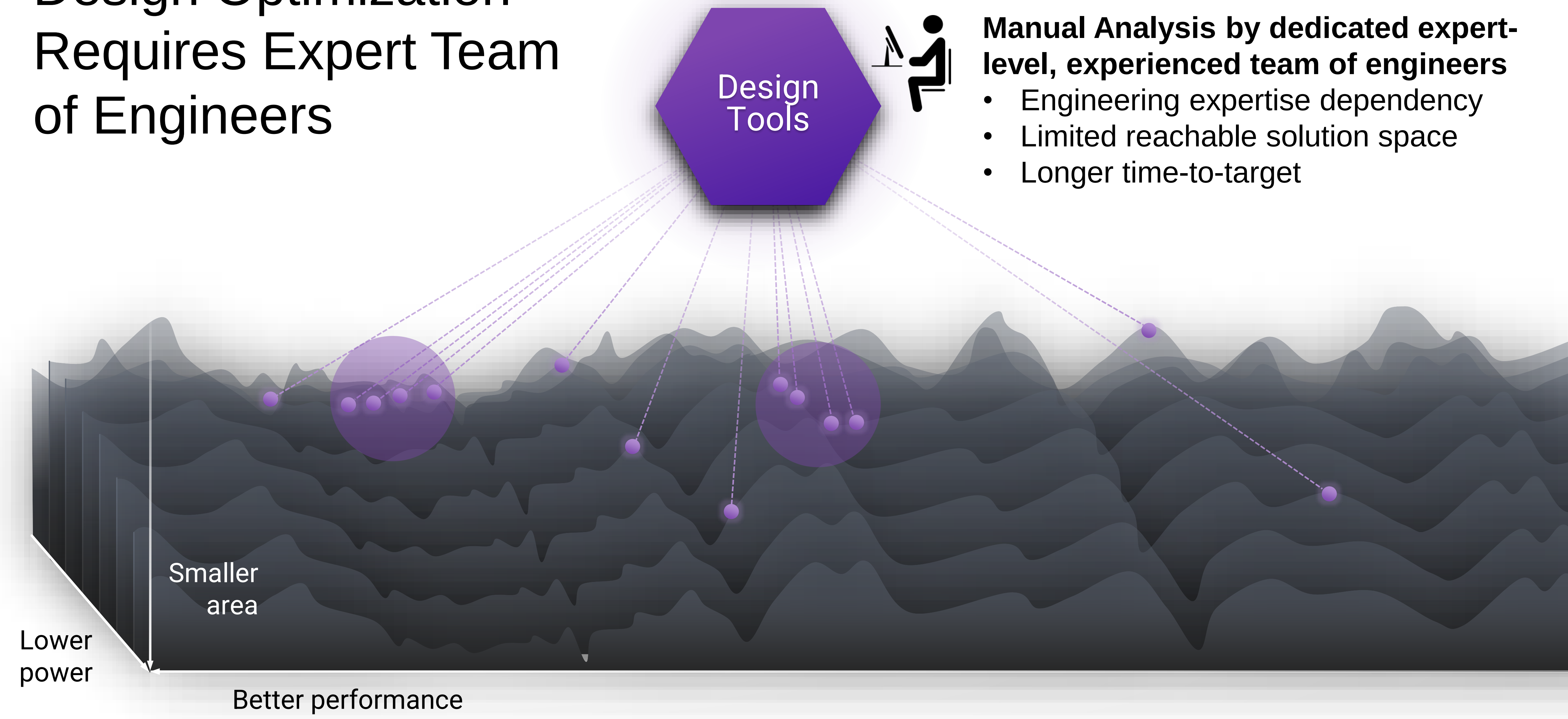
```
set all_cells [get_flat_cells -hierarchical *]


foreach_in_collection cell $all_cells {
    set cell_name [get_attribute $cell full_name]
    # Perform actions on each cell here
    # For example, print the cell name
    puts $cell_name
}
```

This script first retrieves all cells in the design using the `get_flat_cells` command and stores them in the `all_cells` collection. Then, it iterates over each cell in the collection using the `foreach_in_collection` command, retrieves the full name of the cell, and performs any desired actions on each cell. In this example, it simply prints the name of each cell.

2. Design Space Exploration

Design Optimization Requires Expert Team of Engineers



Manual Analysis by dedicated expert-level, experienced team of engineers
- Engineering expertise dependency
- Limited reachable solution space
- Longer time-to-target

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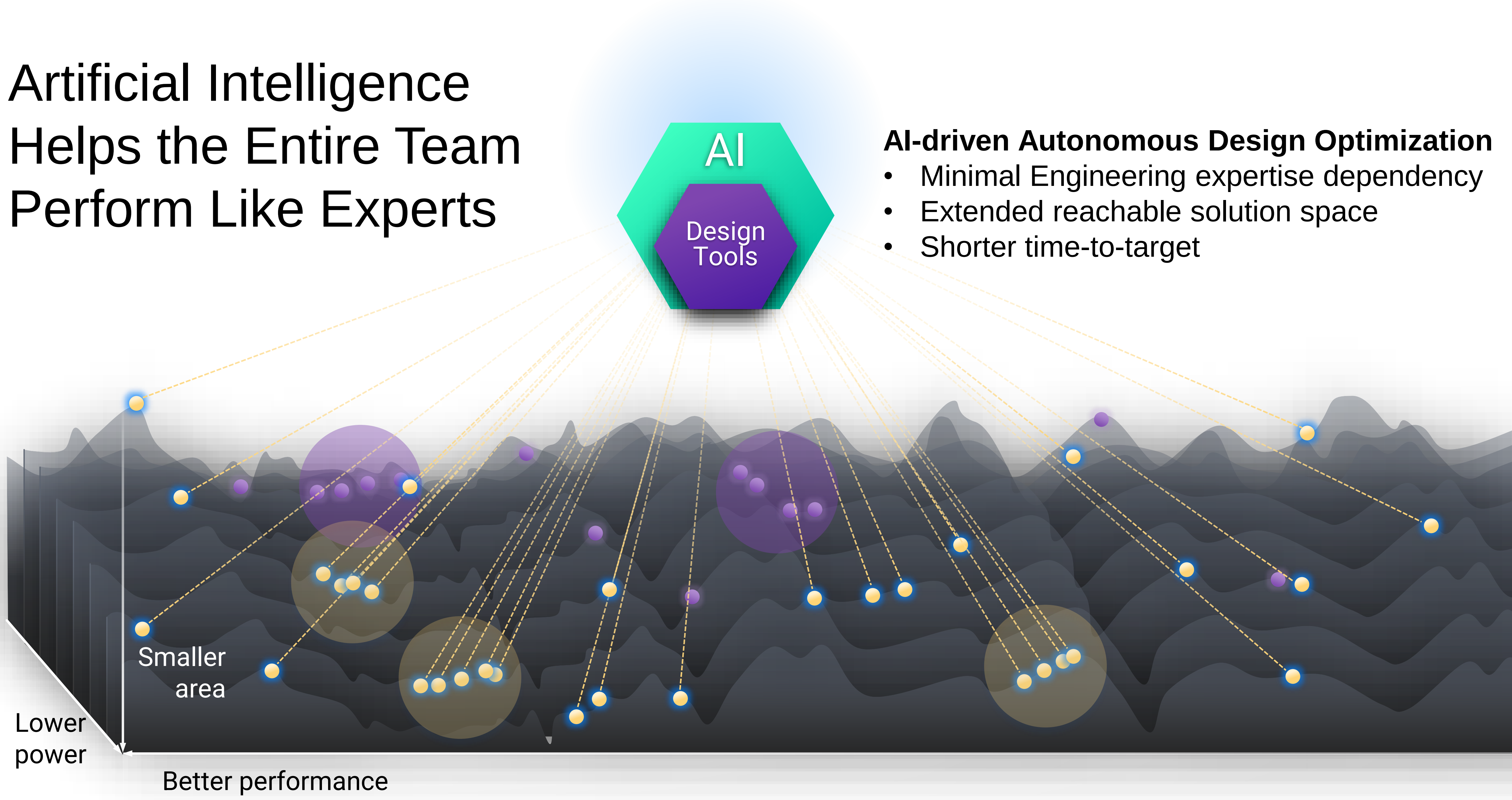
Artificial Intelligence Helps the Entire Team Perform Like Experts

AI-driven Autonomous Design Optimization

- Minimal Engineering expertise dependency
- Extended reachable solution space
- Shorter time-to-target



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Synopsys DSO.ai — AI-driven Digital Design

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Breakthrough Reinforcement Learning

Capable of searching trillions of RTL-to-GDSII design permutations for best results

Fast Ramp-Up

Fully-integrated with the Digital Design Family—industry’s richest technology foundation

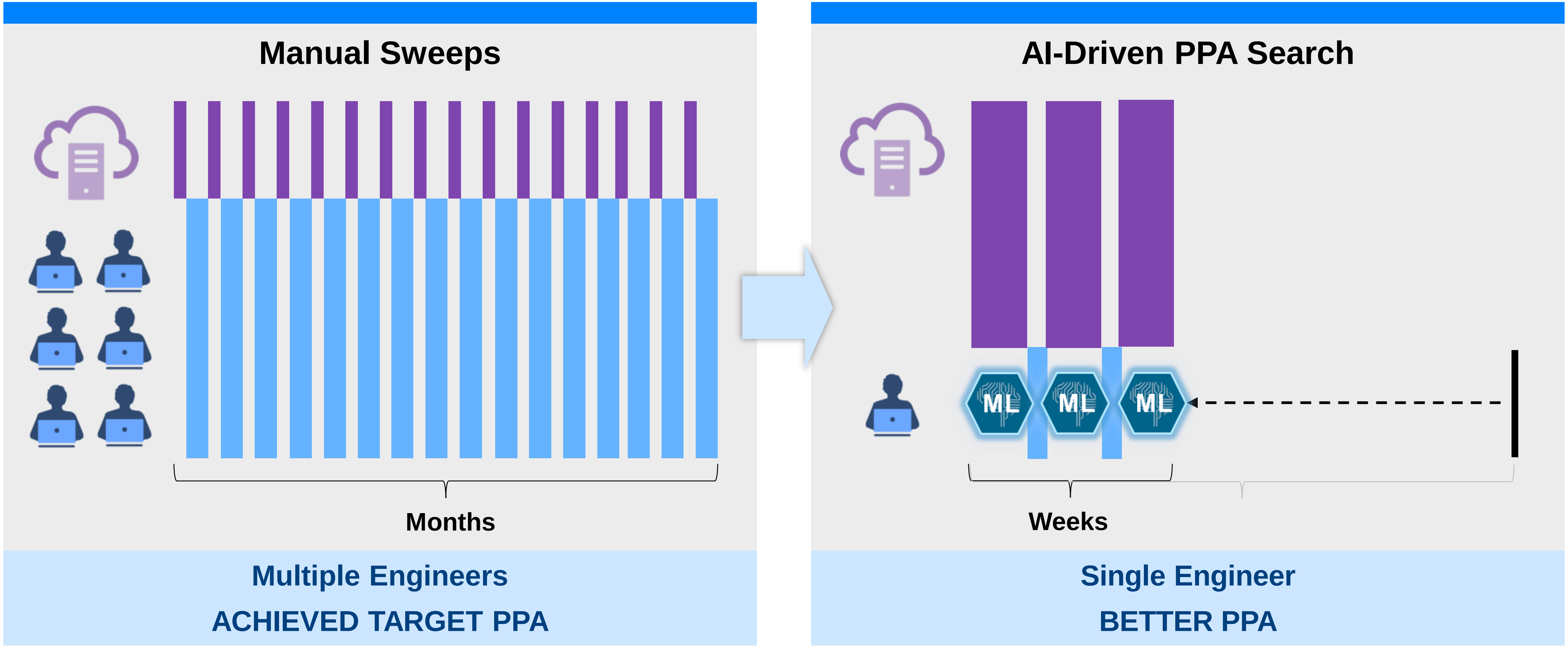
Cloud-Ready

Supports on-prem, public, and hybrid clouds for fast deployment

World’s First Autonomous Design Space Optimization

AI-Driven Design Space Optimization (DSO)

10X productivity compared to traditional, manual exploration



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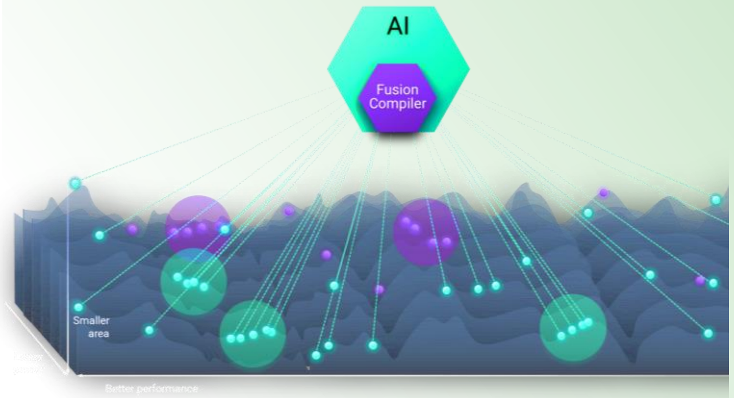
DSO.ai Use Models in the Implementation Flow

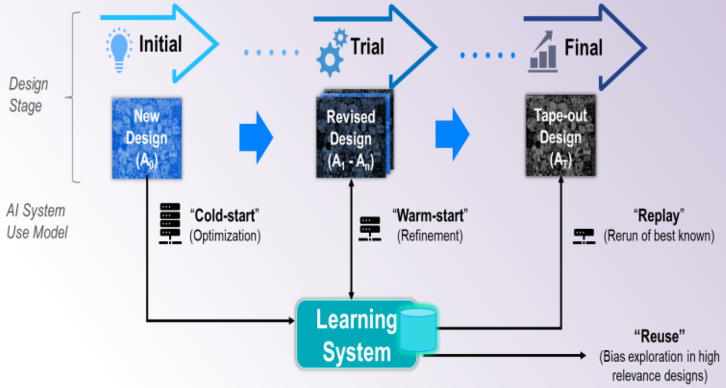
PPA Push, Project Reuse, Early Feasibility

PPA Push



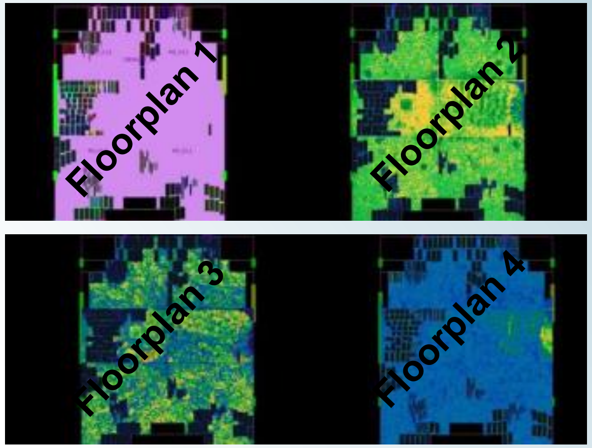
- Unmatched PPA with Design Space Optimization
- Up to 20% better quality of results

Project Reuse



- Learning and reuse on derivative blocks/designs
- 3x reduction in compute resources

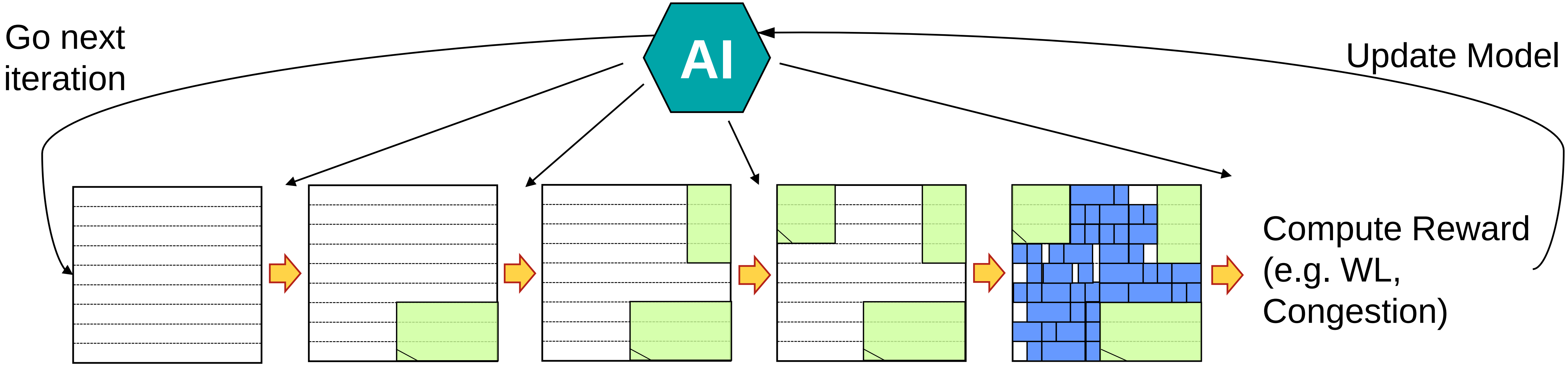
Early Feasibility



- Multiple floorplan configuration exploration
- 5x productivity improvement

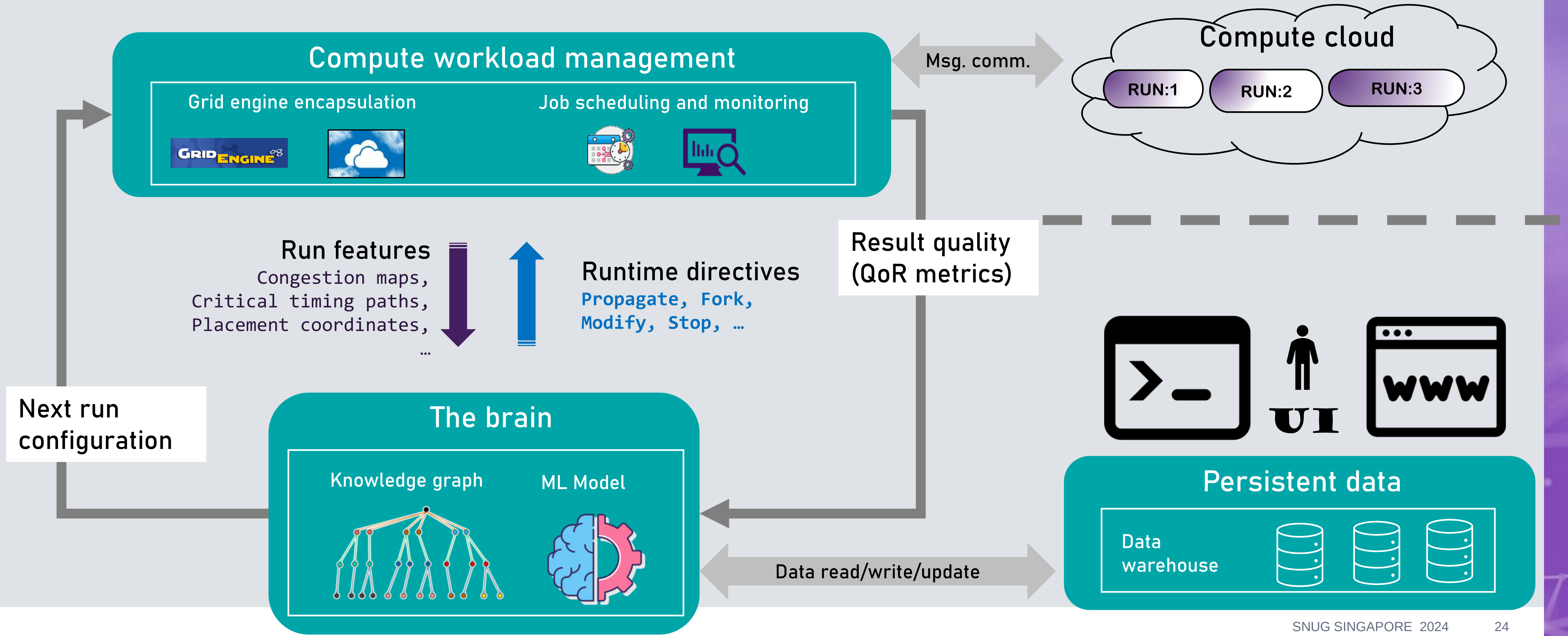
AI in Floorplanning and Placement

- Reinforcement learning placement
- Intelligent agents take actions to maximize the cumulative reward
- Mirhoseini et al. “A graph placement methodology for fast chip design,” Nature 2021



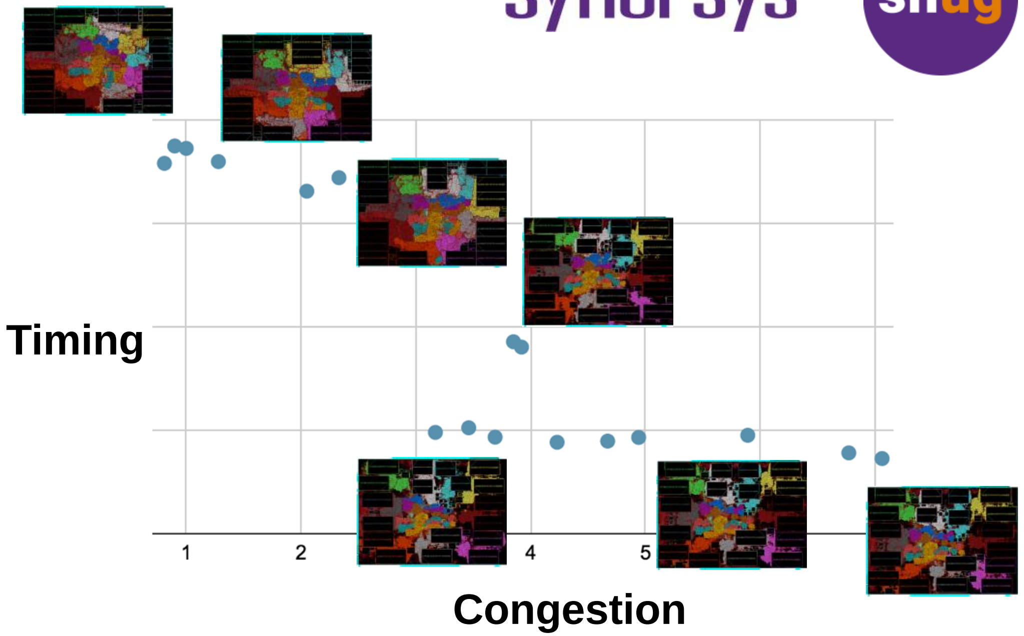
Architecture

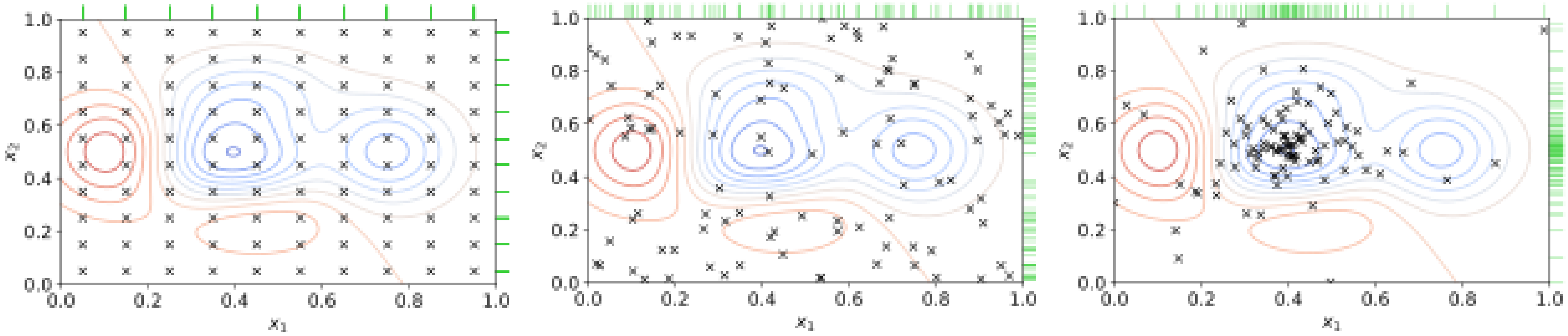
A scalable distributed system with continuous learning



Hyperparameter Optimization

- Parameters
  - Cell density, utilization, module location, floorplan styles
  - Multi-objective efforts
    (congestion, timing, power)
- Approaches
  - Grid search, random search, Bayesian optimization



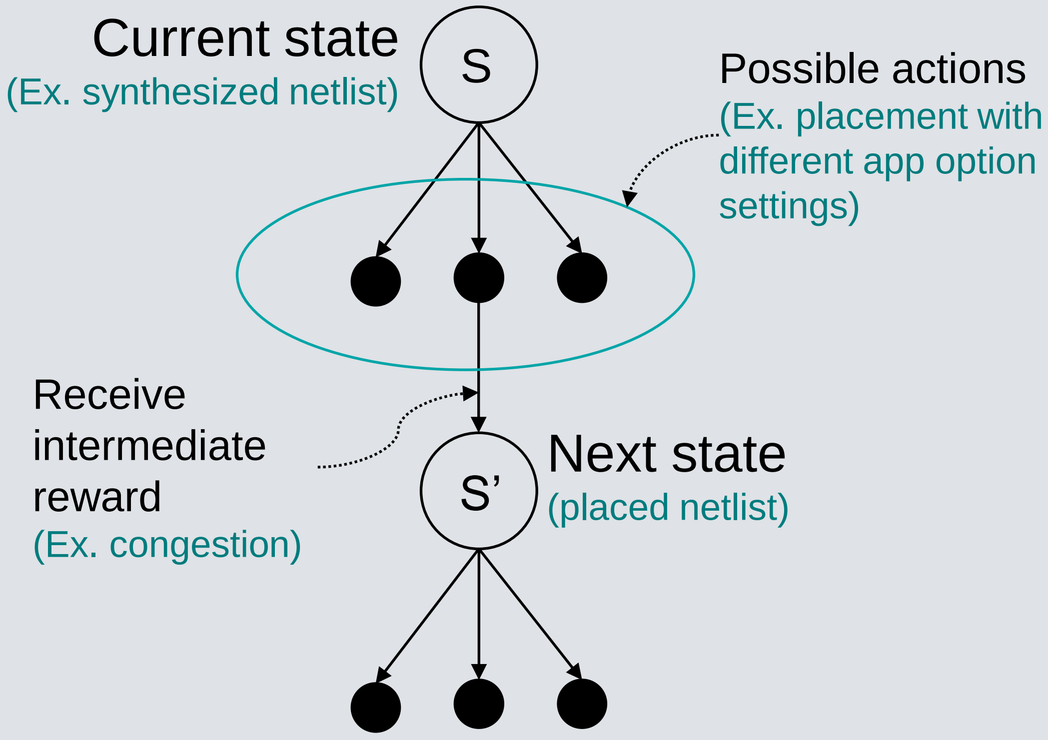


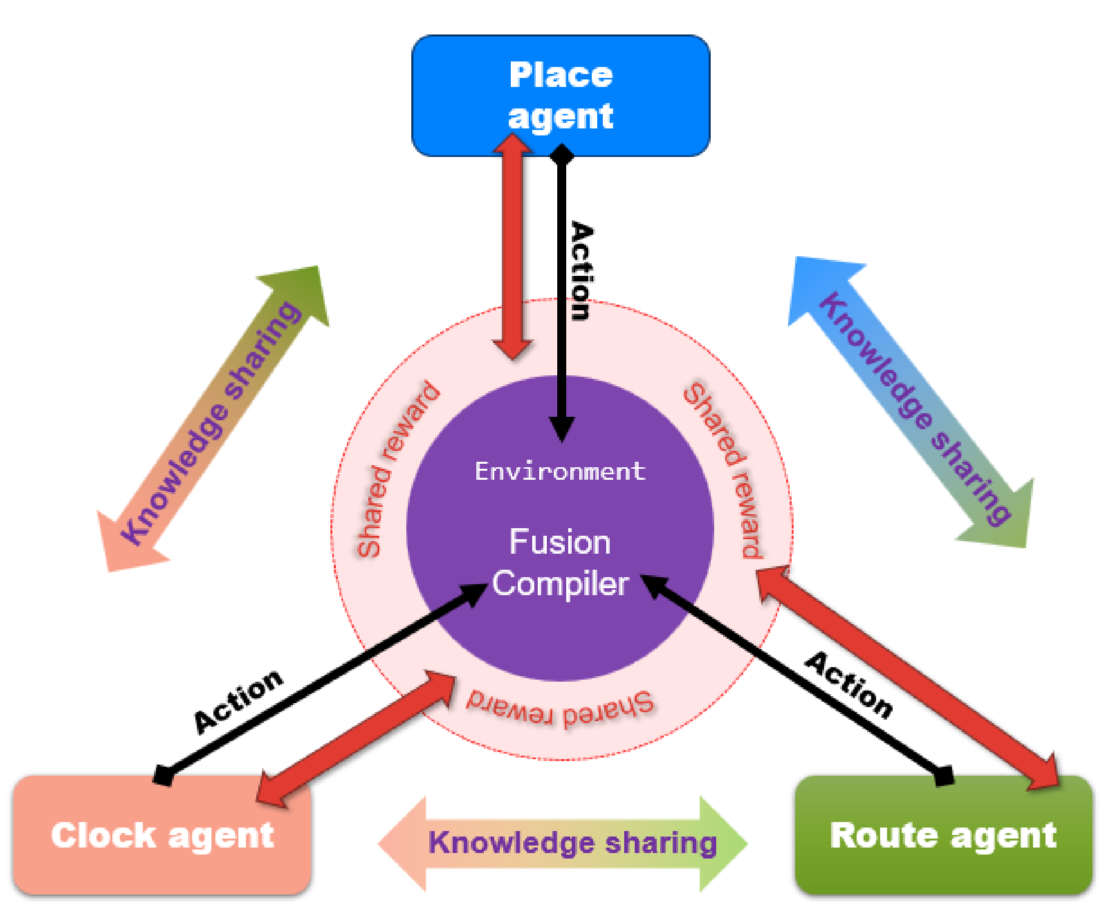
https://en.wikipedia.org/wiki/Hyperparameter_optimization

Reinforcement learning

Specialized RL agents operating at the flow level

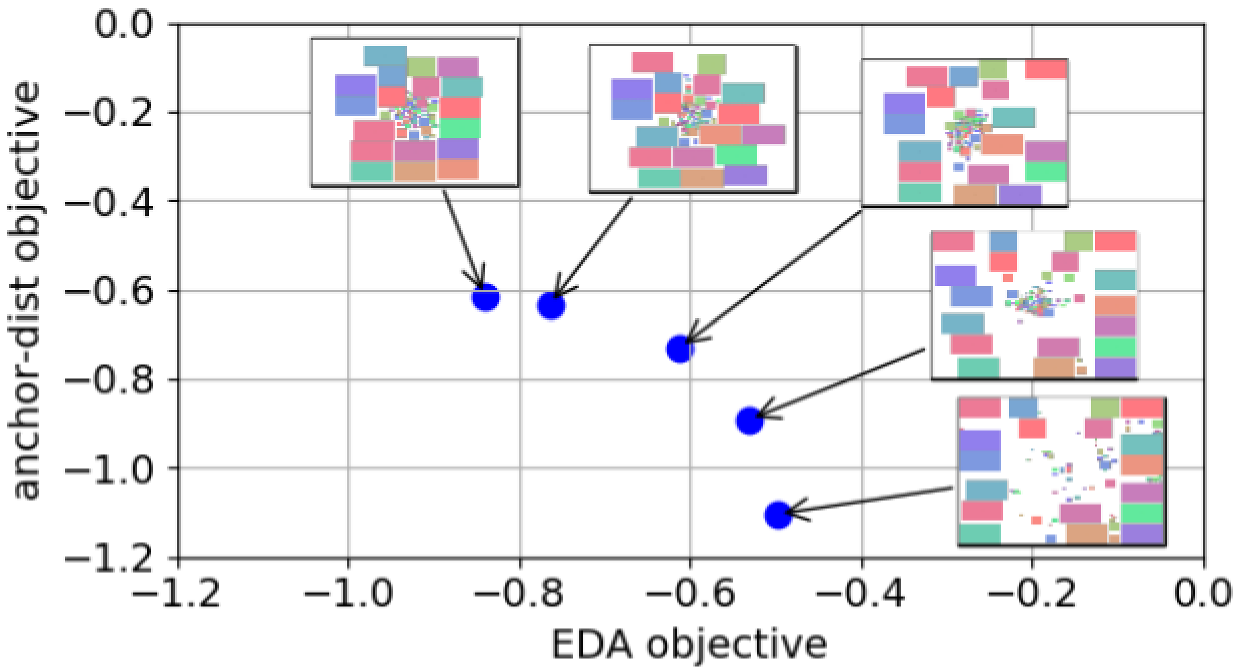
Sequential decision making





Flexible Multiple-Objective Reinforcement Learning for Chip Placement (Source: DAC 2022, MediaTek/Maxeda)

- Fixed-weighted models cannot generate the diversity of placement
- Need flexible multiple-objective reinforcement learning using a single pretrained model



(a) fixed preference $\omega = (0, 1)$. (b) MOPPO $\omega = (0, 1)$. (c) MOPPO $\omega = (0.3, 0.7)$. (d) MOPPO $\omega = (0.5, 0.5)$.

(e) MOPPO $\omega = (0.7, 0.3)$. (f) MOPPO $\omega = (1, 0)$. (g) fixed preference $\omega = (1, 0)$. (h) tapeout $\omega = N/A$.

Customers Share Success with Production Deployment

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Results from AI Track, SV SNUG 2023 Proceedings, customer engagements

Power Opt.

5nm

3% Total Power

HPC

DSO.ai at Microsoft – Power - Block 1

Microsoft snug

ADES_power	R2R_TNS	dso_metric_total_power	UTILIZATION	BLOCK_SAVE	
0.75803	-1.2	0.97	0.98	ADES_power:0	dso_metric_total_power:0
0.76060	-1.3	0.97	0.98	ADES_power:1	dso_metric_total_power:1
0.76136	-0.57	0.98	0.99	ADES_power:2	dso_metric_total_power:2
0.77674	-0.8	0.98	1	R2R_TNS:0	
0.99805	-1.10	1	1	R2R_TNS:2	dso_metric_leakage_power:0
1.00000	-1	1	1	R2R_TNS:1	dso_metric_leakage_power:1

Multiple choices with various tradeoffs

Composite Score (lower is better)

Non-DSO baseline (Designer database replayed in DSO)

- 3% better total power improvement with DSO power toolbox as measured in signoff power analysis
- Replayable for future iterations of the block via warm start

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Power Opt.

Adv. FinFET

5% Total Power

XEON

Results – DSO.ai vs PrimeTimeECO

snug

* All power measured at sign-off

Power Saving Strategy	*P-Lkg*	*P-Dyn*	*P-Tot*	*Tot mW Saving*
Baseline	-	-	-	
Baseline + PT ECO	9%	0%	2%	2.9
Baseline + DSO	18%	0%	5%	6.4
Baseline + DSO + PT ECO	19%	0%	5%	6.7

- **Key Takeaway**
  - Run with DSO enabled shows 2x total power saving as compared to PT-ECO
  - Concurrent timing and power optimization in early stage led to better optimized design
  - DSO in compile stage allowed sequential cells to be down-sized and placed before they were fixed in clock stage

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PPA Opt.

7nm

3X productivity

A510

DSO.ai enabling PPA exploration

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DSO/CLOUD Infrastructure

FC License up to 100

Search space 10^{+25}

100% of PPA exploration performed with DSO.ai

180
Permuton number

2.7K FC runs
DSO runs to cover search space

3x Productivity Gain
PPA exploration
* SNPS/ST press release

Performance ✓
Reached targeted frequency

Power ✓
Best power compromise (Dynamic/Leakage)

Area ✓
Keep same floorplan shape dimension

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PPA Opt.

7nm

3X productivity

A78

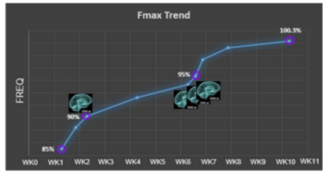
Fusion x AI for RTL-to-GDSII fast convergency

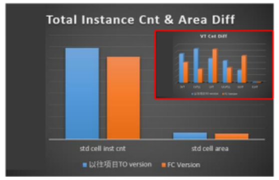
Results on ARM CPU

紫光展锐 UNISOC

- Goal: Achieve target PPA for Adv. FinFET ARM CPU Core within 4 months
- Results: 90% FMAX target met in 2 weeks with FC QIK; 100% in 2.5 months using FC + DSO.ai (1.6X faster)
- Conclusion: Fusion Compiler X DSO.ai met target faster by less engineering effort
- Next step: reuse AI models across projects

- **基于FC QIK flow 实现：**针对High Performance 模块（特指Arm core）自带内置special setting，PPA 更优
  - 分析发现：具体physical位置摆放更合理；减少传统流程设定等带来的误差；跟signoff tool correlation 更好
- **与以往TO项目相比：**
  - Std cell cnt 减少10.09%，Std cell area 减少14.6%
  - IR drop 违例点更少（8k VS 500）
  - Run time相比于传统流程更优（8.2 days vs 14days）





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Recent Customer Success with Broad Applications

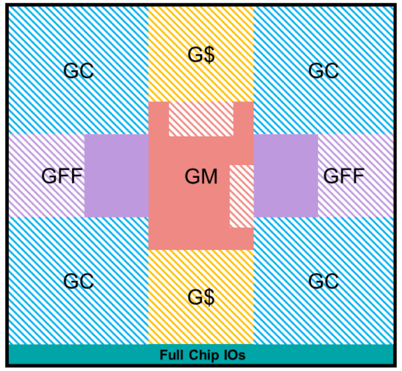
Results from AI Track, SV SNUG 2024 Proceedings

Results – Setup and Scope

- Setup
  - Fusion Compiler T-2022.03-SP5* Build
  - DSO.ai U-2022.12-SP5* Build
  - 2-3X higher disk allocation + additional compute resources
- Selected blocks for DSO.ai based optimization

Clusters	Unique Blocks	Selected Blocks
GFX Compute (GC)	8	8
GFX Fixed Functions (GFF)	15	7
GFX Cache (G$)	1	1
GFX Misc (GM)	27	5

- Contribution to Full-chip
  - ~75% of the Die-area
  - ~80% of the Total Power



GPU Full-Chip

Blocks implemented with DSO.ai Auto-convergence flow

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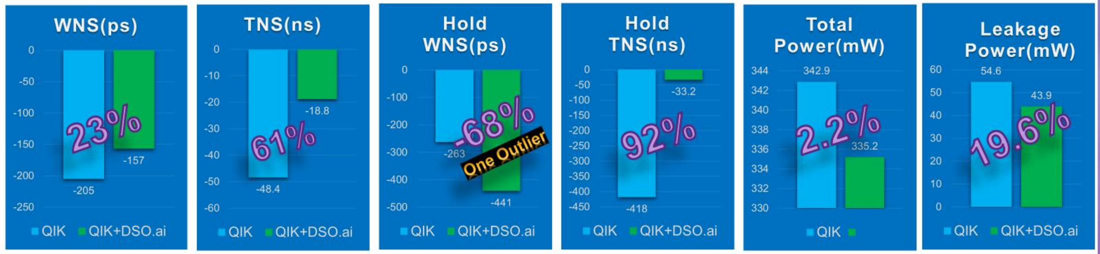
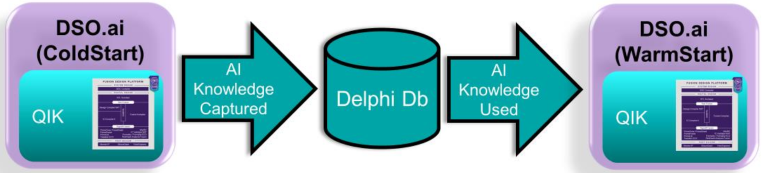
GPU Power Opt.
~75% Of Full Chip Die-area

DSO.ai Timing and Power Improvements

synaptics

Turn Around Time





SNUG SILICON VALLEY 2024 30

Synopsys ARC CPU Migration
60% Timing; 20% Leakage Improvements

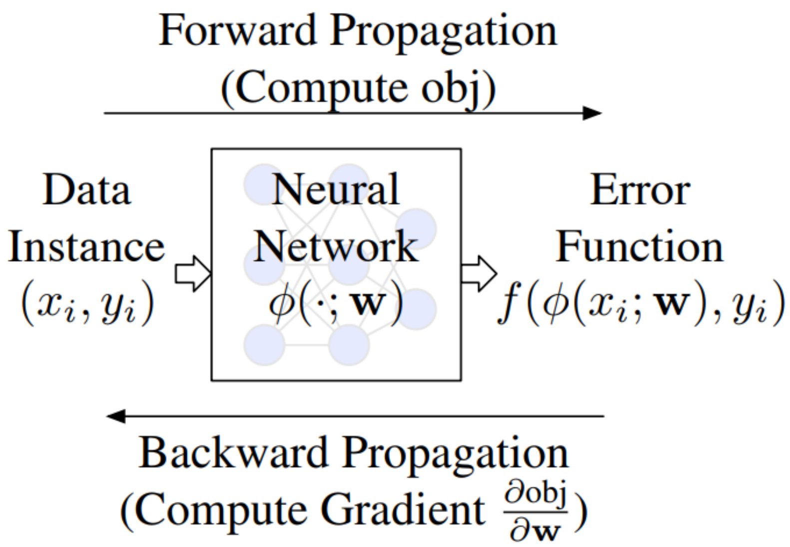
3. GPU Acceleration

Analogy between VLSI Placement and NN Training

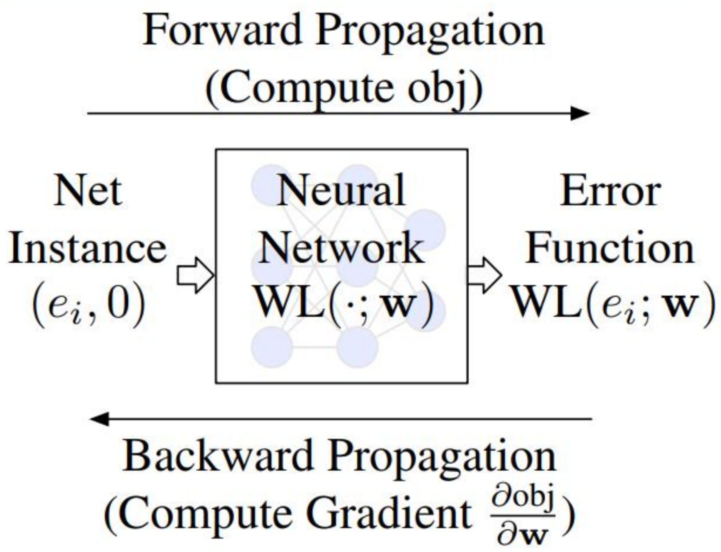
SYNOPSYS® snug

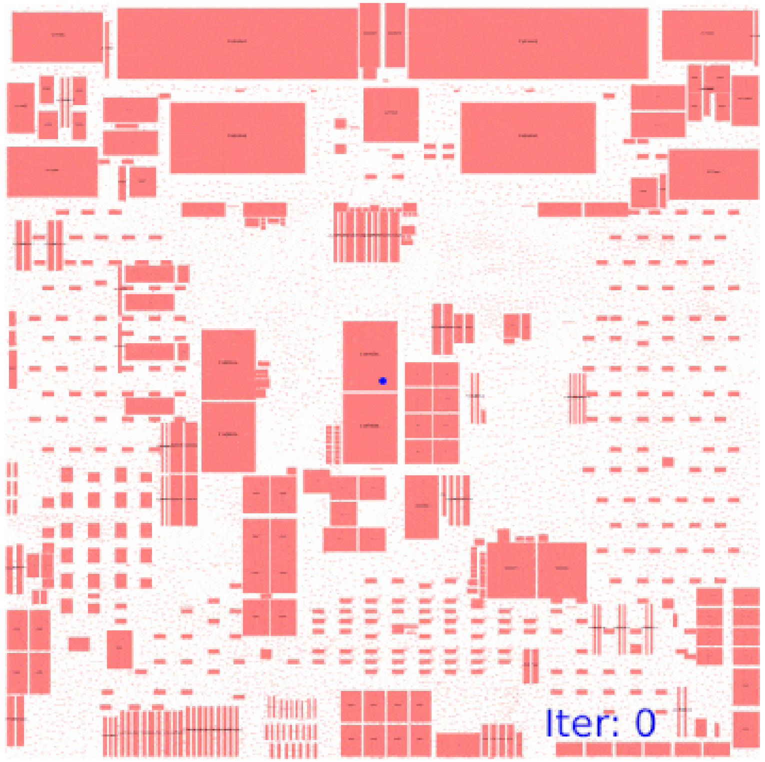
- Lin et al., DAC 2019; 10x-50x faster for runtime speedup

$$\min_{\mathbf{w}} \sum_{i}^{n} f(\phi(x_i; \mathbf{w}), y_i) + \lambda R(\mathbf{w})$$



$$\min_{\mathbf{w}} \sum_{i}^{n} \text{WL}(e_i; \mathbf{w}) + \lambda D(\mathbf{w})$$





Train a neural network ⟺ Solve a placement

GPU-Accelerated AI-Driven Placement

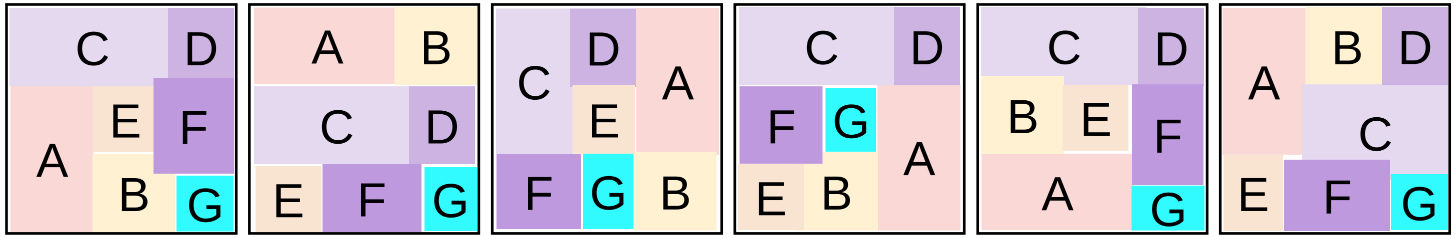
Expand search space by 15x to 20x with autonomous design space optimization

SYNOPSYS® snug

Core placement has more than 10X speedup.

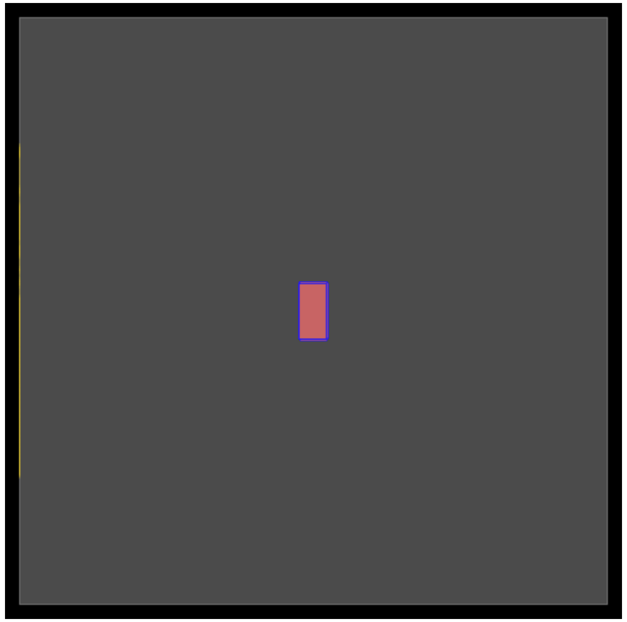
Design	Tech Node (nm)	Number Of Placeable Standard Cells	Number Of Placeable Hard Macros	CPU-driven Placement 16-Cores x86 CPU	GPU-driven Placement NVIDIA A100 80GB	Comparison
GPU Streaming Multiprocessor	3nm Variable Row Height	1.4M	20	12.5 Minutes	38 secs	20X
Automotive CPU	12nm	2.9M	200	18.7 Minutes	82 secs	14X

- Explore various module placements by autonomous design space optimization.
- GPU-accelerated placement can explore more placement possibilities in the same runtime.
- Initial seed exploration

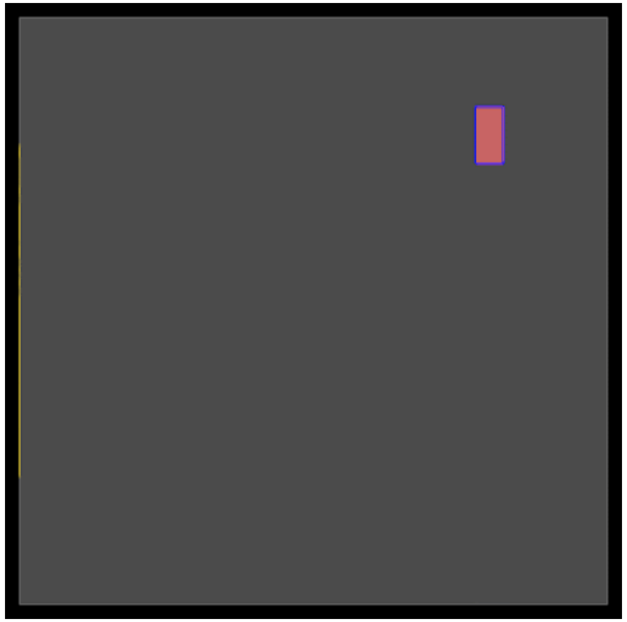


Placement Exploration

- Source: NVIDIA Technology Blog
- Agnesina et al., ISPD-2023



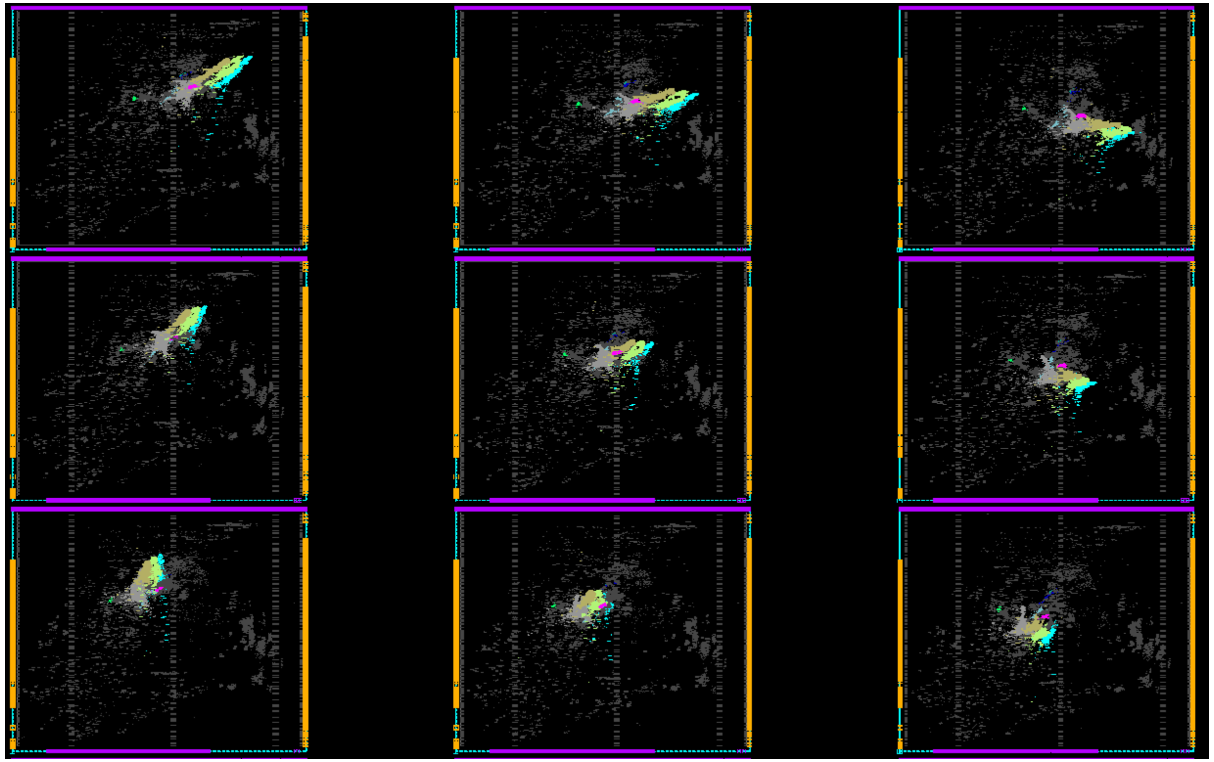
Seed 1
Center Position



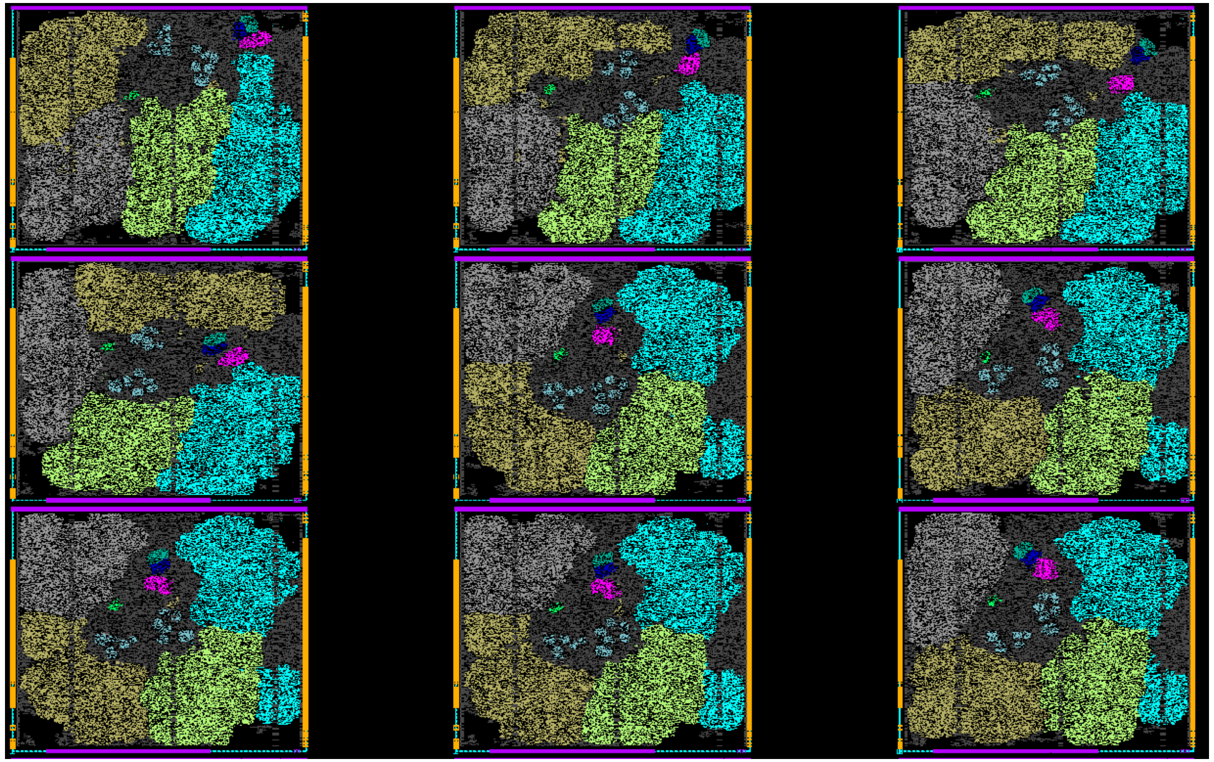
Seed 2
Upper Right Position

Placement Exploration

Seeds



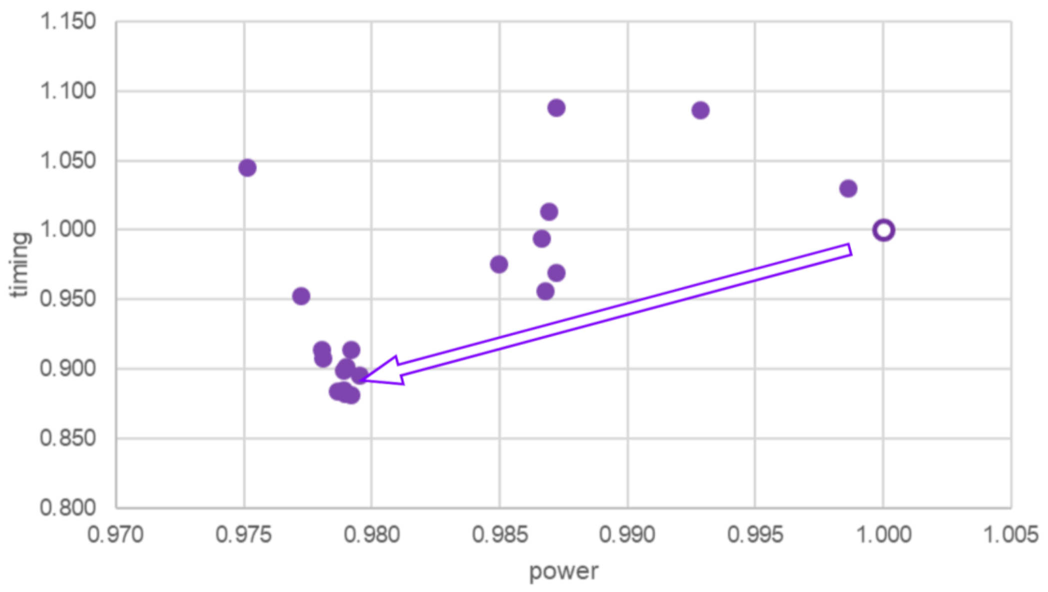
Placement Results



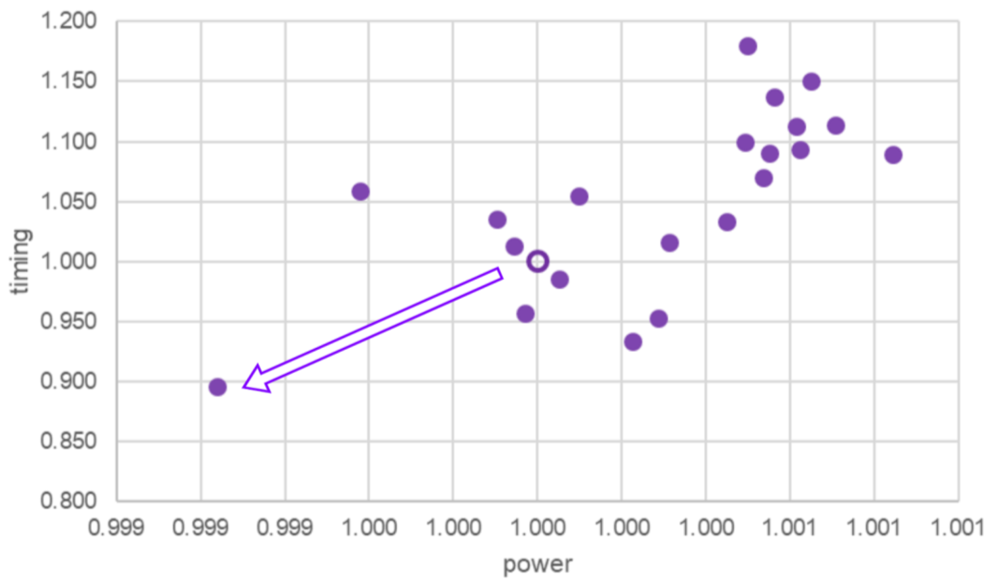
PPA Improvement through Placement Exploration

Achieved Better Timing and Power

Case 1



Case 2

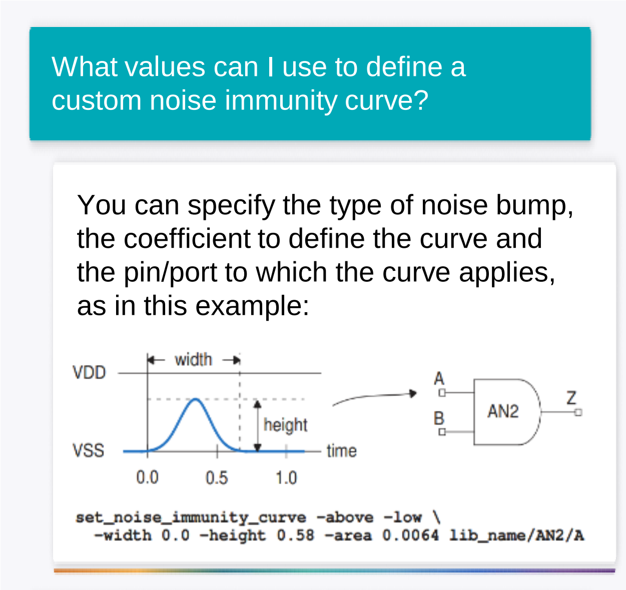


Summary

Recap: AI-Driven Productivity Enhancement

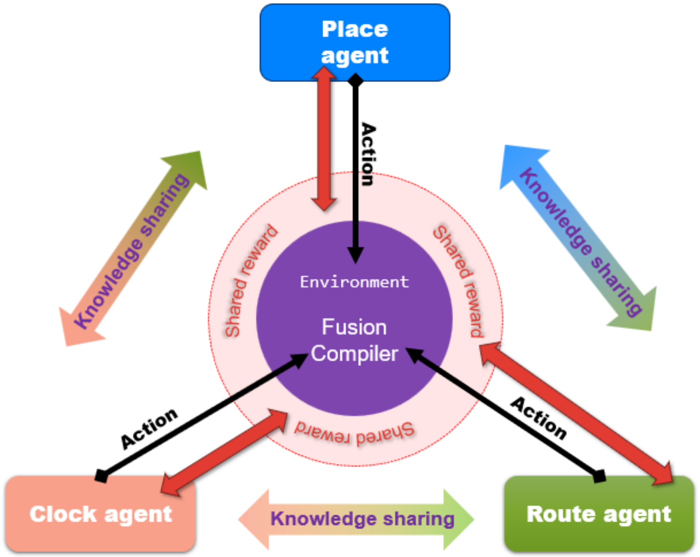
Copilot

- Knowledge assistance to answer expert questions



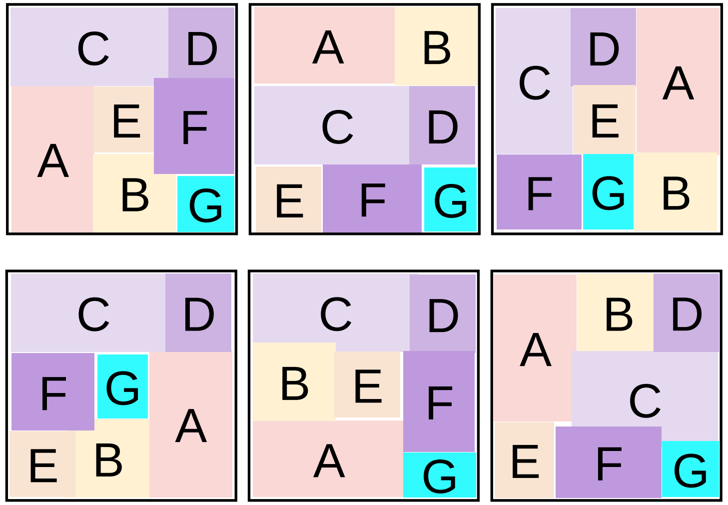
Design Space Exploration

- AI-driven autonomous design optimization



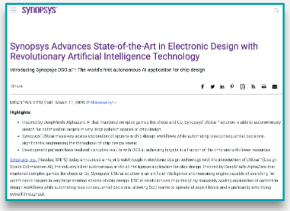
GPU Acceleration

- PPA improvement through placement exploration



Synopsys – Leading the Era of AI-driven Chip Design

2020



Synopsys introduces DSO.ai, world's **first AI** application for chip design

DSO.ai named **Innovative** Product of the Year by EETimes

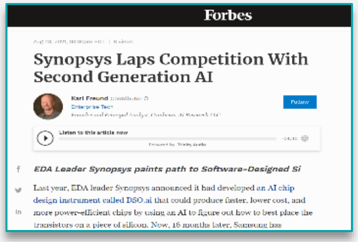
2021

World productivity record:

10 blocks
-9% total pwr
ONE engineer

Wired: World's first **AI-designed** chip design

2022

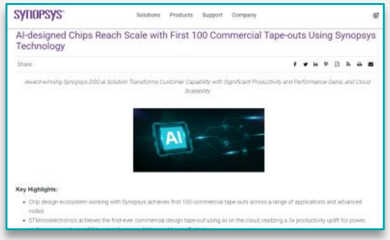


Record adoption:

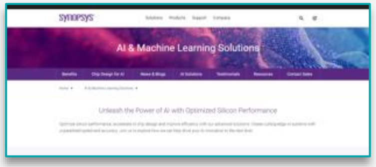
9 of Semi Top-10

100% Better Results

AI-designed Chips cross **100 Commercial Tape-outs** with DSO.ai



2023



Synopsys.ai

Industry's first AI driven EDA suite – Design, test, verification, manufacturing

AI-designed Chips cross **450 Commercial Tape-outs** with DSO.ai

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THANK YOU

Our Technology, **Your Innovation**™