Synopsys TestMAX - Our Technology is Your Innovation

Shanshan Zhou
Solutions Engineering, Sr Manager
Synopsys

Key Test Challenges

Key Test Challenges of Advanced Designs

Turn-around Time

Requirements

Scalable Test Methodology

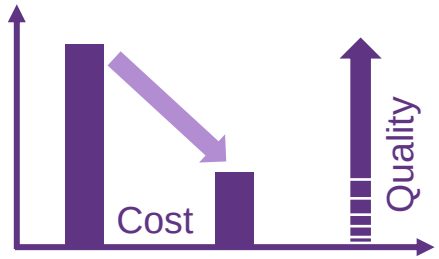
Maximize Shift-left into RTL

Fast Runtime & Iterations

Hierarchical Test

Physical Design Scalability

Test Cost and Quality



Requirements

Minimize Manufacturing Test Time

Minimize Pattern Volume

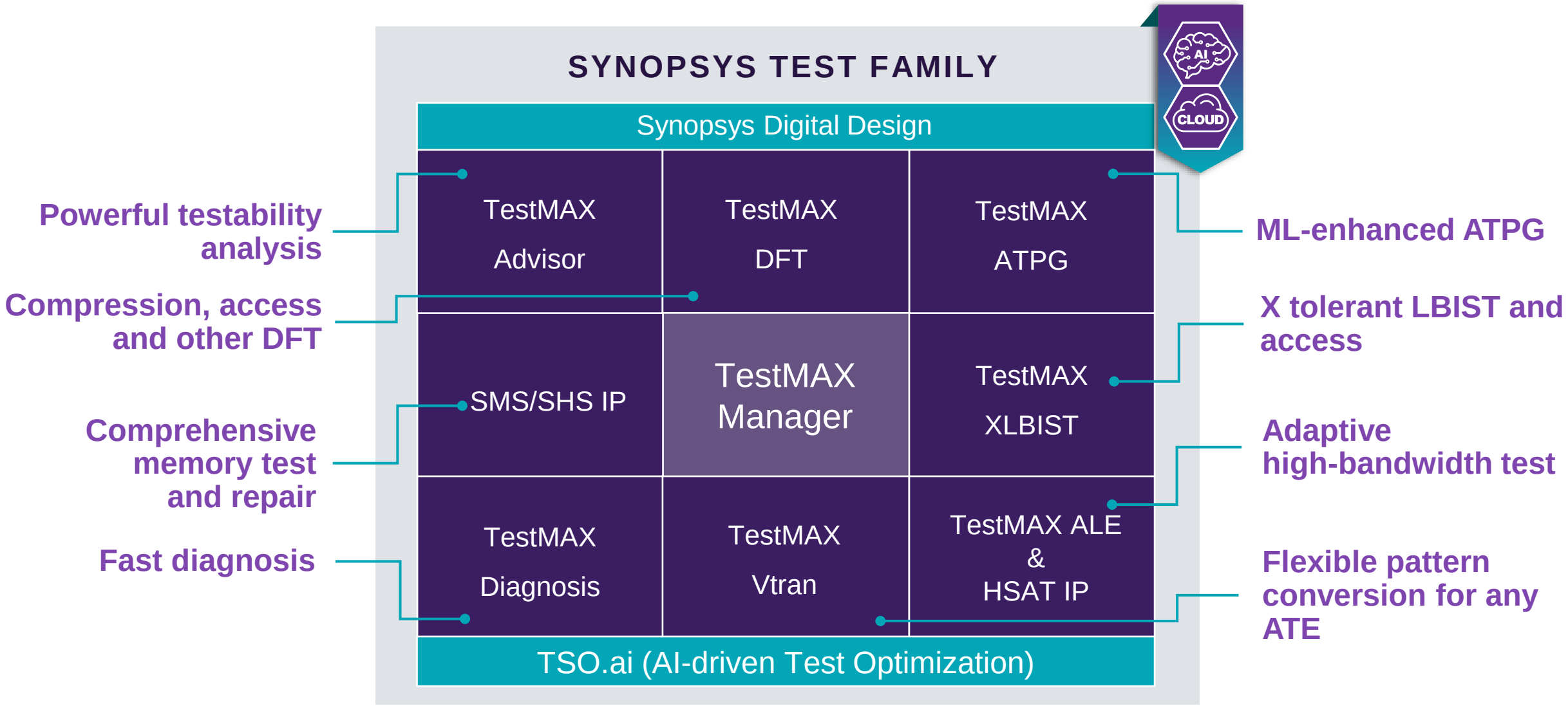
High Defect Coverage

In-system Test Time and Coverage

Advanced Fault Models

TestMAX Overview

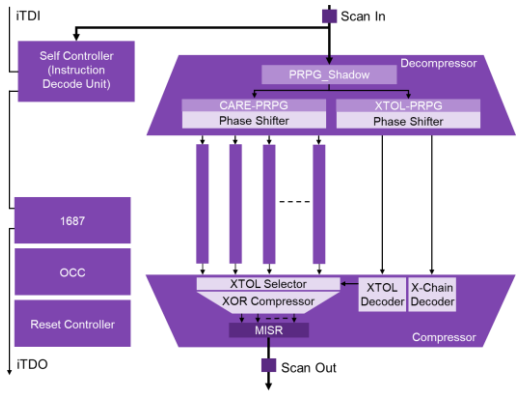
Synopsys Test Family



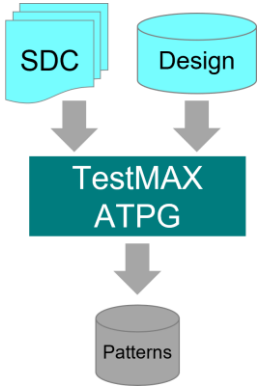
TestMAX End-to-End Solutions

Scalable End-to-End Test Solution Advancements

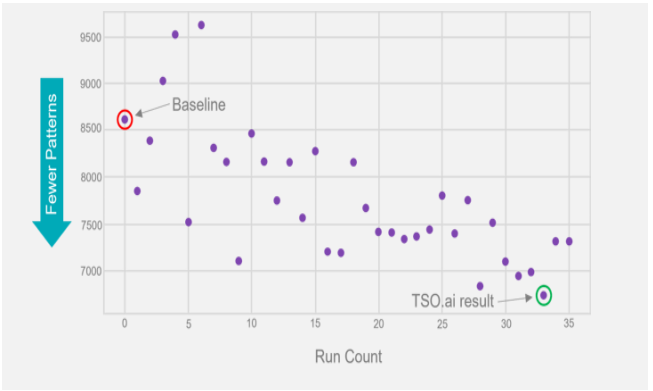
Unified CODEC Architecture (SEQ/XLBIST)



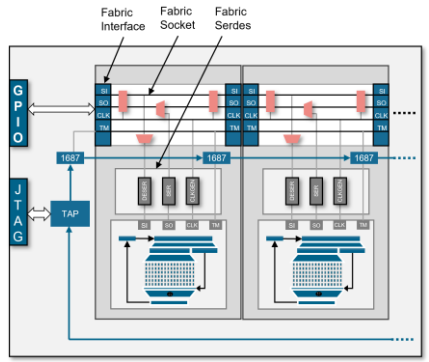
Core ATPG Advancements



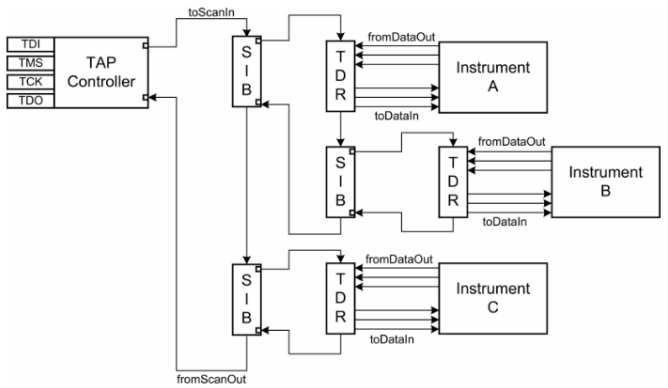
Advanced Test (TSO.ai)



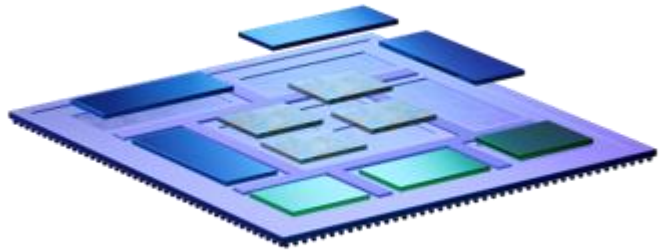
Improved Hierarchical Test & Pattern Porting



Unified Test Architecture with 1687



Multi-Die Testability



Unified CODEC Architecture (SEQ/XLBIST)

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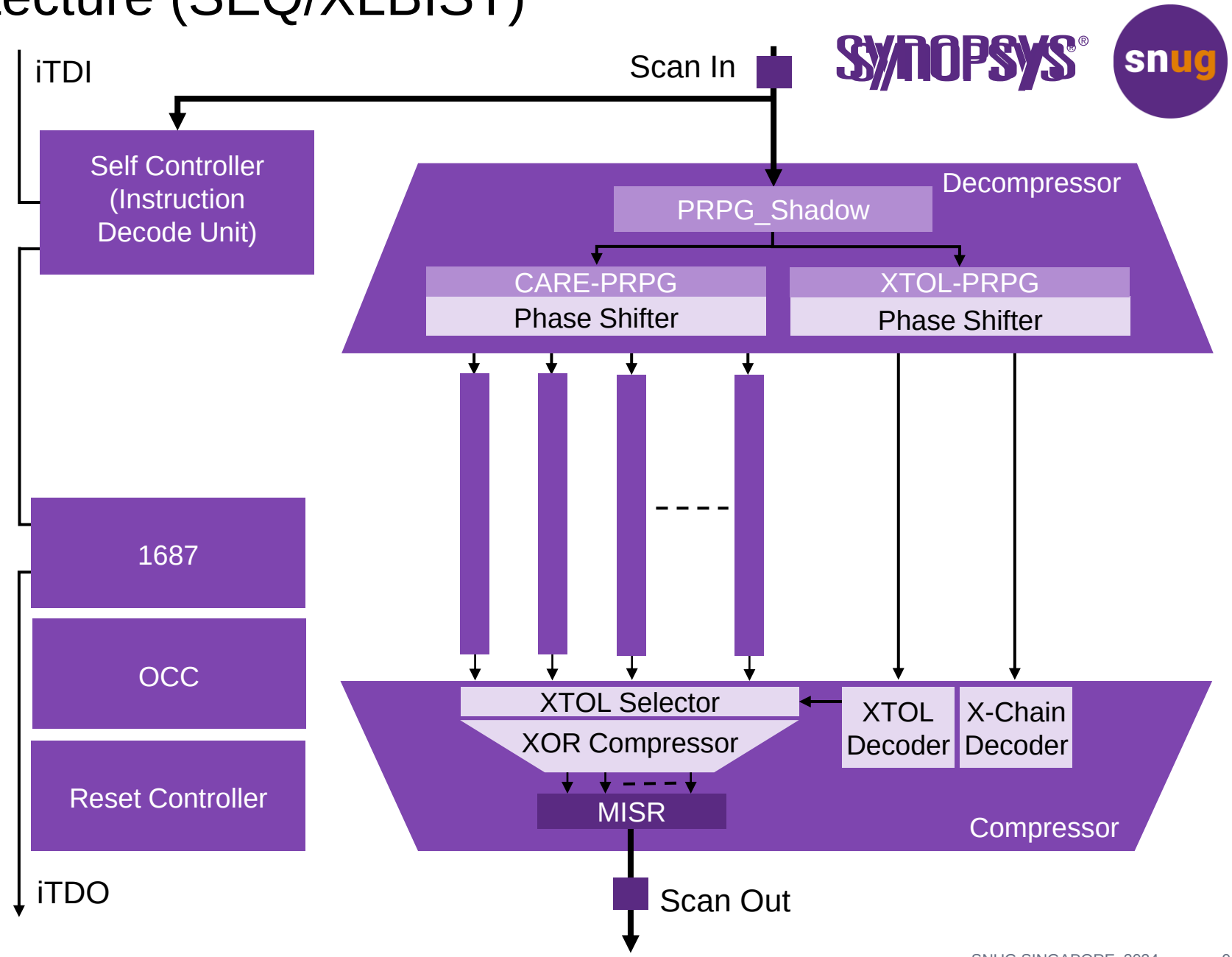
- Deterministic test with scan interface
- In-Field LBIST with 1687 interface
- Configurable MISR Unload
  - MISR Unload per Pattern (MUPP)
  - MISR Unload per Shift (MUPS)
  - MISR Unload per Test (MUPT)
- Full resolution during Chain and Logic test diagnosis
  - High Mappable patterns
    - Force XTOL patterns
    - Lossless Mapping Patterns
- High resolution pattern
- Transform pattern



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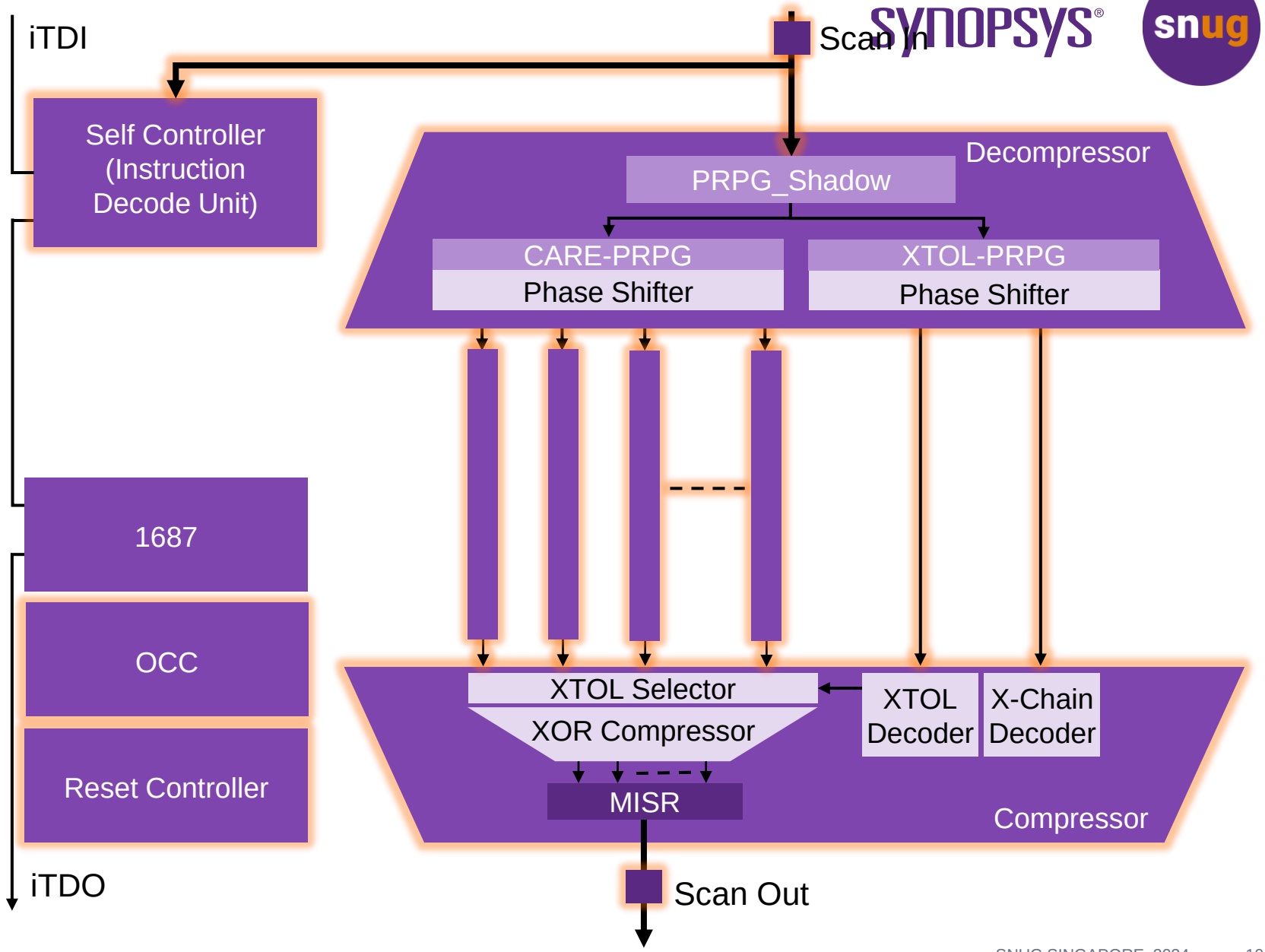

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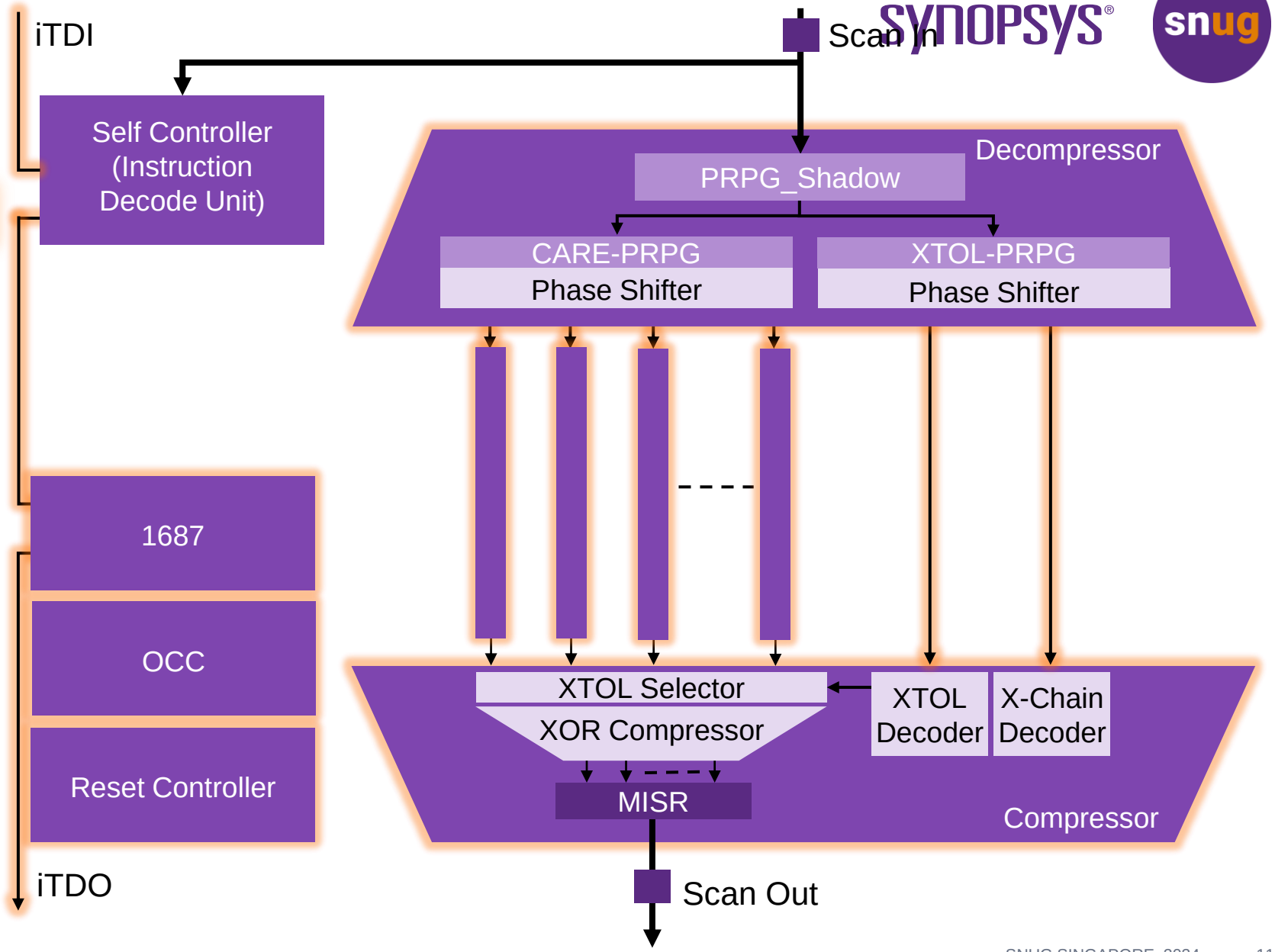

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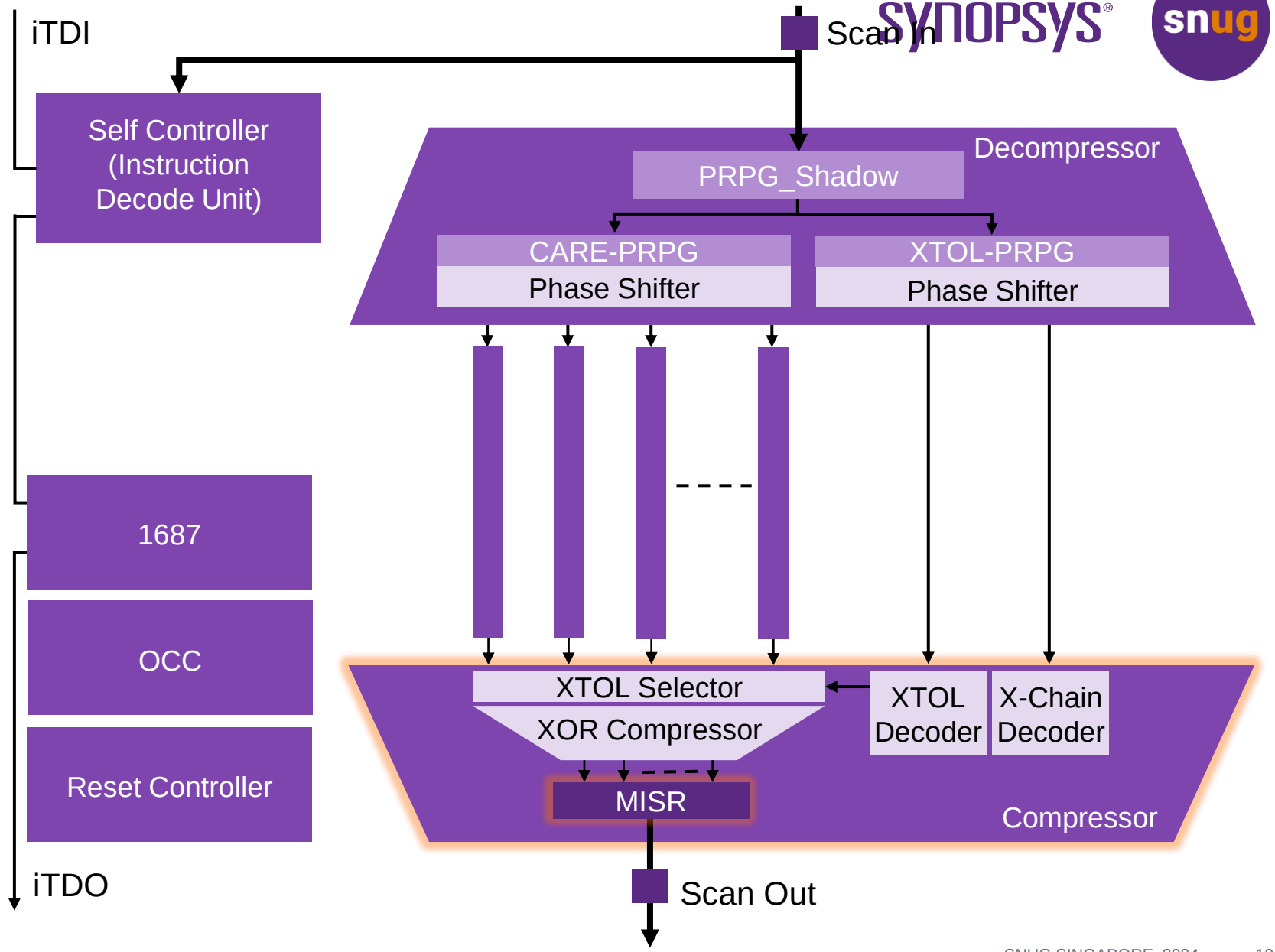

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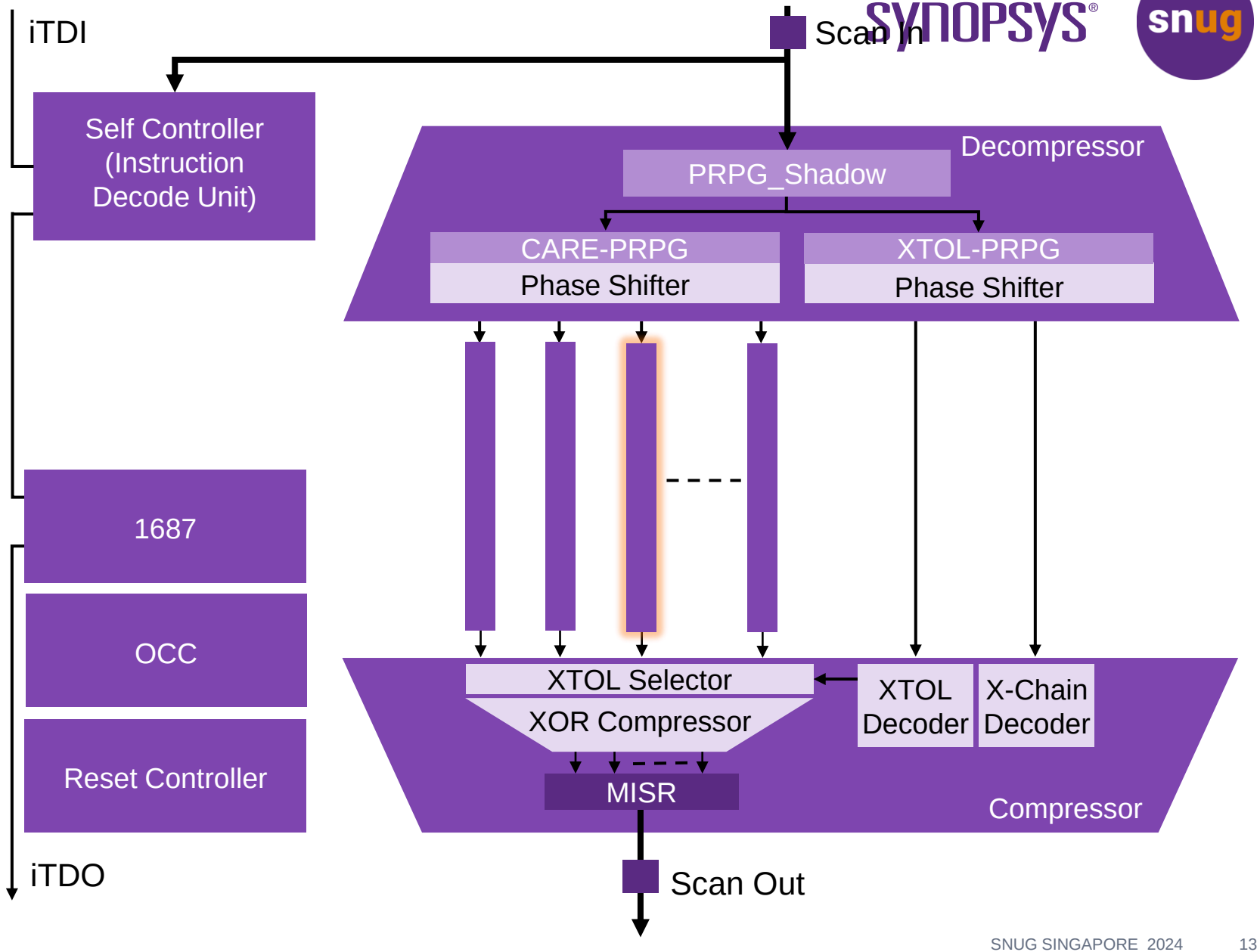

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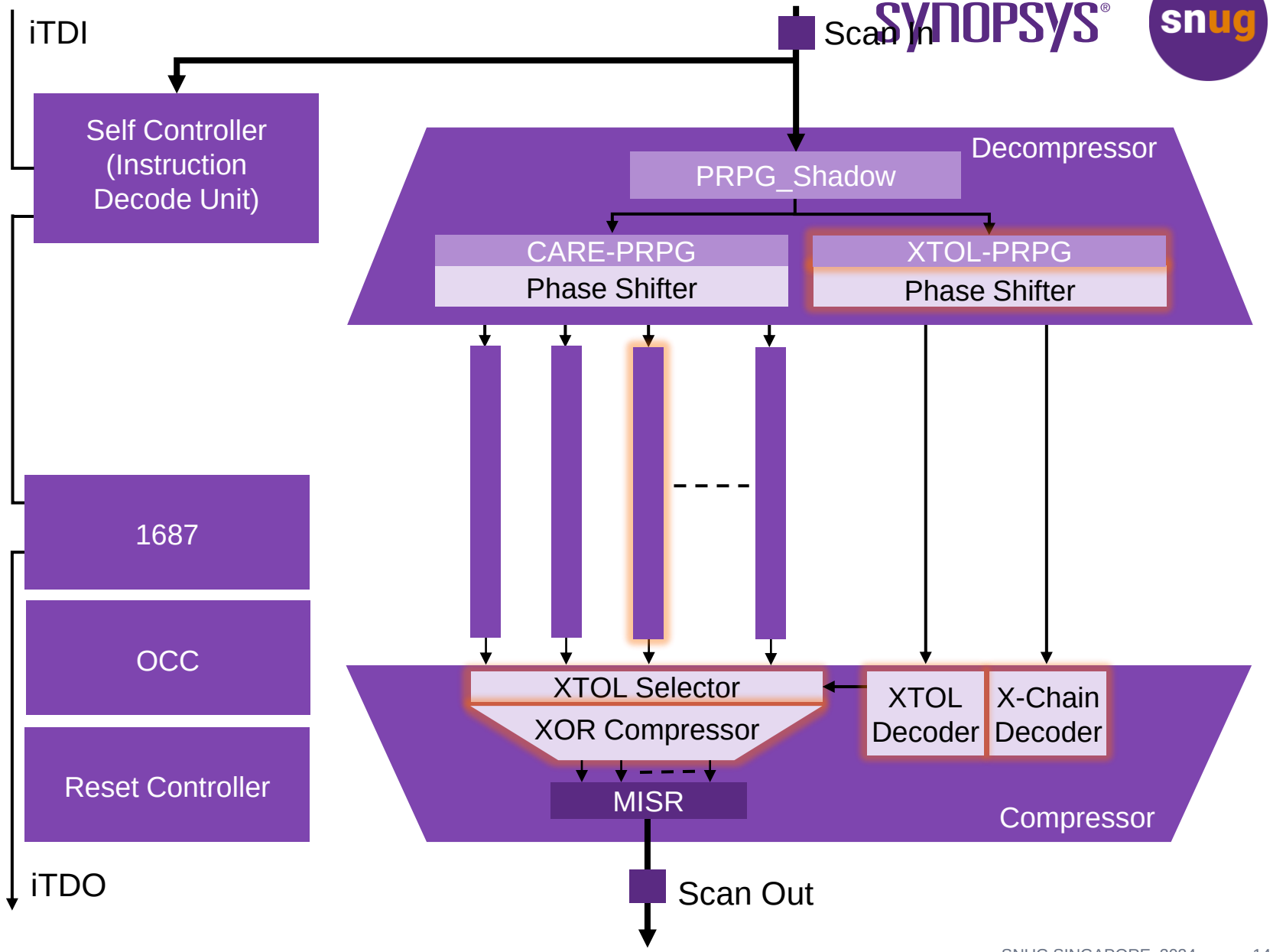
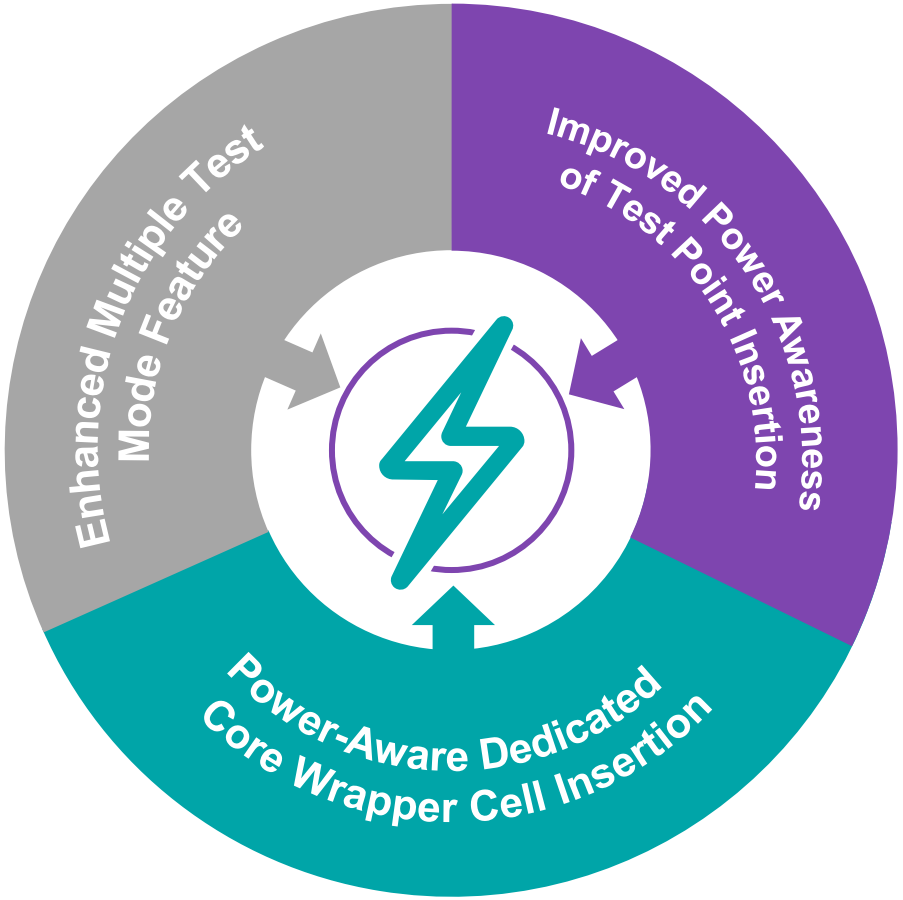


Optimized DFT Synthesis with Fusion compiler

- Fine grain control over scan architecture: Scan chain for each mode are architected separately



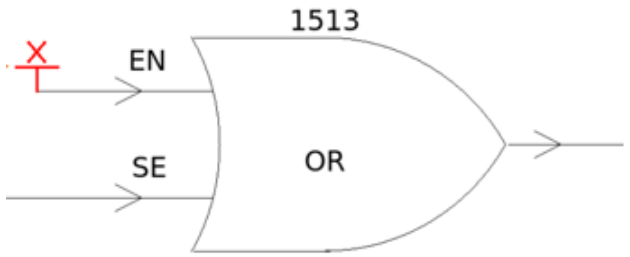
- Test point insertion is more power-aware
- Test Points (TP) rejected if causing MV issue due to
  - User clock Specified to TP
  - Location of TP
  - Tool selected control signal

- Dedicated core wrapper cells insertion with Multi Voltage intent

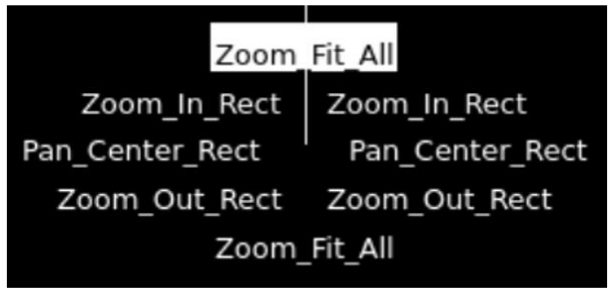
Targeting multi voltage domain designs

Core ATPG Advancements

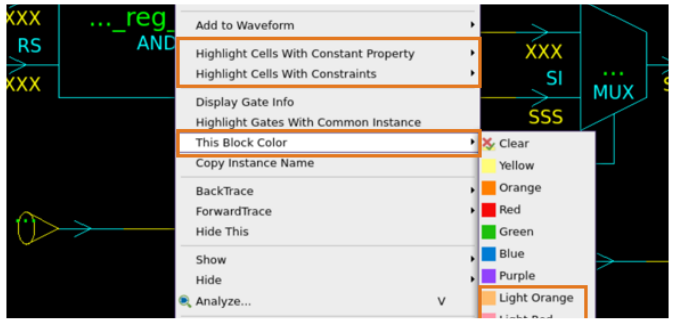
Enhancements to TestMAX ATPG GUI



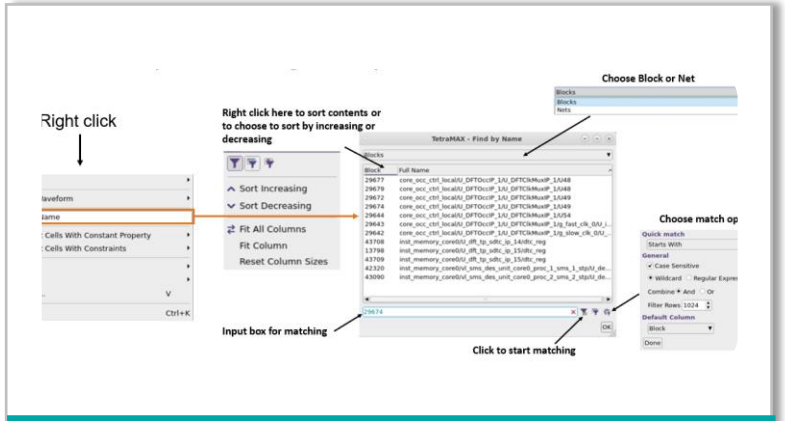
Symbols (Gate and Tied symbols)



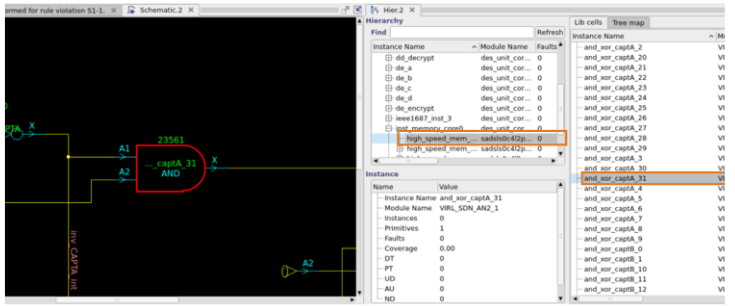
Operations (Flexible zoom in/zoom out)



Highlight
(More colors & Expanded fanin fanout)

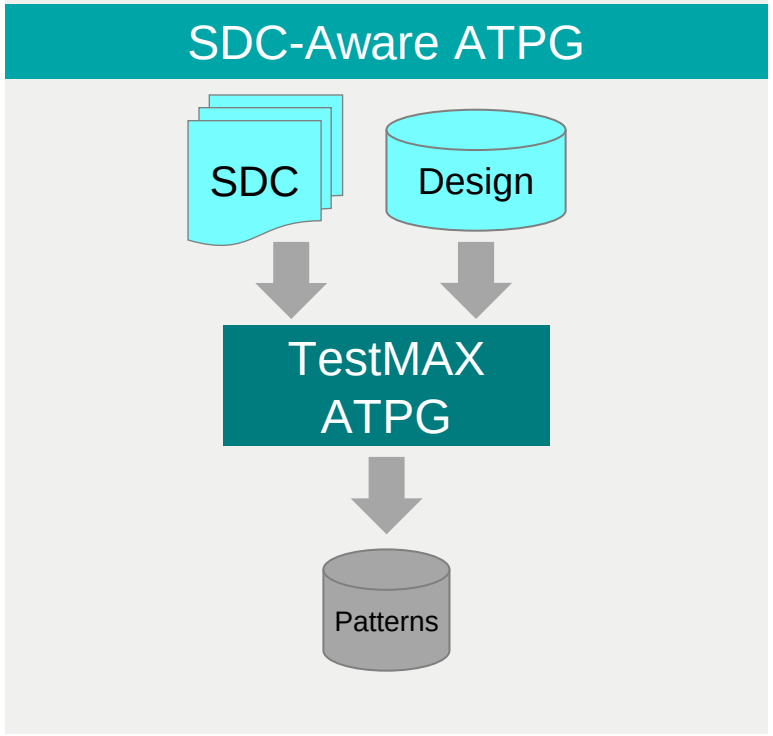


Find by name
(Support search gate by name or ID)



Show in Hierarchy (Interactive between schematic and hierarchy browser)

SDC Aware ATPG



- SDC source points are controlled to constant during ATPG reducing X propagations for higher QOR
- Observed 15% pattern reduction with SDC present

Advanced Test

TSO.ai

Synopsys.ai: Industry's First Full-Stack, AI-Driven EDA Suite

For design, verification, testing & manufacturing of digital and analog chips

- System Architecture
- Design Capture
- Verification
- Implementation
- Signoff
- Test & SLM
- Silicon Manufacturing

Design Space Optimization	Achieve power, performance and area (PPA) targets, and boost productivity with DSO.ai
Verification Space Optimization	Faster functional testing closure, higher coverage and predictive bug detection with VSO.ai
Test Space Optimization	Automated test generation resulting in fewer, optimized test patterns with TSO.ai
Analog and Manufacturing	Rapid migration of analog designs and development of lithography models

Advanced DFT and ATPG with AI/ML

DFT Optimization

Coverage and Pattern Optimization

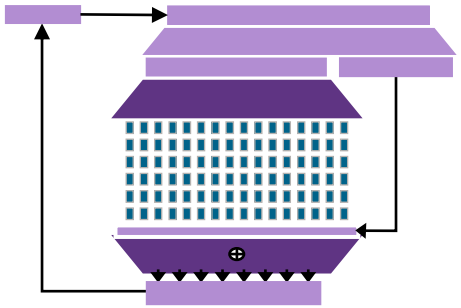
Faster TAT
Optimal Codec

Lower Patterns
Higher Coverage

Optimal Production
Patterns

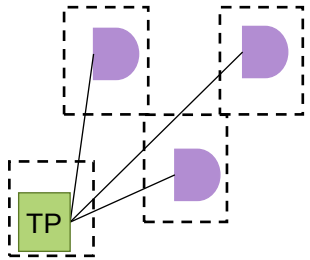
Faster Runtimes With
Same Coverage

TSO.ai – Test Configuration*



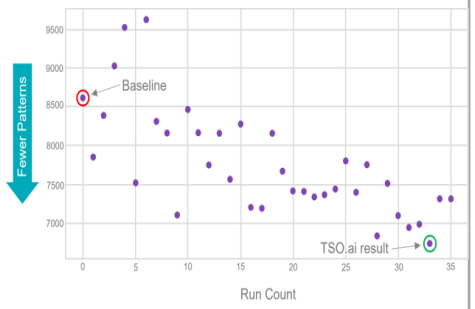
Intelligent Configuration Analysis

TSO.ai – TestPoints**



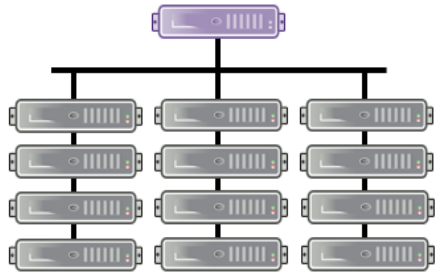
Intelligent TestPoint Selection

TSO.ai - ATPG



Intelligent Minimal Pattern Search

TSO.ai w/ Distributed ATPG*



Accelerate Time-to-Results

AI Database

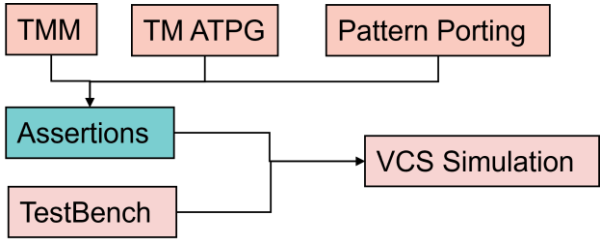
***Beta** ****Roadmap**

Improved Hierarchical Test & Pattern Porting

De-bug / Validation

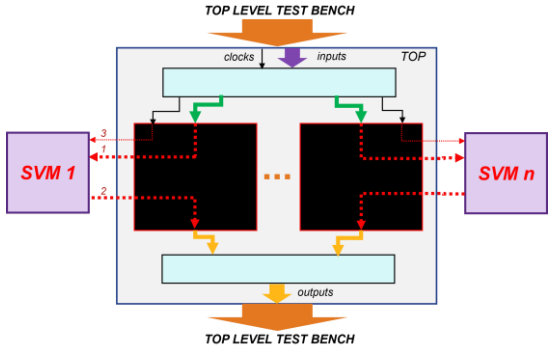
Hierarchical Test - Improved Pre and Post Silicon Validation

Design Validation with Assertions (Pre-Silicon)



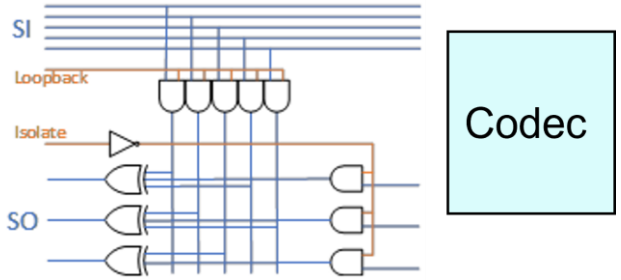
- Validates Post test setup, Streaming Fabric TDRs and Core level constants

Pattern Validation with Scalable Verification Model (Pre-Silicon)



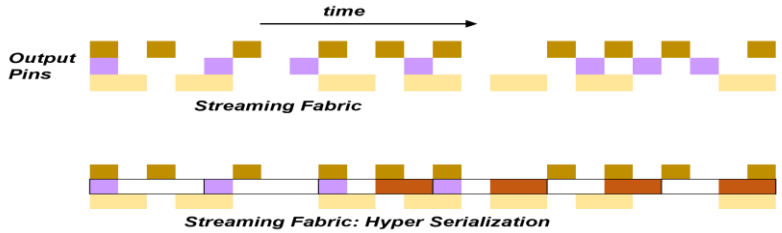
- Replaces core simulation with model of test patterns
- Up to 3x Simulation time speedup
- Up to 1.5x Compile time speedup

Streaming Fabric Self-test Pattern (Post-Silicon)



- Loopback (“Self test” Patterns for Streaming Fabric)

ATE Support for Streaming Fabric (Post-Silicon)



- Fail Core Identification on Tester
- Synopsys Provides Fail Map as part of STIL file
- VTRAN support for Pattern and Fail Map translation

Unified Test Architecture with 1687 to support DFT and SLM IPs

Synopsys DFT Solutions & IPs

SF
Streaming Fabric

SEQ
SEQ Compression

SMS
SMS MBIST

SLM
SLM Sensors

PVT
PVT Sensors

IP
Synopsys IPs

SiB
Custom Instruments

IP
3rd Party Unwrapped IPs

Synopsys DFT Solutions & IPs with 1687 support

Streaming Fabric

SEQ Compression

SMS MBIST

SLM Sensors

PVT Sensors

Synopsys IPs

Custom Instruments

3rd Party 1687 IPs

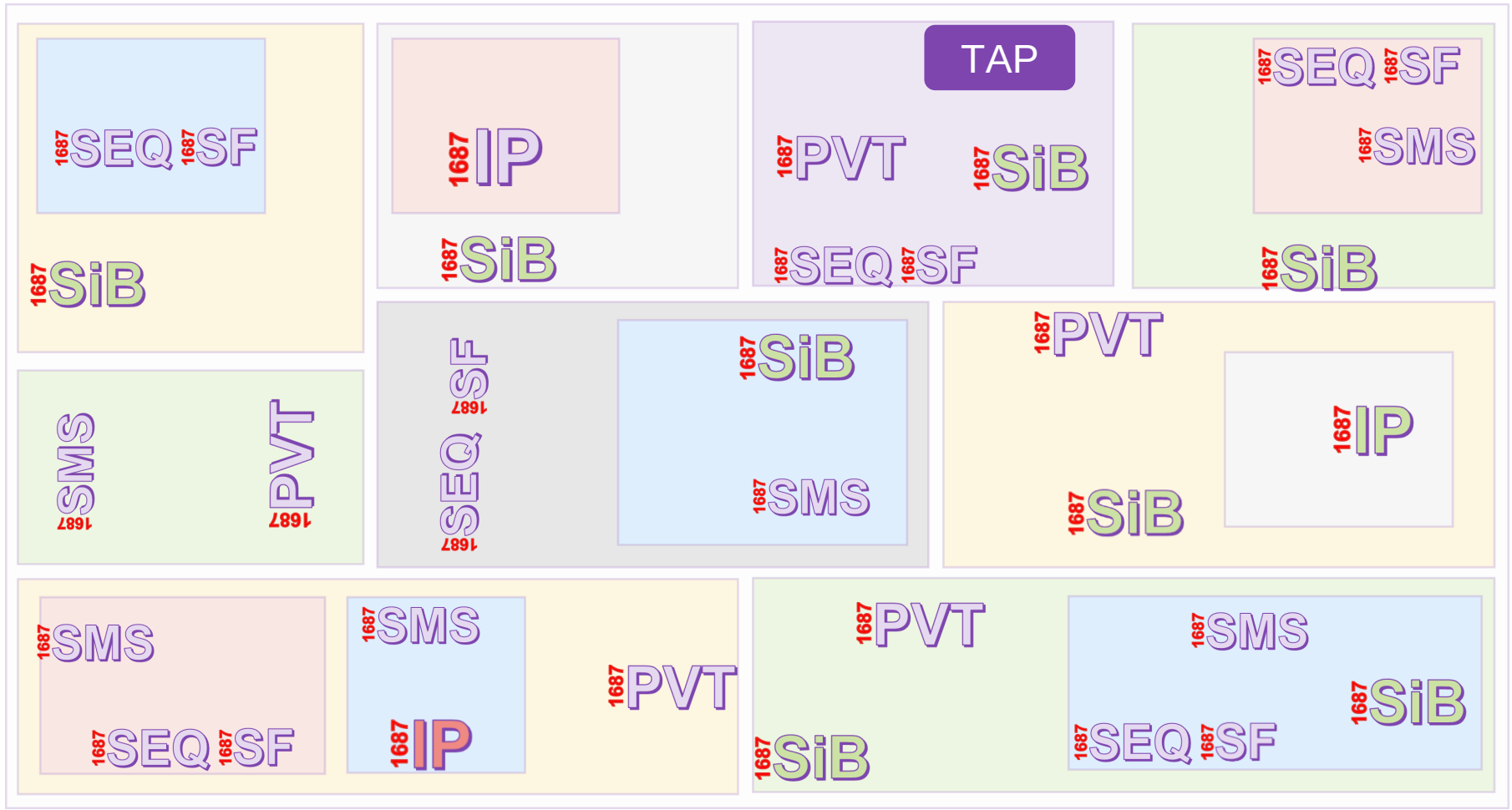
3rd Party TMM Wrapped IPs

Major classification of 1687 Instruments

Synopsys IPs & DFT Solutions

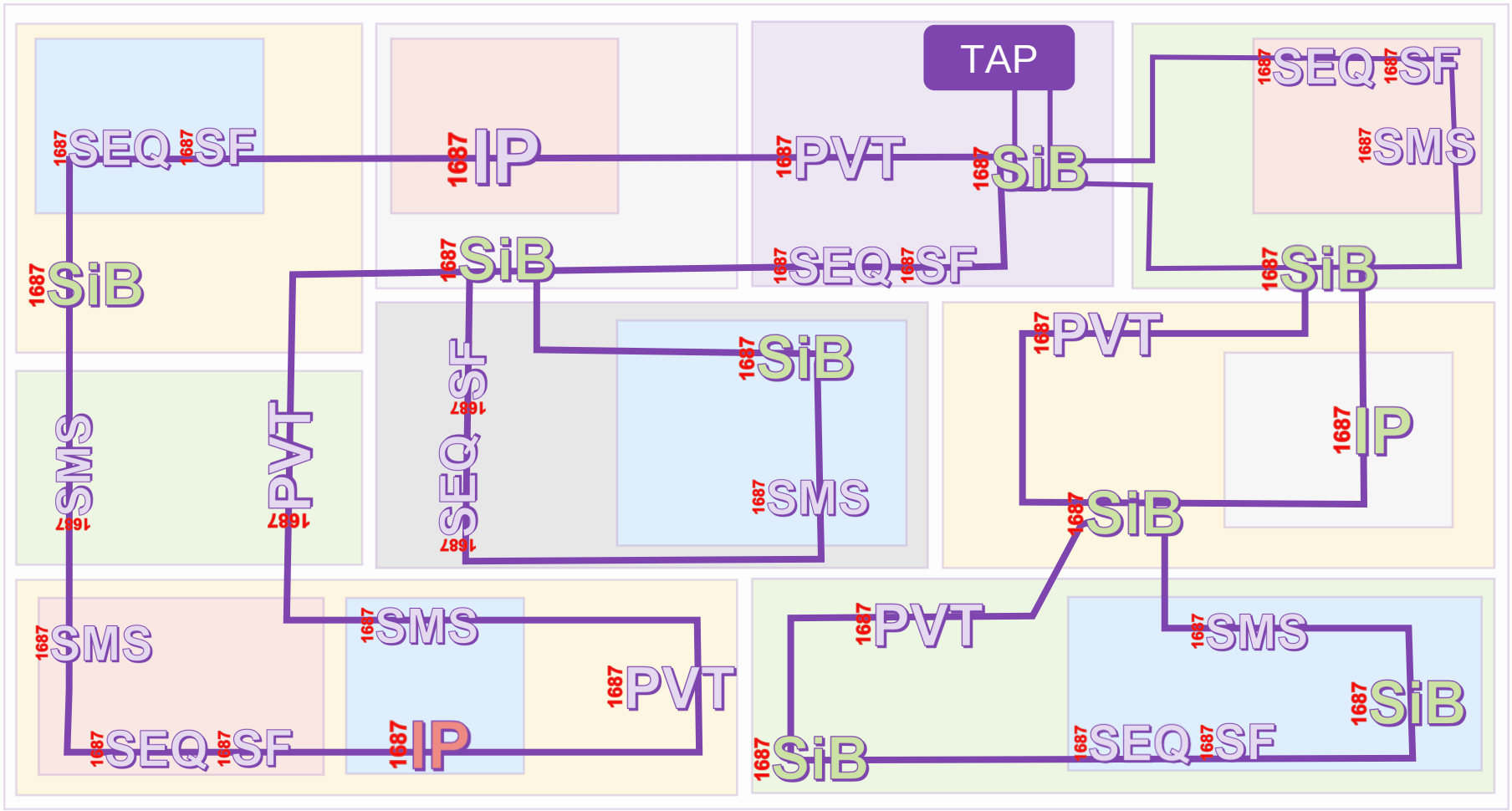
Custom or 3rd Party IPs/Instruments

DFT Implementation in Hierarchical SoC Design



Unified Test Architecture with 1687

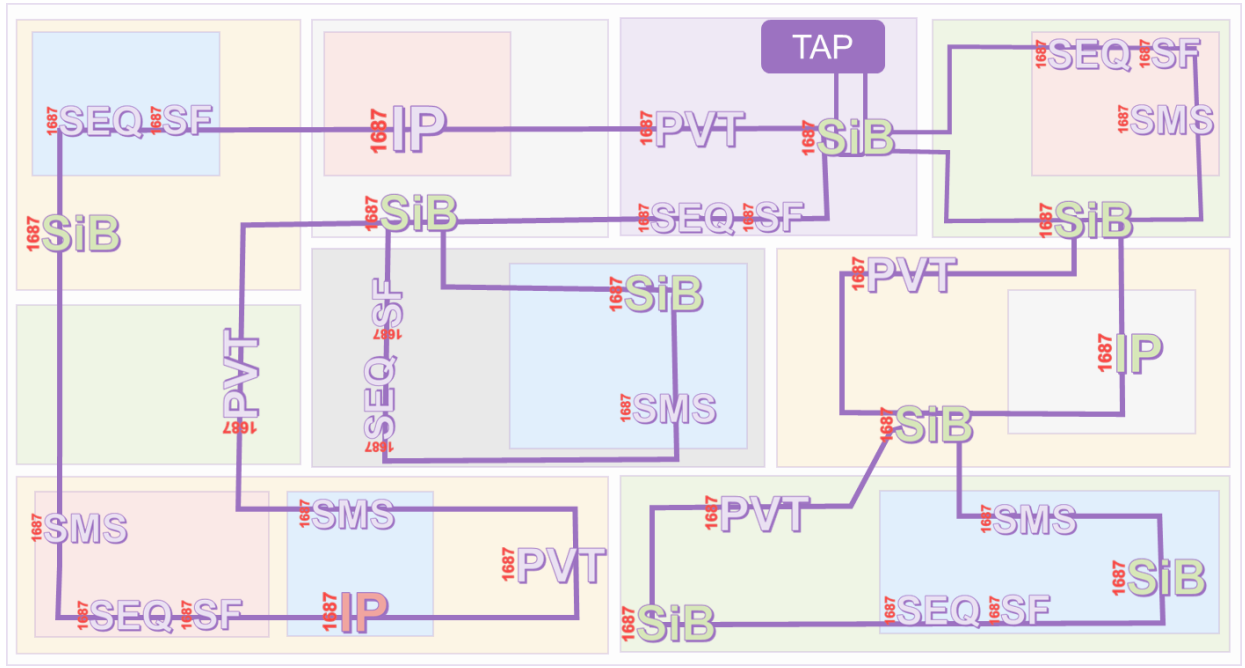
Complex Hierarchical 1687 Implementation



TestMAX IEEE1687 Support

Features and Capabilities

1. **Comprehensive support of the 1687 standard**
2. Top Level or hierarchical **ICL/PDL creation, extraction and validation**
3. Native support for **3rd Party 1687 IPs ICL/PDL**
4. Advance capabilities like **eTAP or Advance secure SiB architectures**
5. TCL based **ICL/PDL database** access for automation scalability

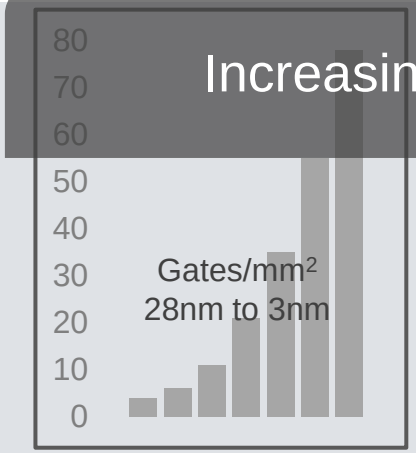


Multi-Die Testability

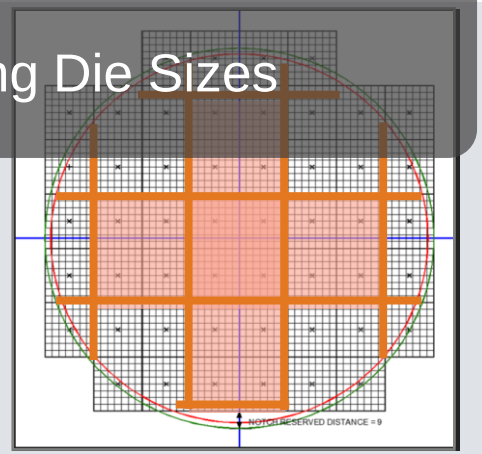
Market Demands Are Driving Multi-Die Design

Bandwidth, performance, power, latency, cost and schedules

Increasing Die Sizes

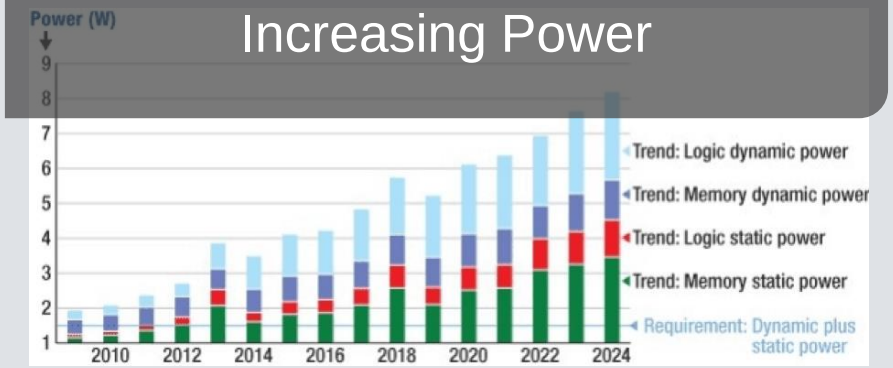


Increasing Functionality



Wafer and reticle size
Max. Stepper ~800 mm²

Increasing Power



Increasing Functionality Integration

...Driving Need for New Multi-die Design Solutions

Multi-Die Chiplet Design and Test

Multi-pronged Challenges

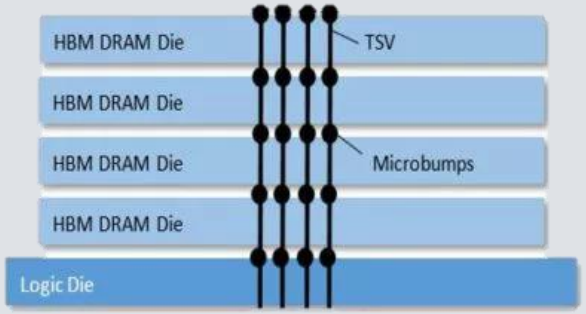
- Die-to-die configurations (3D/2.5D)
  - *Logic-to-Memory*: High-speed memory interfaces
  - *Logic-to-Logic*: High-speed PHY-to-PHY, and non-PHY interfaces
- Multi-Level test, repair, diagnosis, debug…Pre-bond (WS), mid-bond and post bond
  - *Intra-die*: Die level
  - *Inter-die*: D2D interconnect
  - *Multi-die*: Package-level
- Design & Test Automation
  - Multi-Die DFT, D2D interconnect test & stack level access
  - Physical Aware D2D interconnect pattern generation
  - Pattern porting & Multi-die diagnosis

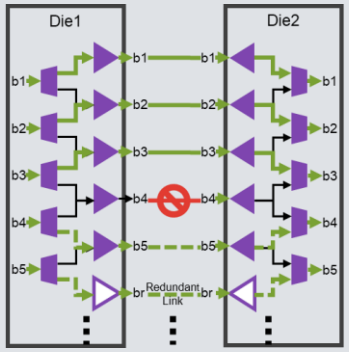
With Substrate / RDL

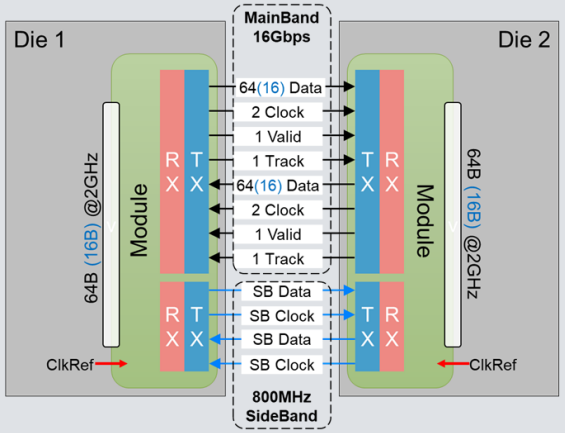
With Si-Interposer / Bridge

With Hybrid Bonding

Die2Die Test & Repair Challenges







Various Design Configuration

- Memory-On-Logic
  - *Post Package Repair for DRAM*
  - *Differentiate between faulty memory die Vs damaged interconnect*
- High Speed Lane Test & Repair
  - *Yield improvement by lane test and repair*
  - *Planning for Repair Logic and Spare Lanes*
  - *Performing various levels of loopback tests*
- UCIe Based Die2Die High Speed Interfaces
  - *Probing challenge for advanced packages (~25un)*
  - *No additional DFT ports at for stack-level test*
  - *Lane redundancy & remapping for multiple corners*

Synopsys Enabling Quality, Reliability and Yield for Multi Die

Optimized for Synopsys PHY IP's

Support for IEEE 1838

- DFT access architecture
- **Individual dies and D2D interconnects test**
- Integration with on-chip hierarchical management

UCIe MTR
Test, Monitoring, Repair

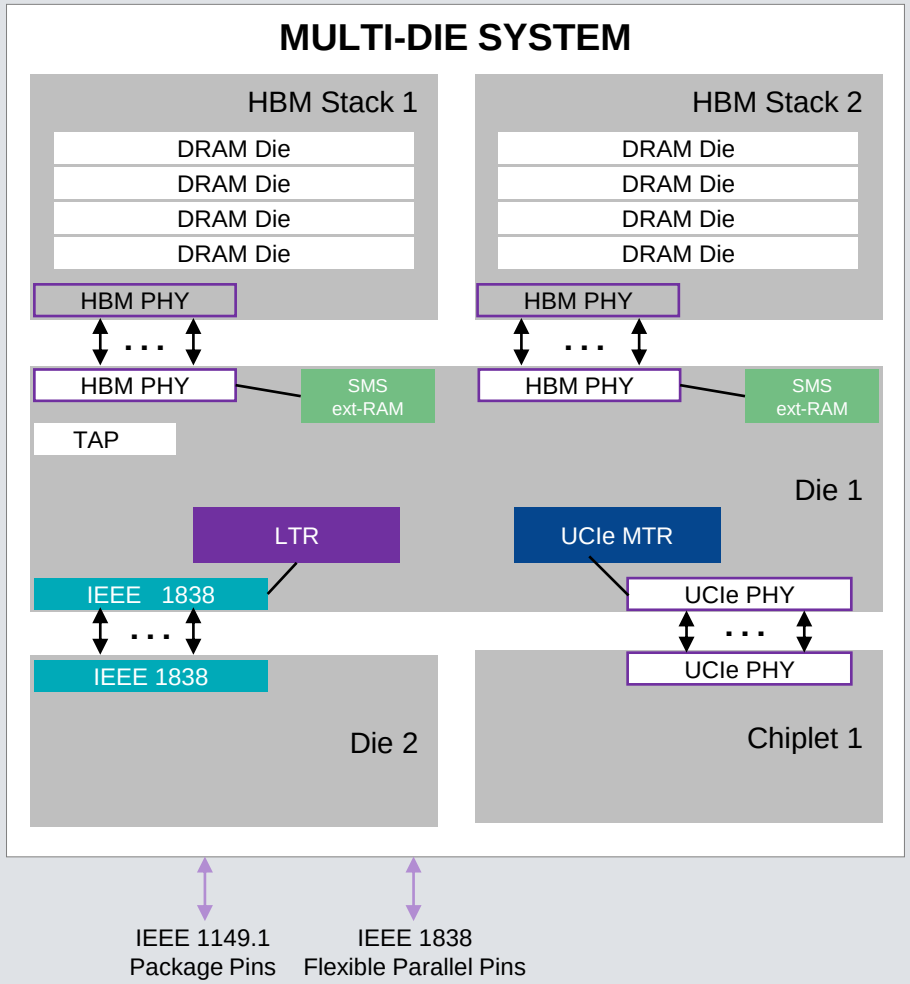
- Supports **logic-to-logic PHY** standards UCIe (or HBI/AIB)
- **At-speed inter-die lane test, monitoring & repair**
- Chiplet-level TMR, calibration

SMS ext-RAM

- Supports **logic-to-memory PHY** standards (HBM, DDR)
- **At-speed interconnect test, repair**
- Programmable at-speed External DRAM test
- System level repair, calibration

Lane Test & Repair (LTR)

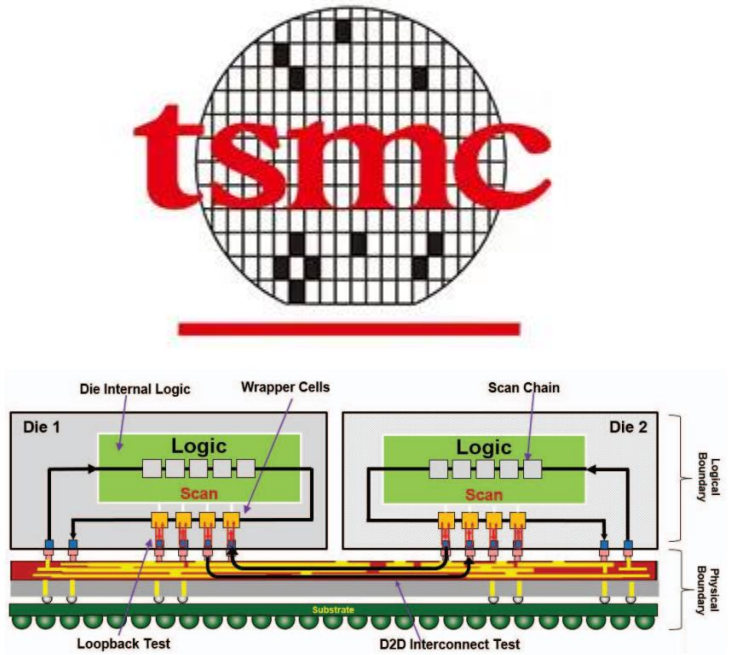
- Provides **system level Built-In Self-Test for D2D high-volume lanes**
- Performs reconfiguration & repair using redundant lanes

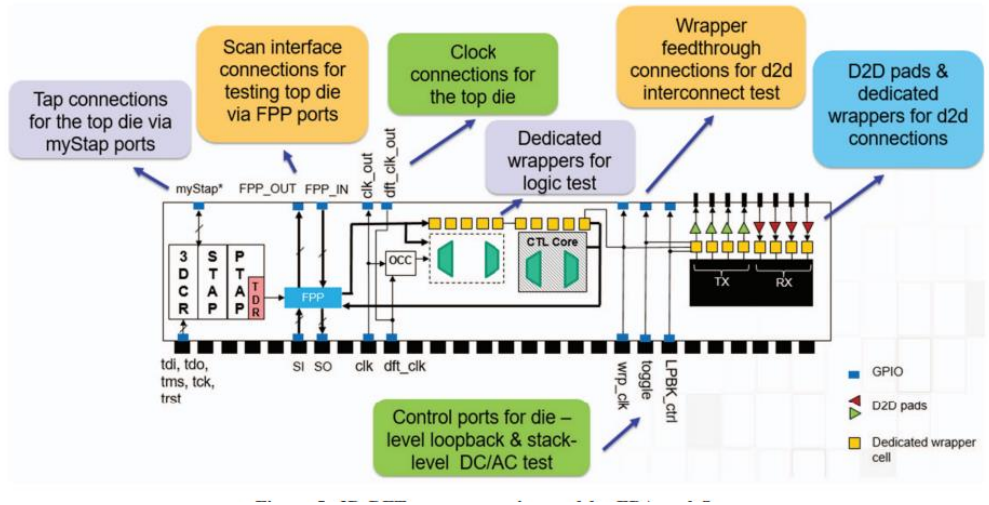


NEW→ TSMC Multi-Die @ITC 2023

ITC 2023 — 2023 IEEE International Test Conference
8-13 October 2023
Disneyland, Anaheim, CA

A Case Study on **IEEE 1838** Compliant Multi-Die **3DIC DFT** Implementation



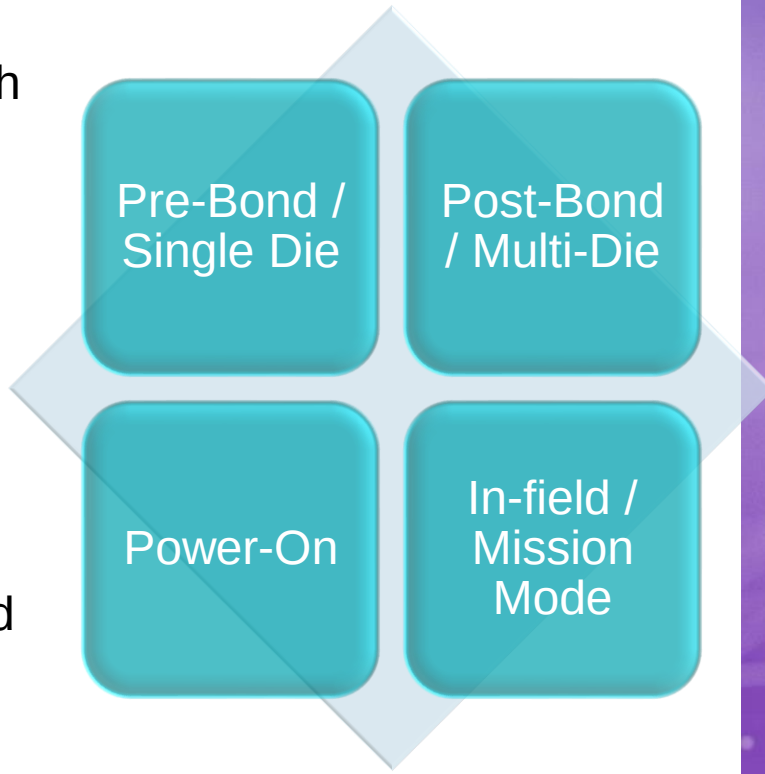


3D DFT components inserted by EDA tool flow.

"We used **the Synopsys TestMAX** tool suite for automatic insertion of 3D DFT logic. Synopsys TestMAX suite provides a comprehensive set of tools to seamlessly insert and validate the test logic outlined in **the IEEE 1838** standard for **3DIC test** at both die and stack level."

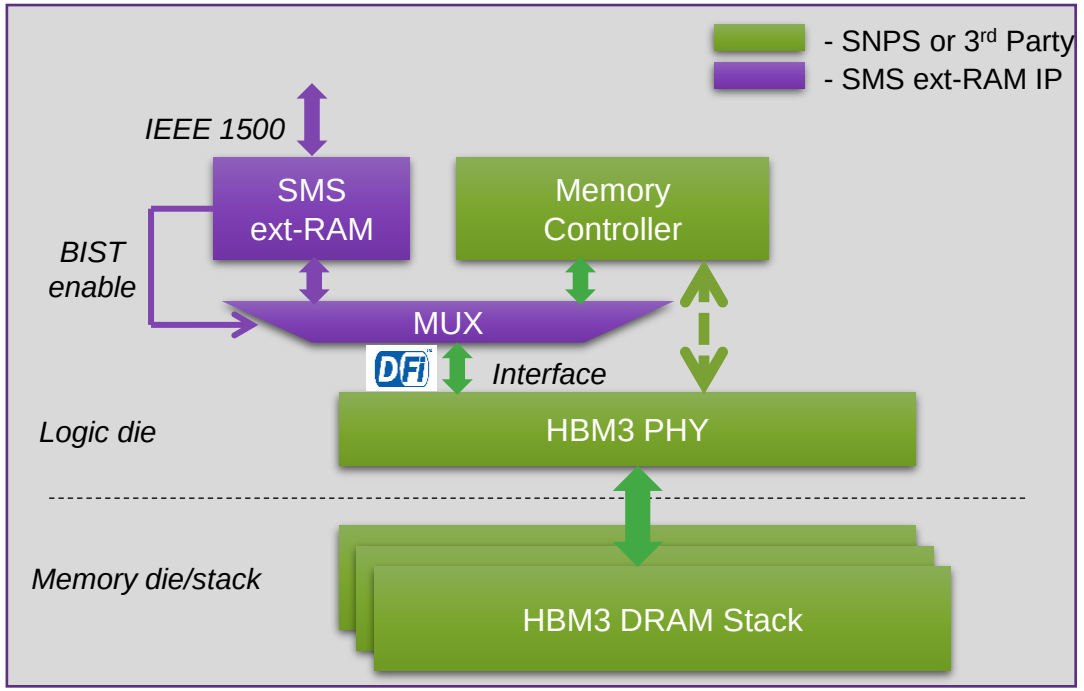
NEW→ TSMC Multi-Die Collaboration

- **TSMC-Synopsys Multi-die Collaboration early results announced at TSMC OIP – Sept 2023**
- Leveraging UCIe for High-Speed Stack Testing of Multi-Die Systems through Monitoring, Test & Repair (MTR) and HSAT IPs
- Two configurations:
  - Die-to-Die communication via high speed **UCIe using MTR**
  - Die-to-Die communication via GPIO using **IEEE1838**
- Both configurations also support full execution of test, monitor, debug, and repair capabilities, utilizing on-chip resources such as SMS IP for embedded memory blocks; and SHS and MTR IP for UCIe blocks
- Includes pre-bond and post-bond manufacturing stages, in-field power-on stage, and periodic mission health monitoring stage
- Multi-die system leverages **TSMC's** CoWoS interposer technology



Extensive SMS ext-RAM IP (Logic-to-Memory) Test Adoption

Application	Customer Region	Protocol Support	Foundry and Tech	Status
Cloud/ Networking	NA	LPDDR4X	GF14LP	Delivered in 2020
Enterprise	NA	LPDDR 5/4/4X (6400 max)	TSMC N7	Delivered in H2 2021
Cloud	China	DDR54	TSMC N7	Delivered in early 2022
HPC	China	DDR54 (6400 max)	TSMC N5	Delivered in early 2022
Enterprise	Japan	HBM2	TSMC N7	Delivered in H1 2022
Cloud	NA/Israel	DDR5 (max 6400)	TSMC N5	Delivered in H2 2022
Enterprise	NA	DDR54 (6400 max)	TSMC N5	Delivered in H2 2022
Enterprise	NA	Support for JESD209-5B for LPDDR5 and 5X (6400 max)	TSMC N7	Delivered in H2 2022
AI/ML	EU	LPDDR5/5X (max 6400)	TSMC N7	Delivered in early 2023
Enterprise	NA/Israel	LP4X/LP5 (6400 max)	TSMC N5	Delivered early 2023
Enterprise	NA	DDR5 (max 8400)	TSMC 3E	Delivered in H1 2023
Cloud	NA	DDR5 (max 7200)	TSMC N5	Delivered in H1 2023
AI/ML	NA	DDR54 (max 5600)	TSMC N5	Delivered in H1 2023
Enterprise	NA/Israel	LPDDR5/5X (max 6400) with PPR	TSMC N5	Delivered in H2 2023



Summary

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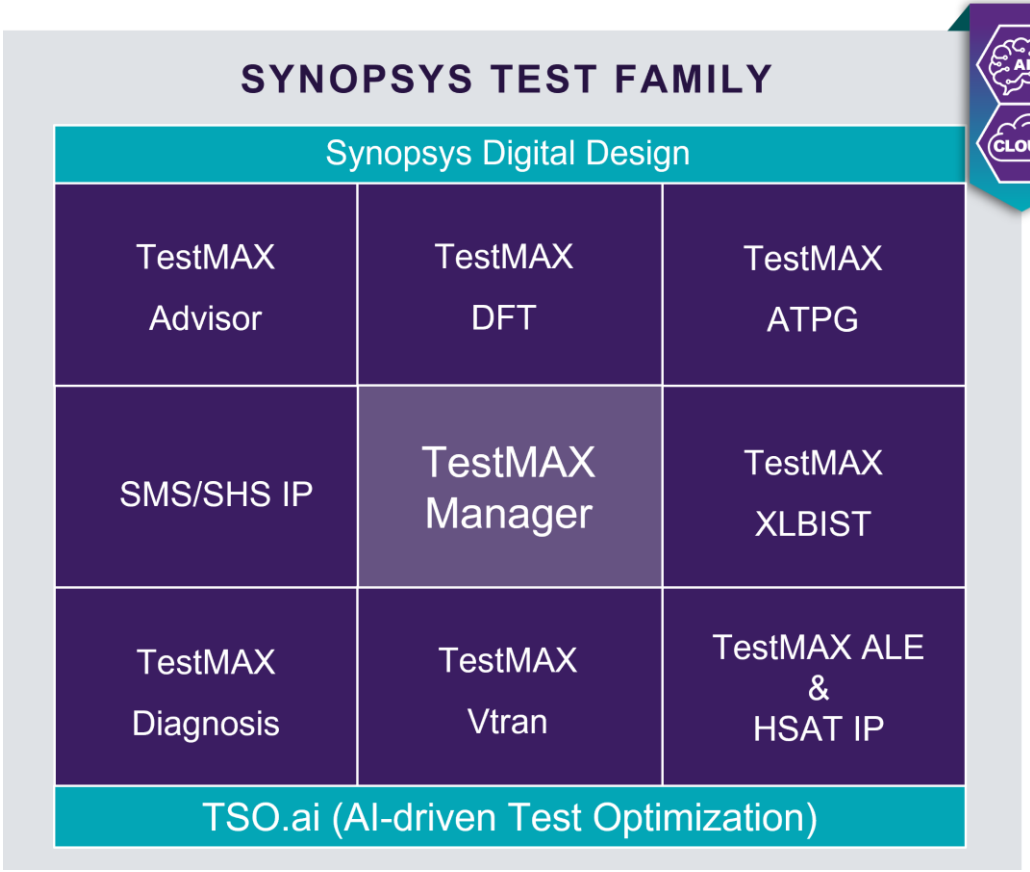
- Scalable end-to-end test solution with Streaming Fabric, SEQ/XLBIST & HSAT
- Industry first AI-Driven Test Solution
- Unified test architecture with 1687
- Pioneering Multi-Die monitoring, test and repair solutions across the silicon lifecycle



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