IC Validator

2X Faster with ½ Resources

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Agenda

- Challenges at advanced nodes
- Why IC Validator
- Customer case studies
- Technology differentiators
- ESD solution
- License package

Challenge


DECIDING WHERE TO EAT


LONG CAI FAN QUEUES


DISAPPEARING FOOD


BOJIO BUBBLE TEA

Solution

Where to Eat?

Long Cai Fan Queues

SYNOPSYS® snug

MAXIMISE YOUR CAI PNG ORDER

ORDER MOST EXPENSIVE DISH FIRST

Seafood or Fish > Meat > Veggies

CHOOSE DISHES CLOSE TO EACH OTHER

Make it easier for the person scooping

LINGER WHEN CHOOSING

Keep pointing and you might get more

LOOK FOR DISHES THAT'RE RUNNING OUT

Might get everything + something extra!

ASK FOR "A LITTLE MORE RICE"

Not "Add Rice"

ORDER LESS QUANTIFIABLE DISHES

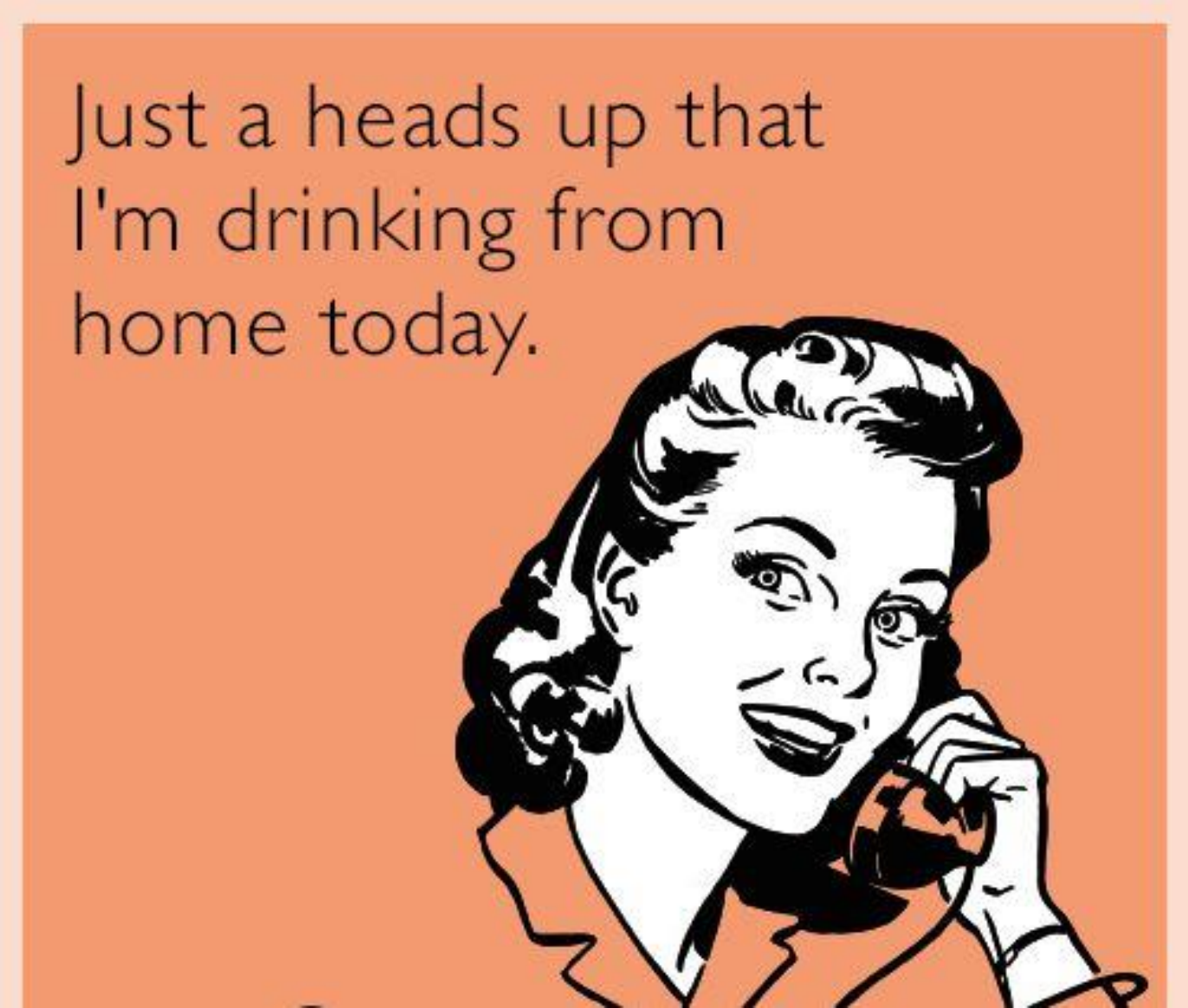
Sweet & Sour Pork vs a whole Pork Cutlet

or get the economic rice auntie to like you...

Seedly Reads

Disappearing Food

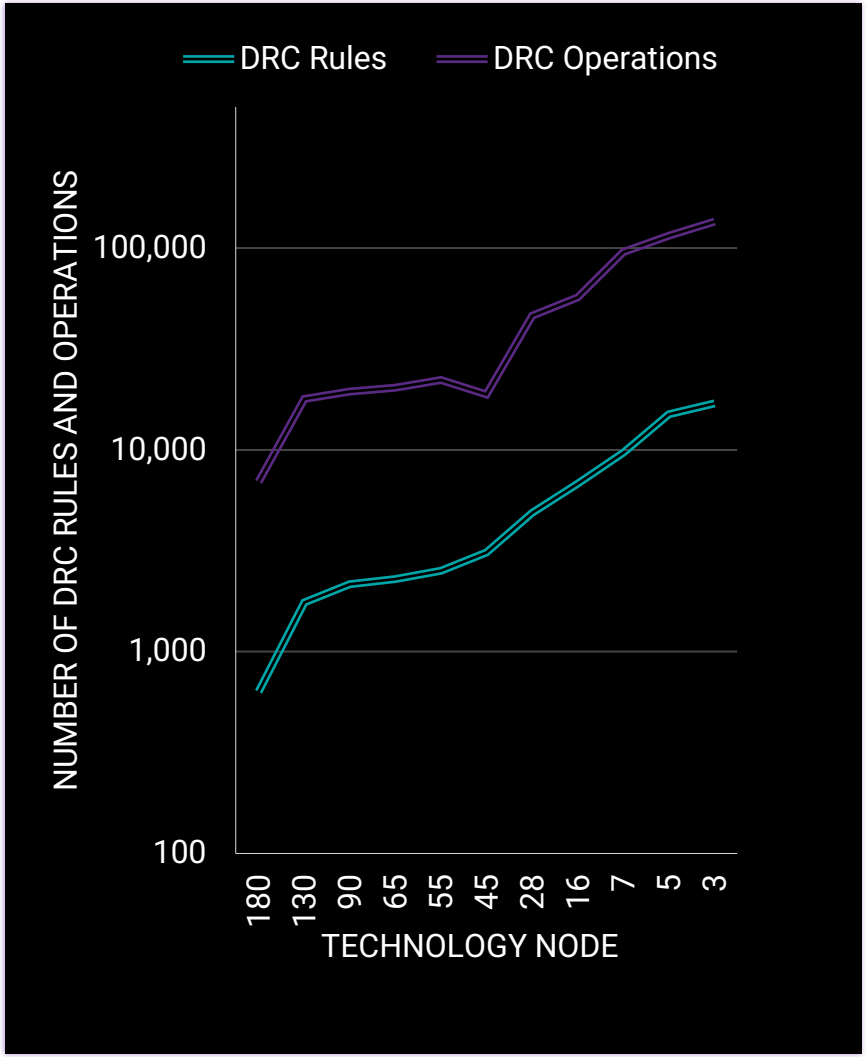
Sharing Bubble Tea??



Some Other Challenges

Challenges at Advanced Nodes

Increasing Rules Increases Complexity and Runtime



- **Multi-day runtimes due to increasing rules, complexity**
  - Large N3 SoC runtime > 24 hrs with 1000 cores
- **Debug is complex and time-consuming**
  - Require guidance to find root cause of DRC, LVS and Antenna issues
- **Extensive hardware compute requirements**

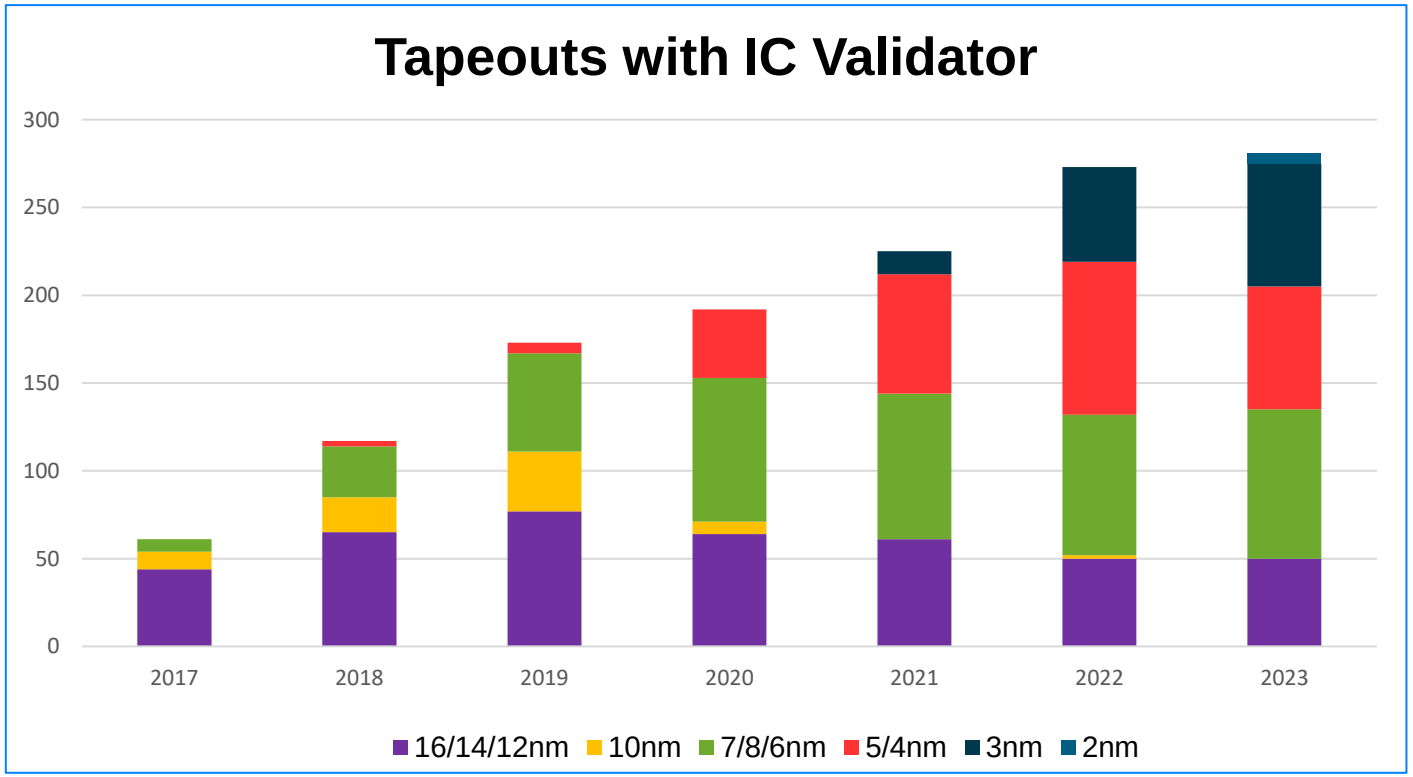
Why IC Validator

Scalability to 4000 Cores	**Overnight Runtimes**
40% Compute Savings	**Elastic CPU:** Optimized use of compute **Cloud:** PPU license model for peak demand
Explorer DRC & LVS	Isolate key design weaknesses within hours
2X Faster Debug Convergence	Find root cause of issues quickly to accelerate TAT
Fusion	Signoff DRC/Fill, Live DRC and PGA in FC and StarRC early-start flow

2X Faster with ½ Resources

IC Validator Signoff Momentum

Tapeouts Across Broad Range Of Designs / IPs, Foundries & Process Nodes



Key Customers

Source: TSMC OIP, DDTS, SNUG Presentations, Webinar

6+ 2nm
Testchip

100+ 3nm
Tapeouts/Testchips

80+ 5nm
Tapeouts/Testchips

60+ 12nm
Tapeouts/Testchips

Strong Foundry Collaboration

Golden Signoff Certified at TSMC, Samsung, IFS and GF

TSMC

Process	DRC	LVS	Fill
N2	✓	✓	✓
N3	✓	✓	✓
N4	✓	✓	✓
N5	✓	✓	✓
N6	✓	✓	✓
N10	✓	✓	✓
N12	✓	✓	✓
N16	✓	✓	✓
N20	✓	✓	✓
N22	✓	✓	✓
N28	✓	✓	✓
N45/N40	✓	✓	✓
N65/55	✓	✓	✓

Natively developed and Same day runset release for N5 & newer

Samsung Foundry

Process	DRC	LVS	Fill
14A	●	●	●
2nm	●	●	●
3nm	●	●	●
4nm	●	●	●
5nm	●	●	●
7nm	●	●	●
8nm	●	●	●
10nm	●	●	●
11nm	●	●	●
14nm	●	●	●
18nm	●	●	●
28nm	●	●	●

Multiple 3nm or newer projects signoff using IC Validator

Global Foundries

IC Validator Signoff Status for GF 12nm and 22nm PDKs

Runset	Status
DRC	Qualified
LVS	***Qualified*
FILL	Qualified
MAS	Qualified
DRC+	Qualified

** *LVS is not required for signoff.*

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Signoff certified for 12nm, 14nm and 22nm processes

100% Intel process projects signoff with IC Validator

TSMC Collaboration Beyond Enablement

N2 Technology partnership with TSMC

Early Technology Exploration	Learning from Early Designs	Stabilize and Co-optimize	General Deployment
Early specs discussion	Rule and performance fine-tune		Production certification
Features enablement	Synopsys IP & Design Service for TSMC Test chip		Customer support

N2 runsets: V0.1 released on 10/31/2022
Natively developed and Same day runset release for N5 & newer

Tool of choice for TSMC IP team

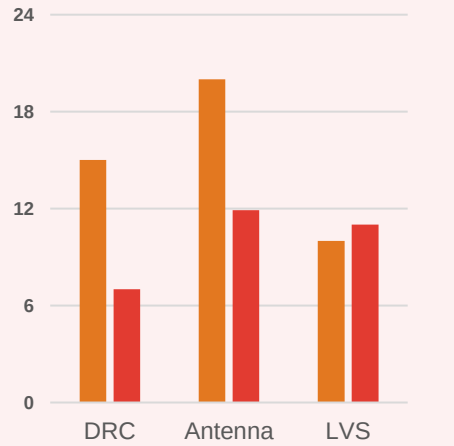
- **Primary** DRC / LVS Signoff at DTP
- Foundry tapeouts for pathfinding and IP silicon validation
- **TSMC tapeouts** – **6** at N2 and **24** at N3
- **100+** tapeouts at N3 across all customers

Key Signoff ICV Wins

Resource Optimization	Accelerate Design Closure	1.5X Faster LVS
Hardware Cost	Dirty Design Verification	Performance
Intel CPU 3nm, 5nm Elastic automatically optimizes allocation of machine resources	Cerebras AI 5nm, 7nm Explorer enables rapid iterations to accelerate dirty design verification	Astera Labs High Speed Connectivity IP 5nm, 7nm Scalability enables LVS to be 1.5X faster than competition
40% Compute Savings	4X Faster DRC/LVS	200 Core LVS Scalability

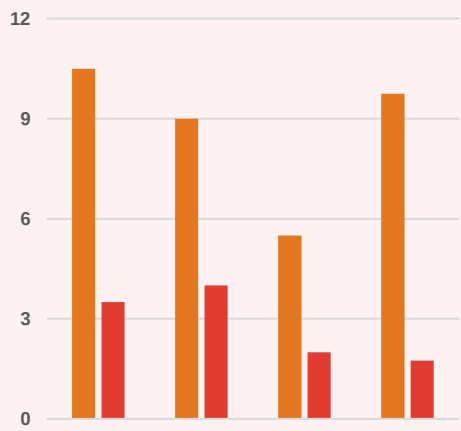
Performance Leadership at Advanced Nodes

Recent Benchmark data

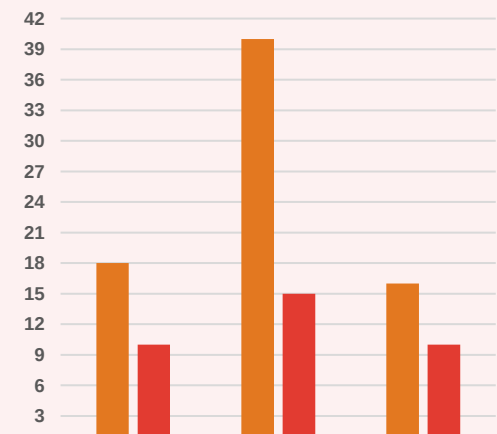


3nm
Testchip
448 cores

5nm
Networking
552 cores (DRC)
200 cores (LVS)



5nm
Graphics
144 cores

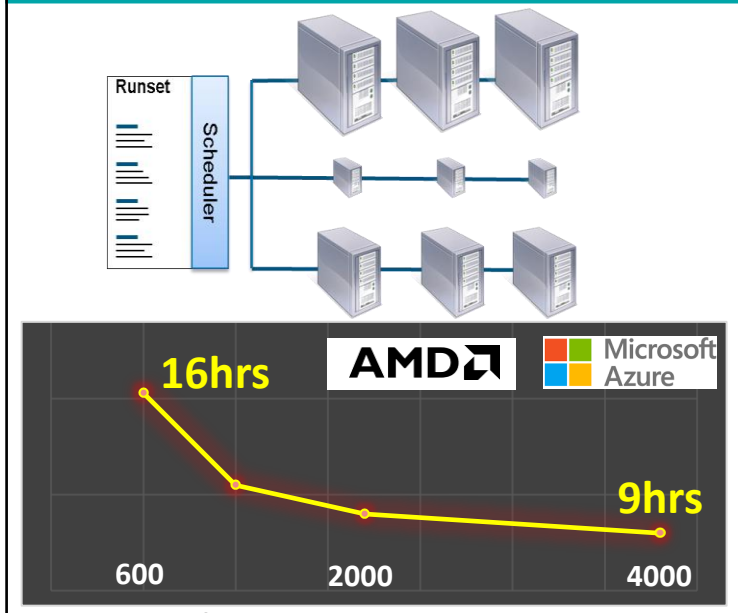


5nm
Mobile
360 cores (DRC BE/FE)
288 cores (ANT)

1.5X faster on DRC, PERC and ANT

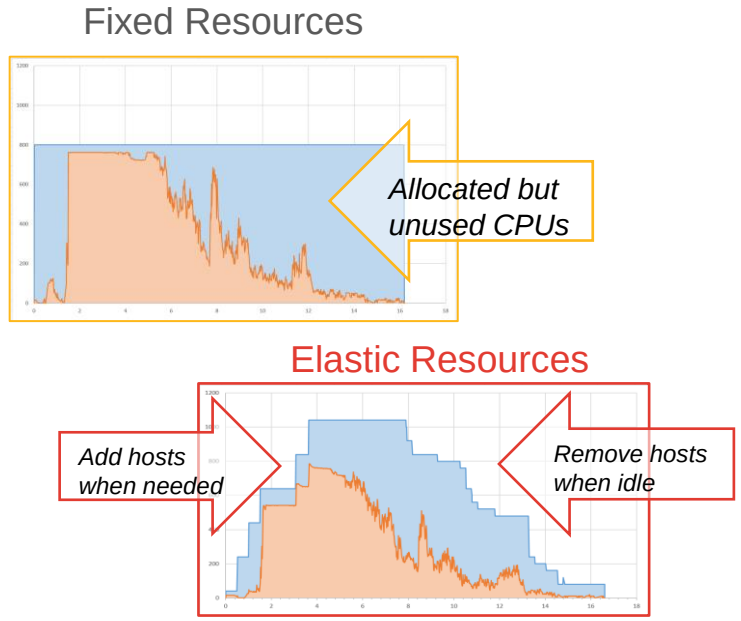
Scalability Technology Leadership

Scalability To 4000 Cores

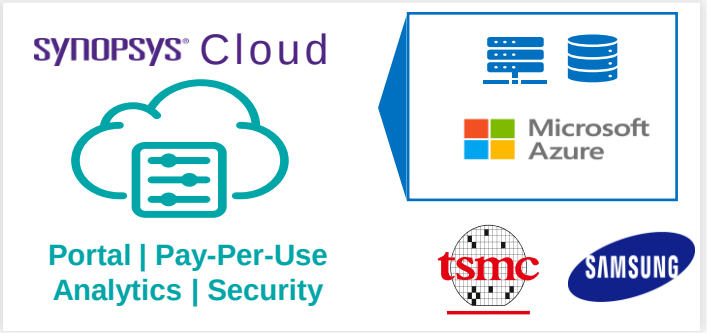


Source: Webinar, TSMC OIP

Elastic CPU



Cloud Optimized



TSMC Cloud Alliance
Samsung SAFE

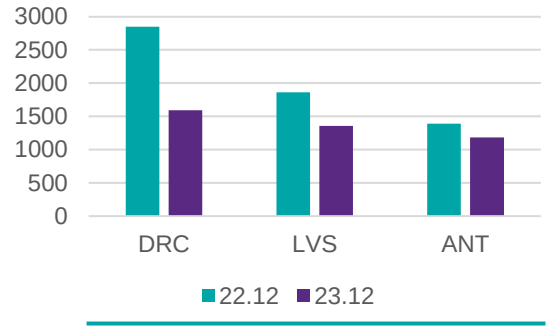
2X Speed-Up
- Massive Parallel Processing
- Memory aware Smart Scheduler

40% Compute Savings
- Eliminate queue time
- Lower peak license usage

40% TTR Improvement
- Immediate on-dema use for peak

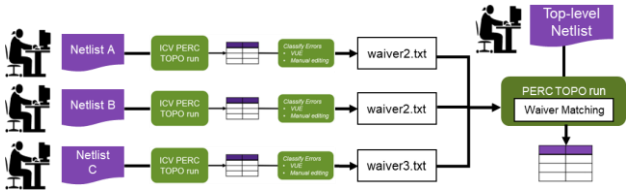
IC Validator 2023.12 Release Highlights

Performance



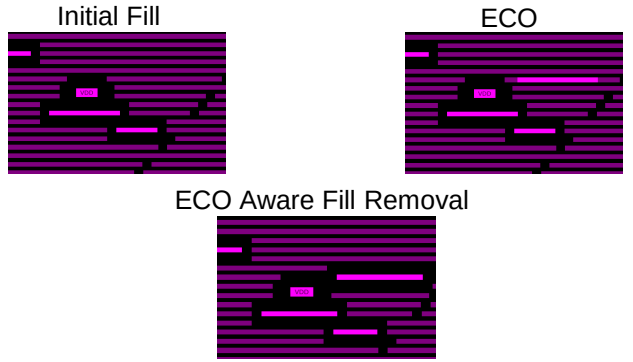
1.5X Faster

PERC ASCII Waiver Flow



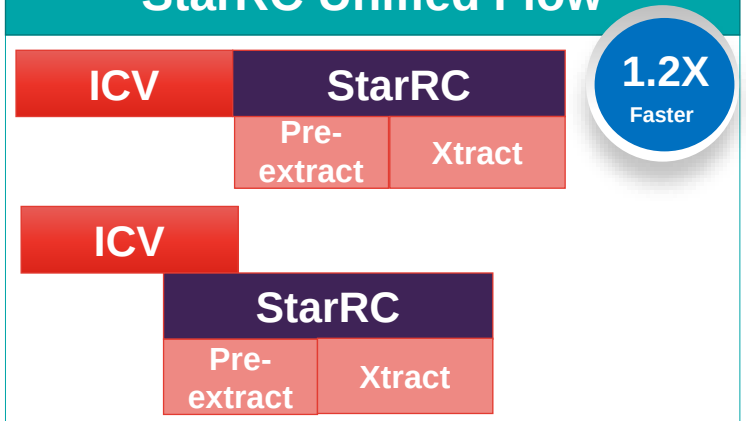
Accelerate waiver management across hierarchy

InDesign ECO-Aware Fill



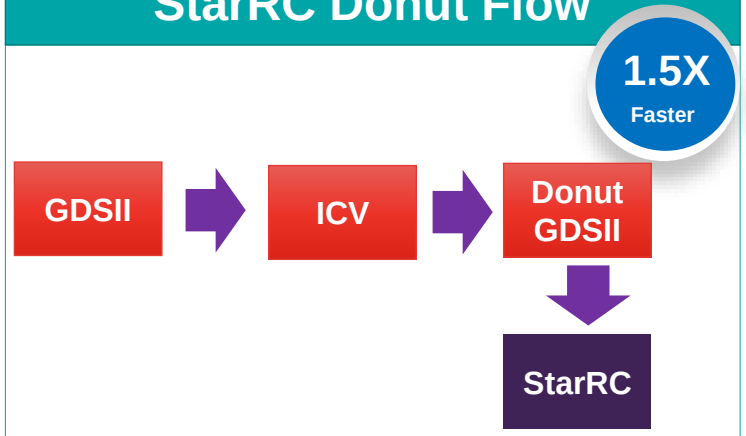
Faster ECO with minimum timing impact

StarRC Unified Flow



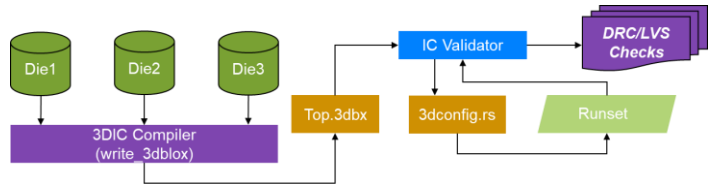
Run StarRC just as interface files are ready

StarRC Donut Flow



ICV creates donut on the fly

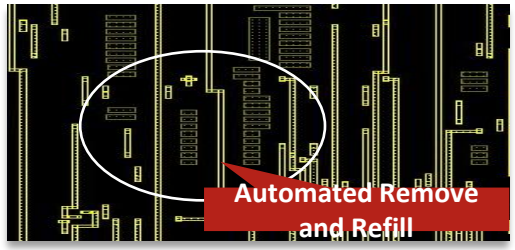
3Dblox Support



Automatically reads input from multiple dies and executes DRC/LVS

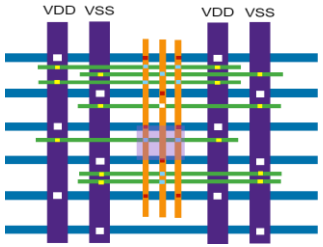
Faster Design Convergence with Fusion and StarRC

Timing Aware Signoff Fill

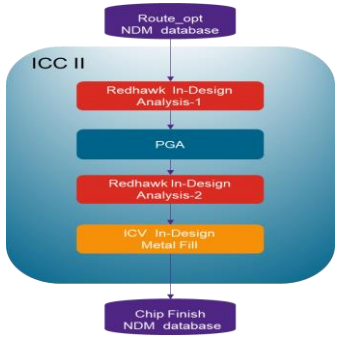


Balance timing and density requirements

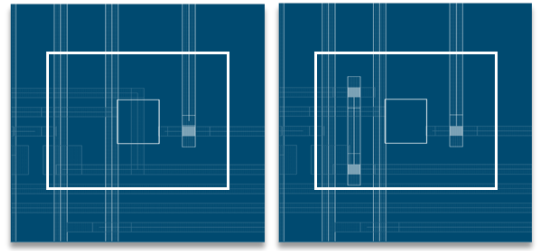
Power Grid Augmentation



Improve Voltage Drop

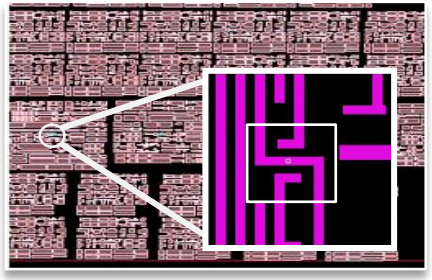


Automatic DRC Fixing (ADR)



Accelerate closure with nominal impact to timing

Ultra Fast ECO



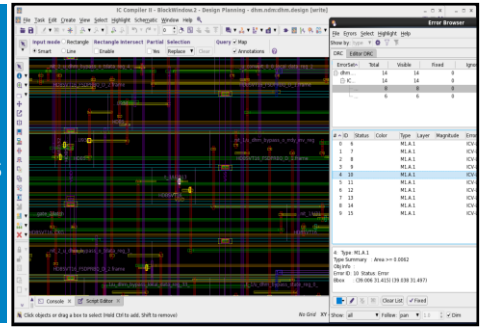
DRC and Fill ECO within minutes

Live DRC
DRC feedback within seconds

FC / IC Compiler II

shapes ⇩ ⇧ errors

IC Validator Live



StarRC Donut Flow

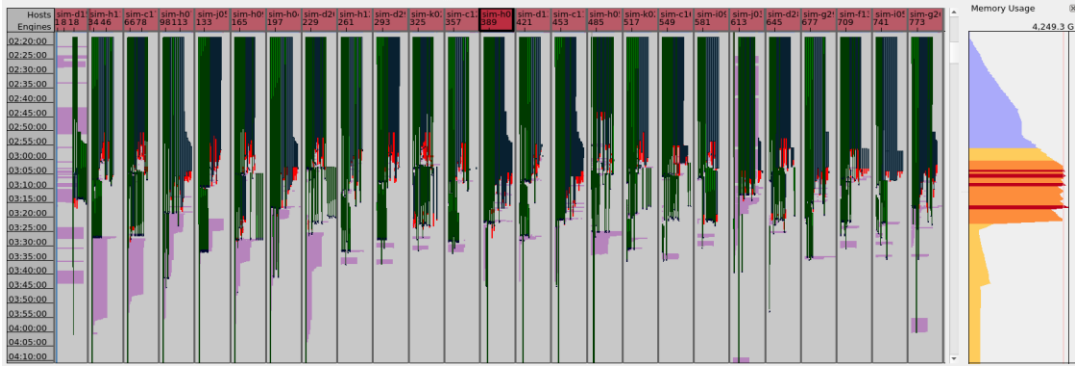
I/P GDSII → ICV → Donut GDSII → StarRC

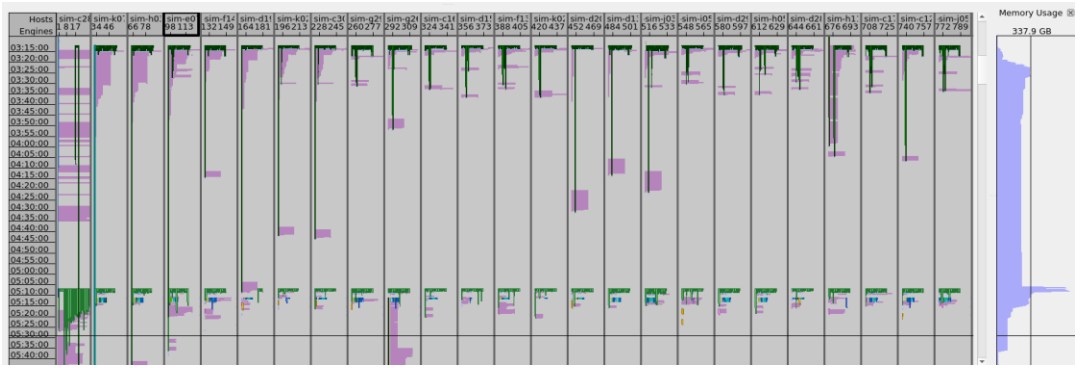
Use ICV to create donut on the fly and send to StarRC

1.5X Faster TAT

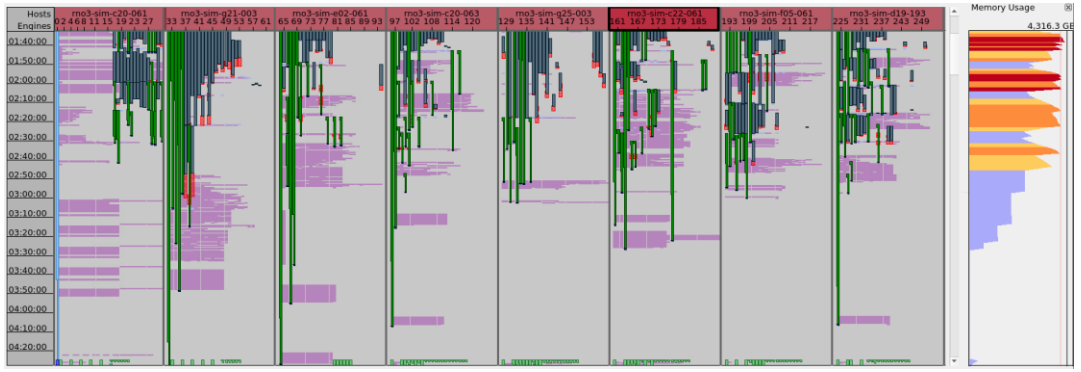
Customer Case Study: Peak Memory on N5 Design

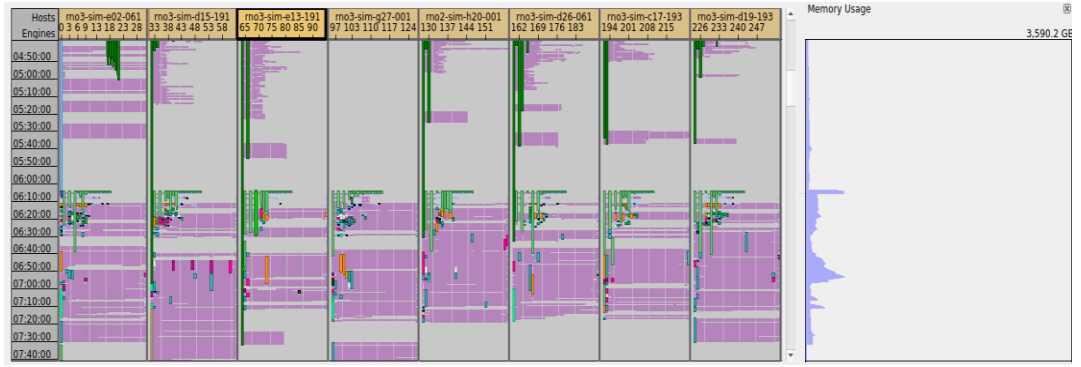
DRC Default Peak Memory: 4T
After Improvements: 337G





Antenna Default Peak Memory: 4T
After Improvements: 200G





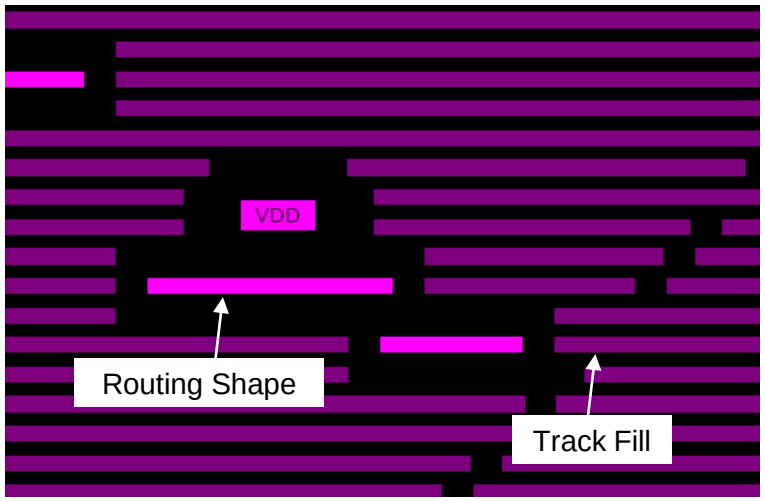
10X DRC and 20X Antenna Peak Memory Reduction

InDesign ECO-Aware Fill Removal For DRC Clean Results

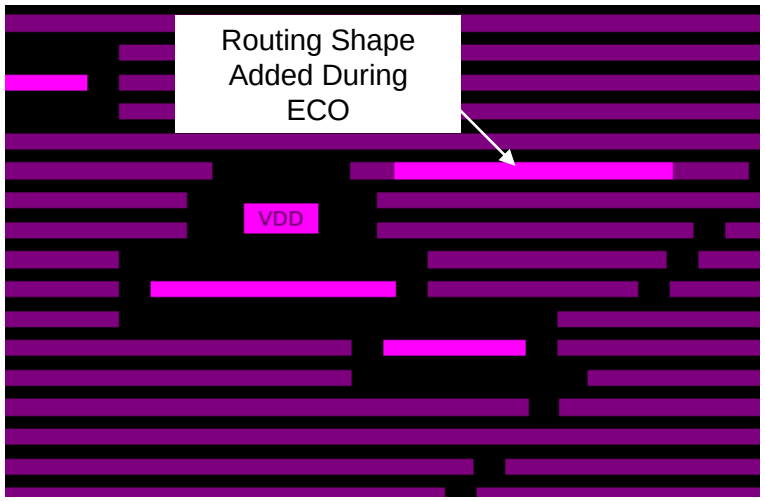
- Automatic track fill removal in ECO areas
  - Applicable to normal track fill and power grid augmentation (PGA) flows

- No need to generate DRC error markers with signoff_check_drc, check_routes, or check_pg_drc

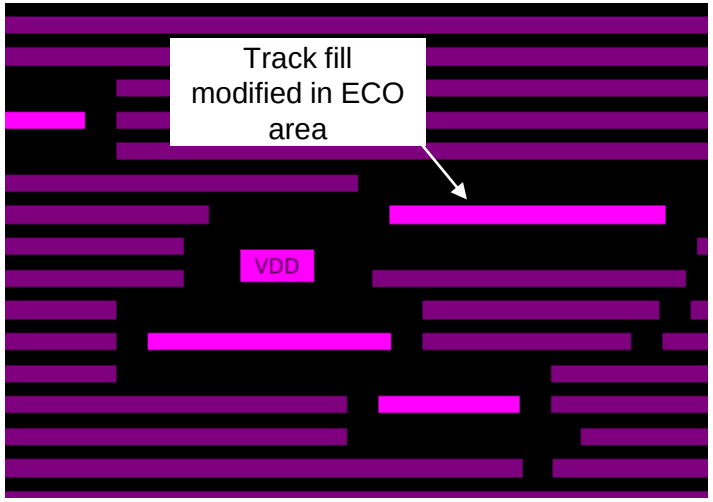
Design After Initial Track Fill Insertion



ECO Change

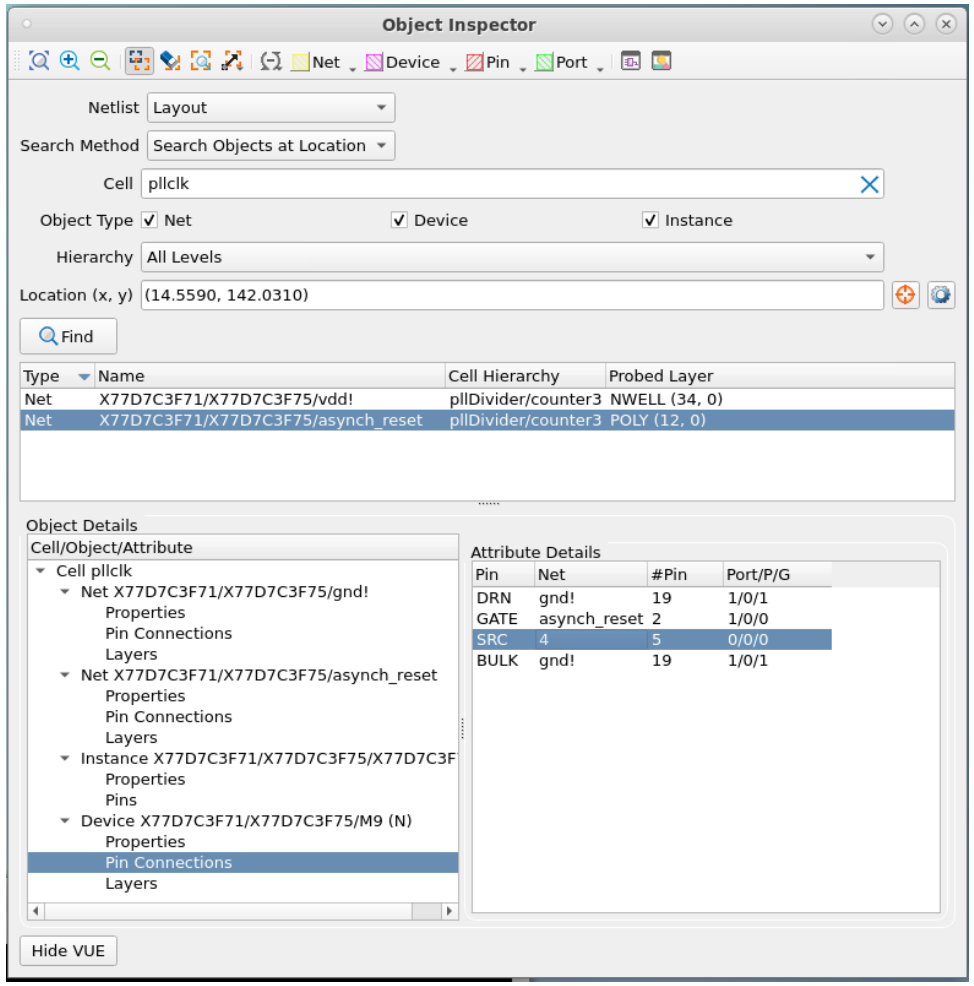


Design After ECO Aware Fill Removal



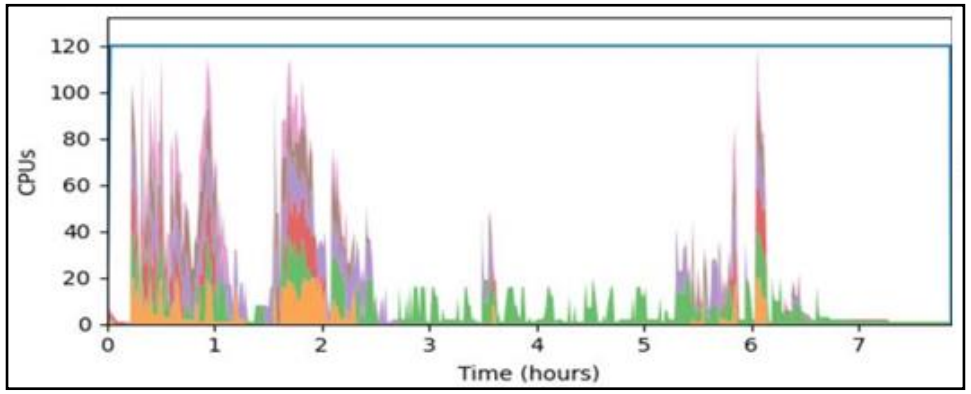
LVS VUE Object Inspector

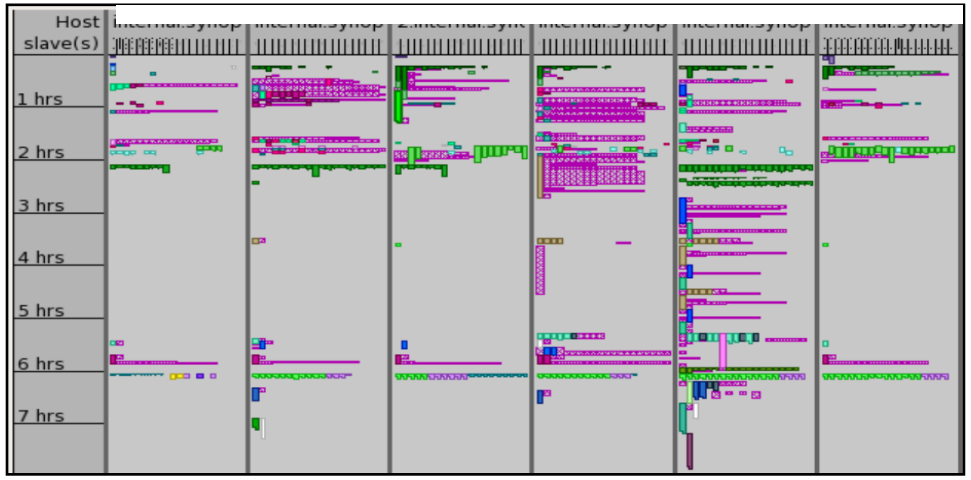
- Direct Access to extracted netlist data for debugging LVS ERC or complex LVS errors
- Probe the layout to get a list of netlist objects located at that point
- Find detailed information about items like pin connections, properties, or layers
- Flexible highlight controls
- Trace Paths through devices



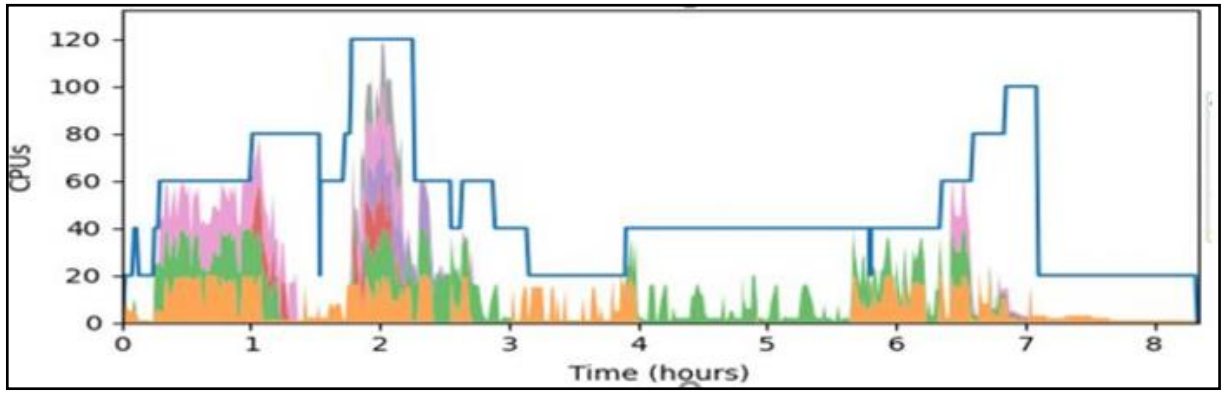
Customer Case Study: Elastic CPU for LVS on N5 Design

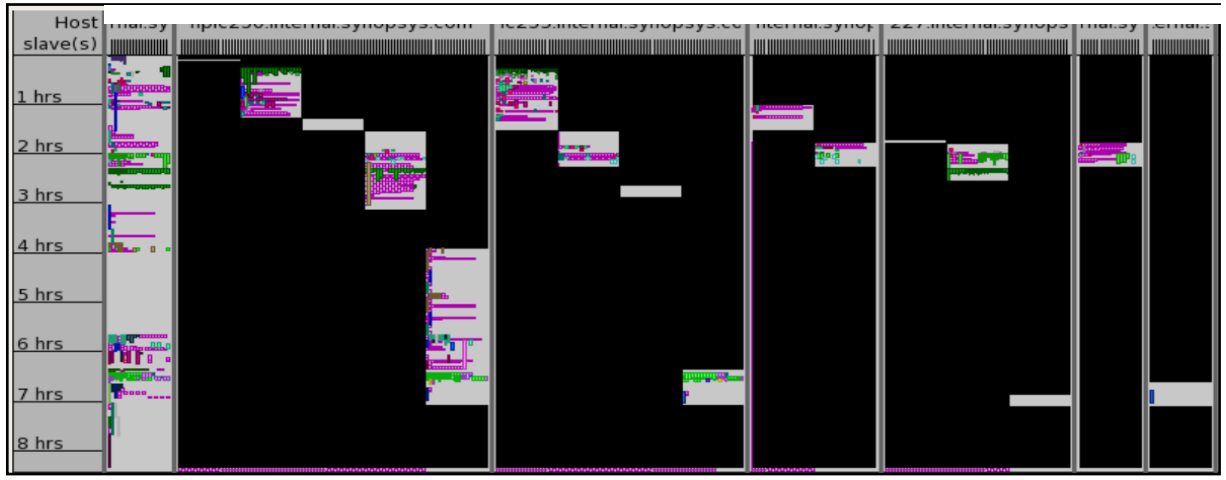
Normal run: Wall time 7:50Hours
Allocated CPU Hours: 943.7





Elastic run: Wall time 8:20Hours
Allocated CPU Hours: 410

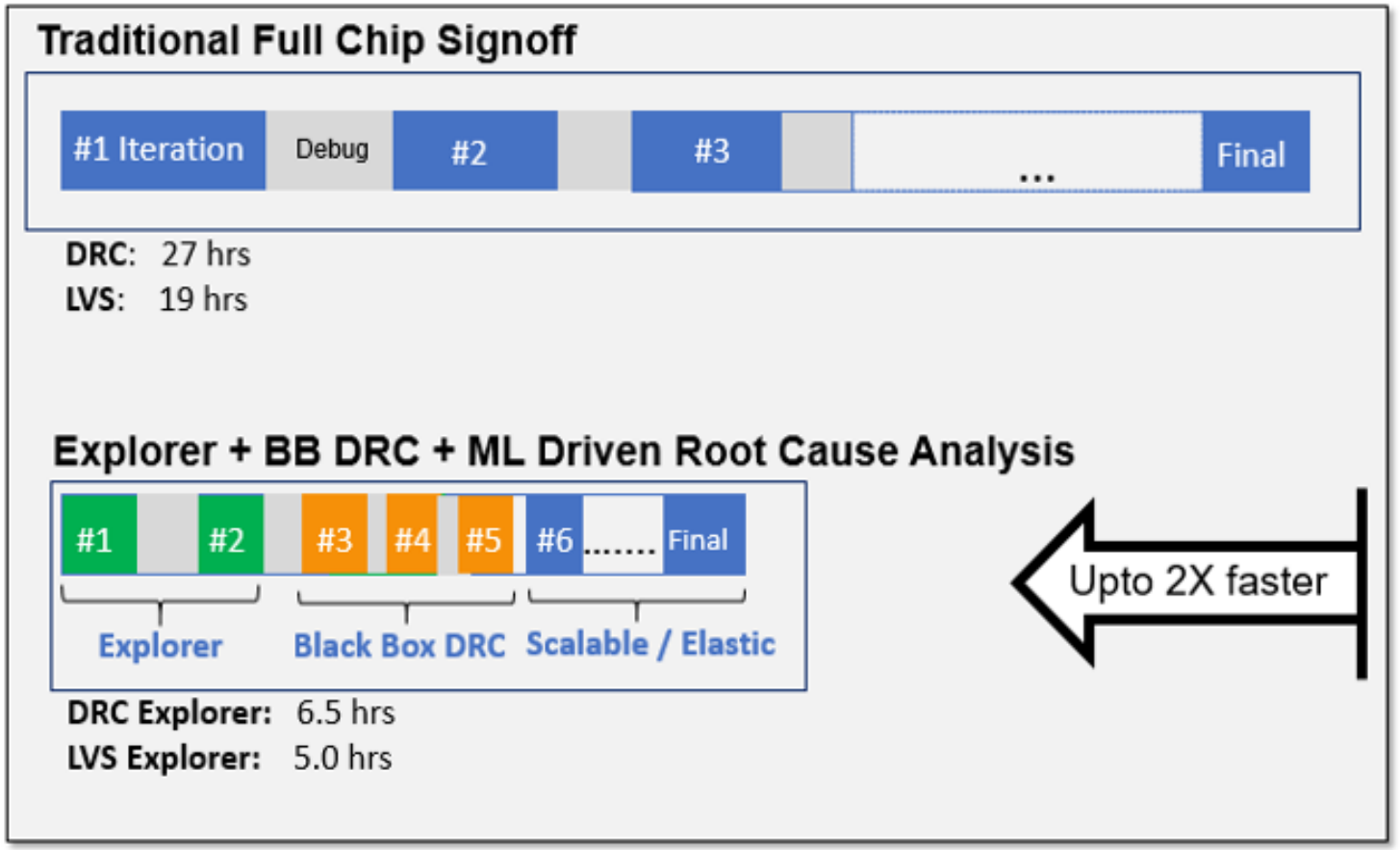




50% resource and license savings with 5% overhead in wall time

Customer Case Study: 7nm 650 mm² design

Rapid verify → fix turns during chip integration



LVS Explorer – 4X Faster

- Shorts/Opens at Top and all design hierarchy
- Connectivity mismatches

DRC Explorer – 4X Faster

- Fill/Block/Via overlaps
- Pin Location Mismatches

Black Box DRC – Decrease Noise

- Filter known macro errors

Root Cause Analysis

- Identify structural design issues

Scalable / Elastic

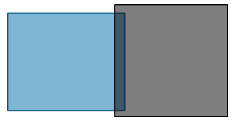
- Improve compute / license efficiency

Explorer DRC Identifies Key Design Issues Within Hours

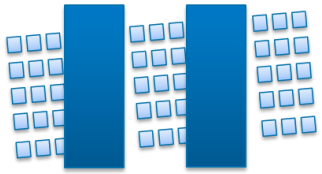
Innovative technology for dirty design verification

Issues During Integration

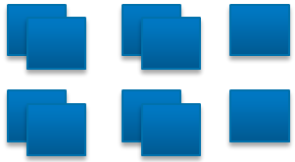
Block Overlap



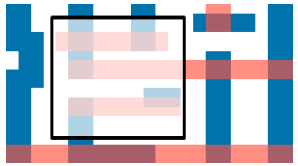
Fill Overlap



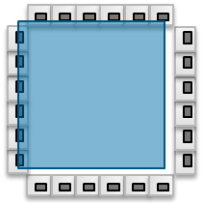
Via Overlap



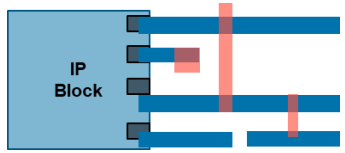
Missing Blockages



Pad Ring Overlap



Pin Location Mismatch



Long runtimes,
Billions of errors – tough to debug root cause

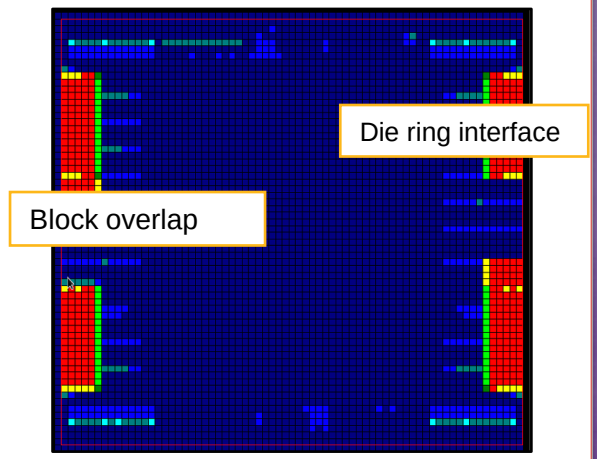
Explorer DRC

5X Faster **Runtime**

5X Fewer **CPUs**

Identify key issues within hours

DRC Heat Map

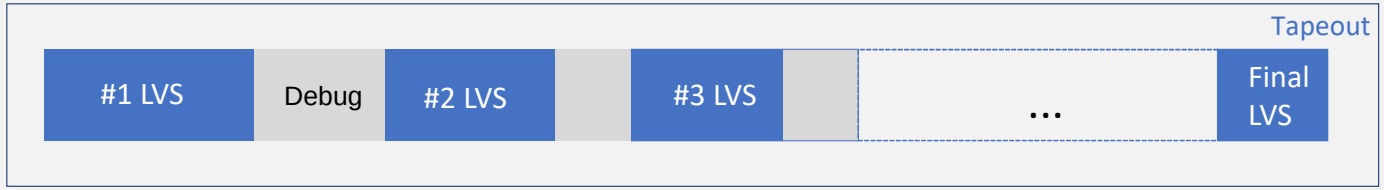


Immediately isolates clusters of errors

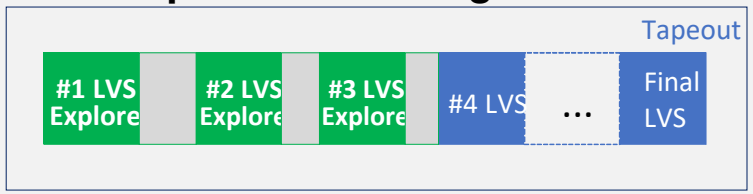
Explorer LVS: 2X Faster LVS Signoff Cycle

Able to do rapid verify → fix turns

Traditional Full Chip LVS Signoff



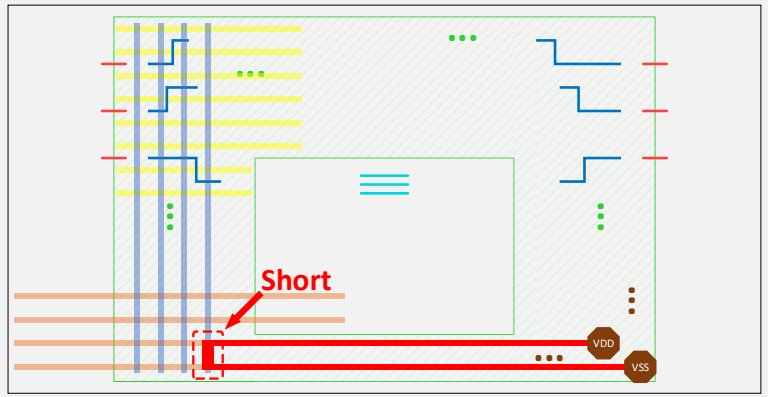
LVS Explorer + LVS Signoff



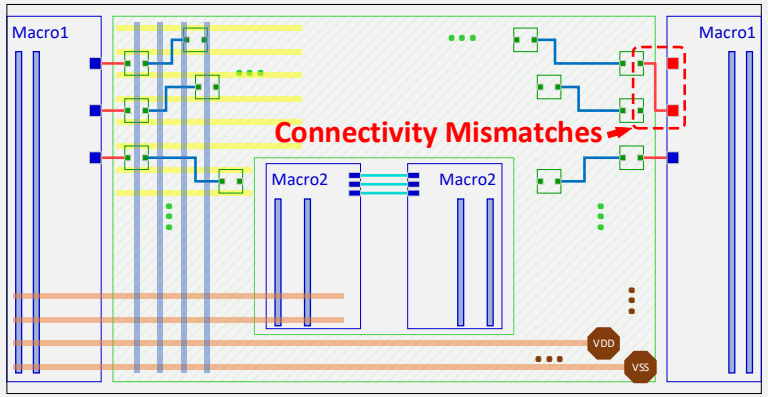
Upto 2X faster PV Cycle

Quickly find – Up to 10x Faster

- Shorts at Top
- Shorts/Opens in all design hierarchy
- Connectivity mismatches in all design hierarchy



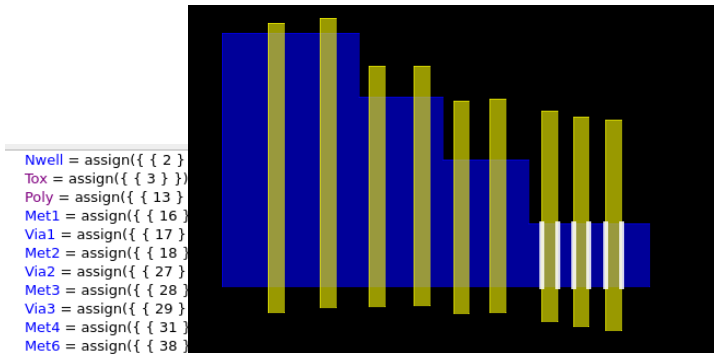
Metal only, text based short check



Connectivity mismatches check

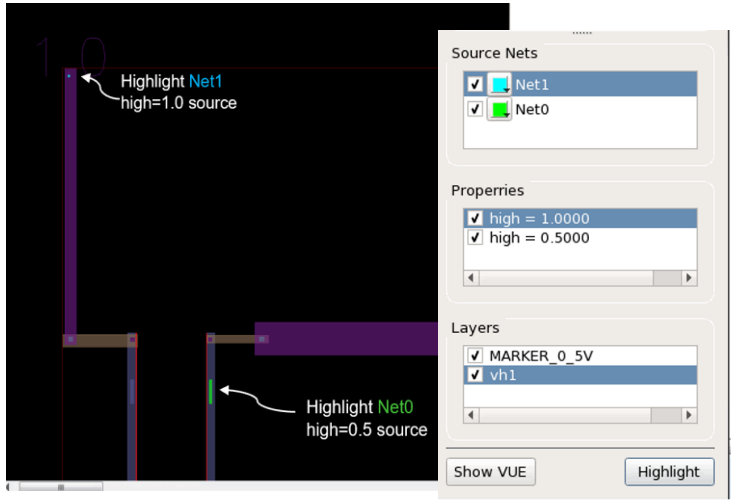
Unparalleled Innovations to Accelerate Debug

Layer Debugger



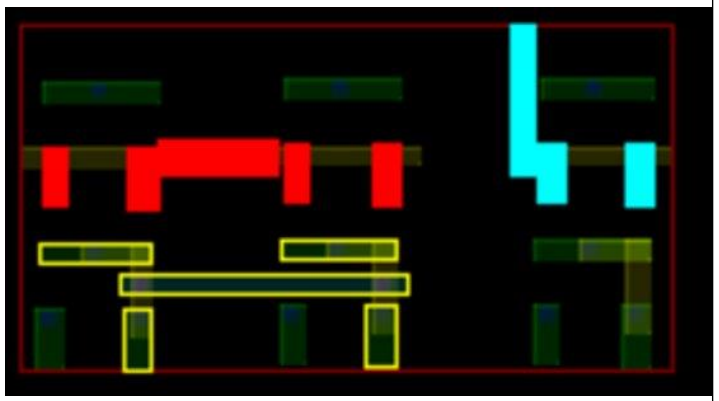
Highlight intermediate layers out-of-the box to debug complex rules

Delta-Voltage



Highlight entire net with voltage sources for faster debug

Antenna Debug

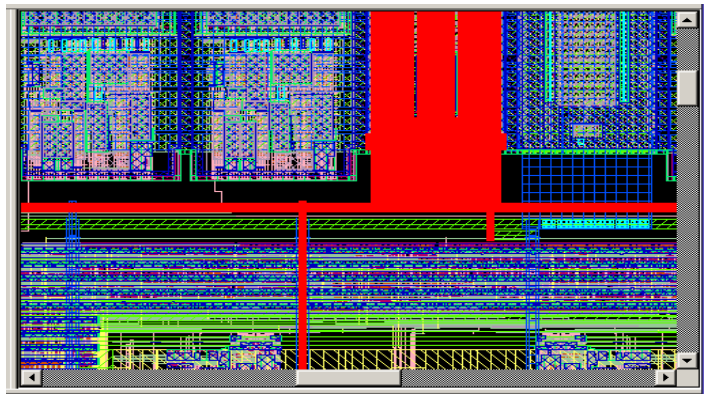


Highlight multiple nets for easier debug

2X Faster PV Convergence

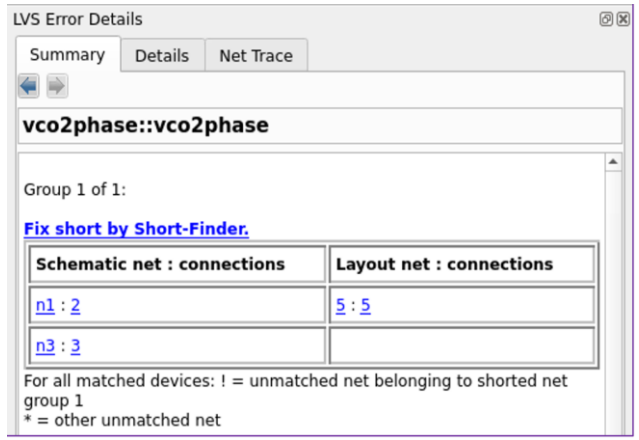
Unparalleled Innovations to Accelerate Debug

LVS Short Finder
Interactive Short Analysis



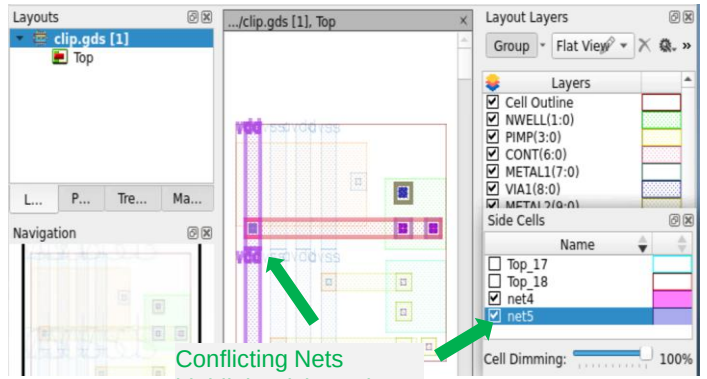
Multiple text-shorts debug without rerunning LVS

LVS-Aware Short Finder



Fix logical shorts using interactive short finder

LVS Soft Check



Conflicting Nets highlighted through Net Trace for Debugging

Show conflicting metal nets attached to well islands

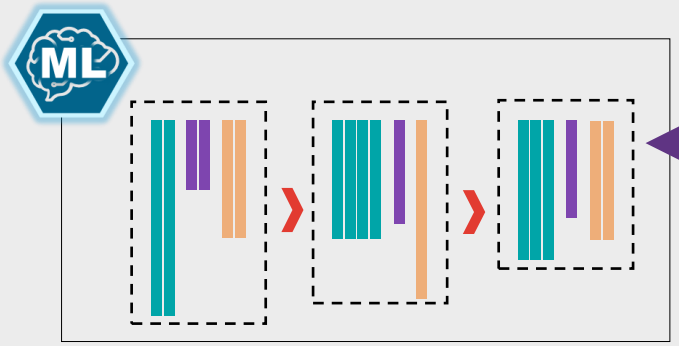
2X Faster PV Convergence

Machine Learning Solution

ML-Enhanced Physical Verification

Accelerate Verification

Faster performance

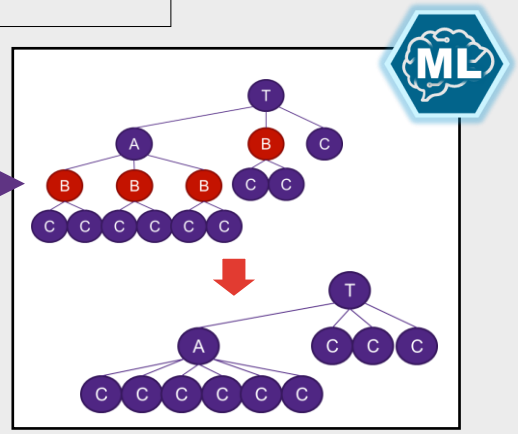


Scheduler

Fast runtime

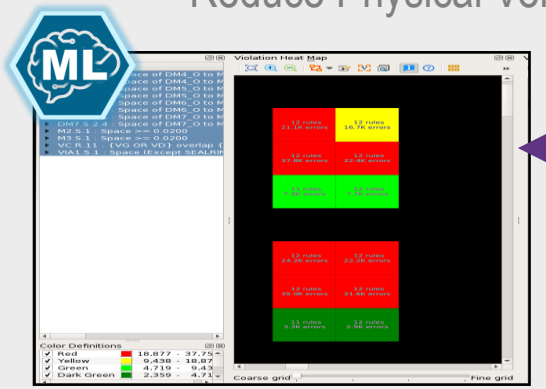
Hierarchy Optimization

Efficient DRC, LVS data processing



Leap in Productivity

Reduce Physical Verification TAT

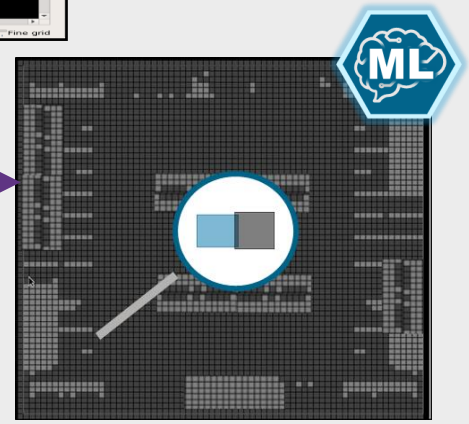


Heatmap Clusters

Fast convergence

Automatic Root-cause identification

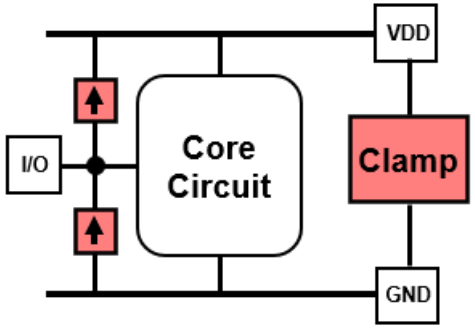
Fast convergence



End-to-End ESD Solution

Technologies from Schematic to Layout

ICV PERC - TOPO



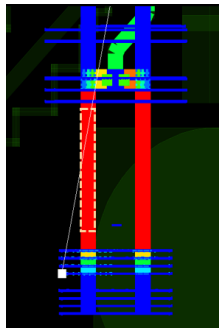
Fully programmable netlist analysis

Recognize and report full ESD network

Foundry Certified

Python programming language

ICV PERC – CD/P2P



Unmatched full chip performance, 94B Tx

Star-RC golden Extraction

Foundry Certified

Silicon Proven on SNPS IP

PrimeESD - HBM

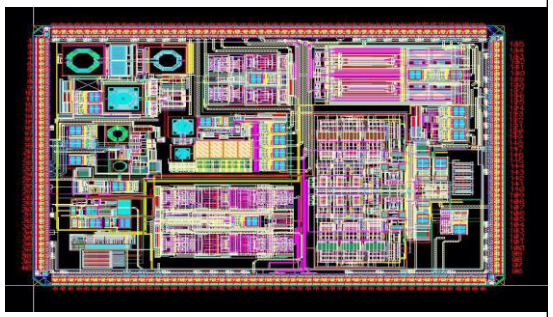
Full chip HBM Analysis

Finds core device and interconnect failures

Highlights cause of failures

Identifies unused or lightly used ESD Devices

PrimeESD - CDM



Full chip CDM Analysis

Supports ESD Device snapback

Charge distribution algorithm supports all design styles

Supports inductance and capacitance

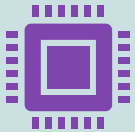
Enabling Designers to Achieve ESD Proof Designs

Customer Successes

CDM Issue -Transient Effects	CDM Issue - Package Effects	HBM Issue - Device Stress Checks
Inductance Issue	Charge Distribution Issue	Core Device Failures
European Customer RF Design 16nm PrimeESD CDM uncovered failure due to Inductance missed by other tools	Major IDM Touch Screen Design 28nm PrimeESD CDM uncovered failure due to charge distribution caused by package	US Customer AMS Design 40nm PrimeESD HBM uncovered failure In core devices missed by other tools
Improved Design Reliability	Improved System Reliability	Improved Design Reliability

Summary

TSMC Golden Certified, Natively Developed Runsets,100+ N3 Tapeouts



Scalability to 4000 cores

40% compute savings

2X faster debug convergence

How to get through in Ho Chi Minh Traffic

Smart Traffic là việc sử dụng công nghệ và thông tin để cải thiện hiệu suất và giải quyết các vấn đề về giao thông. Sử dụng các công nghệ tiên tiến như cảm biến, hệ thống thông tin liên lạc, trí tuệ nhân tạo và phân tích dữ liệu để thu thập, xử lý và chia sẻ thông tin về giao thông.

Extreme heat during Ho Chi Minh Summer

Tận hưởng mùa hè thật phong cách


THANK YOU
Our Technology, Your Innovation™