ICV Signoff with Advanced Node Designs

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Agenda

- Introduction
- Methodology Innovations
- Analyze and Debug Density Violation
- Voltage Dependent DRC Flow
- Next Step
- Conclusion

Introduction

Introduction

Who we are & What we do

- DMM.make is a new team of the DMM Group that focused on semiconductor Research & Development and IC Design.

- We cooperate with companies which are doing advanced nodes to develop our products.

Introduction

Challenges

- The benefits for Power, Performance and Area of advanced process node is crucial to the success of our product.
- However, advanced nodes possess many challenges for IC design due to the complexity in making smaller features and more advanced transistor structures.
- Challenges for layout includes Design Rule complexity, Multiple Patterning, Design for Manufacturing (DFM), Signal Integrity and Power Delivery.
- Hence, an efficient and productive method for Physical Verification (PV) is required.

Methodology Innovations

Fully Utilized DRC Explorer and Debug Features

IC Design Phase

Methodology Innovations

- 4 new Methodology Innovations are being proposed in the subsequent slides which would focus on stage 2 & stage 3.

Synopsys Reference Methodology (RM) Flow

Early Mode Runtime Advantage

Three Design State Options in RM Flow

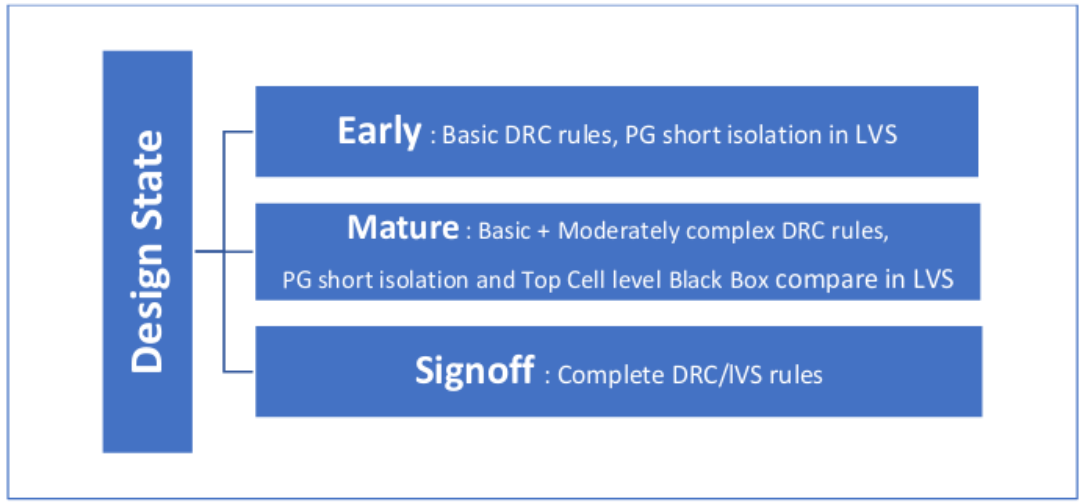


Fig. 1. Three design state

Early: -explorer standalone
Mature: -explorer tiers:3

Runtime & Memory Usage

	Early Mode	Signoff Mode
Runtime	1hr 01min	16hr 24min
Overall Memory	3.68 GB	11.14 GB
Peak Memory	7.37 GB	92.75 GB

Design Used

Process	**N4P**
Metal layers	**11**
Area	**50mm²**
Hierarchy levels	**16**

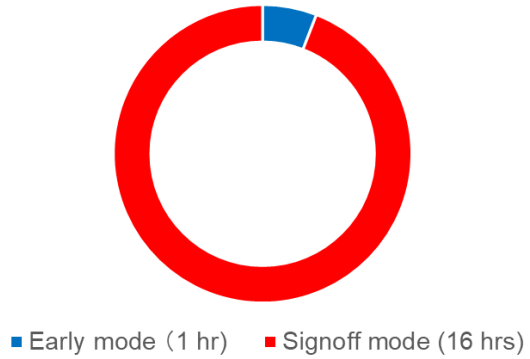


Fig. 2. Comparison of Early mode & Signoff mode

*Early Mode gives a significant runtime advantage with the trade off of running basic DRC rules only.

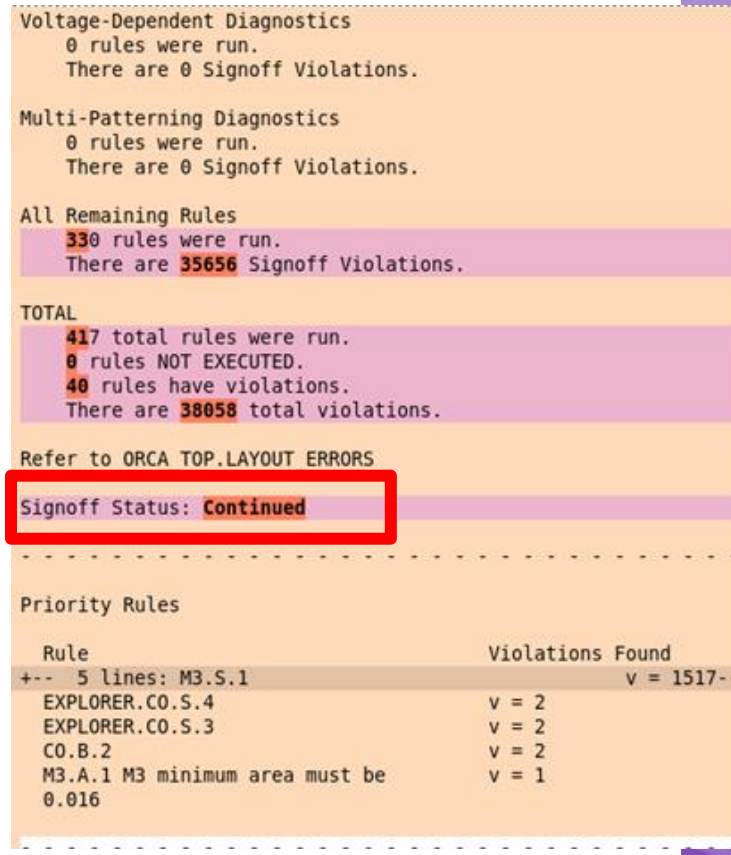
ICV Explorer Mode

ICV Native Option

- RM Flow utilized explorer mode:

Early: -explorer standalone
Mature: -explorer tiers:3

- Explorer has another option: -explorer **auto**
  (not part of RM flow)
- Explorer **auto** mode: ICV internal engine will decide to run Explorer mode or Signoff mode.
- If ICV decided to use Signoff mode, “Signoff Status: Continued” is printed in the log file.
- However, it is unclear how ICV internal engine decide the design is clean enough for Signoff mode.
- A methodology which is able to set our own criteria is required.



Methodology Innovation 1

Stage 2
Floorplanning
, early P&R

Automation for Productivity & Efficiency

- When the design is dirty, run Early followed by Signoff in series or parallel with an automated script.
- Analyze and debug Early Mode's result as the runtime is short.
- Analyze the rest of the violations after Signoff Mode has completed.
- It is recommended to run Signoff mode at least once the early stage to get the full picture with all the DRC rules being run.

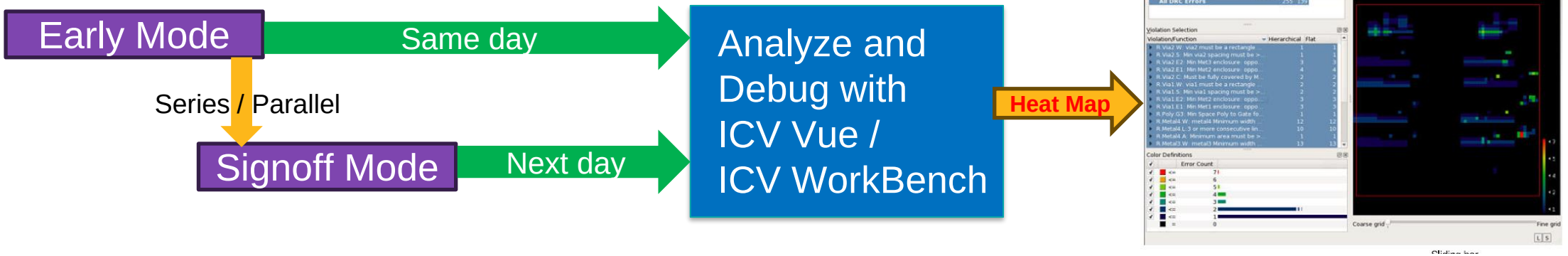
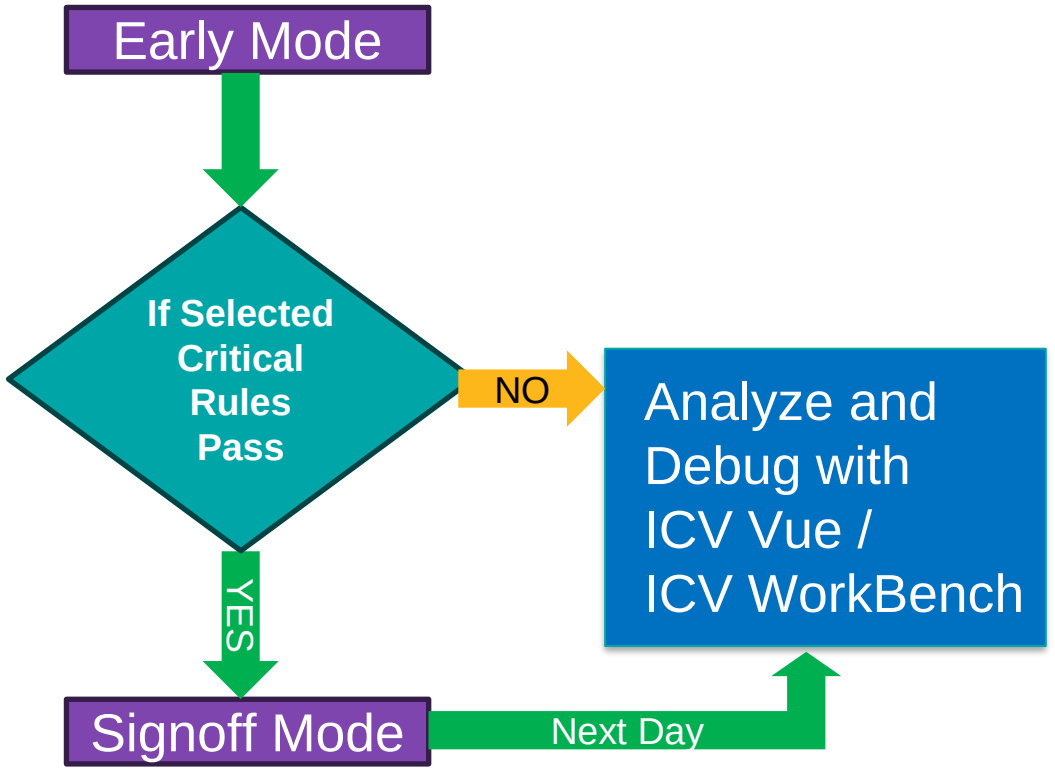


Fig. 3. Heatmap debugging

Methodology Innovation 2

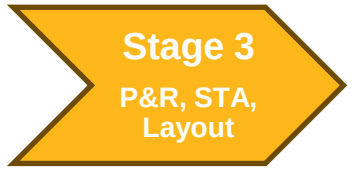
Automation for Productivity & Efficiency

- The automated script would ensure some critical rules are passing before moving forward.
- In some cases, it is not meaningful to run Signoff if the critical rules are failing.
- It is recommended to analyze and debug before taking further action.

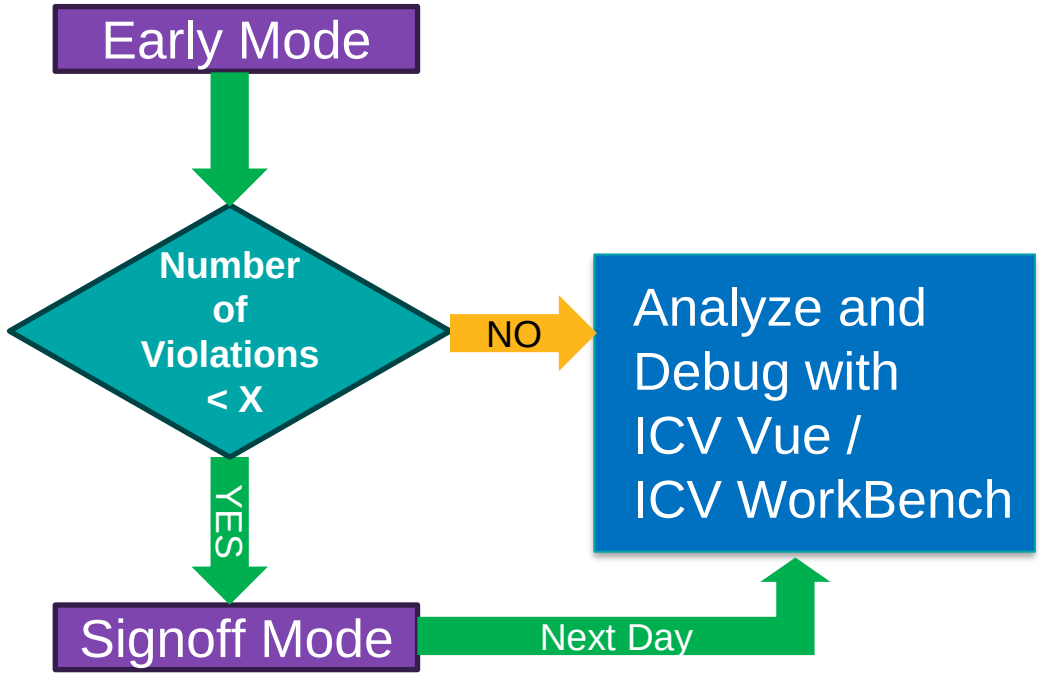


Methodology Innovation 3

Automation for Productivity & Efficiency

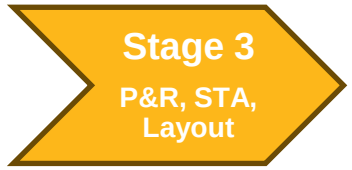


- When the layout is too dirty, it may not be meaningful to run Signoff mode.
- An automated script will run Early mode and checks if the violations is below the violations threshold (X) set by user before running Signoff.
- If the total violations is above the threshold (X), the flow will not continue.

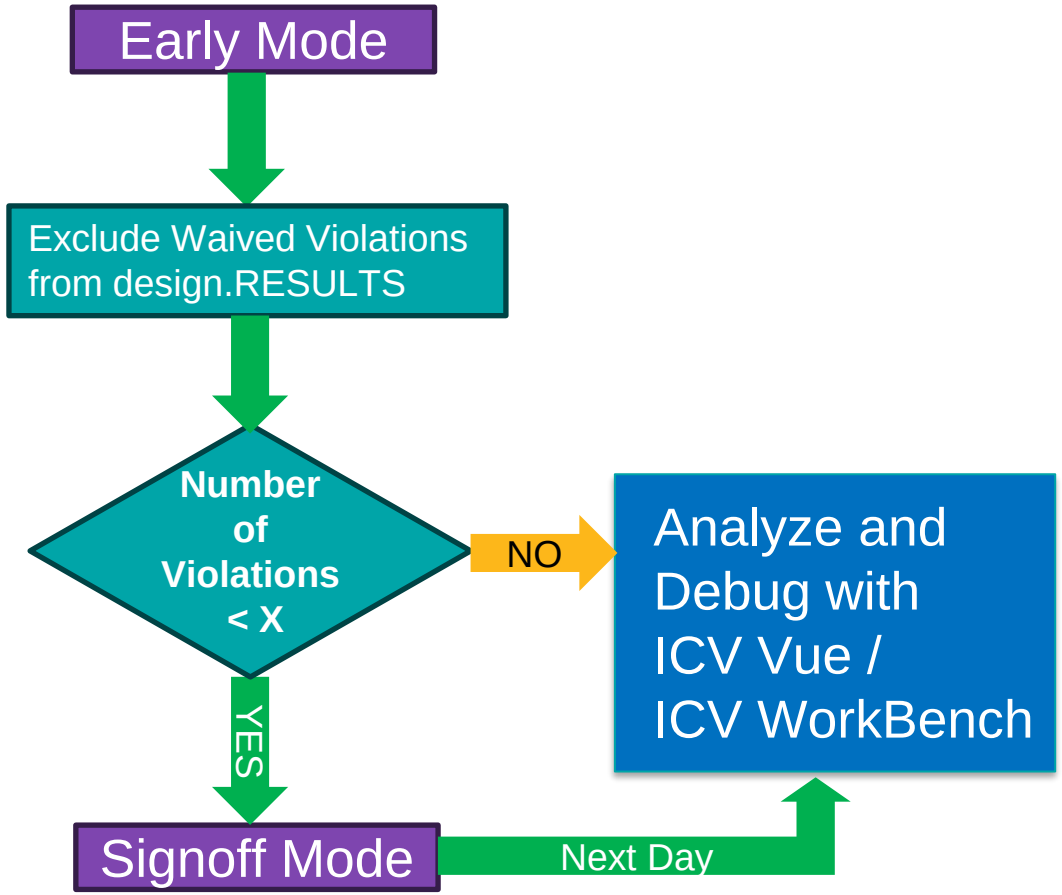


Methodology Innovation 4

Automation for Productivity & Efficiency



- In the middle phase of the design state where analysis has been done on previous release, we know that some of violations could be waived or will be resolved in future release.
- Hence, the script will exclude these violations from the total violations and check if it exceeds the threshold (X).
- If the violations is lesser than X, it will continue to run Signoff mode.



Reference Flow Modification

Fully Utilized ICV Vue Features -> Heat Map

- Heat Map is a useful feature in ICV Vue to visualize error distributions.
- As ICV Vue can be used in ICV WorkBench, ICC2, FC and Custom Compiler, it is useful feature to analyze, debug and make layout edits.
- Heat Map is generated in Early mode (DRC explorer) by default.
- However, it is **not** generated in Signoff mode.
- Add –hm options to generate the Heat Map during ICV DRC run.

In rm_icv_scripts/icv_run_drc.tcl:

```
set TEV(custom_drc_options) "-hm "
```

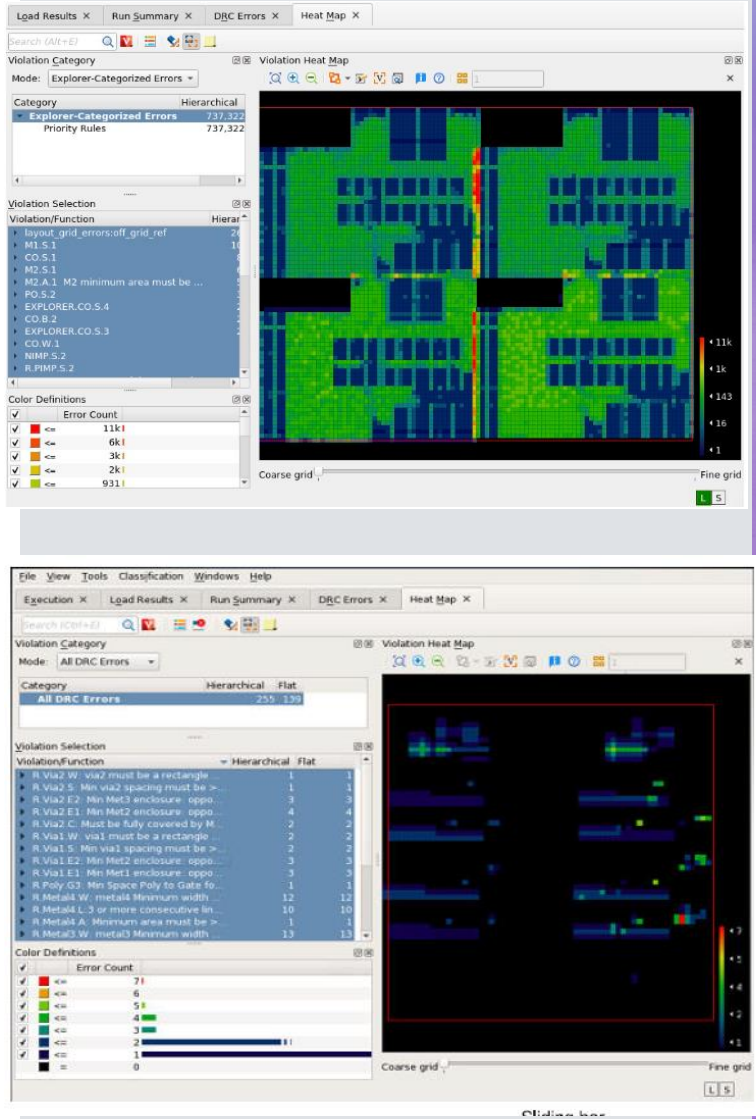


Fig. 4. Heat Map in ICVWB

Analyze and Debug Density Violation

Manipulate runset for analysis

Density Violation Challenge

Density Violations at Via Contact Layer

- The mentioned design faced a Maximum Density violation at Via Contact Layer.
  - Maximum Density = MD%
  - Actual Density = AD%
  - Design rule states that **AD% <= MD%**
- As majority of the metals in Via Contact Layer is inside standard cells, the only solution is to control the usage of standard cells.
- To minimize the design impact, changing the decap and filler cells is preferred.
- Hence, extract the density contribution by decap and filler cells is required for further analysis.

Extracting Density Contribution

How to extract density contribution?

- In order to extract density contribution quickly without modifying the layout, modification of runset is necessary.

Remove All Filler Cells	Remove All Decap Cells

`hierarchy_options(`
`  delete = "FILL*"`
`);`
	`hierarchy_options(`
	`  delete = "DCAP*"`
	`);`

  - It can be done to any cells with the regular expression or just deleting the specific cells.

- Run ICV with single rule option for the specific density rule instead of running all the DRC rules to get the results within minutes.
  - `-svn` *`violation_name`*
  - OR `-svc` *`violation_comment`*

Extracting Density Contribution

Density Violations at Via Contact Layer

- From the results extracted, calculate the density contribution by Decap cells and Filler cells respectively.

Criteria	Total Density
No exclusion	Actual Density %
Decap Cells Only	Actual Density % - Remove All Decap Cells %
Filler Cells Only	Actual Density % - Remove All Filler Cells %

- This information is crucial for design engineer to conclude if reducing the usage of decap cells or swapping decap to filler can improve or meet the maximum density requirement.

Voltage Dependent DRC Flow

Manipulate runset for analysis

Voltage Dependent DRC flow

Read voltage text

- Voltage dependent DRC requires designer to annotate the voltage text.
- Generate a Voltage text file from a script with the following Edtext format.
  - { “CELL”, “NET”, CAD_LAYER, DATA_TYPE, COORDINATE_X, COORDINATE_Y },

- Read in the Voltage text file as an external **edtext.**
- Verify the text provided is used by **report_text**. Results will be shown in design.text_report file (EDTEXT).

Runset:

```
text_options(
    edtext = {
      #include "/directory/icv.voltage.txt"
    },

    report_text = {cells = ALL, functions = "*"}
);
```

Example icv.voltage.txt:

```
{ “DESIGN1”, “VDD”, 202, 74, 6987.1, 4123.66 },
{ “DESIGN1”, “0.35”, 74, 6, 6987.1, 4123.66 },
{ “DESIGN1”, “0.28”, 74, 6, 6987.1, 4123.66 },

{ “DESIGN1”, “VSS”, 202, 74, 4345.1, 3789.7 },
{ “DESIGN1”, “0”, 74, 6, 4345.1, 3789.7 },
{ “DESIGN1”, “0”, 74, 6, 4345.1, 3789.7 },

{ “DESIGN1”, “PORT_A”, 202, 74, 2567.236, 5123.206 },
{ “DESIGN1”, “0”, 74, 6, 2567.236, 5123.206 },
{ “DESIGN1”, “0”, 74, 6, 2567.236, 5123.206 }

……
```

Next Step

Future Development

Next Step

Future Development

- Multi patterning in advanced nodes contribute challenges to engineers as there are many more DRC rules to meet. Some of these rules are very difficult to fix as fixing one rule may fail another rule in the same region.
- Hence, a shift left approach is necessary to tackle these challenges by doing physical verification and layout modifications earlier in the design phase.

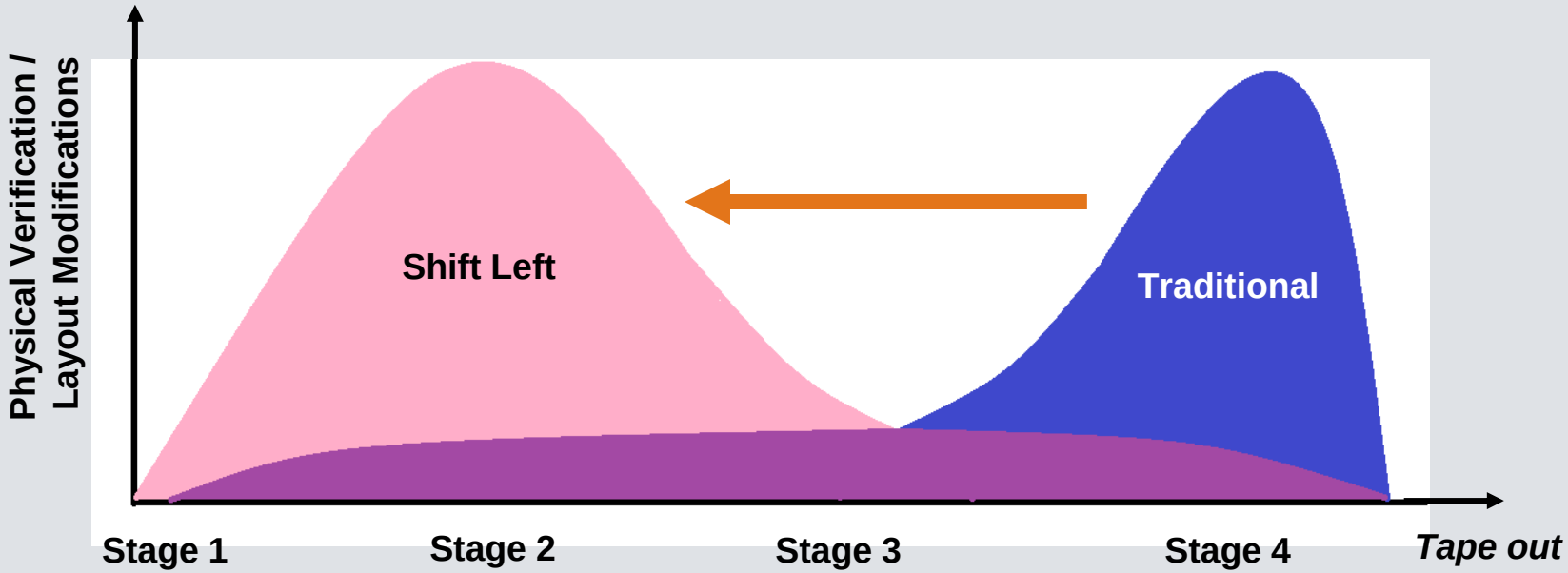


Fig. 6. Shift left diagram

Next Step

Future Development

- As DRC runtime is long on advanced nodes and large designs, verification after some layout edits is taking a long time.
- Incorporate ICV Live DRC into our methodology will improve the productivity and efficiency. As engineers can quickly verify it with the fixes or fix proposals pass DRC in a specific area.

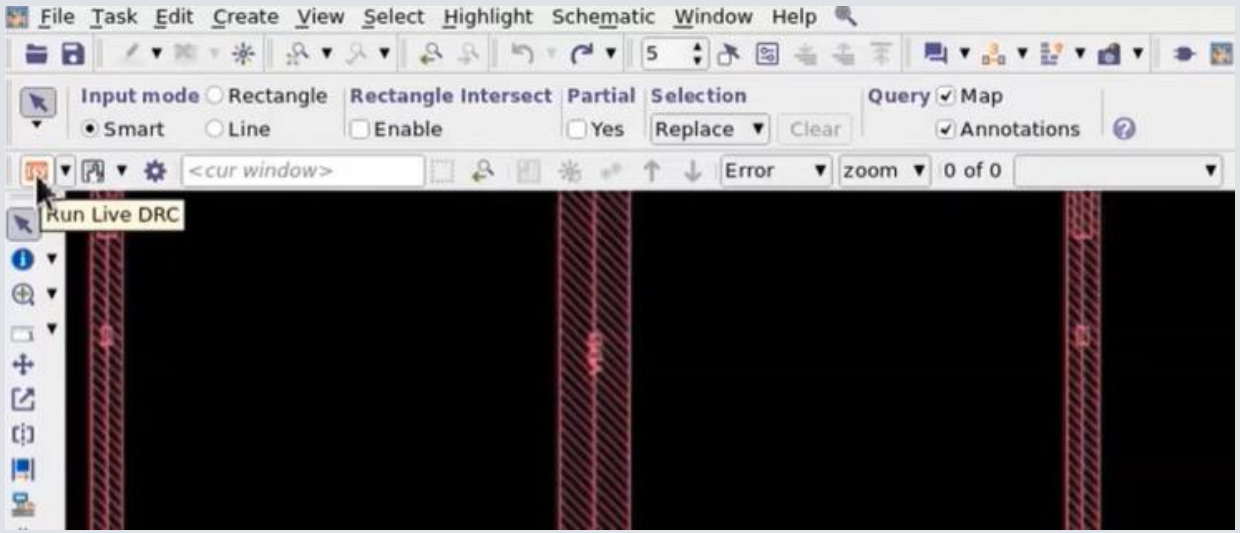


Fig. 7. Live DRC within ICC II GUI

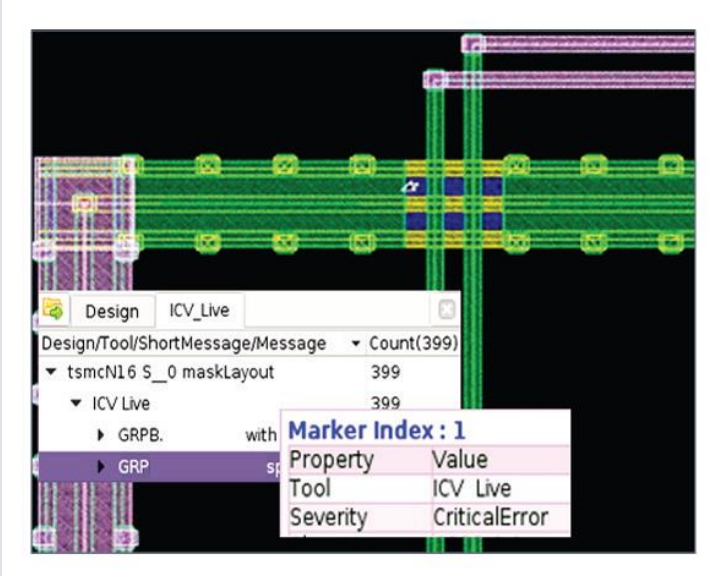


Fig. 8. Live DRC checking for Custom Design Flow

Conclusion

Conclusion

- As Advanced Nodes DRC is challenging on runtime and convergence, traditional methodology is not sufficient.
- New Methodology Innovations based on Reference Methodology improved productivity and efficiency.
- Manipulate runset and utilize ICV option to analyze and debug very quickly.
- Voltage dependent flow is necessary for voltage dependent DRC.
- Future development to improve productivity and efficiency would include layout modifications.


THANK YOU
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INNOVATION
YOUR
COMMUNITY