PrimeClosure

Accelerating ECO Convergence with PrimeClosure Advanced Technologies

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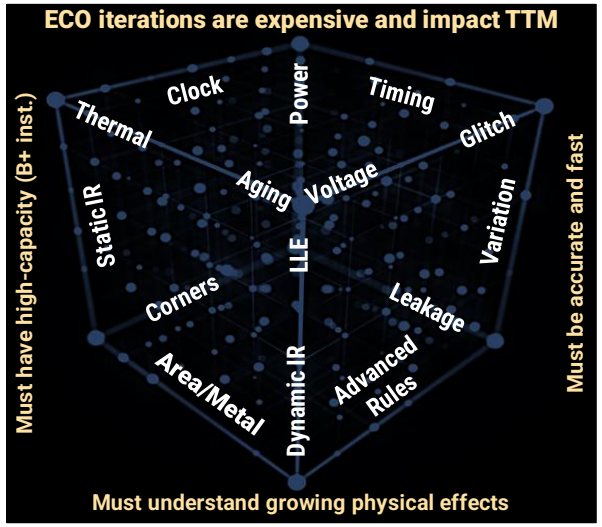
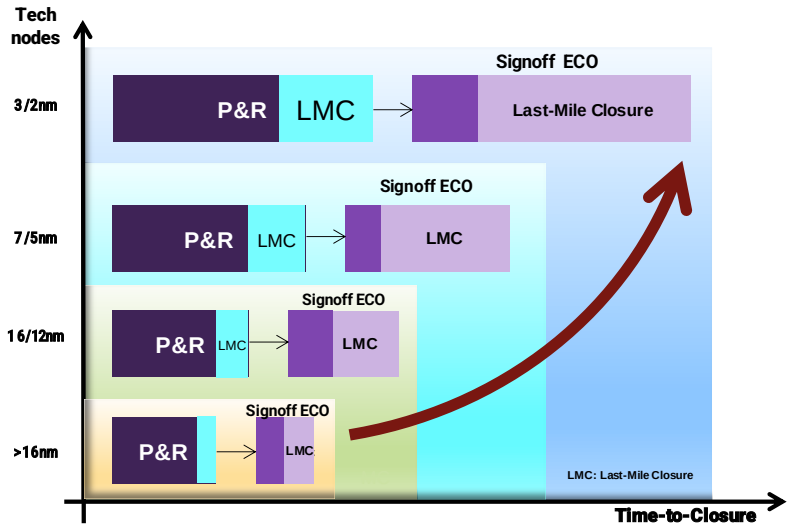
Advanced Node Challenges Impact ECO Time-to-Results

Signoff PPA last-mile design closure TAT and iterations have significantly increased

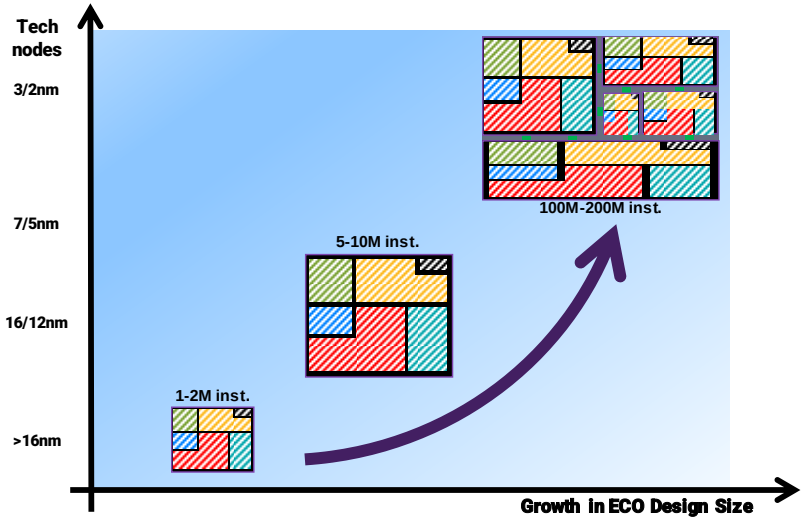
Multi-dimensional
ECO Problem Space



Advanced Node ECO
Requirements



Last-mile signoff closure
complexity growing
exponentially

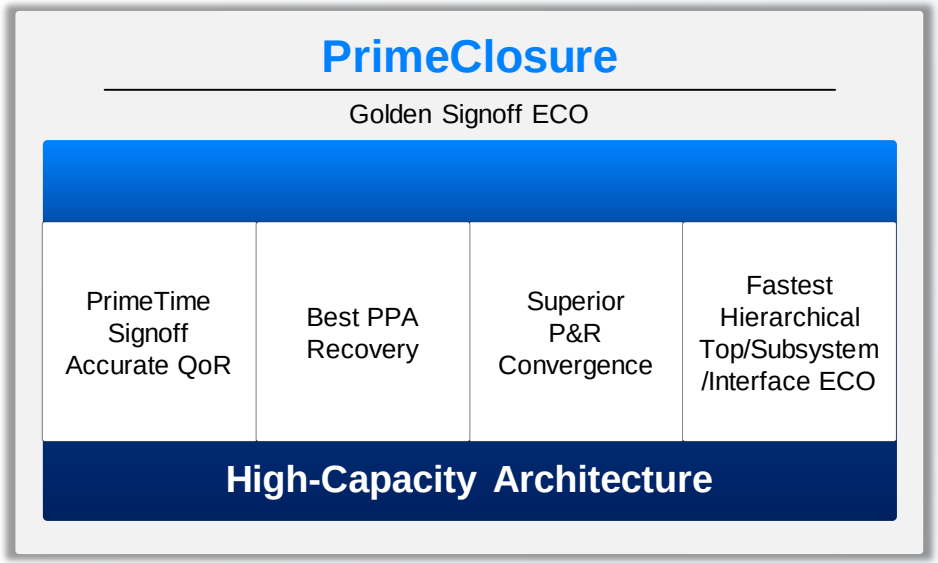


Signoff accurate
subsystem-level / closure
required for large SoCs

Increased iterations delay product time-to-market and increase project cost

PrimeClosure: Golden Signoff ECO

Next-Generation Design Closure System



~5%
Lower Total Power

~50%
Reduction in ECO Iterations

~4X
Faster Power ECO Runtime

~10X
Less Compute Resources

CPU/GPU
5/3nm
Top 5 Semiconductor
50% Better Fix Rate
10X Lesser Compute

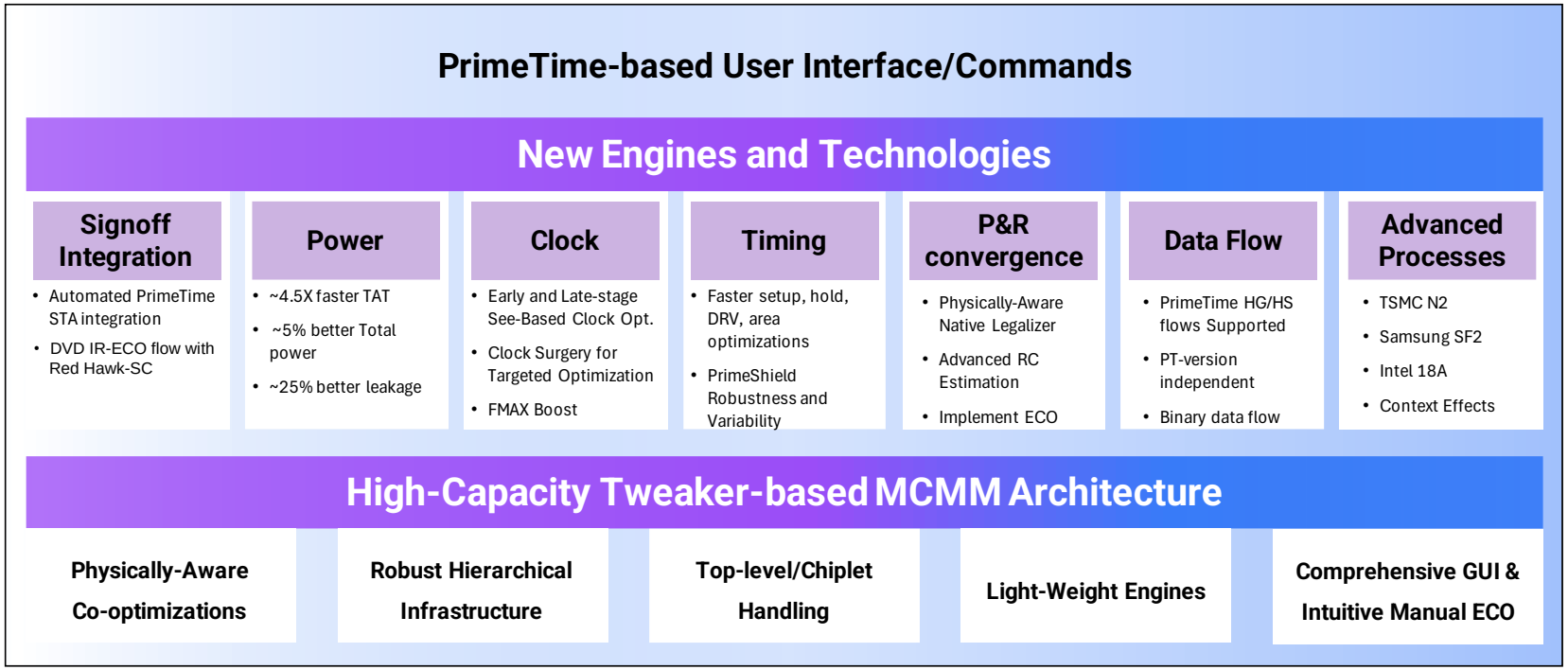
GPU
3nm
Top 5 Semiconductor
>40% Better Setup TNS
4% Lower Leakage
15% Faster TAT

CPU
5/3nm
Top US Hyperscaler
4X Faster Power ECO
27% Lower Leakage
2.2% Better FMax

CPU, SoC
3nm
Top 5 Semiconductor
4X Faster Power ECO
10X Lesser Compute
35% Lesser Iterations

High-Capacity Architecture

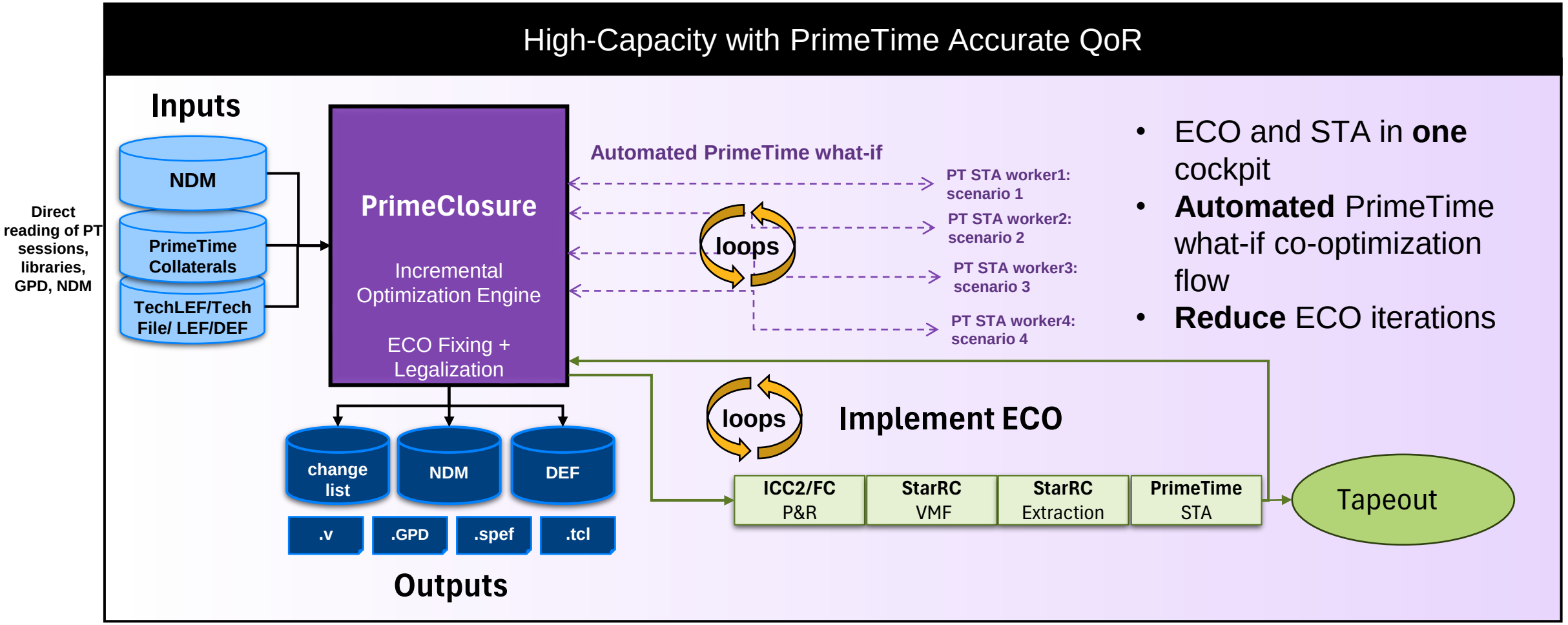
Leverages production-proven Tweaker infrastructure



- New, faster optimization TAT
- Better QoR, and PPA
- Signoff Analysis Integration
- 100% Tweaker scripts migration
- PT version independent
- Faster TAT

Automated Signoff Accurate QoR for Demanding Designs

PrimeTime integration for signoff QoR

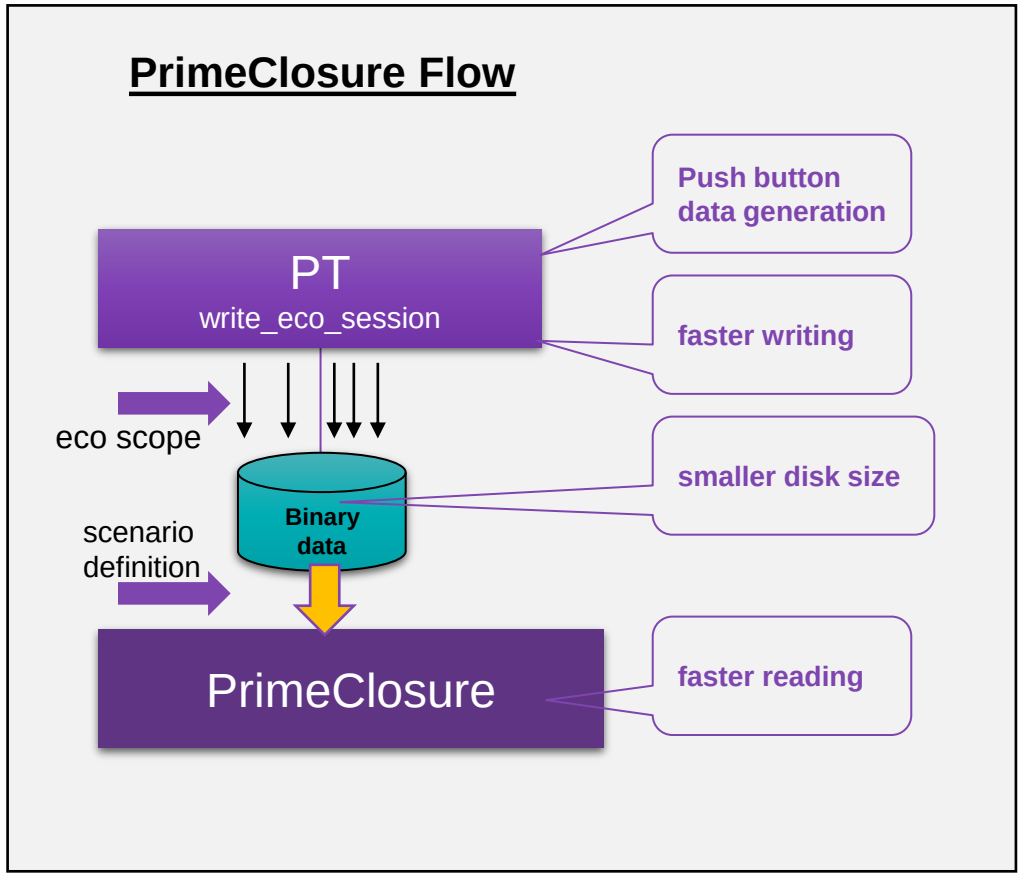


Benefits of Integrated ECO Session Data Flow

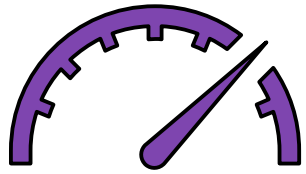
write_eco_session and start_eco auto config mechanisms

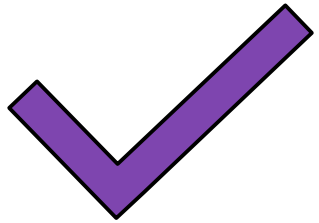
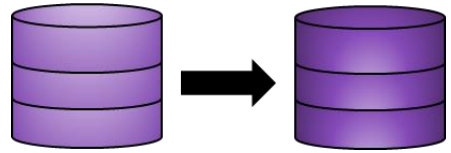
- PT settings
  - library location
  - derating, drc, aocv, pocv
  - don’t_touch, don’t_use
- simplified hier_prefix, auto partitioning flow
- timing info transfer, no need for reporting transfer
- netlist, spef, gpd, upf
- voltage scaling, MV settings
- corner building
  - eco scope
  - configurable corner definitions

Consolidated and Easy to Transfer



Key PrimeClosure Differentiations

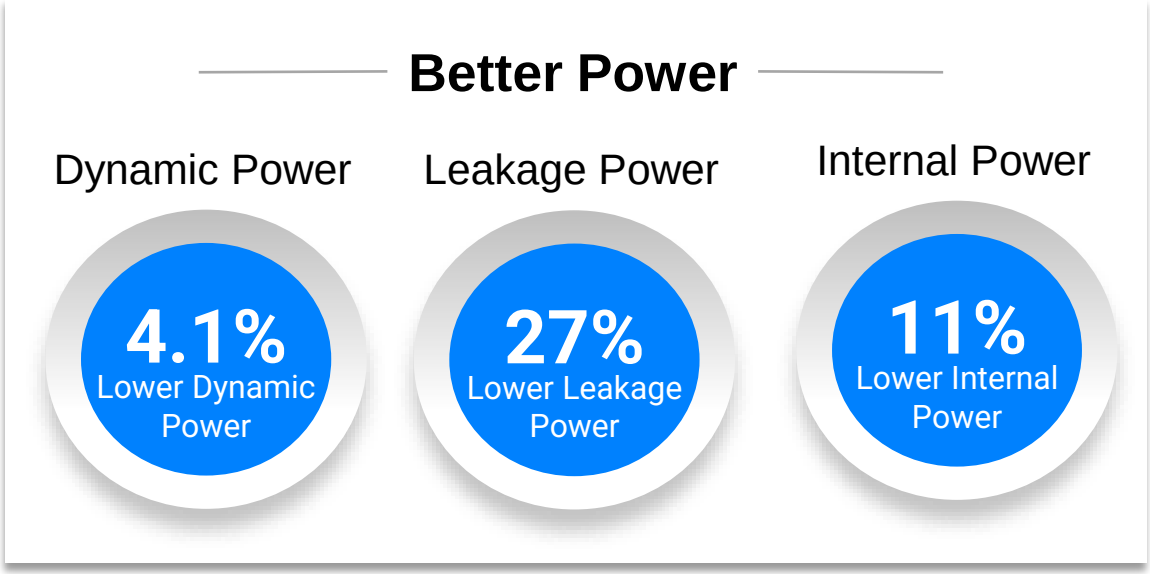
POWER	TAT	QoR	P&R CONVERGENCE	MIGRATION

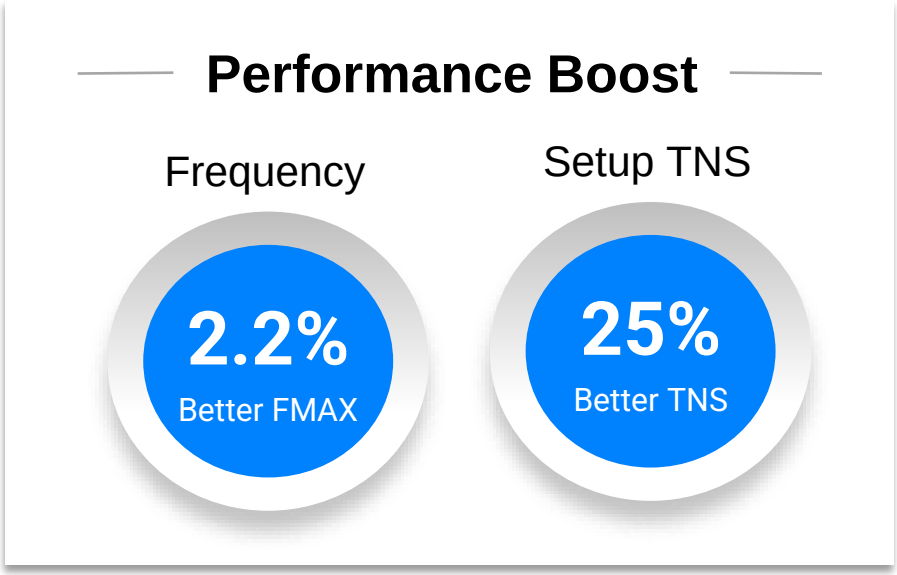
• **PPA:** up to **5% better total power** recovery
• **TAT:**
  • vs. **PT-ECO: ~4X** faster
  • vs. **Tweaker: ~2X** faster
	• **TAT: ~2X faster** vs. Tweaker
	• Input **collateral size**: **~50% reduction** vs. Tweaker
		• **QoR**: Better via **OOTB (out-of-the-box) recipe**
		• **Automated PrimeTime** what-if for signoff-accurate optimization
		• Automated **IR-ECO with RedHawk-SC**
			• **Convergence:** Advanced RC estimation, router guidance, congested design
			• **Incremental Fusion Compiler/Signoff flow**
			• **3rd party P&R:** Flow supported
				• Migration: **100% of Tweaker** scripts to PrimeClosure
				• Migration: **PT cross version support**
				• **PT-HS** and **PT-HG** flows supported

Top US Hyperscaler Reduces Power and Boosts Performance

Results on Arm Neoverse v3

Design: 3nm, ~7M instances, 16 cores, Peak Memory: 150GB





Power Group	Leakage (mW)	
	Combinational	Register
preECO	158.9	53.4
postECO	111.7	40.8
Savings	47.2	12.6
Average	-27%	

Power Group	Internal (mW)	
	Combinational	Register
preECO	30.6	99.7
postECO	28.1	86.3
Savings	2.5	13.4
Average	-11%	

- **Clock Surgery** delivered 2.2% FMAX boost
- TNS improved by about ~25% on endpoint opt DB
- **Power ECO TAT is ~4X faster TAT**
- Results are post-implementation

PrimeClosure Delivers Superior Results @ 5nm Evaluation

Better Hold QoR, Setup QoR, TAT, and post implementation vs. Tweaker

Timing QoR Comparison (PC vs. TWK)

Post Tweaker eco - timing

Hold violations (Pre-ECO->Post-ECO)

	Total	reg ->	reg
WNS	-0.17 -> -0.17	-0.14 ->	-0.10
TNS	-864.29 -> -271.42	-625.52 ->	-32.67
NUM	90675 -> 10708	82367 ->	2404

Setup violations (Pre-ECO->Post-ECO)

	Total	reg ->	reg
WNS	-0.18 -> -0.18	-0.10 ->	-0.01
TNS	-384.36 -> -378.98	-5.39 ->	-0.01
NUM	7274 -> 6514	760 ->	1

Post PC eco - timing

Hold violations (Pre-ECO->Post-ECO)

	Total	reg ->	reg
WNS	-0.17 -> -0.17	-0.14 ->	-0.05
TNS	-864.62 -> -243.89	-625.85 ->	-5.15
NUM	90706 -> 8800	82398 ->	498

Setup violations (Pre-ECO->Post-ECO)

	Total	reg ->	reg
WNS	-0.18 -> -0.18	-0.10 ->	-0.00
TNS	-384.36 -> -378.98	-5.39 ->	-0.00
NUM	7274 -> 6515	760 ->	2

- **~84% improvement in Hold QoR**
- **>4X reduction in violations**
- **Better improvement in Setup QoR**

Post-implementation (PC vs. TWK)

Post tweaker eco implementation - hold timing

min	WNS	TNS	PATHS	100	50	20	10	5	0
core_clk	-0.1	-42.731	5640	0	69	491	627	850	3603
ate_core_clk	-0.1	-41.702	5368	0	66	482	624	824	3372
wrck_clk	-0.054	-1.144	230	0	2	12	14	21	181
CIF	-0.047	-0.771	149	0	0	6	16	15	112
clock_gating_default	-0.008	-0.019	8	0	0	0	0	1	7
ate_wrck_clk	-0.001	-0.001	1	0	0	0	0	0	1
TOTAL_R2R	-0.1	-86.368	11396	0	137	991	1281	1711	7276

Post PC eco implementation - hold timing

min	WNS	TNS	PATHS	100	50	20	10	5	0
core_clk	-0.068	-12.889	3266	0	1	77	185	354	2649
ate_core_clk	-0.068	-12.039	2986	0	1	74	178	336	2397
wrck_clk	-0.035	-0.46	123	0	0	5	7	6	105
CIF	-0.017	-0.285	122	0	0	0	2	2	118
clock_gating_default	-0.006	-0.018	6	0	0	0	0	1	5
ate_wrck_clk	-0.004	-0.008	3	0	0	0	0	0	3
TOTAL_R2R	-0.068	-25.699	6506	0	2	156	372	699	5277

- **~70% better Hold QoR**

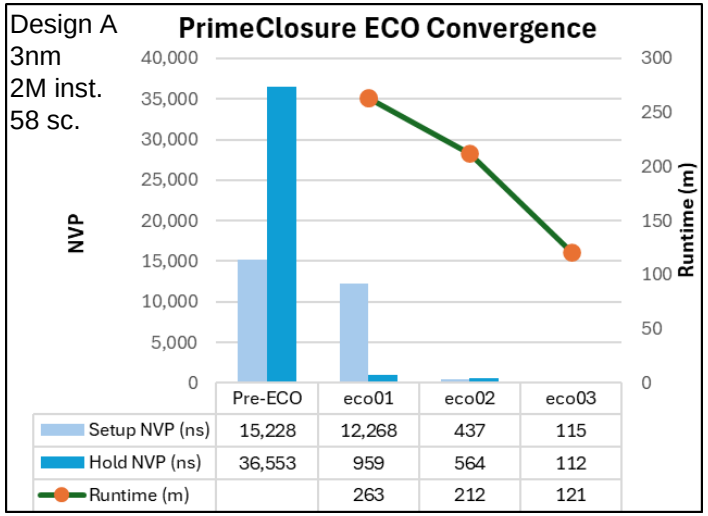
- Technology node: N5
- Size (# of cells/mem):3.57M/510
- # of Corner: 12
- Violation type: max_tran, setup,hold

Source: Cisco May 6 eval summary

Top 5 Semiconductor Reduced ECO Iterations by 40%

PrimeClosure delivered better timing, leakage power, and TAT

Design A
3nm
2M inst.
58 sc.

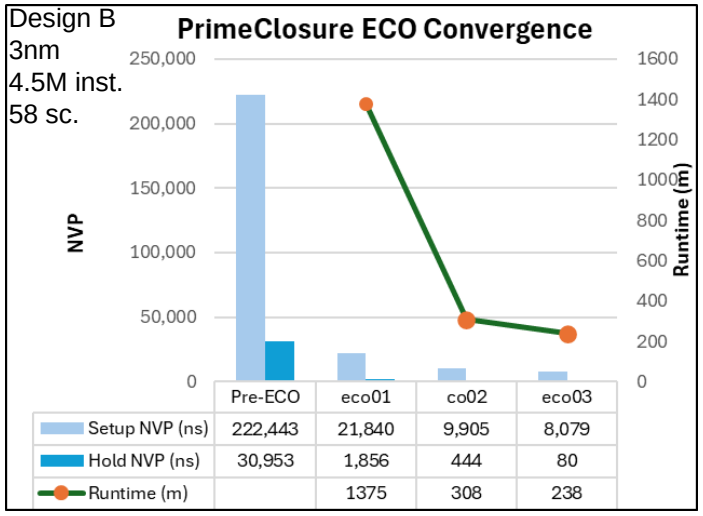


	Pre-ECO	eco01	eco02	eco03
Setup NVP (ns)	15,228	12,268	437	115
Hold NVP (ns)	36,553	959	564	112
Runtime (m)		263	212	121

TAT Target
eco01: < 24hrs
eco02: < 20hrs
eco03: < 10hrs

PC TAT (16 cores)
eco01: 4.4hrs
eco02: 3.5hrs
eco03: 2.0hrs

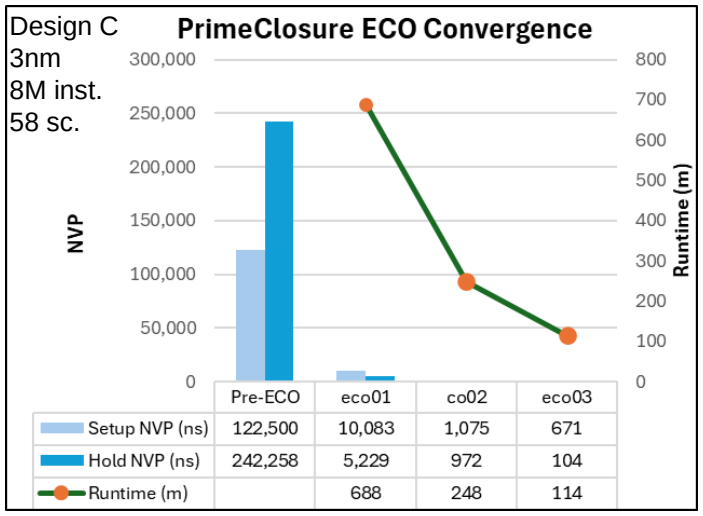
Design B
3nm
4.5M inst.
58 sc.



	Pre-ECO	eco01	co02	eco03
Setup NVP (ns)	222,443	21,840	9,905	8,079
Hold NVP (ns)	30,953	1,856	444	80
Runtime (m)		1375	308	238

PC TAT (16 cores)
eco01: 22.9hrs
eco02: 5.1hrs
eco03: 3.9hrs

Design C
3nm
8M inst.
58 sc.



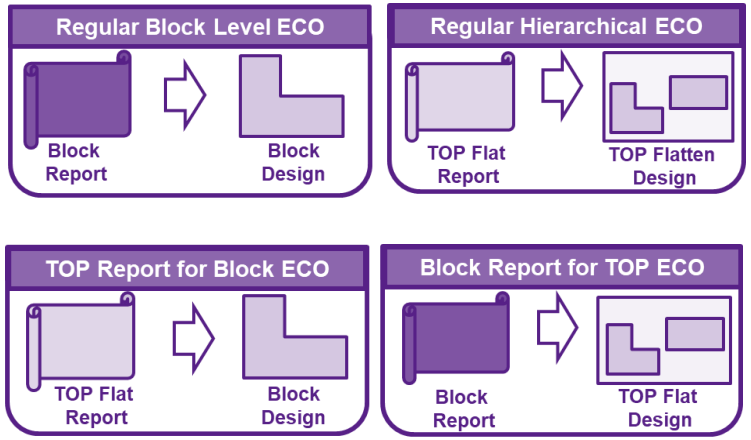
	Pre-ECO	eco01	co02	eco03
Setup NVP (ns)	122,500	10,083	1,075	671
Hold NVP (ns)	242,258	5,229	972	104
Runtime (m)		688	248	114

PC TAT (16 cores)
eco01: 11.4hrs
Eco02: 4.1hrs
Eco03: 1.9hrs

- TAT can be reduced with more cores

Strong Hierarchical Technologies Reduce Time-to-Results for Large Designs

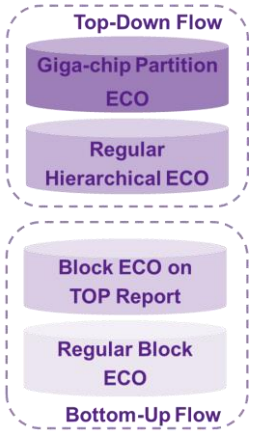
Robust Hierarchical, Gigachip Hierarchical ECO



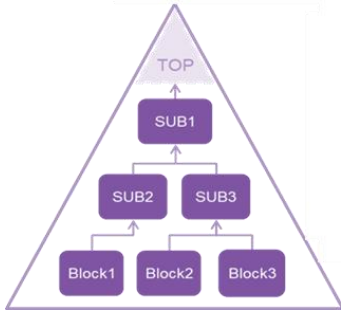
Multiple hierarchical flows to enable fastest TAT, memory reduction on single boxes → ***low cost-per-run***

Top-Down, Bottom-up Hierarchical Flow

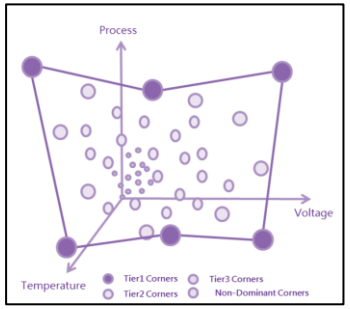
- **Gigachip** hierarchical ECO for **very large designs**
- **Single-box** SoC/ subsystem/ block/ MIM convergence with **PrimeTime: HyperScale, HyperGrid, Flat STA**



Hierarchy and Corner Pruner



Hierarchy Pruning



Corner Pruning

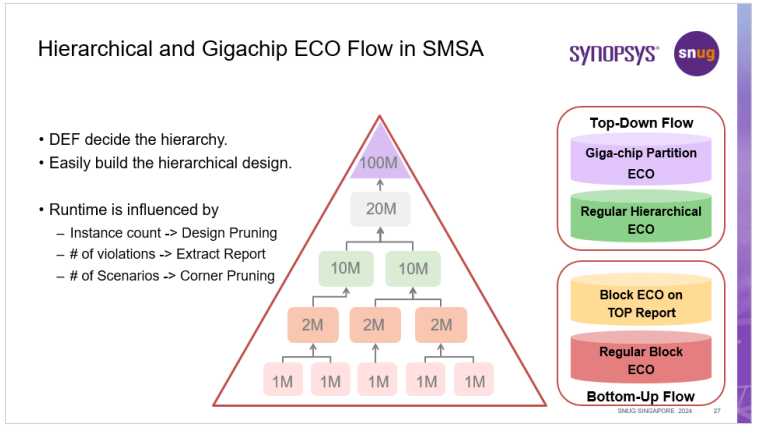
Pruner:

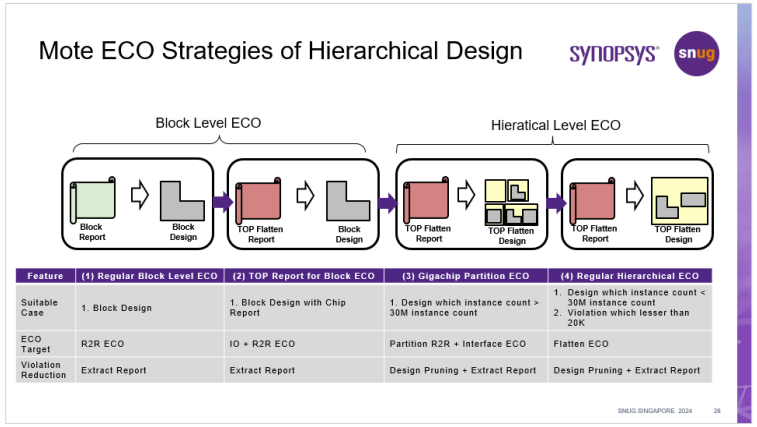
- **~30% lower memory with** hierarchy and corner reduction
- ***2X Speedup TAT***

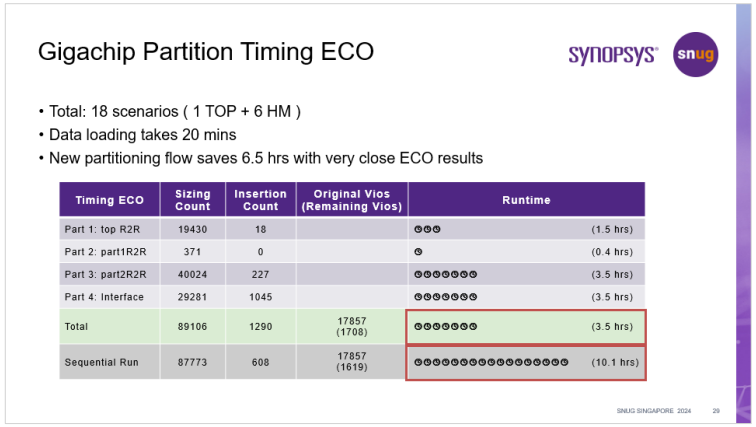
PrimeClosure Gigachip Hierarchical Flow

Hierarchical ECO TAT Acceleration Solution

- Runtime Bottleneck Identification
- ECO Strategies to Reduce TAT
- Speed up with Gigachip Hierarchical Flow

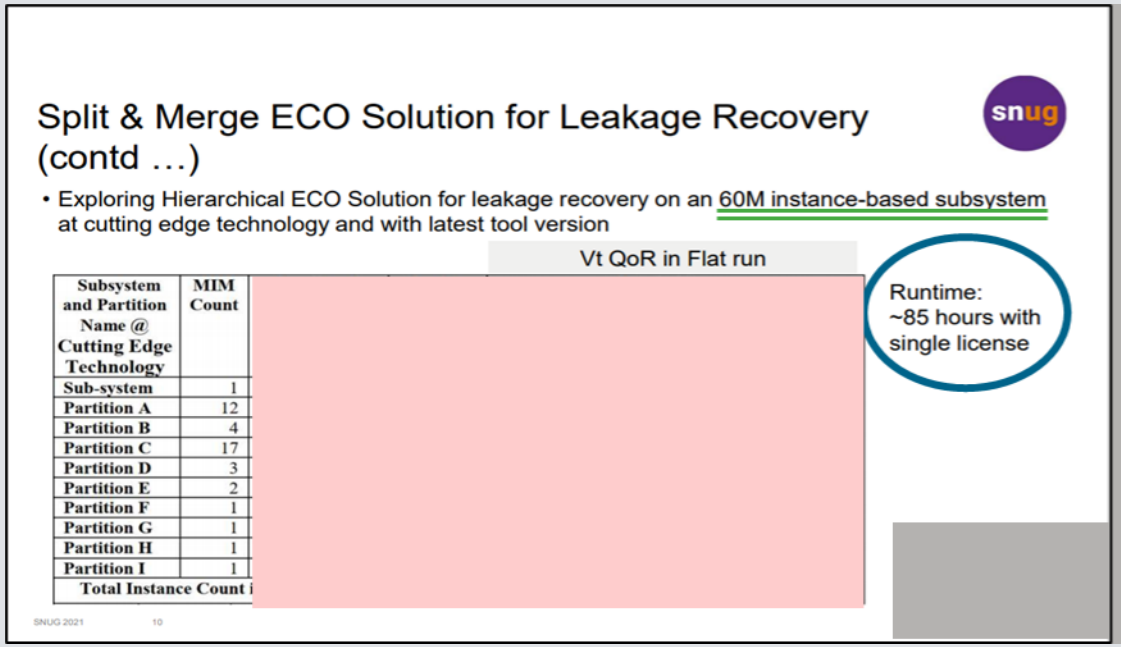


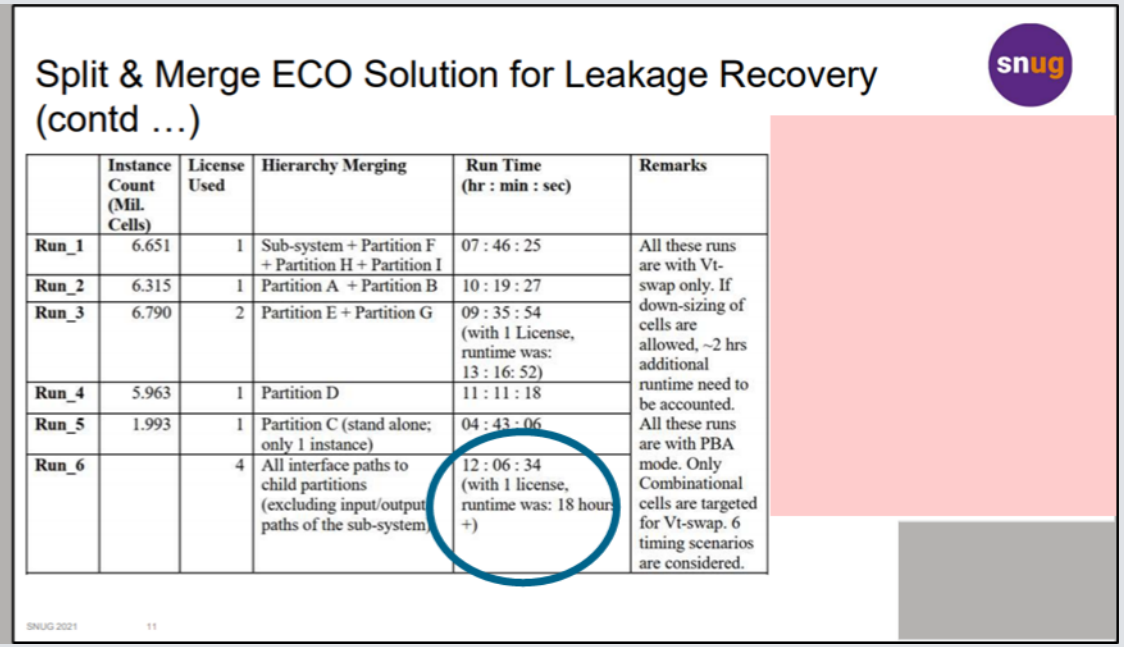




Hierarchical Leakage Recovery Delivers ~7X TTR Speedup

Top 10 semiconductor company presentation at SNUG



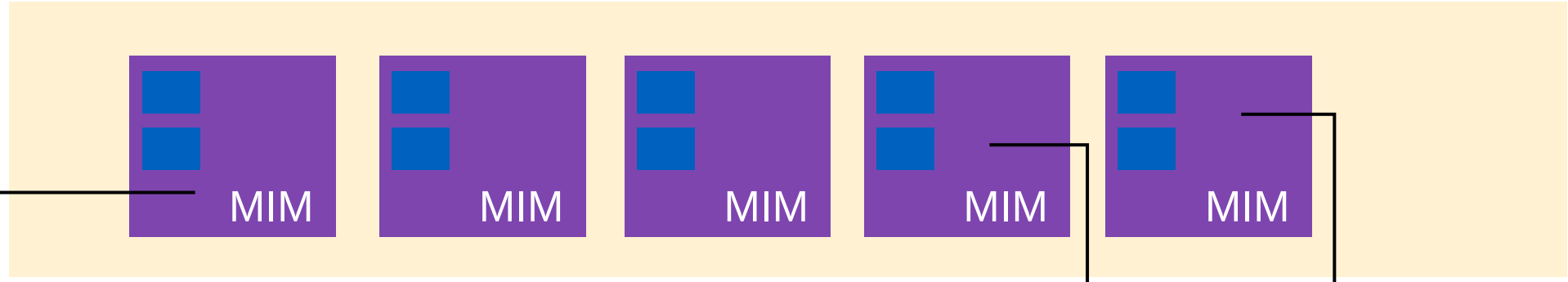


Total Time-to-Results Reduced from 85hours to 12hours

Efficient MIM Flow

Multiple Instantiated Module Flow

- ECO for MIM
- Hierarchical MIM
- Consolidated Timing Information



Blocking Code Shows
ECO pin (max, min)
impacted pin (max, min)
Estimated Timing Post ECO
DRC impact pins

Check All At Once

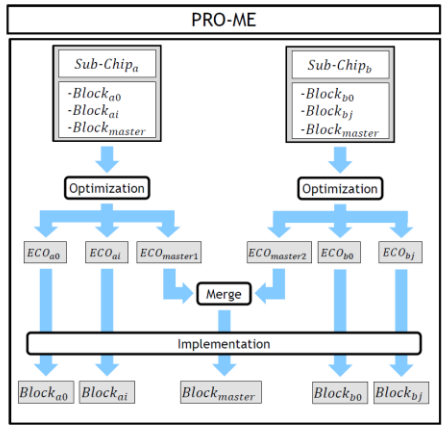
Customer Success Story of MIM Flow

- Merge ECO Flow user example presented in SNUG 2024

Proposed Model: PRO-ME

Case 1: with one shared block

- merge step
  - Merge ECO feature in Tweaker tool
- Remove serial dependency
  - $Sub\text{-}Chip_a$ and $Sub\text{-}Chip_b$ use same netlist for PPA
  - Run PPA optimization simultaneously
- Remove unnecessary implementation job
  - One ECO file for $Block_{master}$
  - Only one implementation



Results

- Testcase:
  - Two sub-chips, each with 12 blocks
  - 2 blocks are instantiated in both sub-chips
- Runtime improvement
- Better Quality of Results in timing

Metric	Value
% Runtime Improvement	47.32%
% Resource Reduction	4.35%

Metric	Setup % Improvement	Hold % Improvement	Transition % Improvement
Worst Negative Slack	58.66%	45.27%	0.02%
Total Negative Slack	97.54%	98.06%	86.87%
Endpoints	89.50%	95.13%	39.12%

https://www.synopsys.com/community/snug/snug-silicon-valley/location-proceedings-2024.html

Scope Based Technology Applied to ECO Phases

Result in Faster TAT, Reduced File Size, Flexibility to Selectively Group Output

Scope Based Data Preparation

ECO Session

- scope based
- smaller size
- faster dump time
- block context info

Scope Based ECO

- load faster
- no extra filter needed
- Golden Sign off data

ECO

- focused ECO
- simplified fixing scripts
- Easier violation review

Scope Based ECO Tcl

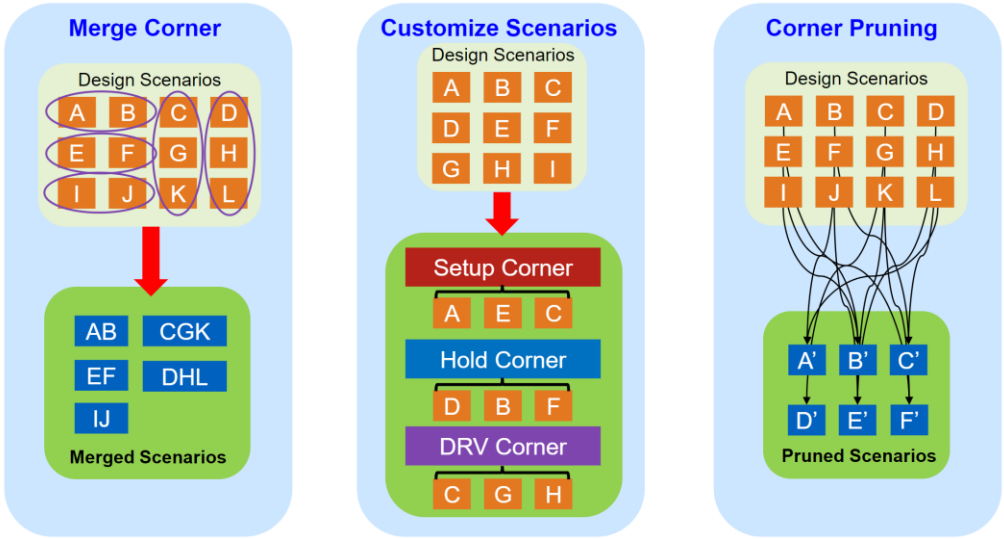
- Selective implement
- Checks before apply
- Error version proof

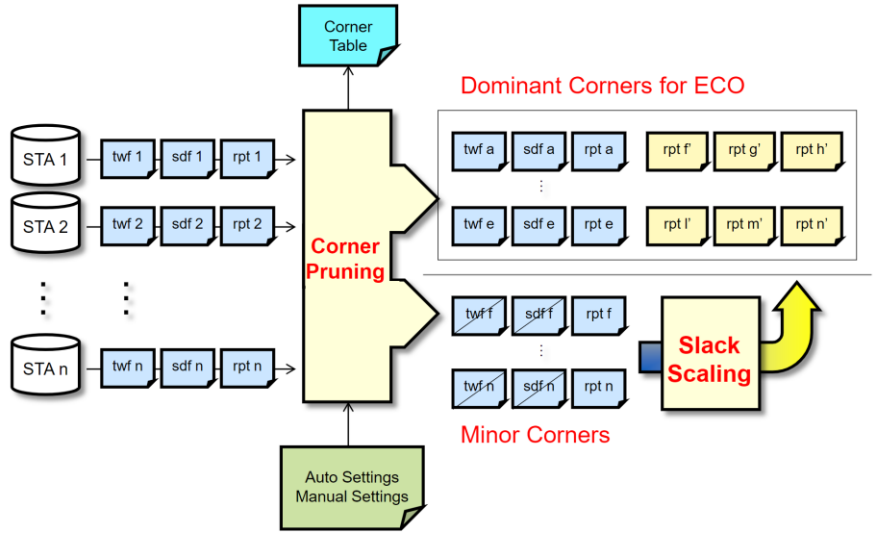
Implement

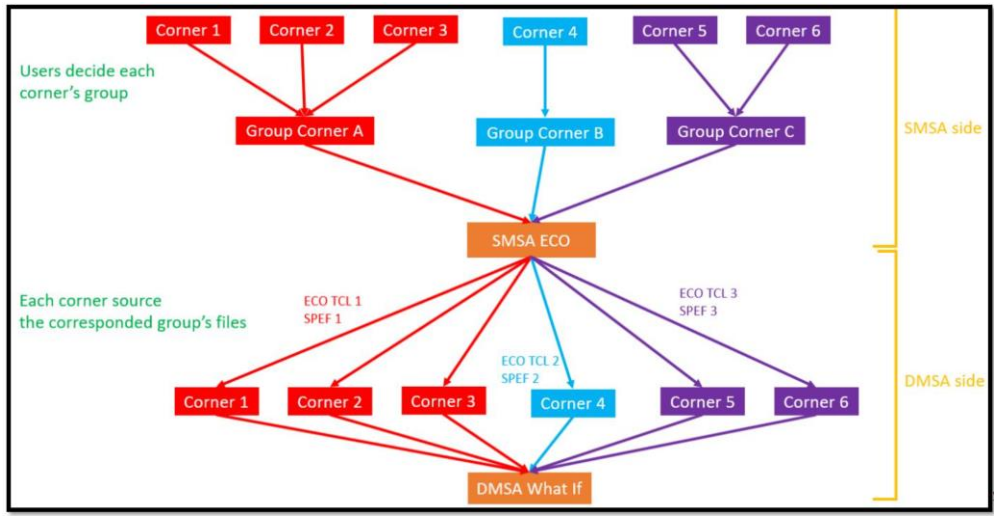
Smart Corner Reduction Technologies

Enables Faster TAT and Memory Reduction

- Merge Corner
- Customizable Scenario Definitions
- Corner Pruning

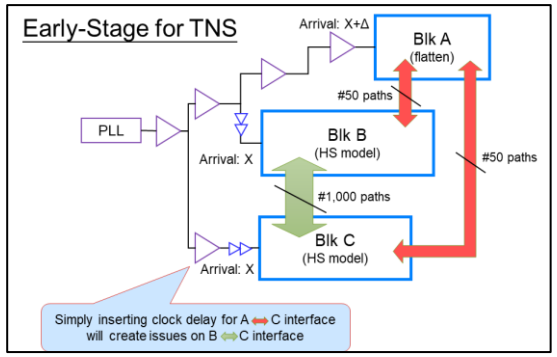


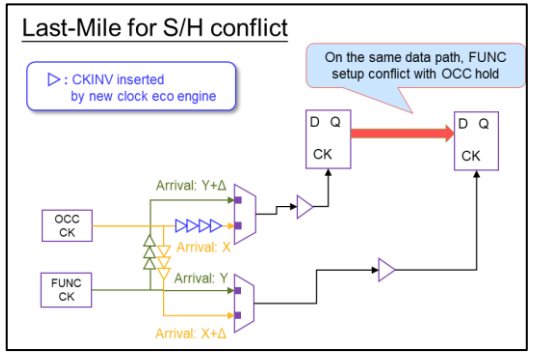




Seed-Based Clock ECO Improves Timing and Convergence

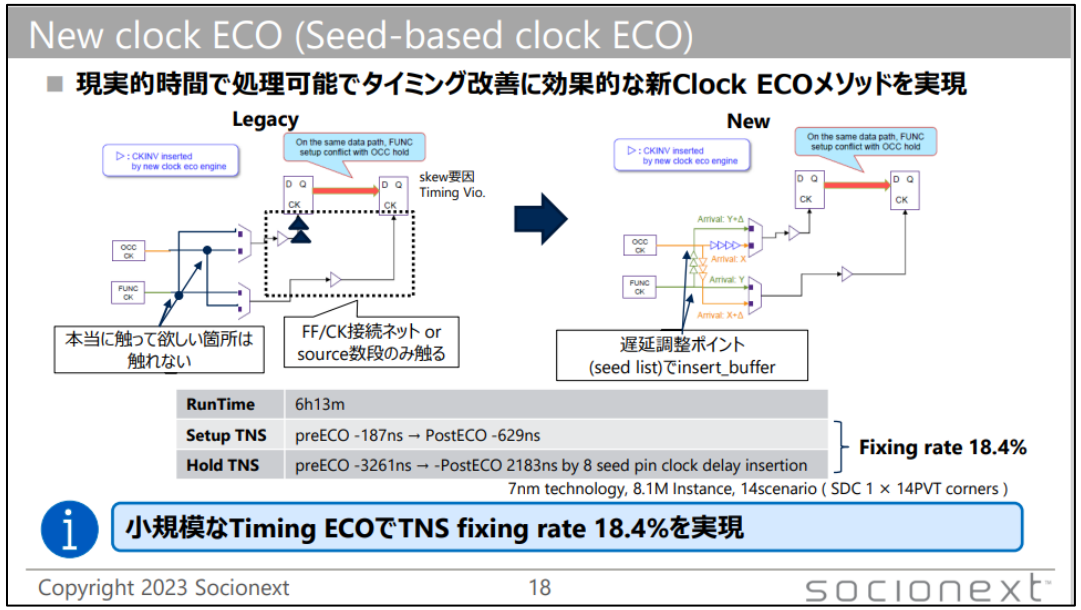
Better TNS and improved productivity





- New technology looks at optimal locations along entire clock network
- Minimizes # of points where changes need to be made (insertion, bypass)
- Looks across multiple stages, applicable to both block or cross boundary paths

Socionext: TNS Fixing Rate Improved by 18%

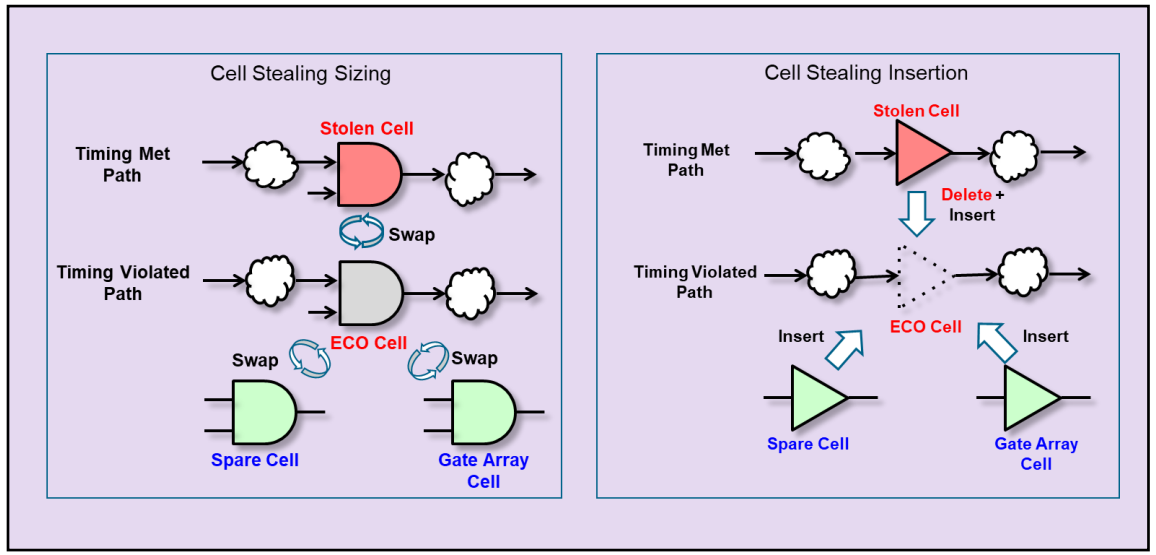


Seed Base Clock ECO Target Total TNS (setup+hold) and improved 18.4% by just performing 8 insertion commands

Unique Metal ECO Transforms Driven Further Timing Closure

Demonstrated ~60% setup TNS improvement at top memory company

Post-Mask Transforms Improve Timing QoR



Timing ECO Results (Postmask)

Postmask ECO(Gate Array)(1st run) (Slacks in the table were obtained by PrimeTime STA)

Tool	Setup (Worst corner)			Hold (Best corner)			Cell area increased(um^2)	Runtime(h:m:s)
	WNS(ns)	TNS(ns)	FEP	WNS(ns)	TNS(ns)	FEP		
Base timing	-3.457	-168.6	178	-0.420	-74.1	985	-	-
Tweaker	-1.794	-59.555	130	-0.260	-9.173	123	23519.69	00:13:01
PrimeTime (Physically aware)	-3.582	-253.1	393	-0.192	-2.8	47	18011.32	00:10:23

- Setup: Mainly improved by cell stealing (over 60% improvement in TNS)
- Hold: Mainly improved by buffer insertion

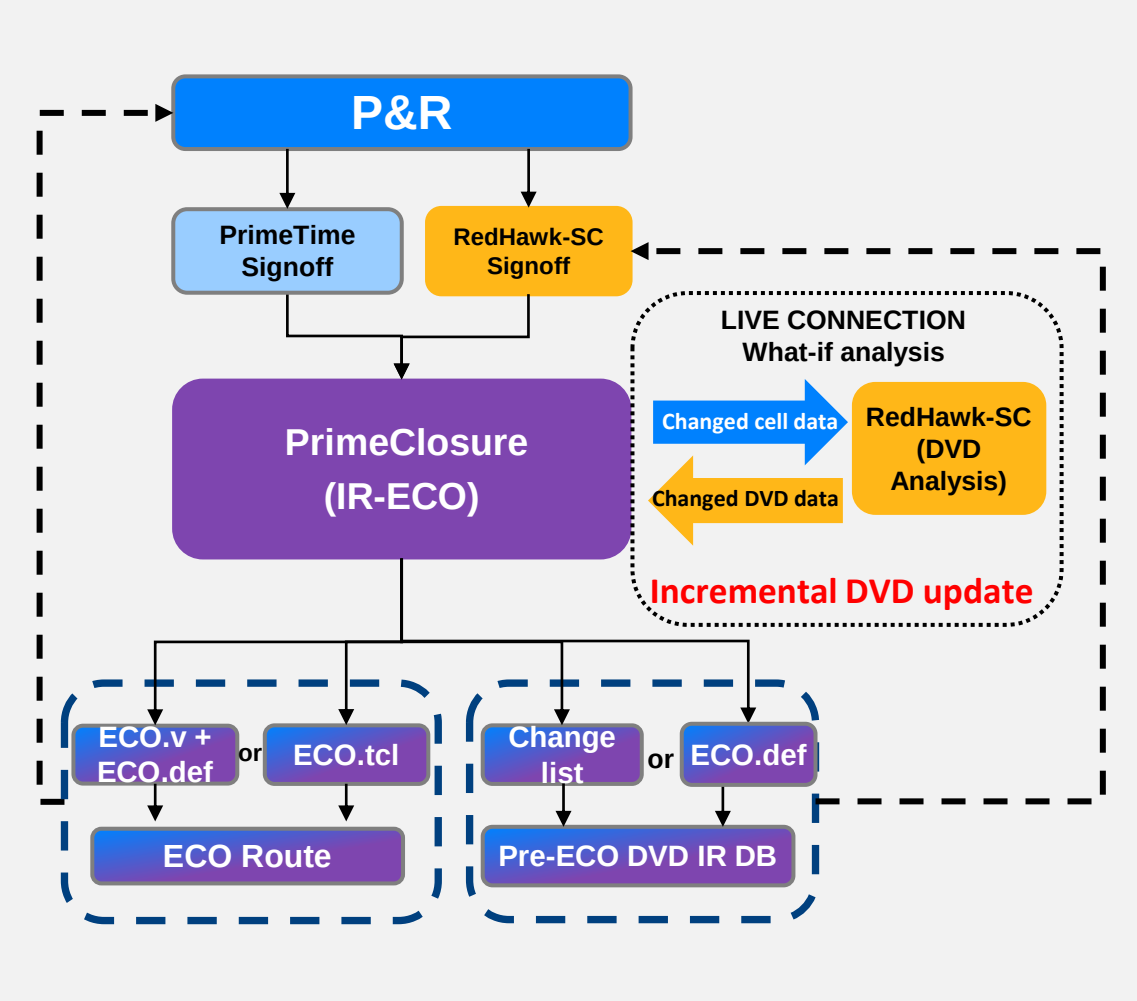
Better QoR for setup timing can be obtained by using cell stealing technology while maintaining hold timing

- Numerous post-mask transforms for improving timing QoR
- SpareCell/GateArray/RecyclingCell/ConstantCell/CellStealing

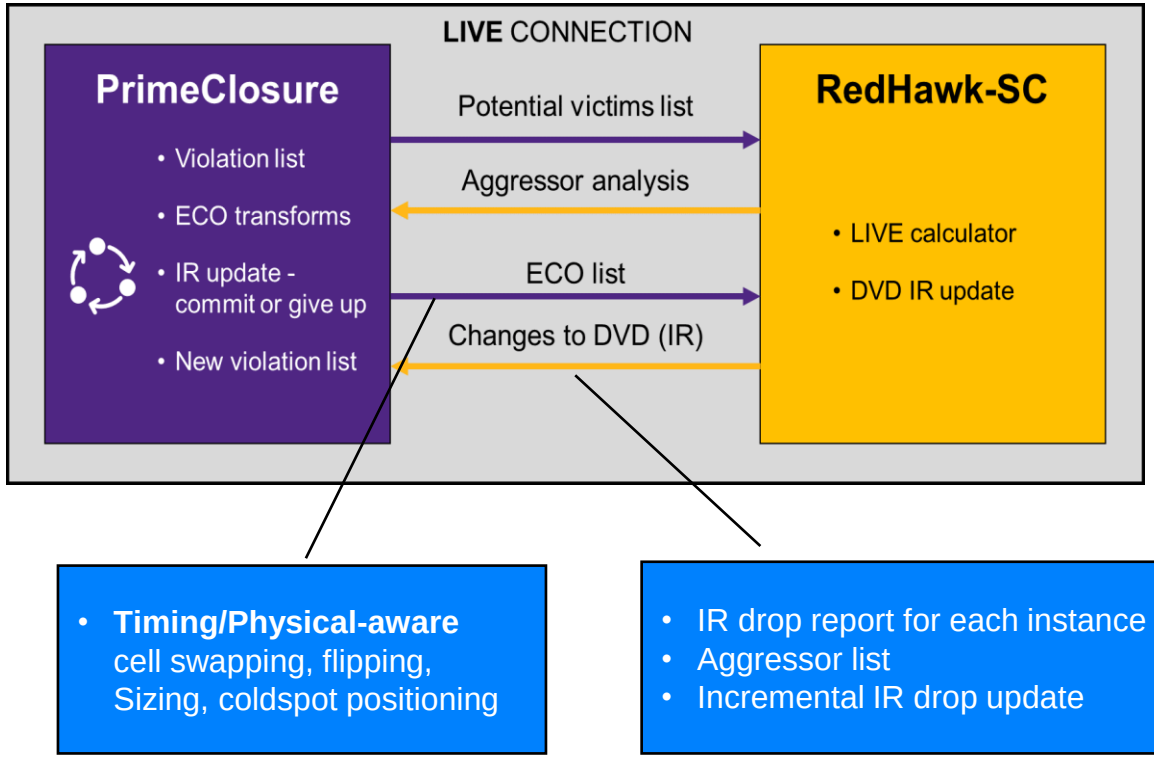
- Better setup timing QoR using cell-stealing technology
- >60% improvement in setup TNS

PrimeClosure / Redhawk-SC Dynamic IR-ECO Flow

State of the art Ansys and Synopsys collaboration to ensure convergent last-mile closure



- Incremental Automated IR Drop Update Methodology

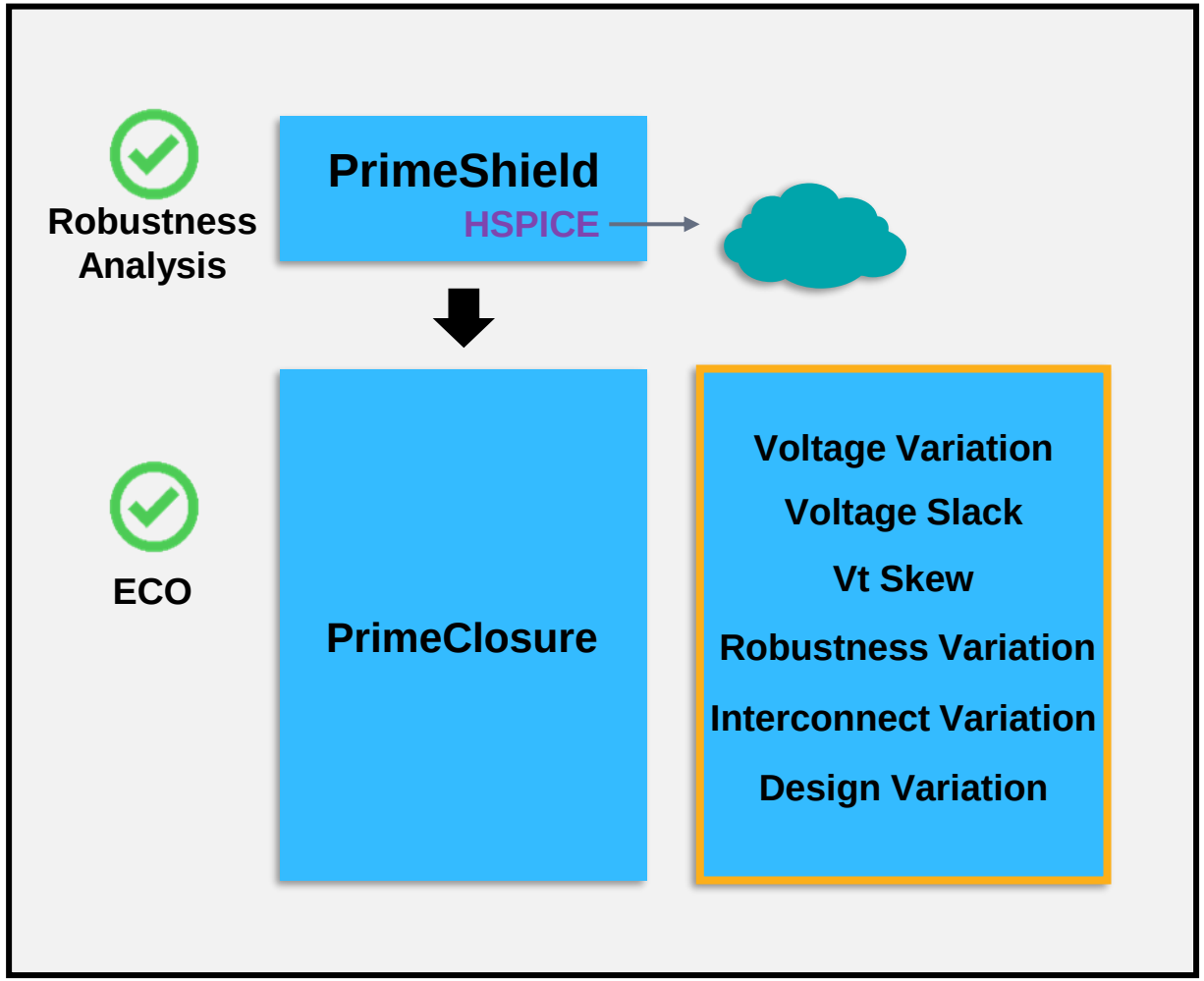


PrimeClosure/PrimeShield Robustness ECO Flow

Improved design reliability with PrimeShield analysis and PrimeClosure ECO fixing

- Integrated with PrimeShield robustness analysis PrimeClosure brings superior closure for robustness, voltage, parasitic variation, aging analysis improves overall design PPA-RA (Power, Performance, Area, Robustness, Aging).

Robustness Type	ECO Type	smsa fix types	ECO Methodology
Cell Robustness	Variation	variation	VT_swap + sizing
	Voltage	voltage	
	Transition	transition	
Path Robustness	Voltage slack (Vmin)	voltage_slack	VT swap + sizing
	VT skew (Mix VT)	vt_skew_setup vt_skew_hold	VT swap + Sizing + insertion
	Interconnect skew (BEOL)	isa_setup isa_hold	VT swap sizing+insertion
	DvD-aware ECO	setup hold	VT swap + sizing +insertion
Design Robustness	POCV variation	dva_setup dva_hold	VT+sizing+ insertion
	Bottleneck	bottleneck	VT+sizing



PC UI – Simple and Fully Customizable

```
# hier-prefix for block instances

sdfin -collateral ./top_timing/ -hier_prefix block1

begin_corner ss_cworst
...
twfin -collateral ./top_timing/ -hier_prefix block1
...
slackin -collateral  -setup -hold ./top_timing/-hier_prefix block1
slackin -collateral  -max_trans ./top_timing/ -hier_prefix block1
slackin -collateral  -setup -hold ./block_timing/

...
end_corner ss_cworst
```

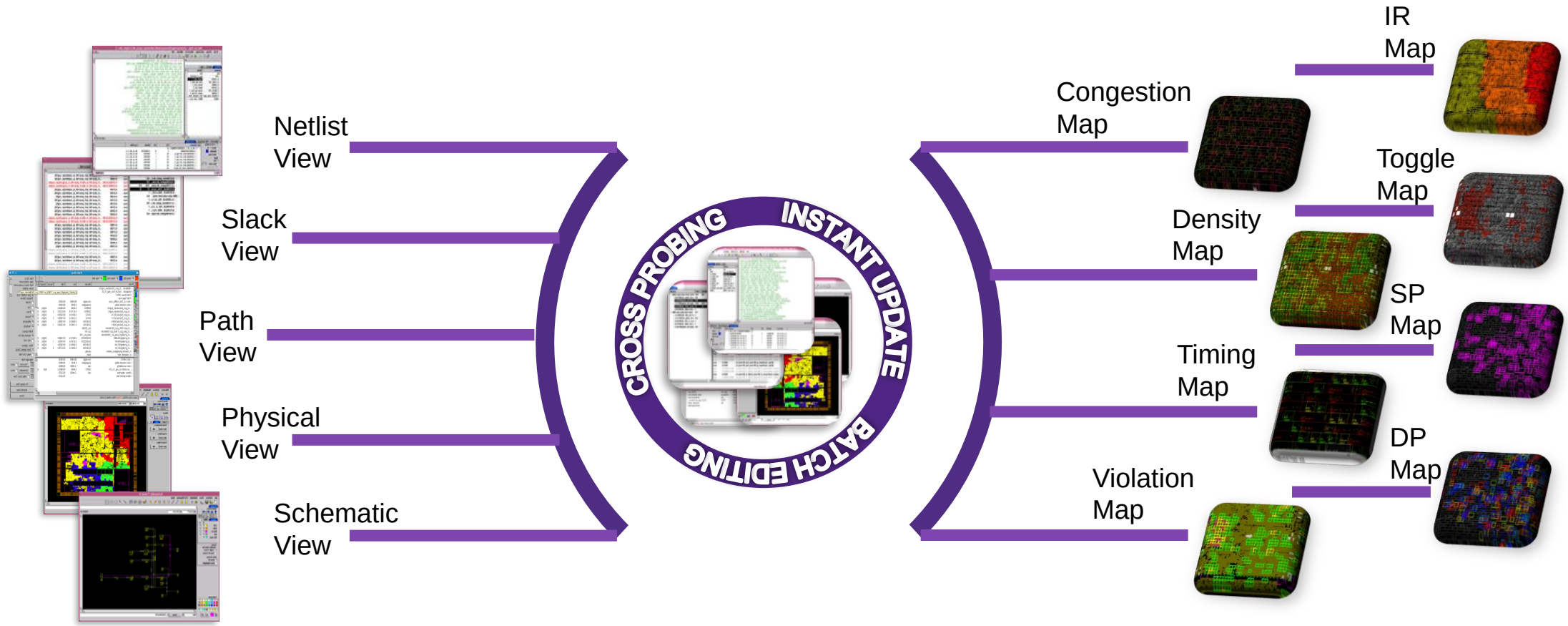
```
# put each corner's ChipTop report in blk collateral directory
# specify the ChipTop report name and hier_prefix options

start_eco -mode smsa -hier_prefix block1
```

```
# put each corner's ChipTop report in blk collateral directory
# specify the ChipTop report name and hier_prefix options

start_eco -mode smsa -add_slackin_name \
  { {setup_to_pc_ChipTop.rpt "-extended_if"} \
  {hold_to_pc_ChipTop.rpt "-extended_if"} }
```

```
# add slackin command for loading ChipTop in every corner

begin_corner S1
       set_group -lib -name corner_S1
       ...
       twfin twf.gz
       slackin S1/setup_to_pc.rpt
       slackin S1/setup_to_pc_ChipTop.rpt -extended_if
       slackin S1/hold_to_pc_S1.rpt
       slackin S1/hold_to_pc_ChipTop.rpt -extended_if
end_corner S1
begin_corner S2
       set_group -lib -name corner_S2
       ...
       twfin twf.gz
       slackin S2/setup_to_pc.rpt
       slackin S2/setup_to_pc_ChipTop.rpt -extended_if
       slackin S2/hold_to_pc_S1.rpt
       slackin S2/hold_to_pc_ChipTop.rpt -extended_if
end_corner S2
```

Powerful GUI – Final Stage ECO Solution

Violations analysis through different Views, design analysis through different Maps



Clear blocking messages for un-fixable violations

Versatile and interactive editing in all views

Very easy flow control and maintenance

Summary:
PrimeClosure Delivers Best PPA Recovery with Signoff QoR

- MCMM architecture to handle B+ instance designs, and deliver lower cost-per-run
- Efficient resource utilization for multi-billion instance designs
- 100% PrimeTime accurate QoR reduces ECO iterations
- Seamless convergence with P&R with signoff accuracy
- High Capacity to handle 100's of block with mixed PNR solution


THANK YOU
Our Technology, Your Innovation™