Synopsys Fusion Compiler Enhancements for Improved Out-of-the-box PPA with Intel 18A

Ahmet Ceyhan, Principal Engineer and Engineering Manager
Intel Foundry

Agenda

Agenda

Body Slide Subtitle

- Intel Foundry Offerings
- Intel 18A Ribbon FET and Power Via Technologies
- Differentiated Intel 18A PPA Enhancements and Results
  - Recap of Differentiated PPA Phase 1 Details and Results
  - Differentiated PPA Phase 2 Details and Results
  - Future Enhancements
- Conclusions

Intel Foundry Offerings

IDM2.0 Strategy and Roadmap

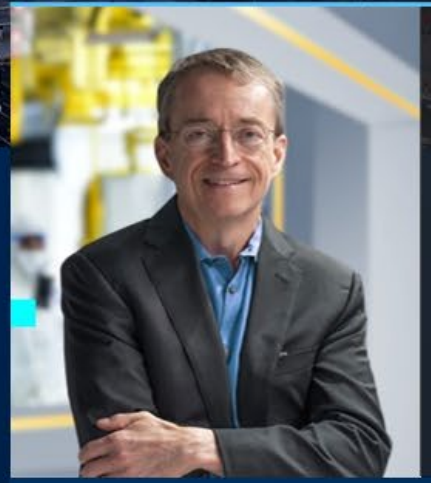
IDM 2.0

Internal factory network

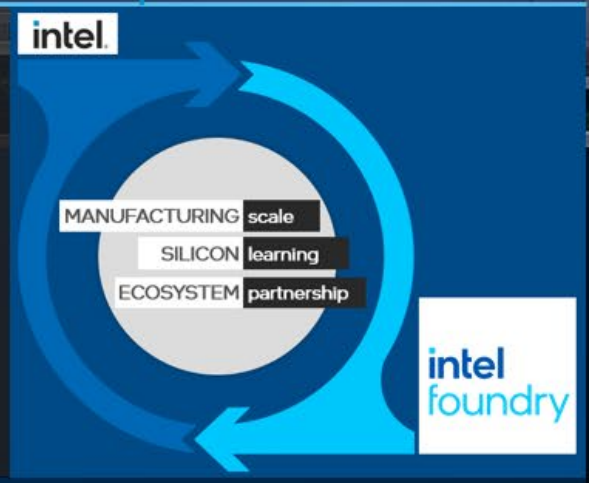
External foundries

Intel Foundry

World's #2 Foundry in This Decade



"We will be **differentiated** from other Foundry offerings with a combination of **leading-edge packaging and process technology**, committed capacity in the **US and Europe** – available for customers globally – and a world-class **IP portfolio** that customers can chose from."

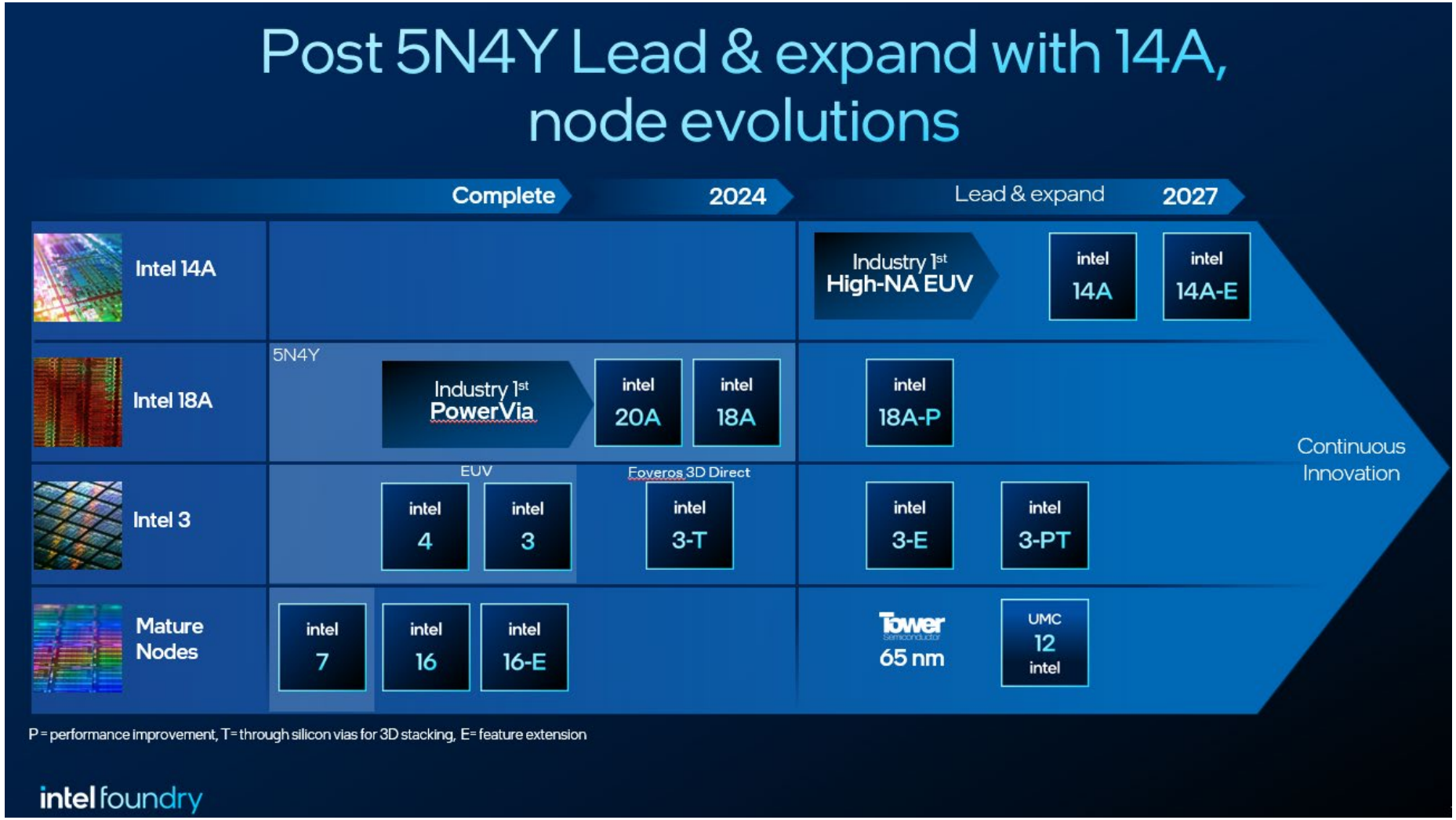


"Intel Foundry will make IDM better and IDM will make Intel Foundry better" – Pat Gelsinger

Intel Foundry Technology Roadmap

RibbonFET & Power Via

Ultimate FinFET node

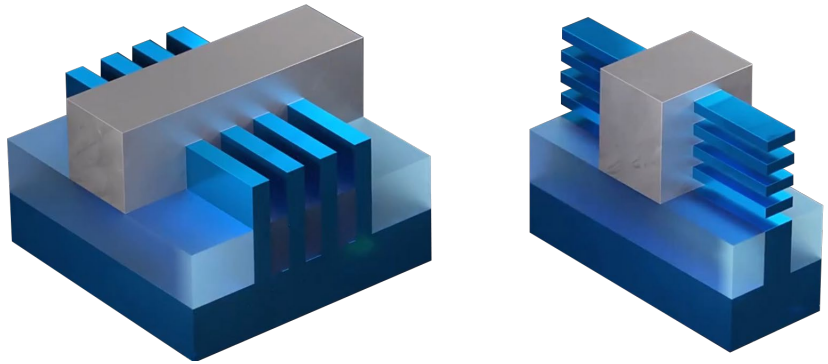


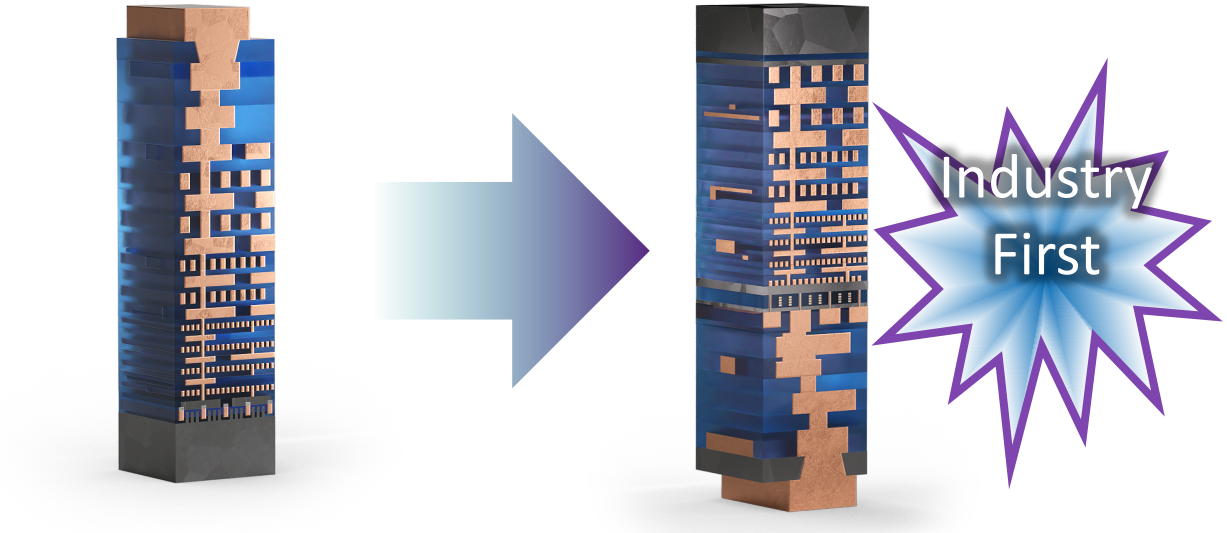
Ribbon FET and Power Via Technologies

Biggest innovations since FinFET in 2011

Angstrom Era Innovations

Ribbon FET Transistors and PowerVia Interconnects





Largest innovation in transistors since Intel introduced FinFETs in 2011.

Better electrostatics compared to FinFETs.

Optimized ribbon architecture for best Perf/W & Vmin.

Largest interconnect innovation since Cu wires in the late 1990s.

Improved density and cell utilization.

Reduced resistive power delivery droop.

EDA tools fully enabled.

Intel 18A market opportunity

Unprecedented levels of performance and density scaling

- Cloud/AI
- HPC
- Cryptography
- Networking
- Accelerators (DPU)

- AP/ModAP
- Modem
- GNSS

- Smart Home/City
- Smart Factory
- Gaming

- Telematics
- Connectivity
- HPC
- eCockpit

- Avionics
- Electronic Warfare
- Satcom/Milcom
- Radar

Breakthrough technology delivering unprecedented levels of performance and density scaling for next gen applications.

Intel Foundry is heavily investing in enabling the full breadth of EDA tools across technology platforms.

Intel Foundry PPA Team

Goals

- Evaluate Intel Foundry offerings from customer experience point of view.
  - Industry standard process design kits (PDK),
  - Block PPA analysis based on an understanding of customer market segment conditions and products,
  - PPA infrastructure that provides max coverage without IDM methods.
- Development of key design flows and features with industry standard tooling.
  - Enable the EDA ecosystem and optimize for Intel Foundry with reference flow development with overrides to open exploration for PPA/DTCO activities.
  - Create end to end flows.
- Implementing and analyzing a wide variety of blocks with node offerings.
  - Understand deltas to customer expectations where applicable.
  - Help co-optimize design and technology to meet customers at their segment.
  - Push PPA, cost, runtime, manufacturability, ease-of-use.

Intel 18A PPA Enhancements and Results

Phase 1 Recap and Phase 2 Summary

Differentiated Intel18A PPA Overall Plan

- Identify key features of technology that can be leveraged best with algorithm updates.

Stage	Categories	Opportunities	Technologies	Phase
Early Analysis	Library Content Analysis	New trade-offs and sensitivity analysis		1, 2
Compile	Logic Synthesis Improvements	New design space with GAA cells	EIO	1
Compile	Cell Selection	Tune cost-based selection/sizing for Intel 18A	EIO	1
Compile/Clock	Congestion/Placer Analysis	Improved routing resource awareness Refined cell and wire density thresholds	Enhanced density	2
Compile/Clock	Layer Assignment/Promotion	Routing density, length sensitivity and resource awareness tuned to 18A.	EWI	1
Route	SI impact Mitigation	Account for no frontside power grid accurately	SI aware track_opt	2
Optimization steps	Cell Selection	Restrict flows applied during optimization steps specific for Intel18A library content	Dynamic restriction	2
All	Timing correlation	Updated ML extraction models for Intel 18A		Open

Differentiated Intel18A PPA Phase 1 Recap

Enhanced Initial Opto (EIO)

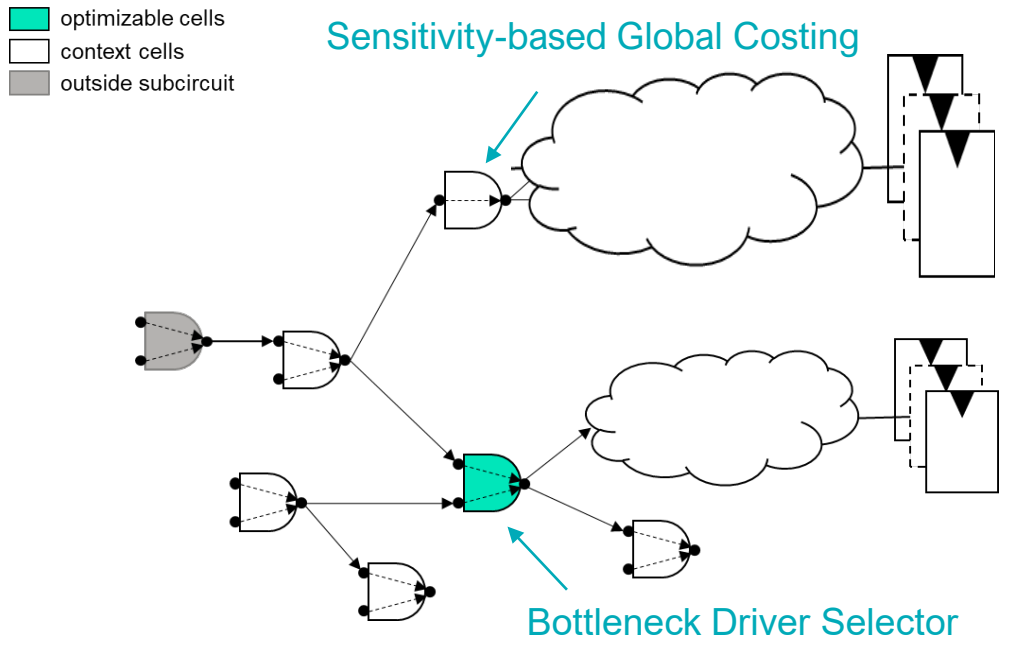
PPA improvement

- bottleneck-based pin selection
- bottleneck-based costing tuned for Intel 18A
- enhanced pre-conditioning sizing engine
- composite costing added to all initial_opto/final_opto delay loops based on library content
- high-effort area-driven restructuring updated for Intel 18A (HET-only)

New cost-based sizing

- Cost all sizes for **delay, slew, area, leakage** and pick the best size based on composite cost. No VT dependency.
- Shows good improvement in area/leakage/timing

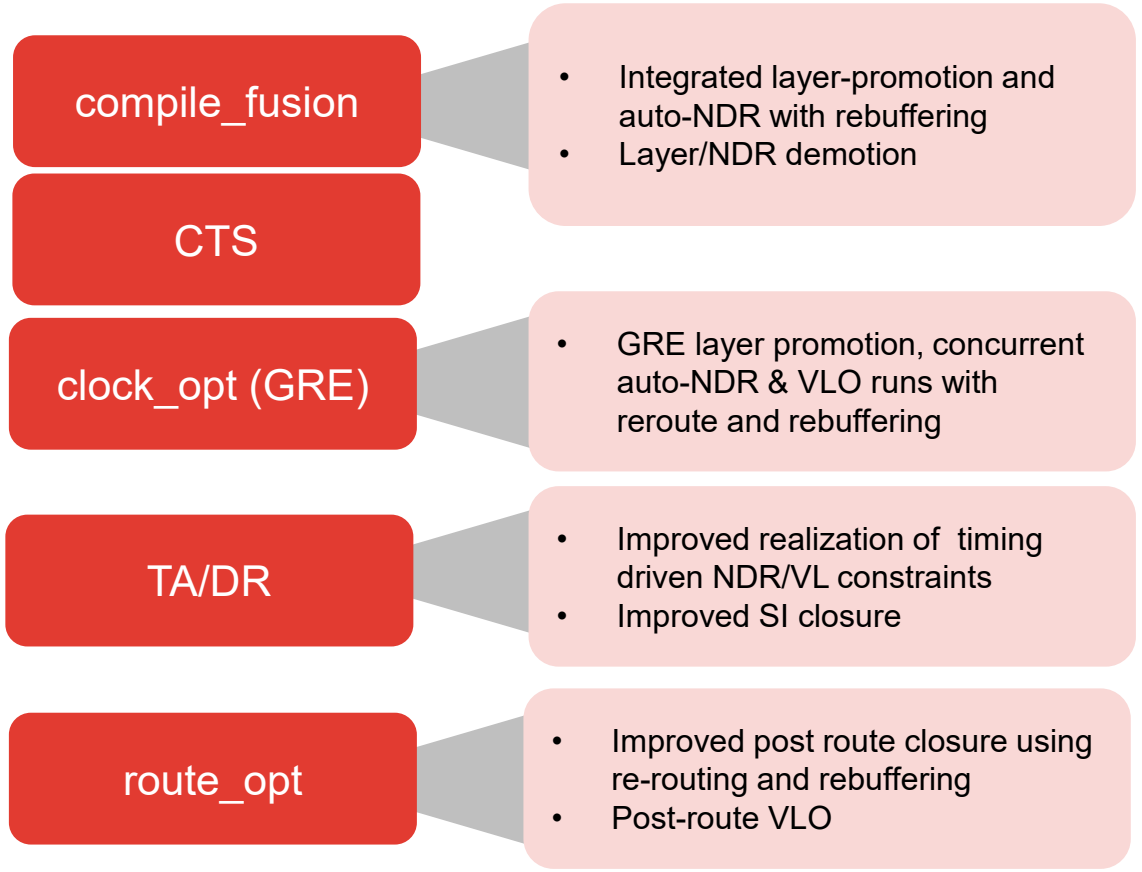
- **Take advantage of richness of Intel 18A cell library content.**



Differentiated Intel18A PPA Phase 1 Recap

Wire Optimization

- Pre-route and routing key improvements
  - Congestion modeling and RDE-GR handshake
  - Realization of NDRs in GR and DR
  - Hybrid GRE Via Ladder (VL) flow
  - Improved GR extraction (ML-GR OBD in 22.03)



- Post-route key improvements
  - NDR through rerouting and rebuffering,
  - New post-route VL optimization (VLO) engine,
  - Timing aware VL implementation in ECO-DR.

- Intel 18A specific binning, congestion and resource remodeling, length tuning, pruning, promotion/demotion, power-aware NDR optimization.

Differentiated Intel18A PPA Phase 1 Recap

ML-GR Extraction for GR/DR Correlation – Retrained for Intel 18A features

- **ML Track Spacing**
  - The track-spacing model depends on layer distribution and local layer density.
  - Denser top layer usage enabled by Intel 18A was not covered in previously available training data.
  - Additional incremental model training with backside PG routing carried out to enhance routing behavior predictability of track spacing.
- **ML Detour**
  - Intel 18A implementations yield different detour and layer variation behavior due to backside PG routing.
  - Detours improve considering extra amount of routing resources for signal routing.
  - Models were updated with additional training to predict the detours in Intel 18A.
- **ML Via**
  - Extra signal resources affects via count on signal routing as well.
  - Pre-trained model updated with additional training to account for these effects.

Differentiated Intel18A PPA Phase 1 Recap

Results

- Differentiated PPA results compared to a PPA-optimized design using reference methodology (RM) flow.

IP	Features	Optimization	D-PPA Improvement
Arm Core Sub-hierarchy	High cell density	Highest frequency	+4.5%
Arm Core Sub-hierarchy	Interconnect dominated	Highest frequency	+4.7%
Graphics	High cell density, low voltage range	Iso-power performance	+4%
RISC-V Core	High performance	Iso-power performance	+4.5%
IDM Block	High crosstalk	Iso-power performance	+4.3%
IDM Block	Interconnect dominated	Iso-power performance	+4.2%

Differentiated Intel18A PPA Phase 2

Auto Density Control Enhanced (ADCe)

❑Retune ADCe for Intel18A with updated default settings for the following:

- Target routing density (TRD)
  - TRD is a route density threshold for congestion hot spots.
  - Default settings tuned for technologies with frontside PG. Default values improve without hurting routability in Intel18A.
  - Monitored effect on post-route SI while increasing route density.
  - Intel 18A enables less expansion considering the extra signal resources advantage.
  - Both timing and power improve.
- Max density and congestion response
  - Changed the way cell density responds to congested areas in a design.
  - Intel 18A can tolerate higher densities when backside PG is considered.
  - Tuned algorithm with awareness of sizing/buffering requirements while pushing cell density.
  - A higher density can improve wirelength, which helps both timing and power.

Differentiated Intel18A PPA Phase 2

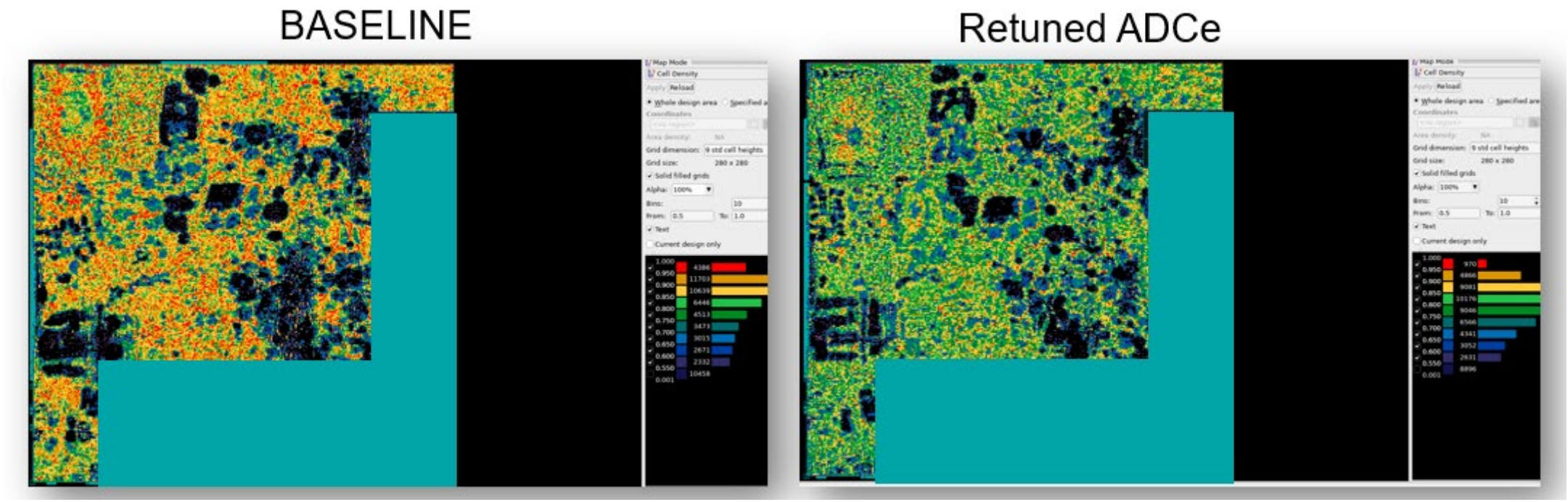
Auto Density Control Enhanced (ADCe)

- Intel 18A BS power enables an opportunity to pack more cells together before any convergence issues arise in timing or routability.
- Opportunity to retune ADCe for Intel18A with updated default density settings:
  - Target routing density (TRD) for congestion estimation and cell expansion
    - TRD is a route density threshold for congestion hot spots.
    - Default settings tuned for technologies with frontside PG.
    - Careful monitoring of the impact on post-route SI critical while increasing route density.
    - Intel 18A enables less expansion considering the extra signal resources advantage.
    - Both timing and power improve.
  - Cell density and layer specific congestion response optimization
    - Changed the way cell density responds to congested areas in a design for Intel 18A layer stack.
    - Intel 18A can tolerate higher densities when backside PG is considered.
    - Tuned algorithm with awareness of sizing/buffering requirements while pushing cell density.
    - A higher density can improve wirelength, which helps both timing and power.

Differentiated Intel18A PPA Phase 2

Auto Density Control Enhanced (ADCe)

- Efficient distribution of density demonstrating reduced >90% density areas at iso-block area.
  - Better handling of 80-90% density area improves overall resource usage and improves PPA.
  - Enables area reduction.



Differentiated Intel18A PPA Phase 2

Cell Selection Updates – Restrict flow

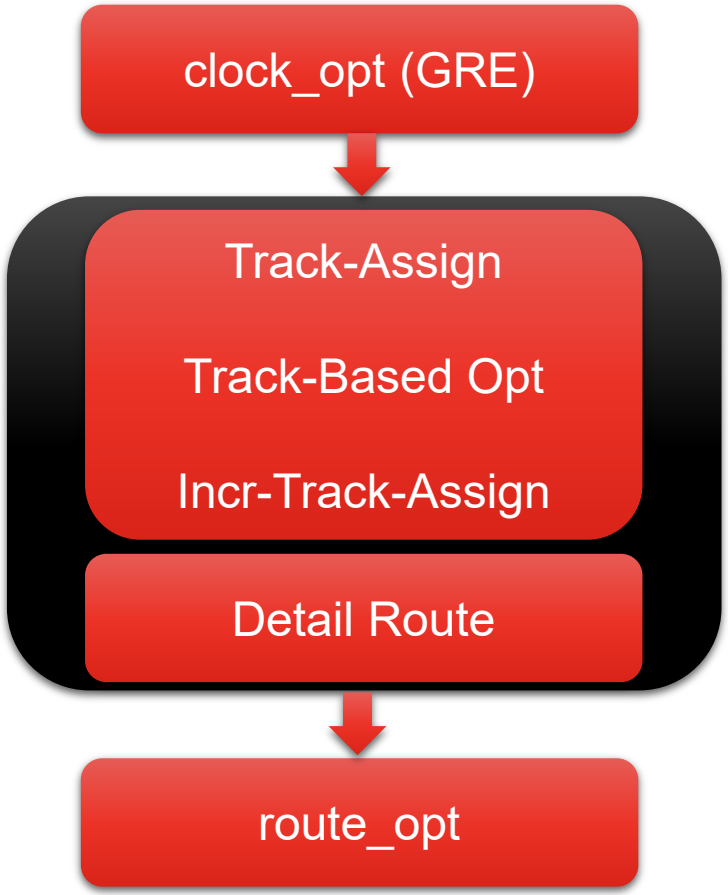
- The restrict flow contains several improvements during optimization:
  - Classification of equivalent lib cells based on power characteristics into multiple sets.
  - Dynamically restrict high power lib cells during certain optimization steps based on these sets.
  - Controlled power thresholds when optimizing area.
  - Library cell groups are tuned to accommodate the richness of the Intel18A library content.

- Restrictions are removed in certain phases and delay optimization steps:
  - In route-opt, after first pass/phase, remove any restrictions.
  - Add a non restricted delay pass in each delay step.

Differentiated Intel18A PPA Phase 2

Enhanced SI optimization for BS PG

- Additional track availability with Intel18A provides more opportunities for SI aware optimization engines to make changes to design before route_opt.
- New SI closure flow using track-based SI optimization.
  - TR to DR handshake improvement in SI awareness.
  - Enhanced SI prevention during track assignment/detail route.
  - Leverage track-based optimization to clean-up easy delta delay nets.
  - Improved delta-delay distribution allow better SI closure in route_opt.
  - Allow track/detail route to focus on harder to fix delta delay nets.



Differentiated Intel18A PPA Phase 2

Results

IP	Features	Optimization	D-PPA Improvement
Arm Core Sub-hierarchy	Crosstalk driven	Iso-power performance Iso-frequency power	+3% -7% -2% util at iso-area
Arm Core Sub-hierarchy	Interconnect dominated	Iso-power performance Iso-frequency power	+2% -5% -1% util at iso-area
Graphics	High cell density, low voltage range	Iso-power performance Iso-frequency power	+4% -10% -3% util at iso-area

Differentiated Intel 18A PPA

Future Development

Categories	Opportunities/Potential Challenges	Technologies
Library cell selection	The design space enabled by the rich Intel 18A content has room to squeeze more PPA	Dynamic cell filtering
Spacing aware full flow solution	Utilize Intel18A library content more efficiently Reduce any legalization displacements	CLO, legal_opt
Layer assignment and promotion	Tune algorithms for Intel18A stack with detailed RC profile analysis	
SI Mitigation	Improved SI awareness earlier in flow for improved PPA	Early GR for SI awareness tuned to Intel 18A route resources
Timing correlation	Layer resource handling with backside PG still has room to squeeze more PPA with better correlation	MLGR new proposal for Intel18A

Conclusions

Conclusions

- Intel 18A Ribbon FET and Power Via technologies open a new design space that needs to be navigated efficiently through early EDA engagement.
- Intel Foundry is heavily investing in enabling full breadth of EDA tools for customers to achieve the best PPA with its technology offerings out of the box.
- Intel 18A specific feature development and tuning in Fusion Compiler yielded differentiated PPA results across a variety of benchmark blocks.
- Phase 1 results we summarized, and Phase 2 results were demonstrated.
- Future phases of developing differentiated technology will work to push the boundaries even further.


THANK YOU
YOUR
INNOVATION
YOUR
COMMUNITY