Revamping SoC Design with RTL Architect and NoC Innovations

Frank Schirrmeister, VP Solutions & Business Development
Arteris

Arteris – A Leading SoC System IP Company

ARTERIS IP snug

Global customer base deploying Arteris interconnect IP and SoC Integration Software

- Silicon-proven IP used in ~3.5 billion+ SoCs shipped to date
- 200+ customers and 725+ SoC design starts to date
- 70-80% market share of automotive ADAS SoC market[1]
- Strong presence in Artificial Intelligence/Machine Learning (AI/ML) system IP
- Broad interoperability - any processor, any IP, any EDA, any foundry
- Innovative technology coupled with expert support results in a 90+% customer retention rate
- 71 patents and 77 patent applications (As of July 31, 2023)
- ISO 9001:2015 Quality Management System (QMS) Certified

Source: Arteris Q4'23 Earnings Call, [1] Management estimates

Diversified Customer Base

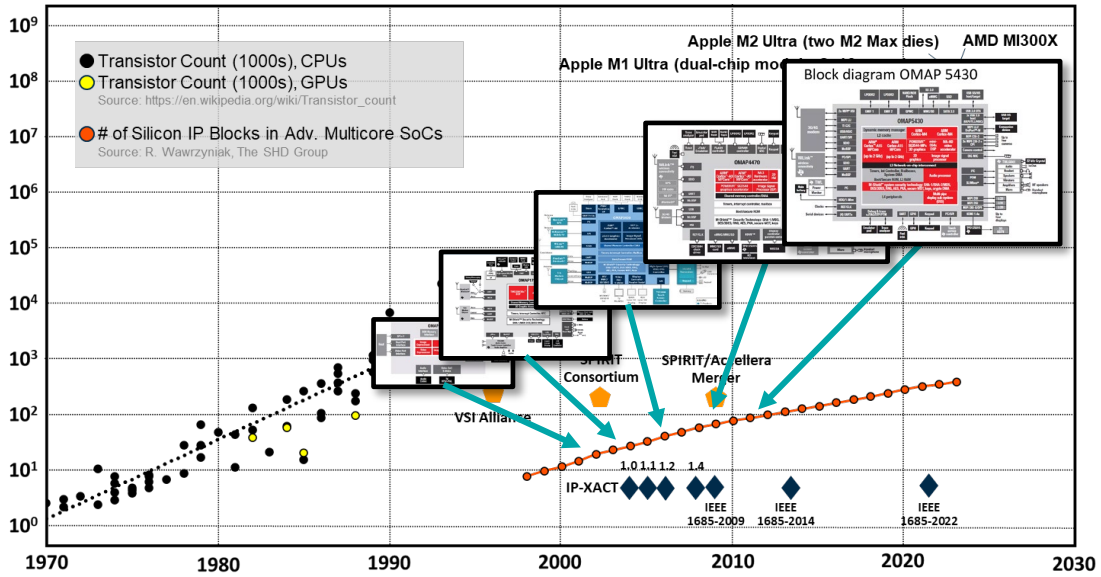
Subset of Publicly Disclosed Customers

Challenges

Challenges with Traditional Flow

Semiconductor Complexity, SoC Integration and Networks-on-Chips(NoCs)

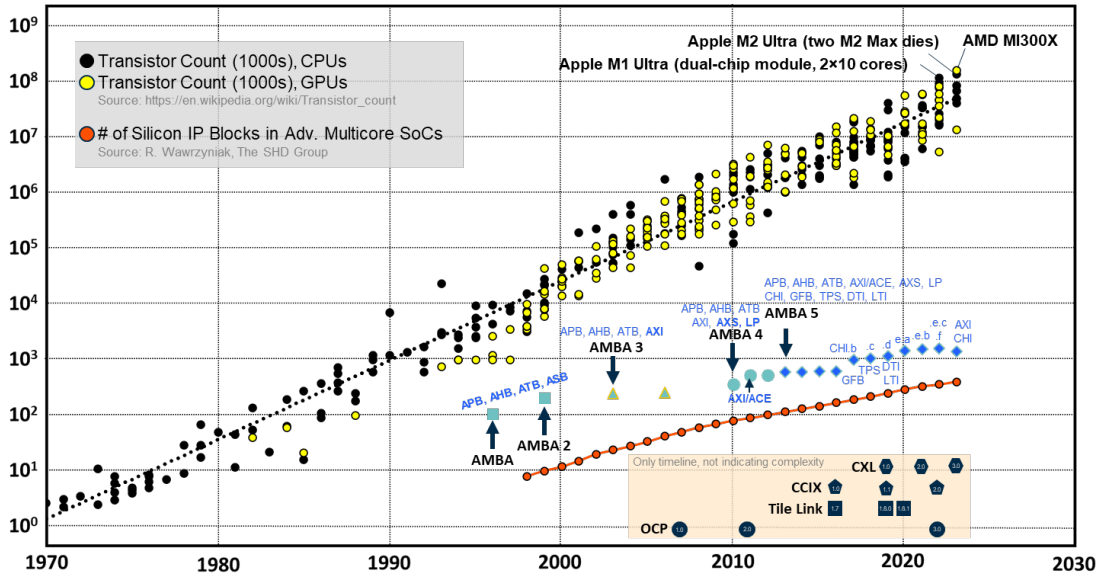
Growing SoC Integration Complexity



Source: Frank Schirrmeister, Arteris, plotted based on https://bit.ly/3P5y9OK, The SHD Group, Public Press Releases

- # of IP Blocks in SoC has grown from 10s to 100s
- Disaggregation offers design version variety
- Standards like IP-XACT need to extend too

Growing Network-on-Chip Complexity



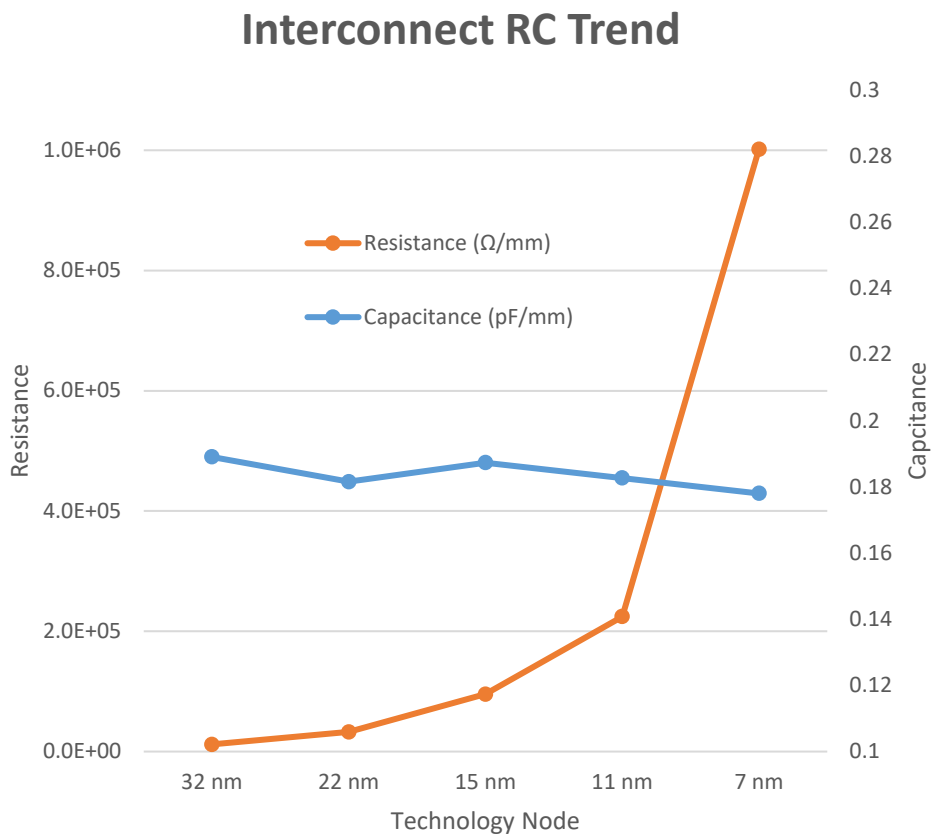
Source: Frank Schirrmeister, Arteris, plotted based on https://bit.ly/3P5y9OK, The SHD Group, Public Protocol Specs

- Complexity of NoC protocols have grown 10x (# of pages)
- Variety of NoC protocols has grown
- NoCs evolve into Super-NoCs when split across chiplets

.

Interconnect Timing Design Challenges

- No standard methodology for **timing closure** for on-chip IP communications
- Process node advances **add to RC delays for long, cross-chip distances** traveled
- Interconnects that connect different IP blocks span **long distances** and hence **suffer from RC delays**



Interface-Layer Effects and Grain Scattering Impact Resistance Scaling

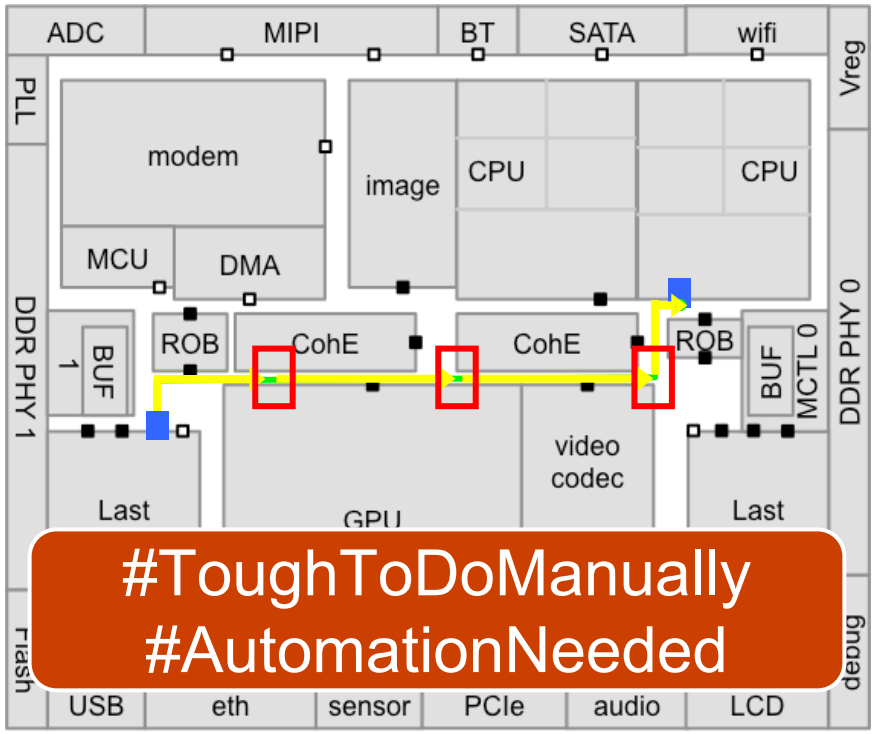
Source: Serkan Kincal, et al., "RC Performance Evaluation of Interconnect Architecture Options Beyond the 10-nm Logic Node," IEEE (2014)

SoC Timing Issues

Can’t Cross Advanced Node SoCs in One Clock Cycle

Physical distance impacts the number of pipeline stages

Clock Cycles



Endpoint (NIU)

Single NoC cycle path

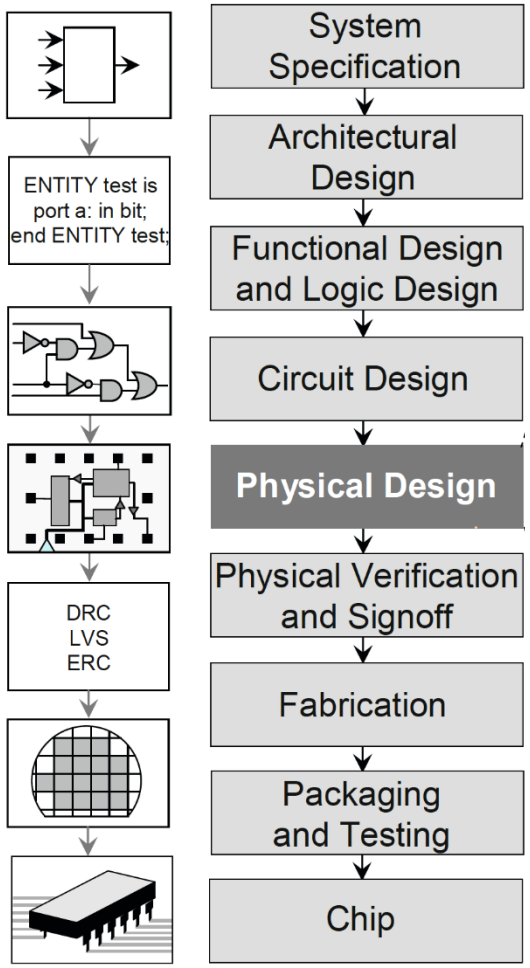
Pipeline

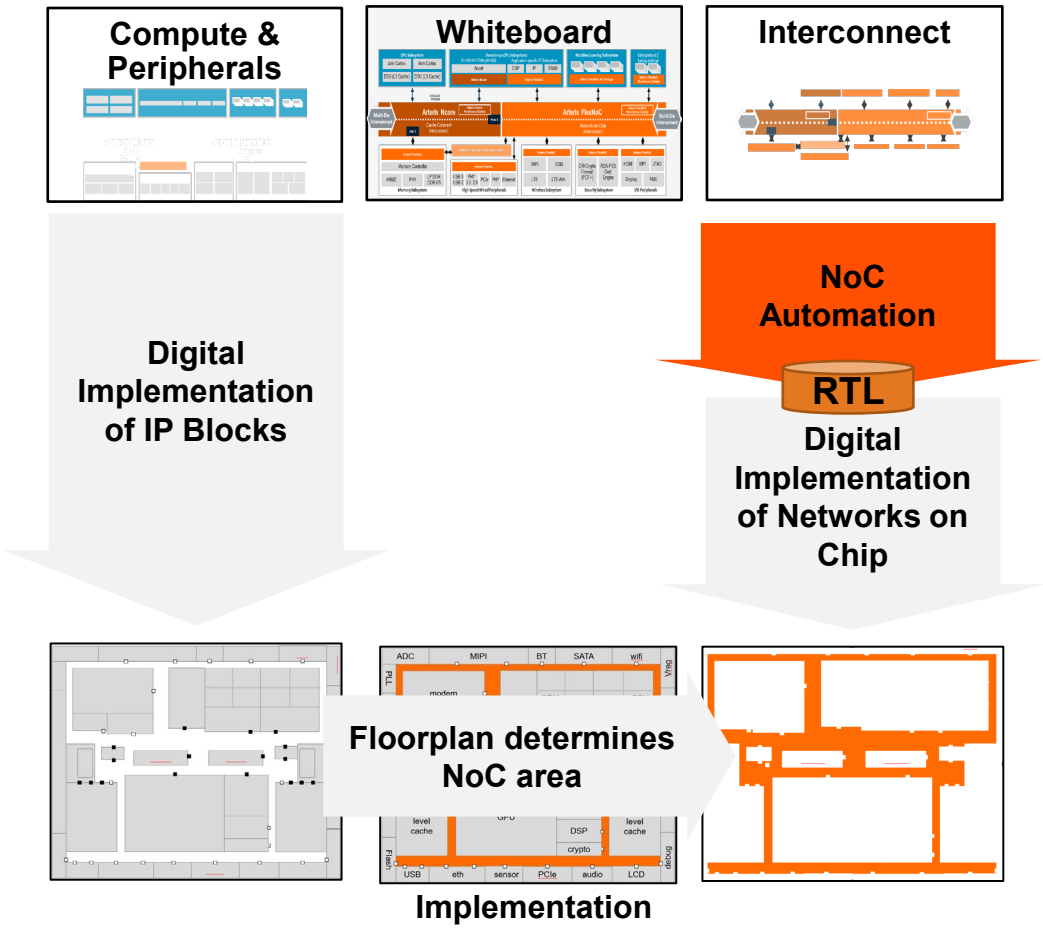
Transport delay = F (foundry, routing stack, type of driving cell, process voltage, temperature, …)

The EDA Flow & NoC Design

Customer uses Arteris tools to design the Network on Chip (NoC)

Customer uses Synopsys tools to implement from RTL to GDSII





EDA flow diagram source: Andrew B. Kahng, et al., "VLSI Physical Design: From Graph Partitioning to Timing Closure," Springer (2011)

The EDA Flow & NoC Design

ARTERIS IP

snug

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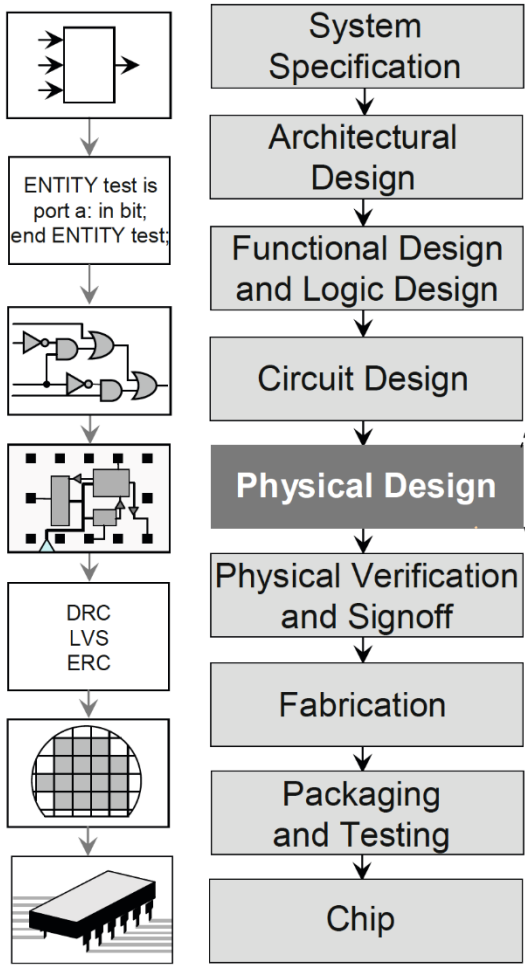
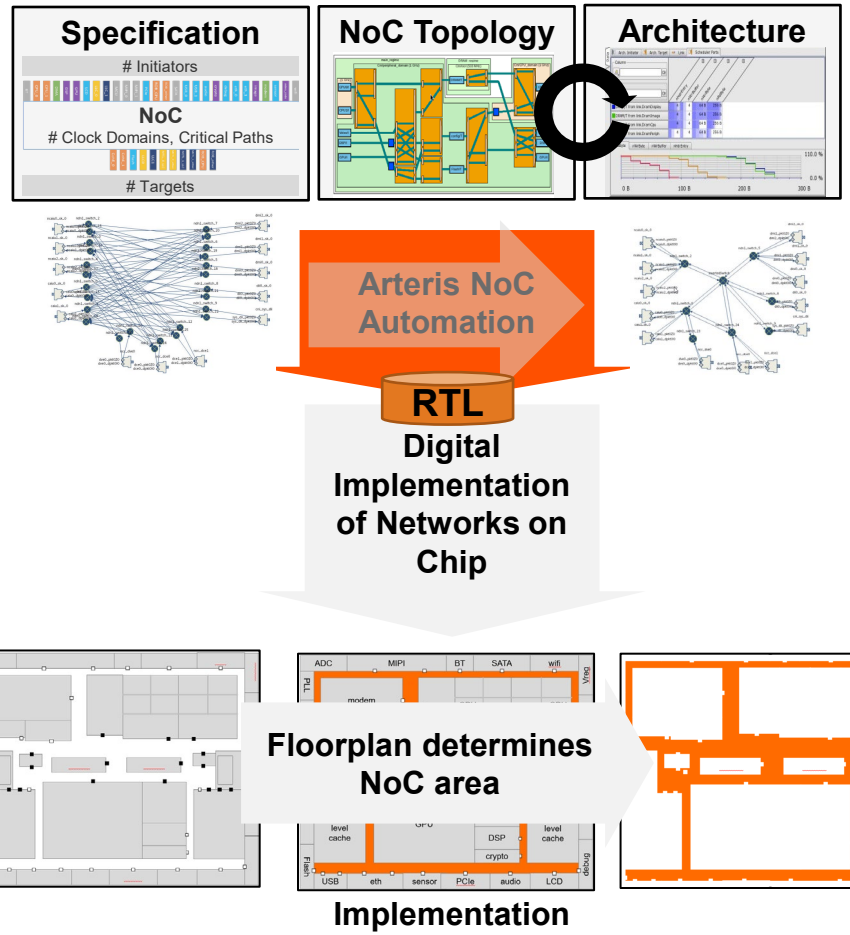


SNPS Platform Architect



EDA flow diagram source: Andrew B. Kahng, et al., "VLSI Physical Design: From Graph Partitioning to Timing Closure," Springer (2011)

The EDA Flow & NoC Design

ARTERIS IP

snug

Time per iteration

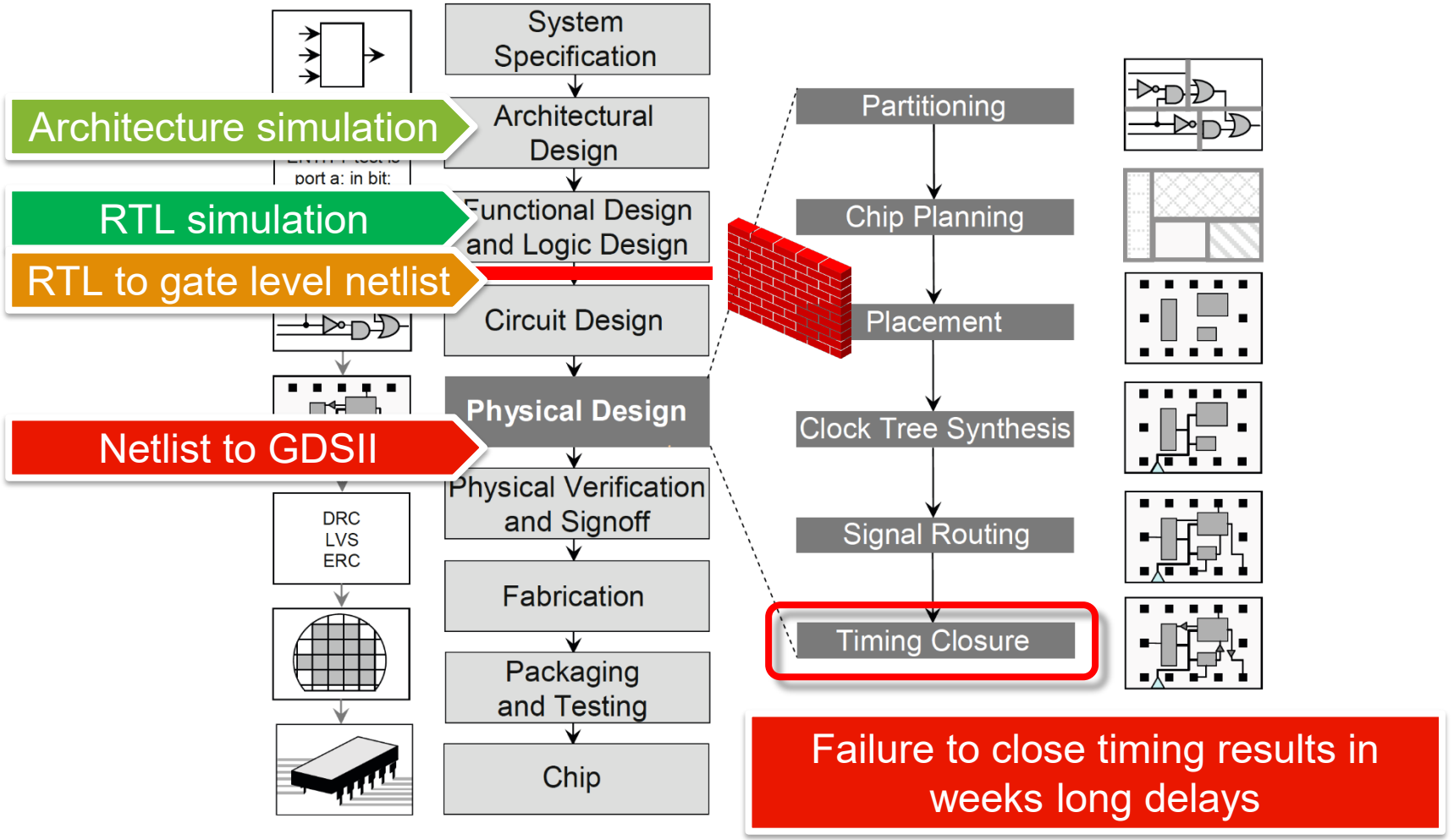
Minutes to Hours

10x

Hours to Days

Days

Weeks



EDA flow diagram source: Andrew B. Kahng, et al., "VLSI Physical Design: From Graph Partitioning to Timing Closure," Springer (2011)

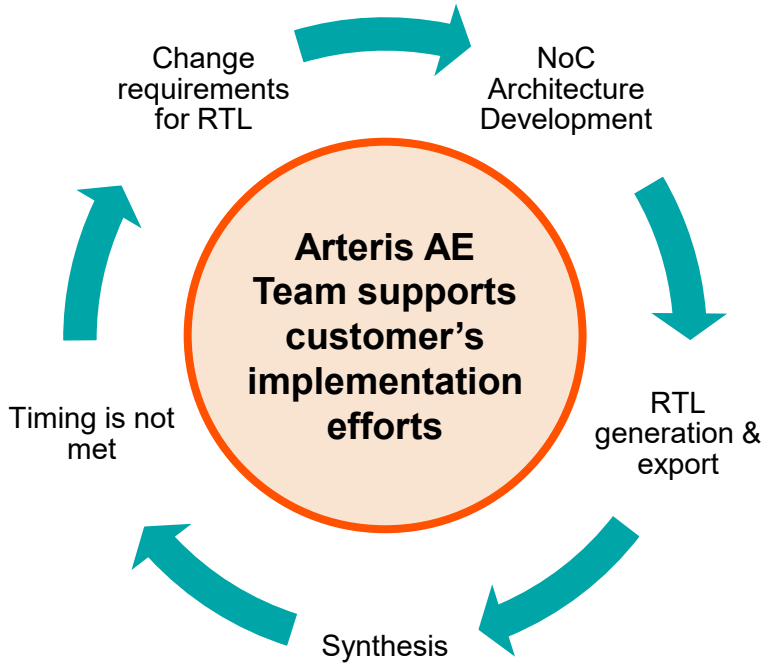
The Customer PPA Struggle

NoC RTL is different for every refinement

Customer uses Arteris tools to design the Network on Chip (NoC)

RTL

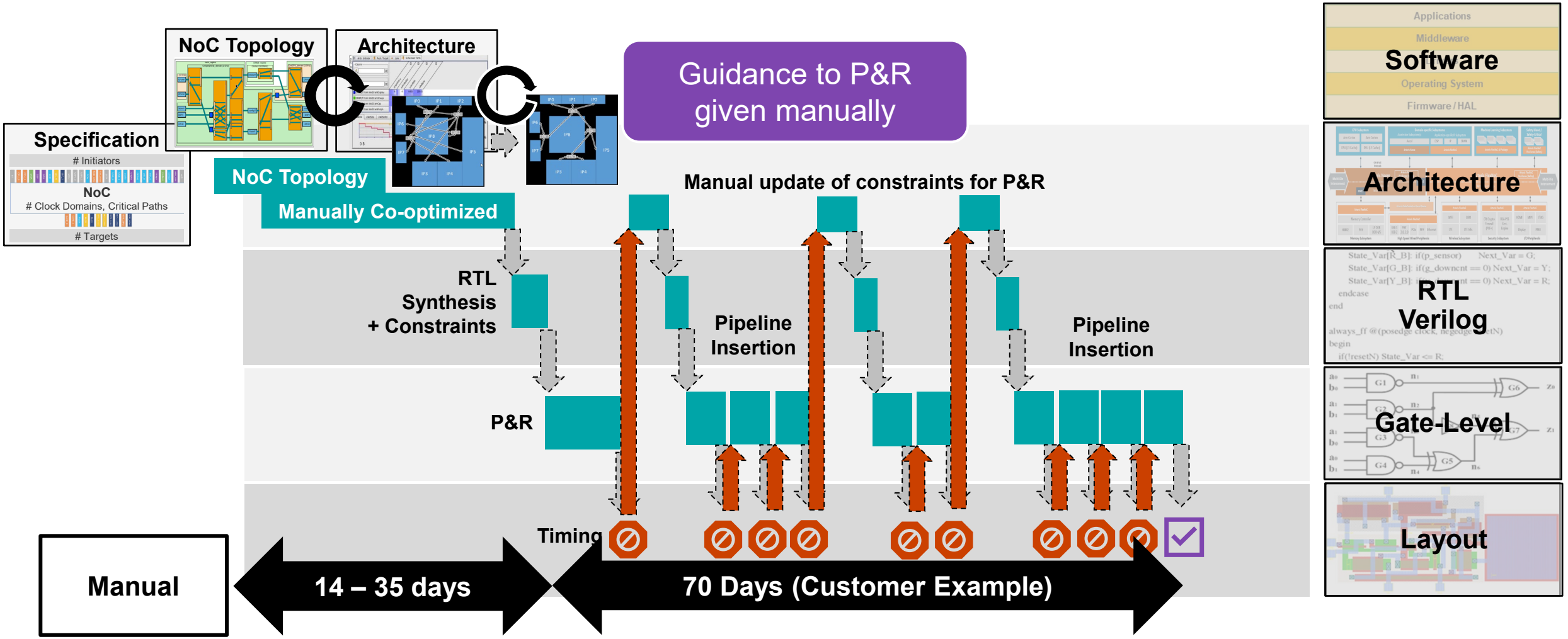
Customer uses Synopsys tools to implement from RTL to GDSII



EDA flow diagram source: Andrew B. Kahng, et al., "VLSI Physical Design: From Graph Partitioning to Timing Closure," Springer (2011)

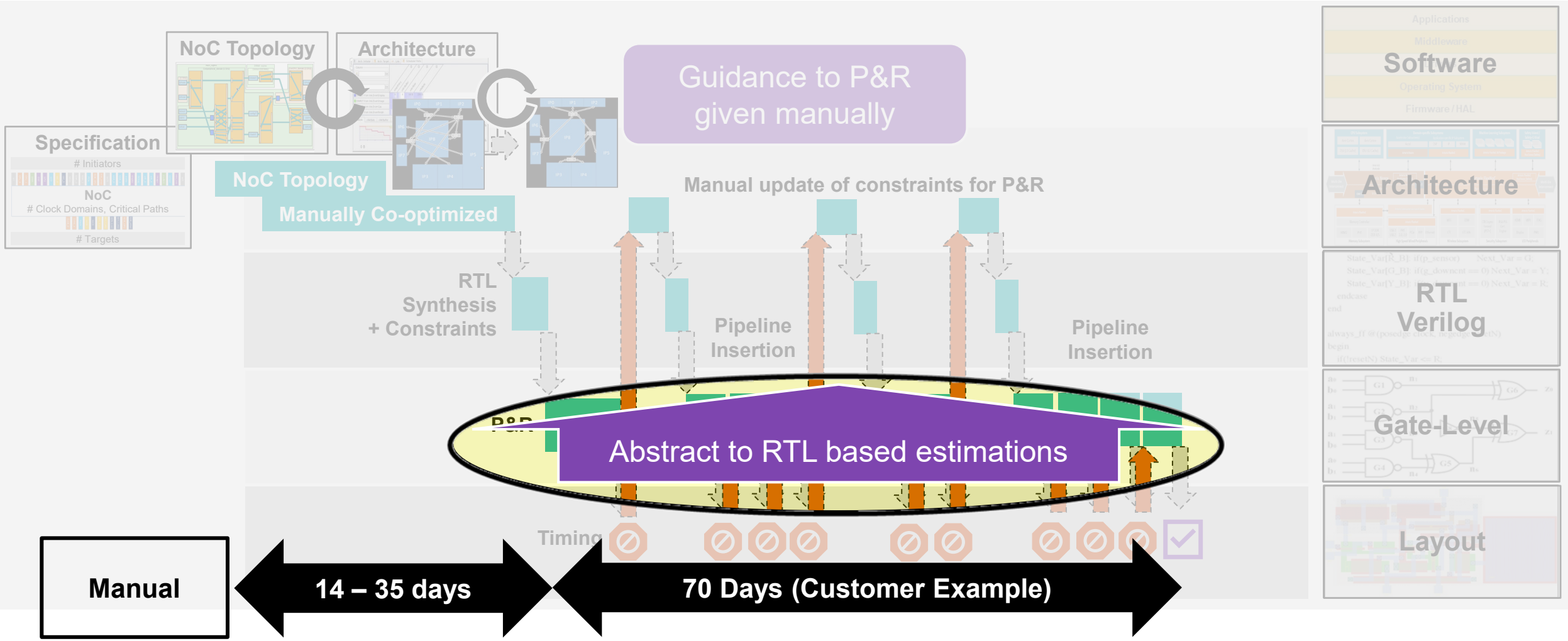
A Customer Example

Manual Flow With Some Layout Awareness & Guidance



Automation Opportunities

Abstract estimations of interconnect delay after layout

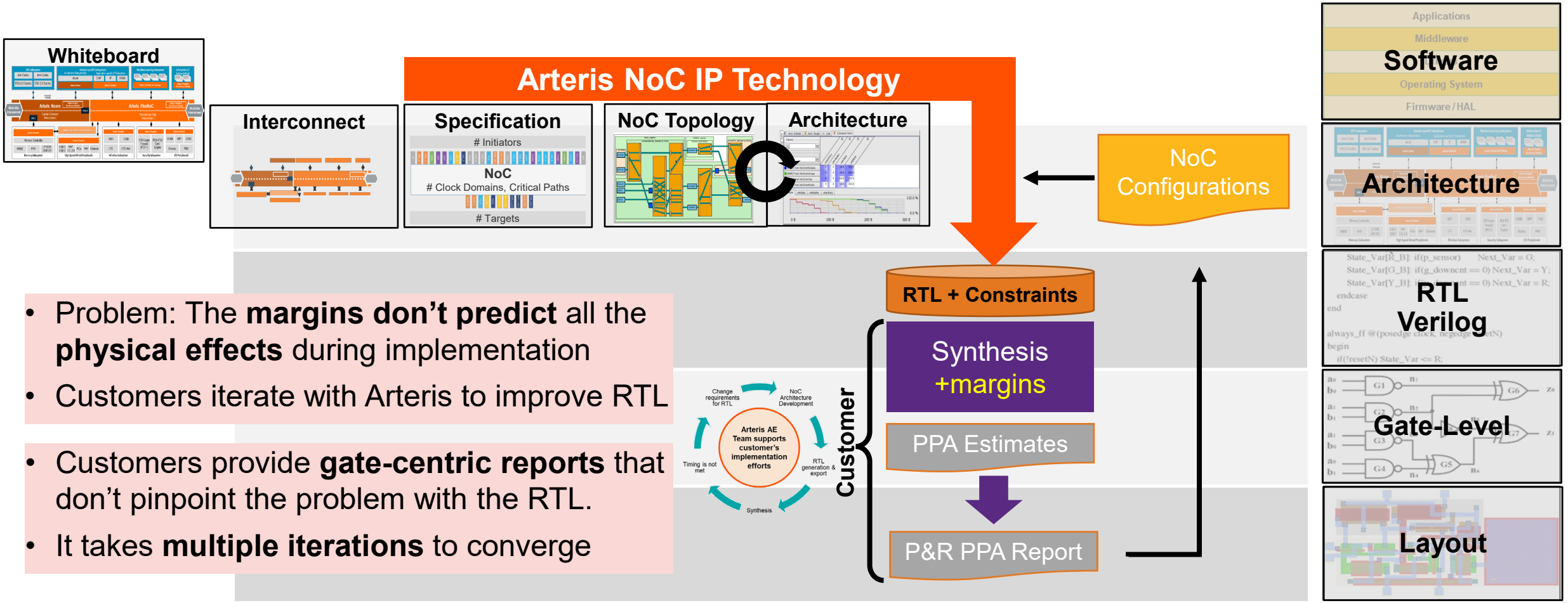


Physical Exploration with RTL Architect

Limitations of the Existing Flow

Traditional Flow

Slow to converge with many customer iterations

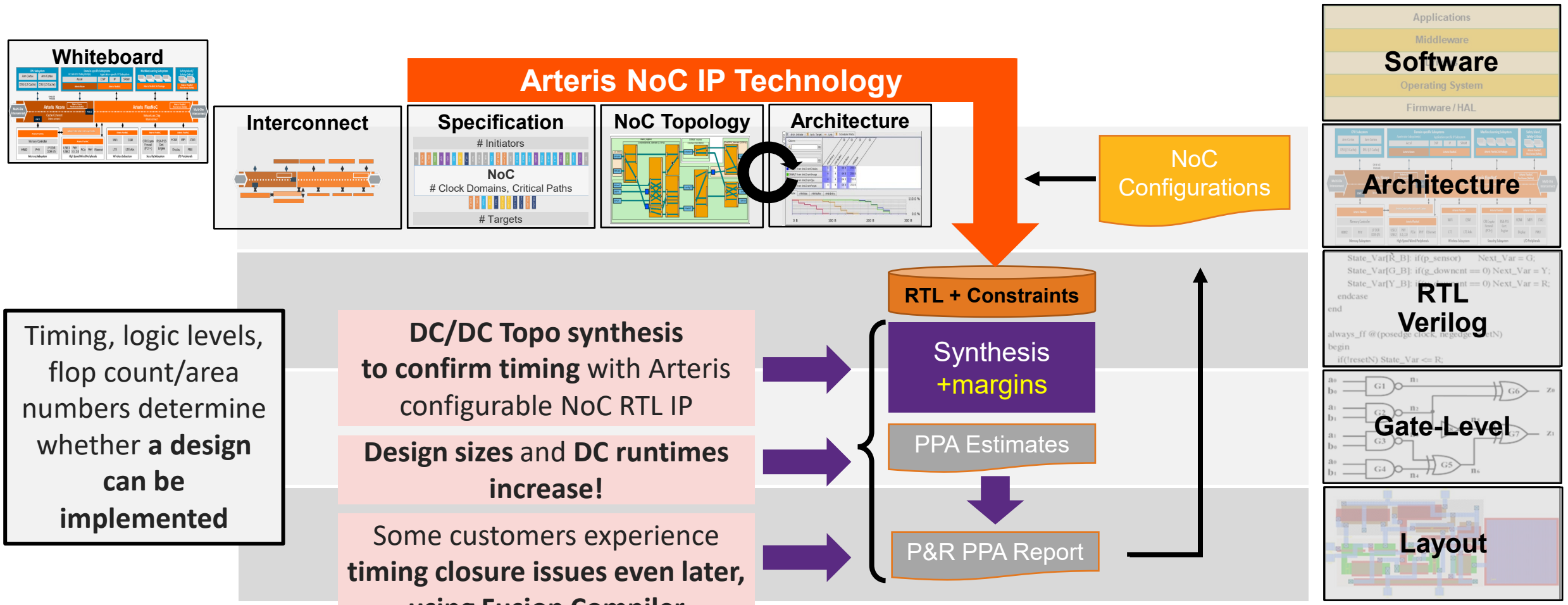


- Problem: The **margins don't predict** all the **physical effects** during implementation
- Customers iterate with Arteris to improve RTL

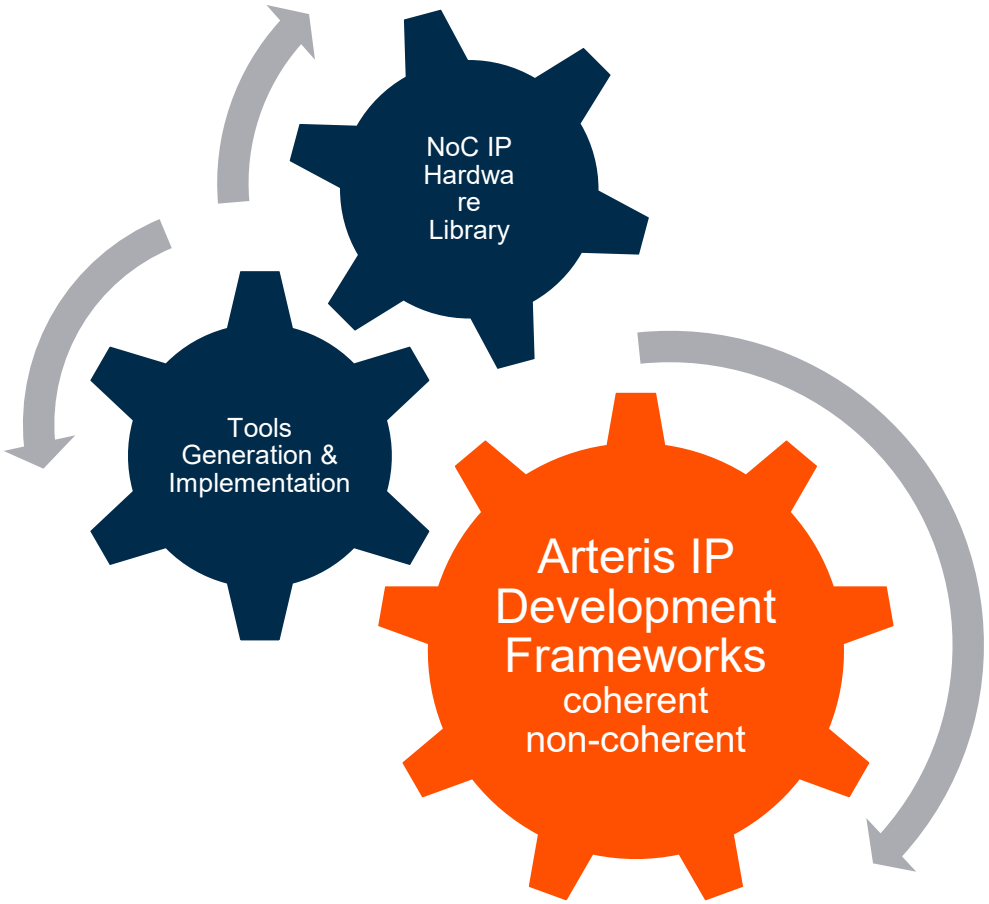
- Customers provide **gate-centric reports** that don't pinpoint the problem with the RTL.
- It takes **multiple iterations** to converge

Traditional Flow

Slow to converge with many customer iterations



NoC IP Development Frameworks



NoC Interconnect IP Hardware Library
Protocol converters, switches, rate adaptors, etc

Tools Generation & Implementation
Generation of Implementation RTL, Collaterals
Links to EDA Implementation

Tools Architecture & Validation
Testbench creation
SystemC models for performance analysis

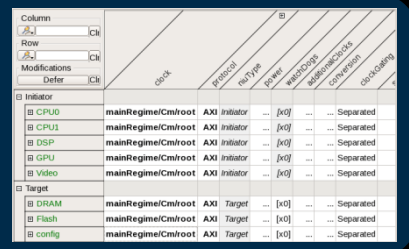
Modular Tool Library

Category	Library units
Network Interface Units	**ACE-Lite, AXI, AHB, APB, PIF, OCP, others**
Transport	mux, demux, serializer, buffer
Domain adapter	clock, power, voltage
Timing	pipeline stage
QoS	bandwidth limiter/regulator
Security	user defined firewalls
Probes	error, statistics, trace
Interchip link	PSI
Resilience/Safety	timeout, safety controller, checkers

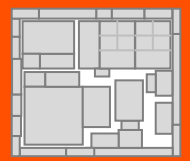
Tool Flow

Inputs
Specification
Socket specifications
Floorplan outline
LEF/DEF
Visio
Perf Analysis
Traffic Scenarios
P&R
Timing Reports

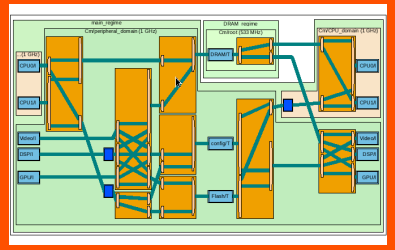
Specification



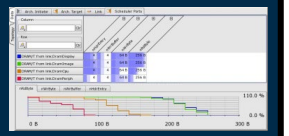
Physical Awareness & Architecture
auto pipe, placement



switch topology
QoS, buffers
serialization

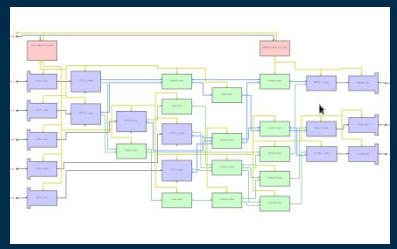


Performance Analysis
use case based performance



Outputs
Structure
RTL
SystemC
IP-XACT
Scripts / constraints
Gate Estimates
Verification testbenches

Structure

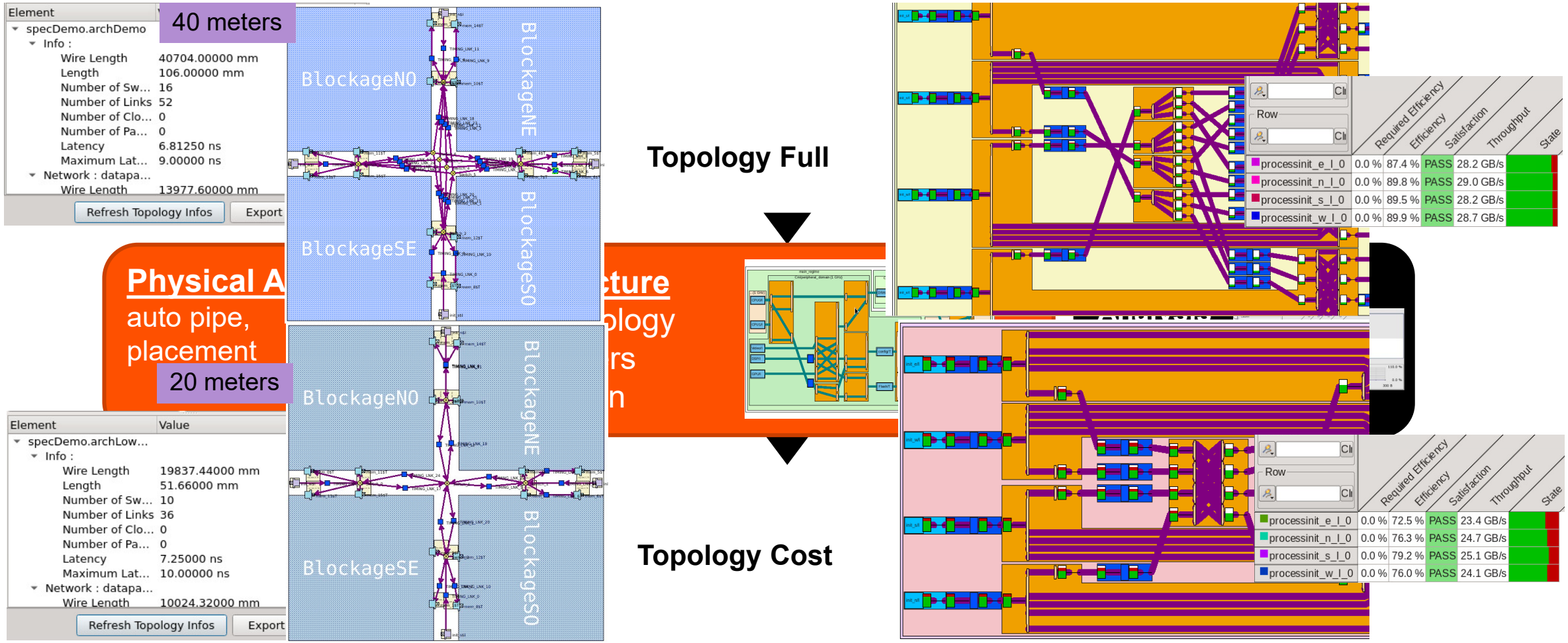


Timing reports

P&R ← Synthesis

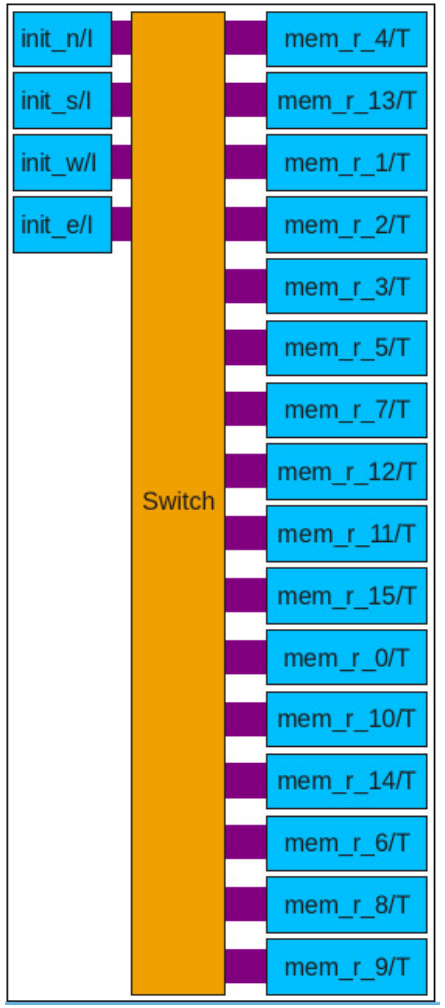
Architecture Refinements

Physical and Performance Co-design

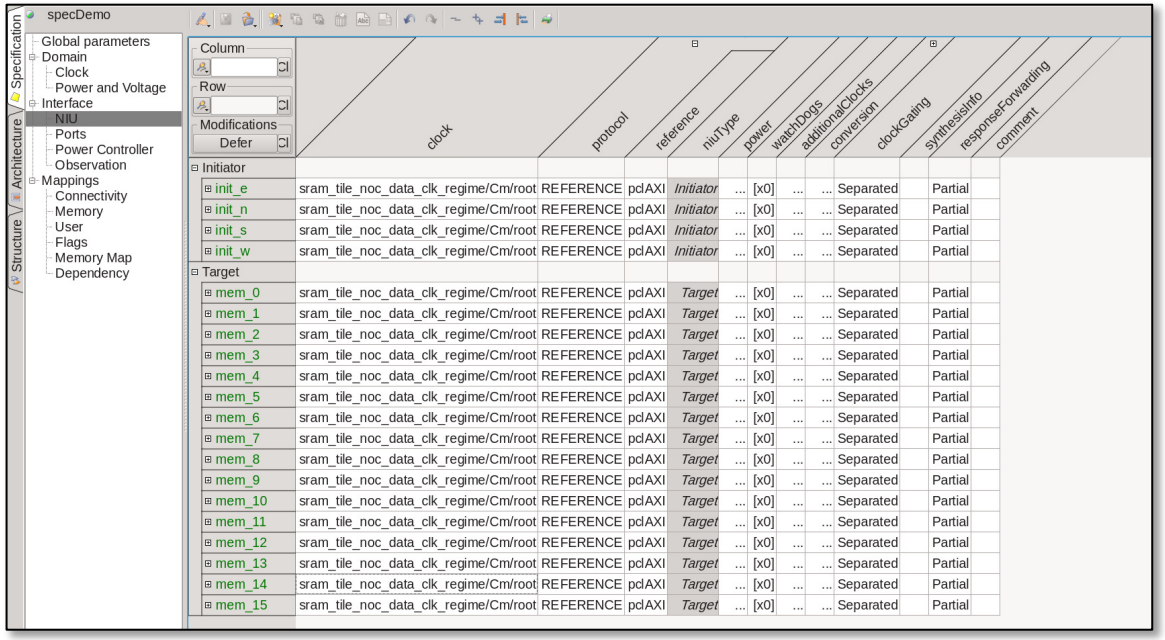


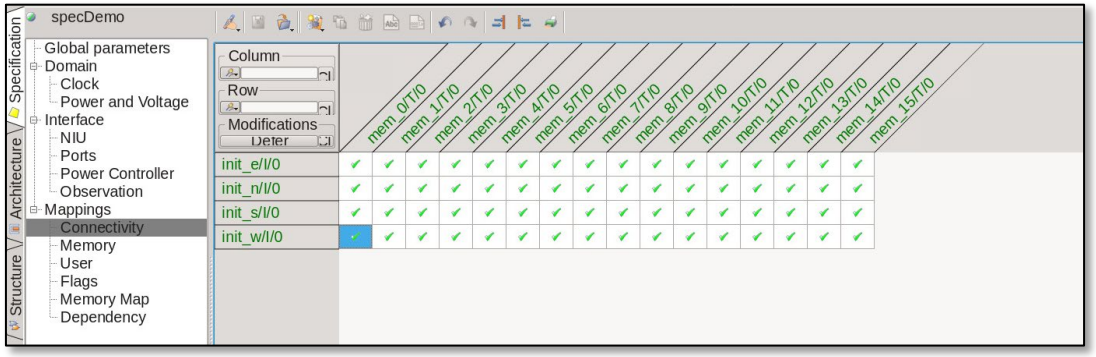
Signal Processing Design Example

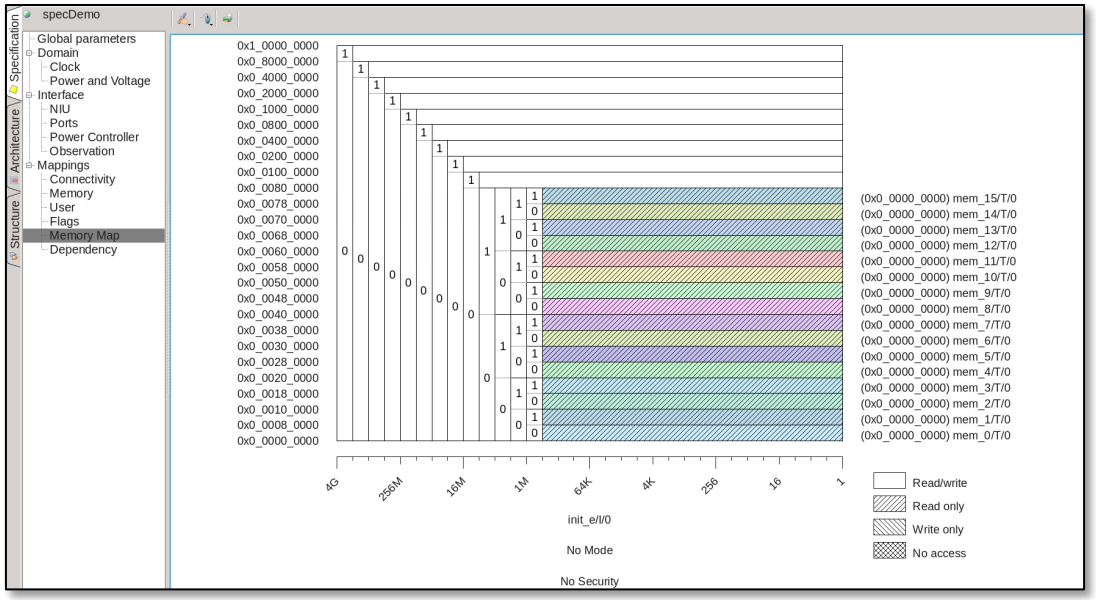
- Use case: Signal processing as part of a larger Communications SoC.
- The design includes x4 DMAs that need to access ‘scratchpad’ SRAMs.
- A crossbar approach is a good starting point.



Specifiy Network Interface Units, Connectivity and Address Maps





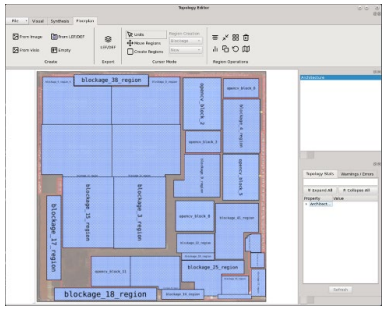


Consider Floorplan Early

EARLY stage:

Image

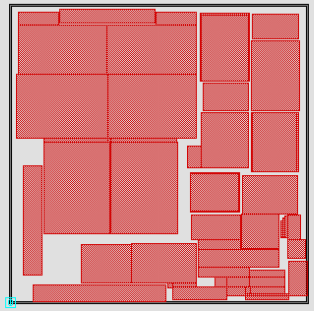
Import



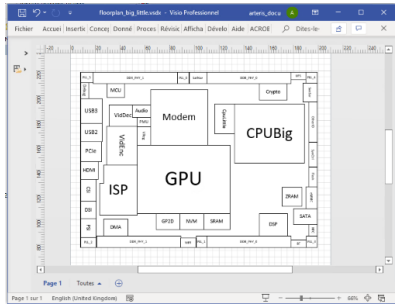
file
Tcl

Export

LEF/DEF



Visio



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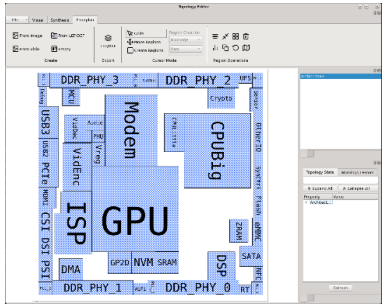

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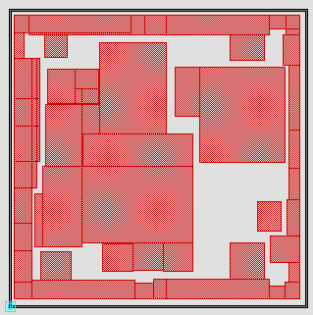
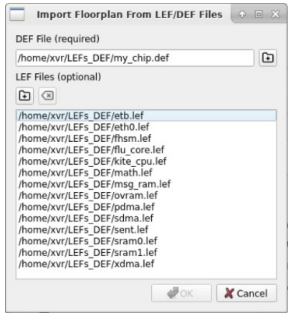


LATER stage:

LEF/DEF



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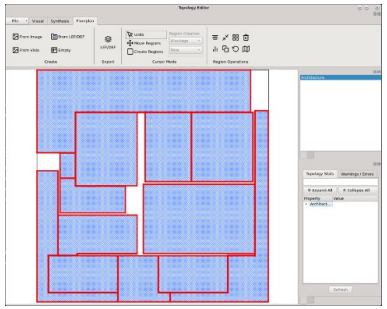

file
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Export

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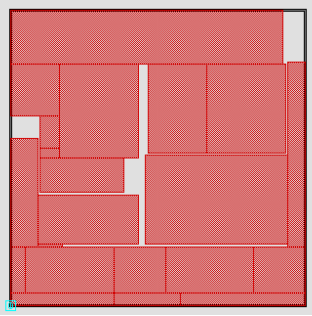
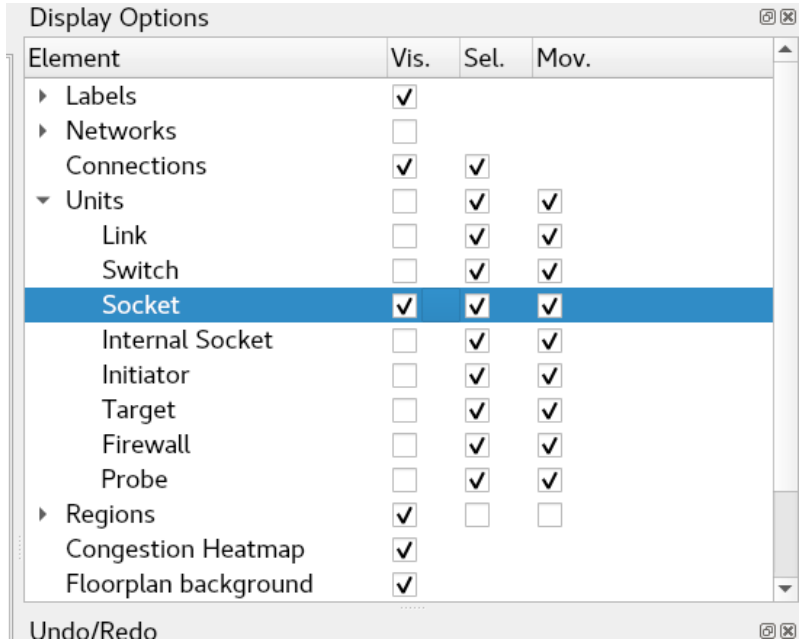
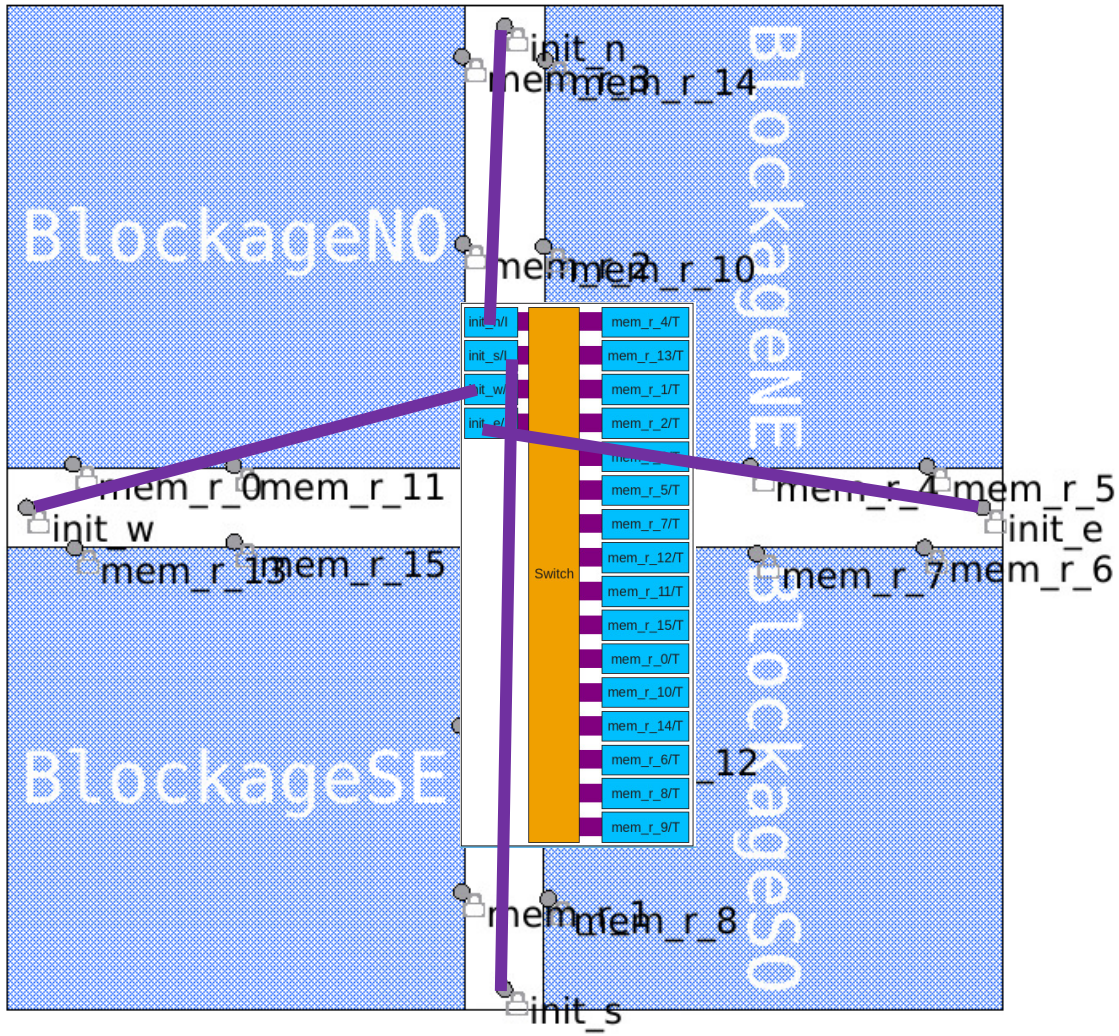


Example Case

Physical Socket Placement

- Initial constraints
  - Blockages on Floorplan View
  - Socket Positions

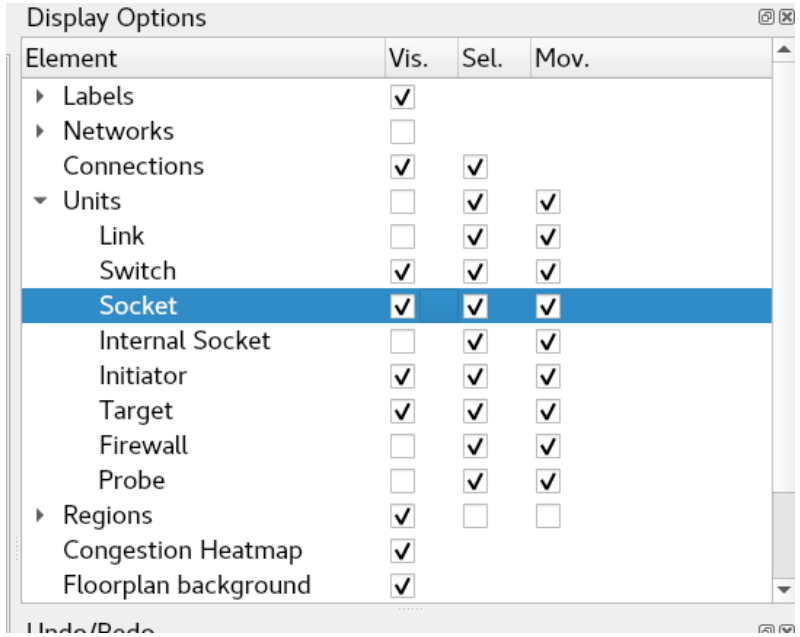


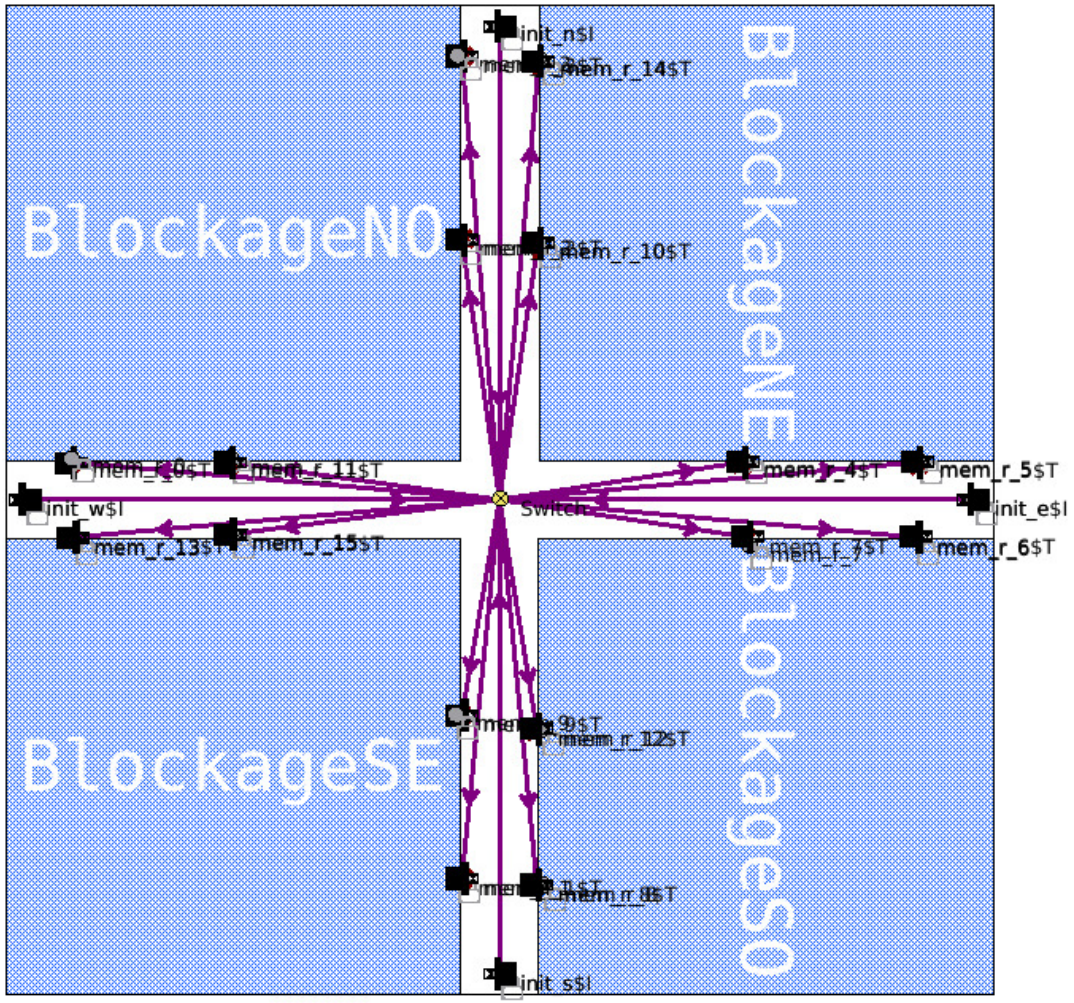


Example Case

Initial Crossbar Design

- Place the initial topology
  - Automated starting point
  - Note the possible central congestion issue

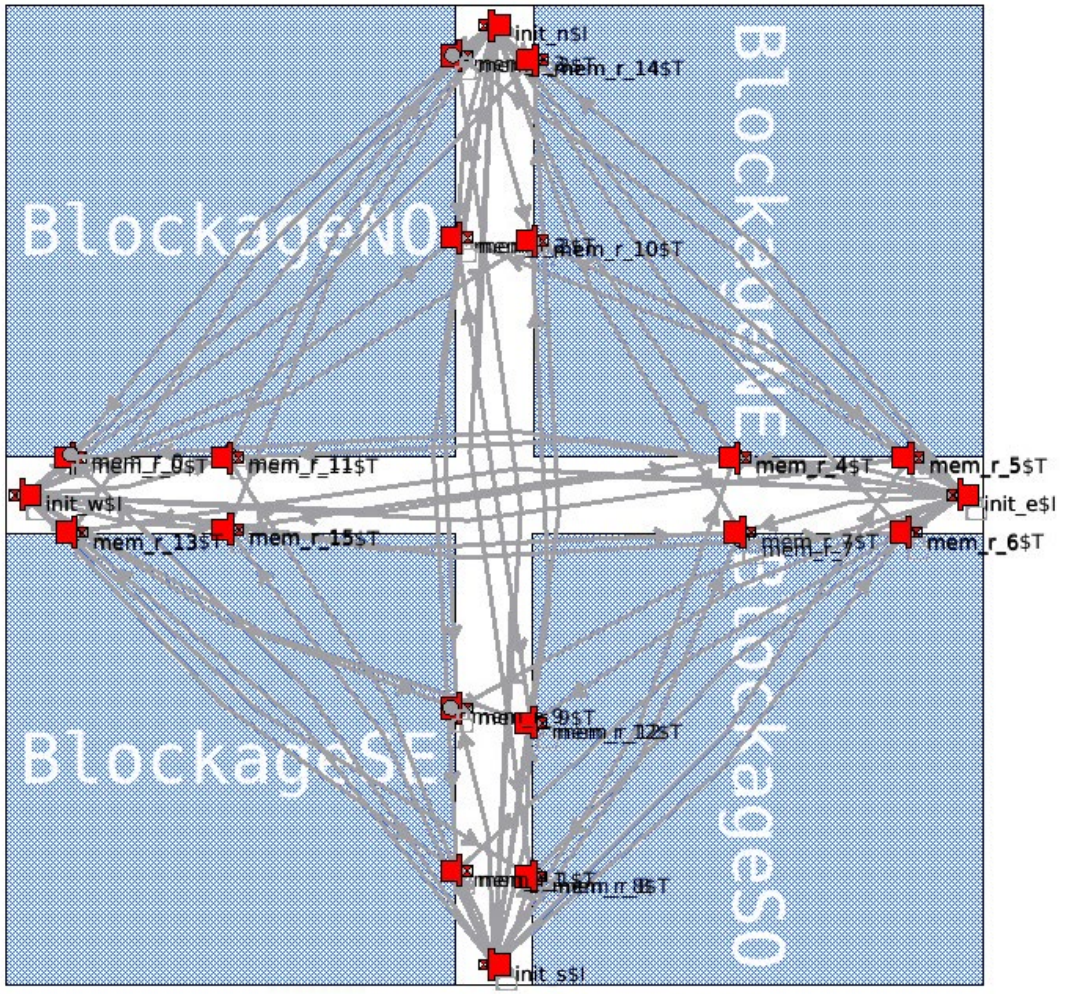




Example Case

Considering Options – Step 1

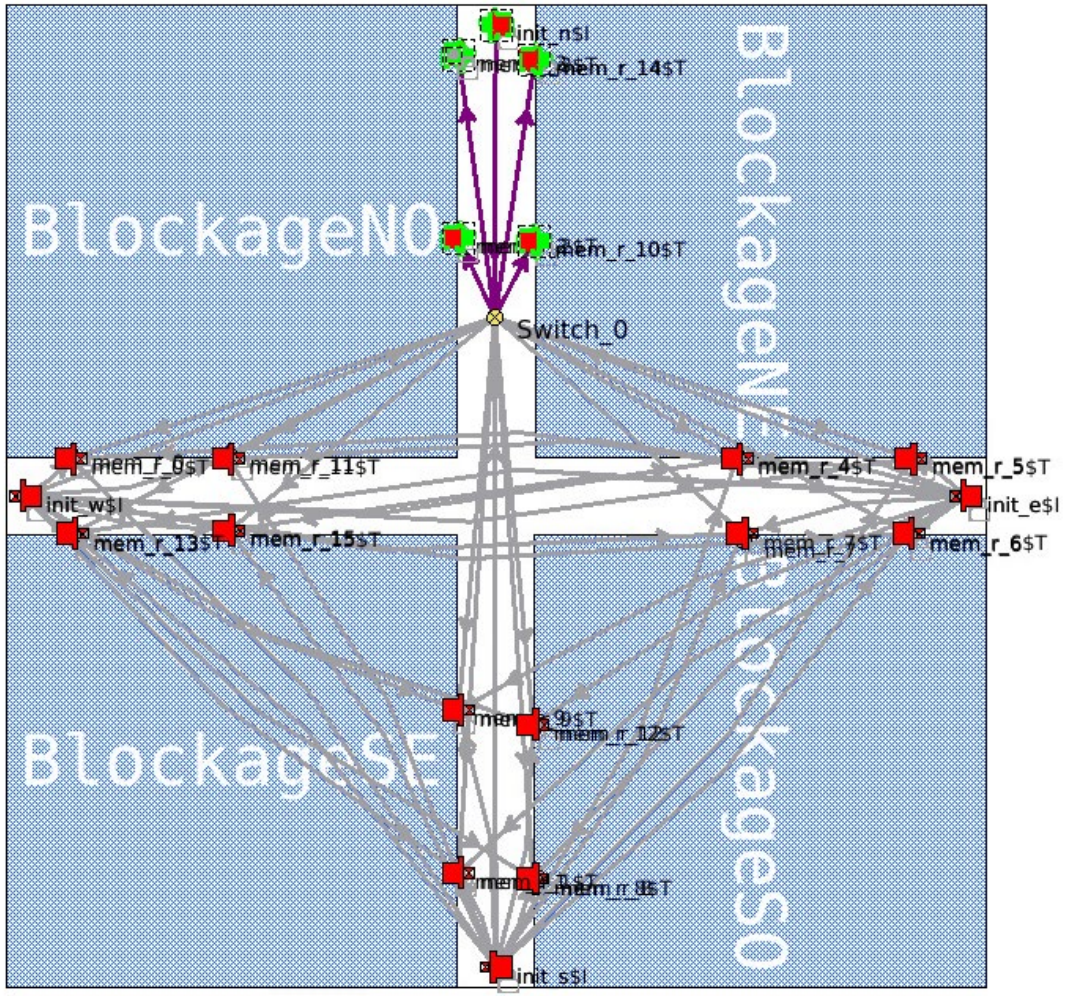
- Reset the initial topology
  - Users can create a more optimal version using the floor plan as a guide



Example Case

Considering Options – Step 2

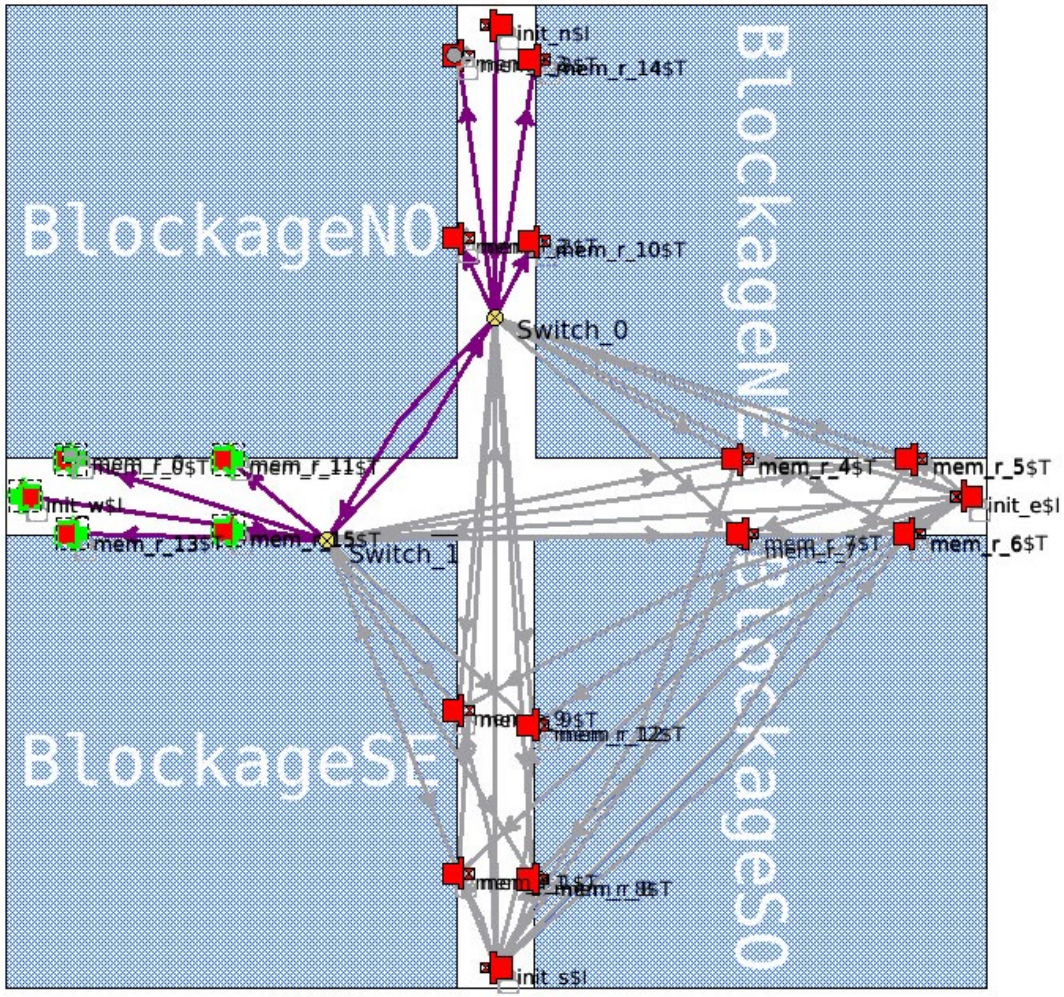
- Add a switch
  - Selecting 5 connections to be connected to a new switch as a group



Example Case

Considering Options – Step 3

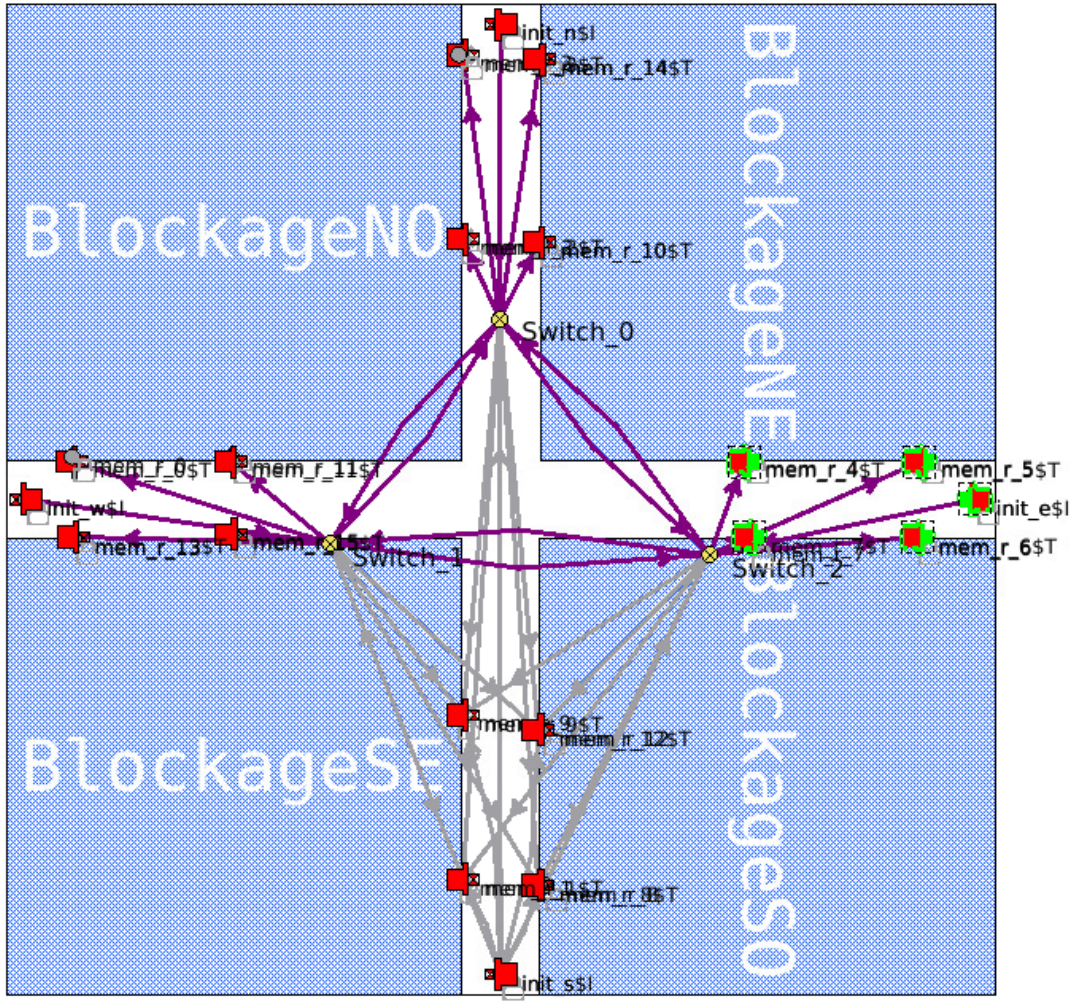
- Add another switch
  - Selecting another 5 connections to be connected to a new switch as a group



Example Case

Considering Options – Step 4

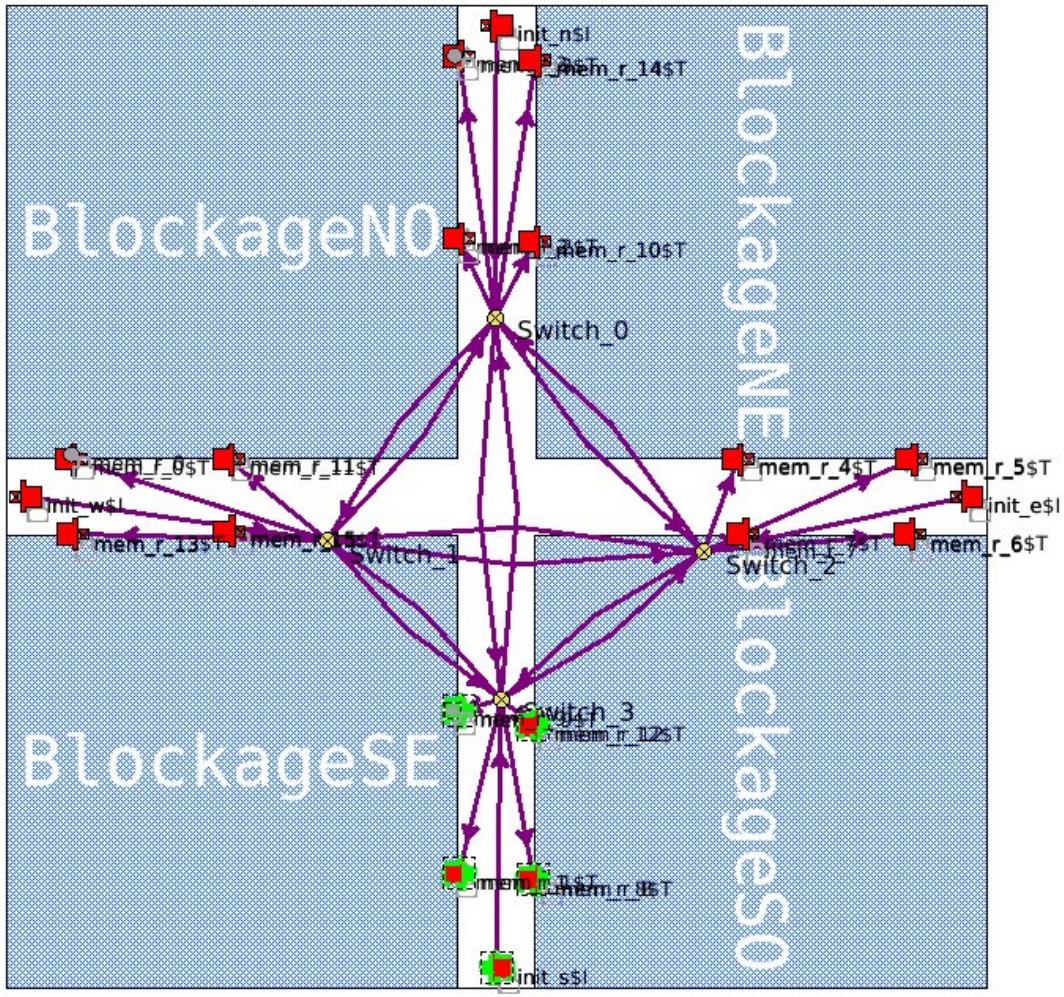
- Add another switch
  - Selecting another 5 connections to be connected to a new switch as a group



Example Case

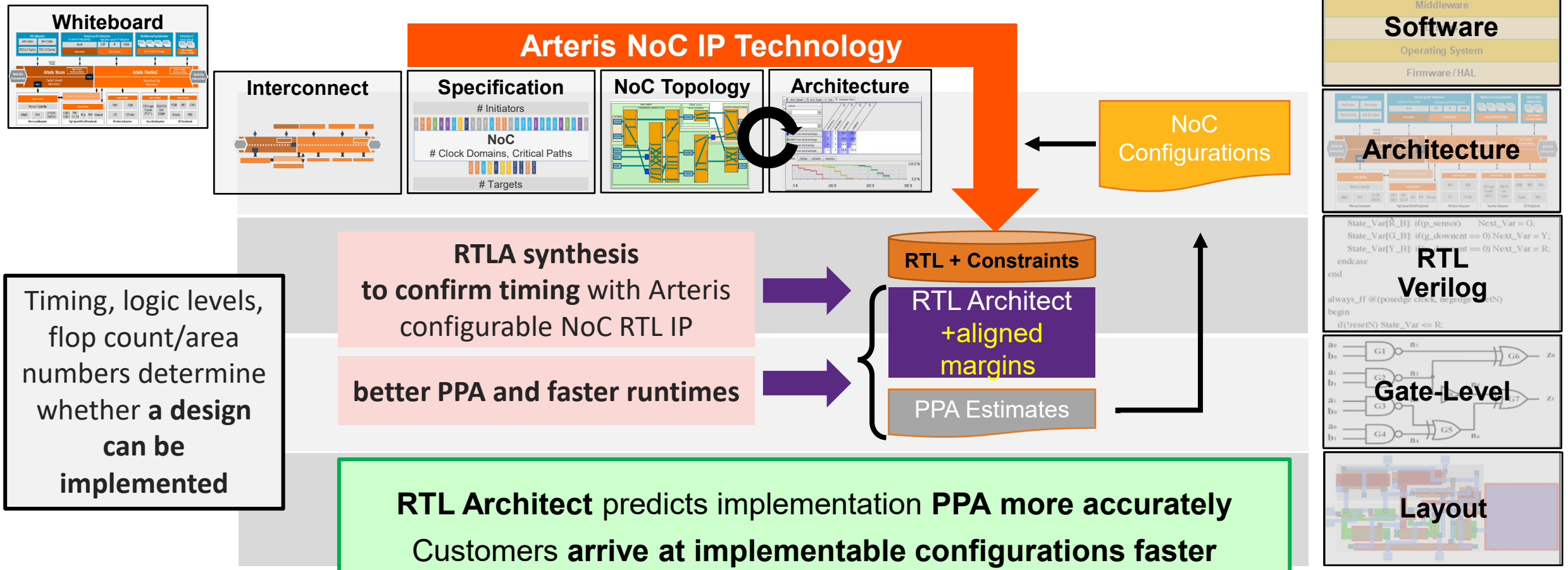
Considering Options – Step 5

- Add another switch
  - Selecting another 5 connections to be connected to a new switch as a group



RTL Architect Exploration

Converge faster with less customer iterations



PPA Review with RTL Architect

- RTL Architect
  - Provides reliable timing
  - Allows assessments early
  - … to fix high logic levels
- Designers review violations
  - Possible timing bug
  - Possible recoding
  - Allowing ULVT
  - Adding a pipe stage
  - Choosing faster memory

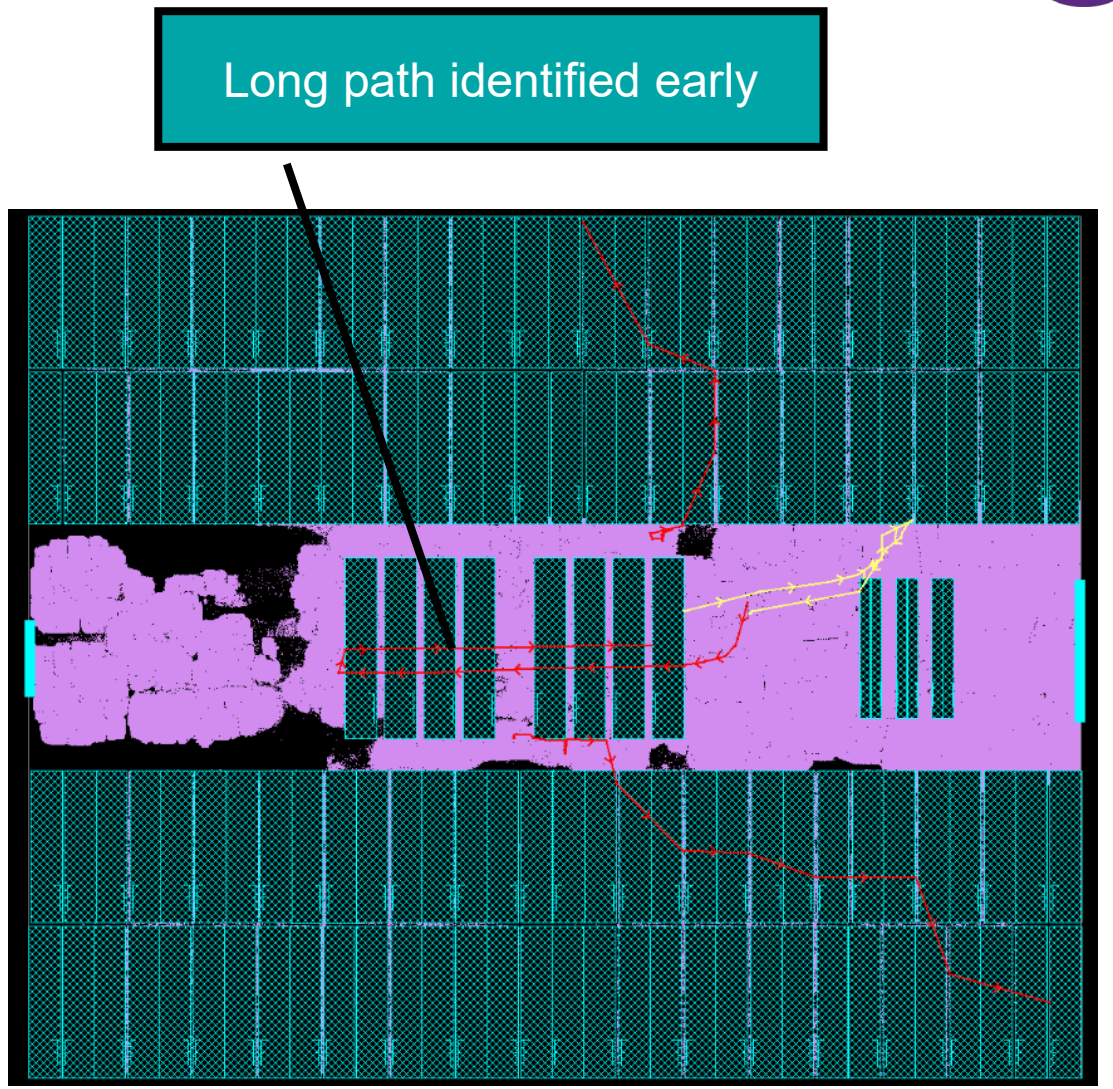
Example Results

Floorplanned Blocks	Wed Mar 8 19:24:44 2023							
	Flop2Flop Paths				Macro2Flop	Flop2Macro	Errors & Warnings	Bucketizer Link
Block	WNS (ns)	TNS (ns)	NVP	LOL	WNS	WNS		
aiu_top_a	-0.0116	-0.99	149	36				Bucketizer
aiu_top_b	0.1731	0.00	0	19	0	0		
aiu_top_c	0.2067	0.00	0	21	0	0		
aiu_top_d	0.1083	0.00	0	19	0	0		
config_dii_a	0.0186	0.00	0	25	0	0		
csr_network_a	0.0328	0.00	0	10	0	0		
dce_a	0.0019	0.00	0	19	0.1519	0.0095		
dii_top_a	0.0103	0.00	0	25	0	0		
dmi_a	-0.0168	-1.87	431	19	-0.0585	-0.0509		Bucketizer
dmi_b	-0.0105	-0.95	251	35	-0.0530	-0.0403		Bucketizer
dmi_c	0.2524	0.00	0	16	1.3984	0.3572		
dmi_d	0.2524	0.00	0	16	1.3984	0.3572		
dn_a	0.0008	0.00	0	8	0	0		
dve_a	0.0259	0.00	0	3	0	0		
fsc_a	0.1764	0.00	0	4	0	0		
gen_wrapper	-0.0115	-0.36	178	5	-0.0701	-0.0915		Bucketizer
grb_a	0.1342	0.00	0	6	0	0		
ioaiu_top_a	0.0026	0.00	0	4	0.0680	0.0090		
ioaiu_top_b	0.0003	0.00	0	20	0.0622	0.0005		
ioaiu_top_c	0.0024	0.00	0	37	0	0		
ioaiu_top_d	0.2839	0.00	0	19	0	0		
ndn1_a	0.0083	0.00	0	3	0	0		
ndn2_a	0.0367	0.00	0	6	0	0		
ndn3_a	0.0722	0.00	0	4	0	0		

Source: Internal Reference Design, 5 nm

PPA Review

- RTL Architect allows early review of placement issues
- Allows to address well before actual layout runs are done
  - Refining Floorplan
  - Exploring with placement bounds
  - Exploring rtl recoding



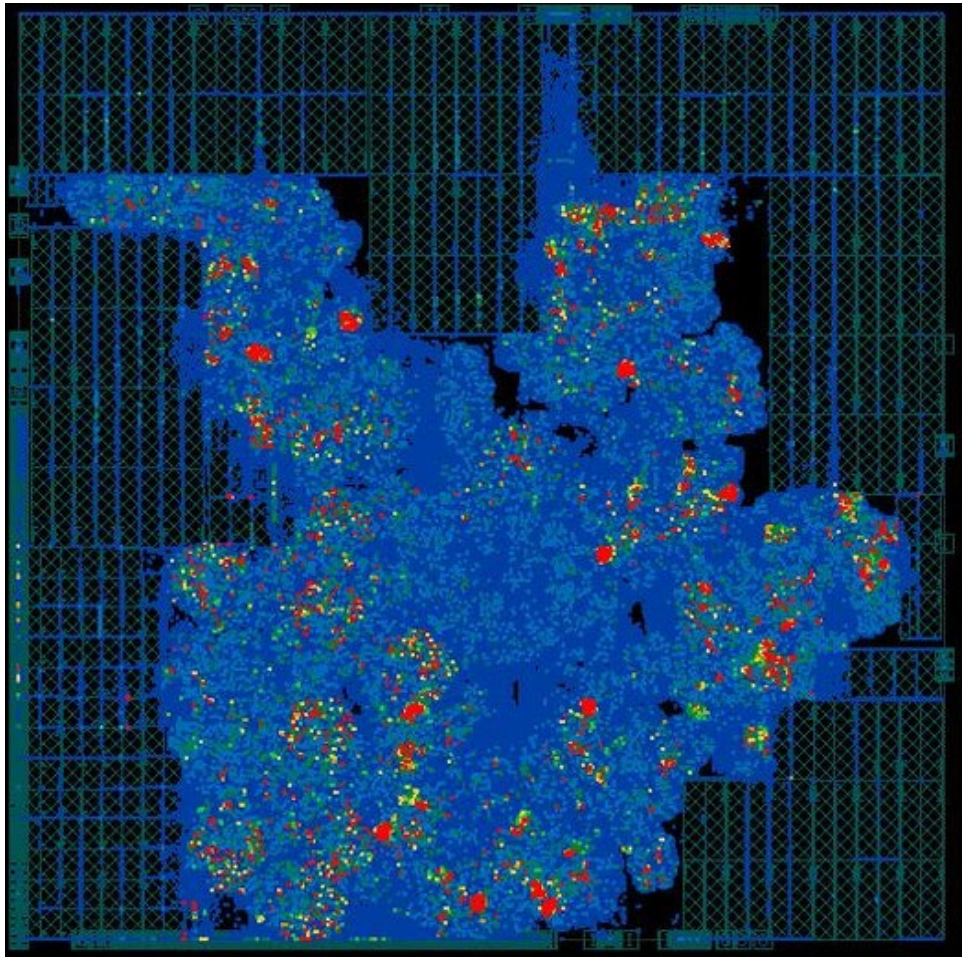
Source: Internal Reference Design, 5 nm

PPA Review

- Using RTL Architect in early congestion analysis with PG
  - Review Cell Density map & Hot spots
  - Review Utilization
  - Make floorplan changes if any

```
Both Dirs: Overflow = 133855 Max = 140 (1 GRCs) GRCs = 56061 (0.18%)
H routing: Overflow = 50390 Max = 140 (1 GRCs) GRCs = 17718  (0.11%)
V routing: Overflow = 83465 Max = 90 (1 GRCs) GRCs = 38343  (0.24%)
1
```

Source: Internal Reference Design, 5 nm

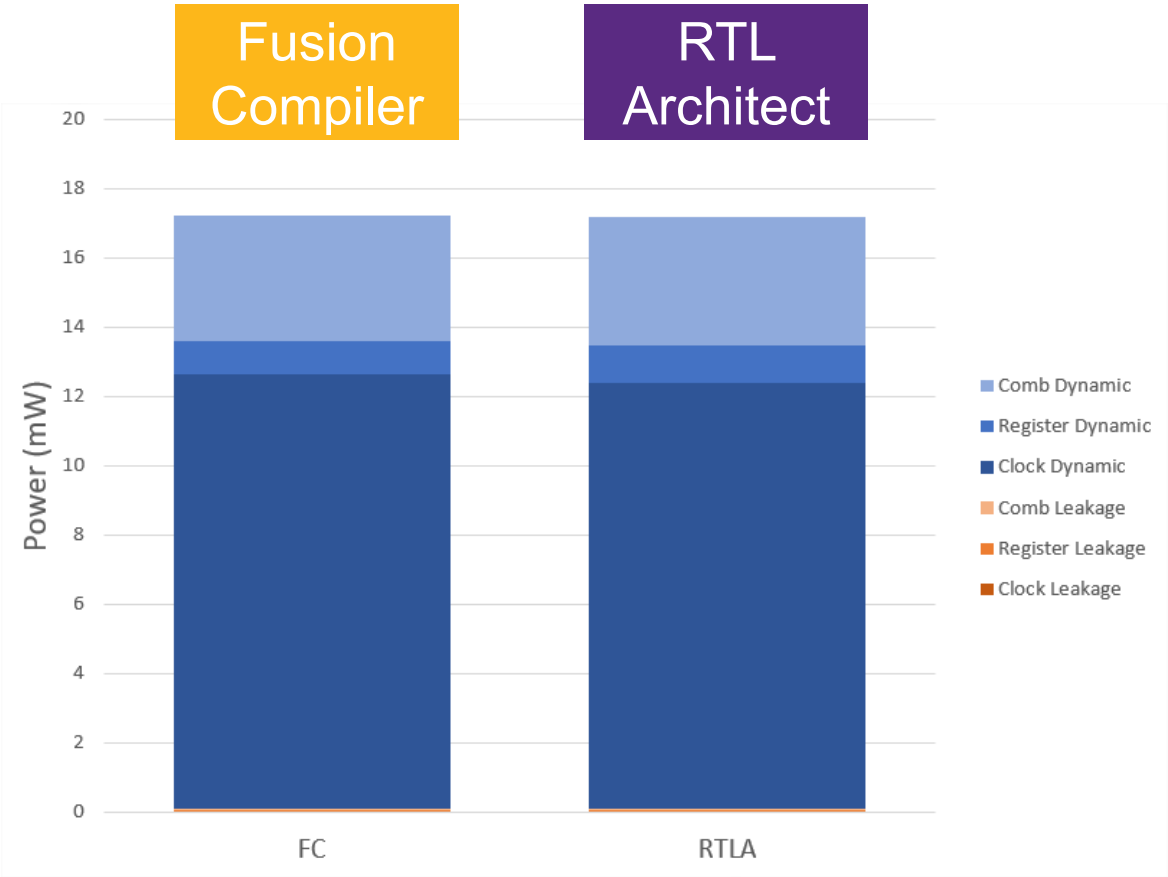


Source: Internal Reference Design, 5 nm

Early Power Estimation

- RTL Architect provides reliable power estimates

Run	Clock Leakage	Register Leakage	Comb Leakage	Clock Dynamic	Register Dynamic	Comb Dynamic	Total
FC	5.12E-04	5.00E-02	4.25E-02	1.25E+01	9.71E-01	3.61E+00	1.72E+01
RTLA	5.10E-04	5.27E-02	4.07E-02	1.23E+01	1.08E+00	3.72E+00	1.72E+01
Deviation	-0.4%	5.4%	-4.2%	-2.1%	10.9%	2.9%	-0.2%

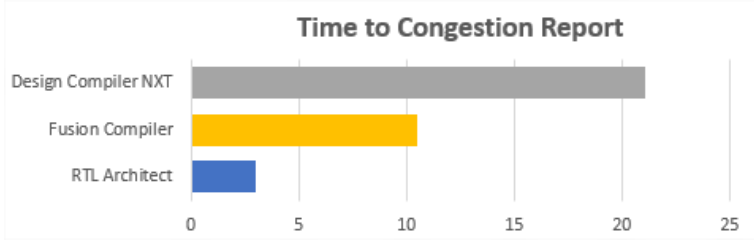


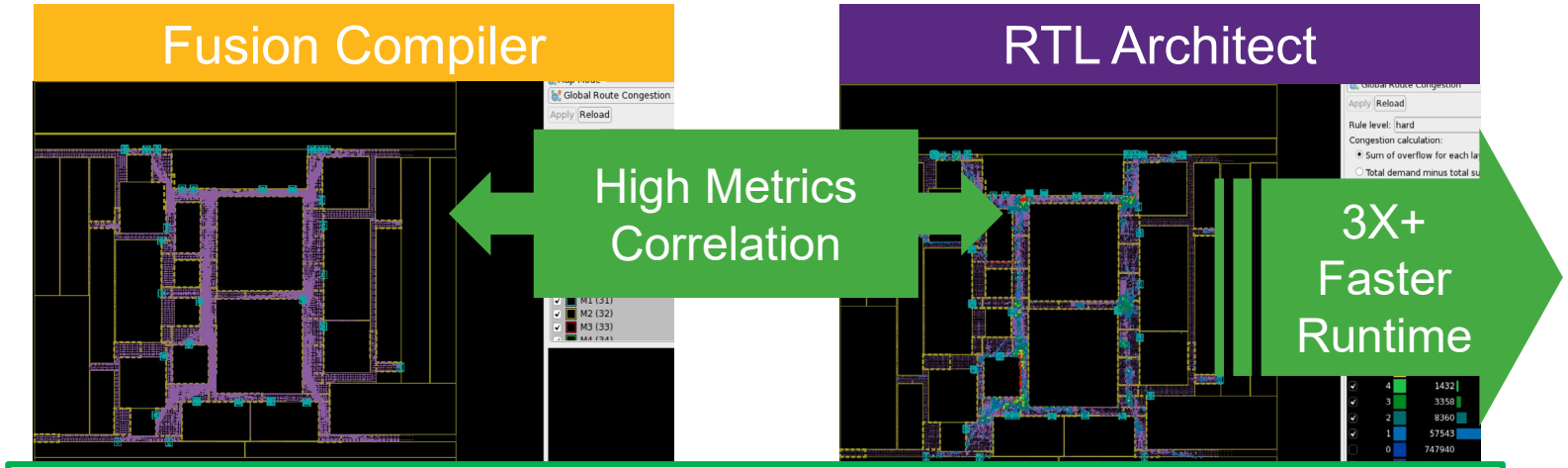
Source: Internal Test Design, 16nm

NoC Implementation with RTL Architect

- RTL Architect QoR results highly correlated to Fusion Compiler
  - Area within 2%
  - Timing within 10%
  - Power within 5%

- RTL Architect runtime 3X+ faster than Fusion Compiler & 6X+ faster than DCNXT





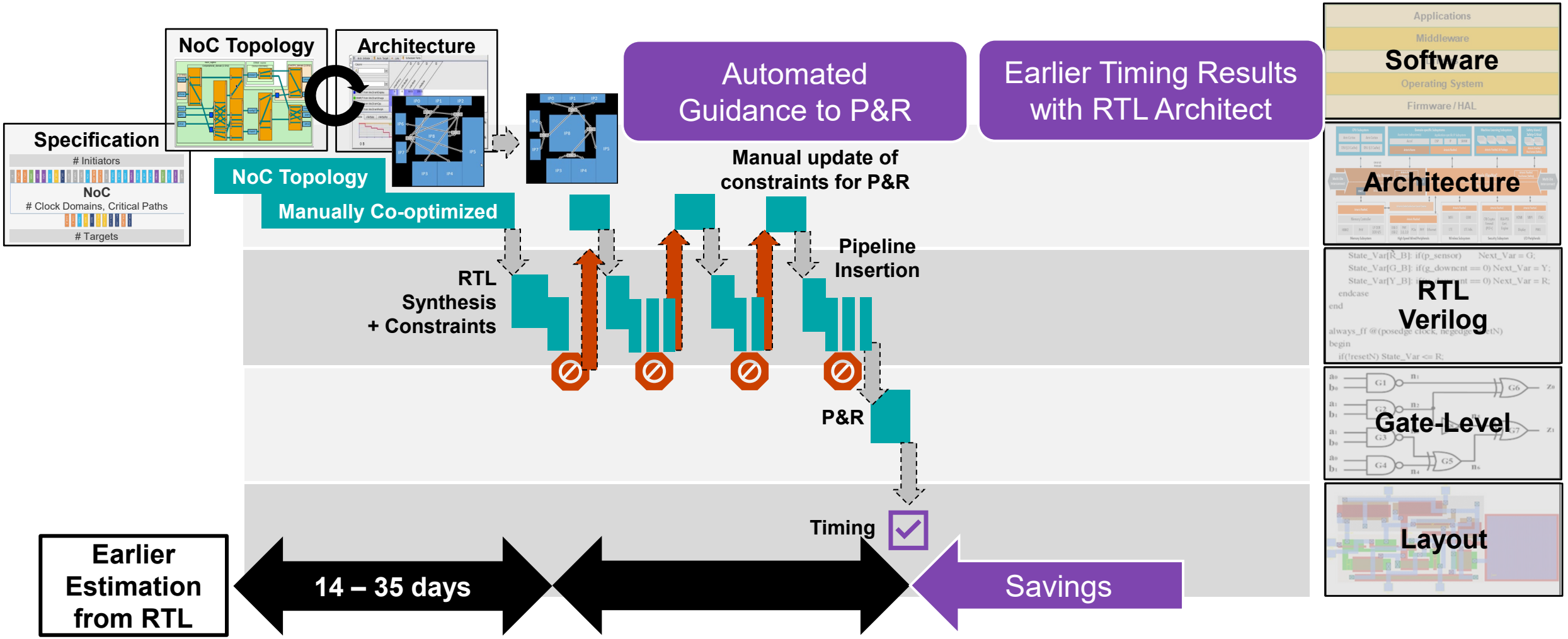
Improved RTL quality with RTL Architect
Better RTL delivering better PPA

Applying RTL Architect Earlier Estimations

ARTERIS IP

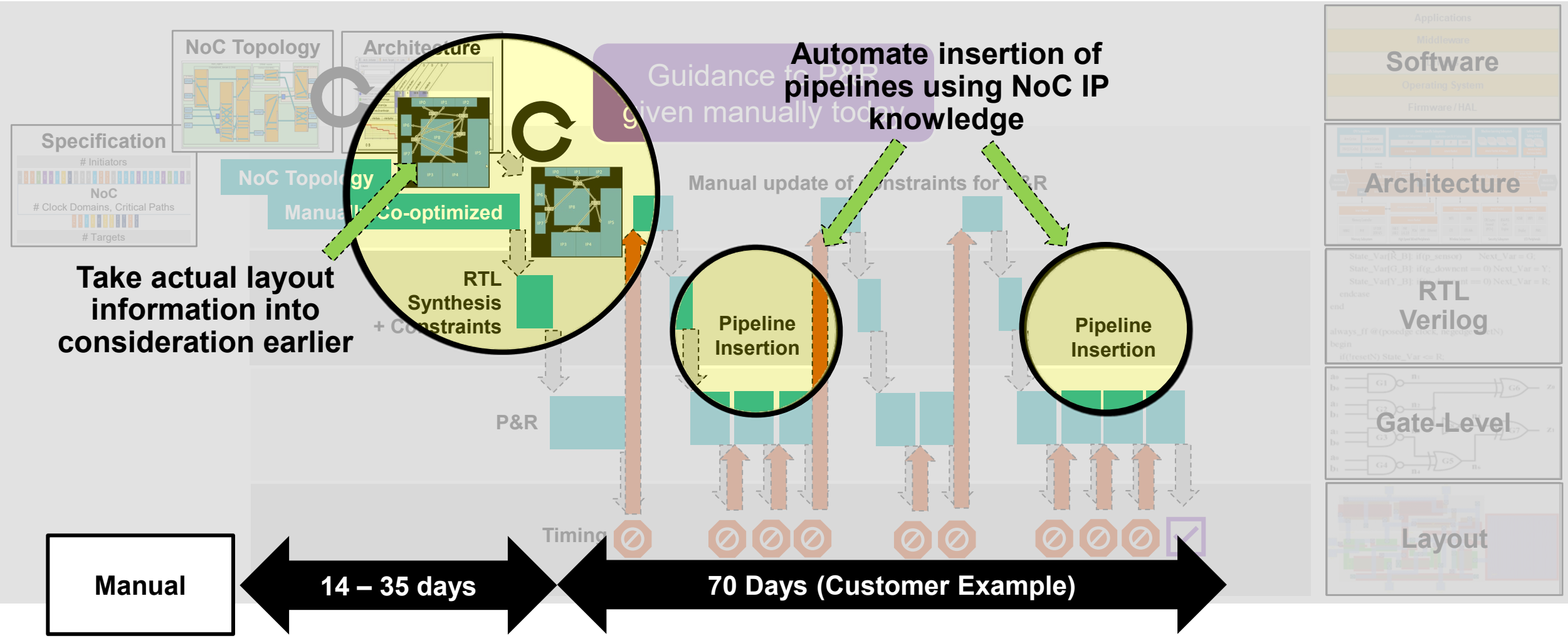
snug

Accelerate Turn-Around-Time



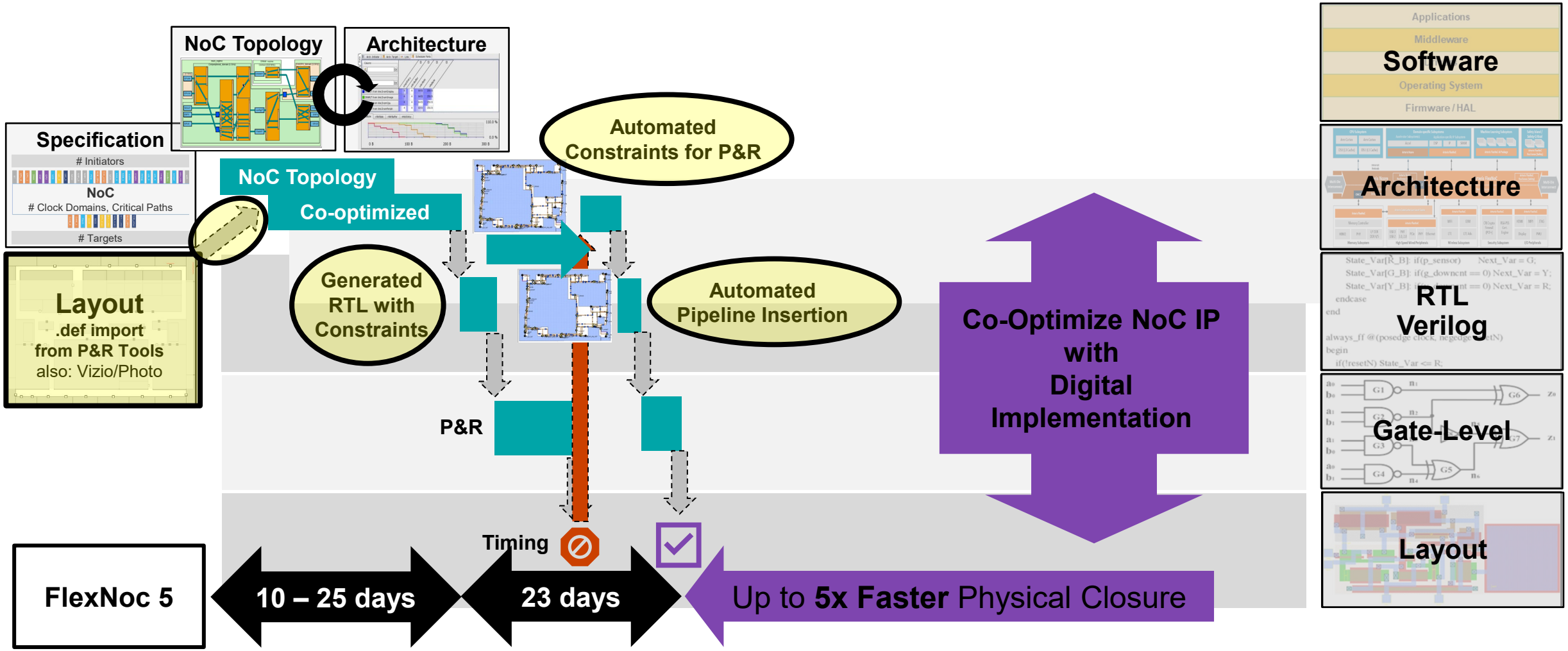
Further Automation Opportunities

Apply further abstraction



FlexNoC 5

Announced February 2023



Conclusions

Conclusion

- Fast RTL Exploration Solution
  - Built on implementation and signoff engines for improved convergence
  - Will benefit our customers and easy interaction
- Collaboration and Next Steps
  - Arteris IP to update physical constraints generation to drive floor plan refinement based on RTL Architect's timing and power estimation
  - Expand support of abutted vs. channel-based implementation

➢**Synopsys and Arteris are collaborating to improve NoC implementation flows for tough floorplans**

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THANK YOU

YOUR
INNOVATION
YOUR
COMMUNITY