Revolutionizing Synthesis to Preserve CDC Integrity

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About Broadcom

Global technology leader that designs, develops and supplies a broad range of semiconductor, enterprise software and security solutions.

Broadcom is a Delaware Corporation Headquartered in Palo Alto, CA.

AGENDA

Introduction 1

- Traditional Synthesis Challenges
- CDC in Digital Design

Static Aware Synthesis (SAS) 2

Addressing CDC Issues with SAS 3

Case Studies 4

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Conclusion 6

Introduction

- Traditional Synthesis Challenges
- CDC in Digital Design

Introduction

Traditional Synthesis Challenges

1

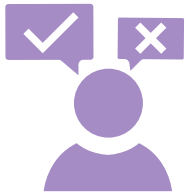
CDC Issues

Issues leading to
Glitches
Data Corruption
System Instability

2

Manual Input

Heavy reliance on manual input and decision-making, inefficient and error-prone



3

Post-Synthesis CDC

Post-synthesis CDC analysis is challenging due to the volume and complexity of data

4

Deep Understanding

Require deep understanding of CDC issues, precise solutions & impact TTM

Introduction

CDC in Digital Design

1

Managing CDC

Managing CDC is crucial for data transfer across different clock domains, due to asynchronous nature

2

Challenges

Risks of data loss, metastability, and timing errors, in systems with numerous interacting clock domains

3

Reliable Digital Circuits

For reliable functioning, integrity of CDC paths is fundamental

4

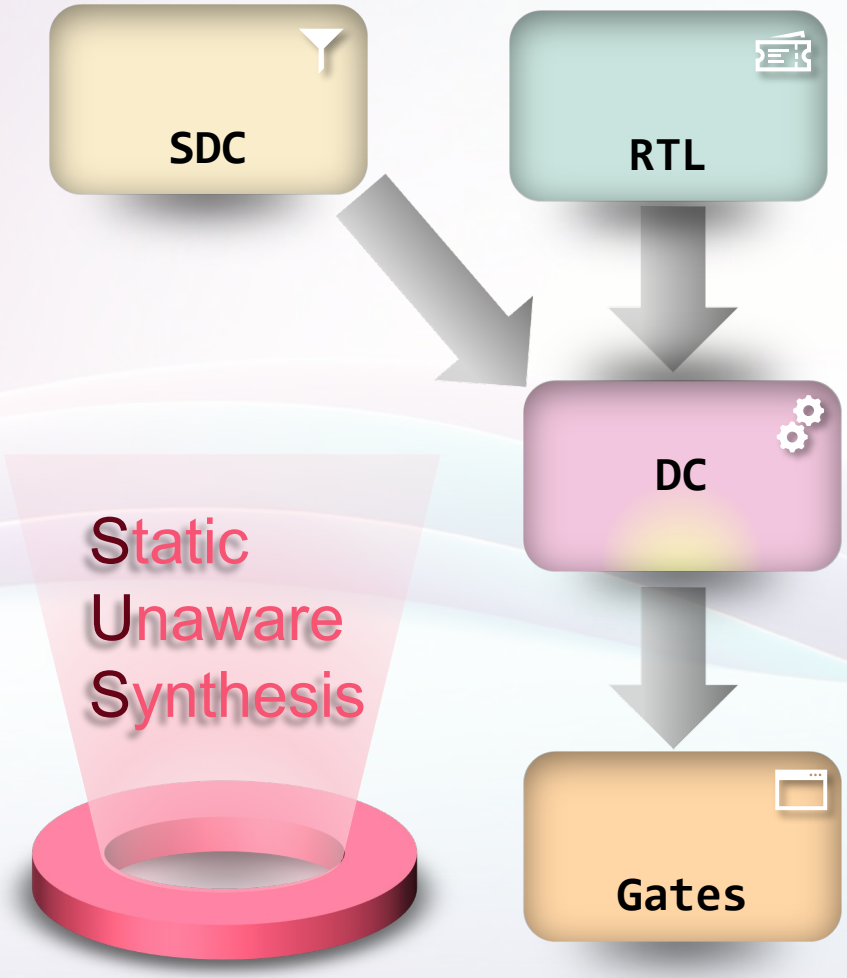
CDC Analysis

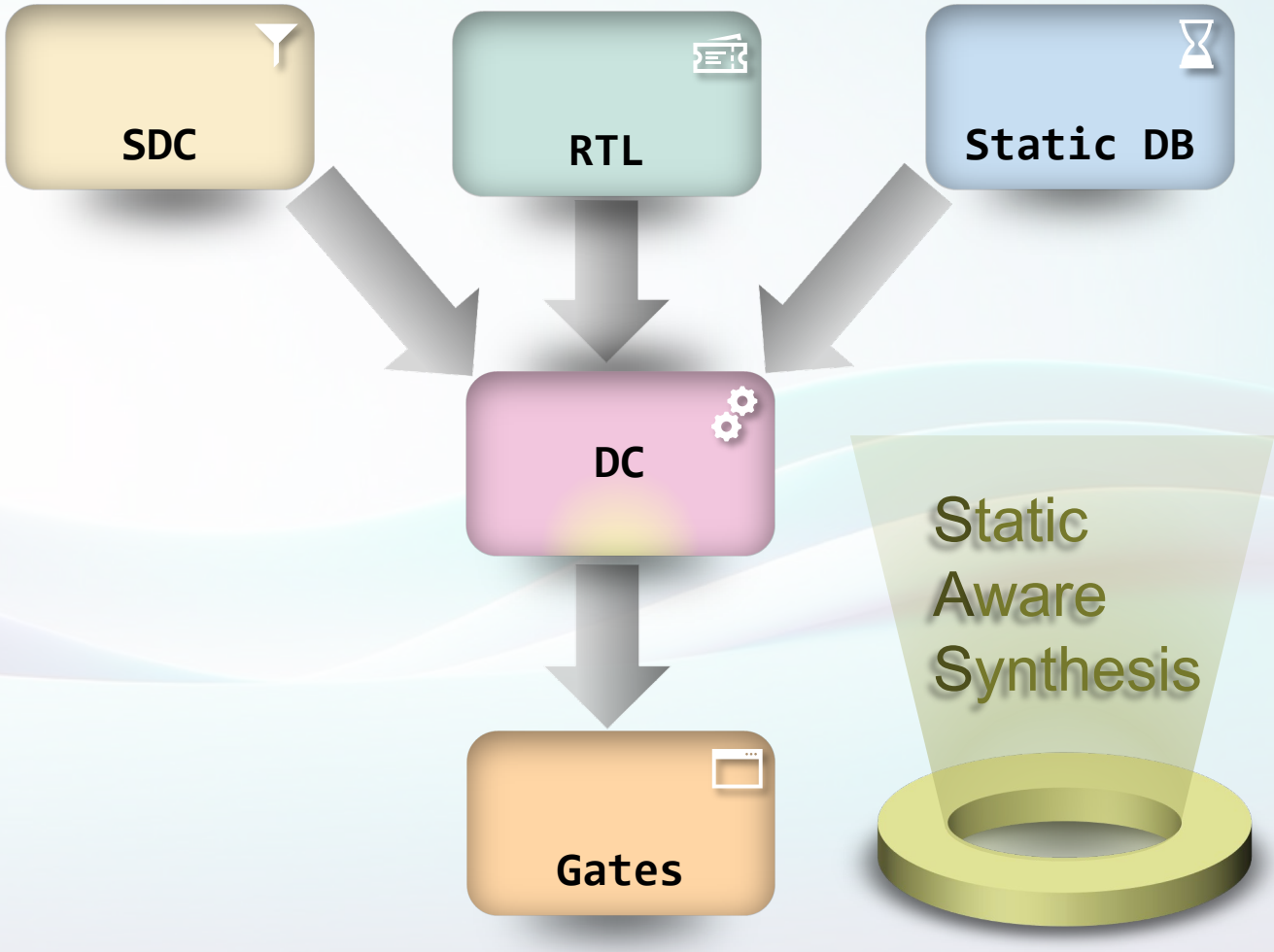
Conducted twice in the design process (pre and post-synthesis) to mitigate potential risks

Static Aware Synthesis
(SAS)

2

Traditional Synthesis Flow & SAS Flow Using Design Compiler (DC)





SAS Process - Synthesis

Post - Synthesis / Post - DFT CDC Validation
Proficiency in writing CDC-aware RTL & advancements in SAS Methodology could eliminate

Post-Synthesis CDC Validation
Remains necessary during UPF based synthesis

Post-DFT CDC Validation
Remains necessary when DFT on gate-level netlist

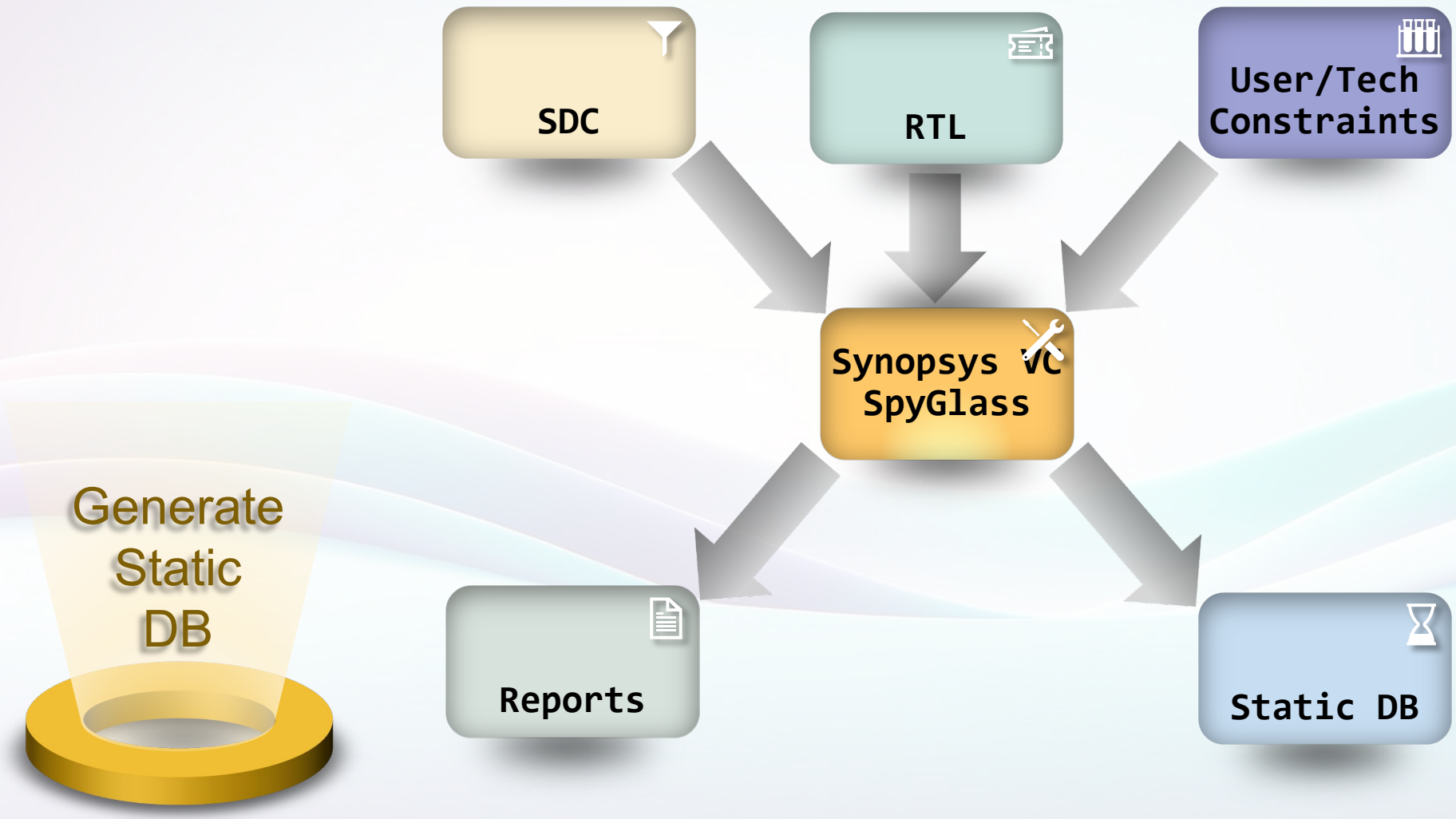
New CDC Issues
Be aware the processes that modify the netlist, may introduce new CDC issues

```
# sythesis.tcl
analyze -format sverilog { ../rtl/top.v }
elaborate top
current_design top
link
source -verbose -echo ./scripts/constraints.tcl
```

Reads input database from VC Spyglass to analyze CDC paths & apply restrictions for synthesis to avoid breaking the CDC paths

```
set_cdc_restrictions
-input ../vcst_rtdb/static_aware_synthesis_db/cdc \
-mux_effort none \
-verbose > DC_restrictions.log
report_cdc_restrictions > ./reports/cdc_restrictions.rpt
```

Generate Static DB (CDC) File Using VC SpyGlass



SAS Process – CDC Analysis

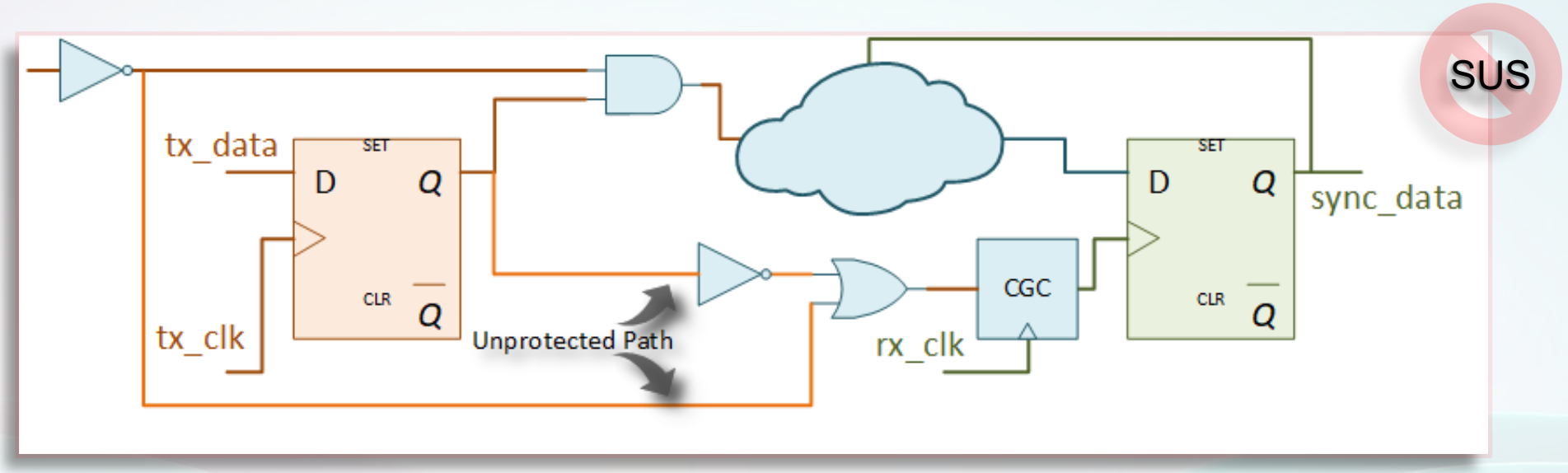
```
# vc_static.tcl
analyze -format sverilog {../rtl/top.v } \
-vcs { +define+DC -work WORK -f ./scripts/vcs_opts_vlog.f }
elaborate top -vcs { -liblist_work -liblist_nocelldiff }
read_sdc ./scripts/top.sdc
```

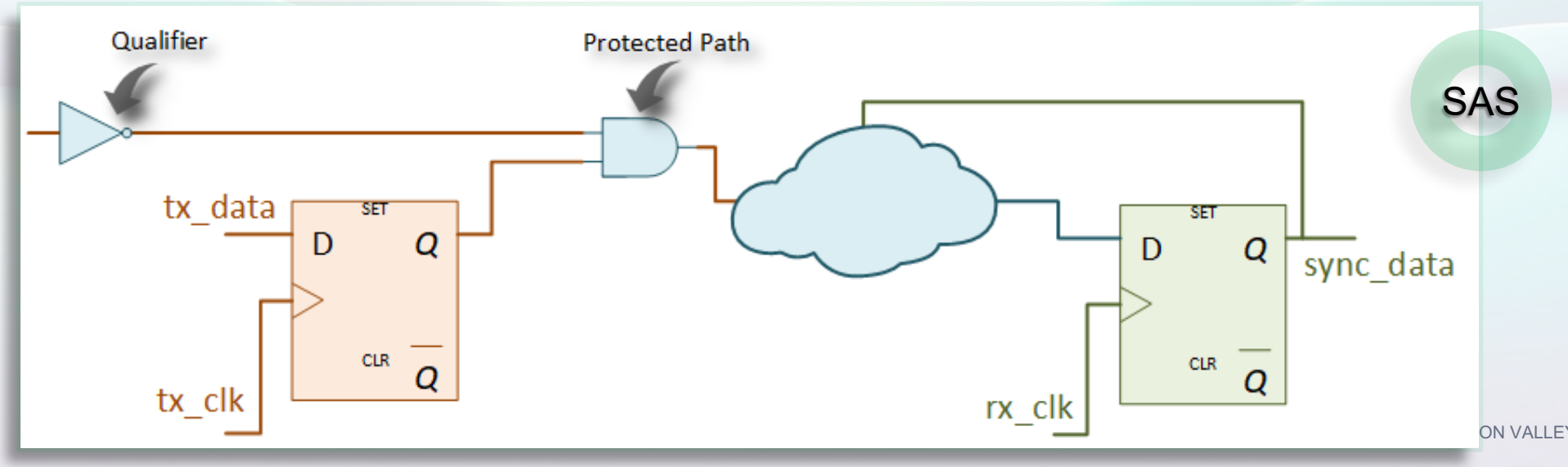
Use this command to control the generation of static database for synthesis tools.
Synthesis tools consume/understand static database which helps to perform various operation.
For example, if CDC app is specified with the command, the synthesized netlist is CDC aware, that is, certain synthesis optimizations are not performed around CDC paths, that can potentially introduce new CDC issues in the netlist.

```
configure_static_aware_synthesis \
-app cdc -enable -dc_path /tools/synthesis/2022.12-SP7
check_cdc
report_cdc
```

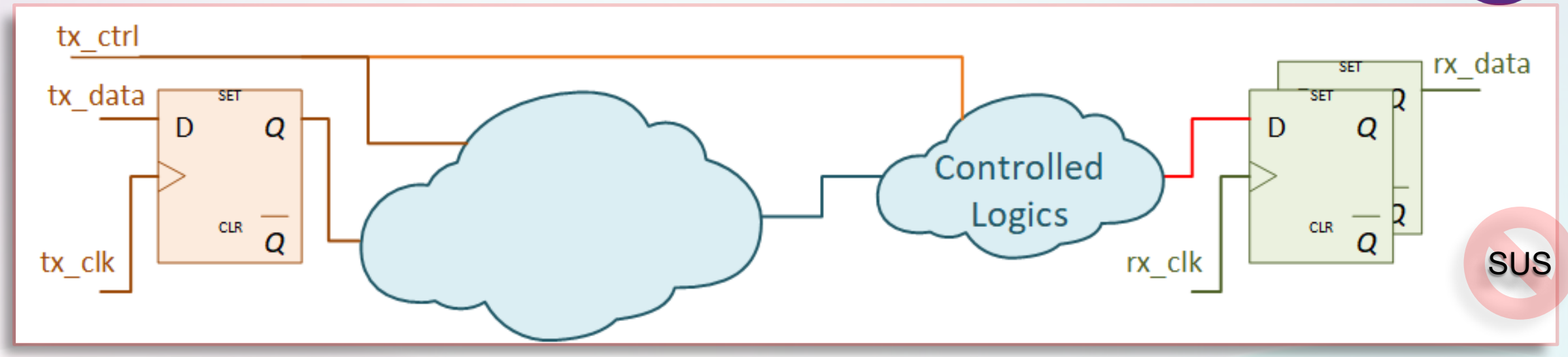
Addressing CDC Issues
with SAS

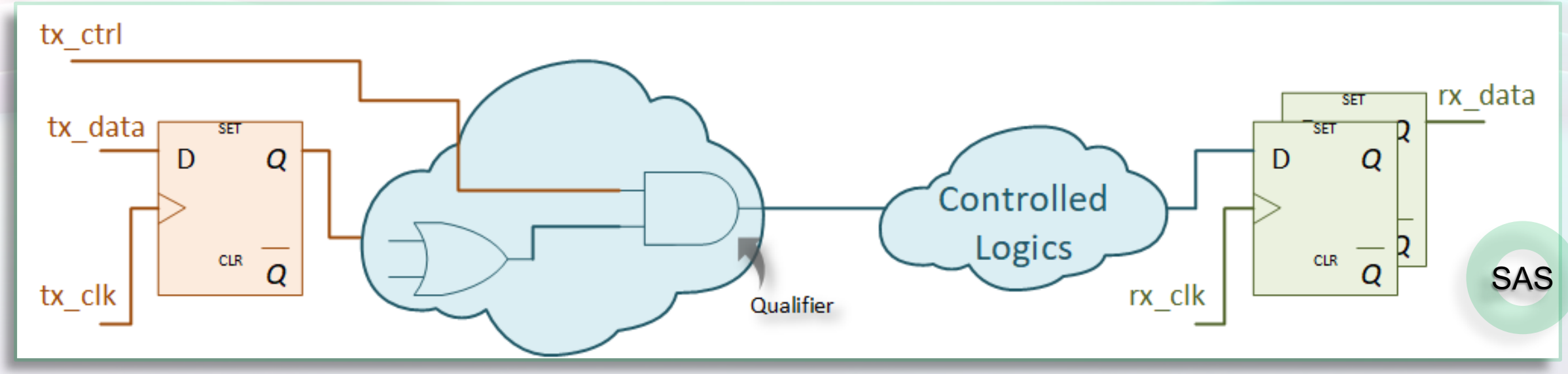
Data Clock Domain Crossing



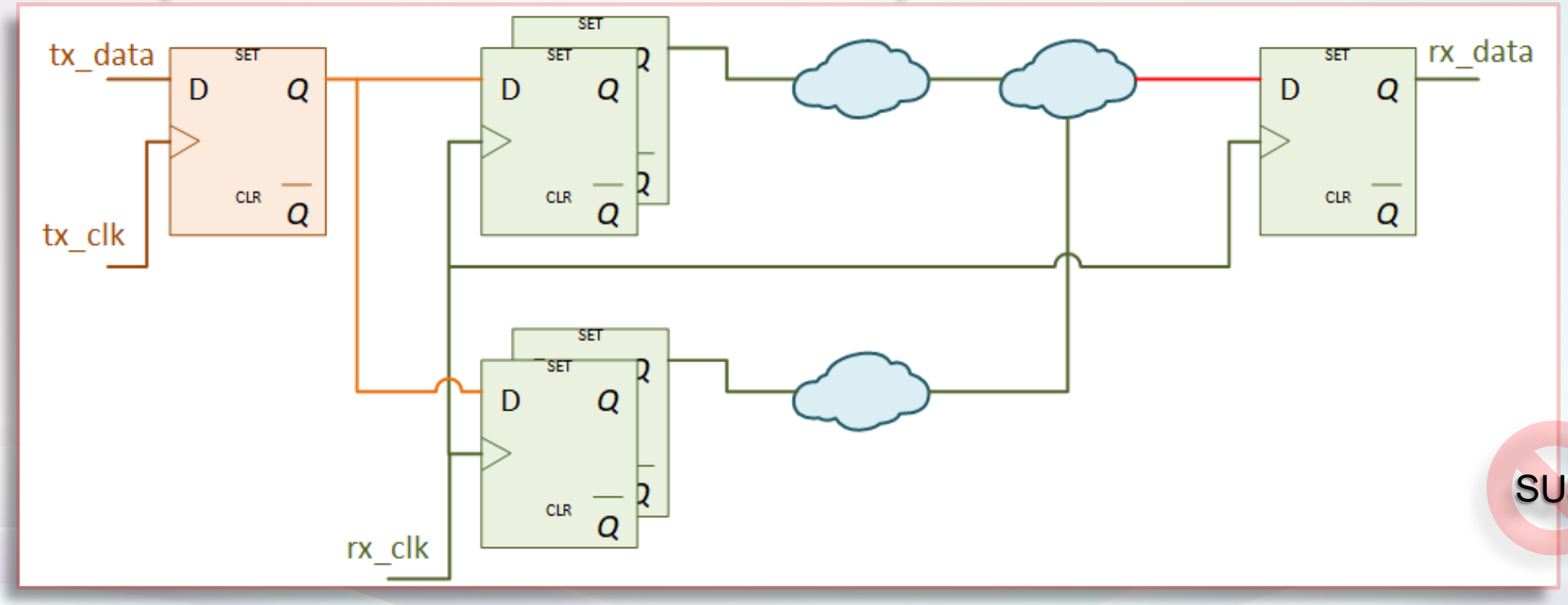


Glitches - Combinational Control Signal Crossings

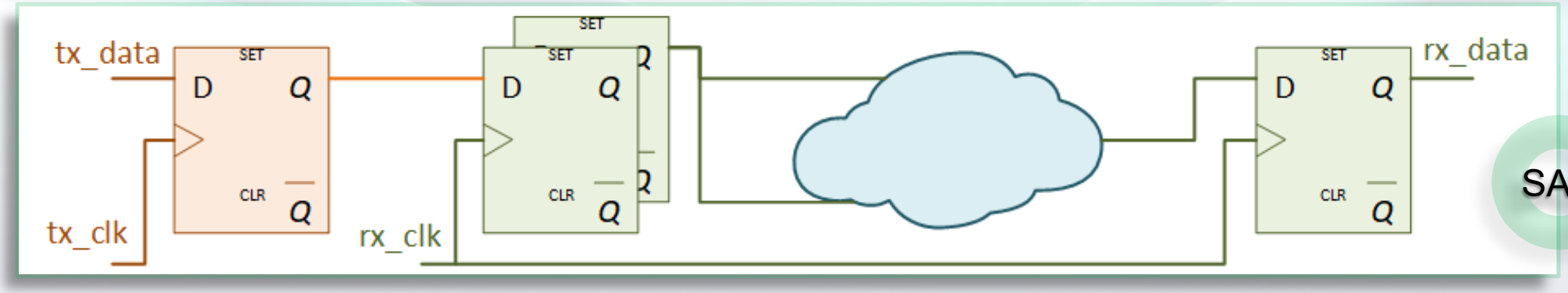




Control Synchronization Coherency



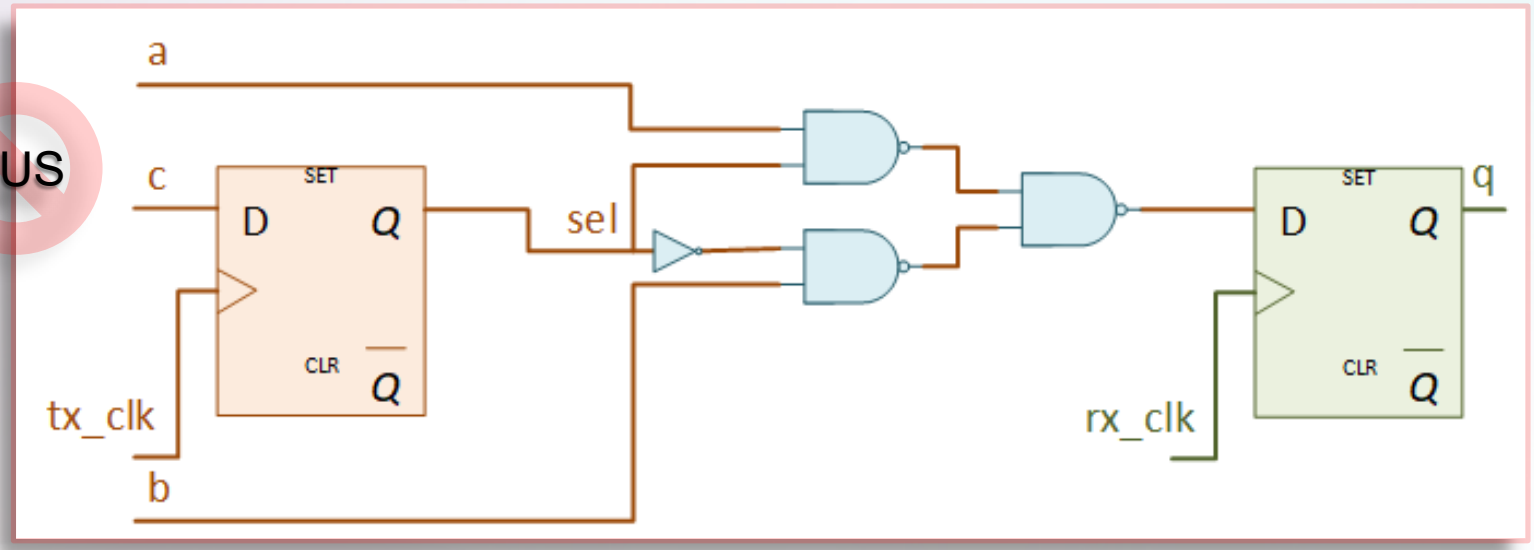
SUS



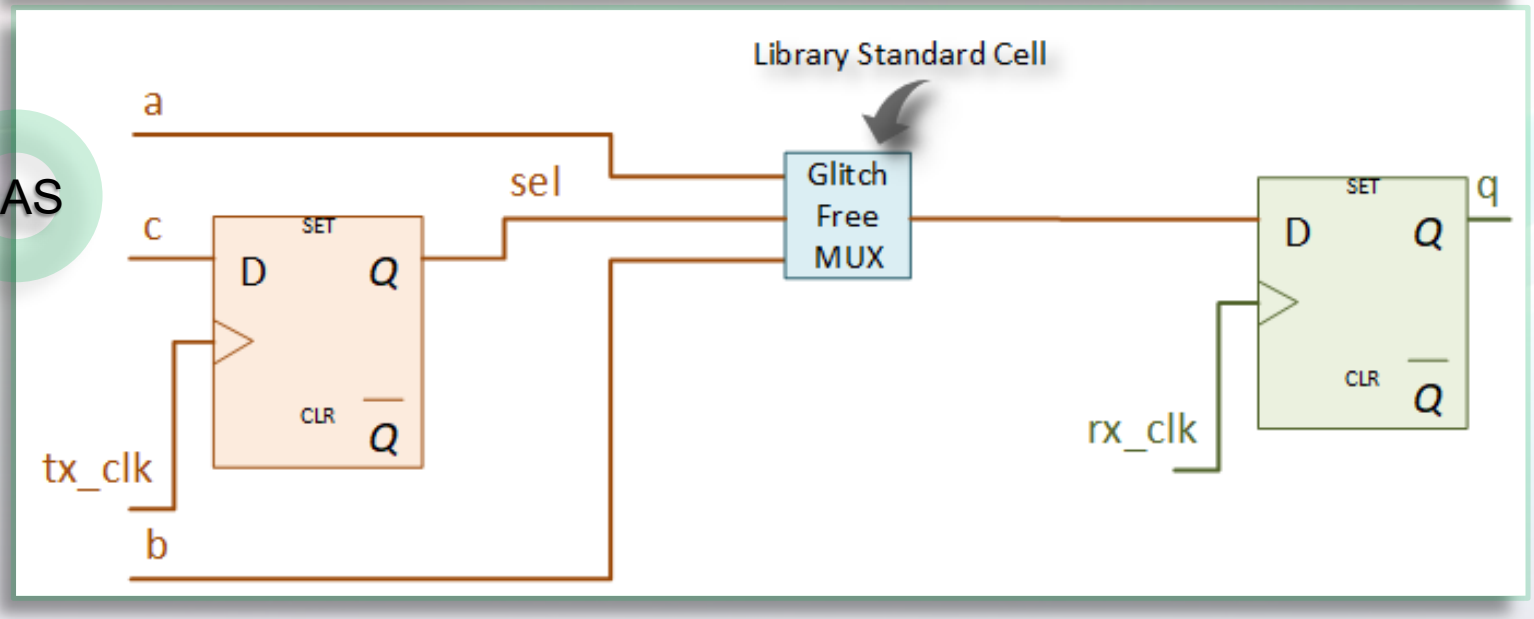
SAS

MUX Decomposition

SUS

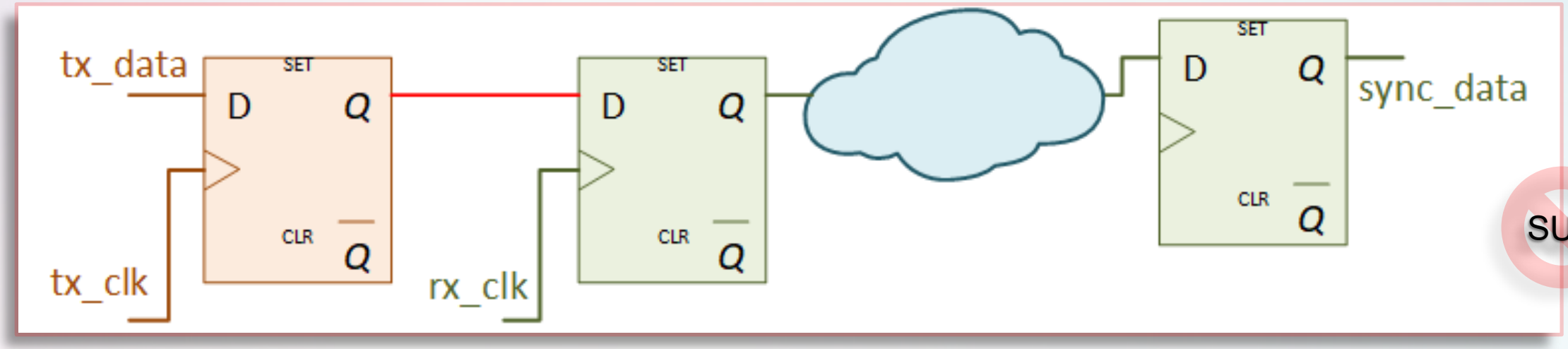


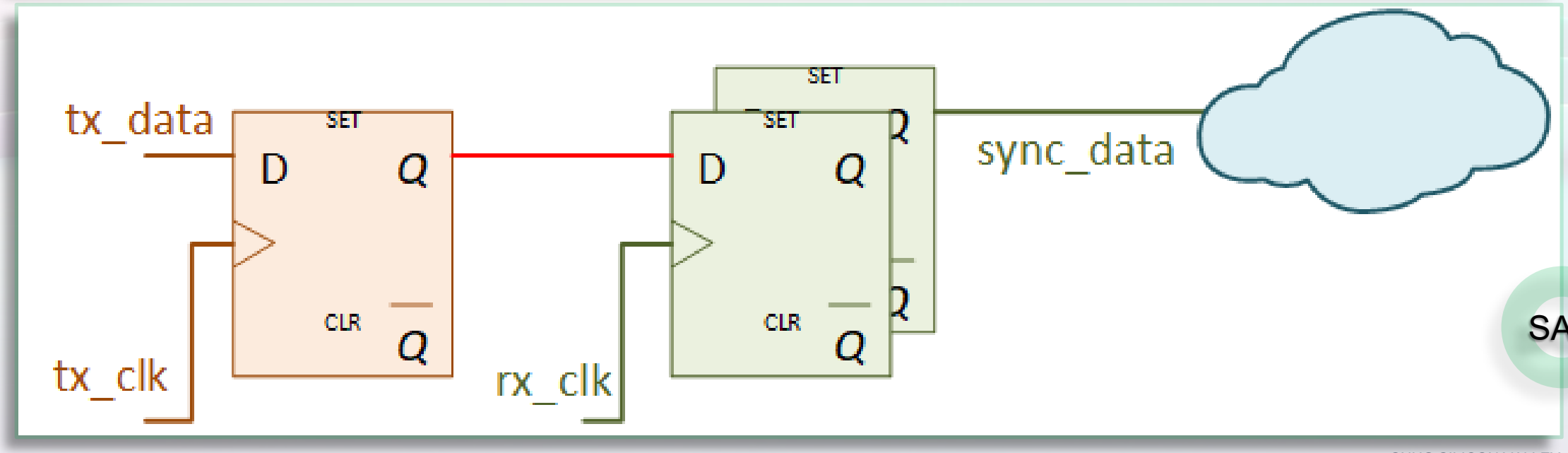
SAS



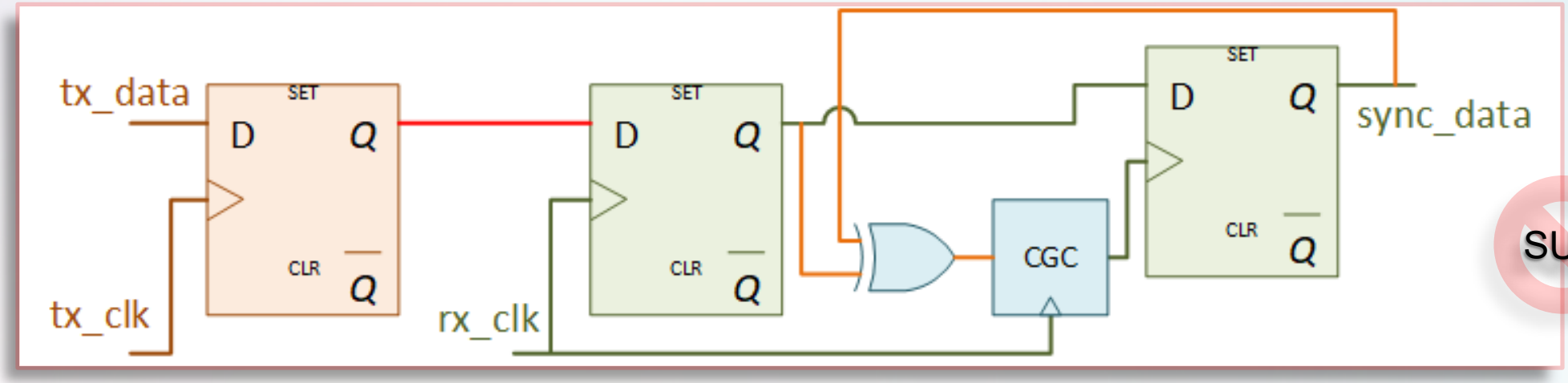

```
 1  module aoi_mux_ex
 2  (output q,
 3  input a,
 4  input b,
 5  input c
 6  );
 7
 8  reg q;
 9  reg sel;
10
11  always_ff @(posedge rx_clk)
12  if (sel) q <= a;
13  else     q <= b;
14
15  always_ff @(posedge tx_clk)
16      sel <= c;
17
18  endmodule
```

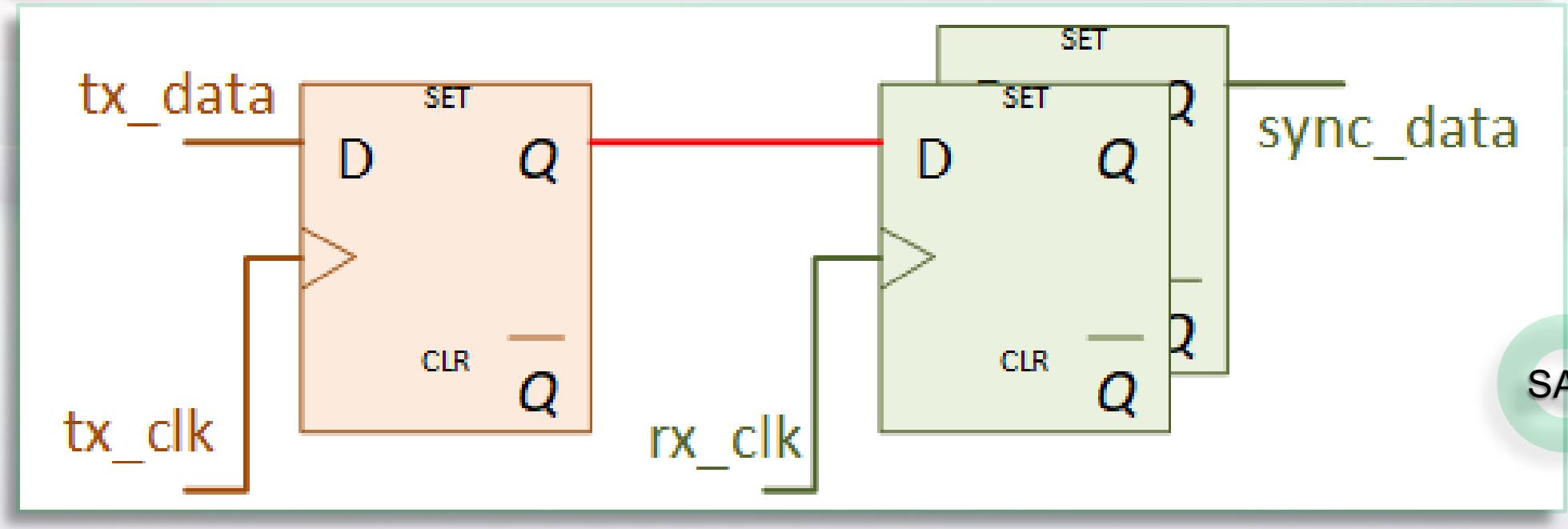
Re-Timing


tx_data
SET
D
Q
CLR
Q
tx_clk
rx_clk
sync_data
SUS


tx_data
SET
D
Q
CLR
Q
tx_clk
rx_clk
sync_data
SAS

Unexpected Clock-Gate Insertion Between Synchronizers





Case Studies

4

VC Static CDC Summary

On RTL & Static Un-aware Synthesis Gate

Stage Order Summary | Severity Order Summary

Severity	Stage	Family	Tag	Open	Waived	Compressed
info	SETUP	CLKPROP	SETUP_DATA_CONSTANT	3	0	0
info	SETUP	CLKPROP	SETUP_CLOCK_PROPAGATED	2	0	0
info	SETUP	RESET	SETUP_RESET_CONSTANT_INACTIVE	40	0	0
info	SETUP	RESET	SETUP_RESET_PROPAGATED	1	0	0
info	SETUP	CLKPROP	SETUP_PORT_CONSTRAINED	29	0	0
info	SYNC	CTRLPATH	CDC_SYNC_CTRL	3	0	0
info	SYNC	DATAPATH	CDC_SYNC_DATA	19	0	0
info	SYNC	IGNOREPATH	CDC_IGNOREPATH_QUASI_STATIC	106	0	0
info	GLITCH	GLITCH	CDC_GLITCH_DATA	3	0	0
warning	SETUP	RESET	SETUP_ASYNCRESET_UNUSED	1	0	0
warning	CONV	NOCONV	CDC_COHERENCY_VECTOR_DIFF_SYNC	5	0	0
Total:	212			212	0	0

RTL

Stage Order Summary | Severity Order Summary

Severity	Stage	Family	Tag	Open		
error	SETUP	CLKPROP	SETUP_CLOCK_UNDECL	41		
error	SETUP	CLKPROP	SETUP_BBOXPIN_UNCONSTRAINED	123		
error	SYNC	DATAPATH	CDC_UNSYNC_DATA	16	0	0
error	GLITCH	GLITCH	CDC_GLITCH_UNSYNC	16	0	0
info	SETUP	CLKPROP	SETUP_DATA_CONSTANT	3	0	0
info	SETUP	CLKPROP	SETUP_BBOXPIN_CONSTRAINED	41	0	0
info	SETUP	CLKPROP	SETUP_CLOCK_PROPAGATED	2	0	0
info	SETUP	RESET	SETUP_RESET_CONSTANT_INACTIVE	3	0	0
info	SETUP	CLKPROP	SETUP_PORT_CONSTRAINED	29	0	0
info	SETUP	CLKPROP	SETUP_PORT_IGNORED	7	0	0
info	SETUP	SDC	SETUP_SDC_CMD_IGNORED	1	0	0
info	SYNC	CTRLPATH	CDC_SYNC_CTRL	3	0	0
info	SYNC	DATAPATH	CDC_SYNC_DATA	44	0	0
info	SYNC	IGNOREPATH	CDC_IGNOREPATH_QUASI_STATIC	114	0	0
info	GLITCH	GLITCH	CDC_GLITCH_DATA	6	0	0
Total:	449			449	0	0

SUS

VC Static CDC Summary

On Static Un-aware & Aware Synthesis Gates

Stage Order Summary | Severity Order Summary

Severity	Stage	Family	Tag	Open	Waived	Compressed
info	SETUP	CLKPROP	SETUP_DATA_CONSTANT	3	0	0
info	SETUP	CLKPROP	SETUP_CLOCK_PROPAGATED	2	0	0
info	SETUP	RESET	SETUP_RESET_CONSTANT_INACTIVE	3	0	0
info	SETUP	CLKPROP	SETUP_PORT_CONSTRAINED	29	0	0
info	SETUP	CLKPROP	SETUP_PORT_IGNORED	7	0	0
info	SETUP	SDC	SETUP_SDC_CMD_IGNORED	1	0	0
info	SYNC	CTRLPATH	CDC_SYNC_CTRL	3	0	0
info	SYNC	DATAPATH	CDC_SYNC_DATA	755	0	0
info	SYNC	IGNOREPATH	CDC_IGNOREPATH_QUASI_STATIC	1212	0	0
info	GLITCH	GLITCH	CDC_GLITCH_DATA	246	0	0
warning	INTEGRITY	CLKPROP	INTEGRITY_CLOCKRESET_OUTPUT_RACE	2	0	0
warning	INTEGRITY	CLKPROP	INTEGRITY_RESET_UNEXPECTED_CELLS	6	0	0
warning	CONV	NOCONV	CDC_COHERENCY_VECTOR_DIFF_SYNC	25	0	0
Total:	2294			2294	0	0

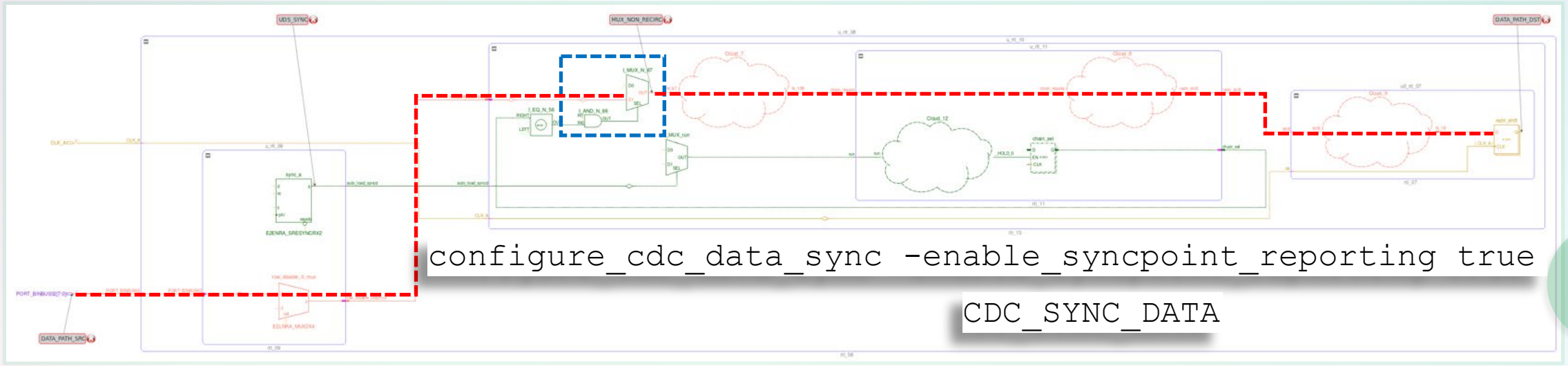
SAS

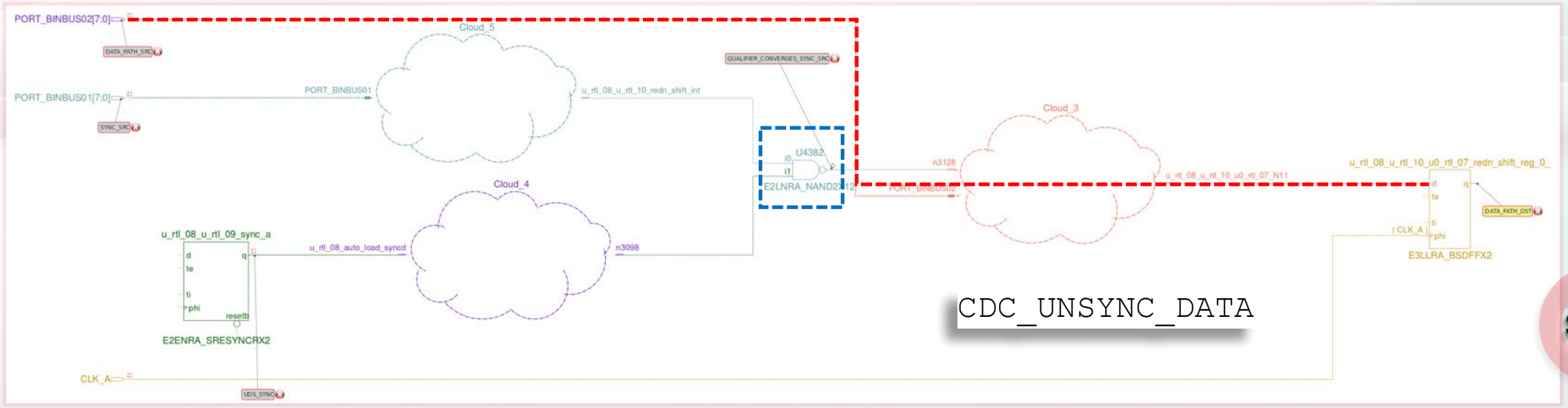
Stage Order Summary | Severity Order Summary

Severity	Stage	Family	Tag	Open	Waived	Compressed
error	SETUP	CLKPROP	SETUP_CLOCK_UNDECL	41	0	0
error	SETUP	CLKPROP	SETUP_BBOXPIN_UNCONSTRAINED	123	0	0
error	SYNC	DATAPATH	CDC_UNSYNC_DATA	16	0	0
error	GLITCH	GLITCH	CDC_GLITCH_UNSYNC	16	0	0
info	SETUP	CLKPROP	SETUP_DATA_CONSTANT	3	0	0
info	SETUP	CLKPROP	SETUP_BBOXPIN_CONSTRAINED	41	0	0
info	SETUP	CLKPROP	SETUP_CLOCK_PROPAGATED	2	0	0
info	SETUP	RESET	SETUP_RESET_CONSTANT_INACTIVE	3	0	0
info	SETUP	CLKPROP	SETUP_PORT_CONSTRAINED	29	0	0
info	SETUP	CLKPROP	SETUP_PORT_IGNORED	7	0	0
info	SETUP	SDC	SETUP_SDC_CMD_IGNORED	1	0	0
info	SYNC	CTRLPATH	CDC_SYNC_CTRL	3	0	0
info	SYNC	DATAPATH	CDC_SYNC_DATA	44	0	0
info	SYNC	IGNOREPATH	CDC_IGNOREPATH_QUASI_STATIC	114	0	0
info	GLITCH	GLITCH	CDC_GLITCH_DATA	6	0	0
Total:	449			449	0	0

SUS

CDC Data Crossing Analysis – RTL & SUS

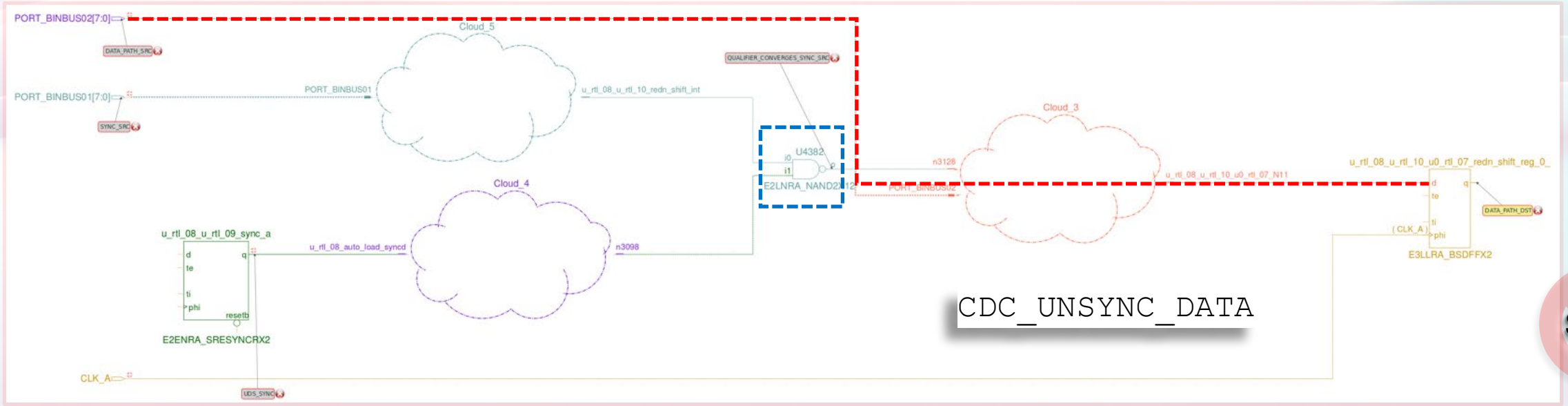




CDC Data Crossing Analysis – SUS & SAS

CDC_SYNC_DATA

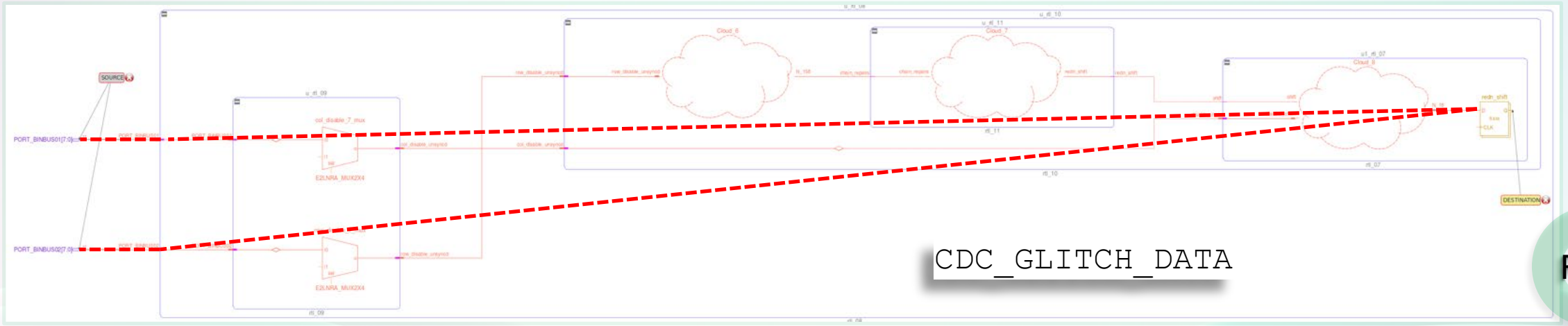
SAS



CDC_UNSYNC_DATA

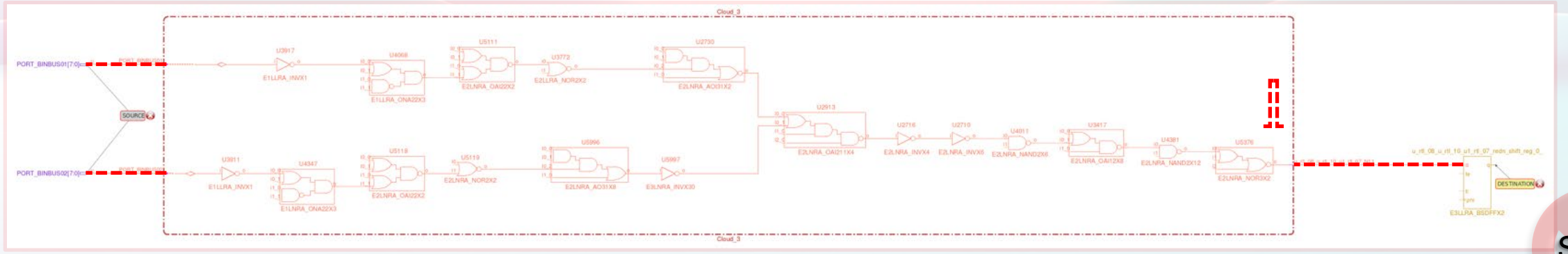
SUS

Analysis of Glitches Caused by Unsynchronized Signal Crossing – RTL & SUS



CDC_GLITCH_DATA

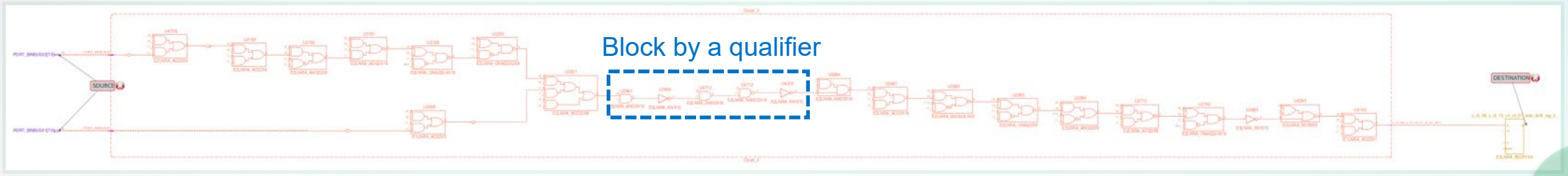
RTL



CDC_GLITCH_UNSYNC

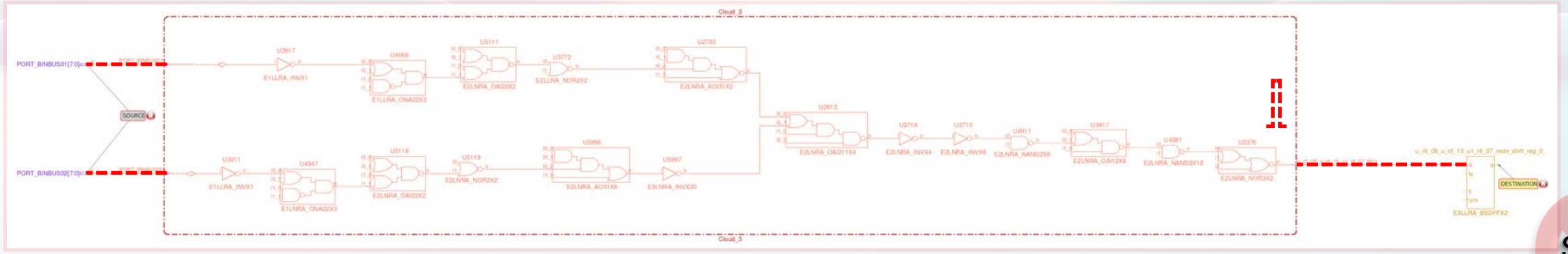
SUS

Analysis of Glitches Caused by Unsynchronized Signal Crossing – RTL & SUS



CDC_GLITCH_DATA

SAS



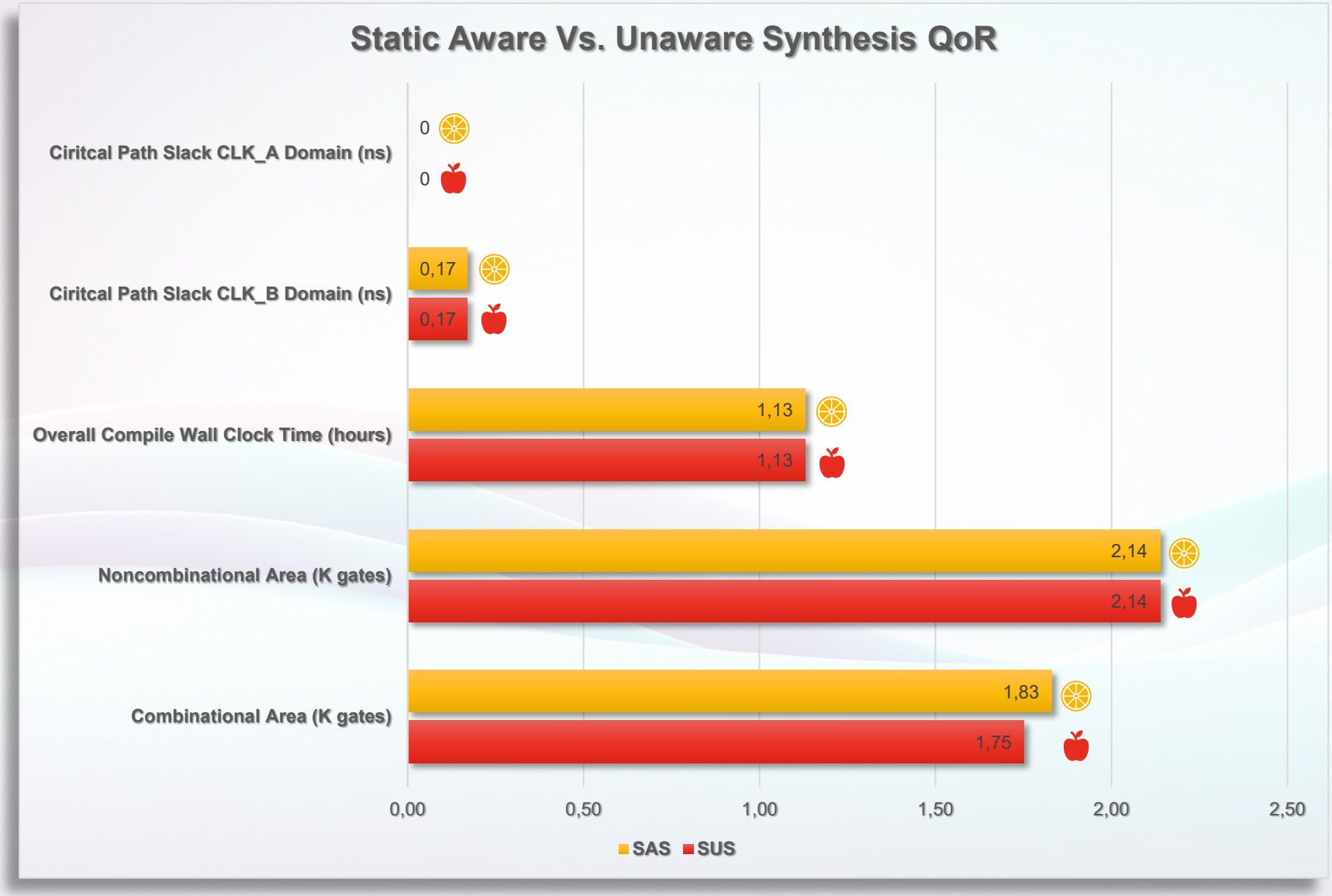
CDC_GLITCH_UNSYNC

SUS

Results

5

Results



1

Critical Path Slack

Remained same between SAS and SUS

Conclusion

Conclusion

1. **Reduction** in CDC errors & demonstrating its effectiveness in **mitigating CDC complexities**
2. Significant **time savings** & **efficiency** gains by integrating CDC analysis into the synthesis process, **reducing manual debugging** and correction time
3. Enhanced **data integrity** across clock domains with SAS, ensuring **reliable** circuit performance even in complex designs with multiple clock domains
4. **Faster TTM** and superior alternative to traditional synthesis methods, with SAS streamlining development cycles and improving design quality

"**SAS** has been evaluated in this paper. Gave constructive feedbacks to **Synopsys**. Could significantly benefit the industry as a whole"

THANK YOU

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INNOVATION
YOUR
COMMUNITY