

# Laker CDPR LEF/DEF Tutorial

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# 1 Overview

The Laker<sup>™</sup> Custom Digital Placer and Router (CDPR) provide unique automation for placement and routing of custom and standard cells within the Laker Custom Layout environment. It allows precise custom design of the digital blocks often used in mixed signal and custom digital designs in order to meet the critical performance requirements that often times cannot be achieved with a standalone digital automatic place and route (P&R) tool. Its proprietary technology allows you to:

- Save time with automated creation of digital blocks without leaving the Laker Custom Layout environment
- · Achieve the performance of full-custom layout with the speed of P&R
- Enjoy the confidence of using proven standard cells while maintaining hand-crafted quality
- Leverage all the features of the Laker Custom Layout Automation System for things like hand-routing of critical nets, or hand-drawing of routing spines.
- Save time using proven standard cells for high performance digital applications that previously had to be done by hand
- Avoid time-consuming switching between digital automatic place and route (P&R) and custom layout environments and the associated data preparation and translation



• Improve yield with post-route optimization that includes double via insertion, antenna fixing, and jog removal

# 2 Technology Overview

## 2.1 The Laker<sup>™</sup> Custom Digital Placer

The Laker<sup>™</sup> Custom Digital Placer can obtain optimum placement results with ease by allowing the user to:

- · Quickly and automatically place standard cells, optimized for minimum wire length
- Perform incremental selection and placement with drag-and-drop simplicity
- Pack the placement area or selected regions automatically
- Manually optimize placement, layout, or routing with any of the standard features of the Laker Custom Layout Automation System
- Automatically place pins
- Avoid the set-up, data translation, and time penalty of using a standalone P&R tool
- Work seamlessly with the Laker Custom Digital Router

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Figure 1: The Laker Custom Digital Placer

## 2.2 The Laker<sup>™</sup> Custom Digital Router

The Laker<sup>™</sup> Custom Digital Router saves time with unique automation technology for routing of digital blocks within the Laker Custom Layout Automation System in the following ways:

• Unique hybrid routing technology combines gridded- and shape-based routing for very high route completion rates. Global routing enables congestion analysis, mapping, and display during the floor-planning and placement stage (see Figure 2).





#### Figure 2: Optimize Placement and Routing Channels Using Congestion Maps

- Next, shape-based routing is used to go off the digital routing grid to connect to off-grid pins, complete routes, and avoid DRC violations.
- Spine-style routing is available that is ideally suited for the routing of memory blocks.

# **3 Tutorial Introduction**

In this tutorial, we will guide you through the typical Laker<sup>™</sup> Custom Digital Placer and Router flow starting from preparing the LEF library and DEF design, and then finishing digital routing. The following topics are included:

- 4 Environment Setup
- 5 Library Preparation
- 6 Design Preparation
- 7 Post-Placement
- 8 In-Route

# 4 Environment Setup

## 4.1 Tool Installation Version

Laker OA2011.03 for PG router and digital router is required.

## 4.2 Open Cell Library

The Si2 Nangate Open Cell Library is a generic open-source, standard-cell library provided for the purposes of research, testing, and exploring EDA flows. Therefore, the Si2 Nangate 1 PDKv1.3\_2009\_07 release of the Open Cell Library was selected for common library preparation.

<sup>&</sup>lt;sup>1</sup> The example information was obtained from the Si2 website (<u>http://www.si2.org/openeda.si2.org/projects/nangatelib</u>).



For more information, refer to the following website page: <u>http://www.si2.org/openeda.si2.org/projects/nangatelib</u>

Both Laker DB and Laker OA utilize the basic Open Cell Library in data preparation.

The following steps are optional if you only want to install the original package for reference:

## 4.3 Laker CDPR LEF/DEF Tutorial

On top of previous work of the Open Cell Library database, the following derivatives are created for the Laker CDPR LEF/DEF Tutorial:

source/technology	
OpenCellLibrary.tf	Laker technology file with advanced routing rules
laker.dsp	Laker display file
OpenCellLibrary.captbl	OpenCellLibrary reference CapTable file
source/library	
OpenCellLibrary.gds	Laker revised GDS file with new cells.
OpenCellLibrary.sp	Laker revised SPICE file with new cells and PG ports.
OpenCellLibrary.lef	Laker revised LEF file with modified metal1 fat metal rules and new cells.
OpenCellLibrary.cpf	Laker cell property file for updating Cell Property
OpenCellLibrary.idx	Laker generic cell content index file for Row Placement
TAPCELL_X1.gds	Laker generic TAP cell, it is necessary for tap-less standard cell flow
FILLCELL_X3.gds	Laker generic FILL3 cell, it is necessary for nofiller1 flow
PGMUX2_X1.gds	Laker generic pass-gate MUX2 design for PG ESD spacing flow
PGMUX2_X1.sp	Laker genetic pass-gate MUX2 design for PG ESD spacing flow
source/liberty	OpenCellLibrary Liberty Timing Library
source/design	
Divide.sp	CDL netlist of Divide example
Divide_pl.def	DEF floorplan file
Divide_pl.gds	GDS floorplan file
Divide.v	Gate level Verilog netlist of Divide example
Divide_vlog.f	List file for Import Verilog
CPU.sp	CDL netlist of CPU example
CPU.v	Gate level Verilog netlist of CPU example
CPU_vlog.f	List file for Import Verilog
source/constraint	
pin_bus.const	Laker pin constraint for Auto Pin Assignment in bus format
pin_opt.const	Laker pin optimization constraint for Auto Pin Assignment
placement.const	Laker placement constraint
matrix_rp.tcl	Laker hierarchical matrix constraint Tcl file
source/map	



lef_layer.map	Laker layer map file for Import LEF
lef_layer_out.map	Laker layer map file for Export LEF
lef2oa.map	Laker OA lef2oa layer map file for Import LEF
gds_layer.map	Laker layer map file for Import Stream
gds_font.map	Laker font size map file for Import Stream
SDL_def.map	Laker model map file for SDL flow
SDL_oa_def.map	Laker OA model map file for SDL flow
SDL_ref_nangate.map	Laker OA model map file for reference library flow
source/script	
route.tcl	Sample script for batch procedure of digital routing

The following steps install tutorial source files and a working directory:

- 2. Set up a new working directory environment.
  - > copy work\_clean work
  - > cd work

# **5** Library Preparation

## 5.1 Lab-1: Library Preparation by LEF

LEF library preparation is only necessary for pure LEF/DEF flows. In this lab, you will learn how to create an LEF library in abs (abstract) view.

#### 5.1.1 Import LEF Files

Usually, the library vendor provides an LEF file as an abstract view for DEF/LEF design flows. This standard file can be imported into Laker to create physical shapes with Pin/Port information.

- 1. Invoke File  $\rightarrow$  Import  $\rightarrow$  LEF to input an LEF file.
- 2. In the *Import LEF* form, do the following:
  - a. Select **Design File** as OpenCellLibrary.lef
  - b. Assign Library Name to OpenCellLibrary\_lef
  - c. Assign Technology → ASCII File to OpenCellLibrary.tf
  - d. Assign Layer Map File to lef\_layer.map.

After importing an LEF file with a Laker technology file, the MACRO cell information will be derived from the imported LEF file, and the router rules will be derived from the technology file section *tfNetRouteRule*.

Route vias has a higher priority than MCell vias if both of them exist.



-	Import LEF
Design File:	.torial/source/library/OpenCellLibrary.lef
Top Cell Name:	
Run Directory:	
Library Name:	OpenCellLibrary_lef
- Technology File-	
ASCII File:	/technology/OpenCellLibrary.tf
C Technology Lil	orary:
🖌 Create Pin Nam	e as Text
Text Layer Nam	e: Purpose Name:
Text Font Heigh	nt: 0.02
□ Snap Vertices t	o Min Grid Resolution
🗑 Overwrite Dupli	cated Information
🗌 Invoke Batch 🗠	lode
Cell Map File:	
Layer Map File:	/source/map/lef_layer.map
Log/Error File:	
	Apply OK Cancel

Figure 3: Import LEF Form

## 6 **Design Preparation**

The support of LEF/DEF flow provides the same essential kernel features for third party tools. In this lab, you will learn how to create a DEF design by referring LEF library

## 6.1 Lab-2: Design Preparation by DEF

In this lab, you will learn how to create a DEF In design library with a Laker library in abstract (abs) view.

#### 6.1.1 Import DEF Files

- 1. Define a cell library in the library mapping path using the Library → Mapping Path command. Make sure *OpenCellLibrary\_lef* is listed in the mapping path.
- Invoke the File → Import → DEF command to import a DEF design. Standard vias, custom vias, and the site information used in a DEF file are pre-defined in a corresponding LEF file. A correct Laker TF/LEF library is necessary for a successful DEF import task.
- 3. In the Import DEF form, complete the following steps:
  - a. Set Input File Name to Divide\_pl.def
  - b. Set Library Name to def\_in
  - c. Set Technology File → Attach to Library to OpenCellLibrary\_lef
  - d. Set Create Pin Name as Text → Text Font Height to 0.2
  - e. Enable Create Instance Connection Information



-	Impo	ort DEF				
Input File Name:	Divide_pl.def	:				
Run Directory:	/home/work/r	oute/ocdk/laker				
Library Name:	def_in					
-Technology File						
ASCII File:						
Attach to Libr	ary: Oper	nCellLibrary_lef				
Options Sections	1					
🗌 Define Cell Bou	undary Layer					
Layer Name:		Purpose Name:				
🗌 Create Net Na	me as Text					
Text Layer Na	me:	Purpose Name:				
Text Font Heig	ht: 1.0					
🕷 Create Pin Nar	m <b>e a</b> s Text					
Text Layer Na	me:	Purpose Name:				
Text Font Heig	ht: 0.2					
🗌 Update Top Ce	ell with Increr	mental Mode				
🖉 Create Instanc	ce Connectio	n Information				
□ Snap Vertices	to Min Grid I	Resolution				
Merge Continuous Wires to a Single Route						
🗌 Invoke Batch I	vlode					
Log/Error File:						
		Apply OK	Cancel			

Figure 4: Import DEF Form

4. Click **OK** to finish importing a DEF file.

[Note]: Remember that the logic view of the SDL flow is not created for pure DEF/DEF flow. Only a layout view is created after Import DEF.

[Note]: Row area created by DEF/LEF flow cannot be recognized by the Laker SDL flow. You can only use **Placer**  $\rightarrow$  **Place All** from the *Layout* window.

# 7 Post-Placement

#### 7.1 Lab-3: Add Core Fillers

Core filler insertion can be done before routing or after routing. The benefit of post-placement insertion is to enable better performance and database size without too many core filler cells in an ASIC chip design.

To add core fillers, follow the steps below:

- 1. Invoke the **Placer** → **Add Filler Cell** command.
- 2. In the Add Filler Cell form, set filler cell names by specifying Filler Cell → FILLER\*.

🖌 Add Fi	ller Cell			_ ×
Mode:	🔷 Full Cell	💠 Area		
Filler Cel	l: FILL*			
			ОК	Cancel

Figure 5: Add Filler Cell Form



3. Click **OK** to finish core filler insertion in a row area.

#### 7.1.1 PG Connection of Physical Cells

Power and ground ports of a physical only cell are floating because they are not defined during design import. You must connect the power and ground ports to the global PG nets.

- 1. Invoke the Router  $\rightarrow$  Digital Router  $\rightarrow$  Assign Instance Port to Net command.
- 2. Fill in instance names, power, and ground net/port names.
- 3. Click **OK** to assign global power and ground nets to a physical cell by cell type.

🗙 Assign Ins	tance Port to N	et	×	🗙 Assign Ins	tance Port to Net	×
Net:	VDD			Net:	VSS	
Instances:	♦ Names:	*		Instances:	♦ Names: ★	
	♦ File:				♦ File:	5
Port:	VDD			Port:	VSS	
		Apply OK Cancel	_		Apply OK Cancel	

Figure 6: Assign Instance Port to Net Form

#### 7.1.2 Connect PG Rails of Standard Cells

PG rails routing has an impact on routing resources and DRC checking in a limited layer design. It is recommended to finish PG rails before you start signal routing.

- 1. Invoke the customized **Router**  $\rightarrow$  **Digital Router**  $\rightarrow$  **PG Route** command.
- 2. Switch to the **Follow Pin** tab.

YPG Route	
General Core Ring Macro Ring Stripe Follow Pin	
Net Names: VDD VSS	I
Enable Layer Jump with 1 Via Array(s)	
Use Layers in Non-preferred Direction Extend to Boundary	
	Apply
Undo	Close

Figure 7: PG Route Form, Follow Pin Tab

# **SYNOPSYS**®

# 8 In-Route

## 8.1 Introduction

The Custom Digital Router flow is a series of routing kernels executed in a pre-defined sequence for global router, track assignment, detail route, violation check, violation fix, and notch gap filling.



Figure 8: Introduction of In-Route

## 8.2 Set Routing Layers

The Custom Digital features honor the Laker routing resource files for available routing layer planning.

When 4 metal routing layers (metal1 ~ metal4) are used, the 6 non-available metal routing layers (metal5 ~ metal10) have to be disabled in the Laker technology file.

- 1. Invoke the **Router**  $\rightarrow$  **Digital Router**  $\rightarrow$  **Rule Setting** command.
- 2. Disable availability of non-available layers and vias by clicking the **Avail** field of the **Metal** and **Via** tabs.
- 3. Click **Save** to save the 4 metal routing conditions to *default* for future use.
- 4. Click **Cancel** to close *Rule Setting* form.



	Me	etal				Vi	a	
Specific	Spacing Rule	1				<b></b>	1	
Avail	Layer	Direction	Width	Spacing	MWL	MSL	MWWSL	MAR
	dg poly	÷ ⊻	0.050	0.075	10.000	0.000	0.000	0.000
$\checkmark$	dg metal1	🔶 🝸	0.070	0.065	0.000	0.000	0.000	0.012
$\checkmark$	dg metal2		0.070	0.070	0.000	0.000	0.000	0.030
<b>~</b>	dg metal3	🔶 🗹	0.070	0.070	0.000	0.000	0.000	0.030
<b>~</b>	dg metal4		0.140	0.140	0.000	0.000	0.000	0.040
	dg metal5	🔶 🗹	0.140	0.140	0.000	0.000	0.000	0.040
	dg metal6		0.140	0.140	0.000	0.000	0.000	0.040
	dg metal7	🔶 🗹	0.400	0.400	0.000	0.000	0.000	0.600
	dg metal8	<u></u>	0.400	0.400	0.000	0.000	0.000	0.600
	dg metal9	🔶 <u>7</u>	0.800	0.800	0.000	0.000	0.000	0.800
	dg metal10	<b>♦</b> <u>7</u>	0.800	0.800	0.000	0.000	0.000	0.800

Figure 9: Rule Setting Form

## 8.3 Lab-3: Auto Route

In this lab, you will learn how to easily finish routing most typical designs.

#### 8.3.1 Digital Route

- 1. Invoke the **Router → Digital Router → Digital Route** command.
- 2. In the *Digital Route* form, set up global options as the default under the **General** tab.

🗙 Digital Route	la de la companya de
-Settings-	
Applied Nets: Nets	A A
Ignored Nets: Nets 🗹	<u> </u>
🗇 Routing Area:	
Global Rule: default 🔤 🔍	More>>
General Advanced Net Prior	ty Run Step Report
Run Threads: Auto	Preferred Routing Area: Auto
Routing Track: Auto	
Spine Routing Pattern	
Do Not Use Pins as Feedthrough Via Settings	
☐ Via Enclosed by Pins	Style of Vias: Single Via 💆
Do Not Use Wire Touch Pins	
Load Save Dump	Close

Figure 10: Digital Route Form, General Tab

- 3. On the *Digital Router* form, switch to the **Run Step** tab.
  - a. Enable the Initial Route and Detail Route procedures.
  - b. Enable the Post Optimization procedure (as the demo case is small).
  - c. Enable the **Double Via Insertion** procedure.



d. Enable the Notch Gap Filling procedure.

🗙 Digital Route	×
Settings	
Applied Nets: Nets	
Ignored Nets: Nets	
☐ Routing Area:	E
Global Rule: default 🝸 🔍	More>>
General Advanced Net Priority Run Step	Report
Initial Route	
Detail Route     On Track     No Pushing	Iteration: 5
Post Optimization     Detour     Pattern	Iteration: 3 1
Double Via Insertion	]
Notch Gap Filling	]
Default	Apply
Load Save Dump	Close

Figure 11: Digital Route Form, Run Step Tab

4. Click **Apply** to complete the auto routing tasks.

The **Post Route** option on the **Auto Route** tab is disabled by default to create a fast routing result for debugging once a routing problem is detected.



Figure 12: Routing Results

#### 8.3.2 Routing Quality of Result

- 5. Switch to the **Report** tab for reporting several routing quality results.
  - a. Enable **Route Information** to report wire and via statistics. Double cut rate per layer can be reported this way.



- b. Enable the Check Connectivity option to check routing connectivity.
- c. Enable **Jog Information** to get jog counts.
- d. Enable **Violations** and its sub-option **Show Violations** to bring up the *Error Viewer* form if any DRC violations are found.

Area:		
Global Rule: default 🗾 🔍		More>>
General Advanced I	Net Priority Run Step	Report
Design Information	Layout Data Validation	
Route Information     Connectivity     Nets with Detour Patio >= 2,000	Sub-optimal Patterns Antenna Rule Skin Brimitive Violations	
Jog Information     Corner Information	Show Violations	
J Output File:		
		Apply
Load Save Dump		Close

Figure 13: Digital Route Form, Report Tab

6. Click **Apply** to complete router verification tasks.



# **Revision History**

Revision	Date	Description	
7.2	02/05/13	Updated the footer information and fixed broken hyperlinks.	MY
7.1	12/26/12	Updated the header and footer information.	MY
7.0	03/28/11	Split the Custom Digital Tutorial as CDPR LEF/DEF Tutorial and CDPR_SDL Tutorial, and updated the tutorial contents. Based on Laker OA2011.03.	HLH
6.0	12/16/10	Added an Overview section.	Rich Morse
5.0	11/02/10	Updated "Lab-1B: Foundry DRC rules".	HSW
4.0	09/09/10	Updated Model Map file section for Laker OA2010.08. Add LEF/DEF flow for Laker OA.	HSW
3.0	08/05/10	Updated tutorial materials.	HSW
		Removed Tcl scripts which are supported by Laker2010.07 features. For example, Pin Placer, etc.	
		Updated Laker OA incremental Tech.	
		Updated notch gap fill.	
2.0	06/11/10	Changed DigitalRouteAll to CustomDigital.	HSW
		Changed routing track definition of OpenCellLibrary.tf for better hierarchical layout implementation.	
1.6	04/16/10	Added a limitation of PG routing with read only LEF master library.	HSW
1.5	04/13/10	Added details to Introduction, modified Verilog Import, and added SPINE. Based on Laker 2010.03.	HSW
1.4	3/31/10	Update OpenCellLibrary source file, change menu name to CustomDigital, add Main window menu. Based on Laker 2010.03.	HSW
1.3	3/23/10	Added cell level ESD spacing. Based on Laker 2010.03.	HSW
1.2	3/18/10	Added Cell level OD spacing and overlap. Based on Laker 2010.03.	HSW
1.1	3/11/10	Added a technology file preparation section. Based on Laker 2010.03.	HSW
1.0	3/1/10	Initial release. Based on Laker 2010.03.	HSW

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