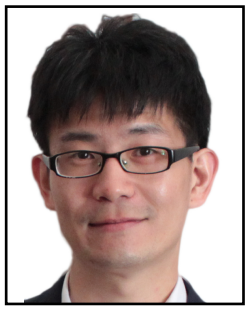
Session 21 Overview: *Audio Amplifiers*

ANALOG SUBCOMMITTEE



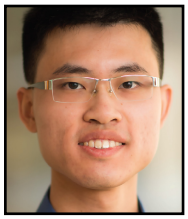
Session Chair: Shon-Hang Wen
MediaTek, Hsinchu, Taiwan

Session Co-Chair: Chinwuba Ezekwe
Robert Bosch, Sunnyvale, CA

This session highlights the continuing advances in audio amplifiers to enable improvements in their performance, efficiency, and cost. The techniques revealed include the use of HV tri-level IDAC units with an ISI-mitigating RTDEM scheme to improve the DR of a 14.4V filterless Class-D amplifier (Paper 21.1), and the use of input feedforward and two passive PWM aliasing-reduction schemes to improve the wideband linearity of a filterless Class-D amplifier (Paper 21.2). Also included are the use of current feedback to relax the linearity and tolerance of the LC components of a feedback-after-LC Class-D amplifier to save PCB area and BOM cost (Paper 21.3), and the combination of SIMO power-conversion and several analog techniques in a Class-H amplifier to improve efficiency, linearity, and BOM cost (Paper 21.4).

979-8-3503-0620-0/24/$31.00

8:00 AM



21.1 A 121.7dB DR and -109.0dB THD+N Filterless Digital-Input Class-D Amplifier with an HV Multibit IDAC Using Tri-level Output and Employing a Transition-Rate-Balanced Bidirectional RTDEM Scheme

Huajun Zhang, Delft University of Technology, Delft, The Netherlands

In Paper 21.1, Delft University of Technology and Goodix Technology present a filterless digital-input Class-D audio amplifier. The amplifier achieves 121.7dB DR and -109.0dB peak THD+N using HV tri-level IDAC units combined with a transition-rate-balanced bidirectional RTDEM scheme.

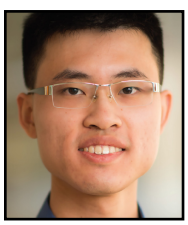
8:25 AM

21.2 A 0.81mA, -105.2dB THD+N Class-D Audio Amplifier with Capacitive Feedforward and PWM-Aliasing Reduction for Wide-Band-Effective Linearity Improvement

Kaiwen Zhou, Fudan University, Shanghai, China

In Paper 21.2, Fudan University presents a filterless Class-D audio amplifier. The amplifier employs a capacitive feedforward technique and PWM-aliasing reduction to achieve -105.2dB THD+N.

8:50 AM

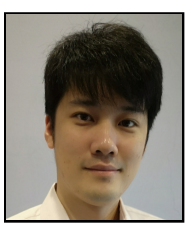


21.3 A -106.3dB THD+N Feedback-After-LC Class-D Audio Amplifier Employing Current Feedback to Enable 530kHz LC-Filter Cut-Off Frequency

Huajun Zhang, Delft University of Technology, Delft, The Netherlands

In Paper 21.3, Delft University of Technology and Goodix Technology present a feedback-after-LC Class-D audio amplifier. The amplifier uses current feedback to achieve -106.3dB THD+N with a 530kHz LC filter cut-off frequency.

9:15 AM



21.4 A -108dBc THD+N, 2.3mW Class-H Headphone Amplifier with Power-Aware SIMO Supply Modulator

Chuan-hung Hsiao, MediaTek, Hsinchu, Taiwan

In Paper 21.4, MediaTek reveals a Class-H headphone amplifier. The amplifier uses a SIMO converter to enhance envelope tracking accuracy and an improved CMFB circuit to reduce supply-induced distortion to achieve -108dBc THD+N.

21.1 A 121.7dB DR and -109.0dB THD+N Filterless Digital-Input Class-D Amplifier with an HV Multibit IDAC Using Tri-level Output and Employing a Transition-Rate-Balanced Bidirectional RTDEM Scheme

Huajun Zhang*[1], Mingshuang Zhang*[1], Mengying Chen[1], Arthur Admiraal[1], Miao Zhang[1], Marco Berkhout[2], Qinwen Fan[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Goodix Technology, Nijmegen, The Netherlands
*Equally Credited Authors (ECAs)

Digital-input Class-D amplifiers (CDAs) are widely used in audio applications and offer high power efficiency and high levels of integration. As human ears have a dynamic range (DR) of ~130dB, high DR is preferred in high-performance audio CDAs, and low THD+N is required for sound fidelity. Prior digital-input CDAs often employ multi-bit resistive DACs (RDACs) [1] or current-steering DACs (IDACs) [2], but their DR and THD+N are limited to ~115dB and ~-98dB respectively. In [3], a capacitive-DAC-based digital-input CDA achieves high DR (120.9dB) and low THD+N (-111.2dB). However, it is only suitable for CDAs employing an LC filter and, therefore, does not support the low-cost filterless configuration. IDACs using tri-level unit cells can potentially offer higher DR than their 2-level IDAC and RDAC counterparts, but they exhibit inferior linearity that can result in high THD+N, e.g., only -93dB THD+N in [4]. This paper presents a 14.4V filterless digital-input CDA that achieves high DR and low THD+N by employing a high-voltage (HV) multi-bit IDAC with tri-level unit cells. To overcome nonlinearity due to mismatch and ISI, a transition-rate-balanced bidirectional real-time (RT) DEM scheme is introduced. Implemented in a 0.18µm BCD process, the prototype achieves 121.7dB DR, -104.0dB, and -109.0dB peak THD+N for 1kHz and 6kHz signals, respectively. Furthermore, it can deliver 12.7W at 10% THD into an 8Ω load with 90% efficiency.

The system block diagram of this CDA is shown in Fig. 21.1.1. The digital audio input is first up-sampled to f_S=768KHz (16×48kHz) and then truncated to 5 bits by a 6th-order digital ΔΣ modulator (DSM), which achieves an SQNR of 130.9dB with a maximum stable amplitude (MSA) of 95%FS. The DSM output D_{IN} is then converted into the analog domain by a multi-bit IDAC. The latter drives a closed-loop CDA that includes a 3rd-order loop filter, a PWM modulator, an HV (14.4V) 2-level output stage operating in fully differential mode, and feedback resistors (R_{FB}). To achieve a signal-to-jitter-noise ratio (SJNR) of 128.9dB with 10ps of white clock jitter on fs [1], a 33-level IDAC is chosen. The DAC current is defined by an external reference voltage and an on-chip resistor of the same type as that of R_{FB}, such that the output amplitude of the CDA is PVT-independent.

Using tri-level IDAC cells can significantly improve the CDA DR since most IDAC cells are disconnected from the loop filter and do not contribute noise at small signal levels [4]. However, this means the CM voltage of the CDA virtual ground ($V_{XP/N,CM}$) is defined by that of the output stage (7.2V in this work). Using pull-down resistors [1] or a current DAC-based common-mode (CM) regulation loop [2] can reduce $V_{XP/N,CM}$ so that the loop filter and the DAC can be implemented completely in a low-voltage (LV) domain. However, this negates the tri-level IDAC cells' noise benefit due to the noise generated by the pull-down resistors or the CM regulation loop. In this work, an HV input stage for the 1st integrator OTA, together with HV tri-level IDAC cells, is employed to maximize DR. The DAC and the 1st integrator draw 375µA and 1.4mA from the HV supply, respectively, which in total accounts for only <8% of the CDA idle power. Due to the bond-wire parasitic inductances and high di/dt of the switching output stage, the output stage HV supply exhibits aggressive ringing on-chip. To isolate this switching noise from the DAC cells and the 1st integrator, their HV supply is directly connected to the external 14.4V via a separate bond pad and bond wire. The rest of the loop filter is implemented in the 1.8V domain.

To mitigate DAC mismatch, an RT DEM [5] is employed, which effectively suppresses mismatch errors even with a relatively low oversampling ratio (19.2 in this work). However, for an IDAC using tri-level cells, the standard RT DEM alone suffers from severe ISI distortion. Since the DAC cells only switch between +1 and 0 when the input data is positive and between 0 and -1 when the input is negative, any ISI mismatch between "+1" and "-1" introduces signal-dependent distortion. In this work, a transition-rate-balanced bidirectional RT DEM is introduced to mitigate this issue, which is illustrated in Fig. 21.1.2. To balance the number of each type of transition (0 to +1, +1 to 0, 0 to -1, and -1 to 0) under different input polarities, a dummy pattern of (+1, 0, -1, 0) is added at the end of each DAC code ≥0, and (0, +1, 0, -1) at the beginning of each DAC code <0, as shown in Fig. 21.1.2 (middle). The dummy pattern rotates through all the elements with the original thermometer code without altering the total DAC output current. In 100 Monte-Carlo simulations that include only ISI errors, this reduces the worst-case distortion by 27dB compared to a conventional RT DEM. To realize 33 output levels, 16 tri-level unit cells are required. With the added dummy pattern, a total of 20 unit cells are employed, and their input codes are rotated at 20×f_S. The "+1" and "-1" in the dummy pattern slightly increase the DAC's output noise, but this is 5.5× less compared to the thermal noise of the CDA.

Moreover, instead of using a fixed direction of rotation as in a conventional RT DEM [5], a bidirectional RT DEM is employed, where the direction of rotation is reversed every other cycle, as shown in Fig. 21.1.2 (bottom). This bidirectional RT DEM scheme produces double-sided PWM signals driving each DAC cell, which has lower PCM-to-PWM distortion compared to the single-sided PWM signals produced by the conventional RT DEM [6]. Since the DAC mismatch causes this PCM-to-PWM distortion to leak into the output [5], the bidirectional scheme has lower residual mismatch distortion. A Monte Carlo simulation with only DAC cell mismatches shows that the residual distortion for a -1dBFS input is improved by 13dB when the bidirectional RT DEM is used. It should be pointed out that the bidirectional RT DEM effectively reduces the RT DEM's PWM frequency by 2×, resulting in some quantization noise folding. However, this only leads to an insignificant increase in the quantization noise floor (<2dB) and hardly affects the thermal-noise-limited DR.

Figure 21.1.3 shows the HV IDAC. D_{IN} is processed by RT DEM logic, retimed by MCLK, and buffered by DAC drivers to control the 20 HV tri-level DAC cells. Each DAC cell consists of complementary current sources implemented by 1.8V transistors and six 1.8V DAC switches. The former is source-degenerated by 270kΩ poly resistors and cascoded by 5V I/O transistors. Thanks to source degeneration, thermal and 1/*f* noise from the 1.8V transistors are largely suppressed. For compact area and better matching, all NMOS current sources share one HV isolation ring, and so do all PMOS ones. To achieve a high large-signal SNR (~118dB), 2nd-order RC filters are employed on-chip in the biasing circuitry, occupying an area of 0.13mm^2 (1.7% of the total die size).

To allow direct interfacing of the DAC output to $V_{XP/N}$, a CM reference (PVCM = 7.2V) is generated on-chip and shared by all the DAC cells, which serves as the throw-away point for the IDAC current in state "0" and a local supply for the DAC switch drivers as shown in Fig. 21.1.3. The control signals of the DAC switches, implemented by 1.8V devices, must be level-shifted to around PVCM. To save static power, capacitive level shifters [7] can be used, requiring two HV low-density MOM capacitors for each DAC switch, potentially occupying a relatively large area. In this work, an area-efficient level shifter is introduced. As shown in Fig. 21.1.3, two LV floating voltage domains are created by C_{FP} and C_{FN} around PVCM for the PMOS and NMOS DAC switches, respectively, and shared across all DAC cells. They are implemented by MIM capacitors and stacked on top of the DAC switches, thus consuming no extra chip area. Each level shifter includes a latch to maintain the switch control signal. Thus, to level shift the 1.8V switch control signals, only one HV MOM capacitor $C_{1N/P}$ is needed. To minimize the disturbance of the tail current sources due to charge injection and clock feedthrough, the 1.8V clock signal is attenuated to 1.2V using a capacitive divider with $C_{1N/P}$:$C_{2N/P}$=2:1. The DAC drivers, $C_{1N/P}$, and latches also function as charge pumps, thus automatically establishing 1.2V across $C_{FN/P}$. Thanks to the transition-rate-balanced RT DEM scheme, at least one DAC cell always switches. Thus, the charge in $C_{FN/P}$ is constantly refreshed.

The CDA prototype is fabricated in a 0.18µm BCD process and occupies a die area of 7.9mm^2. The 24-bit digital input source and the CDA output measurement are both provided by the APx555 audio signal analyzer, with FPGA-based interpolation filter and digital DSM. The CDA is loaded with 8Ω+44µH, which represents the speaker. Figure 21.1.4 shows the measured FFT spectra when the CDA delivers a 1kHz sinewave. A THD+N of 102.3dB is achieved at 1W. At -60dBFS input, an SNR of 61.7dB is measured, indicating a DR of 121.7dB. Figure 21.1.5 (top) shows the measured THD+N vs. output power, demonstrating a peak THD+N of -104.0dB and -109.0dB for 1kHz and 6kHz inputs, respectively. Figure 21.1.5 (bottom) plots the PSRR and power efficiency. The CDA achieves 93dB of PSRR at 217Hz and a peak efficiency of 90%.

Figure 21.1.6 compares the performance of this work with state-of-the-art digital-input CDAs using IDAC or RDAC. It achieves the highest DR by >6.2dB. Thanks to the transition-rate-balanced bidirectional RTDEM scheme, its THD+N is >6.8dB and >11.3dB lower compared to other HV CDAs for 1kHz and 6kHz signals, respectively. Compared to an LV CDA employing tri-level IDAC cells [4], it achieves 8.7dB higher DR, and 11dB and 19dB better peak THD+N for 1kHz and 6kHz signals, respectively.

References:

[1] E. Cope et al., "A 2×20W 0.0013% THD+N Class-D Audio Amplifier with Consistent Performance up to Maximum Power Level," *ISSCC*, pp. 56-57, Feb. 2018.
[2] D. Schinkel et al., "A Multiphase Class-D Automotive Audio Amplifier With Integrated Low-Latency ADCs for Digitized Feedback After the Output Filter," *IEEE JSSC*, vol. 52, no. 12, pp. 3181-3193, Dec. 2017.
[3] H. Zhang et al., "A 120.9dB DR, -111.2dB THD+N Digital-Input Capacitively-Coupled Chopper Class-D Audio Amplifier," *ISSCC*, pp. 54-55, Feb. 2023.
[4] A. Matamura et al., "An 82mW ΔΣ-Based Filter-Less Class-D Headphone Amplifier with -93dB THD+N, 113dB SNR and 93% Efficiency," *ISSCC*, pp. 432-433, Feb. 2021.
[5] E. v. Tuijl et al., "A 128fs Multi-Bit ΣΔ CMOS Audio DAC with Real-Time DEM and 115dB SFDR," *ISSCC*, pp. 368-369, Feb. 2004.

 979-8-3503-0620-0/24/$31.00

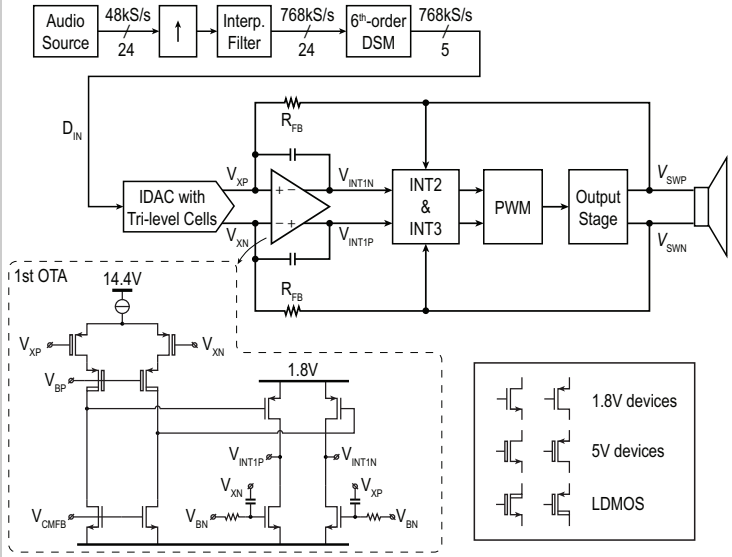


Figure 21.1.1: Overview of this CDA with an HV multibit IDAC using tri-level outputs.

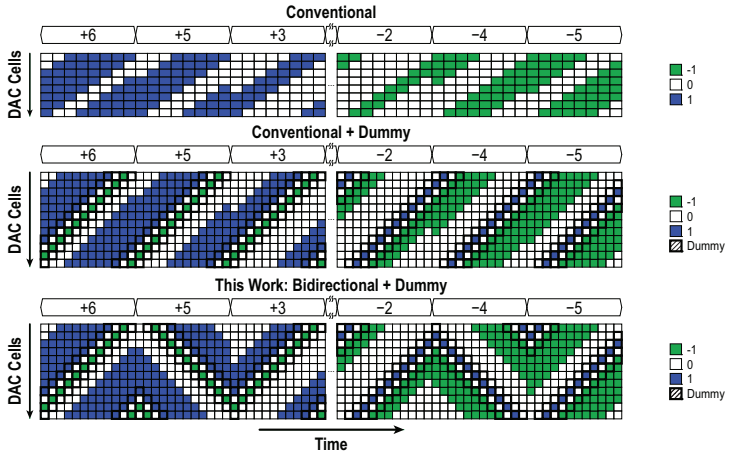


Figure 21.1.2: RT DEM schemes for a multibit IDAC with tri-level unit elements.

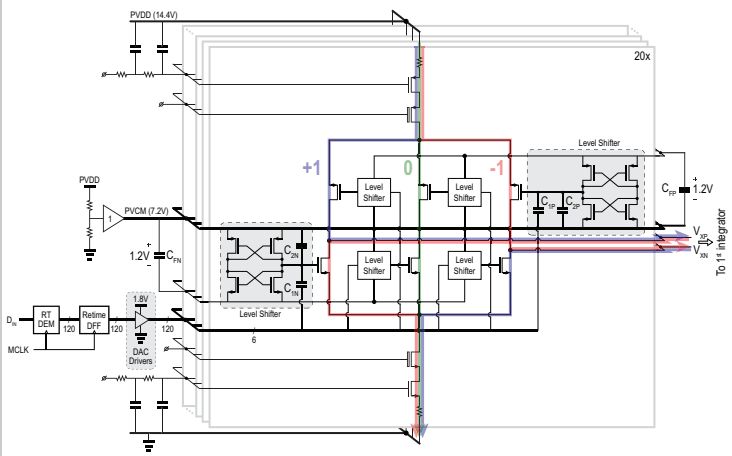


Figure 21.1.3: Schematic of the HV IDAC with tri-level unit elements.

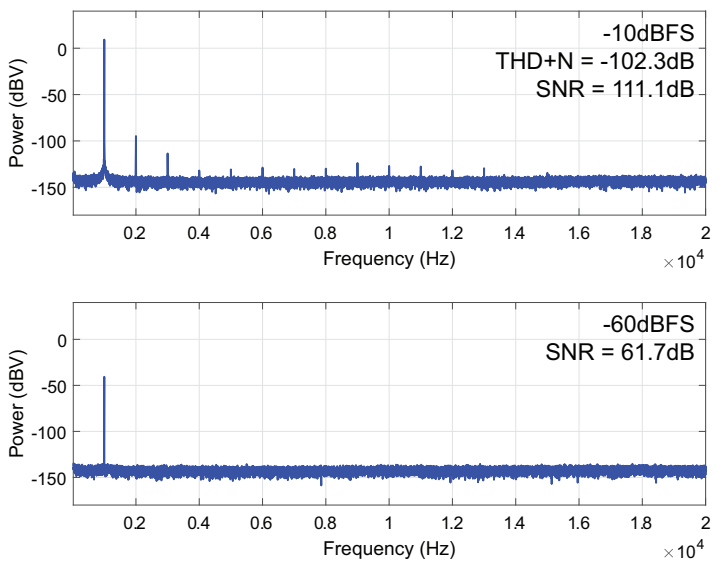


Figure 21.1.4: Measured output spectra (128-point FFT, 4× averaged).

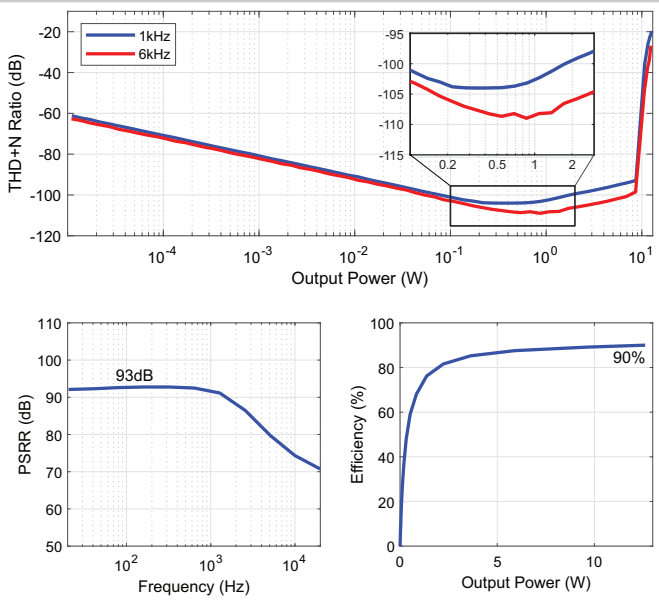


Figure 21.1.5: Measured THD+N vs. output power, PSRR, and power efficiency.

	This Work	A. Matamura ISSCC 2021 [4]	E. Cope ISSCC 2018 [1]	D. Schinkel JSSC 2017 [2]	T. Ido ISSCC 2006 [8]
Process	**180nm BCD**	40nm CMOS	180nm BCD	140nm BCD	-
Area (mm^2)	**7.9**	1.33	4.3	-	23(1)
DAC Type	**Tri-level IDAC**	Tri-level IDAC	RDAC	2-level IDAC	2-level IDAC
Supply (V)	**14.4**	1.8	8~20	25	35
DR (dB)	**121.7**	113	115.5	115	113
Output Noise (μV_{RMS})	**8.0**	-	20	34	-
THD+N (dB) at 1kHz	**-104.0**	-93	-97.2(2)	-88.6	-94.9
THD+N (dB) at 6kHz	**-109.0**	-90(2)	-97.7	-90(2)	-90(2)
Efficiency	**90%**	93%	90%	>90%	81%
$I_{Q,PVDD}$ (mA)	**22**	1.23	20.5	-	-
R_{LOAD} (Ω)	**8**	16	8	4	4/6/8
$P_{OUT,MAX}$ (W)	**12.7**	0.086	20	80	130/99/74(1)
PSRR (Frequency [Hz])	**93~71 (20~20k)**	94 (1k)	80~50 (20~20k)	88~60 (100~20k)	-

(1) Output stage is off-chip
(2) Estimated from figure

Figure 21.1.6: Comparison with state-of-the-art digital-input CDAs using an IDAC or RDAC.

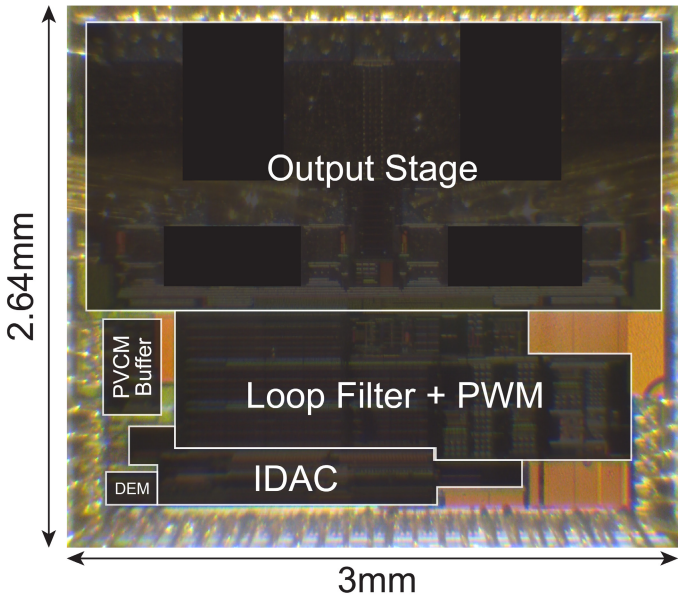


Figure 21.1.7: Die micrograph.

Additional References:
[6] K. Nielsen, "Audio Power Amplifier Techniques with Energy Efficient Power Conversion," Ph.D dissertation, Dept. of Applied Electronics, Technical Univ. Of Denmark, April, 1998. [online]. Available: osti.gov/etdeweb/servlets/purl/10147859
[7] Q. Fan et al., "A Capacitively Coupled Chopper Instrumentation Amplifier with a ±30V Common-Mode Range, 160dB CMRR and 5μV Offset," *ISSCC*, pp. 374-375, Feb. 2012.
[8] T. Ido et al., "A Digital Input Controller for Audio Class-D Amplifiers with 100W 0.004% THD+N and 113dB DR," *ISSCC*, pp. 1-2, Feb. 2006.

979-8-3503-0620-0/24/$31.00

21.2 A 0.81mA, -105.2dB THD+N Class-D Audio Amplifier with Capacitive Feedforward and PWM-Aliasing Reduction for Wide-Band-Effective Linearity Improvement

Kaiwen Zhou, Jianhong Zhou, Yuxiang Tang, Jiahua Li, Zhiliang Hong, Jiawei Xu

Fudan University, Shanghai, China

In Class-D audio amplifiers (CDAs), nonlinearity of power stages and pulse-width-modulation (PWM) modulators poses a main challenge in pursuit of high-fidelity audio output. The distortion is typically suppressed by a closed-loop topology with high in-band loop gain [1,2]. However, due to the roll-off of the loop gain, the total harmonic distortion plus noise (THD+N) of the CDA tends to increase at high frequency. Another source of distortion arises from the aliasing of high-frequency PWM residuals, which limits the minimum THD+N [3]. Although this can be improved by adopting a higher-order loop filter (LF) or a higher switching frequency (f_{SW}), both entail a trade-off between THD+N and quiescent power [3]. All of these raise the need to reduce distortion in an energy-efficient manner over a wider bandwidth of interest. State-of-the-art CDAs alleviated the PWM residuals aliasing by using replicated loop filters [3] or PWM residual-aliasing reduction (PRAR) [4]. The former exhibits low phase shift but higher power consumption while the latter does the opposite. By further combining the PRAR with frequency equalization [5], low THD+N with excellent power efficiency can be achieved. However, frequency equalization is highly dependent on the loop coefficient and requires complex equation solving, impairing the suppression of wide-band distortion.

This work describes a high-precision and power-efficient CDA (Fig. 21.2.1) that addresses the distortions from PWM modulation and residuals aliasing through three techniques: 1) a capacitive feedforward (CFF) path to mitigate input-dependent distortion caused by comparator delay; 2) 2nd-order PRAR with transfer function recovery (TFR) for steeper filtering and wider-band-effective linearity improvement; 3) a passive anti-PWM-aliasing filter (APAF) to further remove the PWM residuals with affordable hardware cost. As a result, the proposed CDA with a 2nd-order LF achieves a state-of-the-art THD+N of -105.2dB with a FOM_{THD+N} of 2119, and an A-weighted SNR of 112dB with a FOM_{SNR} of 4661. Furthermore, the CDA is capable of delivering a maximum output power of 1.76W into an 8Ω load under 5.5V supply.

Figure 21.2.2 shows the functional block diagram of CFF and illustrates its principle. In conventional PWM modulation, the loop-filter output (V_{LF+}) with the input signal swing is compared with a triangle wave ($V_{carrier+}$). Consequently, the crossing points of the comparator spread over the entire carrier range (1.375V to 4.125V, G_{PWM}=2, CDA gain=1), resulting in >50ns comparator delay variation and nonlinearity at full-scale input. To mitigate such input-signal-dependent distortion, we propose CFF to decouple the comparator delay from input-signal magnitude. The CFF generates a new carrier signal ($V_{carrier+}$) by superimposing the audio input signal on the triangle wave. The overall feedback of the CDA ensures that V_{LF+} is stable at V_{DD}/2=2.75V, thus keeping the crossing points of the comparator constant and independent of input signal fluctuations. As a result, the comparator delay variation is significantly reduced by 500× to <0.1ns even at full-scale input. The highpass corner of CFF is designed below 20Hz to prevent attenuating low-frequency audio signals. After enabling the CFF, the measured THD+N is improved by 10dB compared with conventional PWM modulation that is susceptible to comparator-delay variations. Additionally, the low output swing of the LF facilitates the use of power-efficient amplifiers with relaxed output headroom. Note that the CFF employs only coupling capacitors and bias resistors, which improves linearity with negligible noise and power.

Another source of distortion is the aliasing of PWM high-frequency components fed back to the LF. In [5], a 1st-order PRAR is proposed to reduce PWM residuals but suffers from increased THD+N at high-frequency inputs. To maintain low THD+N over the entire audio band, this work proposes a 2nd-order PRAR scheme with TFR. As illustrated in Fig. 21.2.1, the 2nd-order PRAR comprises two CFF PWM comparators and a 2nd-order bandpass RC network, exclusively permitting high-frequency PWM components to pass through as I_{PRAR}. Then the I_{PRAR} cancels the inverted-phase PWM residuals in the feedback current I_{FB}. Consequently, the current flowing through INT1, i.e., $I_{C1}=I_{R1}-I_{FB}+I_{PRAR}$, contains less PWM contents and thus mitigates aliasing. Compared to the 1st-order PRAR [4,5], the proposed 2nd-order PRAR with higher bandpass selectivity exhibits less leakage of audio band components, enabling more effective PRAR over a wide bandwidth, especially for high frequency response of audio signals. However, a remaining challenge of prior PRAR is that its transfer function $H_{PRAR}(s)$ also alters the main loop transfer function of the CDA from $V_{OUT}(s)=V_{IN}(s)$ to $V_{OUT}(s)=(1+H_{PRAR}(s))\cdot V_{IN}(s)$. This introduces errors $V_{IN}(t)*H_{PRAR}(t)$ at V_{OUT} and $V_{IN}(t)*H_{PRAR}(t)/G_{PWM}$ at V_{LF}, respectively. Although these errors can be compensated by frequency equalization [5], unfortunately it is only applicable to the 1st-order PRAR and requires complicated formula derivation. In contrast, as shown in Fig. 21.2.1, we address this challenge by using TFR, whose transfer function is $H_{TFR}(s)=-H_{PRAR}(s)/sR_8C_8$, and $R_8C_8=R_1C_1$ holds. The TFR replicates the same error produced by PRAR and cancels it at the input of INT2. In Fig. 21.2.3 (top right), the waveform diagram illustrates how the error is nulled by TFR to eliminate the PWM residuals in I_{C1}. The bode plot further verifies that the TFR can completely recover the original transfer function of $V_{OUT}(s)=V_{IN}(s)$. Since TFR utilizes the same $H_{PRAR}(s)$ network as the PRAR, both $H_{PRAR}(s)$ and $H_{TFR}(s)$ would experience the same process variations, resulting in more robust error compensation. The proposed TFR departs from frequency equalization [5] in that high-order $H_{PRAR}(s)$ can be compensated and this is independent from the main loop. The amplifier OP3 occupies the largest share of current from PRAR and TFR and it consumes 26μA, accounting for only 3.2% of the total current consumption.

In conventional LF design, increasing in-band loop gain is mainly achieved by designing a higher-order LF with extended unity-gain bandwidth. However, this would compromise the suppression of out-of-band PWM residuals and deteriorate aliasing distortion [3]. To break this trade-off of linearity, we introduce an APAF with its detailed schematic illustrated in Fig. 21.2.4. In addition to the pole constructed by INT2, C_2 and C_4 add two additional poles at 1.2MHz to filter high-frequency components. The loop gain versus frequency plot shows that enabling the APAF realizes -60dB/decade attenuation compared to the conventional case of -20dB/decade. In Fig. 21.2.4 (top right), the frequency-domain illustration and waveform diagram demonstrate a suppression of PWM residuals at V_{LF} and the aliasing distortion. The current I_{C2} passing through C_2 is less than 0.8μA (at full scale input) which is negligible for the OP1 output stage. Since the newly added poles are 11 times the 110kHz unity-gain bandwidth, there is no impact on the loop margin. Note that the fully passive APAF minimizes noise and power consumption with acceptable area penalty (1.9% of total active area).

The CDA was fabricated in a 0.18μm CMOS process, occupying an area of 2.6mm² (Fig. 21.2.7). It is worth noting that the proposed techniques occupy only 16.7% of the active area of 1.8mm² and consume only 6.9% of the total current of 0.81mA. The top of Fig. 21.2.5 shows the measured THD+N versus output power with 1kHz input. The minimum THD+N is -105.2dB when delivering 1W output power to an 8Ω load at 5.5V supply. This is a 24.2dB improvement over conventional CDA. The bottom of Fig. 21.2.5 shows the measured THD+N versus input frequency with -3dBFS input. The THD+N is below -100dB over the entire audio band. The maximum improvement of 31dB is achieved at 4kHz input.

The plots at the top of Fig. 21.2.6 compare this work with state-of-the-art CDAs by showing the measured minimum THD+N versus FOM_{SNR} and minimum THD+N versus worst-case THD+N over the audio band. As demonstrated, this work achieves a competitive THD+N of -105.2dB at the highest FOM_{SNR} of 4661, while the worst-case THD+N below -100dB from 20Hz to 20kHz is leading the results. The table at the bottom of Fig. 21.2.6 outlines the measured performance of this work and other state of the art. Thanks to the proposed power-efficient and wide-band-effective linearization techniques, the proposed CDA achieves the best performance of THD+N over the entire audio band with excellent power efficiency (FoM_{SNR}>4000 and FoM_{THD+N}>2000). It also achieves the lowest THD+N among CDAs utilizing 2nd-order LF.

Acknowledgement:
This work was supported by the State Key Laboratory of Integrated Chips and Systems, Fudan University.

References:

[1] M. Kinyua et al., "Integrated 105 dB SNR, 0.0031% THD+N Class-D Audio Amplifier with Global Feedback and Digital Control in 55 nm CMOS," *IEEE JSSC*, vol. 50, no. 8, pp. 1764-1771, Aug. 2015.
[2] W. Wang and Y. Lin, "A 118 dB PSRR, 0.00067% (-103.5 dB) THD+N and 3.1 W Fully Differential Class-D Audio Amplifier with PWM Common Mode Control," *IEEE JSSC*, vol. 51, no. 12, pp. 2808-2818, Dec. 2016.
[3] T. Kuo et al., "A 2.4 mA Quiescent Current, 1 W Output Power Class-D Audio Amplifier with Feed-Forward PWM-Intermodulated-Distortion Reduction," *IEEE JSSC*, vol. 51, no. 6, pp. 1436-1445, June 2016.
[4] S. Chien et al., "A Low Quiescent Current, Low THD+N Class-D Audio Amplifier with Area-Efficient PWM-Residual-Aliasing Reduction," *IEEE JSSC*, vol. 53, no. 12, pp. 3377-3385, Dec. 2018.
[5] Y. Qiu et al., "A 0.4-mA-Quiescent-Current, 0.00091%-THD+N Class-D Audio Amplifier with Low-Complexity Frequency Equalization for PWM-Residual-Aliasing Reduction," *IEEE JSSC*, vol. 57, no. 2, pp. 423-433, Feb. 2022.
[6] W. Sun et al., "A 121dB DR, 0.0017% THD+N, 8× Jitter-Effect Reduction Digital-Input Class-D Audio Amplifier with Supply-Voltage-Scaling Volume Control and Series-Connected DSM," *ISSCC*, pp. 486-487, Feb. 2022.
[7] J. Lee et al., "An 8Ω, 1.4W, 0.0024% THD+N Class-D Audio Amplifier with Bridge-Tied Load Half-Side Switching Mode Achieving Low Standby Quiescent Current of 660μA," *IEEE Symp. VLSI Circuits*, pp. 1-2, June 2020.

 979-8-3503-0620-0/24/$31.00

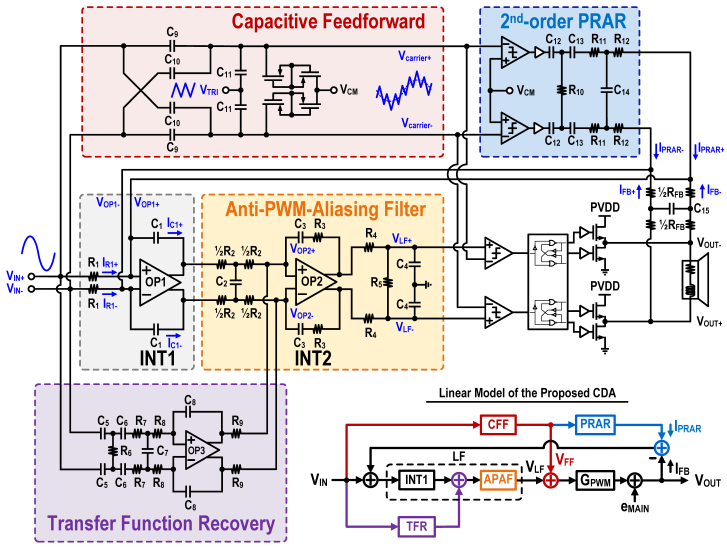


Figure 21.2.1: Block diagram of the proposed CDA with capacitive feedforward, 2nd-order PRAR, transfer function recovery and anti-PWM-aliasing filter.

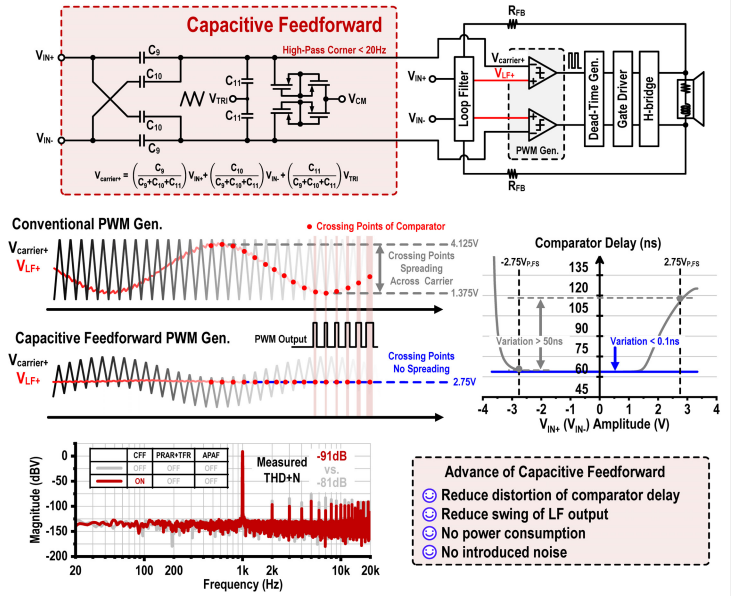


Figure 21.2.2: The proposed capacitive feedforward (CFF) technique.

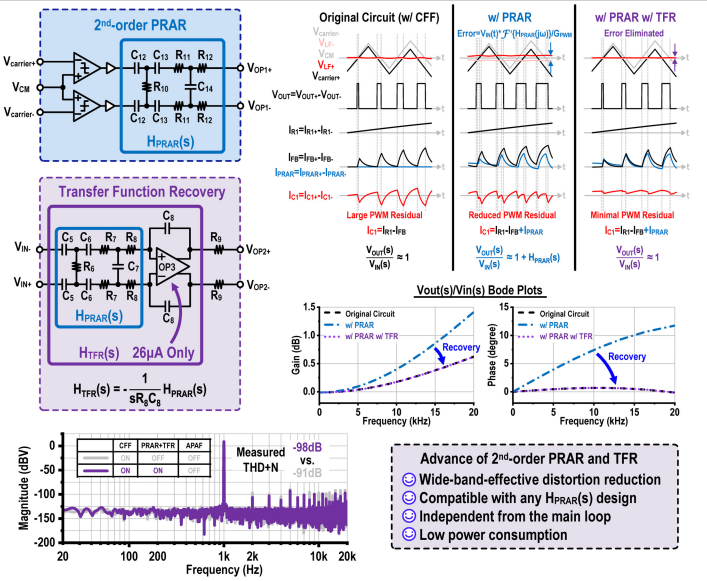


Figure 21.2.3: The proposed 2nd-order PRAR and transfer function recovery (TFR) technique.

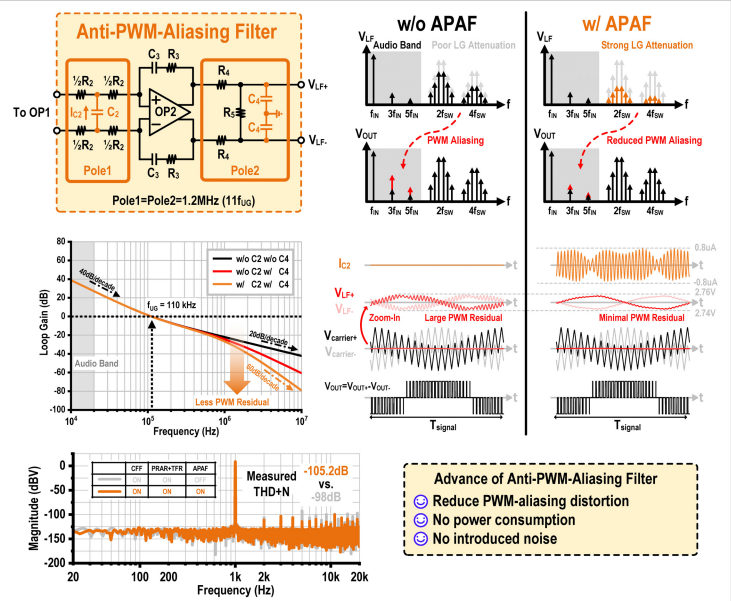


Figure 21.2.4: The proposed anti-PWM-aliasing filter (APAF) technique.

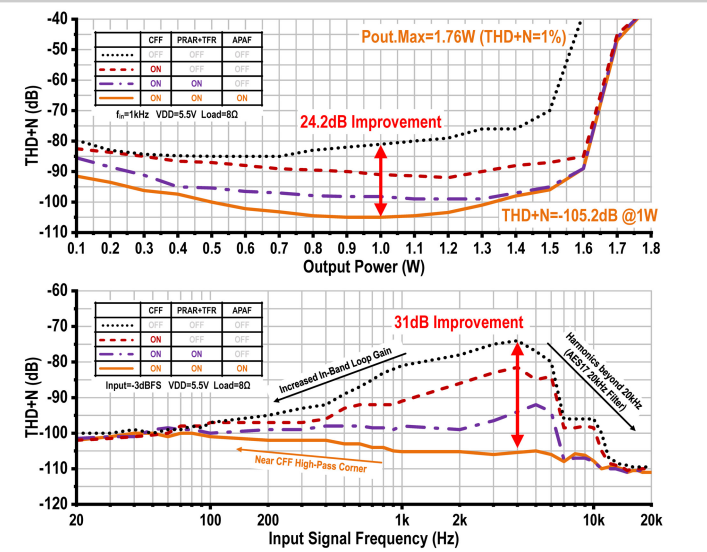
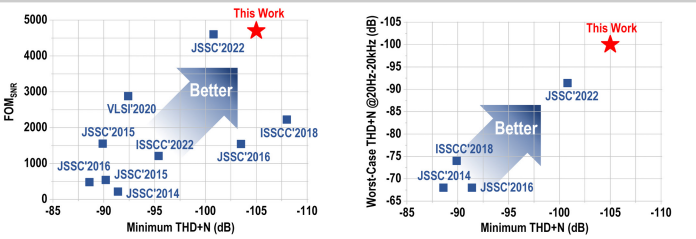


Figure 21.2.5: Measured THD+N vs. output power with and without the proposed techniques (top). Measured THD+N vs. input signal frequency with and without the proposed techniques (bottom).



	This Work	[6] Sun ISSCC'2022	[5] Qiu JSSC'2022	[7] Lee VLSI'2020	[4] Chien JSSC'2018	[8] Wang ISSCC'2018	[3] Kuo JSSC'2016	[2] Wang JSSC'2016	[1] Kinyua JSSC'2015	[9] Guo JSSC'2014
Supply Voltage (V)	2.5-5.5	0.625-5	2.5-5.5	3-5	2.5-5.5	3-5.5	2.5-5	3-5.5	2.5-5.5	1.2-4
A-wt. Peak SNR (dB)	112	102	106	106	104	112	102	108	105	97
Minimum THD+N (dB)	-105.2	-95.4	-100.8	-92.4	-89.9	-108	-88.6	-103.5	-90.2	-91.4
Worst-Case THD+N (dB) @20Hz-20kHz	-100	n/a*	-91.4	n/a*	-74	n/a*	-68	n/a*	n/a*	-68
Pout. Max (W) @1kHz THD+N=1%	1.76 (5.5V 8Ω)	1.5 (5V 8Ω)	1.42 (5V 8Ω)	1.4 (5V 8Ω)	1.45 (5V 8Ω)	3.15 (5.5V 4Ω)	1.02 (4.2V 8Ω)	3.1 (5.5V 4Ω)	1.5 (5V 8Ω)	0.85 (4V 8Ω)
Efficiency η (%)	94.4	92	92.3	95	94	89	92	89.5	85	94
PSRR (dB) @217Hz	85.6	100	100	80	81	118	72	118	92	101
I_Q (mA)	0.81	0.95	0.4	0.66	0.96	1.6	2.4	1.45	2.8	3.1
f_{SW} (kHz)	350	384	168	600	215	650	200	650	2133	320
Process (nm)	180	500	500	180	500	153	500	153	55	65
Chip Area (mm²)	2.6	4	1.56	0.83	0.91	2.28	0.86	1.85	1.17	1.69
Loop Filter's Order	2	5+2	2	3	2	3	2	3	4	4
FoM_{THD+N}**	2119	570	2536	600	306	1391	104	921	98	112
FoM_{SNR}***	4661	1211	4610	2879	1554	2225	479	1543	542	217

*Only measured at 1kHz input **$FoM_{THD+N} = \frac{\eta}{I_{Q|mA} \times THD+N|_{1kHz,min} \times 10^5}$ ***$FoM_{SNR} = \frac{\eta}{I_{Q|mA} \times SNR|_{A-wt} \times 10^5}$

Figure 21.2.6: Measured performance summary compared with state of the art.

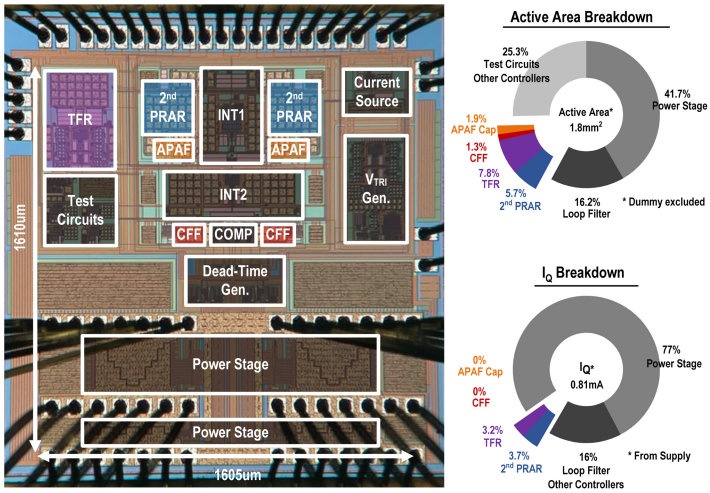


Figure 21.2.7: Die micrograph (left). Active area breakdown and I_Q breakdown (right).

Additional References:
[8] W. Wang and Y. Lin, "A 0.0004% (–108dB) THD+N, 112dB-SNR, 3.15W Fully Differential Class-D Audio Amplifier with Gm Noise Cancellation and Negative Output-Common-Mode Injection Techniques," *ISSCC*, pp. 58-59, Feb. 2018.
[9] L. Guo et al., "A 101 dB PSRR, 0.0027% THD + N and 94% Power-Efficiency Filterless Class D Amplifier," *IEEE JSSC*, vol. 49, no. 11, pp. 2608-2617, Nov. 2014.

979-8-3503-0620-0/24/$31.00

21.3 A -106.3dB THD+N Feedback-After-LC Class-D Audio Amplifier Employing Current Feedback to Enable 530kHz LC-Filter Cut-Off Frequency

Huajun Zhang[1], Haochun Fan[1], Miao Zhang[1], Marco Berkhout[2], Qinwen Fan[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Goodix Technology, Nijmegen, The Netherlands

Class-D amplifiers (CDAs) are used in various audio applications thanks to their high power efficiency. However, they produce high-frequency switching energy that poses EMI challenges. For applications such as automotive, the stringent EMI requirement necessitates the use of an LC filter, which can add significant bulk and cost. To reduce these, not only the LC component values but also their linearity requirements should be reduced. Moreover, a certain LC tolerance should be allowed for practical usage. In [1], high LC filter cut-off frequency (f_{LC}) (580kHz) is enabled, resulting in small LC component values. However, relatively expensive and bulky linear LC components are still required to achieve low THD+N due to a lack of LC nonlinearity suppression. Using a voltage feedback-after-LC architecture to suppress LC nonlinearity, the CDA in [2] enables the use of more nonlinear, smaller, and cheaper LC components and allows ±30% component tolerance. However, f_{LC} is greatly reduced (106kHz max.) due to a fundamental tradeoff between f_{LC} and LC nonlinearity suppression. Alternatively, current feedback can be applied to CDAs [3,4]. However, they employ bulky LC filters (e.g., f_{LC}≈20kHz in [3]), and analysis on LC nonlinearity suppression and tolerance is absent. In this work, current feedback is exploited in a feedback-after-LC CDA to maximize f_{LC}, achieve sufficient LC nonlinearity suppression, and allow good component tolerance. Implemented in a 180nm BCD process, the prototype enables a maximal f_{LC} of 530kHz while achieving –106.3dB peak THD+N, 12.8× inductor volume reduction compared to [2] and ±30% LC tolerance. The CDA can deliver 14W into an 8Ω load with 90% efficiency, measured at 10% THD.

Most feedback-after-LC CDAs employ voltage feedback, where an outer loop after LC suppresses the LC filter nonlinearity and an inner loop(s) before LC stabilizes the CDA [2,5]. Figure 21.3.1(top) shows a simplified block diagram of [2], where the inner loop consisting of a 1st-order lowpass filter forms a lead compensator. In the following analysis, the PWM modulator and the power output stage are combined and linearized as G_{PWM} [2], and the speaker is represented as R_{SPK} for conciseness. The unity-gain frequency of the inner loop f_U is limited to f_{PWM}/π [2], while the cross-over frequency f_{CROSS} of the inner loop gain (G_1) and outer loop gain (G_2) can be placed at below $f_U/2$ to achieve a ~60° phase margin (PM). The output stage nonlinearity $V_{NL,OS}$, is suppressed by (G_1+G_2), but the LC filter nonlinearity $V_{NL,LC}$, is only suppressed by $(G_1+G_2)/(1+G_1)$. As f_{LC} increases, G_2 in the audio band must decrease by 12dB per octave to maintain the same f_{CROSS} for the same PM while G_1 remains unchanged. As a result, $V_{NL,LC}$ suppression would quickly drop to ~0dB as G_2 drops below G_1. f_{CROSS} and f_{PWM} can be increased together to enable higher f_{LC}, but this increases idle power consumption.

Alternatively, a feedback-after-LC CDA can leverage current feedback [3], whose simplified block diagram is shown in Fig. 21.3.1(middle). As shown in the bode plot, restrictions among f_{CROSS}, f_{LC}, and f_U are similar to [2]. However, the inductor is incorporated in the current feedback, so its nonlinearity $V_{NL,L}$ is suppressed by G_1+G_2, which is $1+G_1$ times higher than [2]. The capacitor's nonlinearity, modeled as $I_{NL,C}$, gives rise to a voltage error $V_{NL,C}$ at V_{OUT} and is suppressed by $(G_1+G_2)/(1+G_1)$. Usually, G_1 in current feedback is much smaller than that in [2] as it only peaks around f_{LC} and decreases towards the audio band, working favorably for capacitor nonlinearity suppression. However, current feedback also boosts the impedance seen at the output of the inductor by G_1 (~20dB in [3]). Thus, a significant portion of $I_{NL,C}$ flows into R_{SPK}, resulting in a $V_{NL,C}$ much higher than that in [2], where most of $I_{NL,C}$ would flow to the low-impedance inductor instead. Another limitation of [3] is that the suppression of output stage nonlinearity is rather limited due to a relatively low G_2 (20dB).

This work addresses the abovementioned issues with two simple but effective system modifications, shown in Fig. 21.3.1(bottom). First, a PI compensator with a zero at f_{Z1} is employed to increase G_2 in the audio band to better suppress $V_{NL,OS}$ and $V_{NL,L}$. However, this also increases G_1, which is not desired for capacitor nonlinearity suppression. To reduce G_1 in the audio band, a highpass filter (HPF) with a corner frequency f_{HPF} of 90kHz is employed, reducing $V_{NL,C}$ by >13dB at 20kHz and more towards lower frequencies. The choice of f_{Z1} is a tradeoff between $V_{NL,OS}$ and $V_{NL,L}$ suppression and system stability, as a higher f_{Z1} can increase G_2 in the audio band but will decrease system stability as it approaches f_{CROSS}. The choice of f_{HPF} is a tradeoff between capacitor nonlinearity and system stability, as a higher f_{HPF} can reduce G_1 to boost $(G_1+G_2)/(1+G_1)$ but will reduce system stability since it adds a pole in the overall closed-loop system and can degrade stability as it approaches f_{CROSS}.

For practical use, the CDA is designed to maintain stable operation under a ±30% variation on the LC components [2]. Since the current feedback incorporates the inductor in the inner loop, the effects of L and C on system stability are different and, hence, should be analyzed and accommodated separately, which is illustrated in Fig. 21.3.2. The inner loop's unity-gain frequency, f_U, can be expressed as $G_{PWM}K_P\beta_{CFB}/2\pi L$. The smallest L is limited by $f_U < f_{PWM}/\pi$ (~1.5MHz in this design), and to allow a -30% inductance tolerance together with PVT variations, a nominal f_U of ~900kHz is chosen. The largest L is also limited since a larger L reduces the distance between f_U and f_{CROSS}, degrading PM as shown in Fig. 21.3.2 (left). Similarly, a smaller C moves f_{CROSS} closer to f_U, as shown in Fig. 21.3.2 (right). To accommodate a +30% change in L and -30% change in C values, f_{CROSS} is chosen to be ~380kHz. A +30% larger C is easier to achieve since it moves f_{CROSS} to a lower frequency, resulting in more PM. Under the above considerations, the CDA is designed to accommodate the following inductance and capacitance range (L: 470nH to 820nH; C: 190nF to 330nF), which yield a relatively wide f_{LC} tolerance from 297kHz to 530kHz for practical use cases.

A detailed circuit implementation of this CDA is shown in Fig. 21.3.3. The current feedback is realized by two sense resistors R_{SENSE} (~30mΩ), and a fully differential amplifier. The fully differential structure minimizes the high-voltage (HV) CM disturbance at the virtual ground of the amplifier. The sense resistors are placed after the inductors to minimize high-frequency interference from the HV switching nodes. The HPF is realized by R_1 = 98kΩ and C_1 = 18pF. To ensure sufficient suppression on the nonlinearity of the output stage (~-40dB) and the LC filter, G_1+G_2 should be at least 60dB to achieve -100dB of THD. Hence, two more integrators with local feedback through resistor R_{RES} are added [2], boosting the total output stage and inductor nonlinearity suppression to above 64dB in the audio band. A 3-level output stage is employed to minimize idle power [1]. To reduce process variation, the capacitors in the loop filter are 2-bit trimmable. To clearly demonstrate the stability of the 6th-order CDA (3 integrator poles + 2 LC poles + 1 HPF pole), a pole-zero plot of the closed-loop system's signal transfer function (STF) is shown in Fig. 21.3.3(bottom left) with various extreme LC combinations. The STF plot (Fig. 21.3.3 bottom right) demonstrates a flat transfer function in the audio band (within 0.008dB), and the NTF plots show the nonlinearity suppression of the output stage, the inductor ($NTF_{OS,L}$), and the capacitor (NTF_C).

The prototype CDA is implemented in a 180nm BCD process and occupies 7mm² (Fig. 21.3.7). The sense resistors are manufactured in the same process and occupy 0.67mm² each but are mounted between the inductors and capacitors on the PCB for the convenience of PCB routing. Figure 21.3.4(top) shows the measured FFT results with a 1kHz input. A peak THD+N of -105.0dB and -106.3dB with 1kHz and 6kHz signals is achieved, respectively, with an 8Ω load, as shown in Fig. 21.3.4(bottom). To demonstrate nonlinearity suppression, the THD+N results are measured both before and after the LC filter with linear and nonlinear LC components, where the LC filter nonlinearity is revealed in the former and the overall system linearity is demonstrated in the latter. It is shown that with linear LC, the THD+N with and without LC suppression do not differ much. Thanks to LC nonlinearity suppression, the THD+N with nonlinear LC components approaches that with linear ones, but the volume of the components, especially that of the inductor, is significantly reduced by 190× to only 2mm×1.25mm×1mm (in Filter B) from 8.4mm×7.9mm×7.2mm (in Filter A). It is also observed that the LC filter contributes less nonlinearity compared to [2], which is expected because as both L and C values become smaller, their effect in the audio band also gets reduced. The nonlinearity of the CDA is then mainly limited by the output stage. To verify f_{LC} tolerance (297kHz to 532kHz), Figure 21.3.5(top) shows the THD+N results with extreme LC combinations. The CDA's PSRR and power efficiency are shown in Fig. 21.3.5(bottom).

Figure 21.3.6 compares this CDA with the state of the art. This work achieves the highest f_{LC} (5× higher than [2] and 26× higher than [3]) and uses the smallest inductors (12.8× smaller than [2]) among all feedback-after-LC CDAs while achieving competitive THD+N. It is the only current feedback CDA that demonstrates LC nonlinearity suppression and tolerance. Finally, it offers competitive efficiency, idle power, and PSRR.

References:

[1] H. Zhang et al., "A High-Linearity and Low-EMI Multilevel Class-D Amplifier," *IEEE JSSC*, vol. 56, no. 4, pp. 1176-1185, Apr. 2021.
[2] H. Zhang et al., "A -121.5-dB THD Class-D Audio Amplifier With 49-dB LC Filter Nonlinearity Suppression," *IEEE JSSC*, vol. 57, no. 4, pp. 1153-1161, Apr. 2022.
[3] N. Anderskouv et al., "High-Fidelity Pulse-Width Modulation Amplifiers Based on Novel Double-Loop Feedback Techniques," *Proc. 100th AES Convention*, May 1996.
[4] J. H. Jeong et al., "A Class-D Switching Power Amplifier with High Efficiency and Wide Bandwidth by Dual Feedback Loops," *Int. Conf. Consumer Electronics*, pp. 428-429, June 1995.
[5] P. Adduci et al., "Switching Power Audio Amplifiers with High Immunity to the Demodulation Filter Effects," *J. AES*, vol. 60, no. 12, pp. 1015-1023, Dec. 2012.
[6] D. Schinkel et al., "A Multiphase Class-D Automotive Audio Amplifier with Integrated Low-Latency ADCs for Digitized Feedback After the Output Filter," *IEEE JSSC*, vol. 52, no. 12, pp. 3181-3193, Dec. 2017.

 979-8-3503-0620-0/24/$31.00

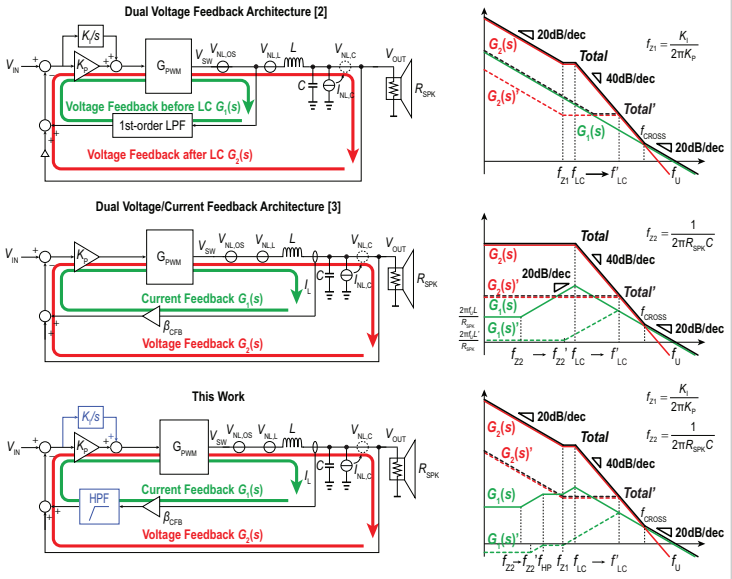


Figure 21.3.1: Class-D amplifier architectures with feedback after the LC filter.

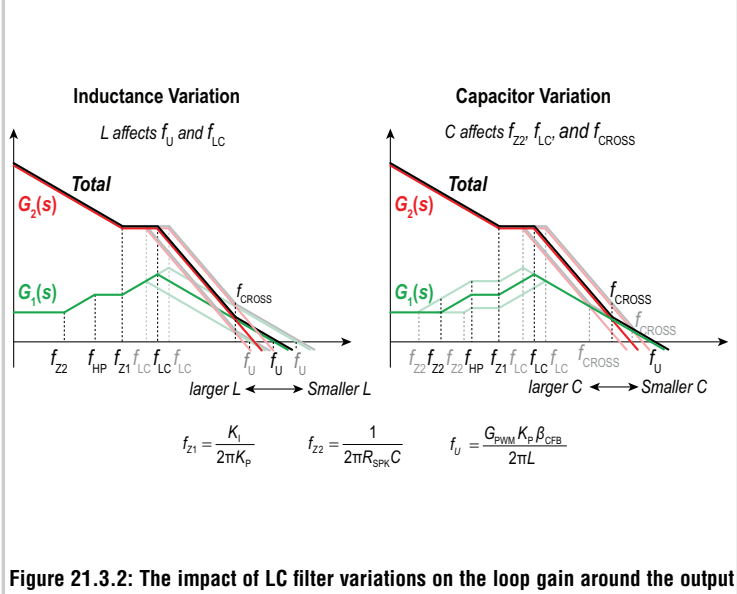


Figure 21.3.2: The impact of LC filter variations on the loop gain around the output stage for the CDA in this work.

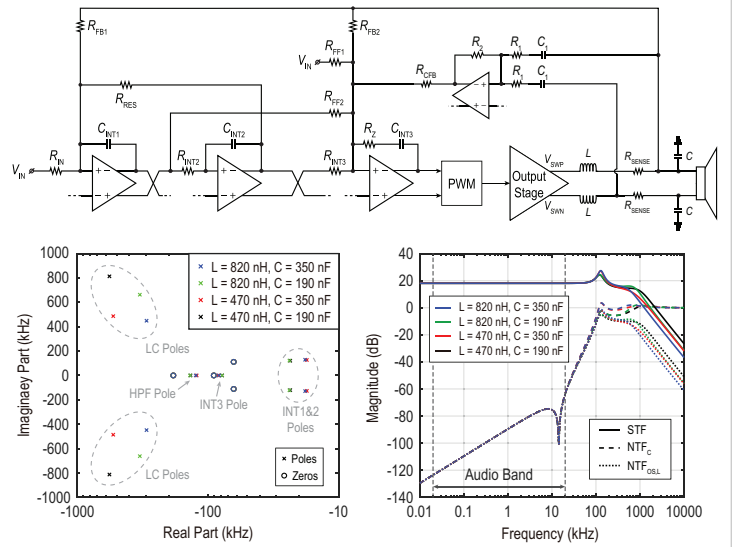


Figure 21.3.3: (Top) Schematic of the proposed CDA, (bottom left) pole-zero map under LC filter variations, and (bottom right) STF, and NTFs for error introduced by the output stage and LC filter inductor ($NTF_{OS,L}$) and capacitor (NTF_C).

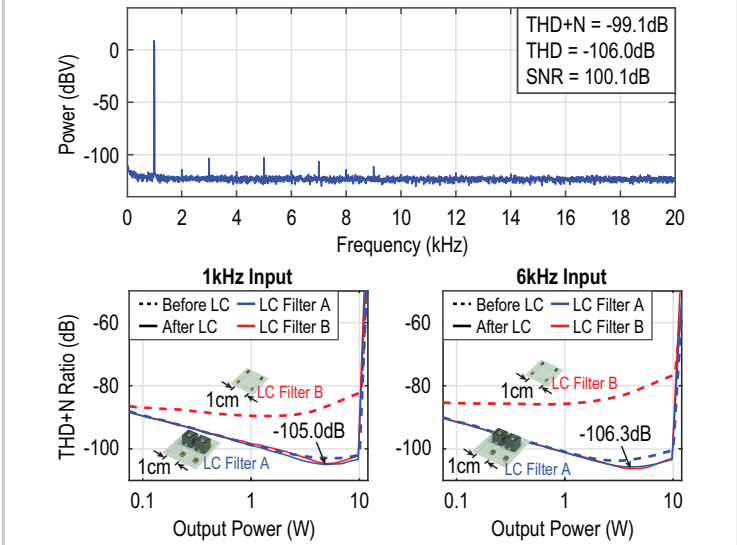


Figure 21.3.4: (Top) Measured 8k-point FFT at an output power of 1W, and (bottom) THD+N vs. output power measured at the input (before) and output (after) of the LC filter.

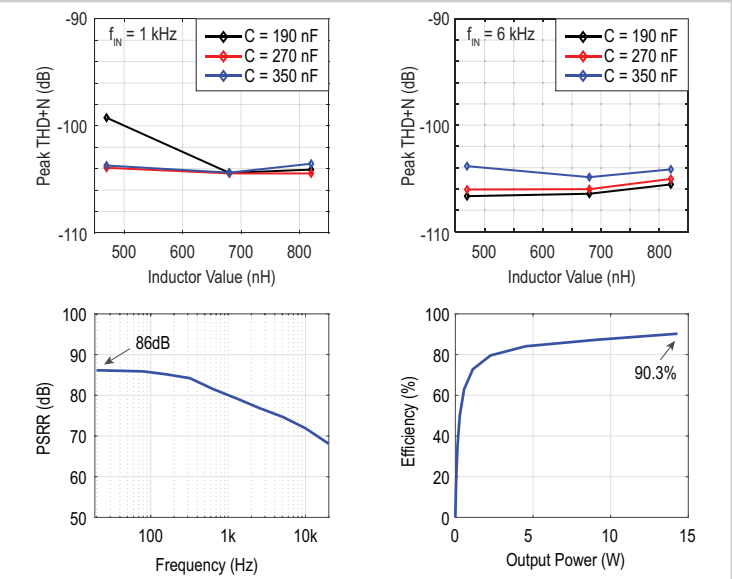


Figure 21.3.5: Measured (top) peak THD+N under LC variations, (bottom left) PSRR, and (bottom right) power efficiency.

	This work	Zhang JSSC'22 [2]	Zhang JSSC'21 [1]	Anderskouv J.AES'96 [3]	Schinkel JSSC'17 [5]	Adduci J.AES'12 [4]
Process	**180nm BCD**	180nm BCD	180nm BCD	-	140nm BCD SOI	-
Topology	**Current FB After LC**	Voltage FB After LC	Voltage FB Before LC	Current FB After LC	Voltage FB After LC	Voltage FB After LC
Supply Voltage (V)	**14.4**	14.4	14.4	70	14.4/25	25
R_L (Ω)	**8**	8	8	8/4	4	4
Efficiency	**90.3%**	91%	91%	90%	>90%	89%
$I_{Q,PVDD}$ (mA)	**7.6**	-	7	-	-	-
Idle Power (mW)	**133***	120	94	12000	-	-
Inductor Size (mm)	**2 x 1.25 x 1**	4 x 4 x 2	-	-	-	-
f_{LC} (kHz)	**297 ~ 532**	62 ~ 106	580	20	-	-
Peak THD+N at 1kHz (dB)	**-105.0**	-107.1	-107.8	-84.4	-87.9	-67.9
SNR (dB-A weighted)	**109.0**	110.0	109.7	113.0	115.0	110.0
Output Power (W)	**14**	14	14	200	80	-
PSRR (dB) (Frequency Range [Hz])	**86 ~ 68 (20 ~ 20k)**	70 ~ 58 (20 ~ 20k)	-	-	88 ~ 60 (20 ~ 20k)	-
f_{PWM} (KHz)	**4800**	4200	4200	630	500	352.8

*Total from 1.8V supply and 14.4V supply

Figure 21.3.6: Performance summary and comparison.

21

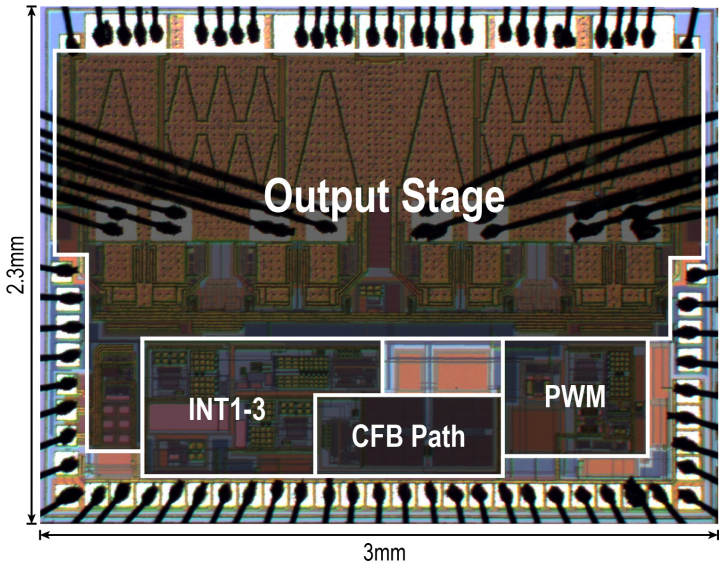


Figure 21.3.7: Die micrograph.

979-8-3503-0620-0/24/$31.00

21.4 A -108dBc THD+N, 2.3mW Class-H Headphone Amplifier with Power-Aware SIMO Supply Modulator

Shon-Hang Wen*, Chuan-Hung Hsiao*, Yi-Wei Huang*, Kuan-Yu Lin, You-Shin Chen, Ya-Chi Chen, Ming-Chung Tsai, Kuan-Hung Chen, Kuan-Dar Chen

MediaTek, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

Class-G/H amplifiers are becoming popular in modern mobile devices with diverse communication systems for their high efficiency and low EMI [1-4]. However, three design issues that arise for high-fidelity Class-G/H amplifiers are: 1) Inaccurate envelope tracking limiting achievable full-path efficiency [1-3]; 2) THD+N degradation due to limited PSRR in output drivers; and 3) Distortions at high temperature arising from the DAC reference bias drift caused by a high gate leakage in the advanced process [5]. In the first issue, to achieve high full-path efficiency, a supply modulator needs to efficiently generate precise positive and negative envelope-tracking supplies for ground-referenced audio outputs. Compared to the conventional Buck-NCP (negative charge-pump) cascade topology [1], which has limited efficiency for the negative supply due to the two-stage conversion, the single-stage multi-level charge-pump in [2,3] could generate both supplies more efficiently. However, the more than 1A of input peak current (I_{peak}) might cause serious electromigration and supply bouncing issues, restricting the envelope-tracking bandwidth [3]. In [2], the tracking bandwidth is 16Hz, thus limiting the full-path efficiency to 23.5% at 10mW output (1kHz). Additionally, the common constant ON-time (T_{ON}) discontinuous conduction mode (DCM) control scheme for buck converters can only optimize the efficiency in a narrow output voltage range, not suitable for wide-range supplies [6]. Second, the signal-dependent supply ripple at the high-frequency audio band might degrade THD+N seriously if the driver's PSRR is not sufficient, for which a higher CMFB loop gain is required [7]. However, such design might compromise the amplifier stability. Lastly, the gate leakage might cause serious reference bias drift and generate I_P/I_N mismatch in a tri-level DAC. In [5], the gate-leakage-compensated off-transistor-based bias noise filter is introduced to reduce the impact. However, if the resistance of an off-transistor is too large, the increased gate leakage at high temperature might saturate the compensation amplifier, leading to severe distortions. To solve the aforementioned issues: 1) a single-stage inductor-based supply modulator is introduced to relieve I_{peak} and then efficiently generate the fast envelope tracking at more than 1kHz, and a power-aware T_{ON} control scheme is leveraged to enhance the envelope-tracking accuracy for all output power levels as well, thus improving the efficiency to 34.8% at 10mW output (1kHz); 2) A gain-boosting CMFB circuit with a new frequency compensation scheme is presented to enhance the loop gain without sacrificing the amplifier stability; 3) An R_{OFF}-controlled technique is employed in the noise filter design to address the DAC reference bias drift and maintain the THD+N up to 85°C. Combining these techniques, the Class-H amplifier achieves -108dBc THD+N, 126dB DR, and 2.3mW quiescent power.

Figure 21.4.1 shows the block diagram of the Class-H amplifier. To save PCB area and BOM cost, a single-inductor multiple-output (SIMO) converter is used to generate one fixed negative supply (VSS) for analog DAC circuits, and two envelope-tracking supplies (PVDD and PVSS) for stereo headphone amplifiers. The controller in the SIMO converter detects signal levels in an audio memory beforehand, then provides target voltage references (VREF1/2/3) for VSS/PVDD/PVSS-comparators and corresponding control signals for power transistors respectively. Compared to the charge-pump topology [2,3], the inductor-based converter can control I_{peak} precisely by restricting the maximum T_{ON} in the DCM operation. Figure 21.4.2 shows the operation concept of the SIMO converter. If one of the output supplies is below its target voltage reference, the corresponding comparator will trigger the controller for charging the output. The VSS has the highest priority to ensure the normal operation. For example, if both VSS and PVSS are insufficient at the same time, the SIMO converter will store the energy into an inductor (L_{IND}) via path (1) and release it to VSS through path (2) first, and then charge PVSS in the next cycle. The T_{ON} event is triggered by comparator output and T_{ON} duration is controlled by the digital controller. A multi-input auto-zero zero-current detector (AZ-ZCD) is used to monitor the finish of the energy release and command the converter to enter the freewheeling state, thus effectively preventing the reverse inductor current and improving the efficiency. For a wide-range envelope-tracking supply from 0.3V to 1.8V (from silence to 62mW output), the conventional constant-T_{ON} scheme suffers limited efficiency at low power levels due to a long T_{ON}, which is required for the 62mW output power delivery. Moreover, for 0.1mW-to-10mW power levels, a fixed long T_{ON} design might overcharge output capacitors, causing high ripple loss in the power converter and large power dissipation in the output driver. To conquer the limitation, a digitally controlled power-aware T_{ON} control scheme [6] is leveraged to provide proper T_{ON} for different output power levels. A longer T_{ON} is used for a higher PVDD/PVSS level and vice versa, thereby greatly reducing the supply fluctuation and improving the envelope-tracking accuracy. In simulation, the power-aware T_{ON} control improves the current by 4.2mA, and the full-path efficiency by 12%, from 33% to 45% at 10mW, when compared to the constant-T_{ON} scheme.

The proposed gain-boosting CMFB circuit and its frequency compensation scheme are introduced in Fig. 21.4.3 (left). To enhance the CMFB loop gain against the supply ripple, a 3-stage CMFB amplifier is employed. In the conventional design, the transconductance of the CM-sense amplifier ($G_{m,CM}$) is not fully used since only one output ($M_{1,2}$) of the $G_{m,CM}$ is coupled to the main amplifier 1st-stage output (G_{m1}) through the current mirror (M_{5-7}) and the other output ($M_{3,4}$) is connected to a dummy diode-connected load. To improve the gain without increasing power, this design further connects the $M_{3,4}$ output to the G_{m1}. However, it extends the UGB and degrades the amplifier stability. Thus, a damping RC circuit is introduced to provide a pole-zero pair to control the UGB. Two capacitors are connected to the differential output of G_{m1} to form a large Miller capacitance, greatly filtering the $M_{1,2}$ signal component at higher frequencies and reducing UGB to $G_{m,CM}/(2C_{m1})$ as in the conventional design. In this work, the simulated CMFB loop gain is enhanced by 6dB over the audio band, improving supply-induced distortions by 7dB, from -106dBc to -113dBc, while driving 62mW into a 16Ω load.

The R_{OFF}-controlled noise filter to allow a high gate leakage current is illustrated in Fig. 21.4.3 (right). In an advanced process, gate leakage current increases exponentially with gate-source voltage and temperature [8]. The increased leakage current might saturate the compensation amplifier output (V_X) in [5] due to a large and uncontrollable off-resistance of the M_C, resulting in serious I_P/I_N mismatches in tri-level DACs and largely degrading THD+N. In simulation, the gate leakage increases from 30fA to 80fA as the temperature raises from 25°C to 85°C, degrading the THD+N to -98dBc. In this work, an R_{OFF}-controlled circuit is presented to control the off-resistance of the M_C within a desired range to minimize the V_X bias drift while still providing sufficient R_{OFF} for the noise filtering corner frequency of interest. The R_{OFF} is designed with a proper sizing ratio (N) to prevent the use of a tiny current reference (I_B). With the proposed circuit, the simulated V_X drift is controlled within 1mV and the THD+N is improved by 14dB, to -112dBc even with a 80fA gate leakage at 85°C.

The Class-H amplifiers, which include DACs, headphone drivers and the SIMO converter, are realized in a 28nm CMOS process. An NCP is also implemented to compare the power efficiency of Class-AB and Class-H operations. All measurements are done with a single-ended load of 16Ω||1nF. The measured THD+N sweep plot and FFT spectra with different temperatures are shown in Fig. 21.4.4. At 85°C , the increased gate leakage current causes severe harmonic and supply-induced distortions, degrading the THD+N to -97.8dBc. With the R_{OFF}-controlled technique, the distortions can be greatly mitigated and THD+N is improved to -107.5dBc. The measured THD+N and DR at 25°C are -108dBc and 126dB(A-weighted) respectively. Figure 21.4.5 shows measured supply current sweep plots and output waveforms. For a 1kHz and 10mW output, the power-aware Class-H improves the full-path efficiency to 34.8%, which is 14% and 7% higher than the Class-AB counterpart and constant-T_{ON} Class-H scheme respectively. As the output frequency increases from 20Hz to 10kHz, the voltage headroom and the tracking accuracy start to decrease since the minimum T_{ON} is limited by the comparator-to-controller delay of 135ns, thus degrading the efficiency. For 5% current tolerance in our system specification, the tracking bandwidth is 3kHz. Figure 21.4.6 summarizes the measured results and Fig. 21.4.7 shows the die photo. Among Class-G/H amplifiers with envelope-tracking supply modulators, this work improves the power consumption by 35% at 1mW when compared to the two-stage topology [1], and by 32% at 10mW (thanks to a higher tracking bandwidth) when compared with the single-stage work [2]. Moreover, the amplifier achieves comparable -112dBc THD and 126dB DR, as to the Class-AB prior-art [9], and consumes merely 2.3mW quiescent power, resulting in a 1.2× higher linearity FoM and 2.1× higher SNR FoM.

References:

[1] Texas Instruments, Class-G Directpath Stereo Headphone Amplifier, Rev. A, Aug. 18, 2009 [Online]. Available: http://www.ti.com/lit/ds/symlink/tpa6141a2.pdf

[2] Maxim, Low-Power, Low-Offset, Dual Mode, Class H DirectDrive Headphone Amplifier, Rev. 3, Aug. 21, 2012 [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/MAX97200.pdf

[3] S. Galal et al., "A 60 mW Class-G Stereo Headphone Driver for Portable Battery-Powered Devices," *IEEE JSSC*, vol. 47, no. 8, pp. 1921-1934, Aug. 2012.

[4] A. Lollio et al., "Class-G Headphone Driver in 65nm CMOS Technology," *ISSCC*, pp. 84-85, Feb. 2010.

[5] C. Lo et al., "10.1 A 116μW 104.4dB-DR 100.6dB-SNDR CT ΔΣ Audio ADC Using Tri-Level Current-Steering DAC with Gate-Leakage-Compensated Off-Transistor-Based Bias Noise Filter," *ISSCC*, pp. 164-165, Feb. 2021.

[6] C. Schaef et al., "A Fully Integrated Voltage Regulator in 14nm CMOS with Package Embedded Air-Core Inductor Featuring Self-Trimmed, Digitally Controlled Variable On-Time Discontinuous Conduction Mode Operation," *ISSCC*, pp. 154-155, Feb. 2019.

[7] W. Wang et al., "A 118dB-PSRR 0.00067% (-103.5dB) THD+N and 3.1W Fully Differential Class-D Audio Amplifier with PWM Common-Mode Control," *ISSCC*, pp. 90-91, Feb. 2016.

 979-8-3503-0620-0/24/$31.00

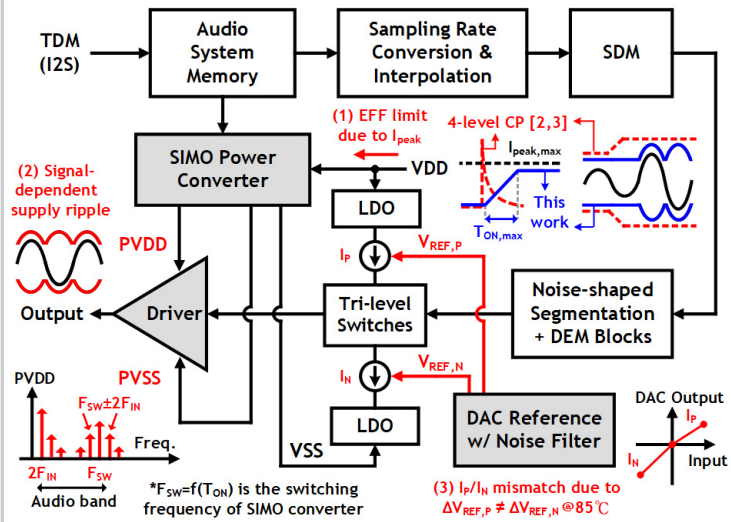


Figure 21.4.1: The block diagram of the Class-H amplifier.

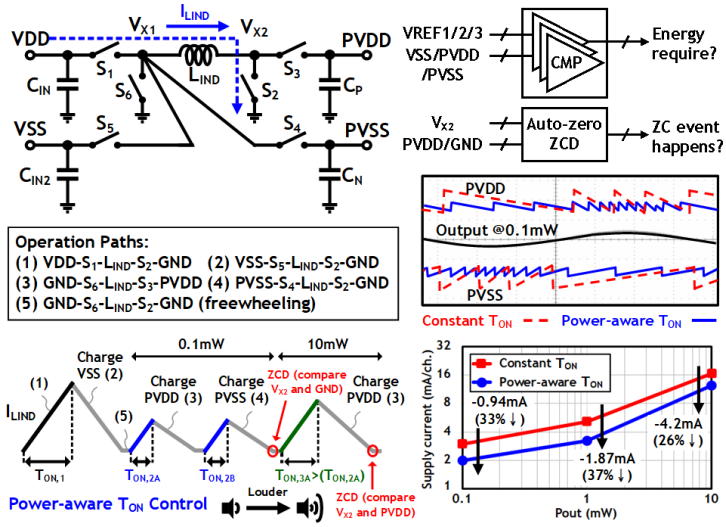


Figure 21.4.2: The power-aware SIMO envelope-tracking supply modulator.

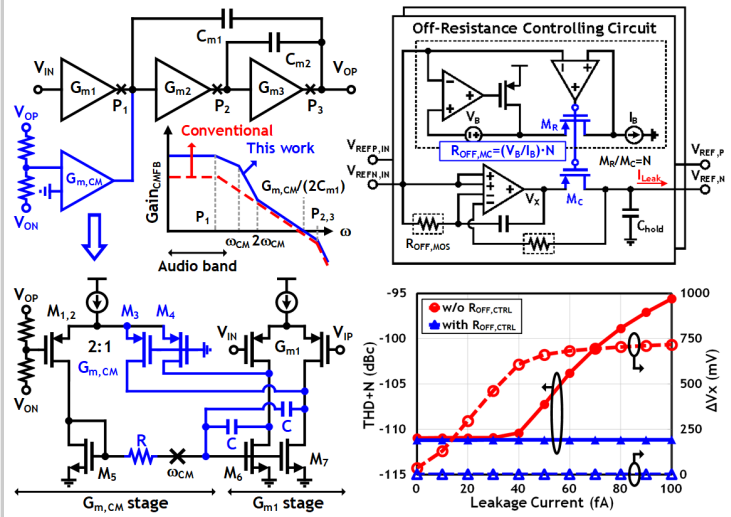


Figure 21.4.3: Gain-boosting CMFB (left) and R_{OFF}-controlled noise filter (right).

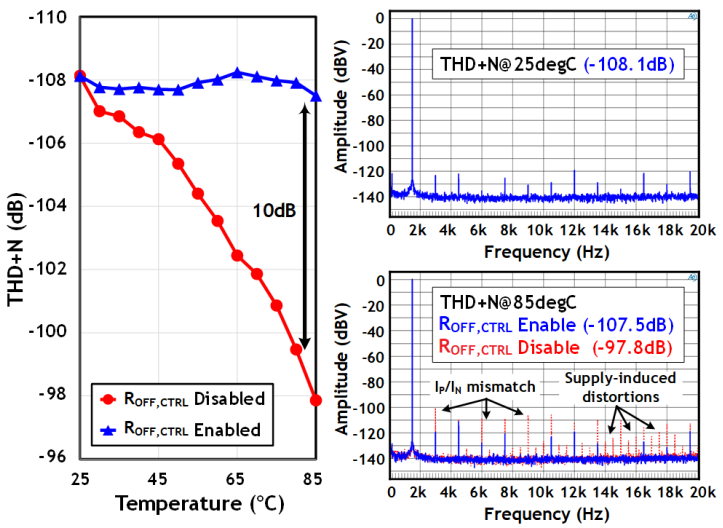


Figure 21.4.4: Measured THD+N sweep plot and FFT spectra.

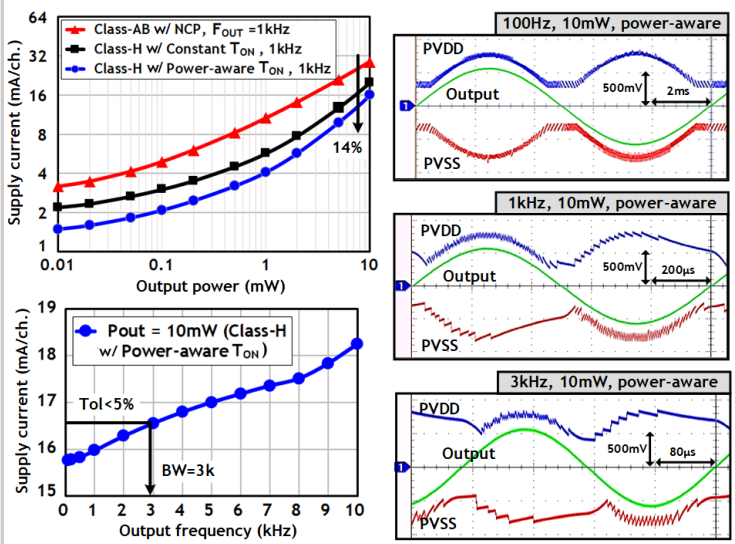


Figure 21.4.5: Measured supply current sweep plots and output waveforms.

	This work	[9] ISSCC'21	[4] ISSCC'10	[2] MAX97200	[1] TPA6141
Process	28nm	28nm	65nm	-	-
Dac+Amp	dac+amp	dac+amp	amp only	amp only	amp only
PMU topology	SIMO	NCP	-	4-level CP	Buck+NCP
Class-AB/G/H	Class-H	Class-AB	Class-G	Class-H	Class-G
Supply (V)	1.8	1.8	1.4	1.8	2.5
Load (Ω)	16	16	32	16	16
Output type	SE	SE	SE	SE	SE
Peak output power	62	62	45	45	40
@ Lowest THD+N, 1kHz					
Output voltage (Vpp)	2.82	2.82	2.02	1.13	1.89
Output power (mW)	62	62	16	10	28
THD+N / THD (dBc)	-108 / -112	- / -117	-80 / -	-91 / -	-76 / -
SNR (A-weighted) (dB)	126	126	101	105	105
Tracking Bandwidth (Hz)	3k	-	-	16	-
Power consumption, 1kHz (mW)					
(Driver only, per channel)	(***)	(est.*)	(est.*)	(**)	(**)
@ no output power (mute)	2.3	4.8	0.41	1.04	2.2
@ 0.01mW output power	2.6	6.1	-	-	2.5
@ 0.1mW output power	3.7	9.2	0.87	-	4.5
@ 1mW output power	7.3	18.6	2.1	8.5	11.3
@ 10mW output power	28.7	48.9	21.3	42.5	31.3
FoM (THD) †	107,316	91,443	6,338	15,353	1,147
FoM (SNR) ‡	53,785	25,772	7,111	7,694	3,233

* The power estimation in [9] and this work assumes the EFF(NCP)=85%, and the data in [4] doesn't include the power consumption and efficiency of the power converters. ** Extracted from the plots.
*** The quiescent current of the driver (w/ SIMO) and the decoder (include DACs, drviers and LDOs) are 1.3mA@ 1.8V/channel and 3.5mA@1.8V/channel, respectively.
† FoM(THD)=Pout,max/[Quiescent power*THD(%)] ‡ FoM(SNR) = Pout,max/[Quiescent power*SNR*1000]

Figure 21.4.6: Performance summary and comparison to state of the art.

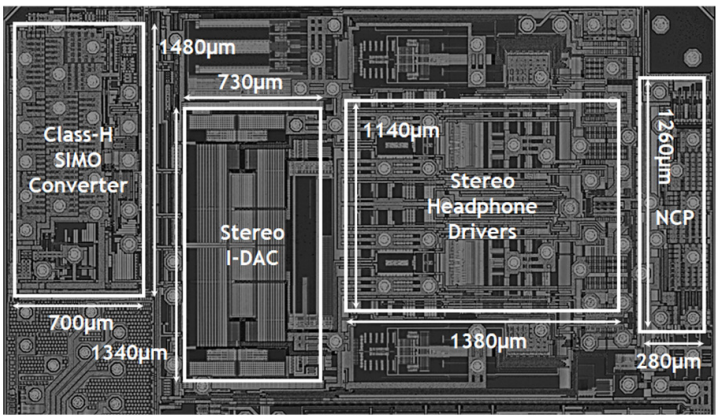


Figure 21.4.7: Die micrograph.

Additional References:
[8] Jongyup Lim et al., "A 224 pW 260 ppm/°C Gate-Leakage-based Timer for Ultra-Low Power Sensor Nodes with Second-Order Temperature Dependency Cancellation," *VLSIC*, pp. 117-118, June 2018.
[9] S. Wen et al., "A -117dBc THD (-132dBc HD3) and 126dB DR Audio Decoder with Code-Change-Insensitive RT-DEM Algorithm and Circuit Technique for Relaxing Velocity Saturation Effect of Poly Resistors," *ISSCC*, pp. 482-483, Feb. 2022.

979-8-3503-0620-0/24/$31.00