PrimeTime Suite Error Messages

Version V-2023.12-SP3, April 2024

SYNOPSYS®

Feedback

Contents

1

PrimeTime Suite Error Messages

This document describes the error messages supported by the PrimeTime Suite tool.

ADES

ADES-002

(info) Checking scenario '%s': %s

Description

This status message is printed during *analyze_design*. It shows the scenario and type of rules currently being checked.

ADES-003

(info) Checking global rules: %s.

Description

This status message is printed during *analyze_design*, while checking scenario-independent rules. It shows the type of rules currently being checked.

ADES-004

(error) Scenario '%s' is empty; no rule checks will be performed.

Description

This status message is printed during *analyze_design*. Rules will not be checked for this scenario because it has no constraints.

ADES-005

(error) The 'create_rule_violation' command can only be called during 'analyze_design'.

Feedback

Description

You cannot generate violations of user-defined rules except in the Tcl procedures called during the *analyze_design* command.

What Next

Use *analyze_design* to invoke the user-defined rule check procedures.

See Also

- create_rule_violation

ADES-006

(error) Rule '%s' is not user-defined.

Description

The *create_rule_violation* command must specify a user-defined rule.

What Next

The Tcl procedure for checking user-defined rules should invoke *create_rule_violation* with a user-defined rule. Use *create_rule* to create a user-defined rule.

See Also

- create_rule
- create_rule_violation

ADES-007

(error) Incorrect number of parameters specified for rule '%s':\nrule has %d parameter, create_rule_violation specified %d.

Description

The *create_rule_violation* command must be specified with the number of parameter values expected by the rule.

What Next

Fix the Tcl procedure to invoke *create_rule_violation* with the correct number of parameters.

Feedback

See Also

- create_rule
- create_rule_violation

ADES-017

(error) Violations of a scenario-dependent rule '%s' issued in user-defined global check procedure.

Description

User-defined global check procedure should not perform scenario-dependent checks.

What Next

Consider moving scenario-dependent checks into a user-defined scenario-dependent check procedure.

See Also

- create_rule

ADES-018

(error) Violations of a global rule '%s' issued in user-defined scenario check procedure.

Description

User-defined scenario check procedure should not perform global scenario independent checks.

What Next

Consider moving global checks into a user-defined scenario independent global check procedure.

See Also

- create_rule

ADES-021

(info) Running user-defined checker : %s.

Feedback

Description

This status message is printed during *analyze_design*, while running user-defined checkers. It shows the currently running user-defined checker.

ADES-022

(warning) User-defined rule '%s' is not associated with user-defined checker proc '%s'.

Description

This message is printed when a 'create_rule_violation' command issues a violation of a user-defined rule that is not associated with the current user-defined checker procedure.

What Next

Check the user-defined rule in the user-defined checker procedure associated with the rule when the rule is created.

See Also

- create_rule

AOCVM

AOCVM-001

(error) The field '%s' has already been specified for the current '%s'

Description

This error occurs when a field is specified more than once for a given table. The error can also occur if the user does not include all fields during a table specification.

What Next

Correct the AOCV syntax by ensuring that each field is only specified once for a given table.

AOCVM-002

(error) The current table is missing one or more fields

Feedback

Description

This error occurs when a table is found at the end of the AOCV file without the required number of fields.

What Next

Correct the AOCV syntax by adding the missing fields to the file.

AOCVM-003

(Error) Expected to find a valid field name but found '%s'.

Description

This error occurs when the parser cannot find a valid field name.

What Next

Correct the AOCV syntax by ensuring that each field is specified in the format name: data where name is one of version, table, distance, depth, object_spec, derate_type, delay_type, rf_type, object_type.

AOCVM-004

(error) Cannot specify '%s' for field '%s'.

Description

The data found in the AOCV file is not valid for the given field.

What Next

Check the AOCV spec to see allowed values for the field, and update the AOCV file appropriately.

AOCVM-005

(warning) Cannot associate table with leaf cell '%s'.

Description

AOCV does not support the association of AOCV data with leaf cells.

What Next

Associate AOCV tables with hierarchical cells, library cells and designs only.

Feedback

AOCVM-006

(warning) Cannot find any objects of type '%s' for specification '%s'.

Description

Could not find any objects for the given specification. The table is not annotated on any objects, but parsing and annotation does not stop due to this warning.

What Next

Check that the specification is correct.

AOCVM-007

(error) Expected table of size %d but found table of size %d.

Description

The size of the 2D AOCV table must equal the number of depth indexes by the number of distance indexes.

What Next

Correct the size of the table.

AOCVM-008

(error) Cannot finish AOCV file on a line continuation

Description

The AOCV file ends with a line continuation. The parser expects more data, but there is none.

What Next

Remove the line continuation character.

AOCVM-009

(error) Could not find the specified AOCVM file

Description

The AOCV file could not be found.

Feedback

What Next

Correct the name and path of the AOCV file.

AOCVM-010

(error) The field '%s' must be specified before '%s'

Description

While parsing an AOCV 2D table, a field cannot be set because another field is not specified.

What Next

Change the order of the field specifications.

AOCVM-011

(error) The version '%s' is not valid. Allowable versions are '%s'

Description

An invalid version number has been specified.

What Next

Check the version number.

AOCVM-012

(error) An AOCV file version must be specified.

Description

The version number is used for backward compatibility purposes if the AOCV file format changes in the future. It can affect the analysis results.

What Next

Specify the version of the AOCV file on the first line of the AOCV file. For example:

```
version:1.0
```

AOCVM-013

(error) The %s array does not increase or decrease sequentially

Feedback

Description

Sequential elements in the specified array must sequentially increase or decrease.

What Next

Fix the array so that it sequentially increases or decreases.

AOCVM-014

(error) Negative values are not allowed

Description

Negative values are not allowed for the distance, depth arrays or in the 2D tables.

What Next

Remove negative values from the AOCV file.

AOCVM-015

(error) Cannot specify delay type %s with object type %s

Description

This combination of delay type and object types is not allowed as it makes no sense.

What Next

Correct the AOCV file to remove the invalid combination of delay type and object type.

AOCVM-016

(error) Cannot specify a non-monotonic derate table.

Description

This message is issued because the derate table specified in the message is incorrectly defined. The table has not been annotated.

The timing derates specified in each row and each column of the derate table must increase or decrease monotonically.

What Next

Fix the specified table so that sequential elements in each row and each column of the table sequentially increase or decrease.

Feedback

AOCVM-017

(error) Derate table variability is not decreasing with increasing depth.

Description

This message is issued because the derate table specified in the message is incorrectly defined. The table has not been annotated.

For a late derate table, the timing derates specified in each row of the derate table must decrease monotonically as depth increases. For an early derate table, the timing derates specified in each row of the derate table must increase monotonically as depth increases.

No further restriction is placed on the table contents; however, typically, derate variability should be proportional to 1/sqrt(depth).

What Next

Fix the specified table so that sequential elements in each row of the early (or late) table sequentially increase (or decrease) as depth increases.

AOCVM-018

(error) Derate table variability is not increasing with increasing distance.

Description

This message is issued because the derate table specified in the message is incorrectly defined. The table has not been annotated.

For a late derate table, the timing derates specified in each column of the derate table must increase monotonically as distance increases. For an early derate table, the timing derates specified in each row of the derate table must decrease monotonically as distance increases.

No further restriction is placed on the table contents; however, typically, derate variability should be proportional to distance.

What Next

Fix the specified table so that sequential elements in each column of the early (or late) table sequentially decrease (or increase) as distance increases.

AOCVM-019

(warning) Voltage value is missing in the table at line number %d in the file %s.

Feedback

Description

A voltage field is specified, but an associated voltage value is missing.

What Next

Verify that the missing voltage value is intentional.

AOCVM-020

(warning) Replacing the old table specified for %s %s with voltage %s, with the latest specified table with the same voltage.

Description

Two tables with the same voltage value are specified for the same object. The first table is ignored.

What Next

Investigate to see why two tables with the same voltage are specified for the same object.

AOCVM-021

(Error) Expected to find a valid field name but found '%s'.

Description

This error occurs when the parser cannot find a valid field name.

What Next

Correct the AOCV syntax by ensuring that each field is specified in the format name: data where name is one of version, table, distance, depth, object_spec, derate_type, delay_type, rf_type, object_type, path_type.

AOCVM-022

(error) Cannot set/reset table group on a design that is not the current design.

Description

This message is issued if the user has called the set_aocvm_table_group/ reset_aocvm_table_group with a design, which is not the current design, as an argument.

What Next

If the user has intended to operate on the specified design, then set the current design using the current_design command.

Feedback

See Also

- current_design
- reset_aocvm_table_group
- set_aocvm_table_group

AOCVM-023

(error) Cannot set/reset table group on a hierarchical cell within the current design for the block level flow in HyperScale.

Description

This message is issued in a block level HyperScale flow if the user has called the set_aocvm_table_group/reset_aocvm_table_group command on a hierarchical cell within the current design

What Next

Associate AOCV table groups with the current design only in block level HyperScale flow

See Also

- current_design
- reset_aocvm_table_group
- set_aocvm_table_group

AOCVM-024

(Error) Expected to find a valid field name but found '%s'.

Description

This error occurs when the parser cannot find a valid field name.

What Next

Correct the AOCV syntax by ensuring that each field is specified in the format name: data where name is one of version, table, distance, depth, object_spec, derate_type, delay_type, rf_type, object_type, path_type, group_name.

Feedback

AOCVM-025

(error) Parametric OCV coefficient value is missing in the table at line number %d in the file %s.

Description

A coefficient field is specified but an associated value is missing.

What Next

Enter a valid value for the parametric OCV coefficient.

AOCVM-026

(warning) Variation extracted from AOCV table (%f) overwritten by user-specified variation (%f).

Description

Variation extracted from AOCV table overwritten by user-specified variation.

What Next

Investigate whether inconsistency of user-specified variation with AOCV table is intentional.

AOCVM-027

(Error) Field (%s) cannot be specified with field (%s)

Description

Field (%s) cannot be specified with field (%s).

AOCVM-028

(error) Field (%s) cannot be specified when ocvm_type is specified as (%s).

Description

Invalid field (%s) specified.

What Next

Refer to the (%s) table format in documentation.

Feedback

AOCVM-029

(warning) There is no %s named table set "%s". Ensure that it is loaded before update_timing.

Description

This message is issued when a named table set is assigned to a design or hierarchy but no table set with this name has been read yet. Since there is no required order for the *set_ocvm_table_group* and read_ocvm commands this is only a warning because it is possible that the named table set will still be read after the *set_ocvm_table_group* command.

What Next

Verify the sequence of commands in your script, and crosscheck the names in your name table sets against the names used in the *set_ocvm_table_group* command.

AOCVM-030

(error) Invalid OCV derate group %s "%s".

Description

To manually assign an OCV table from a library to a library cell, you must use the following syntax:

```
library_name/[lib_cell_name/]derate_group_name
```

If this syntax is not adhered to, or you reference a table that has not been read, this error message is issued.

What Next

Correct the name of the derate group and the syntax.

AOCVM-031

(warning) Lib cell based OCVM table can be only assigned to same lib cell.

Description

When manually assigning a library cell based OCV derate group to a library cell, it can only be assigned to the library cell that owns the derating group. If assignment to a different lib cell is attempted, this message is issued and the assignment is ignored.

Feedback

What Next

Remove the unmatched library cells from the library cell collection passed to set_ocvm_table_group.

AOCVM-032

(error) Field (%s) cannot take more than one voltage.

Description

Incorrect number of voltages specified.

What Next

Refer to the (%s) table format in documentation.

AOCVM-033

(error) Incorrect table value.

Description

The bottom right value of the 2D COCV table must be zero.

What Next

Correct the table values.

AOCVM-034

(Information) Removing side file based derates if loaded as OCVM derate side file scaling flow was enabled/dissabled.

Description

Side file based derates are reset when side file derate scaling flow is either enabled or dissabled.

AOCVM-035

(error) Incorrect syntax at line %s of file %s. %s

Description

Unrecognized symbols or extra symbols present at the specified line.

Feedback

What Next

Correct the syntax error.

AOCVM-036

(warning) Unsupported %s derate type "%s" specified and this derate column values will be ignored.

Description

Unsupported derate type specified in the derate file.

What Next

Correct the derate type name.

AOCVM-037

(error) %s derate bin label "%s" already defined.

Description

A given derate bin label can be associated with only one bin.

What Next

Specify unique labels across derate bins.

AOCVM-038

(error) Number of bin values is different from number of derate columns.

Description

Number of derate values in every bin must be same as the number of entries specified as DERATE_COLUMNS field of the derate side file.

What Next

Provide proper number of derate values.

AOCVM-039

(error) "default" bin must be specified and must be the last bin.

Description

Default bin definition missing in the COCVM CPODE dertate side file.

Feedback

What Next

Include default bin definition.

AOCVM-040

(warning) COCVM CPODE timing derate definition missing for lib cell(s) of library %s.

Description

At least one type of COCVM CPODE derate must be defined for all the lib cells of the library.

What Next

Load appropriate COCVM CPODE derates.

AOCVM-041

(warning) No COCVM CPODE timing derate associated with cell %s, using lib cell %s.

Description

At least one type of COCVM CPODE timing derate must be defined for associated lib cell.

What Next

Load appropriate COCVM CPODE derates.

ATTR

ATTR-1

(warning) Attribute '%s' has not been defined for %s

Description

The attribute is not defined for the class of objects that you are using. It is possible that the attribute is not defined at all.

Application attributes are all defined at runtime by the application. You can create user-defined attributes at any time.

Feedback

What Next

Verify that the attribute name is spelled correctly. If this is a documented application attribute, contact support. If this is a user-defined attribute, ensure that you have defined the attribute for all appropriate classes.

ATTR-2

(warning) Attribute '%s' is not user-defined for %ss; can't %s it

Description

The attribute you are referencing is an application attribute. You cannot set or remove this attribute by using the *set_user_attribute* or *remove_user_attribute* command, respectively. There might be other commands that allow you to set or remove the attribute.

What Next

See the documentation to determine if it is possible to set or remove this attribute.

ATTR-3

(Warning) Attribute '%s' does not exist on %s '%s'

Description

The attribute you are trying to get is not found on the object. This is definitely a sparse attribute and most likely user-defined. To suppress this message, use the -quiet option.

ATTR-4

(warning) Value '%s' is not valid for '%s' on %ss

Description

The value you are trying to set on the attribute cannot be converted to the data type defined for the attribute. For example, if the attribute is defined as "float", setting the attribute to *true* is not valid.

What Next

Enter an appropriate value for the attribute.

ATTR-5

(warning) Value '%s' for '%s' is not in range (%s)

Feedback

Description

The numeric value you are trying to set on the attribute is not in the range specified for the attribute. Ranges are either within a minimum and maximum value, greater than or equal to a minimum value, or less or equal to a maximum value. The message text indicates the violated constraint.

What Next

Enter an appropriate value for the attribute.

ATTR-6

(warning) Value '%s' for '%s' is not valid. Specify one of: %s

Description

The string value you are trying to set on the attribute is not one of the valid strings defined for the attribute. The message text indicates the allowable values.

What Next

Enter an appropriate value for the attribute.

ATTR-7

(information) Inferred definition of attribute '%s' for class '%s' because it is imported for class '%s'

Description

You used the *define_user_attribute* command to define a design or port attribute, and asked for it to be imported from DB files. Because design attributes are inherited onto cells (an instance of a design), and port attributes are inherited onto pins (an instance of a port), the attribute you defined for a design/port must also be defined for a cell/pin, respectively. The tool defines the attribute for you if you have not already done so, and issues this message.

What Next

If you want to remove this message, add the appropriate class to the list of classes in your *define_user_attribute* command, or add a dedicated *define_user_attribute* command earlier in the script to define the attribute for the cell or pin class.

See Also

- define_user_attribute

Feedback

ATTR-8

(Error) Remote access is not implemented for attribute %s of %s

Description

You are trying to report the value of an attribute which has no access functionality in the distributed context.

What Next

If you want to remove this message, update your script to remove the call to access the shown attribute.

See Also

- get_attribute

ATTR-9

(Warning) Attribute '%s' is of unsupported type '%s'

Description

The attribute you are trying to create is of unsupported data type.

ATTR-10

(Error) Unsupported attribute %s of %s in all of the modes

Description

Attribute is not supported. It cannot be accessed in both remote and local mode.

What Next

If you want to remove this message, update your script to remove the call to access the shown attribute.

See Also

- get_attribute

ATTR-11

(Warning) More than 1 dvfs scenario not supported for '%s' attribute\n

Feedback

Description

Attributes other than float don't have a well defined way to merge / worst-case them because of that such attributes must be queried with fully specified scenario to that only one value matches the scenario.

ATTR-12

(Error) Incorrect format for attribute value max_transition_sigma_derate_per_voltage: %s

Description

This message tells you that the format for the *max_transition_sigma_derate_per_voltage* attribute is incorrect. Various things can be wrong. The attribute must be a list. Each element of the list is a pair, where the first element is the lower voltage of range and the second is a sigma derate value. The voltage values must be in ascending order. The content of the message isolates where the problem exists.

What Next

Check man page for lib pin attribute *max_transition_sigma_derate_per_voltage* for the example of correct usage.

ATTR-13

(Error) Attribute %s has been defined on library %s, it cannot be overridden.

Description

The given attribute has been already defined on the library. The user cannot override the value specified in the library.

What Next

If you want to remove this message, update your script to remove the call to set the attribute.

ATTRDEF

ATTRDEF-001

(error) This visual (%s) does not exist.

Description

This visual does not exist. Please check the visual name.

Feedback

ATTRDEF-002

(error) Internal error. Not valid type set %s.

Description

Type set is not valid.

ATTRDEF-003

(error) Not valid class name.

Description

Design object class is not valid. Please, specify one of the following: %s

ATTRDEF-004

(error) (error) Incompatible type and subtype values.

Description

Subtype can be specified only if type is string.

ATTRDEF-005

(error) (error) Type must be specified.

Description

Type must be specified if subtype is presented.

ATTRDEF-006

(error) Incompatible type and format values.

Description

Format can be specified only if type is int or double.

ATTRDEF-007

(error) Type must be specified.

Description

Type must be specified if format is presented.

Feedback

ATTRDEF-008

(error) Attribute %s not found.

Description

Specified attribute not found.

ATTRDEF-009

(error) Internal error. Can't create attribute %s.

Description

Specified attribute can not be created.

ATTRDEF-010

(error) Attribute %s already exists.

Description

Specified attribute already exists and can not be created.

ATTRDEF-011

(error) Attribute %s is not user-defined.

Description

Specified attribute is not user-defined and not allowed for this command.

ATTRDEF-012

(error) Internal error. Removing of attribute %s failed.

Description

Removing of attribute failed.

ATTRDEF-013

(error) Internal error. Error getting list of attdefs for %s.

Description

Getting list of attdefs failed.

Feedback

ATTRDEF-014

(error) Internal error. Error getting list of object types.

Description

Getting list of object types failed.

ATTRDEF-015

(error) Error. Option -name valid with -class only

Description

Option -name valid with -class only.

ATTRDEF-016

(error) Attribute group %s already exist.

Description

Specified attribute group already exist and can not be created.

ATTRDEF-017

(error) Attribute group %s not found.

Description

Specified attribute group not found.

ATTRDEF-018

(error) Internal error. Removing of attribute group %s failed.

Description

Removing of attribute group failed.

ATTRDEF-019

(error) Internal error. Removing all attribute groups of class %s failed.

Description

Removing of attribute groups failed.

Feedback

ATTRDEF-020

(error) Error. Options -add, -delete or -move are exclusive with -attr_list.

Description

Options -add, -delete or -move are exclusive with -attr_list.

ATTRDEF-021

(error) Error. Attribute name -attr is required.

Description

Attribute name -attr is required.

ATTRDEF-022

(error) Error. Attribute list or single attribute is required.

Description

Attribute list or single attribute with add/delete/move option is required.

ATTRDEF-023

(error) Error. Option -anchor should be specified with -move.

Description

Option -anchor should be specified with -move after/before options.

ATTRDEF-024

(error) Error. Either -add, -delete or -move should be specified.

Description

Either -add, -delete or -move should be specified.

ATTRDEF-025

(error) Internal error. Error getting list of attribute groups for class %s failed.

Description

Getting list of attribute groups failed.

Feedback

ATTRDEF-026

(error) Attribute %s is application defined.

Description

Specified attribute is aplication defined and can not be deleted.

ATTRDEF-027

(error) Attribute %s is user-defined.

Description

Specified attribute is user-defined. Options -width, -show|-hide, and -show_infotip|-hide_infotip are valid for this type of attribute.

ATTRDEF-028

(error) Content of attribute group %s is system defined.

Description

Specified attribute group is system defined and cannot be deleted or modified.

CATEGORY

CATEGORY-001

(error) cannot create category rule '%s' since the previously created rule is not built-in.

Description

This error message occurs when an attempt is made to create a category rule with the -builtin option even though the previously created rule is not built-in.

What Next

Rerun gui_create_category_rule without the -builtin option.

See Also

- gui_create_category_rule

Feedback

CATEGORY-002

(error) cannot create category rule with name '%s' since a rule with that name already exists.

Description

This error message occurs when an attempt is made to create a category rule with a rule name that is already in use.

What Next

Rerun gui_create_category_rule with a -name option value which is not a rule name that is already in use.

See Also

- gui_create_category_rule

CATEGORY-003

(error) for category rule '%s' cannot add subrule '%s' since no such rule exists.

Description

This error message occurs when gui_create_category_rule -subrules references a rule which does not already exist.

What Next

One possibility is that the subrule name was mis-spelled when passed to -subrules. In that case rerun gui_create_category_rule but passing the correctly spelled rule name to -subrules. Another possibility is that the rule name passed to -subrules was correctly spelled but does not yet exist. In that case, create a new rule with that name (using gui_create_category_rule -name) and then rerun the gui_create_category_rule -subrules command that failed.

See Also

- gui_create_category_rule

CATEGORY-004

(error) cannot add subrule '%s' since that subrule has already been added to the category rule '%s'.

Feedback

Description

This error message occurs when gui_create_category_rule -subrules references the same subrule (using the same rule name) more than once in the subrules list.

What Next

Rerun gui_create_category_rule -subrule but removing duplicate references to the rule name that was listed in the subrules more than once.

See Also

- gui_create_category_rule

CATEGORY-005

(error) -rule_names or -names contains invalid category rule name '%s'.

Description

This error message occurs when a command is run which accepts a list of category rule names via -rule_names or -names and that list includes a category rule name which does not exist.

What Next

Rerun the command with corrected spelling for the rule name (passed to -rule_names or -names) which was mis-spelled.

See Also

- gui_list_category_rules

CATEGORY-011

(error) cannot create category rule '%s' since it has an error in the category specification string at position %d.

Description

This error message occurs when gui_create_category_rule is run with a -category option value which has a syntax error.

What Next

Fix the syntax error in the -category option string value and rerun gui_create_category_rule.

Feedback

See Also

- gui_create_category_rule

CATEGORY-012

(error) cannot create category rule '%s' since it has an error in the filter specification string.

Description

This error message occurs when gui_create_category_rule is run with a -filter option value which has a syntax error.

What Next

Fix the syntax error in the -filter option string value and rerun gui_create_category_rule.

See Also

- gui_create_category_rule

CATEGORY-021

(error) cannot remove category rule '%s' since it is in use by one or more existing categories.

Description

This error message occurs when gui_remove_category_rule is run to remove a rule that one or more existing categories depends on.

What Next

Fix the issue by removing the affected categories and rerun gui_remove_category_rule.

CATEGORY-031

(error) cannot evaluate expression since no attribute '%s' exists for '%s'.

Description

This error message occurs when -category or -filter specifications reference an attribute which does not exist for an object that the category rule is executed for.

What Next

Revise the -category or -filter specification to use an attribute which exists for the object in question.

Feedback

See Also

- gui_create_category_rule

CATEGORY-032

(error) cannot evaluate expression since attribute '%s' is a collection.

Description

This error message occurs when -category or -filter specifications reference an attribute whose value is a collection containing multiple objects.

What Next

Referencing a collection containing multiple objects is currently not supported in -category or -filter specifications. Use a different attribute instead.

See Also

- gui_create_category_rule

CATEGORY-033

(error) cannot evaluate expression since attribute '%s' of type '%s' has sub-attributes.

Description

This error message occurs when -category or -filter specifications reference an attribute whose value is a collection containing a single object.

What Next

Consider using "dot notation" in -category or -filter specification to access an attribute of the object in the collection. For example, instead of -category <startpoint> try -category <startpoint.full_name>. Use list_attributes to discover the attributes supported for the type mentioned in the error message.

See Also

- gui_create_category_rule

CATEGORY-034

(error) cannot evaluate filter expression since attribute '%s' of type '%s' of data type '%s' is not of data type '%s'.

Feedback

Description

This error message occurs when evaluating a filter expression where an attribute for an object that the category rule is executed for doesn't match a required type in the expression.

What Next

Revise the -filter specification so that the type for the attribute matches what is required.

See Also

- gui_create_category_rule

CATEGORY-035

(error) cannot evaluate filter expression because of an operand type mismatch.

Description

This error message occurs when evaluating a filter expression where a operand type mismatch has occured.

What Next

Revise the -filter specification so that the operands match in type.

See Also

- gui_create_category_rule

CATEGORY-036

(error) cannot evaluate filter expression because operator '%s' has a type mismatch.

Description

This error message occurs when evaluating a filter expression where a operator type mismatch has occured.

What Next

Revise the -filter specification so that the operators match in type.

See Also

- gui_create_category_rule

Feedback

CATEGORY-040

(error) cannot create category tree with name '%s' since a category tree with that name already exists.

Description

This error message occurs when an attempt is made to create a category tree with a category tree name that is already in use.

What Next

Rerun gui_create_category_tree with a -name option value which is not a category tree name that is already in use.

CATEGORY-052

(error) No current category tree found.

Description

This error message occurs when the -tree option is omitted when calling one of the category commands, and there is no current category tree. With these category commands, you can pass an explicit -tree option value to specify the category tree to be operated on. If that optional option is omitted, an attempt will be made to use the current category tree. This error happens if there is no current category tree (which can only happen if no category trees exist).

What Next

Create at least one category tree (so that there will be a current category tree) and rerun the command which generated the error.

See Also

- gui_get_category

CATEGORY-053

(error) the categorization script file '%s' already exists.

Description

This error message occurs when the gui_write_category command is run with a -file option value which identifies a file which already exists, and the -overwrite option was not specified.

Feedback

What Next

Rerun the gui_write_category command specifying the -overwrite option to overwrite the existing file. Or else specify a file which does not yet exist via the -file option.

CATEGORY-054

(error) the categorization script file '%s' could not be opened for write.

Description

This error message occurs when the gui_write_category command is run with a -file option value which identifies the file to be written, and the file cannot be opened for write.

What Next

Investigate parent directory permissions to figure out why the file could not be opened for write. Fix any such permissions problems and rerun the gui_write_category command.

CATEGORY-055

(error) cannot create new subcategories of a hierarchical category which already has subcategories that were created via a separator character

Description

The categorization engine can create category hierarchy as a result of interpreting hierarchical separator characters embedded in the string value produced by a category rule's category specification. This error message occurs when the gui_create_category command is used to try to add additional subcategories to a category which already has one or more subcategories that were created by interpreting a separator character.

What Next

Choose a different category to pass to the -parent_category option of gui_create_category.

See Also

- gui_create_category_rule

CATEGORY-056

(error) cannot remove subcategories of a hierarchical category which has subcategories that were created via a separator character

Feedback

Description

The categorization engine can create category hierarchy as a result of interpreting hierarchical separator characters embedded in the string value produced by a category rule's category specification. This error message occurs when the gui_remove_category command is used to try to remove subcategories of a category which has one or more subcategories that were created by interpreting a separator character.

What Next

Choose a different category to pass to the -parent_category option of gui_remove_category.

See Also

- gui_create_category_rule

CATEGORY-091

(warning) cell '%s' has no block mark.

Description

This warning message occurs when a command is run to get or remove the block mark of a cell instance which has no block mark.

What Next

Rerun the command but specify a cell instance for which a block mark has been previously set.

See Also

- gui_get_cell_block_marks
- gui_remove_cell_block_marks

CI

CI-001

(error) Can not open cell edge info side file '%s'

Description

The cell edge info side file name given is incorrect or the search path for this side file is not given or the path is incorrect.

Feedback

What Next

Check whether the side file exists and has read permissions.

CI-002

(error) Physical data base is not read in successfully. Skip external CPODE spacing calculation.

Description

External CPODE spacing calculation is only available after check_eco.

What Next

Please check check_eco if physical data is loded successfully.

See Also

- check_eco

CI-003

(error) read_cell_info is not performed after external CPODE spacing is updated.

Description

read_cell_info is not performed after external CPODE spacing is updated by update_cell_info

What Next

Please remove_cell_info then read_cell_info again.

CI-004

(warning) read_cell_info found duplicate definition in cell edge side file. '%s' is skipped.

Description

read_cell_info found duplicate definition in cell edge side file. The line is skipped.

What Next

Please check whether the side files have duplicate definition.

Feedback

CI-005

(error) Cell edge info side file is not read in successfully.

Description

Cell edge side file is not read in successfully. Skip CPODE spacing calculation.

What Next

Please check whether the cell edge side files are successfully read in.

CI-006

(error) Found syntax error in cell edge info sidefile on line '%d'. Skip '%s'.

Description

Found syntax error in cell edge info sidefile. The line is skipped

What Next

Please check the syntax error in side file.

CI-007

(error) SITE ROW information is missing. Skip external CPODE spacing calculation.

Description

SITE ROW information is missing. Skip external CPODE spacing calculation.

What Next

Please check check_eco if physical data is loaded successfully.

CI-008

(error) CPP width is missing. Skip external CPODE spacing calculation.

Description

CPP width is missing. Skip external CPODE spacing calculation.

What Next

Please check check_eco if physical data is loaded successfully.

Feedback

CI-009

(error) Cell '%s' (lib cell '%s') is not defined in the side file.

Description

Internal CPODE info of the cell is missing.

What Next

Please check the missing interal CPODE info in side file.

CI-010

(error) Cell '%s' (lib cell '%s') is defined with %d row high in side file but with %d row high in physical database.

Description

Row high of cell in physical database does not match with the side file definition.

What Next

Please check if the LEF/DEF files and side files are matched.

CLE

CLE-01

(information) Command line editor mode is set to %s successfully.

Description

This information message confirms that the command line editor mode is set to the mode that you specified.

To set the line editing mode to vi or emacs, use the *sh_line_editing_mode* variable.

What Next

This is an informational message. No action is required.

See Also

- sh_line_editing_mode

Feedback

CLE-02

(warning) Command line editor mode cannot be set to %s. Proceeding with %s mode.

Description

This warning message occurs when you attempt to set the line editing mode to an invalid value. If you attempt to set the variable to an invalid value, the tool uses the previously specified editing mode or the default emacs mode.

What Next

Set the *sh_line_editing_mode* variable to *vi* or *emacs*.

See Also

- sh_line_editing_mode

CLE-03

(warning) Command line editor is already in %s mode.

Description

This warning message occurs when you specify the same value for the command line editing mode that is currently in use.

What Next

This is a warning message. No action is required.

See Also

- sh_line_editing_mode

CLE-04

(warning) Variable sh_enable_line_editing can be set only in the .synopsys_pt.setup file.

Description

This warning message occurs when you attempt to enable command line editing by setting the *sh_enable_line_editing* variable in the shell rather than in the .synopsys_pt.setup file.

What Next

To enable command line editing, set the *sh_enable_line_editing* variable to *true* in the .synopsys_pt.setup file.

Feedback

See Also

- sh_enable_line_editing

CLE-05

(Warning) Command line editing is not active.

Description

Since command line editing is not currently active, setting the *sh_line_editing_mode* variable has no effect.

What Next

To enable the line editing mode, set the *sh_enable_line_editing* variable to *true* in the .synopsys_pt.setup file.

See Also

- sh_enable_line_editing
- sh_line_editing_mode

CLE-06

(information) %s is currently in %s editing mode.

Description

This information message displays the current editing mode.

What Next

This is only an informational message. No action is required.

To change the line editing mode, set the *sh_line_editing_mode* variable to *vi* or *emacs*.

See Also

- sh_line_editing_mode

CLE-07

(information) Terminal beep is %s.

Description

This information message displays the current terminal beep mode.

Feedback

What Next

This is an informational message. No action is required.

To turn the terminal beep on or off, use the *set_cle_options* command.

CLE-08

(error) Terminal beep mode value can be either on or off.

Description

This message occurs when you attempt to set the line editor beep mode to an invalid value. The value can be either *on* or *off*. If you attempt to set the beep mode to an invalid value, then the tool uses the existing beep mode.

What Next

To specify a valid beep mode, use the *set_cle_options* command.

CLE-09

(warning) -defaults option will override other options.

Description

The *-defaults* option overrides the other options of the *set_cle_options* command.

What Next

This is a warning message. No action is required.

CLE-10

(information) Term was not able to be set up using %s . Using "xterm" by default instead.

Description

This warning message occurs in certain OS when the term cannot be set up under its default term name.

CLE-100

(Warning) Cannot use command line editor for terminal type '%s'.

Feedback

Description

The command line editor has failed to initialize for terminal type '%s'. This can occur when the terminfo database could not be found or the database does not have an entry for the terminal type '%s'. If this message is printed, advanced shell editing capabilities cannot be used.

What Next

Use a terminal window that has the required capabilities, such as a linux dtterm.

CMCR

CMCR-001

(error) Cannot specify option '%s' when setting the local process options.

Description

The command *set_host_options* was used with an option that cannot be specified when *set_host_options* is used to set usage limits of the local process. Note that even if *-local_process* is not specified, the option is implied unless the *-num_processes* option is used.

What Next

If the command was intended to specify remote process options, then specify the *-num_processes* option. Otherwise, remove the option indicated above and reissue the command.

See Also

- set_host_options

CMCR-002

(error) Cannot specify machine name '%s' with local host.

Description

The *set_host_options* command was used with a specified machine name while using the local host setting. The machine name cannot be specified when using the *-local* option.

What Next

See the man page for the *set_host_options* command.

Feedback

See Also

- set_host_options

CMCR-003

(Warning) Replacing host options '%s'.

Description

The command is defining host options with the name specified. However, host options of the same name already exist. The original host options will be removed, and all associated host instances will be shutdown. The new host options will replace the original host options.

What Next

To launch the processes specified by the new host options, use the *start_hosts* command.

See Also

- start_hosts

CMCR-004

(Warning) No submit command or protocol specified to access hosts, the 'rsh' protocol will be used.

Description

The *set_host_options* command has been called specifying no *-protocol* option or *-protocol auto*, no *-submit_command* option and specifying a list of hostnames upon which to launch worker processes. The list of hostnames contains at least one hostname which is remote from the manager so the *rsh* protocol and command will be used to launch worker processes specifed by the host options.

What Next

If a specific protocol and/or submit command is required, remove the host options using the *remove_host_options* command and call the *set_host_options* command with the required options.

See Also

- remove_host_options
- set_host_options

Feedback

CMCR-005

(warning) Not all processes could be added for starting.

Description

While adding the processes to be launched, some of the processes could not be added due to internal limits.

What Next

To determine which host options did not have some processes started, use the *report_hosts* command.

CMCR-006

(error) Timeout has been set to '%d' seconds. Timeout must be set to a nonnegative value.

Description

The *start_hosts* command was used with the *-timeout* option set to a negative value. This parameter specifies the maximum duration the command blocks for remote processes to come online before returning and must be set to a value greater than or equal to 0.

What Next

Specify a value greater than or equal to 0 when using the *-timeout* option of the *start_hosts* command.

See Also

- start_hosts

CMCR-007

(error) The '-min_hosts' parameter has been set to '%d'. This parameter must be set to a nonnegative value.

Description

The *start_hosts* command was used with the *-min_hosts* option set to a negative value. This parameter specifies the minimum number of hosts that must come online before returning and must be set to a value greater than or equal to 0.

What Next

Specify a value greater than or equal to 0 when using the *-min_hosts* option of the *start_hosts* command.

Feedback

See Also

- start_hosts

CMCR-008

(error) The host options named '%s' does not exist.

Description

The specified host option name does not exist.

What Next

To create the named host options, use the *set_host_options* command.

See Also

- set_host_options

CMCR-009

(Warning) Process '%d' could not be stopped for host options '%s'

Description

The process indicated could not be stopped. Since the process could not be stopped, the associated host options could not be removed.

What Next

Examine the logged information when the processes were started. If there was an error in the options used to launch the processes then these process will never come online or be able to shutdown and therefore cannot be controlled. If there was no error during the launch of the processes, wait for the processes to come online, and then remove the host options.

See Also

- remove_host_options
- report_host_usage

CMCR-010

(error) Must specify a resource limit option with -local_process.

Feedback

Description

The *-local_process* option requires the *-max_cores* options to be specified.

What Next

When using the *set_host_options* command with the *-local_process* option, also specify the *-max_cores* option.

See Also

- set_host_options

CMCR-011

(information) %s manager licenses %s worker usage.

Description

When the manager is not using all its licensed cores it will float some of its licenses for worker usage. When the load increases at the manager and it needs to use its cores, it will reclaim its licenses from worker usage.

What Next

No action is required.

CMCR-012

(error) '%s' can only be called in a distributed processing context.

Description

The command specified or options passed to the command specified cannot be used unless PrimeTime is being run or configured to run some form of distributed analysis.

What Next

See the man page for the specific command for details when the command or options should be used.

CMCR-013

(Error) Failed to set the remote working directory because %s

Description

Setting the remote working directory failed due to the specified reason.

Feedback

What Next

See the man page for the working directory variable being set for the conditions necessary when setting the remote working directory.

CMCR-014

(Error) Failed to setup subdirectory '%s' because %s

Description

The directory specified could not be created with write permissions for the reason indicated.

What Next

See the man page for the working directory variable being set, and check the directory to ensure that the directory can be created.

CMCR-015

(error) Failed to start worker processes: %s (%s)

Description

Starting the worker processes failed due to the specified reason.

See also *set_host_options* to verify that your protocol and *submit_command* are configured correctly.

What Next

Check all the logs in the system_log directory for information about the failure. Redo the run with the variable *distributed_logging* set to its highest value to capture more detailed information in the system_log directory to help identify the source of the failure.

Check any output or error files generated by the farm submission engine.

See Also

- set_host_options
- start_hosts
- distributed_logging

Feedback

CMCR-016

(error) Additional processes cannot be added to already started hosts.

Description

You must use the *set_host_options* command before using the *start_hosts* command. Before you add more hosts, use the *stop_hosts* command.

What Next

See the man page for the *set_host_options* command.

See Also

- set_host_options
- start_hosts

CMCR-017

(warning) Hosts already started.

Description

Hosts have already been started by a previous call to *start_hosts*. No further hosts will be started.

What Next

See the man page for the *start_hosts* command.

See Also

- start_hosts

CMCR-018

(error) No host options exist.

Description

No host options exist so there is nothing to start.

What Next

Use the *set_host_options* command to define host options and then call the *start_hosts* command.

Feedback

See Also

- report_host_usage
- set_host_options
- start_hosts

CMCR-019

(Error) Invalid submission command '%s'.

Description

You cannot specify a blank or empty string as the submission command.

What Next

Specify a valid submission command.

See Also

- set_host_options

CMCR-020

(Error) Invalid hostname '%s'.

Description

You cannot specify a blank or empty string for the host name.

What Next

Specify a valid host name.

See Also

- set_host_options

CMCR-021

(Warning) Unrecognized command '%s' for protocol '%s'

Feedback

Description

The command does not match the typical command expected for the protocol. The typical commands expected for each protocol are as follows:

```
Protocol       Command
 sh             sh
 rsh            rsh
 ssh            ssh
 lsf            bsub
 sge            qsub
 rtda           nc
 pba            qsub
```

What Next

If the submission command targets the resource in the same manner as the underlying protocol, you can ignore this warning. All options that are supported by the protocol must be passed through to the underlying protocol command.

See Also

- set_host_options

CMCR-022

(Error) Protocol '%s' cannot target host '%s'.

Description

The current protocol targets the local host on which the manager process is running. It cannot target the specified host because it is remote from the manager.

What Next

Select a protocol that can access hosts remote from the manager, or target the manager host.

See Also

- set_host_options

CMCR-023

(Error) Protocol '%s' does not target hosts in this manner.

Feedback

Description

The protocol indicated either submits jobs to a managed compute resource, or it cannot target hostnames in the specifed manner.

What Next

To target a managed compute resource, do not pass the *hostname* option to the *set_host_options* command.

To use the custom protocol, do not pass the *hostname* option to the *set_host_options* command. The hostnames to be targeted must be part of the custom script passed to the *-submit_command* option of the *set_host_options* command.

To target specific hostnames, ensure that the *-protocol* option of the *set_host_options* command specifies a protocol that can target a host.

See Also

- set_host_options

CMCR-024

(Error) The '%s' protocol requires a submit command.

Description

The submit command cannot be blank or unspecified when this protocol is used.

What Next

Specify a suitable submit command for launching worker processes.

See Also

- set_host_options

CMCR-025

(error) Cannot open temporary file '%s' for %s.

Description

The specified temporary file needs to be opened for reading or writing by the *start_hosts* command.

If reading, the file may not exist, or might have incorrect permissions. If writing, you may not have access to the directory or the file may already exist and cannot be overwritten due to insufficient file permissions.

Feedback

What Next

Verify that you have the correct permissions to access the distributed working directory and to write or read the specified file in this directory. Change the distributed working directory if file permissions cannot be changed.

See Also

- start_hosts
- multi_scenario_working_directory

CMCR-026

(error) Failed to complete writing to file '%s'.

Description

The specified temporary file created by the *start_hosts* command was not fully written. This error is issued when writing of the required data into the specified file was not completed.

What Next

Check the available disk space in the distributed working directory. Check your disk quotas. Verify that a file can be created in the distributed working directory.

See Also

- start_hosts
- multi_scenario_working_directory

CMCR-027

(error) An error occured in closing file '%s'.

Description

An error occured when *start_hosts* command tried to close the specified temporary file. This may happen if there is no available disk space left in the distributed working directory or due to a disk IO error.

What Next

Check the available disk space in the distributed working directory. Check your disk quotas. Verify that a file can be created in the distributed working directory.

Feedback

See Also

- start_hosts
- multi_scenario_working_directory

CMCR-028

(error) the submit_command '%s' can't be executed or is not in the PATH.

Description

The submit command must be available from the current working directory or on the path and the user must have executable permissions.

What Next

Check your path and the permissions of submit command.

See Also

- set_host_options

CMCR-029

(error) %s.

Description

The submit command must not contain the options identified.

What Next

Remove the unsupported options and re-call the command.

See Also

- set_host_options

CMCR-030

(error) Cannot access file '%s' for '%s'.

Description

The specified file needs to be accessed for it to be sourced at startup of a worker primetime shell. It needs to be present at the location where it can be accessed from the worker process.

If reading, the file may not exist, or might have incorrect permissions. The directory where it is present may not be accessible by the worker process owing to several possible reasons such as, the directory is not an NFS point or it might not have execute permission.

What Next

Verify that you have the correct permissions to access the working directory of worker process and to read the specified file in this directory. Change the distributed working directory if file permissions cannot be changed.

See Also

- start_hosts
- multi_scenario_working_directory

CMCR-031

(error) Failed to setup communication infrastructure: %s (%s)

Description

The error indicated arose while initializing critical communication infrastructure and the current operation cannot proceed.

What Next

Examine the logs located in the 'system_log' directory for why the failure occured.

See Also

- distributed_logging

CMCR-032

(error) The host_options are already started, there is nothing to start.

Description

There are no unstarted host_options so there is nothing for the *start_hosts* command to do.

What Next

Defined host_options using the *set_host_options* command and call *start_hosts* again.

See Also

- set_host_options

Feedback

CMCR-033

(error) could not access the current working directory for use as the working directory because '%s'

Description

The working directory was not set and trying to get the current working directory for use failed because of the reason shown.

What Next

See the man page for the working directory variable being set, and check the directory to ensure that the directory can be created.

CMCR-034

(information) start_hosts timeout expired, workers will be accepted online in the background.

Description

The timeout for the *start_hosts* command has expired. All remaining workers launched will be accepted online in the background.

See Also

- start_hosts

CMCR-035

(Information) start_hosts interrupted, workers will be accepted online in the background.

Description

The *start_hosts* command has been interupted by the user. All remaining workers launched will be accepted online in the background.

See Also

- start_hosts

CMCR-036

(error) Cannot use '%s' as a name for host options.

Feedback

Description

An invalid value was specified for the -name option to the *set_host_options* command. The value passed to the *-name* option cannot be empty or whitespace.

What Next

Call the set_host_options command passing a valid value to the *-name* option or pass no -name option resulting in the options being auto-named.

See Also

- set_host_options

CMCR-037

(error) '%d' job submissions failed to launch; the remaining pending and running jobs '%d' cannot meet the required minimum worker count '%d'.

Description

Although the *start_hosts* command submitted the number of worker jobs indicated, while waiting for the queued worker jobs to come online, the PrimeTime distributed manager noticed that some jobs failed to launch. This error message occurs when the remaining pending jobs and running jobs are no longer sufficient to meet the required minimum worker count.

A job fails to launch when:

- The compute farm unqueues (rejects) the job for some reason, such that the PrimeTime process never attempts to run.
- The compute farm runs the job and the PrimeTime process attempts to launch, but it terminates before registering itself (network issues, unavailable working directory, etc.)

Potential causes of this message are:

- Slow or unreliable network connection
- Firewall rules that block communication between the worker and manager processes
- Slow or unreliable network file system
- Inaccessible distributed analysis working directory
- Operational issues with the compute farm manager

This message does not apply to worker processes that terminate after successfully launching on the compute farm.

Feedback

For more information on the check associated with this message, see the *distributed_farm_check_pending_workers_interval* man page.

What Next

Examine the PrimeTime distributed manager's log file (in the system_log directory within the distributed working directory) to determine why submitted workers have been aborted.

If the issue is caused by slow network response times, you can try increasing the value of the *distributed_farm_check_pending_workers_interval* variable.

See Also

- set_host_options
- start_hosts
- distributed_logging
- distributed_farm_check_pending_workers_interval

CMCR-038

(error) launched '%d' workers, requiring '%d' workers to come online but only '%d' workers in the online/launched state due to '%d' failed worker startups.

Description

Although the start_hosts command launched the number of workers indicated, while waiting for workers to come online, the number of workers in the online/launched state dropped below the level needed to satisfy the number of required online workers.

This was caused by workers failing to successfully startup and connect back to the manager.

Since the number of required online workers can never be satisfied by the *start_hosts* command, it has errored out.

What Next

Examine the manager system log file in the system_log directory to determine why launched workers have failed.

Look in the distributed working directory and the users home directory for special log files written by the worker during its startup. The special log files will identify the manager to which the worker tried to connect and why the worker failed to startup. The files have the following naming convention.

pt_worker_<worker_hostname>_<worker_process_id>.fail

Feedback

See Also

- set_host_options
- start_hosts
- distributed_logging

CMCR-039

(error) Empty host options name list specified.

Description

The list of host options specified is empty. In order to report specific host options, pass a list of the names of existing host options to the *report_host_usage* command.

What Next

Specify the names of host options to report.

CMCR-040

(Warning) The value for load_factor (%d) must be within the range 1<=value<=%d. Resetting it to %d.

Description

The argument of the *-load_factor* option in the *set_host_options* command must be an integer in the range from 1 to the maximum value shown in the warning message.

What Next

The command automatically set the load factor to an allowed value and proceeded with the next command. No action is needed to correct the invalid setting, but be aware of the actual load factor being used.

CMCR-041

(error) failed to launch '%d' CDSL servers: (%s)

Description

The error indicated arose while launching CDSL servers and the current operation cannot proceed.

What Next

Examine the logs located in the 'system_log' directory for why the failure occured.

Feedback

See Also

- distributed_logging

CMCR-042

(error) failed to connect to CDSL session: (%s)

Description

The error indicated arose while connecting to the CDSL session and the current operation cannot proceed.

What Next

Examine the logs located in the 'system_log' directory for why the failure occured.

See Also

- distributed_logging

CMCR-043

(warning) Environment variable LD_PRELOAD is set and will be synchronised to remote processes

Description

This warning indicates that the UNIX environment variable LD_PRELOAD is set at the manager process to a non-empty value. This may cause the launching of remote workers to fail if the security settings of the computing farm do not allow LD_PRELOAD usage.

If the farm allows LD_PRELOAD to be set, the remote processes launched by the manager process will inherit this variable.

What Next

If the *start_hosts* command fails to launch workers, check the security policy of your computing farm with respect to allowing LD_PRELOAD to be set. Unset LD_PRELOAD in the manager process if needed.

CMCR-044

(warning) The directory %s set by environment variable %s is not writable.

Feedback

Description

This warning indicates that the directory set by the UNIX environment variable is not writable because the directory does not exist or has the incorrect permissions.

What Next

Check the setting of the environment variable.

CMCR-045

(warning) Worker wrapper %s is not an executable script.

Description

This warning indicates that the worker wrapper script used by the Synopsys Testcase Packager is not an executable script or that the script is not found.

What Next

Check your installation of the Synopsys Testcase Packager to ensure that the wrapper script exists and its permissions allow it to be executed.

CMCR-046

(information) distributed worker process on %s (PID = %d) was shut down

Description

This message informs about the distributed worker that was shut down.

CMCR-047

(warning) The '-min_hosts' parameter has been set to '%d' which is greater than the total number of hosts '%d' to be launched. The option is ignored.

Description

This warning message is issued when the *-min_hosts* parameter has been set to a value which is greater than the total number of hosts to be launched. This warning is triggered when this condition is violated either by *start_hosts* or by *set_host_options*. The incorrectly set value will be ignored and the respective command will proceed as if the *-min_hosts* option was not set.

The *-min_hosts* parameter specifies the minimum number of hosts that must come online before returning and must be set to a value less or equal to the total number of hosts to be launched and greater than or equal to 0.

Feedback

What Next

Specify a value less or equal to the total number of hosts to be launched when using the *-min_hosts* option.

See Also

- start_hosts
- set_host_options

CMCR-048

(error) Unexpected worker setup failure. Check error log file %s.

Description

This errors is produced by a distributed worker process that encountered an unexpected error at startup and exited. Please refer to the log file that was created in the distributed working directory. The file can be identified by its name, the format of the name is pt_worker_$hostname_$pid.fail.

What Next

Check the correctness of the distributed analysis setup. If needed send error log file to Synopsys for analysis.

See Also

- start_hosts
- set_host_options

CMCR-101

(warning) Current host has %d cores, reverting the max_cores limit to %d instead of %d.

Description

The *set_host_options* command was specified to set a local process host cores usage limit greater than the total number of physical cores on the machine.

What Next

Rerun PrimeTime on a machine with more cores, if needed.

See Also

- set_host_options

Feedback

CMCR-102

(error) Cannot modify the local process max_cores limit.

Description

The *set_host_options* command was specified to modify the local process host cores usage limit too late in the script execution.

What Next

Use the *set_host_options* command earlier in the script.

See Also

- set_host_options

CMCR-103

(information) The max_cores limit for the local (current) process has been modified by %d to %d.

Description

The *set_host_options* command was specified to increase or decrease the local process host cores usage limit by the value indicated. This message serves as a confirmation of the user setting after validating the available physical cores on the target hardware.

What Next

No further action is needed.

See Also

- set_host_options

CMCR-104

(warning) Using a max_cores setting of %d instead of %d due to licensing restrictions.

Description

The *set_host_options* command was specified to set a local process host cores usage limit that requires additional licenses. However, queries to the license server failed to appropriate the needed license count. However, the cores limit is still be augmented with a value lesser than requested.

Feedback

What Next

Rerun the command when more licenses are available.

See Also

- set_host_options

CMCR-105

(error) The specified cores limit requires additional licenses, but none could be obtained.

Description

The *set_host_options* command was specified to increase the local process host cores usage limit. The change did require additional licenses to be obtained. However, the query to the license server failed to obtain any new licenses. Therefore, the *set_host_options* command failed, and the original cores limit is unmodified.

What Next

Rerun the *set_host_options* command when more licenses are available.

See Also

- set_host_options

CMCR-106

(Warning) The current local process cores limit is already equal to the total number of cores and cannot be further increased.

Description

The *set_host_options* command was specified to increase the local process host cores usage limit. However, the current local process limit is already equal to the available number of cores on the host machine.

What Next

Rerun on a machine with enough cores to match the required limit.

See Also

- set_host_options

Feedback

CMCR-107

(error) Cannot change the value of %s %s.

Description

Cannot change the value of the variable due to the reason given in the error message.

What Next

Check the script where the error occurs, and move the setting of the variable to an appropriate location.

CMCR-108

(error) Cannot launch workers with %s protocol inside a container environment.

Description

The displayed *set_host_options* protocol is not currently supported to launch distributed worker processes inside a container environment.

What Next

Use one of the supported protocols to launch workers inside a container environment. Refer to the man page of *set_host_options*.for details on unsupported protocols.

See Also

- set_host_options

CMCR-109

(error) Cannot find %s under %s

Description

The Synopsys Container script which is used to launch product binary within a container environment was not found under the shown directory path.

What Next

Check your product installation to ensure that the Synopsys Container script is available in the same folder as the application launch script.

CMCR-110

(Information) Docker containerization is disabled for distributed workers

Feedback

Description

The command that produced this message has disabled Docker containerization for distributed workers. Worker processes launched with *start_hosts* will not be launched within Docker containers.

What Next

No action is necessary unless the Docker containerization has been disabled unintentionally.

See Also

- set_distributed_parameters

CMCR-111

(Error) Communication protocol %s is not compatible with Docker containerization

Description

The specified communication protocol passed as an option to the *set_host_options* command is not compatible with running distributed worker processes inside a Docker container.

What Next

Use one of the supported communication protocols in *set_host_options* or disable Docker containerization.

See Also

- set_distributed_parameters
- set_host_options

CMCR-112

(Error) Incompatible host options %s prevents enabling of Docker containerization

Description

The host options defined by the *set_host_options* command use communication protocols that are not compatible with running distributed worker processes inside a Docker container. This prevents enabling of Docker containerization for distributed workers.

Feedback

What Next

Use one of the supported communication protocols in *set_host_options* or disable Docker containerization.

See Also

- set_distributed_parameters
- set_host_options

CMCR-301

(information) child process (%d) failed to reduce its cores usage within %ld seconds of parent request.

Description

This message indicates the child process is running a multi-threaded task which has been instructed by the manager to reduce cores usage but has yet to comply.

What Next

No further action is required at this time.

See Also

- parallel_execute

CMD

CMD-001

(error) Cannot specify '%s' with '%s'.

Description

The listed command options are exclusive. Only one of them can be specified.

What Next

Look at the manpage for this command for more information on command options.

CMD-002

(error) Value for '%s' cannot be negative

Feedback

Description

The value for this option must be greater than or equal to zero.

What Next

Enter the command again with a valid option value.

CMD-003

(error) Cannot specify %s without %s.

Description

One command option requires another.

What Next

Refer to the manual page for this command for detailed information on valid options.

CMD-004

(error) Must specify one of these options: %s.

Description

This command requires that one of the options in the list is specified.

What Next

Refer to the manual page for this command for detailed information on valid options.

CMD-005

(error) unknown command '%s'

Description

The command is not recognized.

What Next

Look for a typographical error in the command. If it is correct, make sure that the program you are running supports the command, or you have the license to use the command.

CMD-006

(error) ambiguous command '%s' matched %d commands:\n \t(%s)

Feedback

Description

The command does not have sufficient characters to distinguish it from other commands. The first three commands which match the abbreviation are listed. To see them all, use the help as follows: if the abbreviation is cmd, type 'help cmd*'. This lists all commands that begin with 'cmd'.

What Next

Type enough characters so the command is unambiguous.

CMD-007

(error) Required argument '%s' was not found

Description

The listed argument to the command might not be omitted.

What Next

Supply the required argument.

CMD-008

(error) value not specified for option '%s'

Description

The listed argument requires a value (that is, it is not a boolean option), and none were supplied.

What Next

Supply a value for the argument.

CMD-009

(error) value '%s' for option '%s' not of type '%s'

Description

The value given for the listed argument is not the correct type. For example, if 'abc' is given for an integer option, this error occurs.

What Next

Supply a compatible value for the argument.

Feedback

CMD-010

(error) unknown option '%s'

Description

The option is not recognized.

What Next

If this is not a simple mistake, retype the command with by the -help option. This lists all of the possible options.

CMD-011

(error) ambiguous option '%s'

Description

The option does not have sufficient characters to distinguish it from other options.

What Next

Type enough characters so that the option is unambiguous.

CMD-012

(error) extra positional option '%s'

Description

The command expects some positional arguments and has already received enough. It might also be the case that this was intended as a dash option and is misspelled.

What Next

Verify that the option given is not a misspelled dash option. If a list is provided directly instead of as a variable, ensure it is enclosed by curly braces or double quotation marks. Use -help with the command to verify which arguments are already given.

CMD-013

(error) %s\n \tUse error_info for more info.

Feedback

Description

A script or complex command failed and there is a stack trace for the failure. The trace points out the source files and loops where the error occurred. The error_info command is used to display this stack.

What Next

Fix the error indicated by error_info.

CMD-014

(error) Invalid %s value '%s' in list.

Description

A list argument is expected to be a common type (like integer or float) and one or more elements cannot be converted to that format.

What Next

Fix the offending list element.

CMD-015

(error) could not open %s file

Description

A script or an output redirect file cannot be opened.

What Next

Verify that the file exists or that you have write access to the directory. Write access depends on the file type.

CMD-016

(error) could not close %s file

Description

A script or an output redirect file cannot be closed.

CMD-017

(warning) duplicate option '%s' ignored.

Feedback

Description

The given option is already issued. This command uses the first value of the option, and subsequent values are ignored.

What Next

Make sure this is the option you want to use. If so, decide which value you want and verify that you get the correct one.

CMD-018

(warning) duplicate option '%s' overrides previous value.

Description

The given option has already been issued. This command uses the last value of the option, and previous values are ignored.

What Next

Make sure that this is the option you want to use. If so, decide which value you want and make sure that you get the correct one.

CMD-019

(error) value '%s' for option '%s' not in range (%s).

Description

The value given for the listed argument is not in the allowable range. For example, if 4 is given for an integer option, which has a range of 1 to 3, this error occurs.

What Next

Supply a compatible value for the argument.

CMD-020

(error) unknown OR extra positional option '%s'

Description

The dash option is not recognized. Further, all positional arguments have already been received. This is most likely a misspelled dash option.

Feedback

What Next

Check to see if the option is misspelled. Look at the entire command, as other options may have misled the interpreter.

CMD-021

(warning) invoked %s outside of a loop

Description

The listed control command (break or continue) was used outside of the context of control structure (such as foreach, while, and so on).

What Next

Look for a loop that ends prematurely or for a misspelled control word.

CMD-022

(warning) Can't create alias named '%s' - %s%s.

Description

An attempt was create an alias with an invalid name. Invalid names include those which match an existing command or procedure, and those which can be converted to a decimal, hexadecimal, or octal number.

What Next

Choose another name. Use 'help' and 'alias' (with no arguments) to see what names are in use.

CMD-023

(error) Alias loop: %s

Description

You have aliases that refer to one another.

What Next

Use the alias command to look at the aliases listed in the diagnostic. Remove the loop and re-execute the command.

Feedback

CMD-024

(error) can't %s "%s": %s

Description

You attempted an operation on a variable which failed. You may have tried to read a non-existent variable (set var). Or, you may have tried to unset a non-existent or application-owned variable. The text of the message will indicate which operation failed.

What Next

Verify that the variable exists with the printvar command. If it's not a user variable, you cannot remove (unset) it.

CMD-025

(error) No manual entry for '%s'

Description

The topic for which you requested man pages does not exist.

What Next

Verify that the topic is spelled correctly.

CMD-026

(error) %s required for the '%s' argument.

Description

The command is incomplete as entered. The specified argument requires a valid object or list of objects.

What Next

Enter the command with valid values for all arguments.

CMD-027

(error) couldn't change working directory to '%s'

Description

The directory which you specified to the cd command is not valid.

Feedback

What Next

Verify that the directory is spelled correctly.

CMD-028

(error) couldn't get working directory name

Description

The pwd command was unable to access the current directory. It is most likely the case that the directory which you are in no longer exists,

What Next

Use the cd command to get into an existing directory.

CMD-029

(warning) no aliases matched '%s'

Description

You specified a pattern to the unalias command, and there are no aliases which match that pattern.

What Next

There is no adverse effect of this action. However, check the spelling of the arguments to unalias to ensure that you removed all of the aliases which you wanted to remove.

CMD-030

(warning) File '%s' was not found in search path.

Description

The 'which' command evaluated an filename argument and the file was not found.

What Next

No adverse effect on the result of the command, but check spelling, etc.

CMD-031

(error) value '%s' for option '%s' is not valid. Specify one of:\n \t%s

Feedback

Description

The value given for the listed argument is not one of the limited allowable strings. This messages lists all of the appropriate values.

What Next

Supply a compatible value for the argument.

CMD-032

(warning) command '%s' requires some options.

Description

No options were given for the command, yet some are required.

What Next

Supply appropriate arguments.

CMD-033

(error) cannot source the current log file.

Description

An attempt to source the log file of the currently running interpreter is not allowed. It would cause the tool to infinitely loop.

What Next

Copy the part of the log to be a source for another file, then source that file instead.

CMD-035

(error) Value for %s cannot be larger than the %s value.

Description

Some commands work in pairs, specifying a maximum and minimum value. The minimum value should be less than the maximum value. For example, never specify a *min_capacitance* which is larger than the *max_capacitance* for the same design or port.

What Next

Remove the old value or use a different value.

Feedback

CMD-036

(error) Value for list '%s' must have %s elements.

Description

The value given for the list argument does not have the correct number of elements. Some commands have list arguments which require either a specific number or an even number of elements. The message will indicate which it is.

What Next

Supply a correct number of elements in the list. If the list is provided directly instead of as a variable, ensure it is enclosed by curly races or double quotation marks.

CMD-037

(error) value '%s' for option '%s' is invalid: must be %s.

Description

The value given for the listed argument is greater than or less than the allowable limit. For example, if 4 is given for an integer option, which is required to be less than or equal to 3, this error occurs.

What Next

Supply a compatible value for the argument.

CMD-038

(information) The '%s' option for %s is unsupported.%s

Description

The option which you specified is not currently supported.

CMD-039

(information) The '%s' variable is unsupported.%s

Description

The variable which you specified is not supported.

What Next

If a replacement variable is specified, use it instead of this one.

Feedback

CMD-040

(information) No %s matched '%s'.

Description

In command or variable search functions (help and printvar), you specified a pattern that did not match any variables or commands.

Note that printvar cannot find a specific array element; it can only find the entire array by name.

What Next

Try using more wildcards (* or ?) in your search pattern.

CMD-041

(information) Defining new variable '%s'.

Description

This message is issued when a variable is set for the first time.

When combined with the *printvar* command, this message can be used to isolate spelling errors in system (application) variables. However, like many debugging features, this has significant CPU cost. Therefore, the feature should only be used interactively or when developing scripts.

This feature is enabled by setting the *sh_new_variable_message* variable to true. When combined with a true value for variables *sh_new_variable_message_in_script* or *sh_new_variable_message_in_proc*, this setting causes a warning message (CMD-042) to be issued, which indicates that the performance of scripts (or Tcl procedures) will be adversely affected. To enable the feature in Tcl procedures, set the *sh_new_variable_message_in_proc* variable to true. To enable the feature in Tcl scripts, set the *sh_new_variable_message_in_script* variable to true.

In the following example, the user has misspelled the variable *sh_continue_on_error* by making it plural. With this feature, debugging is simplified.

```
prompt> set sh_continue_on_errors true
Information: Defining new variable 'sh_continue_on_errors' (CMD-041)
true
prompt> printvar sh*
sh_arch              = "sparcOS5"
sh_continue_on_error = "false"
sh_continue_on_errors = "true"
sh_enable_page_mode  = "false"
sh_new_variable_message = "true"
```

Feedback

```
sh_new_variable_message_in_proc = "false"
sh_product_version    = ""
sh_source_uses_search_path = "false"
prompt> unset sh_continue_on_errors
prompt> set sh_continue_on_error true
true

Application variables are always defined, so if this message appears,
a new user-defined variable has been created.
```

What Next

If attempting to set an application variable, use *printvar* with wildcards to get the correct spelling for the variable.

See Also

- printvar
- sh_new_variable_message
- sh_new_variable_message_in_proc
- sh_new_variable_message_in_script
- CMD-042

CMD-042

(warning) Enabled new variable message tracing -\n \tTcl scripting optimization disabled.

Description

This message is issued when you enable new variable tracing for Tcl scripts or procedures. That occurs when you set the variable *sh_new_variable_message* to TRUE, and when you set the variables *sh_new_variable_message_in_proc* or *sh_new_variable_message_in_script* to TRUE. It warns you that the performance of the application will be negatively mpacted because this feature is costly in CPU time when enabled.

This feature is intended for debugging, and should only be used interactively or when developing scripts. It should not be used in a main flow.

What Next

Set one or more of the variables to FALSE unless you are debugging a script.

Feedback

See Also

- sh_new_variable_message
- sh_new_variable_message_in_proc
- sh_new_variable_message_in_script

CMD-050

(error) Unknown procedure '%s'.

Description

The procedure name argument to *define_proc_attributes* is not a procedure.

What Next

Verify that the argument is correct.

CMD-051

(error) Procedure '%s' cannot be modified.

Description

The procedure that you passed to *define_proc_attributes* is a permanent procedure that cannot be modified.

What Next

The procedure might be part of the application, in which case it was correctly defined with *-permanent*. If it is not part of the application, it is possible that it was erroneously defined with *-permanent*.

CMD-052

(error) Unknown command group '%s'

Description

The command group referenced does not exist. For example, using the *-command_group* option with the *define_proc_attributes* command, and passing in a non-existent command group will raise this error.

What Next

Verify that the correct command group name is being used.

Feedback

CMD-053

(warning) The body of procedure '%s' is protected

Description

You attempted to examine the body of a procedure using *info body*. That procedure was protected by the writer so that it's body cannot be displayed.

What Next

No action required.

CMD-060

(error) Syntax error in argument definition %d for proc '%s'.

Description

Using the *-define_args* option for *define_proc_attributes*, there is some kind of syntax error, for example, an improperly formatted list.

What Next

Use *error_info* to narrow the problem, then reenter the command.

CMD-061

(error) Need at least 2 fields in argument definition %d for proc '%s'.

Description

Using the *-define_args* option for *define_proc_attributes*, an argument definition had insufficient arguments. At least 2 are required: the argument name and the option help text.

What Next

Reenter the argument definition with the correct number of fields.

CMD-062

(error) Unknown %s '%s' in argument definition %d (%s) for proc '%s'.

Description

Using the *-define_args* option for *define_proc_attributes*, either a data type or attribute is invalid.

The allowable data types are string, boolean, int, float, and list. The allowable attributes are required and optional.

What Next

Correct the invalid data and reenter the command.

CMD-063

(error) Illegal name '%s' for Boolean argument definition %d for\n \t proc '%s': must begin with '-'.

Description

Using the *-define_args* option for *define_proc_attributes*, you attempted to create a Boolean argument with a name not preceded by a '-'. Boolean arguments require a leading '-'.

What Next

Correct the argument name and reenter the command.

CMD-064

(warning) Value help ignored for Boolean option %s\n \tin argument definition %d for proc '%s'.

Description

Using the *-define_args* option for *define_proc_attributes*, you tried to add value help for a Boolean argument. Boolean arguments cannot have the value help.

What Next

Remove the value help field for boolean arguments and reenter the command.

CMD-065

(error) Can't specify both 'optional' and 'required' in argument\n \tdefinition %d (%s) for procedure '%s'

Description

This message indicates an attempt to specify conflicting flag values as part of the definition of a procedure argument within the *define_proc_attributes* command.

What Next

Decide whether the argument is optional or required, and remove the opposite flag.

Feedback

CMD-066

(error) Must specify a value for attribute 'values' when using '%s'\noption type as in option %d (%s) for procedure '%s'

Description

This message is issued by the *define_proc_attributes* command when you attempt to define an argument whose value must be one of a set of pre-defined strings (the one_of_string data type), without specifying the set of valid strings.

What Next

If the value type really needs to be one_of_string, pass the values in as a list within the attributes list (i.e. {values {a b c}}).

CMD-067

(error) Invalid attribute specification for attribute '%s'\n \t(%s)\n \tin option %d (%s) for procedure '%s'

Description

This message is issued by the *define_proc_attributes* command. It indicates an incorrect attempt at specifying an attribute for a procedure argument. The reason for the error is included in the message.

What Next

Fix the syntax of the command and try again.

CMD-068

(error) Could not find procedure '%s'. Arguments can't be parsed.

Description

This message indicates an attempt to use the parse_proc_arguments command from within a procedure which has not been defined using define_proc_attributes.

What Next

Define the procedure's arguments using define_proc_attributes and try again.

CMD-069

(error) Could not set '%s(%s)' while parsing arguments in '%s'.

Feedback

Description

This message indicates that the *parse_proc_arguments* command was not able to set the specified Tcl array variable to hold the value of a command option.

What Next

This typically indicates that the variable was read-only. Use a different variable and try again.

CMD-070

(error) %s can only be called from within a procedure

Description

This message indicates an attempt to use the given command from the interpreter command line. Calls to this command are only supported from within a Tcl procedure.

What Next

Create a procedure and call the command from within the scope of the procedure body.

CMD-080

(warning) Command '%s' is disabled.

Description

Although part of the application, the listed command is not currently enabled. The sh_disabled_is_error variable controls the severity of this message. When true, a Tcl error is issued for this command. When false, the command is a no-op.

What Next

Look at the user documentation to determine how various commands are enabled and disabled.

See Also

- sh_disabled_is_error

CMD-081

(information) script '%s'\n \tstopped at line %d due to %s.

Feedback

Description

The execution of a script was terminated. This message tells you which script stopped, the line number where it stopped, and why it stopped.

If the *sh_continue_on_error* variable is false (the default), any Tcl error, either syntax or semantic, stops the script. If *sh_continue_on_error* is false and the *sh_script_stop_severity* variable is W or E, messages of that severity or higher stop the script.

If the *sh_continue_on_error* variable is true, the *sh_script_stop_severity* variable is ignored and the script continues even if there are errors or warnings.

What Next

Use the information in this message to identify and correct the source of errors and warnings. Then reexecute the script.

See Also

- sh_continue_on_error
- sh_script_stop_severity

CMD-082

(information) %s occurred at or before line %d in\n \tscript '%s'.

Description

You receive this message if an error or warning occurs while a script is executing, and the variable *sh_source_emits_line_numbers* is set to E or W. A setting of E causes this message to be issued only if an error occurs, while for a setting of W, this message is issued for both warnings and errors. This message tells you the error or warning and the line and script in which it occurred.

The setting of the *sh_script_stop_severity* variable affects the output of the CMD-082 message. If *sh_script_stop_severity* is set to E, the script stops executing if an error occurs; for a setting of W, the script stops executing if a warning or error occurs. In both cases, message CMD-081 is issued, and takes precedence over CMD-082.

What Next

Use the information in this message to identify and correct the source of errors and warnings. Then reexecute the script.

Feedback

See Also

- sh_script_stop_severity
- sh_source_emits_line_numbers
- CMD-081

CMD-085

(warning) Renaming %s %s cause %s commands which use it to fail.

Description

You receive this message if you rename a command which is not a user-defined Tcl procedure. Renaming commands can be dangerous. Parts of the application are written in Tcl, and if you rename a command that the application is using, it is possible that those parts of the application will not function.

The only true use for *rename* is to wrap a command. For example:

```
shell> rename command1 command1_orig
shell>  \\
  proc command1 {args} {
    # ...
    eval command1_orig $args
    # ...
  }
```

If you use *rename* in this way, it is more likely that application will continue to function correctly. Still, use *rename* with extreme care and at your own risk.

What Next

Consider using *alias*, Tcl procedures, or a private namespace before using *rename*.

See Also

- rename

CMD-086

(error) Could not find command '%s'.

Description

This message indicates that the command name entered does not exist and therefore operation on associated command mode could not be performed.

Feedback

What Next

Check to make sure command name is typed correctly.

CMD-087

(error) The command requires either a command name or a command mode name.

Description

This command requires either a command name or a command mode name to be specified.

What Next

Enter *set_current_command_mode* with the *-command* option flag followed by a command name or the *-mode* option flag followed by a command mode name. These options are mutually exclusive.

CMD-088

(error) Could not find command mode '%s'.

Description

This message indicates that the command mode name entered does not exist and therefore could not be set as the current mode.

What Next

Check to make sure command mode name is typed correctly. *get_command_modes -all* lists all defined command mode names.

CMD-089

(error) Initialization of command '%s' failed.

Description

This message indicates that a failure occurred during initialization and the specified command could not be evaluated.

CMD-090

(error) Initialization of command mode '%s' failed.

Feedback

Description

This message indicates that a failure occurred during initialization of the command mode and the specified command mode could not be made current.

CMD-100

(warning) Detected use of obsolete/unsupported feature. The following\n \twill not be available in a future release of the application:\n \t%s. Use %s instead

Description

You have used a feature which is no longer supported by the application, and the feature is planned to be removed at some future date. The supported method is given in the message.

What Next

Update your command usage as indicated.

CMD-101

(error) Failed to set value of option %s for command %s.

Description

A run of a command such as set_command_option_value failed to set the default or current value of an option. The command option may not have been enabled for value-tracking or a conversion error may have occurred when attempting to set the option value.

What Next

It may be necessary to enable the option for value-tracking.

CMD-102

(error) No such positional option %d for command %s.

Description

An attempt was made to find the positional option of the command at the given position. No such positional option was found. Either the given command has no positional options, or the given position is "out of range". Note that positional options are numbered 0, 1, 2, ... (N-1) where N is the number of postional options of the command.

What Next

Retry the operation using a positional option position that is "in range" for the command.

Feedback

CMD-103

(error) A Severe error has occurred. \n \tTo ensure that the script does not continue, the value of sh_continue_on_error\n \thas been overridden to be false. Your script is being interrupted.\n \tTo see the Tcl call stack for the part of your script which generated\n \tthe Severe error use the error_info command.

Description

A Severe error has occurred during a command execution. To ensure that the script does not continue, the value of sh_continue_on_error has been overridden to be false. Your script is being interrupted. To see the Tcl call stack for the part of your script which generated the Severe error use the error_info command.

What Next

For details on the Severe error please look in your log file. You can also run man on the Severe error id to learn more about the error. Study the Severe error and try to fix the error in your script.

CMD-104

(error) Variable '%s' is not an application variable. Using Tcl global variable.

Description

The specified variable is not declared as an application variable (not returned by get_app_var -list). This message is only generated when the application variable sh_allow_tcl_with_set_app_var is true.

Please see the manpages for get_app_var and set_app_var for additional details.

What Next

Make sure you are using the correct variable name.

CMD-105

(warning) Option '%s' is deprecated, use '%s' instead.

Description

This option is deprecated, you should use a different option for this command feature. The code has automatically used a compatible option setting, but in the future the old option may be removed, so you should update your scripts.

Feedback

What Next

Update your script to use the new option.

CMD-106

(warning) Option '%s' for command '%s' is obsolete. See the command's man page for alternatives.

Description

This option is no longer supported, specifying it has no effect.

What Next

Update your script

CMD-107

(error) Not enough values specified for option '%s', requires %d values found %d.

Description

The listed option requires that the specified number of values and not enough values were supplied.

What Next

Supply all the required values for the option.

CMD-108

(warning) Command %s is obsolete. See the command's man page for alternatives.

Description

This command is obsolete. Calling it has no effect. Please see product documentation for alternatives.

What Next

Update your script as needed.

CMD-109

(warning) Command %s is deprecated. See the command's man page for alternatives.

Feedback

Description

This command is deprecated. Please see product documentation for alternatives.

What Next

Update your script as needed.

CMD-110

(warning) Option '%s' for command '%s' is deprecated. See the command's man page for alternatives.

Description

This option is deprecated, you should use a different option for this command feature.

What Next

Update your script to use the new option.

CMD-111

(error) The write operation failed: %s.

Description

The write operation failed for the reason shown.

CMD-112

(error) duplicate option '%s'

Description

Duplicate options are disallowed for this command option.

What Next

Provide a single entry for this option.

CMD-113

(error) problem running user derived attribute command for %s attribute %s:\n \t%s

Description

Duplicate options are disallowed for this command option.

Feedback

What Next

Provide a single entry for this option.

CMD-114

(severe) Command raised a C++ exception:\n %s

Description

A command raised a C++ exception. This is a tool bug and should be reported to Synopsys. This script will terminate execution and you may try to conintue by saving or attempting some other operation. Other issues are likely.

What Next

Report the issue to Synopsys.

CMD-999

(severe) A Severe error has occurred during testing.

Description

A Severe error has occurred during testing. This should never happen in production.

CNTXT

CNTXT-001

(error) Cannot characterize context in min and max mode.

Description

The design has a minimum and a maximum operating condition defined on it. Context characterization requires only one operating condition be set on the design.

What Next

Set the operating condition for which you want to characterize the context on the design.

CNTXT-002

(information) Characterizing the context for cell '%s'

Feedback

Description

The *characterize_context* command is characterizing the context for the specified cell.

What Next

This is an informational message only. No action is required on your part.

CNTXT-003

(information) Deleting the context for %s

Description

The internal data structures associated with the context of the cell were deleted. Therefore the context cannot be written out (*write_context*) or reported (*report_context*). This occurs when the context is deleted by *remove_context*.

What Next

This is an information message. No action is required unless you want to use *write_context* or *report_context* on the cell for which *CNTXT-003* was issued. Otherwise context must be created by *characterize_context*.

CNTXT-004

(error) This command applies to hierarchical cells only Cell '%s' is a leaf cell.

Description

The specified cell is a leaf cell, and the command you executed applies only to hierarchical cells.

What Next

Run the command again, and ensure that you do not specify a leaf cell.

CNTXT-005

(information) The design has rise/fall qualified exceptions which will not be written out.

Description

The *write_context* command does not write out the rise/fall qualified exceptions in your design. Rise/Fall qualified exceptions are supported only by PrimeTime; neither *write_context* nor *write_sdc* writes them out for either dcsh or dctcl mode.

Feedback

What Next

This is an informational message only. No action is required on your part.

CNTXT-006

(warning) The remove_context command is not supported any more. No action is taken.

Description

The *remove_context* command is not supported any more. You don't need to delete the context.

What Next

This is a warning message only. No action is required on your part.

CNTXT-007

(warning) The '%s' option in characterize_context and remove_context commands is not supported any more. All types of context are characterized or removed.

Description

Different types of context information can be filtered in *write_context* and *report_context* commands. For *characterize_context* command or *remove_context* command, all types of context will be charactrized or removed.

What Next

This is a warning message only. No action is required on your part.

CNTXT-008

(warning) The no_boundary_annotations option in characterize_context command is not supported any more. No action is taken.

Description

The no_boundary_annotations option in *characterize_context* command is not supported any more. It is set to true by default. The parasitics will not be annotated on boundary net.

What Next

This is a warning message only. No action is required on your part.

Feedback

CNTXT-009

(warning) The instance '%s' has already been characterized.

Description

If the context for an instance has already been characterized, the context characterization for this instance will be skipped. If you want to re-characterize context for an instance, please use remove_context to remove the context for the corresponding instance first.

What Next

This is a warning message only. No action is required on your part.

CNTXT-010

(warning) The context for instance '%s' has not been characterized yet.

Description

If the context for an instance has not been characterized, write_context, report_context or set_context_margin can't be used on that instance. Please use characterize_context to characterize context for the corresponding instance first.

What Next

This is a warning message only. No action is required on your part.

CNTXT-011

(error) Cannot characterize context in single operating condition.

Description

The design has a single operating condition defined on it. Context characterization requires on_chip_variation operating condition be set on the design.

What Next

Set the operating condition to on_chip_variation for which you want to characterize the context on the design.

CNTXT-012

(error) write_context doesn't support '%s' format anymore.

Feedback

Description

write_context doesn't support dcsh format anymore, please choose the format among ptsh, dctcl or sdc

What Next

Choose the format among ptsh, dctcl or sdc.

CNTXT-013

(error) Unsupported object type.

Description

set_context_margin only support to be set on object type of cell. If no cell is given, the context margin is set on the top design.

What Next

Set the context marign on cell or design.

CNTXT-014

(warning) The context for pin '%s' has not been characterized yet.

Description

If the context for the instance containing the pin has not been characterized, report_context can't be used on that pin. Please use characterize_context to characterize context for the corresponding instance first.

What Next

This is a warning message only. No action is required on your part.

CNTXT-015

(error) Object list of report_context must be give unless using -parent option.

Description

A collection of pin/port or instance must be given for report_context command unless using -parent option to report context of hyperscale block loaded from top.

What Next

Give proper objects for report_context to report or use -parent to report context of hyperscale block loaded from top.

Feedback

CNTXT-016

(warning) No context data available to report.

Description

report_context command can only be used to report context of objects that is characterized by characterize_context command or context of current design loaded by read_context command.

What Next

Please check whether the context has been characterized or read properly.

CNTXT-017

(error) design/lib_cell/block %s has no instances.

Description

The collection of design/lib_cell or block name given in the cell_block_list of characterize_context/write_context command do not has any instances in the current design.

What Next

Please check that the collection of design/lib_cell or block name you given in the cell_block_list is correct and has instances in the current design.

CNTXT-018

(error) Failed to merge timing context around instance '%s' with reference instance '%s'.

Description

When *characterize_context* with *all_instance* option is used to characterize context for some reference block, the context data internally computed for all its instances are automatically merged into a single overall context for the block.

In order to automatically merge the context for two block instances of the same block, it is required that the instances must be operated in a similar mode and environment, for example, one of the fundamental reqreuirments is that all the instances of the same block must have exactly matching clock and clock topology on the boundary.

Otherwise, their context data cannot be merged together and analysis must be done seperately to cover each operating context seperately in order for the top level analysis to remain valid.

Feedback

It is worth emphasize that ultimately only the users know the design intention and whether or not the different instances of a same physical block are truly operating similarly or equivalently on the same chip under the targeted timing analysis setup.

When merge fails with this error message, the context for the instance noted is discarded and PrimeTime only saves the context covering the reference instance noted.

What Next

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- characterize_context
- write_context

CNTXT-019

(error) Found clock '%s' propagating to instance '%s' through pin '%s', but no matching clock reaching the equivalent pin on instance '%s' of the same block.

Description

When *characterize_context* with *all_instance* option is used to characterize context for some reference block, the context data internally computed for all its instances are automatically merged into a single overall context for the block.

In order to automatically merge the context for two instances of the same block, it is required that the instances must have exact matching clocking scheme. Otherwise, their context data cannot be merged together and analysis must be done seperately to cover each clocking scheme. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the first instance noted.

What Next

You can use *report_timing*, or *report_attribute* commands to verify the message.

Feedback

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- characterize_context
- write_context

CNTXT-020

(information) Timing context around instance '%s' is successfully merged with instance '%s'.

Description

When *characterize_context* with *all_instance* option is used to characterize context for a given block, the context data internally computed for all its instances are automatically merged into a single overall context for the block. This merged context is intended to cover all the instantiation specified.

When merge succeeds with this message, the context for the instance noted is covered by a merged context noted. And a single context is written for all successfully merged instances for a single block level analysis.

What Next

No action is required.

See Also

- characterize_context
- write_context

CNTXT-021

(error) Found clock '%s' propagating to instance '%s', but no matching clock with equivalent pins of same '%s' on instance '%s' of the same block is found.

Feedback

Description

When *characterize_context* with *all_instance* option is used to characterize context for some reference block, the context data internally computed for all its instances are automatically merged into a single overall context for the block.

In order to automatically merge the context for two block instances of the same block, it is required that the instances must have exact matching clocking scheme. Otherwise, their context data cannot be merged together and analysis must be done seperately to cover each clocking scheme. This error message shows which clocking scheme is causing the merging can not proceed. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the first instance noted.

What Next

You can use *report_timing*, or *report_attribute* commands to verify the message.

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- characterize_context
- write_context

CNTXT-022

(error) Found clock '%s' propagating to instance '%s' through pin '%s', but no matching clock reaching the equivalent pin with the same waveform on instance '%s' of the same block.

Description

When *characterize_context* with *all_instance* option is used to characterize context for some reference block, the context data internally computed for all its instances are automatically merged into a single overall context for the block.

In order to automatically merge the context for two block instances of the same block, it is required that the instances must have exact matching clocking scheme. Otherwise,

Feedback

their context data cannot be merged together and analysis must be done seperately to cover each clocking scheme. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the first instance noted.

What Next

You can use *report_timing*, or *report_attribute* commands to verify the message.

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- characterize_context
- write_context

CNTXT-023

(Error) Instance name '%s' is not a valid name.

Description

The instance name given in the -objects option is not a valid name.

What Next

Please check the instance name given in the -objects option is correct.

CNTXT-024

(Error) Use '%s' required '%s' license.

Description

The required license of the command is not available.

What Next

Please check whehter the required license is available.

Feedback

CNTXT-025

(Warning) The config cannot be updated for single block instance '%s'.

Description

The instance was already set as a HyperScale hierarchical block by the *set_hier_config* command. In the HyperScale flow, it is not necessary to use the *characterize_context* or *write_context* command to update single block instance, except for top-level constraints-only extraction.

What Next

In the HyperScale flow, use the *set_hier_config* command to specify a hierarchical block instance and the *write_hier_data* command to write out the context data for the instance.

CNTXT-026

(warning) The directory '%s' has already been used as gbc context output.

Description

This warning message warns you that the given output directory has already been used with gbc context. The original contxt in that directory will be overwritten with the new generated context.

What Next

Specify another output directory if you still want to keep the original context.

CNTXT-027

(error) Context for %s %s has not been characterized yet, can't be removed.

Description

If the context for an object has not been characterized, remove_context can't be used on that object. Please use characterize_context to characterize context for the corresponding instance first.

What Next

Please check whether the corresponding block/cell has been characterized. If the block is characterized with -all_instance option, you must also use -all_instance to remove the context.

Feedback

CNTXT-028

(error) Cannot characterize context for '%s' because it is inside a HyperScale block.

Description

If the block/cell to be characterized is within a hierarchical cell which is configured as HyperScale, it can not be characterized.

What Next

Please characterize lower level blocks in flat run or in HyperScale block level run.

CNTXT-029

(Error) Cannot use write_context for cell '%s' because it is a HyperScale block.

Description

If the instance has been configured as a HyperScale block, *write_context* cannot write context on it.

What Next

Use the *write_hier_data* command to write out the context for a HyperScale block.

CNTXT-030

(Error) Reference name of instances does not match name given in -block.

Description

All instances given in *-instance* option of *characterize_context* must be of the same reference object as given in -block.

CNTXT-031

(Error) Multiple instances must have MIM group name with -name.

Description

If the instances given in *-instance* option of *characterize_context* is a subset of all instances of reference object given in -block, -name option is required.

CNTXT-032

(Error) '%s'.

Feedback

Description

The charactrize_context command can only characterize hierarchical cell/instance and ETM leaf cell/instance.

CNTXT-033

(Error) no cell/instance has been characterized with characterize_context command.

Description

No cell/instance has been characterized with *characterize_context*. To write out context for HyperScale objects, the instances or blocks must be explicitly given in the *cell_block_list* of *write_context*.

What Next

characterize_context

CNTXT-034

(information) The MIM group of instance '%s' has already been updated by characterize_context command.

Description

The instance was already set as a HyperScale hierarchical block by the *set_hier_config* command. If *characterize_context* command is used, then the instance will be updated as required.

What Next

In the HyperScale flow, use the *set_hier_config* command to specify a hierarchical block instance before linking and the *characterize_context* command to specify the block instance after linking.

CNTXT-035

(error) Command ignored because the instances '%s' specified is a mixture of flat blocks and model blocks.

Description

When using the *characterize_context* command to specify the instances set by *set_hier_config* command, the newly set instances can only from HyperScale or Non-HyperScale. They cannot be mixed with each other.

Feedback

What Next

Use *characterize_context* command to specify instances only set by *set_hier_config* or instances excluded from *set_hier_config*.

CNTXT-036

(error) Command ignored because the mim group '%s' specified contains more than one instance.

Description

When using the *characterize_context* command to specify the instances set by *set_hier_config* command, only individual instance can be re-configured. The -instances cannot contain more than one instance.

What Next

Use *characterize_context* command to specify only one instance set by *set_hier_config* or instances excluded from *set_hier_config*.

CNTXT-037

'%s'.

Description

When using the *characterize_context* command to characterize context for ETM leaf cells, only single instance is supported. Characterizing of ETM for MIMs is not supported.

What Next

Use *characterize_context* command to specify only one ETM instance instead of MIMs.

CNTXT-038

(error) write_context doesn't support ptsh, dctcl or sdc format for ETM leaf cell '%s'.

Description

When using the *write_context* command to write context for ETM leaf cells, only binary context format is supported. Other formats like ptsh, sdc and dctcl are not supported.

What Next

Use *write_context* command to specify only the gbc format.

Feedback

CNTXT-039

(warning) Clock '%s' is one of the multiple clocks reaching the same block pin '%s' and will be merged into '%s', merged context will be applied.

Description

When there are multiple top clocks entering the same block clock port during block level timing analysis, the context of the clocks with the same attributes will be merged and the merged context will be applied.

CNTXT-040

(information) Wrote context data for instance '%s' in directory '%s'.

Description

When *write_context* is used for single instance, the context data for instance is written into specified directory.

What Next

No action is required.

See Also

- characterize_context

CNTXT-042

(information) Wrote merged context data for reference instance '%s' in directory '%s'.

Description

When *write_context* is used for multiple instances, the merged context data for reference instances are written into specified directory.

What Next

No action is required.

See Also

- characterize_context

Feedback

CNTXT-044

(information) Wrote constraints for instance '%s' in directory '%s'.

Description

When *write_context* is used for single instance, the constraints data for block instance is written into specified directory.

What Next

No action is required.

See Also

- characterize_context

CNTXT-046

(information) Wrote merged constraints for reference instance '%s' in directory '%s'.

Description

When *write_context* is used for multiple instances, the merged constraints data for reference instances are written into specified directory.

What Next

No action is required.

See Also

- characterize_context

DA

DA-001

(Error) No hierarchical cell is found with name '%s'.

Description

You receive this message if the -exclude_instances option is used with wrong instance name argument. The given name does not refer to a hierarchical cell.

Feedback

What Next

Check the instance name and reissue the command with correct instance names.

See Also

- set_hier_config
- start_hosts

DA-002

(Warning) Some of the user specified block exclusions are ignored for distributed analysis.

Description

You receive this message if the *set_hier_config -exclude_instances* option is used previously but some or all of the hierarchical instances are ignored for hierarchical distributed analysis partitioning. This can occur because either (a) the specified hierarchy does not have parasitics of its own or (b) the specified hierarchy is not the top level parasitic instance.

What Next

Check the instance name and reissue the *set_hier_config* command with correct instance names.

See Also

- set_hier_config
- start_hosts

DA-003

(Error) The command '%s' is not supported in the distributed analysis manager.

Description

You receive this message if hierarchical distributed analysis is enabled and you have used a command which can not be executed by the distributed analysis manager.

What Next

Check if the command can be used in any block context.

Feedback

See Also

- set_hier_config
- start_hosts

DA-004

(Error) Untranslatable block/instance/design specified.

Description

You receive this message if current_partition was supplied wrong instance name(s) argument. The given name(s) does not refer to a hierarchical cell(s).

What Next

Check the instance name and reissue the command with correct instance names.

See Also

- set_hier_config
- start_hosts

DA-005

(Error) No user commands specified to be executed.

Description

You receive this message if no user commands were supplied to current_partition to be executed at the worker partitions.

What Next

Specify set of commands to be run on partitions.

DA-006

(Error) Remote execution output not available at the manager process.

Description

You receive this message if the remote execution command output could not be captured. Unable to generate command execution reports at the manager process.

Feedback

What Next

Check the command log files of the worker partitions in focus.

DA-007

(Error) Attribute '%s' is not supported in distributed analysis manager.

Description

You receive this message if the hierarchical distributed analysis is enabled and you are trying to access an attribute which can not be accessed by distributed analysis manager.

What Next

Check if the attribute can be used in any block context.

See Also

- set_hier_config
- start_hosts

DA-008

(Error) Option '%s' is not supported with command '%s' in distributed analysis manager.

Description

You receive this message if hierarchical distributed analysis is enabled and you have used an option with a command which can not be executed by the distributed analysis manager.

What Next

Check if the option could be used with the command in any block context.

See Also

- set_hier_config
- start_hosts

DA-009

(Error) Partitions have not been started up to run the command.

Feedback

Description

You receive this message if no partitions are started up to take any task. Please run update_timing to start up partitions in remote hosts.

What Next

Run update_timing before running any distributed command in hierarchical distributed analysis.

DA-010

(Warning) Switching pt_shell out DHA mode unsupported.

Description

pt_shell operates in only one mode DHA/DMSA/AMV at one point in time. Switching out of DHA mode and going back to normal mode is not permitted.

See Also

- set_hier_config
- start_hosts

DA-011

(Error) Design already read and linked cannot run in distributed mode.

Description

You receive this message if you try to enable hierarchical distributed analysis after reading in the design.

What Next

Set *set_hier_config* before reading the design.

See Also

- set_hier_config
- start_hosts

DA-012

(Error) Distributed save could not be performed on partial set of partitions.

Feedback

Description

You receive this message if save_session command has been issued when only a subset of partitions have been restored.

See Also

- save_session

DA-013

(Error) Partition "%s" was not restored with the design.

Description

You receive this message if you are trying to set focus and run commands on a partition which was not restored and thus is not linked to the design.

See Also

- restore_session

DA-014

(Error) Unable to access changelist file %s from %s.

Description

You receive this message if in distributed hierarchical flow either manager or worker machines fail to access temporary eco changelist files dumped by one of the machines.

What Next

Check if the *hier_distributed_working_directory* has enough space left. Try doing ECO in a fresh session.

DA-015

(Error) Partition '%s' could not be restored because '%s' is not accessible.

Description

You receive this message if you are trying to restore a partition which does exist in saved image.

Feedback

See Also

- restore_session

DA-016

(Error) Top partition was not restored from saved session.

Description

You receive this message if Top partition was not requested to be restored in DHA mode.

What Next

Include Top partition in list of partitions to be restored.

DA-017

(Error) Design not available to run hierarchical distributed analysis.

Description

You receive this message if design has not be loaded and linked to distributed analysis manager.

What Next

Load and link the design to distributed analysis manager before issuing any distributed command.

DA-018

(Warning) Started (%d) additional processes on the manager to support (%d) partitions.

Description

You received this message if additional processes had to be started on the manager's host to run all the partitions in the design.

What Next

Please rerun with modified *set_host_options*. Otherwise, the performance of the distributed analysis will not be optimal.

DA-019

(fatal) Internal system error in partition(s) ' %s'. Fatal stack trace available in; %s

Feedback

Description

While executing commands in distributed analysis mode, one or more partition experienced a critical internal error causing it to terminate.

What Next

Examine the worker logs to determine the cause of error and refer to Synopsys for further support.

DA-020

(Error) Insufficient %s resources available to analyze %d partitions.

Description

You receive this message if the number of licensed worker processes online is less than the number of partitions to be analysed due to a lack of licenses or an inability to bring processes online.

What Next

Please rerun with sufficient resources to run the number of partitions determined in the design. If the problem is due to licenses please contact Synopsys for additional licenses or if the problem is due to process startup please modify the *set_host_options* specified.

DA-021

(Error) List values are not supported with option '%s' in '%s' command. Use collections.

Description

You receive this message if hierarchical distributed analysis is enabled and you have used an option values in list form instead of collection with a command which can not be correctly executed by distributed analysis manager with values in list form.

What Next

Provide the option values in collection form.

See Also

- set_hier_config
- start_hosts

Feedback

DA-022

(Error) Only Pin, Port, Cell and Net objects are supported in collection.

Description

You receive this message if hierarchical distributed analysis is enabled and you have used a collection objects other than Pin, Port, Cell and Net.

What Next

Check if the option could be used with the command in any block context.

See Also

- set_hier_config
- start_hosts

DA-023

(Error) Partitions information does not exist. Skipping '%s' command.

Description

You receive this message if no partitions are started up to take any task. This happen if you have not run update timing before the command or your design is non-hierarchical.

What Next

Run update_timing before running any distributed command in DHA. Verify the design.

DA-024

(Error) update_noise failed for distributed analysis.

Description

You receive this message because there was an error happenned during "update_noise".

What Next

Check the out.log of both top and block partitions for details.

DA-026

(Error) netlist/constraint inconsistency detected between manager and top/block partitions

Feedback

Description

You receive this message because there was an inconsistency between the manager netlist/constraint and the top/block session that is being loaded.

What Next

Check the out.log of both top and block partitions for details.

DA-027

(Warning) *Hierarchical distributed analysis* is not fully supported by *set_advanced_analysis*.

Description

You receive this message to inform you *hierarchical distributed analysis* is not fully supported by *set_advanced_analysis*.

What Next

Do not use *set_advanced_analysis* after enabling hierarchical distributed analysis. Alternatively, user can set *timing_enable_auto_mux_clock_exclusivity* to false.

DA-028

(Error) Cannot combine 'report_timing' with 'get_timing_paths' in DMSA when variable 'timing_report_include_eco_attributes' is set to true. Eco attributes will not be reported.

Description

You receive this message because you are using command *report_timing* combined with *get_timing_paths* under DMSA mode in the manager and you have set the value of variable *timing_report_include_eco_attributes* to true. These options are incompatible. The report will not include the ECO attributes.

What Next

Use *remote_execute* to run *report_timing* with these settings on workers. You have to also set variable *timing_report_include_eco_attributes* to true on the workers. Othewise use *report_timing* without *get_timing_paths* or set value of *timing_report_include_eco_attributes* to false.

See Also

- timing_report_include_eco_attributes
- remote_execute

Feedback

DA-029

(Error) Context inconsistency detected between top and block partitions

Description

You receive this message because there was an inconsistency between the top and block session context.

What Next

Make sure that block session has the same context generated by the top session being loaded.

DA-030

(Error) The variable hier_characterize_context_mode is set to constraints_only. Thus, design cannot be run in distributed mode.

Description

You receive this message if you try to enable hierarchical distributed analysis after setting hier_characterize_context_mode to constraints_only.

What Next

Dont set *hier_characterize_context_mode* in hierarchical distributed analysis.

See Also

- hier_enable_distributed_analysis

DA-031

(Error) The variable hier_create_template_scripts is set to true. Thus, design cannot be run in distributed mode.

Description

You receive this message if you try to enable hierarchical distributed analysis after setting hier_create_template_scripts to true.

What Next

Dont set *hier_create_template_scripts* in hierarchical distributed analysis.

Feedback

See Also

- hier_enable_distributed_analysis

DA-032

(Error) The number of workers online '%d' is less than the number of workers needed '%d'.

Description

You receive this error if the number of hosts required to run distributed analysis, is less than the number of hosts online.

What Next

If the -timeout option to the start_hosts command was used and the timeout expired before all workers came online, then increase the timeout specified to allow more worker processes come online.

If the -min_hosts options to the start_hosts command was used, then increase the value specified to at least the number of workers indicated as needed. OR Remove -min_hosts options.

DA-033

(Error) invalid %s '%s' in affinity specification.

Description

You receive this message if hierarchy name or host option name in affinity specification in set_hier_config command is incorrect i.e. hierarchical design corresponding to hierarchy name specified does not exist or host option name specified does not exist.

What Next

Re-run the command with correct values.

See Also

- set_hier_config
- start_hosts
- report_host_usage
- set_host_options

Feedback

DA-034

(Warning) empty affinity specification.

Description

The affinity specification is empty so it will be treated as if no affinity has been specified.

What Next

If you intended to specify an affinity, re-create it specifying a valid affinity.

See Also

- set_hier_config
- start_hosts
- report_host_usage
- set_host_options

DA-035

(Error) The -affinity option can only be used with -partitions option.

Description

You receive this message if partition option is missing with affinity option.

What Next

Re-run the command with partitions options.

See Also

- set_hier_config
- start_hosts
- report_host_usage

DA-036

(Warning) host option name %s specified in affinity does not exist.

Description

You receive this message during restore_session if host option name specified in affinity specification does not exist.

Feedback

What Next

If you are intended to use the host option for affinity then set appropriate host options and restore the session.

See Also

- set_hier_config
- start_hosts
- report_host_usage
- set_host_options

DA-037

(Warning) invalid instance name '%s' in partition specification. Not consider the instance for partitioning.

Description

You receive this message if instance name in partition specification in set_hier_config command is incorrect i.e. hierarchical design corresponding to instance name specified does not exist

What Next

Re-run the command with correct values.

See Also

- set_hier_config

DA-038

(Error) Can not set resource affinity before design is linked.

Description

You receive this message if design has not be loaded and linked.

What Next

Load and link the design at the distributed analysis manager process before setting resource affinity.

Feedback

DA-039

(Warning) full path recalculation with full clock expanded pba reporting is not supported in Distributed Analysis. Thus showing clock path upto partition boundary.

Description

You will get this message when the pba_recalculte_full_path variable is set to true and full clock expanded pba reporting is queried.

What Next

Set pba_recalculte_full_path variable to false and re-issue the query.

DA-040

(Error) We have encountered issues with '%s' passed with 'set_hier_resource_limits' command.\n '%s' seem to be insufficient to analyze design. Please refine them.

Description

You receive this message if the parameters to set_hier_resouce_limits are not well configured.

What Next

Try increasing the memory/cores passed along with set_hier_resource_limits

See Also

- set_hier_config

DA-041

(Error) Cannot run update_timing -full because the compute resources for partitions were released.

Description

You enabled top-only mode in the distributed flow and the compute resources for block partitions were released in the previous timing update.

What Next

Set the *hier_enable_release_resources_in_top_only_flow* variable to *false* if you need to update the timing multiple times in the distributed top-only flow.

Feedback

DA-042

(Error) Cannot update timing because the compute resources for block partitions were released.

Description

You enabled top-only mode in the distributed flow and the compute resources for block partitions were released in a previous timing update.

What Next

Set the *hier_enable_release_resources_in_top_only_flow* variable to *false* if you need to update the timing multiple times in the distributed top-only flow.

DA-043

(Error) Cannot perform reporting because timing is not updated. Skipping '%s' command.

Description

For some reason, timing was not updated in the distributed flow.

What Next

Please check previous error messages to understand the reason behind this error.

DA-044

(Error) Cannot update noise because the compute resources for block partitions were released.

Description

You enabled top-only mode in the distributed flow and the compute resources for block partitions were released in a previous timing update.

What Next

Set the *hier_enable_release_resources_in_top_only_flow* variable to *false* if you need to update the timing/noise multiple times in the distributed top-only flow.

DA-045

(Warning) In distributed analysis, the "Net Interconnect Area" and "Design Area" reported by the report_constraint command are pessimistic.

Feedback

Description

In HyperScale distributed analysis, the "Net Interconnect Area" and "Design Area" reported by the *report_constraint* command are pessimistic due to double-counting the overlap between the top and block levels.

What Next

Be aware that the reported areas can be less than the reported area. No further action is required.

DA-046

(Error) In HyperScale distributed analysis, report_timing was used with the -path_type full_clock_expanded option while operating on a path collection that did not have full_clock_expanded data.

Description

In HyperScale distributed analysis, the *report_timing* command, when operating on a path collection, supports the *-path_type full_clock_expanded* option only if the path collection was also generated with the *-path_type full_clock_expanded* option.

Attempting to report *full_clock_expanded* data that is unavailable in a path collection triggers an error, as in the following example:

```
set mypaths [get_timing_paths -max_paths 200000 -nworst 10]
report_timing $mypaths -path_type full_clock_expanded  ->  Error
```

What Next

To include *full_clock_expanded* data in the path collection during HyperScale distributed analysis, use the *-path_type full_clock_expanded* option when you gather the paths:

```
set mypaths [get_timing_paths -max_paths 200000 -nworst 10 \\
  -path_type full_clock_expanded]
report_timing $mypaths -path_type full_clock_expanded
```

Alternatively, you can get the full report directly without using a path collection:

```
report_timing -path_type full_clock_expanded -max_paths 200000 -nworst 10
```

DA-047

(Error) DMSA and %s doesn't work together.

Description

You receive this message if the DMSA is enabled and you are trying to enable distributed_enable_analysis or hier_enable_distributed_analysis.

Feedback

What Next

Check if DMSA is enabled.

DA-048

(Error) The script %s doesn't exist.

Description

The script mentioned in start_dsta command is wrong.

What Next

Input correct path for the script file.

DA-049

(Error) Option '%s' is not supported with command '%s' in distributed analysis mode.

Description

You receive this message if hierarchical distributed analysis is enabled and you have used an option with a command which can not be executed in distributed analysis engine.

What Next

Check if the you can provide spef/gpd version of the command.

DA-050

(Error) Cannot set timing_aocvm_enable_analysis variable in distributed analysis

Description

You receive this message if distributed analysis is enabled and you have tried to enable aocvm analysis by setting timing_aocvm_enable_analysis variable.

What Next

Please check the script

DA-051

(Error) Attribute %s is not supported in filter_collection.

Feedback

Description

You receive this message if you are trying to access remotely_available attribute in filter collection when distributed_enable_analysis is enabled

---

DA-052

(Warning) Following license was not found for distributed analysis '%s'.

Description

You receive this message if license has not been activated for distributed analysis

What Next

Check which licenses are activated using list_licenses command

---

DA-053

(Information) Setting distributed_working_directory variable to '%s'.

Description

In case distributed_working_directory is not explicitly set by user, the tool sets it to a default value during start_hosts call. If user wants to specify their own, please make sure to set it before calling start_hosts command.

DA-054

(Error) Minimum 2 cores are required in Hypergrid Analysis.

Description

You receive this message because you are using command *set_host_options* with specified max cores option which is less than two. The local process host cores usage limit by the value indicated.

What Next

Use the *set_host_options* with max_cores option set to 2 in HyperGrid Master

See Also

- set_host_options

Feedback

DA-057

(Error) Working directory contain inaccessible file or directory '%s'.

Description

You receive this message if present working directory has a file or directory which doesn't have read/access permission.

What Next

Please check the present working directory for such file or directory.

DA-060

(Error) The netlist connectivity check failed.

Description

You receive this error message if the netlist was partitioned incorrectly by HyperGrid. This is not a user error.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

DA-061

(Error) The following net segment exists in a secondary MIM hierarchy but does not exist in the primary MIM hierarchy: p_hier:%s,s_hier:%s,p_net:MISSING,s_net:%s

Description

You receive this error message if the netlist was partitioned incorrectly by HyperGrid. This is not a user error.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

DA-062

(Error) The cell of the following pin does not exist in the hierarchy: level:%d,hier:%s,net:%s,pin:%s

Feedback

Description

You receive this error message if the netlist was partitioned incorrectly by HyperGrid. This is not a user error.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

DA-063

(Error) The following net segment exists both in the primary and the secondary MIM hierarchies, and it's connected to a cell in the primary MIM hierarchy, which is missing from the secondary MIM hierarchy: level:%d,p_hier:%s,s_hier:%s,p_net:%s,s_net:%s,p_cell:%s,s_cell:MISSING

Description

You receive this error message if the netlist was partitioned incorrectly by HyperGrid. This is not a user error.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

DA-064

(Error) The following net segment exists both in the primary and the secondary MIM hierarchies, and it's connected to a pin in the primary MIM hierarchy, which is missing from the secondary MIM hierarchy: level:%d,p_hier:%s,s_hier:%s,p_net:%s,s_net:%s,p_pin:%s,s_pin:MISSING

Description

You receive this error message if the netlist was partitioned incorrectly by HyperGrid. This is not a user error.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

DA-065

(Error) The following primary net's global net has %s segments than the secondary net's global net: level:%d,p_hier:%s,s_hier:%s,p_net:%s,s_net:%s,#p_g_net_segments:%d,#s_g_net_segments:%d\n Primary net's global net segments:\n%s\n Secondary net's global net segments:\n%s\n

Feedback

Description

You receive this error message if the netlist was partitioned incorrectly by HyperGrid. This is not a user error.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

DA-066

(Error) The following net segment exists both in the primary and the secondary MIM hierarchies, but a net segment of the primary net's global net exists in the primary but not in the secondary MIM hierarchy: level:%d,p_hier:%s,s_hier:%s,p_net:%s,s_net:%s,p_g_net_segment:%s,s_g_net_segment:MISSING

Description

You receive this error message if the netlist was partitioned incorrectly by HyperGrid. This is not a user error.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

DA-067

(Error) min_partition can not be less than 2.

Description

You receive this error message if minimum number of partitions is less than or equal to 1.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

DA-068

(Error) Minimum number of partitions can not be more than NoOfPartitions.

Description

You receive this error message if minimum number of partitions is greater than Number of Partitions provided by the user.

What Next

Please provide this and any previous "DA-###" errors to Synopsys.

Feedback

DA-069

(Information) Enabling hypergrid pre scan.

Description

You receive this information message if you use the enable_hypergrid_pre_scan command.

DA-070

(Information) Disabling hypergrid pre scan.

Description

You receive this information message if you use the disable_hypergrid_pre_scan command.

DA-071

(Error) No Master arc info found for selective disabling, using any loop arc for loop breaking.

Description

You receive this message if there is no selective loop arc breaking at distributed workers to be in sync with arcs broken at master. This will happen under gvar dsta_ignore_loop_break_sync set to true.

DB

DB-1

(error) File is not a DB file.

Description

The identified file was not in the DB file format.

What Next

Check to see what format the file is in, and read it with the appropriate command. For example, edif files can be read into *dc_shell* with the *read -format edif <filename>* command.

Feedback

DB-3

(warning) Can't locate file '%s'.

Description

This warning message will be printed out the first time if we can not resolve a link to a given file. In the absense of the given file, there will be some unresolved references.

What Next

Check the link_library and the search_path variables and set their value accordingly.

DB-4

(error) Open gen_state (0x%x) -- %s object '%s' (0x%x)\n attach '%s' id = %d

DB-5

(error) Limit exceeded: Cannot create attribute %s for class %s, so program cannot continue.

Description

This message appears when the internal limit of 32k attributes per database object is exceeded. Once this limit is exceeded, work in progress cannot be saved and the program cannot continue.

What Next

Check the scripts to see if an excessive number of *create_attribute* commands are run with unique attribute names. Try to reuse names where possible. If many scripts are run in one large session, attempt to break up the single long run into a number smaller runs, saving your work each time.

DB-6

(error) Limit exceeded: Cannot create attach %s for class %s, so program cannot continue.

Description

This message appears when the internal limit of 32k types of attaches per database object is exceeded. Once this limit is exceeded, work in progress cannot be saved and the program cannot continue.

Feedback

What Next

If many scripts are run in one large session, attempt to break up the single long run into a number smaller runs, saving your work each time.

DBPG

DBPG-101

(warning) Missing %s attribute for internal PG pin '%s' of cell '%s' which is defined as fine-grain switch cell in the library. This internal PG pin is not considered as an internal switchable PG pin during power analysis.

Description

Liberty PG pin syntax provides the syntax for modeling fine-grain switch cell in the library. A PG pin is considered as an internal switchable power or ground if the PG pin has pt_type of internal_power or internal_ground and it has both switch_function and pg_function attributes defined. If either attribute is missing, the internal PG pin is not considered as an internal switchable PG pin in PrimeTime; the value of the other switch related DB attribute is ignored.

The switch_function attribute specifies the Boolean condition under which the cell switches off the controlled design partitions. It must refer to valid input signal pins of the cell. The pg_function attribute is used for the switch cell's internal and virtual power output pins to represent the propagated power level through the switch as a function of the input power or ground pin.

When either switch_function or pg_function attribute is missing for an internal_power or internal_ground PG pin of a fine-grain switch cell, the internal PG pin is not considered as an internal switchable PG pin during power analysis. There is no impact on timing analysis. This can result in overestimation of power consumption for the fine-grain switch cell, as PrimePower cannot not detect when a fine-grain switch cell is switched off.

What Next

Refer to Liberty modeling for fine-grain switch cell. Provide switch_function and pg_function definitions in the .lib file for the internal switchable PG pin of a macro switch cell.

DBPG-102

(error) The pin '%s' specified in '%s' as defined for switch_function of PG pin '%s' is not defined for library cell '%s'. The switch_function cannot be interpreted thus ignored.

Feedback

Description

The switch_function attribute specifies the Boolean condition under which the cell switches off the controlled design partitions. It must refer to valid input signal pins of the cell.

If the switch_function attribute cannot be interpreted, the internal PG pin is not considered as an internal switchable PG pin during power analysis. There is no impact on timing analysis. This can result in overestimation of power consumption for the fine-grain switch cell, as PrimePower cannot detect when a fine-grain switch cell is switched off.

What Next

Refer to Liberty modeling for fine-grain switch cell. Provide a correct specification for the switch_function attribute in the .lib file for the internal switchable PG pin of a macro switch cell.

DBPG-103

(error) Invalid specification '%s' for switch_function of PG pin '%s' for library cell '%s'. The switch_function is ignored.

Description

The specification for the switch_function is not a valid Boolean expression. The internal PG pin is not considered as an internal switchable PG pin during power analysis. There is no impact on timing analysis. This can result in overestimation of power consumption for the fine-grain switch cell, as PrimePower cannot detect when a fine-grain switch cell is switched off.

What Next

Check the Boolean expression for the switch_function.

Refer to Liberty modeling for fine-grain switch cell. Provide a correct specification for the switch_function attribute in the .lib file for the internal switchable PG pin of a macro switch cell.

DBPG-104

(error) Boolean expression exceeds length limit for switch_function of PG pin '%s' for library cell '%s'. The current length limit is 2048 characters. The switch_function is ignored.

Description

The current length limit for switch_function Boolean expression is 2048 characters.

The internal PG pin is not considered as an internal switchable PG pin during power analysis. There is no impact on timing analysis. This can result in overestimation of power

Feedback

consumption for the fine-grain switch cell, as PrimePower cannot detect when a fine-grain switch cell is switched off.

What Next

Check the Boolean expression for the switch_function. If needed, contact Synopsys Customer Support Center.

Refer to Liberty modeling for fine-grain switch cell. Provide a correct specification for the switch_function attribute in the .lib file for the internal switchable PG pin of a macro switch cell.

DBPG-105

(error) Unknown function operator '%c' in boolean expression '%s' for switch_function of PG pin '%s' for library cell '%s'. The switch_function is ignored.

Description

The operator used in the Boolean expression for switch_function is not supported. The following operators are allowed: (,), ~, &, |, ^, !.

The internal PG pin is not considered as an internal switchable PG pin during power analysis. There is no impact on timing analysis. This can result in overestimation of power consumption for the fine-grain switch cell, as PrimePower cannot detect when a fine-grain switch cell is switched off.

What Next

Check the Boolean expression for the switch_function.

Refer to Liberty modeling for fine-grain switch cell. Provide a correct specification for the switch_function attribute in the .lib file for the internal switchable PG pin of a macro switch cell.

DBPG-106

(error) Missing close bracket in Boolean expression '%s' for switch_function of PG pin '%s' for library cell '%s'. The switch_function is ignored.

Description

The close bracket (]) in the Boolean expression is missing for switch_function.

The internal PG pin is not considered as an internal switchable PG pin during power analysis. There is no impact on timing analysis. This can result in overestimation of power consumption for the fine-grain switch cell, as PrimePower cannot detect when a fine-grain switch cell is switched off.

Feedback

What Next

Check the Boolean expression for the switch_function.

Refer to Liberty modeling for fine-grain switch cell. Provide a correct specification for the switch_function attribute in the .lib file for the internal switchable PG pin of a macro switch cell.

DBPG-107

(warning) Unable to interpret '%s' as defined for pg_function of PG pin '%s' for library cell '%s'. The pg_function is ignored.

Description

The tool failed to interpret the specific pg_function as defined in the library. The pg_function attribute is used for the switch cell's internal and virtual power output pins to represent the propagated power level through the switch as a function of the input power or ground pin. To derive the switch input from the pg_function, PrimePower requires that the pg_function attribute resolves to only one valid external power or ground pin with matching pg_type. Multiple PG pins in pg_function is not supported.

If there is an unresolved pg_function, PrimePower assumes that the external supply is always on. The fine-grain switch cell can still be switched off internally by its control signal.

What Next

Check the expression for the pg_function.

Refer to Liberty modeling for fine-grain switch cell. Provide a correct specification for the switch_function attribute in the .lib file for the internal switchable PG pin of a macro switch cell.

DBPG-108

(warning) Attribute pg_function for internal PG pin '%s' has unmatched pg_type (library cell '%s'). The pg_function ('%s') is ignored.

Description

The pg_function attribute is used for the switch cell's internal and virtual power output pins to represent the propagated power level through the switch as a function of the input

Feedback

power or ground pin. PrimePower requires that the pg_type must be matched between internal PG pin and its related external PG pin:

- If internal PG has type of internal_power, the PG pin as specified in pg_function must have type of primary_power
- If internal PG has type of internal_ground, the PG pin as specified in pg_function must have type of primary_ground

If there is an unresolved pg_function, PrimePower assumes that the external supply is always on. The fine-grain switch cell can still be switched off internally by its control signal.

What Next

Check the expression for the pg_function.

Refer to Liberty modeling for fine-grain switch cell. Provide a correct specification for the switch_function attribute in the .lib file for the internal switchable PG pin of a macro switch cell.

DBPG-109

(warning) Control pin '%s' in muxed pg_function is not constant, pg_function is ignored.

Description

Control pin in muxed pg_function is always constant.Pg function is ignored , if control_pin in muxed pg_function is not constant.

What Next

Check the expression for the pg_function.

Refer to Liberty modeling for fine-grain switch cell. Provide a correct specification for the switch_function attribute in the .lib file for the internal switchable PG pin of a macro switch cell.

DBR

DBR-001

(error) Cannot read file '%s'.

Description

The file you specified either does not exist or you do not have read access to the file.

Feedback

What Next

Check the search_path or use the *file* command to verify the existence and other attributes of the file.

DBR-002

(information) Errors reading file '%s'.

Description

Errors occurred while reading the specified file.

What Next

Check previous messages, which indicate what went wrong and what action you can take to correct the problem. If there are no messages preceeding DBR-002, then the file is most likely corrupt.

DBR-003

(warning) Design '%s' (file '%s') is already registered. Remove the design before rereading.

Description

While reading a design from a file, that design/file combination was found in memory. This means that the file was read previously.

What Next

If the file has changed and you want to reread it, remove the design using the *remove_design* command, then reread the file.

DBR-004

(warning) Library '%s' (file '%s') is already registered.

Description

While reading a DB file, a library/file combination that is already in memory was found. This means that the file was read previously.

What Next

If the file has changed and you want to reread it, you can remove the library using the *remove_lib* command, then reread the file. However, in the process, if a linked design

references this library, that design will need to be unlinked and will need to be completely rebuilt.

DBR-005

(information) Design '%s' not loaded.

Description

While reading in a design, some inconsistencies were found, so the design was not loaded. It's likely that the db file has errors, such as multiple nets with the same name on a single design.

What Next

Check previous messages which will indicate what went wrong, and what action you can take to correct the problem. Usually, the application which created the db is the cause.

DBR-006

(error) Unknown pin '%s' makes instance '%s' of '%s' in design '%s' inconsistent with previous instances.

Description

While reading in a design, an instance of a design is inconsistent with previous instances because a pin is not found.

What Next

Make sure that the DB is valid.

DBR-007

(warning) Found unsupported LSI reference '%s' to '%s' in design '%s'. The linker will not be able to resolve this reference.

Description

While reading in a design, an instance of a design was found to be derived from an LSI netlist. This tool only supports fully name-based references from LSI netlists. Order-based or mixed order and name based references are not supported.

What Next

Use another Synopsys tool to read the DB, link it, and write it out to a new DB file. This will resolve the naming issue.

Feedback

DBR-008

(error) Cannot remove library '%s': %s%s%s

Description

The library contains objects which are being referenced. For example, some cells may used in the current design, or a wire load model may be in use. If a QTM model is being created, and it is referencing the library, then it must be saved before the library can be removed.

Each reason why the library cannot be removed is listed.

What Next

Remove the designs with the *remove_design* command before using *remove_lib*, since a design is the source of most library references. Other causes, like QTM model creation, may require other actions.

DBR-009

(warning) Found name-based LSI reference '%s' to '%s' in design '%s'. The linker might not be able to resolve this reference.

Description

While reading in a design, an instance of a design was found to be derived from an LSI netlist. The reference is fully name-based. However, even in the case of name-based references, the linker might not be able to resolve references. The LSI netlist allows unconnected pins to be omitted from the reference, so, for example, an FD1 with D, CP, and Q pins connected, would be represented with the QN pin missing. The linker will indicate that the reference has too few ports.

What Next

Use another Synopsys tool (like Design Compiler) to read the DB, link it, and write it out to a new DB file. This will resolve the missing pins issue.

DBR-010

(error) Cannot access temp directory '%s'%s.

Description

The read process utilizes a temporary directory to create transient files. These files are deleted when the read process completes. The name of the directory is found in the variable 'pt_tmp_dir'. In this case, the program was unable to create files in that directory.

Feedback

What Next

Verify that the specified directory exists, is writeable, and that the disk has some space available. If no space is available, try setting pt_tmp_dir to an alternate directory.

DBR-011

(error) Problem in read_%s: %s.

Description

The read process detected an error, which is detailed in the message. Some are intermediate file problems (see DBR-010); others are process related. For example, if the message indicates "invalid access", it means that the command is not being used correctly.

What Next

Action based on the message text.

DBR-012

(error) Cannot read design db files. A db file must be a library.

Description

Reading designs in the db format is not supported. Reading of db files is supported for libraries only.

What Next

Do not read files containing designs in db format. Use other supported formats for reading design files.

DBR-013

(error) read_min_max_lib can only merge libraries.

Description

The *read_min_max_lib* can only be used to read and merge two library DBs - one min library, and one max library.

What Next

Check the arguments provided to command read_min_max_lib.

Feedback

DBR-014

(error) multiple libraries in a single DB not supported.

Description

Command read_min_max_lib can only be used on a DB file which contains multiples libraries.

What Next

Check the arguments provided to command read_min_max_lib.

DBR-015

(warning) Ignoring degenerated cell '%s' from library '%s'.

Description

This message warns you that PrimeTime has found a degenerated cell in the library and is ignoring it.

What Next

Verify that this is what you intended.

DBR-016

(error) Cannot find port '%s' for cell '%s' in all libraries.

Description

You receive this message because PrimeTime has found the specified port in either the min or max condition library db file but not the other. The ports of the library cells in the min and max condition libraries must be identical.

What Next

Examine the min and max condition libraries and ensure that they contain the same set of library cells with the same ports.

DBR-017

(error) Cannot find %s '%s' in all libraries.

Feedback

Description

You receive this message because PrimeTime has found the specified cell in either the min or max condition library db file but not the other. The library cells in the min and max condition libraries must be identical.

What Next

Examine the min and max condition libraries and ensure that they contain the same set of library cells.

DBR-018

(error) %s value '%g' of operating condition '%s' is different from the nominal %s value '%g'.

Description

You receive this message if PrimeTime finds the specified operating condition value in either the min or max condition library db file and that value is different from the nominal value.

What Next

Ensure that all operating conditions in the min and max library db files are nominal.

DBR-019

(error) Cannot find operating condition '%s' in library '%s'.

Description

You receive this message because the operating condition you specified cannot be found in the specified library.

What Next

Use the *report_lib* command to list the operating conditions in the specified library. Then re-execute the command, using only the available operating conditions.

DBR-020

(information) Renamed scalar %s '%s' to '%s' in design '%s'.

Feedback

Description

While reading a Verilog file with PrimeTime's native Verilog reader, two net or port names were found to be in conflict, requiring one of the objects to be renamed. This can occur for one of two reasons: an ambiguous bus naming style or escaped names.

Given a bus_naming_style of "%s%d" and the following verilog port declarations:

```
output z1;
output [1:0] z;
```

the bus reference z[1] infers a port named z1. This conflicts with the scalar port z1, declared with the first output statement.

The second case can be shown with the following verilog wire declarations:

```
wire \\z[1];
wire [1:0] z;
```

Assuming the default bus_naming_style of "%s[%d]", the problem here is that bus reference z[1] infers a net named z[1], and so does the scalar declaration.

What Next

No action is required. This is an informational message.

DBR-021

(warning) Library file '%s' is already registered.

Description

You tried to read a library DB file which has already been loaded into memory.

What Next

If the file has changed and you want to reread it, you can remove the library using the *remove_lib* command, then reread the file. However, in the process, if a linked design references this library, that design will need to be unlinked and will need to be completely rebuilt. If you were using *read_min_max_lib*, then using the -force option will do all of this for you.

DBR-022

(error) Template %s is not the same in min and max libraries.

Description

The two libraries given to command read_min_max_lib contain a template of the same name but different content. Two templates must be the same to allow use of the cell

lookup tables from two libraries as one min-max table. This is both an implementation limitation and a feature to improve performance of delay calculation. Two templates are considered same if the variables and indices have same name and same order, same size of the array for each index, and each index value is the same.

What Next

Check the libraries provided to command read_min_max_lib. They should contain same templates. The easiest way to achieve this is to do textual difference on the two .lib files and make sure that the sections describing templates are absolutely the same (excluding blanks and formating). In case when the templates differ you will have to choose one of the sets of templates, put it into the other .lib file, and manually or using a script recalculate all cell delay tables in that library to conform to the new templates. Another way is to set options in the characterization tool that generates .lib files to use a fixed template for both libraries if such option is available.

DBR-023

(error) Duplicate reference port '%s/%s' in module %s ending at line %d in %s

Description

While reading a Verilog file with PrimeTime's native Verilog reader, an instance was found where a scalar port and a bus port in the terminal list are in conflict because of the bus_naming_style. For example:

BOX i0 (.DATA1(a), .D({c ,d}), .\\D[1] (b), .Z(z));

Here, the scalar port D[1] and the bus port D[1] are in conflict if the bus_naming_style is %s[%d]. If the bus_naming_style is %d(%d), there is no conflict. This is an error because renaming reference ports is unpredictable, and therefore, not supported.

What Next

Either change the bus_naming_style or investigate how such a conflict was introduced into your netlist.

DBR-024

(warning) Can't connect pin '%s' to net '%s' in design '%s': already connected to net '%s'

Description

An attempt was made to connect a pin to a net and the pin is already connected to a net. This is typically an error in the netlist, such as a duplicated connection. For example, this

Feedback

message would be generated when reading an EDIF file which has a construct similar to this:

```
(net d
      (joined
       (portRef d)
       (portRef D (instanceRef n1))
       (portRef D (instanceRef n1))
      )
     )
```

What Next

This is a warning indicating that the connection was ignored, so no specific action is necessary.

DBR-026

(error) Unable to create %s '%s' in design '%s'

Description

While reading in a design, an object (such as a port, cell, or net) could not be created. It's likely that the db file has errors, such as multiple nets with the same name on a single design. The object name and design name are given in the message. Such an error will cause the loading of the design to fail, although other designs in the file which do not exhibit problems will be loaded.

What Next

Usually, the application which created the db is the cause.

DBR-030

(error) Invalid global reference '%s' - %s in module ending at line %d in %s

Description

You receive this message if PrimeTime finds an invalid global reference while reading a Verilog file with PrimeTime's native Verilog reader. A global reference is a connection to a wire in another module. PrimeTime's native Verilog reader puts several restrictions on the use of global references. For a reference of the form *module.wire*, all of the following must be true:

- The module must exist in the file being read.
- The module must precede the module that is making the reference.
- The wire must exist in the module.
- The wire must be a logic constant.

Feedback

Any deviation from these rules generates this error message.

What Next

There is no other support for global signals. You must remove them from your netlist.

DBR-031

(error) Attribute '%s' cannot be imported: You defined it as %s; db defines it as '%s'.

Description

You receive this error message because while reading an attribute from db, there was a mismatch between the type (integer, string, etc.) that db defines for the attribute and the type that PrimeTime defines for the attribute. Usually, this is a user-defined attribute, defined with the *-import* option on *define_user_attribute*, and the types do not match.

What Next

Rerun PrimeTime and define the attribute correctly. You might need to use other Synopsys applications to determine the actual type of the attribute.

DBR-032

(information) Ignoring library cell '%s' which does not have any pins defined on it.

Description

This message indicates that while reading the library, PrimeTime detects that the named library cell does not have any pins defined on it. Library cells without pins are ignored and not loaded because they do not have any effect in the timing analysis.

What Next

There is no user actions required unless you think the indicated cell should have pins. If so, you need to go back to the original source of the library in order to fix it.

DBR-033

(warning) Found bad bus definition for '%s' - %s.

Description

This message indicates that while reading the DB file, PrimeTime detected that the named bus definition is wrong or not consistent. PrimeTime may not be able to properly link the design due to this problem.

Feedback

What Next

Normally, this indicates errors in the DB file. Please fix the bus definition in the DB file by going back to the source of the DB file and regenerate it from the tools originally created this DB file.

DBR-040

(error) Design '%s' was not found in '%s'

Description

You receive this message because *swap_cell* loaded the file you specified using the *-file* option, but did not find the specified design in the file. This error could be caused by a misspelling or typo in the design name or filename, or both; or by inadvertently specifying a file that does not contain the intended design.

What Next

Examine the file, verify that the intended design name is contained in the file, and note the spelling of the design name. Then re-execute *swap_cell* using the correct design and file names.

DBR-050

(warning) Number of state table inputs for %s/%s/%s (%d) exceeds %d.

Description

During the reading of a sequential cell from a DB library, an output pin was found with a state table for more than 16 inputs. This message warns you that the presence of this cell with its large state table will degrade read performance, because processing is exponential.

What Next

This is a warning message only. No action is required on your part.

DBR-051

(error) Too many table inputs for %s/%s/%s (%d). State table information ignored in this case.

Feedback

Description

During the reading of a sequential cell from a DB library, an output pin was found with a state table for more than 30 inputs. PrimeTime cannot load state table information for more than 30 inputs, and is ignoring this information.

What Next

Consult the Library Compiler documentation for alternatives to storing state tables.

DBR-060

(error) Can't set min library to %s.

Description

You receive this message if the min library you passed to *set_min_library* is invalid. For example, the min library you specified might have been the same as the max library, or it might have already been used as the max library in a *set_min_library* command. The max and min libraries must be different. The message text will indicate the condition.

What Next

Re-execute *set_min_library* and specify a valid min library.

DBR-061

(information) '%s' already has '%s' as its min library.

Description

The min library you passed to *set_min_library* has already been related to the max library using *set_min_library*.

What Next

If you intended to change the relationship of the max library to a different min library, check the spelling of the min library argument and re-execute the command if necessary.

DBR-062

(error) Cannot create max/min library cell relationship for '%s': %s.

Description

The *set_min_library* command found a library cell in the min library that matches the library cell in the max library. However, some aspect of the two library cells is different. For example, one might have more pins than the other; the pins might be in a different order;

Feedback

or the timing arcs might be different. The text of the message states the most serious difference. To create a max/min library cell relationship, both cells must have the same timing arcs and the same pins, with the same order and direction.

For cells where the max/min relationship fails, as in the current situation, the command uses a minimum condition delay calculation based on the max library. If even one of the library cell pairs matches and compares correctly, the *set_min_library* command continues executing and succeeds.

What Next

Decide if it is acceptable to not use this min library cell for your design. If you want to use this min library cell for your design, ensure it is consistent in the max and min libraries.

DBR-063

(Error) No match for %s/%s in library '%s'.

Description

The *set_min_library* command could not find a library cell in the min library that matches the specified library cell in the max library. Therefore, a max/min library cell relationship cannot be created for that cell.

For cells where the max/min relationship fails, as in the current situation, the command uses a minimum condition delay calculation based on the max library. If even one of the library cell pairs matches and compares correctly, the *set_min_library* command continues executing and succeeds.

What Next

Find out why there is no match for the specified cell. If this is not acceptable, fix and ensure that the max and min libraries are consistent.

DBR-064

(error) min library %s is in link path.

Description

The min library in the *set_min_library* command should not be in the link path; the max library should be in the link path.

What Next

Delete the min library from the link_path, and put the max library into the link_path.

Feedback

DBR-100

(information) Ignoring external links found in design '%s' (file '%s') because dbr_ignore_external_links is set to true.

Description

You receive this message if your design contains external links but the *dbr_ignore_external_links* variable is set to *true*. In this case, the application ignores the external links and instead searches for an object by name only in the libraries in the *link_path*.

External links are created by Design Compiler in certain situations when writing a DB file; for example, when there is a link from a design to a wire load model in a library. The external link records information about the library to which the wire load was linked. Operating conditions can also have external links created for them.

You would set the *dbr_ignore_external_links* variable to *true* if you wanted to use a different library in PrimeTime than was used in Design Compiler.

What Next

If you intended for the external links to be ignored, no action is required on your part. Otherwise, set the *dbr_ignore_external_links* variable to *false* and reexecute the application.

DBR-101

(warning) Pin '%s' is not found on library cell '%s'. Generated clock defined on this pin will not be created.

Description

While reading in a design, a generated clock definition has been found for a library cell, but the source pin of the generated clock does not exist on that library cell. Thus, the generated clock will not be created if this was the only source pin of the generated clock.

What Next

The Synopsys database format (.db) appears to be incorrect. Please recreate the database with the correct source pin name for the generated clock.

DBR-200

(warning) Cannot read DDC attribute %s for design %s.

Feedback

Description

The specified attribute could not be read for the given design. The attribute is ignored.

What Next

Modify the design in the tool that generated the DDC file so that it does not generate this attribute.

DBR-201

(warning) Unknown pin direction in DDC for pin %s

Description

The DDC file has a pin direction that PrimeTime does not recognize. It uses the internal direction for such pins.

What Next

Change the design so that the tool that generates the DDC file does not generate the bad pin direction.

DBR-202

(error) Scenario name %s supplied when no scenarios stored

Description

A *read_ddc* command was issued with a scenario name argument, but there were no scenarios stored in the DDC file.

What Next

Either re-generate the DDC rile with the scenario, re-issue the *read_ddc* command as *-netlist_only* to ignore all constraints, or re-issue the *read_ddc* command without the scenario to pick up the non-scenario constraints.

DBR-203

(error) Scenario name %s did not match an available scenario %s.

Description

A *read_ddc* command was issued with a scenario name that did not match any of the scenarios in the DDC file. A list of available scenarios is listed.

Feedback

What Next

Choose one of the available scenarios and re-issue the *read_ddc* command with the chosen scenario.

DBR-204

(error) File %s is not in DDC format.

Description

The *read_ddc* command was issued for the given file, but the file is not in DDC format.

What Next

Either remove the file from the *read_ddc* command, or generate the file as a DDC file.

DBR-205

(error) File %s has too old a version for PrimeTime to read.

Description

PrimeTime cannot read the given file because the DDC version number is too old.

What Next

Convert the DDC file to a new version. Simply read the file into a tool that can write DDC (such as DC), then write the file out again. The tool will write it out as a new version.

DBR-206

(Warning) The library has non-continuous base curves and can have a negative impact on PrimeTime's performance and memory.

Description

The base-curve ids for the CCS library that is used is not numbered continuously. For eg, the curve_y ids for the base curves in the library are (1, 2, 5, 6, 7 ..) instead of the recommended sequential ordering (1, 2, 3, 4, 5, ...). Such libraries can cause a negative impact on performance and memory of PrimeTime.

What Next

Use the latest version of Library Compiler to get a compatible version of the library.

Feedback

DBR-207

(error) Library %s does not have a complete set of trip-point thresholds.

Description

Delay and slew trip-point thresholds are critical library characterization information needed by delay calculation. One or more of the following trip-point thresholds is missing in this library

input_threshold_pct_rise input_threshold_pct_fall output_threshold_pct_rise output_threshold_pct_fall slew_lower_threshold_pct_rise slew_lower_threshold_pct_fall slew_upper_threshold_pct_rise slew_upper_threshold_pct_fall

What Next

Check with the library characterization team, add the trip-point thresholds in .lib, and recompile .db file.

DBR-209

(information) The *read_ddc* command no longer supports reading constraints.

Description

The *read_ddc* command reads only the netlist.

What Next

No action is required. This is an information.

DCM

DCM-100

(warning) Unable to load DCM library for '%s'. \n Using the default delay model as specified in the .db library.

Description

The program is unable to load the DCM library corresponding to the .db library as specified in the error message. This happens because of one of the following reasons:

```
* One or more of the following shell environment variables
          are not set or are incorrectly set:
                DCMRULEPATH (or CDCRULEPATH)
                DCMRULESPATH (or CDCRULESPATH)
```

```
                DCMTABLEPATH (or CDCTABLEPATH)
        * The DCM library does not exist in the location specified or
          it does not have the proper file permissions.
        * Your installation is not authorized for the
DCM-Delay-Calculation
          feature.
```

When this error is encountered, the program treats the library as a non-DCM library and derives the delay model as though it were a .db library.

What Next

The error messages preceding this one should make the exact cause of the problem clear. Make sure that the aforementioned shell environment variables are set correctly and the DCM library exists as specified with the correct file permissions. Make sure your Synopsys key file includes the DCM-Delay-Calculation license.

DCM-101

(error) Errors found during rule_init() - library '%s' will be unloaded.

Description

The PI function rule_init() of the Delay Calculation System (DCS) standard returned an error code. Typically, the DCS itself issues the diagnostic messages that display before this message. When this message is issued, the program cannot load the remaining DCM subrules and link the EXPOSE and EXTERNAL functions correctly.

What Next

Please contact the library provider or Synopsys if you encounter this message.

DCM-102

(warning) No DCM model for cell '%s' of library '%s'.

Description

This error message is issued when the DCM library returns a nonzero error status

What Next

Check the error messages issued by the DCM prior to this error message and correct any problems. Verify that you have matching versions of the DCM timing and auxilary cell libraries. Contact your library provider for more information.

Feedback

DCM-103

(error) Unable to load DCM EXPOSE function '%s' from the DCM library. This\n \tlibrary cannot be used by this program without the specified EXPOSE function.

Description

This message is issued when the program tries to load the specified DCM EXPOSE function from the specified DCM library and cannot locate a matching function. Because this EXPOSE function is considered critical for the proper calculation of delay values, this library cannot be used by this program for timing calculations.

What Next

Please contact your library provider for more information.

DCM-104

(error) The following feature of the DCL language is not (yet) \n \tsupported by this program: %s.

Description

The current implementation of the program does not fully support the specified feature of the Delay Calculation System (DCS) standard specification. This can result in this particular DCM library being unsuitable for use for delay calculations by this program.

What Next

You cannot use this DCM library for timing calculations until this restriction is removed. Please contact your library provider to see if a version of the library without the specific feature is available.

DCM-105

(error) Error while processing DCL external function '%s' - passed pin '%s' is\n \tnot part of the current timing arc.

Description

The DCL-PI standard defines a number of functions that request the netlist information from the timer application using the pin name rather than the pin pointer. The current implementation of the program supports this feature only as long as the referenced pin name is part of the timing arc currently under consideration. That is, you can substitute the external call with the equivalent byPin() call.

by the equivalent byPin() call.

Feedback

What Next

If you have access to the DCM library source, modify it such that the equivalent byPin() function is used instead of the named external function. Otherwise, please contact your library vendor. equivalent byPin() function is used instead of the named external function. Otherwise, please contact your library vendor.

DCM-106

(warning) The DCL-PI function '%s' returned a nonzero error code %d while\n \tprocessing the timing segment '%s'.

Description

This message appears when the program calls one of the CALCULATION functions as defined in the DCS standard specification and that function returns a bad error code. This typically indicates a problem in the DCM library itself.

What Next

If you have access to the DCL source code of the library, modify please contact your library provider.

DCM-107

(warning) Unsupported test type or edge propagation pair '%s' specified for\n \tthe arc '%s'. This arc will be ignored.

Description

This message is displayed when the program loads the timing arc and detects that test type or the edge propagation characteristics specified for this arc types and edge propagation pairs, please consult your documentation.

What Next

If you have access to the DCL source code of the library, change program. Otherwise, please contact your DCM library provider.

DCM-108

(warning) Internal timing pin '%s' of cell '%s' in library '%s' is\n \tnot defined in the corresponding .db library. Any timing arcs connecting to or from\n \tthis pin will be ignored.

Feedback

Description

This message is displayed when the program loads the timing arcs and detects that the DCM has requested the creation of a new timing point, but no of the library cell's pins, including the internal timing points, must be defined in the technology library .db file before they can be referenced in the DCM.

What Next

If you have access to the source code of the Synopsys technology library (.lib) corresponding with the DCM being loaded, you can add a new internal timing pin for the corresponding cell in the library. Note that current limitations of the Library Compiler product dictate that a "timing()" group must be present for each internal timing pin. However, when using the DCM library, all the each internal timing pin. However, when the DCM library is used, all the timing information comes from the DCM library and any timing data specified in the .db library is ignored.

DCM-109

(warning) %s '%s' is invalid. The valid values are '%s' and '%s'

Description

This message is displayed when an invalid version is set.

What Next

Change the version to one of the valid values and re-run the design.

DCM-110

(warning) DPCM expose dpcmAddWireLoadModel not supported in DPCL library. Therefore DB/custom wireload models are not supported.

Description

This message is displayed when the expose dpcmAddWireloadModel is not supported in the DPCM Procedural Interface.

What Next

Use DPCM wireloads. If db wireload has to be used support the expose in DPCM.

DCM-111

(warning) The design %s read in has wireload %s, which is not present in the current DPCM. Changing to default DPCM wireload %s.

Feedback

Description

You receive this warning message when the current wireload attached to the design is not present in one of the DPCM libraries.

What Next

Use a wireload that is in one of the DPCM libraries. To see a list of wireloads in the DPCM libraries, use the *report_lib* command.

DCM-112

(warning) The design %s read in has a DCPM wireload %s. Deleting the dpcm wireload.

Description

This message is displayed when the current wireload attached to the design is from a DPCM library and not db.

What Next

Use DB wireloads. List DB wireloads by doing report lib.

DCM-113

(information) Propagating clocks through cell '%s' instantiated from design '%s'.

Description

Generate ouput clocks for special cells such as DLL/DCM.

DCM-114

(information) The clock '%s' with period '%s' generated on pin '%s'.

Description

Generate a clock for ouptut pin of special cells such as DLL/DCM.

DCM-115

(information) Please check CLKFX_DIVIDE value: '%s'.

Description

CLKFX_DIVIDE value is not valid.

Feedback

DCM-116

(information) Please check CLKFX_MULTIPLY value: '%s'.

Description

CLKFX_MULTIPLY value is not valid.

DCM-117

(information) Please check CLKDV_DIVIDE value: '%s'.

Description

CLKDV_DIVIDE value is not valid.

DCM-118

(warning) During the polynomial reduction procedure, the '%s' variable is saturated from %f to %f.

Description

This warning message occurs when a boundary value instead of the original variable value is used for polynomial reduction.

What Next

A polynomial is reduced before final calculation if its parameters contain one of the following variables defined in the operating conditions: *temperature*, *parameter1*, *parameter2*, *parameter3*, *parameter4*, *parameter5*, *voltage*, *voltage1*, ..., *voltage99*.

If the variable value defined in the operating conditions is out of the boundary defined in the polynomial, then the closest boundary value for the variable will be used for polynomial reduction.

For example, if the *temperature* variable defined in the current operating condition is 20, while the range of the *temperature* in the polynomial is [25, 40], then 25 instead of 20 is used to reduce this polynomial.

DDB

DDB-1

(warning) Cell %s not added to design %s because a cell with that name already exists.

Feedback

DDB-2

(warning) Net %s not added to design %s because a net with that name already exists.

Description

A net with the specified name already exists.

What Next

Reissue the command with a new net name. Use the *report_net* command to find a list of all the nets currently present in the design.

DDB-3

(warning) Consistency problem: port %s is not owned by any design or reference.

Description

The specified port is not owned by any design.

What Next

Check the consistency of your design database.

DDB-4

(warning) Consistency problem: a pin is not owned by any cell.

Description

The specified pin is not owned by any design.

What Next

Check the consistency of your design database.

DDB-5

(warning) Consistency problem: cell %s is not owned by any design.

DDB-7

(warning) Consistency problem: net %s is not owned by any design.

Feedback

DDB-8

(warning) Consistency problem: a pin was found without a corresponding port.

DDB-9

(warning) Consistency problem: cell %s was found without a corresponding reference.

DDB-10

(warning) Consistency problem detected in design %s\n%s

DDB-11

(warning) Internal error\n%s

DDB-12

(warning) Removed duplicate cell '%s'.

DDB-13

(warning) The name of net '%s' in design '%s' can't be changed \n\ \tto the name of both ports '%s' and '%s' to which it's connected.

DDB-14

(warning) The net '%s' in design '%s' is connected to both \n \tports '%s' and '%s'.

Description

Two ports can only be connected to a net if they are inout ports or if they drive wired logic. Connecting two input ports to a net can limit the optimization that can be performed by Design Compiler on the net.

What Next

Disconnect one of the ports from the net using the *disconnect_net* command.

DDB-21

(error) Conflict between logic 0 and 1. Can't %s.

Feedback

Description

The two specified ports were set previously as logic 0 and 1. They might not have been directly set, but could have been implicitly set by a sequence of *set_equal* and *set_opposite* commands.

What Next

If the ports were directly set as logic 0 and 1, the next steps are as follows:

```
Use report_attributes commands on the two ports. They will have the
driven_by_logic_zero and driven_by_logic_one attributes set.

Remove one of these two attributes, one of which is incorrect,
using the remove_attribute command

Reissue the original command.
```

If the ports were implicitly set as logic 0 and 1 through a sequesce of *set_equal* and *set_opposite* commands, the next step is as follows:

```
Use the reset_design command to remove the setting of 0 and 1 on the
ports. this command removes all other constraints on the design and
 should
be used with caution.
```

DDB-22

(error) Can't set equal ports opposite in design '%s': '%s' '%s'.

Description

The two ports were set as equal ports previously. They might not have been directly set, but could have been implicitly set by a sequence of *set_equal* and *set_opposite* commands.

What Next

The two specified ports were set previously as equal ports. The only way to revert back this setting is to reset the design using the *reset_design* command. This command removes all other constraints on the design and should be used with caution.

DDB-23

(error) Can't set opposite ports equal in design '%s': '%s' '%s'.

Feedback

Description

The two ports were set as opposite ports previously. They might not have been directly set, but could have been implicitly set by a sequence of *set_equal* and *set_opposite* commands.

What Next

The two specified ports were previously set as opposite ports. The only way to revert back this setting is to reset the design using the *reset_design* command. This command removes all other constraints on the design and should be used with caution.

DDB-24

(warning) Overwriting design file '%s/%s'.

Description

Overwriting the specified version of the design with more recent version.

What Next

Warning only. No action is required.

DDB-27

(error) '%s' value must be positive.

Description

A negative value was entered. Constraint values must be positive (or 0).

What Next

Please enter a non-negative value.

DDB-28

(error) '%s' cannot be set on %s pin '%s'.

Description

The specified constraint cannot be set on a pin of the specified direction. The constraint command will be ignored.

What Next

Please enter a correct constraint command.

Feedback

DDB-29

(error) '%s' cannot be set on %s port '%s'.

Description

The specified constraint cannot be set on a port of the specified direction. The constraint command will be ignored.

What Next

Please enter a correct constraint command.

DDB-30

(error) Can't specify output port '%s' as a path startpoint.

Description

Output ports are not valid as path startpoints. There are no timing paths from such ports.

What Next

Examine the design to determine the correct startpoint for the path.

DDB-31

(error) Can't specify input port '%s' as a path endpoint.

Description

Input ports are not valid as path endpoints. There are no timing paths to such ports.

What Next

Examine the design to determine the correct endpoint for the path.

DDB-32

(error) Can't specify hierarchical cell '%s' as a path '%s'.

Description

Hierarchical cell names are not valid as path startpoints or endpoints.

What Next

Use a clock, port, pin (leaf or hierarchical), or cell (leaf only) as the path startpoint or endpoint.

Feedback

DDB-33

(error) Pin '%s' does not have a library hold time.

Description

None.

What Next

Check the target library.

DDB-34

(error) %s '%s' is in design '%s', but %s '%s' is in design '%s'.

Description

None.

What Next

None.

DDB-35

(error) '%s' does not exist in library '%s'.

Description

The listed key in the error message does not exist in the library.

What Next

Check the key file.

DDB-38

(error) Can't open security file '%s' for protected library '%s'.

Description

Cannot open security file.

What Next

Check the security file.

Feedback

DDB-39

(error) Bad security key in file '%s' for library '%s'.

Description

You are trying to invoked *read_lib* on a protected library.

What Next

If a nodelocked library, check and correct these attributes: key_file, key_seed, and key_bit. If a network licensing library, check and correct these attributes: key_feature, key_version, and key_seed. Then reinvode the *read_lib* command.

DDB-40

(error) Can't read protected library '%s'.

Description

You are trying to invoked *read_lib* on a protected library.

What Next

If a nodelocked library, check and correct these attributes: key_file, key_seed, and key_bit. If a network licensing library, check and correct these attributes: key_feature, key_version, and key_seed.

DDB-41

(error) Incomplete library protection attributes.

DDB-43

(warning) Could not create attribute '%s' for %s objects.

DDB-44

(error) Can't read unprotected library '%s'.

DDB-45

(error) A design with name '%s' already exists in the same\n \tdesign file as design '%s'.

Feedback

DDB-46

(error) A reference with name '%s' already exists in design '%s'.

DDB-47

(error) A cell with name '%s' already exists in design '%s'.

DDB-48

(warning) Creating port '%s' on design '%s' with direction unknown.

DDB-51

(warning) In the value of %s, \n \tthe characters separating the \tthose separating each

DDB-52

(error) The value of %s \n \tmust include one

DDB-53

(error) The value of %s \n \tmust include one

Description

The message is printed out when the current command found invalid value in the indicated variable.

What Next

Check the value of the given variable and provide the valid value.

DDB-54

(error) The value of %s \n \tmust include only one

Description

The error message is printed out when the current command found invalid value in the indicated variable.

What Next

Provide the valid value for this variable.

Feedback

DDB-55

(error) The value of %s \n \tmust include only one

Description

The error message is printed out when the current command found invalid value for the indicated variable name included in the message.

What Next

Provide the valid value for this variable.

DDB-56

(error) In the value of %s, \n \tthere are no characters separating %s.

Description

This error message is printed out when the current command found that there are no character separators.

What Next

Provide the valid value for the command.

DDB-57

(error) In the value of %s, \n \tthe %s of the characters separating \n \t%s must not be%s a digit.

Description

This error message is printed out when the current command found digit in the character separators.

What Next

Provide the valid value for the command.

DDB-58

(warning) In the value of %s, \n \tthere are no characters separating the \tbe ambiguous).

Description

If no characters separate the array name from the member number, the bus names will be ambiguous for arrays whose names end in a digit. For example, with *bus_naming_style*

set to "%s%d", the name of the third member of array "A1" and the thirteenth element of array "A" would both have the name "A13".

What Next

Most likely you should change the value of the bus naming style to contain some characters between the "%s" and "%d". See the help page for *bus_naming_style* for details.

DDB-60

(error) Could not find library pin for pin '%s'.

Description

The back-annotation failed because the pin does not have a corresponding pin in the link library.

What Next

Verify that the design is fully linked with the 'link' command. Verify that all link and target library search paths are valid.

DDB-66

(warning) Removing group '%s'.

Description

The path group is being removed because the operation being performed has removed the last path from the group.

What Next

Be aware that any subsequent attempts to use this path group will fail because the group has been deleted. If you think the group should not have been deleted, identify at least one path you think should still be in the group and trace back to find which action deleted that path.

DDB-67

(warning) Removing %s from group '%s'.

DDB-68

(warning) Removing external delay related to clock %s.

Feedback

Description

When a clock source is deleted from the design using the 'remove_clock' command, all input and output delay values that were specified relative to that clock are also deleted from the design. For example, consider the following script:

create_clock -name CLK -period 10 set_input_delay 2 -clock CLK all_inputs()
set_output_delay 2 -clock CLK all_outputs()

remove_clock CLK

The 'remove_clock' command will also have the effect of removing the input and output delay values that were specified relative to CLK.

What Next

No action is required, this is merely an informational warning.

DDB-70

(error) None of the selected cells were grouped.

Description

When using the 'group' command on an hdl design that has not been compiled yet, it is possible that the cells you specified to be grouped cannot be grouped because they need to stay with thier neighboors until the design has gone through resource sharing in compile.

What Next

Use the 'group' command after the design has been compiled.

DDB-71

(error) Design '%s' requires one of the following licenses: '%s'.

Description

The specified design is licensed and requires one of the listed licenses to be available. An error has occurred because none of the licenses could be obtained.

What Next

Verify that your site has at least one of the specified licenses. If it does not, then one must be purchased. If your site does have one of the licenses, try again when the license is available.

Feedback

DDB-72

(information) Added key list '%s' to design '%s'.

Description

Indicates that the listed set of licenses have been associated with the specified design. Accessing the design will require that one of the listed licenses can be successfully checked out.

What Next

No action is required since this is just an information message.

DDB-73

(warning) License '%s' contains the illegal character '%c'.\n\tIt was ignored.

Description

One of the licenses associated with a design contains an invalid character. That license will be dropped from the list of licenses which can be used to access the design.

What Next

If a design is associated with multiple licenses, it may be possible to access the design via a different, valid license. In any case the license name should be updated so that it does not contain any invalid characters. Invalid characters include: ',', '}', '{', '*', '\'.

DDB-74

(warning) Design '%s' inherited license information from design '%s'.

Description

All of the licenses associated with one design have now been associated with another design. This typically happens when a design is ungrouped. In that situation, the parent design will inherit all licensing information from the ungrouped design.

What Next

Although this is classified as a warning, it is essentially just an information message. No action is required.

DDB-75

(warning) Design '%s' is being converted to a limited design.

Feedback

Description

This message indicates that the indicated design has been converted into a limited design. A limited design is a design which can be compiled and analyzed, but whose contents may not be examined or written out.

A design gets converted into a limited design in two situations. In the first case you have only an evaluation license for the design (obtained by manually setting synlib_disable_limited_licenses = "FALSE"), and the design will remain limited because the intent of an evaluation license is for the design data to be restricted. In the second case the design was derived from a DesignWare part and has not yet been run through the *compile* command. In this latter case the design remains limited only until after it has been compiled, at which point the limitation is removed. The intent of this latter limitation is to protect the technology- independent structure of the design.

What Next

If you have only an evaluation license for the limited design, then the only way to gain access to the internals of that design is through the use of a full license for that part; if a full license is subsequently obtained then the first *compile* command will remove the 'limited design' restrictions. If the design has already been compiled, it is sufficient to run the *get_license* command to convert the limited design back to a regular, unrestricted format.

If you already have a full license for the limited design, then after the first *compile* command you can expect the design to be converted back to a regular, unrestricted format.

DDB-76

(error) Cannot load design '%s'.

Description

The named design cannot be loaded into Design Compiler's internal data structures. This can happen if certain synthetic parts cannot be found.

What Next

Attempt to link the design with the command *link -all*. If this fails, check that the software is correctly installed.

DDB-77

(error) License '%s' is a Synopsys internal key and should\n \tnot have a seed associated with it.

Feedback

Description

When license names are set on a design, third party keys must have a seed associated with them. It is an error, however, for Synopsys internal keys to have seeds.

What Next

When creating your own license names, make sure that they do not clash with the Synopsys internal license names.

DDB-78

(error) No seed provided for the third-party license '%s'.

Description

When adding a third-party license, you must specify both a license name and a non-zero seed. This prevents third party vendors from creating keys for each other's licenses.

What Next

Specify the license name as *name/seed*. For example: "MY_LIC/1234"

DDB-79

(error) The license '%s' has an invalid seed associated with it.

Description

This error occurs when the *set_design_license command* is used to store a third party license and a seed, and the seed that is specified is not consistent with the seed that was used to create the key.

What Next

Either generate a new key with the correct seed, or change the *set_design_license* command line so that the seeds are consistent.

DDB-80

(error) The seed '%s' specified for license '%s' is\n\tnot a valid 32-bit integer.

Description

Licenses can be specified in the from '<license>/<seed>' where <seed> is supposed to be a valid integer which can be represented in 32 bits. In this case the <seed> specified was either not an integer, or was too large to be represented in 32 bits.

Feedback

What Next

The <seed> associated with the license needs to be corrected such that it is a valid integer which can be stored in at most 32 bits.

DDB-81

(warning) Unable to find specified driving_cell for port '%s'.

Description

The driving_cell attributes indicate that a port should inherit its drive capability from a certain library cell. This error means that the tool was unable to locate a matching library cell or pin on that library cell. This may happen if the link_library does not contain the library for that cell, or if the cell name or pin name was incorrect. The driving cell information can be seen using *report_port -drive*. It may have been set by either *set_driving_cell* or *characterize*.

What Next

If the driving cell requires a library that has not been identified in the *link_library*, the *link_library* should be changed to include that library. Otherwise, check the information for errors in cell_name, library name, or pin names using *report_port -drive -only port_name.*

DDB-84

(error) Only ports of the same direction can be grouped.

DDB-85

(error) Objects must be either all ports or all nets.

Description

This error message is issued if a mixture of objects of different types is given as input to a command that requires a homogenous set of ports or nets as input.

What Next

Re-issue the command specifying only ports or only nets as input.

DDB-86

(error) Bus name '%s' conflicts with existing names.

Feedback

Description

This error message is issued when an attempt is made to create a bus with a name that conflicts with the name of an existing bus.

What Next

Re-issue the command with a non-conflicting name for the bus.

DDB-87

(error) All objects must be from the same design.

Description

This error message is issued if a command that requires a set of objects belonging to the same design is invoked with objects that belong to different designs.

What Next

Re-issue the command with a set of objects that belong to the same design.

DDB-88

(error) At least one of the port objects specified is already a member of a bus.

Description

This error message is displayed if an attempt is made to insert a port that belongs to a bus into a new bus.

What Next

Re-issue the command with ports that do not belong to an existing bus.

DDB-89

(error) Type name '%s' conflicts with existing type.

Description

This error message is issued if an attempt to create a type for a new bus object is made with a type name that is already used for another bus object with a different width.

What Next

Change the name of the new bus type.

Feedback

DDB-90

(error) specified range is different from number of objects to be bussed.

DDB-91

(error) only designs or references can have busses created in them.

DDB-92

(error) Cannot load design '%s' for an HDL embedded command.

Description

The named design cannot be loaded for the current command embedded in an HDL file. The current embedded command is not legal within an embedded script. See the HDL Compiler Manual for details.

What Next

Change the embedded script so that it does not use the offending command.

DDB-95

(warning) Unable to find net instance '%s' in design '%s'.

Description

Back-annotation, such as a set_load or set_resistance value, was stored on a net instance within the design, but that instance can no longer be found. This can occur if a lower-level design containing the net instance was modified but the top-level design was unaware of this change. Commands which could modify lower level designs include *ungroup*, *change_names*, and *compile*.

What Next

Perform *ungroup* and *change_names* at the top level so that the top level design will have a chance to update its back-annotation records. Use *characterize* to move annotation to a subdesign before running *compile* or *reoptimize_design* on that subdesign.

DDB-100

(warning) Unable to find minimum version of library cell '%s/%s' in library '%s'.

Feedback

Description

The *set_min_library* command has been used to indicate that timing data for minimum analysis must use a particular library, but this library cell cannot be found in that minimum library. Design Compiler will use the maximum version of the cell for both maximum and minimum analysis in this case.

What Next

Check that the *set_min_library* command specified the correct library for minimum analysis. See if the indicated library cell was accidentally left out of the minimum analysis library.

DDB-101

(warning) Unable to find minimum version of library pin '%s/%s' in library '%s'.

Description

The *set_min_library* command has been used to indicate that timing data for minimum analysis must use a particular library, but the indicated library cell has conflicting pin descriptions between the maximum and minimum libraries. In this case, a pin exists on the library cell in the maximum library, but that pin does not exist in the minimum library. Design Compiler will use the maximum version of the library pin for both maximum and minimum analysis in this case.

What Next

Check that the *set_min_library* command specified the correct library for minimum analysis. See if the indicated library pin was accidentally left out of the minimum analysis library.

DDB-102

(warning) Conflicting timing arc descriptions between maximum library '%s' and minimum library '%s' to pin '%s/%s'.

Description

The *set_min_library* command has been used to indicate that timing data for minimum analysis must use a particular library, but the indicated library cell has conflicting timing arc descriptions between the maximum and minimum libraries. In this case, a timing arc exists on the library cell in the maximum library, but a corresponding timing arc does not exist in the minimum library. Design Compiler will use the maximum version of the timing arc for both maximum and minimum analysis in this case.

In order to consider timing arcs as compatible between minimum and maximum libraries, they must have the same sense (for example, positive unate, or clear), they must have the same SDF condition, and there must be the same number of arcs of each type between a pair of pins.

What Next

Check that the *set_min_library* command specified the correct library for minimum analysis. See if timing arcs to the indicated library pin were accidentally left out of the minimum analysis library.

DDB-103

(warning) Pin %s of lib cell %s exists in maximum library %s but not in minimum library %s. Assuming min delay for pin to be same as max delay.

Description

The *set_min_library* command has been used to indicate that timing data for minimum analysis must use a particular library, but the indicated library cell has some pins in the max library which don't exist in the minimum libraries. Design Compiler will use the maximum version of the timing arc for both maximum and minimum analysis in this case.

In order to be compatible between minimum and maximum libraries, the library cells must have the same pins and same timing arcs (same sense (for example, positive unate, or clear), they must have the same SDF condition), and there must be the same number of arcs of each type between a pair of pins.

What Next

Check that the *set_min_library* command specified the correct library for minimum analysis. See if the specified pins of the specified library cell were accidentally left out of the minimum analysis library.

DDB-105

(warning) Design '%s' requires one of the following licenses: '%s'. \n\tWaiting for license to become available, press <ctrl>-C to terminate.

Description

The specified design is licensed and requires one of the listed licenses to be available. None of the licenses could be obtained. Design Compiler will wait for one of the licenses to become available and then continue.

Feedback

What Next

Verify that your site has at least one of the specified licenses. If it does not, then one must be purchased. If you wish to terminate the command instead of waiting for the license to become available, set synlib_wait_for_design_license = {}

DDB-107

(warning) Deleted or recreated %d internal pin(s) on cell '%s'. All attributes and attaches on it(them) are lost.

Description

The *access_internal_pins* variable controls creation and deletion of internal pins and user access to them. Because of the source of internal pins, they are created or deleted during link time, depending on the setting of this variable. You can use the *find* and *get_pins* commands to show internal pins, if such pins exist. Certain timing commands can also set constraints on internal pins.

What Next

If this is what you intended to do, no action is necessary.

See Also

- find
- get_pins
- link

DDC

DDC-1

(error) Unable to open DDC file '%s' for writing.

Description

dc_shell encountered an I/O error when it attempted to open the specified DDC file for writing.

What Next

Check that the file name is correct, that the directory exists and is writable, and that the filesystem is not full. If the target file already exists it must be writable in order for dc_shell to overwrite it.

Feedback

DDC-2

(error) Unable to open file '%s' for reading.

Description

The tool encountered an error when it attempted to open the specified DDC file for reading.

What Next

Check that the path to the file is correct and that the file is readable by the current user. Also verify that the file was written in DDC format.

DDC-3

(error) DDC internal write error in design '%s'.

Description

dc_shell encountered an internal error while attempting to write the specified design. No DDC file was produced.

What Next

Please contact the Synopsys Support Center for assistance.

DDC-4

(error) DDC internal read error in file '%s'.

Description

dc_shell encountered an internal error while attempting to read the specified file. No designs were read.

What Next

Please contact the Synopsys Support Center for assistance.

DDC-5

(error) Design data is corrupt in DDC file.

Description

The file being read has been modified or corrupted since it was originally written by *dc_shell*.

Feedback

What Next

The DDC file must be re-created from the original design source. Note that DDC files cannot be edited by the user.

DDC-6

(error) DDC file version is not compatible. The DDC file was written with\n dc_shell version %s dated %s.

Description

The file being read was written with an incompatible version of of the .ddc format that cannot be read with this release of the tool. The .ddc format is updated from time to time to support new features or functionality, and sometimes the new format cannot be read with older tool versions.

What Next

Use the current version of the tool to read the .ddc file.

DDC-7

(error) File is not in DDC format.

Description

dc_shell has determined that the file being read is not a DDC format file.

What Next

Verify that the correct format option has been provided to the read_file command, and that the file path is correct.

DDC-8

(error) Attempt to write duplicate design name '%s' to DDC file.

Description

dc_shell detected an attempt to write multiple designs with the same name to a DDC file, which is not allowed by the DDC format.

What Next

Check the list of designs provided to the write command. It is possible, although unusual, for duplicate design names to have been read from different files, such as multiple .db

files. If the duplicate design names must be preserved, they must be written to separate DDC files.

DDC-9

(warning) The DDC format cannot be used to store physical data. Any physical\n information that is present will not be written to the DDC file.

Description

You receive this warning message when you write out a DDC file that contains physical data. The DDC file format is not capable of representing physical data. Only the logical representation will be written to the DDC file.

What Next

It is considered best practice to use the Milkyway storage format for designs that contain physical information. You can use the *write_milkyway* command to write the design to a Milkyway database.

DDC-10

(error) Scenario '%s' does not exist.

Description

The specified scenario, which was provided with the -scenarios option to the *write* command, does not exist.

What Next

Check that the scenario name is correct, and that any scenarios which are to be written to the DDC file have been created.

See Also

- create_scenario

DDC-11

(error) DDC file contains packed command syntax that cannot be processed by\n this version of dc_shell. Please use a current version of dc_shell\n to read this file.

Feedback

Description

The current DDC file contains embedded commands (constraints) which were written by a newer version of *dc_shell* and utilize a syntax which cannot be parsed by the current executable.

What Next

Use the same (or newer) version of *dc_shell* to read the file as was used to write it.

See Also

- read_file

DDC-12

(warning) DDC file was written with a newer version of dc_shell.\n Some embedded commands may be ignored.

Description

You are trying to read a DDC file which was written by a newer version of *dc_shell*, and the DDC file contains some packed commands (constraints) which are not recognized by the older version of *dc_shell*. Normally this would result in a DDC-6 error; however, if the variable ddc_allow_unknown_packed_commands is set to "true" then *dc_shell* will attempt to read the file, but any unrecognized packed commands will be ignored. (A DDC-13 warning message will be printed when each such command is first encountered.)

What Next

To avoid losing potentially important information, always read the DDC file with the same (or newer) version of *dc_shell* as was used to write it.

See Also

- DDC-13
- read_file

DDC-13

(warning) Ignoring unknown packed command #%d: %s

Description

dc_shell attempted to unpack an embedded command which it does not recognize. This can happen when a DDC (or Milkyway) file which was written with a newer version of *dc_shell* is read with an older version of the product, while the variable

Feedback

ddc_allow_unknown_packed_commands is set to "true". The unrecognized command is simply discarded.

What Next

To avoid losing potentially important information, always read the DDC file with the same (or newer) version of *dc_shell* as was used to write it.

DDC-14

(information) This file contains data for the following %d scenarios:\n %s

Description

The DDC or Milkyway reader prints this message if the file being read contains any scenario-specific constraint data. The message will report the name of each scenario for which the file contains data. If the scenario was inactive when the file was written, an asterisk (*) appears after the scenario name.

What Next

This is an informational message. No action is required.

See Also

- read_file
- read_milkyway
- create_scenario
- current_scenario

DDC-15

(warning) Ignoring %s attribute %s on %s object(s):\n Attribute type conflicts with existing attributes.

Description

An attribute contained in the DDC file conflicts in type with with an attribute that is already registered with the tool. The conflicting attribute is ignored by the DDC reader.

An attribute saved in a DDC file must have the same type as an existing attribute of the same name on the same netlist object class (e.g., string attribute on design objects).

This message is most likely seen when reading in DDC files written by the X-2005.09 release or earlier. Attribute conflicts from more-recent files are silently discarded.

Feedback

What Next

This message could appear if there happens to be a user-defined attribute that has the same name (but different type) as a built-in attribute that was added in a later version of the tool. It is good practice to use a prefix for user-defined attributes, such as your company's name, that is unlikely to be used by Synopsys in the future.

See Also

- report_attribute

DDC-16

(error) ddc file contains no scenario-specific data. Cannot specify\n -scenarios option for this file.

Description

The *-scenarios* option to the *read_file* command can only be used to read files that contain scenario-specific constraint data.

What Next

See *read_file*(2) for more information on controlling which scenarios' constraints are read from the ddc file.

See Also

- read_file
- read_ddc

DDC-17

(error) ddc file contains no data for any of the requested scenarios

Description

The specified ddc file does not contain any constraint data for any of the scenarios specified to the *-scenarios* option to the *read_file* command.

What Next

Check the list of scenario names supplied to the *read_file -scenarios* option. See *read_file*(2) for more information on controlling which scenarios' constraints are read from the ddc file.

Feedback

See Also

- read_file
- read_ddc

DDC-18

(error) DDC file contains no data for any of the requested active scenarios

Description

The specified ddc file does not contain any constraint data for any of the scenarios specified to the *-active_scenarios* option to the *read_file* command.

What Next

Check the list of scenario names supplied to the *read_file -active_scenarios* option. See *read_file*(2) for more information on controlling which scenarios' constraints are read from the ddc file.

See Also

- read_file
- read_ddc

DDC-19

(warning) ddc file contains no data for the following requested scenarios:\n %s

Description

The specified ddc file does not contain any constraint data for one or more of the scenarios specified to the *-scenarios* option to the *read_file* command. The file will be read and the list of scenarios to be read in will be restricted according to the remaining scenarios specified to the *-scenarios* option.

What Next

Check the list of scenario names supplied to the *read_file -scenarios* option. See *read_file*(2) for more information on controlling which scenarios' constraints are read from the ddc file.

See Also

- read_file
- read_ddc

Feedback

DDC-20

(warning) This .ddc file contains special features and may only be read by\n\t tools that support the required features.

Description

This warning message occurs when you write a .ddc file that is "feature locked." It is a reminder that the tool that is writing the file has flagged the file as requiring specific features in order for it to be read, and the file might not be readable by other tools or by the same tool if the required features have not been enabled.

What Next

This is only a warning message. No action is required.

See Also

- DDC-21

DDC-21

(error) The feature used to generate this .ddc file is not supported by\n\t this tool or is not enabled in the current session.

Description

This error message occurs when you attempt to read a .ddc file that was "feature locked" by the tool that wrote it. The current session does not have, or has not enabled the specific features required to read the file. This usually happens when *dc_shell* writes the file when it is in a special mode and the resulting files cannot be read by all tools that consume the .ddc format.

What Next

Review any other messages that were printed to understand which tool and features are required to read the file.

See Also

- read_ddc
- read_file
- DDC-20

Feedback

DDC-22

(error) Cannot read design '%s' as a block abstraction because the file does not contain block abstraction information.

Description

This error occurs when the *set_top_implementation_options* command has been run to specify that the design be read as a block abstraction, but no block abstraction information was saved in the .ddc file.

What Next

Make sure you run the *create_block_abstraction* command immediately before writing the .ddc file. Also, verify that the correct design name is specified by the *set_top_implementation_options* command.

See Also

- read_ddc
- read_file

DDC-23

(error) Cannot read design '%s' as a block abstraction because the specified interface features are not present in the file.

Description

This error occurs when the *set_top_implementation_options -load_logic compact_interface* command is used to specify that the named design be read as a block abstraction with a compact_interface, but the block abstraction has been generated with an older version of the tool that does not support the annotation of compact_interface logic.

What Next

Regenerate the block abstraction with the latest version of the tool in order to obtain support for compact_interface markings. Alternatively, the block abstraction can be loaded as a block abstraction with a full_interface.

See Also

- read_ddc
- read_file

Feedback

DDC-24

(error) Output file %s is the source file for the block abstraction.

Description

This error occurs when the specified output file is the source .ddc file for the block abstraction that is being written out. Design Compiler does not allow you to overwrite the original .ddc file because each design's core (non-interface) logic is retrieved from that file and merged with the block abstraction's interface logic in order to write out the complete netlist for the design.

What Next

Specify an output file that is not the source of any block abstractions that are currently in memory.

DDC-25

(error) Block abstraction source file %s appears to have been modified since the design was read.

Description

This error occurs when the design that is being written out is a block abstraction and the .ddc file that it was originally read from has since been modified. The .ddc files containing block abstractions must not be modified until after their blocks have been written back out because the core (non-interface) logic is retrieved from the original files.

What Next

Do not modify the source files for block abstractions if the designs are still being used.

DDC-26

(error) Cannot open block abstraction source file %s.

Description

This error occurs when the design that is being written out is a block abstraction and the .ddc file that it was originally read from cannot be opened. The file might have been deleted or renamed, or there might be a permissions problem. The .ddc files containing block abstractions must remain available until their blocks have been written back out because the core (non-interface) logic is retrieved from the original files.

Feedback

What Next

Make sure the original .ddc files remain available as long as the block abstractions are being used.

DDC-27

(information) Reading %s block abstraction for design '%s' and its hierarchy.

Description

This message occurs when the specified design hierarchy is being loaded as a block abstraction. Only the specified type of interface logic (full or compact interface) is being loaded, not the entire design netlist. This behavior is controlled by the *set_top_implementation_options* command.

What Next

This is an informational message. No action is required.

DDC-28

(error) Block abstraction interface logic has been modified in an unsupported manner. Cannot write .ddc file.

Description

This message occurs when the interface logic of a block abstraction has been modified in a way that the *write_file* command does not expect. This prevents the merging of the interface logic in memory with the core logic from the original .ddc file. This could be caused by manual modifications you have made to the netlist.

What Next

Do not make manual modifications to block abstractions. Any such changes should be made prior to running the *create_block_abstraction* command.

DDC-29

(error) You must specify the output file name when writing a block abstraction.

Description

This message occurs if you are writing a block abstraction to a .ddc file and you have not specified the *-output* option with the *write_file* command. In this case, "block abstraction" refers to either the full design that has been processed by the

create_block_abstraction command or the block abstraction (interface logic only) as specified by the *set_top_implementation_options* command.

Specifying the *-output* option causes Design Compiler to write all designs to a single file, which is required for block abstraction hierarchies.

What Next

Specify an output file when writing block abstractions to .ddc files.

DDC-30

(warning) Forcing the -hierarchy option because a block abstraction is being written.

Description

This message occurs if you are writing a block abstraction to a .ddc file and you have not specified the *-hierarchy* option with the *write_file* command. In this case, "block abstraction" refers to either the full design that has been processed by the *create_block_abstraction* command or the block abstraction (interface logic only) as specified by the *set_top_implementation_options* command.

Design Compiler requires that block abstractions be written hierarchically, starting from the top design of the block abstraction. Therefore, the *-hierarchy* option is inferred if it has not been explicitly specified.

What Next

Specify the *-hierarchy* option when writing block abstractions to .ddc files.

DDC-31

(error) You must specify only the top design of the block abstraction hierarchy.

Description

This message occurs if you are writing a block abstraction to a .ddc file and you have specified more than one design name with the *write_file* command or the specified design is not the top design of the block abstraction hierarchy. In this case, "block abstraction" refers to either the full design that has been processed by the *create_block_abstraction* command or the block abstraction (interface logic only) as specified by the *set_top_implementation_options* command.

A block abstraction's entire hierarchy must be written to a single .ddc file. The only design name that can be specified with the *write_file* command is the top design of the block abstraction. However, the design name can be omitted if that design is the current design. The *-hierarchy* and *-output* options are mandatory when writing block abstractions.

Feedback

What Next

Specify only the top design of the block abstraction when writing .ddc files.

DDC-32

(information) Merging block abstraction with non-interface netlist data from %s.

Description

This message occurs when writing out a design that was loaded as a block abstraction as specified by the *set_top_implementation_options* command. Since the block abstraction's interface logic might have been modified after it was loaded into memory, the interface logic in memory is merged with the core (non-interface) logic from the original .ddc file, and a new .ddc file is written out.

What Next

This is an informational message. No action is required.

DDC-33

(information) Block abstraction information will not be preserved. If this\n information is required, you must run the create_block_abstraction\n command prior to writing the design.

Description

This message occurs when you read a .ddc file that contains block abstraction information that was created by the *create_block_abstraction* command. If the *set_top_implementation_options* command was not used to tell Design Compiler to read the file as a block abstraction (to read the interface logic only), then the design is read in its entirety. This message is a reminder that the block abstraction information is not automatically preserved if the design is written to a new .ddc file. If you want to preserve the block abstraction's information in a new file, you must run the *create_block_abstraction command immediately before writing it out.*

What Next

This is an informational message. No action is required.

DDC-34

(error) Cannot write IC Compiler block abstraction %s in ddc format.

Feedback

Description

This message occurs when you attempt to write a block abstraction that was created by IC Compiler to a .ddc file. Only block abstractions created by Design Compiler can be written in the ddc format.

DDC-35

(error) Reading of ILM designs is no longer supported. Cannot read %s.

Description

This message occurs when you try to read ILM designs in ddc format. ILM designs are no longer supported for use in Design Compiler.

What Next

Migrate to the use of block abstractions instead of ILMs for loading the blocks at the top level.

DEFR

DEFR-001

(error) Cannot find def file %s.

Description

The def file specified to the set_eco_options command cannot be read.

What Next

Check the existence of the def file provided to the set_eco_options in the search_path using the *which* command.

DEFR-002

(error) read def '%s' failed.

Description

read def file failed.

What Next

Check the logfile file provided to the set_eco_options for def file syntax and content related errors.

Feedback

DEFR-004

(error) Cannot find %s '%s' at lineNumber %d.

Description

The specified object cannot be found in the verilog netlist.

What Next

Check that the specified object exists in the design, if it is a design object. Or check that the specified object exists in the library, if it is a library or technology object.

DEFR-017

(warning) Skipping unplaced component '%s' at lineNumber %d.

Description

The specified component is skipped because it has no placement information.

What Next

Check the component in the def file for FIXED, COVER or PLACED placement keywords.

DEFR-050

(error) Reference cell %s of instance %s has invalid size. It's width is %d and height is %d at lineNumber %d.

Description

This error comes when the reference cell to which the def instance is bound to has invalid coordinates.

What Next

Check the reference cell definition in the LEF files provided to set_eco_options command. Usually this definition can be found in the standard cell LEF or the block LEF file. Ensure the existance and correctness of the reference cell width and height coordinates.

DEFR-051

(warning) Instance '%s' extends outside the core area of physical block %s at lineNumber %d.

Feedback

Description

The specified component is not fully contained inside the core area of the physical block it lies in. Any physical constraint that is applicable to the region that lies outside the core area of the physical block will be ignored.

What Next

Check the component bounding box and the physical block bounding box coordinates in the def file provided to the set_eco_options for correctness.

DEFR-052

(warning) Instance '%s' not found in the logical netlist at lineNumber %d.

Description

The specified component cannot be found in the verilog netlist files provided. This component will be skipped.

What Next

Check the verilog netlist files and the def file provided to the set_eco_option. Ensure logical netlist is consistent with the physical information.

DEFR-053

(warning) Physical binding of instance '%s' with reference cell is not consistent with logical binding. Physical reference cell is '%s' while the logical reference cell is '%s' at lineNumber %d.

Description

The specified component is bound to a different reference cell in the physical and logical netlist. The physical binding for this component will be honored while processing the physical information.

What Next

Check the logical and the physical bindings for this component.

DEFR-054

(error) No LEF Macro cell named %s found for instance '%s' in design %s at lineNumber %d.

Feedback

Description

The specified component is not bound to any LEF Macro. The tool will error out.

What Next

Check the list of LEF files provided to set_eco_options command. The LEF file containing this component's macro cell definition maybe missing.

DEFR-055

(error) Instance '%s' is a HALO. However it has invalid coordinates (%d %d %d %d) at lineNumber %d.

Description

The specified component is HALO with invalid coordinates provided to create the HALO blockage.

What Next

Check the HALO definition in the def file provided to the set_eco_options command for correctness.

DEFR-056

(error) Invalid ROW '%s' detected at lineNumber %d.

Description

The specified ROW is invalid.

What Next

Check SITE sitename definitions in the LEF files provided to the set_eco_options. A matching sitename to this ROW name must exist. If it exists, ensure the matching SITE sitename in the LEF has valid width and height specified.

DEFR-057

(warning) Cannot create rectangles from polygon shapes for MACRO instance '%s' defined at lineNumber %d.

Description

The specified component is MACRO cell with polygon shapes. However the polygon shapes inhibit creation of smaller rectangular shapes. This maybe because some or all coordinates of the polygon shape are invalid, non orthogonal or have odd numbere of

intersecting edges. Incase the polygon has intersecting edges, an even number of edges is required to faciliate creation of smaller rectangles from it. The polygon shapes for this MACRO will be ignored and the rectangular shape from the LEF file for this MACRO will be used instead.

What Next

Check the component's polygon shape in the def file provided to the set_eco_options for correctness.

DEFR-058

(Information) Instance '%s' is a MACRO cell with placement obstructions at lineNumber %d.

Description

The specified component is MACRO cell with placement obstructions specified in the LEF file.

DEFR-059

(warning) NAMECASESENSITIVE statement detected with value %d.

Description

The NAMECASESENSITIVE statement's valid value is 0. This NAMECASESENSITIVE will be skipped.

What Next

Check the def file provided to the set_eco_options for correctness of the NAMECASESENSITIVE statement.

DEFR-060

(error) No Metal Layer of TYPE ROUTING defined by LAYER layerName statement in any LEF file.

Description

There are no Metal Layers of TYPE ROUTING defined in any LEF file provided. Metal routing layer information is mandatorily needed to create valid physical information for vias.

Feedback

What Next

Check the LEF files provided to the set_eco_options command for for Metal Layer definitions of TYPE ROUTING. These definitions are usually present in the technology LEF file. Ensure the technology LEF file is provided in your search_path using the *which* command. Additionally ensure it contains some Metal ROUTING layer definitions.

DEFR-061

(warning) Via definition '%s' has invalid number of layers '%d' specified at lineNumber %d.

Description

The via definition specified has invalid number of layers specified. The number of layers specified for each via definition must be greater than or equal to 3. Skipping this via definition.

What Next

Check the DEF file provided to the set_eco_options command for for via definition for correctness.

DEFR-062

(warning) Via definition '%s' has invalid top '%s' or bottom metal '%s' layer specified at lineNumber %d.

Description

The via definition specified has invalid metal layers specified. Each via definition must have a valid top and bottom metal layer. This via definition will be skipped.

What Next

Check the DEF file provided to the set_eco_options command for for layers specified in the via definition for correctness.

DEFR-063

(warning) Placement blockage associated with component '%s' is not supported at lineNumber %d.

Description

The placement blockage is associated with the specified component cell. Component specific placement blockages are not supported. This placement blockage will be ignored.

Feedback

What Next

Component specific placement blockages are specified using the +COMPONENT component_name syntax in the DEF file provided to the set_eco_options.

DEFR-064

(warning) Port '%s' is specified with invalid geometry (%s %s %s %s) at lineNumber %d.

Description

The pin geometry is specified in microns in the (xl yb xr yt) format. The specified pin definition has invalid geometry. Skipping this pin.

What Next

Check the pin placement geometry specified in the DEF file provided to the set_eco_optins for correctness.

DEFR-065

(error) Invalid ROW '%s' detected at lineNumber %d.

Description

The specified ROW is invalid.

What Next

Check SITE sitename definitions in the LEF files provided to the set_eco_options. A matching sitename to this ROW name must exist. If it exists, ensure the matching SITE sitename in the LEF has valid width and height specified.

DEFR-066

(warning) Duplicate ROW '%s' definition detected at lineNumber %d.

Description

The specified ROW is duplicate. This ROW definition will be skipped.

What Next

Check the ROW definitions in the DEF files provided to the set_eco_options for duplicate entries.

Feedback

DEFR-067

(warning) Ignoring net %s as it is (USE : %s) at lineNumber %d.

Description

The specified net is not a signal net. No Physical ECO is permitted on this net. This net will be skipped.

What Next

Check the +USE <type> for this net in the DEF files provided to the set_eco_options. Physically aware ECO commands only work on + USE SIGNAL nets.

DEFR-068

(warning) Identified FIXED cell %s at lineNumber %d. Sizing is disabled for this cell.

Description

The specified component has its DEF placement marked FIXED. Sizing is disabled for this cell.

What Next

Check the + FIXED placement attribute for this component in the DEF files provided to the set_eco_options. Physically aware ECO commands only work on + PLACED components.

DEFR-069

(warning) Identified +COVER cell %s at lineNumber %d. Sizing is disabled for this cell.

Description

The specified component has its DEF placement marked COVER. Sizing is disabled for this cell.

What Next

Check the + COVER placement attribute for this component in the DEF files provided to the set_eco_options. Physically aware ECO commands only work on + PLACED components.

DEFR-070

(warning) Treating filler cell %s as occupied_site as it is marked FIXED at lineNumber %d.

Feedback

Description

The specified component is marked FIXED in the DEF file provided to set_eco_options. This instance of LEF filler cell macro will not be treated as open_site by physically aware ECO commands.

What Next

Check the + FIXED placement attribute for this component in the DEF files provided to the set_eco_options. Only + PLACED components that are instances of LEF filler cell macros will be treated as open_site by physically aware ECO commands when eco_allow_filler_cells_as_open_sites is set to true. This variable's default value is true.

DEFR-071

(warning) Treating filler cell %s as occupied_site as it is marked COVER at lineNumber %d.

Description

The specified component is marked COVER in the DEF file provided to set_eco_options. This instance of LEF filler cell macro will not be treated as open_site by physically aware ECO commands.

What Next

Check the + COVER placement attribute for this component in the DEF files provided to the set_eco_options. Only + PLACED components that are instances of LEF filler cell macros will be treated as open_site by physically aware ECO commands when eco_allow_filler_cells_as_open_sites is set to true. This variable's default value is true.

DEFR-072

(warning) DEF Port %s has POLYGON shape at lineNumber %d.

Description

The specified PORT has POLYGON shape in DEF file provided to set_eco_options. Polygon shapes are not supported for DEF port pins. This port will be ignored and no physical ECO is supported for paths to and from this port.

What Next

Check the PINS section in the DEF file provided to set_eco_options for this port's definition for POLYGON shape. Only ports with RECT shapes are currently supported by physically aware ECO commands.

Feedback

DEFR-073

(warning) DEF Port %s is marked SPECIAL at lineNumber %d.

Description

The specified PORT is marked as a special pin in the DEF file provided to set_eco_options. Regular routers do not route to special pins. The special router routes special wiring to special pins. This port will be ignored and no physical ECO is supported for paths to and from this port.

What Next

Check the PINS section in the DEF file provided to set_eco_options for this port's definition for SPECIAL routing. Only ports routed by regular routers are supported by physically aware ECO commands.

DEFR-074

(warning) Cell %s is inside a placement blockage or is marked FIXED or COVER.

Description

The specified cell lies either inside a placement blockage or is marked FIXED or COVER in the DEF file provided to set_eco_options. As a consequence physically aware ECO commands will not size this cell. Sizing is only permitted on cells that lie outside of placement blockages and are marked PLACED. If buffer insertion is an available ECO fixing method provided, the portion of the net connected to this cell that does not lie in a physical blockage can be leveraged for buffer insertion to fix violations.

What Next

Check the COMPONENT section in the DEF file provided to set_eco_options for this cell's placement specification for FIXED or COVER. Incase the placement specification is PLACED, then check if this cell lies in a placement blockage.

DEFR-075

(warning) Could not find the via cell %s used by net %s.

Description

The specified via cell's definition not exist in any LEF file provided to the set_eco_options. This net cannot be traced to all sink pins routed through this via cell. As a consequence if there a timing/ DRC violation on one or more of those sink pins, physically aware ECO commands cannot deploy buffer insertion as a fixing methodology to fix those violations. Sizing can still be used to fix violations on such pins. This via cell will be ignored.

Feedback

What Next

Check the via cell definition in the LEF files provided to set_eco_options for correctness.

DEFR-076

(warning) Ignoring + HALO 0 0 0 0 for component %s as it does not enclose a region inside this component at lineNumber %d.

Description

The specified component has a hard HALO 0 0 0 0 defined on it in the DEF file provided to the set_eco_options. This HALO specification is invalid as it does not enclose any region inside the component. This HALO will be ignored.

What Next

Check the HALO specification for this component in the DEF file provided to set_eco_options for correctness. Only hard HALOs that specify a valid region inside the component are considered HALOs by physically aware ECO commands. No placement blockage will be created for this HALO specification.

DEFR-077

(warning) Identified physical only PORT '%s' at lineNumber %d.

Description

The specified PORT pin cannot be found in the verilog netlist. This PORT will be ignored.

What Next

Check that the specified PORT exists in the design, if it is a design object. Or check that the specified object exists in the library, if it is a library or technology object. Incase this a valid physical only PORT pin, this PORT pin will be ignored. No paths to or from this PORT can be traced in the design. Physically aware ECO commands only work on PORTS and paths to and from PORTS that are preesent both in the verilog netlist and in the physical LEF/DEF files provided to the set_eco_options.

DEFR-078

(warning) Net '%s' has no parasitic nodes with location. add_buffer_on_route to fix setup violations is disabled for this net.

Feedback

Description

Technique add_buffer_on_route can only take place to fix setup violations on nets which have SPEF files generated with parasitic node locations. This net does not have any parasitic node location. add_buffer_on_route will be disabled for this net.

What Next

Check that the SPEF file provided to PrimeTime that contains this net for locations. It is likely the SPEF file is generated without location generation enabled. Parasitic Node locations are manditorily needed for physically aware setup buffer add_buffer_on_route ECO guidance.

DEFR-079

(warning) DEF for physical block %s is missing. Will apply a set_dont_touch on it and all its sub blocks.

Description

The specified component is missing DEF information. No physical ECO guidance will be provided for this physical block and all its sub blocks. The tool will proceed by applying a set_dont_touch attribute on this block and all its sub blocks. Physical ECO guidance will be provided for all other blocks for which DEF is available and which do not lie in the missing block's design sub-hierarchy.

What Next

Check the list of DEF files provided to set_eco_options command for completeness. The DEF file for the specified component maybe missing.

DEFR-080

(information) No LEF Macro cell named %s found for instance '%s' in design %s at lineNumber %d.

Description

The specified component is not bound to any LEF macro. This is allowed for any component with a model name that has been provided in the -allow_missing_lef option.

What Next

The specified component will be omitted from the physical database. If there are cell rows underneath the component's intended footprint, then it may be necessary to add placement blockage to a DEF file to protect that area from cell insertion.

Feedback

DEFR-081

(information) LEF macro named '%s' found for instance '%s' in design '%s' at line number %d, despite being allowed to be missing.

Description

A LEF macro was found for the listed DEF component, despite that macro being allowed to be missing, as specified with the -allow_missing_lef option. Its special dispensation will be ignored, and the instance will be treated normally.

What Next

Check the provided LEF/DEF files and -allow_missing_lef list to ensure that they reflect the desired state of affairs.

DEFW

DEFW-001

(warning) The specified units-per-micron value of %d is less than the database length precision of %d.

Description

The database units is less than precision.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-002

(warning) The DEF syntax does not support multiple spacings for non-default rule %s layer %s.

Description

Unsupported syntax detected for non-default rules.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

Feedback

DEFW-003

(warning) Skipping invalid scan chain %s; %s.

Description

Scan chain is invalid.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-004

(error) Failed to write from unsupported current design view '%s'.

Description

current design view is invalid.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-005

(error) Cell '%s' has multiple keepouts; only the %s keepout is written.

Description

The cell has multiple keepout margins.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-006

(Information) Creating dummy net '%s' for unconnected port '%s'.

Description

The port is unconnected.

Feedback

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-007

(warning) Library '%s' is missing technology information.

Description

Missing technology information.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-008

(Information) The specified %s '%s' cannot be written; %s.

Description

unsupported DEF syntax detected.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-009

(Information) DEF %s section is filtered by the -objects option list; %d %s written to this section.

Description

DEF section is filtered out.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-010

(warning) %d %s ignored in the -objects option list; %s.

Feedback

Description

DEF syntax is ignored.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-011

(warning) Unsupported mask '%s' found for %s '%s'.

Description

Mask is unsupported for this DEF category..

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-012

(Information) Converted site definition '%s' to '%s'.

Description

Site row converted.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-013

(Information) Design '%s' contains net fills which cannot be expressed using DEF 5.7 syntax.

Description

Net fills are not supported in DEF 5.7.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

Feedback

DEFW-014

(warning) 'routing_rules' is not in the include_list for option -include.

Description

Routing rules are not included.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-015

(error) Technology information is missing for layer number '%d'.

Description

Missing technology information for layer.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-016

(error) Via definition '%s' referenced by routing rule '%s' is undefined.

Description

Missing via definition.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-017

(warning) Skipping invalid trim metal shape on layer "%s".

Description

Trimp metal shapes on said layer are ignored.

Feedback

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-018

(warning) Layer "%s" has wrong-way default width.

Description

Layer definition is invalid.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-019

(warning) Technology information is missing for purpose number '%d' of layer number '%d'.

Description

Missing technology information.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-020

(error) DEF version 5.7 does not support '%d' units per micron.

Description

The DEF version 5.7 file cannot be written out with the specified units per micron value.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-021

(error) Tech precision value is used as units per micron and DEF version 5.7 does not support '%d' unitsPerMicron.

Feedback

Description

The DEF version 5.7 file cannot be written out with current units per micron value.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-022

(error) Routing rules must be included when the application option 'file.def.non_default_width_wiring_to_net' is true.

Description

Routing rules are necessary because write_def needs to generate nondefault rules in DEF, when the the application option 'file.def.non_default_width_wiring_to_net' is set to true. This application option causes write_def to output nondefault width wiring to the DEF NETS section. In order to do so correctly, write_def needs to generate dummy nondefault rules with the wiring width in the DEF NONDEFAULTRULES section. These rules are referenced by the DEF NETS section to define the nondefault width wiring. If the rules are missing, the DEF is incomplete and read_def cannot process the DEF NETS section.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-023

(warning) Cannot output shield net for net '%s', because it is shielded by unnetted shapes.

Description

The specified net is shielded by shapes that are not owned by any net. In order to express the net's shield net relationship with the DEF "+ SHIELDNET shieldNetName" statement in the output, the shield shapes must be owned by a net (e.g., a ground net).

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

DEFW-030

(warning) Net shape '%s' shields multiple nets. Writing the first shielded net only.

Feedback

Description

The given shape shields more than one nets. The DEF SPECIALNETS wiring syntax "+ SHIELD shieldNetName" supports shielding one net only. The DEF Writer writes out this syntax, only for the first net shielded by the net shape.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

Use 'add_shield_association' and 'remove_shield_association' commands to correct the shield association between the specified net shape and shielded net in Fusion Compiler.

DEL

DEL-001

(error) You cannot mix an LCD operating conditon with a non LCD operating condition.

Description

A operating condition is detected to be an LCD operating condition, while another specified operating condition is not an LCD operating condition. The ability to specify two different types of operating conditions is not supported.

What Next

Supply a consistent min and max operating conditions. Either two non-LCD operating conditions or two LCD operating conditions.

DEL-002

(error) You cannot specify a single LCD operating conditon.

Description

LCD operating conditions can be specified in min-max mode only.

What Next

You need to use the min-max mode with LCD operating conditions.

DEL-003

(warning) Library '%s' has time unit of %gnsbut the main library unit is %gns

Feedback

Description

If multiple libraries are used in analysis, they must have the same units. This restriction will be removed in a future version of PrimeTime.

What Next

Convert the units in the .lib and regenerate a library .db file using Library Compiler if possible.

DEL-004

(warning) Library '%s' has capacitive_load unit of %gpFbut the main library unit is %gpF

Description

If multiple libraries are used in analysis, they must have the same units. This restriction will be removed in a future version of PrimeTime.

What Next

Convert the units in the .lib and regenerate a library .db file using Library Compiler if possible.

DEL-005

(error) Cannot remove operating_condition from cell '%s': Power rails inherited from '%s' would not match rails of cell '%s'.

Description

Removing rail voltages or an operating condition from a hierarchical cell, may cause a lower level leaf cell to inherit a new set of power rails from a higher level hierarchical cell. Such a removal is disallowed unless the power rails in the library of the leaf cell are a subset of the newly inherited rails.

What Next

Ensure that appropriate rail voltages/ operating conditions have been previously set on such leaf cells.

DEL-006

(warning) The operating condition does not define all rails of cell '%s'.

Feedback

Description

The operating condition or rail voltage does not contain all power rails therefore default voltages will be used on the remaining power rails. The default voltages are defined in power_supply section of the .lib.

What Next

Ensure that the power rails specified in the library of the cell are same as (or a subset of) the rails in the operating condition.

DEL-007

(warning) Setting of multi-rail operating condition or rail voltage on hierarchical cell '%s' may result in incomplete assignment of power rails.

Description

Assignment of voltages to power rails on multi-rail cells is based on matching rail names in the operating conditions and power_supply definition in library description of the cell.

When setting operating condition or rail voltages on hierarchical cell this information is inherited by all cells in the hierarchy unless they have their explicit operating condition or rail voltage. Since rails in two different libraries can have same name then the effect of setting operating condition or rail voltage with multiple rails on hierarchical cell may result in unintended or incomplete voltage assignment.

What Next

Set an operating condition or rail voltages on any lower level cells that require different power rail voltages.

DEL-008

(warning) Default %s operating conditions per library resulted in cells having different temperature, e.g., %s has %g but %s has %g.

Description

This warning message tells you that default operating conditions assigned to cells may not represent actual operating environment because temperature is not same for all cells in the design.

This message is displayed during update_timing.

What Next

If the temperature difference is intentional and you are trying to model temperature variation on the chip then no action is required. If not intentional then use

set_operating_conditions to explicitly set operating conditions on the design or individual blocks.

See Also

- set_operating_conditions
- report_cell
- default_oc_per_lib

DEL-009

(error) Cannot set single rail voltage on multirail cell '%s'.

Description

You may not set a single rail voltage on a cell using set_rail_voltage -rail_rvalue if that cell has multiple power rails defined in the library.

What Next

Use set_rail_voltage -rail_list.

DEL-010

(Error) Unable to parse input/output_voltage in lib '%s': ('%s' = '%s').

Description

When parsing the input_voltage or output_voltage attribute of a library, PrimeTime has encountered a string that it cannot parse. Note that PrimeTime can only parst binary expressions for input/output_voltage.

What Next

Ensure that the input/output_voltage attributes of you library contain only binary expressions.

DEL-011

(information) The most constraining rise and fall values of the '%s' constraint arc occur for different input conditions.

Description

Due to non-monotonicity in arc data, the most constraining rise and fall delay values arise from different computation input parameters. In most libraries, constraint arcs are

characterized with respect to the transition time at the clock or reference pin as well as the transition time at the data or related pin. In min-max analysis modes, the arc delay can be computed in two libraries, with min and max values on the input transitions. Specifically, in on-chip-variation (OCV) mode, up to eight calculations may be necessary to identify the most constraining value of the arc delay.

Given that the delay is a potential permutation of various input parameters, it is possible that the most constraining, or maximum, rise and fall delays arise from different permutations of the input parameters. This scenario has occurred for the specific constraint arc delay being reported.

What Next

This is an advisory message as no further action is necessary.

DEL-012

(error) The desired operating-condition setting for cell '%s' is improper for '%s' analysis due to %s.

Description

Operating-condition or rail-voltage or temperature setting should only be set so that it is covered by the scaling library group or the linked library when there is no scaling group. If the *define_scaling_lib_group* command was used to setup a group of libraries that includes the specified lib cell, any operating-condition or rail-voltage set on the cell must be within the process, voltage, and temperature domain covered by the group. When -exact_match_only is specified on that scaling group, the operating condition of the cell must match with the operating condition of one library in the scaling group. In the above two cases, set_voltage, set_rail_voltage, set_operating_conditions, or set_temperature command are not allowed to set a wrong operating condition. When there is no associated scaling group, and the desired setting does not match that of the linked libraray, this message is issued to let you know wrong setting is used and there is no CCS scaling support. However the setting is allowed to be performed so that you can still use k-factor scaling on NLDM data.

Note that the complete operating_conditions check is so far only available in *check_timing*. There is no operating_condition check in *update_timing* to avoid runtime penalty on every *update_timing*. *check_timing* does not issue *DEL-012*, but it performs the same check and report all violations.

What Next

Correct either the operating condition or the scaling library group.

Feedback

See Also

- define_scaling_lib_group
- create_operating_conditions
- set_operating_conditions
- set_voltage
- set_rail_voltage
- set_temperature
- check_timing

DEL-013

(information) Assuming the default level shifter strategy '%s'

Description

The commands without any arguments resets the level shifter strategy to the default 'all'. Default strategy is to reports all driver and load signal signal level mismatches.

What Next

To set a specific startegy use *set_level_shifter_strategy -rule <strategy>*.

See Also

- set_level_shifter_strategy
- check_timing
- set_level_shifter_threshold

DEL-014

(information) The operating conditions set are outside the conditions defined by the libraries in the scaling group for atleast one instance in the design, so extrapolation is being done.

Description

If you set an operating-condition that goes outside the domain covered by an applicable scaling library group, extrapolation will be done for the given operating condition it the scaling libraries are defined for atleast two different operating conditions. If the define_scaling_lib_group command was used to setup a group of libraries that includes

the specified cell, any operating-condition or rail-voltage set on the cell must be within the process, voltage, and temperature domain covered by the group to avoid any extrapolation.

What Next

Correct either the operating condition or the scaling library group if extrapolation is not desirable.

See Also

- define_scaling_lib_group
- create_operating_conditions
- set_operating_conditions

DEL-015

(warning) The operating conditions set are far outside the conditions defined by the libraries in the scaling group for atleast one instance in the design, so extrapolation far beyond the safe range is being done.

Description

If you set an operating-condition that is outside the domain covered by an applicable scaling library group, extrapolation will be done for the given operating condition if the scaling libraries are defined for atleast two different operating conditions. If the define_scaling_lib_group command was used to setup a group of libraries that includes the specified cell, any operating-condition set on the cell must be within the process, voltage, and temperature domain covered by the group to avoid any extrapolation. The accuracy of results may not be good if the operating conditions are set far outside the domain of the scaling group.

What Next

Correct either the operating condition or the scaling library group if extrapolation is not desirable.

See Also

- define_scaling_lib_group
- create_operating_conditions
- set_operating_conditions

Feedback

DEL-016

(information) PrimeTime did not compute a valid '%s' transition at input; report_delay_calculation will use zero instead.

Description

Transition times at the output of disabled arcs or non-driven transitions of half unate arcs are considered invalid and are propagated as such in PrimeTime so as not to merge with valid signal transitions downstream. For the purposes of delay calculation, a zero slew is used to perform the cell arc calculation. Even though using a zero input slew could result in a corresponding non-zero output slew, this output slew is in turn marked invalid.

What Next

This is an advisory message as no further action is necessary.

DEL-017

(information) The minimum values of the '%s' constraint arc are not used by timing analysis.

Description

For the evaluating the worst possible conditions for a timing violation and given that timing constraint senses implicitly encode minimum versus maximum conditions such as hold and setup, PrimeTime strictly uses the maximum computed constraint arc delay values for computing endpoint slack.

PrimeTime computes and preserves the minimum delay values for constraint arcs for two reasons. First, these minimum values are exported through attributes off the timing_arc object for general use. Second, other applications dependent on PrimeTime delay calculation through SDF generation do require minimum values to be present.

What Next

This is an advisory message as no further action is necessary.

DES

DES-001

(error) Current design is not defined.

Feedback

Description

The current design is not defined. Many commands require that the current design is set.

What Next

You must read a design database file and link a design.

DES-002

(error) Cannot find %s '%s' in design '%s'

Description

The specified object cannot be found in the given design. This is sometimes seen while reading SDF and parasitics files. In those cases, it could indicate a file which is out of sync with the design.

What Next

If reading SDF or parasitics, verify that the file matches the design.

DES-003

(error) '%s' cannot be used on %s %s '%s'.

Description

Certain commands are valid only for input or output objects.

What Next

Enter the command with a valid list of objects.

DES-004

(error) Cannot find design '%s'.

Description

There is no design with that name is in memory.

What Next

Read in the design or reenter the command with a different name.

DES-005

(Error) Cannot set current instance to leaf cell '%s'.

Feedback

Description

The current instance must be a hierarchical cell.

DES-006

(error) Cannot find pin '%s' on cell '%s'.

Description

The pin does not exist on the specified cell.

What Next

Use *query_objects [select_pin -of_object [select_cell cell_name]] to list pin names on the cell.*

DES-007

(warning) '%s' is not a valid object type.

Description

When -from or -to option is used with set_disable_timing or remove_disable_timing , the object list can only be a cell or a lib cell. This warning is generated for objects of type port and pin.

What Next

Don't use -from or -to option to disable pins or ports.

DES-008

(error) Cannot find %s '%s' in library '%s'.

Description

The specified object cannot be found in the given library.

What Next

Enter the command again with a valid object name.

DES-009

(error) Cannot find pin '%s' on library cell '%s'.

Feedback

Description

The pin does not exist on the specified library cell.

What Next

Enter the command again with a valid object name.

DES-010

(error) Cannot find %s '%s'.

Description

The specified object cannot be found.

What Next

Enter the command again with a valid object name.

DES-011

(error) Cell '%s' is not hierarchical.

Description

The command only works on hierarchical cells.

What Next

Enter the command again with a hierarchical cell.

DES-012

(Error) Cannot use '%s' command on %s '%s'.

Description

The command works only on ports of a specific direction.

DES-013

(Error) Current design is not in min-max mode.

Description

Most of the -min and -max options of commands work only when the design is in min-max mode. The design is considered in min-max mode when 2 operating conditions are specified, such as "set_operating_condition -min OCbest -max OCworst". The design can

also be in min-max mode after reading an SDF file with the -min_max option (for example, read_sdf -min_max mydesign.sdf).

DES-014

(Error) Object '%s' is not in the current design.

Description

You attempted an operation on an object that is outside of the scope of current design. For example, if you select a cell from one design, and attempt to set the current instance to that cell in a different (current) design, this error is generated.

DES-015

(error) Cannot use '%s' command on %s '%s' because it is a limited design.

Description

Access to a design is limited because it requires a license and the only license available was a limited license. As a result, the internals of the design are hidden. Some reports are able to work around limited designs (and instances of them), but some cannot.

What Next

If the design is licensed for full access, ensure that you can check out that license before reading the design. Some designs will always be limited.

DES-016

(error) Cannot use '%s' command on %s '%s' because it contains instances of limited designs%s.

Description

Access to a design is limited because it requires a license and the only license available was a limited license. As a result, the internals of the design are hidden. Some reports are able to work around limited designs (and instances of them), but others cannot.

What Next

If the design is licensed for full access, ensure that you can check out that license before reading the design. Some designs will always be limited.

DES-017

(information) Could not auto-link design '%s'.

Feedback

Description

You executed a command that tried to link the current design. The design could not be linked or it already failed to link. The design now has unresolved references.

What Next

Determine the reason for the unresolved references. This might require changing the value of the search_path or link_path variables. If these references are not yet defined, you can make the linker create black-boxes for them by setting the variable link_create_black_boxes to true. Finally, relink the design using the *link_design* command.

DES-018

(error) There is already an operating condition named '%s' in library '%s'.

Description

The *create_operating_condition* command cannot overwrite an existing operating condition.

What Next

Choose a new name for the operating condition. To list the existing operating conditions in the specified library, use *report_lib*.

DES-019

(warning) Library '%s' has been generated with an old version of the Library Compiler. It needs to be rebuilt to support case analysis on sequential cells.

Description

You receive this message if the current library DB is out of date. The library DBs have detailed functional information generated by Library Compiler from the library .lib file. Information generated by Library Compiler prior to version 2000.11 is not supported.

What Next

Use Library Compiler to regenerate your library DB. Follow these steps:

1. Read in the .lib file.

   ```
   dc_shell> read_lib mylibrary.lib
   ```

2. Write out the .db file.

   ```
   dc_shell> write mylibrary.db
   ```

Feedback

DES-020

(warning) No operating condition is specified, assuming a voltage value of %s volts for RC delay calculation.

Description

No operating condition is specified for the current library, so PrimeTime does not know what is the voltage value when performing RC delay calculation

What Next

Specify the operating condition of the current library with *set_operating_condition*. To get a list of the operating conditions of your library, use *report_library*.

```
pt_shell> report_library my_lib.db

   Name                 Process     Temp        Voltage     Tree Type

 --------------------------------------------------------------------------
---
   WCCOM                3.00      115.00        3.00     balanced_case

pt_shell> set_operating_condition WCCOM
```

DES-023

(warning) Net '%s' is multi-driven.

Description

The specified net is multi-driven by non-three-state cells. PrimeTime will try to peform multi-driven delay calculation for all switching scenarios defined by the networks attached to the drivers' from-pins. In order for such scenarios to be valid, a given from-net must uniquely cover all of the strong drivers attached to the multi-driven to-net.

If a from-net does not cover all of the strong drivers, or if a from-net is attached to more than one pin on a specific driver, detailed RC delay calculation cannot be performed. Instead, fractional lumped analysis will be used; the load will be assumed to be the total capacitance of the multi-driven net divided by the number of drivers.

What Next

Verify that you indeed want the indicated net to be multi-driven. This capability is commonly used to wire cells in parallel to achieve greater drive strength.

Feedback

See Also

- RC-002
- RC-003

DES-024

(warning) Net '%s' has an incomplete RC network.

Description

The specified net has an imcomplete RC network. This means that some RC elements are dangling, or that all drivers and loads of the nets are not connected by all the RC elements.

What Next

The RC network annotation is ignored for the specified net.

DES-025

(error) Pin '%s' is not connected to net '%s'. Ignoring annotation on net '%s'.

Description

You receive this message if the *read_parasitics* command has found the specified pin in the parasitics file but not in the design file; therefore, *read_parasitics* cannot annotate the associated net. Possible causes for this error could include spelling errors or typos, or writing the parasitics file and the design file from different versions of the design.

What Next

Verify that the specified pin is connected to the specified net in both the parasitics file and the design file, and that both are spelled correctly. Regenerate the files if necessary, then reexecute *read_parasitics*.

See Also

- read_parasitics

DES-026

(error) %s pin '%s' is not connected to the RC network of net '%s'. Ignoring the incomplete RC network of the net.

Feedback

Description

You receive this message if *report_annotated_parasitics* detects an incompletely back-annotated RC network in the current design. The message informs you that the RC network on the specified net is being ignored, because it is incomplete; the specified pin is not physically connected to the RC network.

An incomplete RC network might be caused by errors in the parasitics file, or by missing information from the tool that generated the parasitics file. For example, a parasitics file generated by a place and route tool that has parasitics only for the top level (between the blocks) would generate this error, because PrimeTime requires the RC network to connect all leaf drivers to all leaf nodes.

What Next

Examine the SPF or SPEF file to determine why the specified RC network is incomplete. If the error is caused by a valid incomplete network, you can complete it using the parasitics completion feature *read_parasitics -complete_with* or *complete_net_parasitics*. For other errors, you must correct the parasitics file manually. You might need to estimate the missing segments and manually add them. After you have corrected the SPF or SPEF file, reexecute *read_parasitics*.

To determine whether the parasitics file contains a valid incomplete RC network, start from a driver and try to reach all loads through resistances. If all missing segments of a net are between two pins, you can complete them using the parasitics completion feature; otherwise, you must correct the SPF or SPEF file manually.

See Also

- complete_net_parasitics
- read_parasitics
- report_annotated_parasitics

DES-027

(warning) net '%s' has too many (%d) RC elements. Lumped capacitance is used.

Description

The specified net has too many RC elements (more than 10,000). RC delay calculation using AWE technique cannot handle such large RC networks.

What Next

The very large RC network of the net needs to be reduced to a smaller number of RC elements to be handled by PrimeTime.

Feedback

DES-028

(Information) Derived library resistance unit is %f Kohm (Time unit is %.f ns, and Capacitance unit is %f pF).

Description

The library resistance unit is implicit in the synopsys library, it is derived from the library time and capacitance units which are explicit.

DES-029

(Error) Library '%s' has no voltage rails defined.

Description

An attempt was made to define rail voltages to a library which does not have defined rail voltages. It is usually because the library is not a DPCM library, or that the DPCM library does not have pre-defined rail voltages.

DES-030

(error) cannot find rail voltage '%s' in library '%s'.

Description

The specified rail voltage is not declared in the DPCM library. It may be because of a typo.

What Next

Report the specified rail voltage names specified in the DPCM library by executing command report_lib for the specified library. report_lib reports all specified rail voltage names declared in DPCM.

DES-032

(warning) Failed to compute %s RC net delay from '%s' to '%s'.

Description

The delay calculation failed to compute the delay for the given detailed RC network, hence the lump model will be used for delay calculation.

What Next

Simplify the RC network and check if the RC enviorment vairables are set correctly.

Feedback

DES-033

(Error) Failed to compute C-effective for the following timing arc: (%s) %s/%s-->%s (%s %s)

Description

The cell delay calculation failed to compute the effective capacitance of the detailed RC network driven by a specific timing arc, so the total capacitance will be used.

The following are the two most common reasons for this failure:

1.An unrealistically large input transition time or output capacitance has occurred. 2.The RC threshold environment variables are set incorrectly.

Another frequent reason is that library data for the specific sense of timing arc in question is missing or invalid.

The timing arc is displayed by the warning message in the following manner: (<reference-name>) <instance-name>/<from-pin>--><to-pin> (<sense-name>) The sense name has two parts: a rising/falling direction on the to-pin and a sense description.

What Next

You may have to annotate transition times with set_annotated_transition to circumvent unrealistic loading conditions (e.g. like those which you might later solve with buffer trees). Also, be sure the library delay and slew thresholds are set correctly, and that valid library data exists for the desired sense of timing arc through the cell of interest.

See Also

- set_annotated_transition

DES-034

(Warning) subckt '%s' is defined multiple times.

Description

The SPICE deck and all its include files that define the pin order for the SPICE output of the critical has define a subcircuit multiple times.

DES-035

(Error) Out of memory at file %s line %d.

Feedback

Description

Run out of memory during SPICE pin order deck parsing.

DES-036

(Warning) Pin '%s' defined multiple times in subckt '%s'.

Description

A pin is defined multiple time on the SPICE subcircuit header. Only the first one is used.

DES-037

(warning) No SPICE pin order info for cell '%s' (%s).

Description

You receive this message if *write_spice_deck* cannot find the specified cell type in the file you specified using the *-sub_circuit_file* option.

What Next

Examine the subcircuit file and verify that it contains the subcircuit description of the specified library cell. Make any corrections necessary, then re-execute *write_spice_deck*.

DES-038

(error) Library pin '%s' for cell '%s' is not in the SPICE sub-circuit definition.

Description

You receive this message if *write_spice_deck* finds the specified cell in the file you specified using the *-sub_circuit_file* option, but does not find the specified pin.

What Next

Examine the subcircuit file and verify that it contains the specified pin and is consistent with the PrimeTime library. Make any corrections necessary, then re-execute *write_spice_deck*.

DES-039

(warning) SPICE pin '%s' for cell '%s' is not in the library.

Feedback

Description

You receive this message if *write_spice_deck* finds the specified pin in the subcircuit file but cannot find it in the library. If the pin is a power or ground pin, PrimeTime might still be able to do the analysis.

What Next

If the pin is not a power or ground pin, examine the subcircuit file and verify that it is consistent with the PrimeTime library. Make any corrections necessary, then re-execute *write_spice_deck*.

DES-040

(warning) The driver waveform %s is bad and will be ignored.

Description

While reading the driver waveform, the application found that waveform is bad. For example, the number of voltage points in the waveform are less than two.

What Next

Examine your waveform is according to the liberty syntax for driver waveforms. Correct the waveform and re-execute it.

DES-050

(error) Too many %ss matched '%s' in design '%s'

Description

While searching for an object by name, the application found multiple objects that match the name. This usually occurs after some flattening of the design, when the hierarchy character becomes embedded in the names. For backannotation, this is an ambiguous situation, because the application cannot determine which object to annotate.

This situation occurs rarely, during the reading of parasitics files, and could be caused by a design error. Multiple objects in the flat space should not have the same name.

What Next

Examine your design to determine why multiple objects in the flattened file have the same name. Correct the design, then re-execute the application.

Feedback

DES-051

(Error) Command requires a linked design but linking is blocked because auto_link_disable is TRUE.

Description

You receive this message if you execute a command that requires a linked design, your design is not linked, and the *auto_link_disable* variable is set to true. By default, many PrimeTime commands automatically attempt to link the current design for you (for example, *set_load* invokes the linker if the current design is not linked). Setting *auto_link_disable* to true disables the default auto-link process.

What Next

If you intend for auto linking to be disabled, you must link the design manually before executing any commands that require a linked design. Setting *auto_link_disable* to true is intended to be used in conjunction with a manual link step. For more information, see the manual page for the *auto_link_disable* variable.

Alternatively, if you want to enable auto linking, set the *auto_link_disable* variable to false.

DES-060

(warning) Ignoring retain library timing arc from '%s' to '%s'.

Description

You receive this message if the current library DB is out of date. Retain arcs generated by Library Compiler prior to version 2000.11 are not supported.

What Next

Use Library Compiler to regenerate your library DB. Follow these steps:

1. Read in the .lib file.

   ```
   dc_shell> read_lib mylibrary.lib
   ```

2. Write out the .db file.

   ```
   dc_shell> write mylibrary.db
   ```

DES-061

(warning) Found duplicate instantiation of cell '%s' when flattening the hierarchical netlist.

Feedback

Description

You receive this message while outputting a hierarchical netlist in a flattened manner. When flattening the netlist, two instances are being mapped to same name. For example, you may have a cell by name "a/b" at top level and a cell named "b" inside a hierachy named "a". The name of the cell under conflict is given in this message.

What Next

You should uniquify the names of the cells under conflict before doing the current operation.

DES-062

(warning) '%s' unit specified as '%s' does not match with the main library unit '%s%s'.

Description

set_units command can only check the consistency of the specified units with the main library units. Actual setting of units are not allowed.

What Next

If the units of sdc scripts are different, change the sdc scripts so that the units are same as the main library units. It is also possible to select a different library as the main library, which has consistent units as that of sdc scripts.

DES-063

(warning) '%s' unit should be specified in '%s'.

DES-064

(warning) Power unit cannot be checked.

Description

Power unit cannot be checked since no power unit available.

What Next

Enable power analysis mode by setting power_enable_analysis to true, and running power related commands, such as update_power, read_vcd, read_saif, set_switching_activity, etc.

Feedback

DES-065

(warning) '%c' is an unsupported scale.

Description

Valid scales are f|p|n|u|m|k|M.

What Next

Scale the value to the supported scale.

DES-066

(error) Command requires a linked design but linking is blocked because of existing collections.

Description

You receive this message if you execute a command that requires a linked design, your design is not linked, and there are some collections with this design.

What Next

Perform a link first and re-issue the command.

DES-067

(error) Design is already linked.

Description

You are attempting to link a design that is already fully linked. If you want PT to relink, please use -force option.

What Next

No need of any action.

DES-068

(error) Could not find library cell '%s'.

Description

You are attempting to use a library cell in a command and the library cell could not be located in any of the loaded libraries.

Feedback

What Next

Re-issue the command with the correct library cell.

DES-069

(Error) Variable '%s' cannot be set after linking or be reset.

Description

This variable needs to be set before linking or it is not allowed to be reset once is set.

DES-070

(information) Current instance is the top-level of design '%s'.

Description

You executed a command that changes the current instance back to the top-level.

What Next

Check if this design name matches with current design.

DES-071

(info) current_design won't return any data before link

Description

current_design won't return any data before link. Don't use current_design before link to query for any design objects.

What Next

use current_design after link to get the collection.

DES-072

(error) Incompatible options to report_signature. Failed due to: %s

Description

The behaviour of report_signature is dependent on the mode of operation of the current pt_shell (DMSA or regular PT flow etc). Some options to report_signature are hence incompatible.

Feedback

What Next

Refer to the reason for failure in the error message to proceed.

DES-073

(Error) The current_design command must specify the top module name as the argument in the Parasitic Explorer flow.

Description

In the Parasitics Explorer flow, the *current_design* command must specify the top module name as the argument. For example,

```
set_app_var parasitic_explorer_enable_analysis true
read_parasitics -format gpd my_gpd_dir
current_design TOP
```

In this example, the *read_parasitics* command prepares for reading the parasitics but does not actually do the reading until the *current_design TOP* command is run. Using the *current_design* command without an argument triggers the DES-073 error.

When the *current_design TOP* command is run, the tool links the design specified by the *current_design* command and reads in the GPD parasitic data from the specified directory.

What Next

Run the *current_design* command again and specify the top module name as the argument.

See Also

- read_parasitics
- parasitic_explorer_enable_analysis

DES-074

(Information) Resistance unit is %f Kohm (Capacitance unit is %f pF).

Description

The resistance unit is implicit in the synopsys library, it is derived from the library time and capacitance units which are explicit.

DES-075

(error) Cannot set target library subset on cell '%s'; it is not hierarchical.

Feedback

Description

The command only works on hierarchical cells.

What Next

Reissue the command with a hierarchical cell.

DES-076

(Error) Verilog writing disabled due to the presence of encrypted verilog.

Description

When encrypted verilog file is read with read_verilog command, all the commands which writes out the verilog files (like hyperscale netlist) will fail.

What Next

Writing verilog is not possible if the input verilog was encrypted. Please read un-encrypted verilog.

DES-078

(Error) Variable '%s' cannot be set after define_scaling_lib_group.

Description

This variable needs to be set before define_scaling_lib_group.

DES-080

(Information) Detect physical variant lib cell '%s/%s'.

Description

This message is to tell user that physical variant lib cell is detected, this one time information only display one example physical lib cell name, the design could contain other physical variant lib cells.

DFTSCHD

DFTSCHD-001

(warning) No schematic support for DFT violation (%s).

Feedback

Description

Check the man page for %s DRC violation.

DIST

DIST-001

(Error) No user commands specified to be executed.

Description

You receive this message if no user commands were supplied to remote_execute to be executed at the worker machines.

What Next

Specify set of commands to be run on worker machines.

DIST-002

(Error) "%s" option cannot be used in present distributed mode.

Description

You receive this message if an option was specified with remote_execute command whihc is not compatible with the present mode of execution.

What Next

Refer to remote_execute man page.

DIST-003

(Error) No %s specified for the command.

Description

You receive this message if you have not specified a list of objects to be the subject of the remote execution focus.

What Next

Provide a list of objects to be the subject of the remote execution focus.

Feedback

See Also

- remote_execute

DIST-004

(Error) remote_execute cannot be called inside parallel_execute.

Description

You receive this message if you are calling remote_execute inside parallel_execute. remote_execute is not supported to be called inside parallel_execute.

What Next

Refer to man page of remote_execute and parallel_execute

DIST-005

(information) Variable '%s' is assigned the value '%s' following merging of the worker-side value '%s' and the manager-side value '%s'

Description

In the distributed analysis, the indicated variable can be set both at the manager and worker. In this case, the value of the variable at the manager is added to the value of the variable at the worker.

DIST-006

(Warning) The variable '%s' contains a directory '%s' that could not be resolved to an absolute path.

Description

The manager was unable to find the absolute directory location of an entry in a resolved variable. This erroneous entry will not be sent to the worker.

What Next

Remove or correct the erroneous resolved variable entry.

DIST-007

(Error) The distributed farm has encountered a critical failure and all hosts are being stopped, see logs for more information.

Feedback

Description

There was an error in the distributed farm processing that has placed it into an irrecoverable state. Consult the logs to see more about what happened.

What Next

Consult the logs to see more about what happened.

DIST-008

(warning) The type of the specified object is not supported.

Description

The object is not of type list, variable, array, or collection.

What Next

Specify an object that is a list, variable, array, or collection.

DIST-009

(warning) The object %s does not exist.

Description

The specified object does not exist. No object is returned.

What Next

Specify an object that does exist.

DIST-010

(warning) The collection type for object %s is not supported.

Description

The collection type for the specified object is not supported by the distributed objects feature.

What Next

Only query supported collections.

DIST-011

(error) The specified object is not an array.

Feedback

Description

The specified object must be an array indexed by a scenario name.

What Next

Specify an array of the correct type. An array can be created using the array set command.

DIST-012

(error) The specified object %s already exists.

Description

The specified object cannot be returned to the manager because a variable of that name already exists at the manager.

What Next

Use unset to remove the variable at the manager.

DIST-013

(error) Cannot send collection %s to the worker.

Description

The specified collection cannot be sent from the manager to the worker because the collection type is unsupported for the *set_distributed_variable* command.

What Next

Transfer information from the collection into a list or array. Send information to the worker in a list or an array format.

DIST-014

(error) Could not set variable %s because the variable already exists and cannot be overwritten due to incompatible type.

Description

This error has occurred because the *get_distributed_variables* or *set_distributed_variables* command has been issued, and a variable cannot be overwritten at the manager/worker as a variable of that name already exists at the manager/worker of incompatible type.

Feedback

The following variable type transitions are allowed:

```
variable -> collection
variable -> list
collection -> variable
collection -> list
list -> variable
list -> collection
```

The following variable type transitions are disallowed:

```
+0.25in
array -> collection
array -> list
array -> variable
collection -> array
list -> array
variable -> array
```

What Next

Remove the existing variable using the unset command.

DIST-015

(error) Found null value in merged_object when -null_merging_method was set to error.

Description

When merging variables at the manager, this error is issued because the -null_merging_method is set to error and a null value has been found.

What Next

Find the source of the null value.

DIST-016

(error) Could not set %s to be the error log .

Description

The error log was set to an invalid file name. The file name given was either a directory or the file name resolved to a file that could not be opened, or the file name contained a path that could not be resolved.

What Next

Choose a valid file name for the error log.

Feedback

DIST-017

(error) Variable %s size exceeds Tcl limit of 2147483647 characters.

Description

PrimeTime tried to create a Tcl variable of size exceeding Tcl variable size limit of 2147483647 characters (2 GB - 1 byte). For example, this error may be issued if *get_distributed_variables* is called with the option *-merge_type* to merge variables from multiple scenarios into a list and the size of the merged list exceeds the Tcl variable size limit.

What Next

Ensure that *get_distributed_variables* does not create merged variables of sizes larger than 2147483647 characters by limiting the cumulative size of variables received by the command from scenarios.

DIST-018

(Error) Manager job stopped because '%s' [Scope:%s Reason:%s]

Description

A critical error has arisen in the manager process stopping the job managing the tasks being executed by worker processes. This is an unrecoverable error and all tasks and worker processes will be terminated.

What Next

Please run the analysis again with the *distributed_logging* variable at the manager set to highest and send the content of the *system_log* directory to Synopsys for analysis of the problem.

DIST-019

(warning) You are supplying an empty collection or an invalid object pattern / class to %s.

Description

The supplied object specification does not yield any objects (e.g nets, pins, cells) to process.

What Next

Please supply a valid object specification to the command.

DIST-020

(warning) The %s command was issued at %s %s.

Description

The *exit* or *quit* command was issued at a distributed worker process. The behaviour of the command at a distributed worker is controlled by the setting of the *distributed_worker_exit_action* variable.

In the Distributed Multi-Scenario Analysis, the execution of commands for the scenario which issued the 'exit' or 'quit' command is stopped and the scenario will be removed from the current session. The remote worker process running the scenario may be terminated depending on the setting of the *distributed_worker_exit_action* variable.

What Next

Check if the 'exit' or 'quit' command was issued intentionally at a distributed worker.

See Also

- distributed_worker_exit_action
- report_host_usage

DMM

DMM-010

(Warning) Switching between mismatch configs is not recommended.

Description

It is not recommended to switch between configs because there might be some design mismatches already repaired in previous config. And those mismatches will not be in sync with current config anymore. There is currently no provision to re-mitigate or invalidate those already mitigated objects.

What Next

Make sure not to change current config if some mismatches have already been repaired.

DMM-011

(Warning) Changing current repair(handler) for a mismatch type in between a flow is not recommended.

Feedback

Description

It is not recommended to change current repair(handler) for a mismatch type in between a flow because there might be some design mismatches already repaired with previous handler. And those mismatches will not be in sync with current repair anymore. There is currently no provision to re-mitigate or invalidate those already mitigated objects.

What Next

Make sure not to change current repair if some mismatches have already been repaired.

DMM-012

(Warning) Changing action for a mismatch type in between a flow is not recommended.

Description

It is not recommended to change action for a mismatch type in between a flow because there might be some design mismatches already repaired with previous action. And those mismatches will not be in sync with current action anymore. There is currently no provision to re-mitigate or invalidate those already mitigated objects.

What Next

Make sure not to change action if some mismatches have already been repaired.

DMM-013

(Information) No mismatch exists on ref library '%s'.

Description

The specified reference library is found with no mismatch information.

DMM-014

(error) Action '%s' is not allowed for '%s' mismatch type.

Description

This action type is not in the allowed list of actions for this mismatch type.

What Next

Use report_mismatch_config output to check which action types are allowed for this mismatch type.

Feedback

DMM-015

(error) Mismatch config '%s' do not exists.

Description

The provided mismatch config do not exists. Check and use existing configs.

What Next

Use report_mismatch_configs output to check which mismatch configs are available to use.

DMM-016

(error) Mismatch config '%s' already exists.

Description

The provided mismatch config already exists.

What Next

Use report_mismatch_configs to see available configs to use.

DMM-017

(error) Config '%s' does not exists.

Description

The named config does not exists. Please use '-all' option to see the existing configs and use one of them.

What Next

Use report_mismatch_configs to see available configs to use.

DMM-021

(Warning) Over-riding current design mismatch config '%s' by block-specific config '%s'.

Description

The design mismatch config settings are stored on a block when it is created. When it is opened or made the current block, these are restored. If they are different from the session's current config settings, the block's settings over-ride the session's settings and come into effect.

Feedback

What Next

Use 'get_current_mismatch_config' and 'report_mismatch_config -verbose' to check what config settings came into effect. for this mismatch type.d

---

DMM-022

(Information) Restoring current design mismatch config value to '%s'.

Description

The block-specific design mismatch config settings are active when the block is open and is the current block. When the block is closed, these block-specific settings are removed and are replaced by the session's config settings that were in effect before this block was opened. This message indicates that the mismatch config setting has been restored to the previous value.

What Next

Use 'get_current_mismatch_config' and 'report_mismatch_config -verbose' to check what config settings came into effect.

DMM-030

(error) '%s' is an empty rtl module.

Description

This denotes that an empty rtl module is read-in. Configure DMM mismatch empty_logic_module to convert it into macro.

What Next

Use report_mismatch_config output to check which action types are allowed for this mismatch type.

DMM-040

(information) Resizing cell ‘%s’.

Description

When creating a macro type blackbox on an empty module mismatch mitigated using the create_macro strategy, tool will resize the macro without creating a new blackbox.

What Next

This is an information message no action is needed.

Feedback

DMM-041

(warning) Mitigated empty module cannot be moved to specified library or renamed.

Description

When creating a macro type block-box on an empty module mismatch mitigated using the create_macro strategy -library & -name options will be ignored.

What Next

Review your design mismatch configuration and set the correct strategy action for the empty_logic_module, to disable the mitigation.

See Also

- report_design_mismatch

DMM-042

(warning) Mitigated empty module cannot be move to library ‘%s’

Description

When creating a macro type blackbox on an empty module mismatch mitigated using the create_macro strategy the -name option will be ignored.

What Next

Review your design mismatch configuration and set the correct strategy action for the empty_logic_module, to disable the mitigation

See Also

- report_design_mismatch

DMM-100

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

Feedback

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
```

DMM-101

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
```

DMM-102

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
```

```
  Repaired State    %repairedstate
  Repair Strategy    %mmhandler
```

DMM-103

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name    %mmobjname
  Object Name    %objname
  Object Type    %objtype
  Repaired State    %repairedstate
  Repair Strategy    %mmhandler
```

DMM-104

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name    %mmobjname
  Object Name    %objname
  Object Type    %objtype
  Repaired State    %repairedstate
  Repair Strategy    %mmhandler
```

Feedback

DMM-105

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
```

DMM-106

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
```

DMM-107

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type existing on this design. Out of these %d objects are repaired using %s repair strategy.

Feedback

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
  Related Instance Count   %instcount
```

DMM-108

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
  Related Instance Count   %instcount
```

DMM-109

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

Feedback

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
  Related Instance Count   %instcount
```

DMM-110

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
  Related Instance Count   %instcount
```

DMM-111

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
```

```
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
  Related Instance Count   %instcount
```

DMM-112

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
```

DMM-113

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
```

Feedback

DMM-114

(Info) Information: Mismatch type %s is detected on object type %s at object %s. There are total %d objects of this mismatch type on this design. Out of these %d objects are repaired using %s repair strategy.

Description

The mismatch type %mmtype is found to exists on %objtype %objname .

The following table lists more information of the mismatch type:

Table:

```
Field   Information
  Mismatch Object Name   %mmobjname
  Object Name   %objname
  Object Type   %objtype
  Repaired State   %repairedstate
  Repair Strategy   %mmhandler
```

DMM-115

(Warning) Auto deriving '%s' routing direction for layer '%s'.

Description

There is no layer routing direction provided by user and also not available in technology file. So auto deriving the routing direction for the specified layers.

DMM-116

(information) Total %d mismatches are found on block '%s'.

Description

If there exists any inconsistency between design and reference data, they are regarded as a mismatch in the flow. These mismatches can be related to a missing reference, port name case, missing routing direction on a metal layer etc.

When such a mismatch is detected, it is collected and recorded on design. These mismatches are captured during specific flows like linking and routability checks.

What Next

Check output of report_design_mismatch to find more details about mismatches.

Feedback

See Also

- report_design_mismatch

DMM-117

(warning) Reporting design mismatch(es) or creating or setting design mismatch configuration after early data check has been enabled.

Description

User is reporting on design mismatch(es) or is creating or setting design mismatch configuration after the early data check (EDC) system has been enabled. The design mismatch commands and reports are still accepted by the tool after enabling the EDC system. However, the design mismatch manager turned inactive and will no longer check, record, or repair design mismatches since these are now checked and handled by the EDC system. It is still possible to report the mismatches that have been recorded by the design mismatch manager before the EDC system got enabled.

What Next

The warning can be ignored when reporting design mismatches that got recorded before enabling EDC. When creating or configuring design mismatch configuration, consider using the EDC system instead by using related EDC checks with matching policies and strategies. The EDC system is enabled by 'set_early_data_check_policy' or by 'set_qor_strategy -mode early_design' command. Please refer to below commands related to the EDC system.

set_early_data_check_policy

```
report_early_data_checks
get_early_data_check_records
```

DMM-121

(warning) Repair skipped for '%s' for object '%s' as it would cause loss of UPF data.

Description

Repaired skipped for design mismatch as it would cause UPF data loss as part of converting empty logic module to macro.

What Next

If you do not want to repair then change action to 'ignore'. If still repair is needed then enable design mismatch to repair before loading upf.

Feedback

DVD

DVD-001

(error) Can not open DvD file '%s'.

Description

The DvD file name given is incorrect or the search path for this DvD file is not given or the path is incorrect.

What Next

Check whether the DvD file exists and has read permissions.

DVD-002

(warning) Can not close DvD file '%s'.

Description

The DvD file cannot be closed.

DVD-003

(error) Please remove the DvD before reading DvD file '%s'.

Description

Read_dvd is not performed because design has already been annotated with a previously read DvD file.

What Next

Assigning the DvD is allowed only after the existing DvD is removed.

See Also

- remove_dvd

DVD-004

(error) Read_dvd is not performed because there is no format header from file '%s'.

Description

Read_dvd requires a format header in the DvD file.

Feedback

What Next

Make sure the format header is in the beginning of your DvD file, containing "inst_name", and "STA_VDD" or "eff_VDD". For example, "# loc_x loc_y eff_vdd max_pg_w domain inst_name STA_VDD".

DVD-005

(error) Read_dvd is not performed because there is no valid data from file '%s'.

Description

Failed to read any cell name and DvD voltage from the DvD file. Read_dvd is skipped.

What Next

Check your DvD file for the correct syntax.

DVD-006

(warning) Cannot read in cell name and DvD voltage from file "%s" lines [%s]. These lines are skipped.

Description

Failed to read cell name and DvD voltage from the reported lines of the DvD file.

What Next

Check your DvD file for the correct syntax.

DVD-007

(error) Please read the DvD before removing it.

Description

Remove_dvd is not performed because design has not been annotated with a DvD file.

What Next

Use command 'read_dvd' to read in a DvD information first.

See Also

- read_dvd

Feedback

DVD-008

(warning) DvD-aware timing analysis is not performed because -pba_mode is not specified.

Description

DvD-aware timing analysis is only available for *PBA mode*.

What Next

To enable DvD-aware timing analysis, specify the *-pba_mode path|exhuastive* option on *get_timing_paths* or *report_timing*.

See Also

- get_timing_paths
- report_timing

DVD-009

(error) DvD-aware timing analysis cannot specify both -path and -strip_path for read_dvd.

Description

DvD-aware timing analysis can only specify one of -path and -strip_path for read_dvd.

What Next

Use command 'read_dvd' with one of -path and -strip_path only.

DVD-010

(error) read_dvd -rail_map is not performed while parsing file "%s" lines [%s].

Description

read_dvd -rail_map requires correct "object_spec" and "version" in the DvD file.

What Next

Check your DvD file for the correct syntax.

DVD-011

(warning) Cannot read the syntax of rail_map file from file "%s" lines [%s]. These lines are skipped.

Feedback

Description

Failed to read rail_map file from the reported lines of the DvD file.

What Next

Check your DvD file for the correct syntax.

DVD-012

(info) Removing existing dvd rail map.

Description

Removed existing dvd rail map

DVD-013

(info) No existing dvd rail map to remove.

Description

remove_dvd -rail_map_only is not performed because there is no existing dvd rail map to remove.

DVD-014

(info) %lu out of %lu cell(s) annotated with DvD voltage in the design. Annotation rate is %.3f%%.

Description

The message shows the numbers of all cells, cells annotated with DvD voltage in the design and annotation rate.

DVD-015

(error) DvD-aware timing analysis cannot specify both -mode and -rail_map for read_dvd.

Description

DvD-aware timing analysis can only specify one of -mode and -rail_map for read_dvd.

DVD-016

(error) read_dvd -rail_map is not performed while parsing file "%s" lines [%s].

Feedback

Description

read_dvd -rail_map requires only one or two value in scaling, offset and clamp

What Next

Check your DvD file for the correct syntax.

ENV

ENV-001

(error) Value for %s cannot be larger than the %s value.

Description

Some commands work in pairs, specifying a maximum and minimum value. The minimum value must be less than the maximum value. For example, never specify a min_capacitance that is larger than the max_capacitance for the same design or port.

What Next

Remove the old value, or use a different value.

ENV-002

(warning) Invalid value '%s' for variable '%s'. %s

Description

You specified an invalid value for the specified variable. The message should provide valid values for the variable.

What Next

If the message did not provide valid values for the variable, refer to the man page for the variable. Reset the variable with a valid value, then run the command again.

ENV-003

(Information) Using automatic %s wire load selection group '%s'%s.

Description

Automatic wire load selection by area is being performed on the design or on a hierarchical cell. The specified selection group is used to determine which wire load model

to apply to hierarchical cells at and below this cell or design, based on their cell area. There might be a different selection group for max and min conditions.

What Next

To see which wire load models are set, use the *report_wire_load* command.

ERRDM

ERRDM-001

(error) Failed to open error data which is not for the current design.

Description

An attempt was made to open an error data which is not associated with the current design.

What Next

Select an error data file which is associated with the current design.

ERRDM-002

(error) Failed to open error data which does not exist.

Description

An attempt was made to open an error data file which does not exist.

What Next

Select an existing error data file which is associated with the current design.

ERRDM-003

(error) Could not create the error data file.

Description

The error data file could not be created.

What Next

Check for inadequate write permissions on the disk or a possible collision with existing filenames.

Feedback

ERRDM-004

(error) Invalid file format.

Description

An invalid file format was specified for the error data file.

What Next

Provide a valid file format.

ERRDM-005

(error) Corrupt error data.

Description

A syntax error was encountered while reading a corrupt error data file.

ERRDM-006

(error) The error data has unsaved changes.

Description

An attempt was made to close an error data file which has unsaved changes.

What Next

Use the -force option to force closure without saving changes, discarding any pending changes. For exported error data files, you may also use the -save option to first save the unsaved changes. For standard error data attached to a design block, first save the block with save_block, then close the error data.

ERRDM-007

(error) The error data %s is open.

Description

An attempt was made to remove an error data file which has not been closed.

What Next

Close the error data before removing it.

Feedback

ERRDM-008

(error) An error type with the given name already exists.

Description

An attempt was made to create an error type with an existing name. Error type names must be unique.

What Next

Specify a unique name for the new error type.

ERRDM-009

(error) The error class was missing or was invalid.

Description

An attempt was made to create an error type without specifying a valid error class.

What Next

Specify a valid error class.

ERRDM-010

(error) Invalid error type.

Description

An attempt was made to create an error for an invalid error type.

What Next

Specify a valid error type.

ERRDM-011

(error) Invalid error specification.

Description

An attempt was made to create an error with invalid parameters.

What Next

Specify a valid parameters.

Feedback

ERRDM-012

(error) An error data file with the given name already exists.

Description

An attempt was made to create an error data file with an existing name. Error file names must be unique.

What Next

Specify a unique name for the new error data file.

ERRDM-013

(error) The given error data file is read-only.

Description

An attempt was made to edit an error data file which was open in read-only mode.

What Next

Open the error data file in read-write mode.

ERRDM-014

(error) For a top level 3DIC design, you cannot create drc errors with layers.

Description

create_drc_error command cannot be used to specify layers for a top level 3DIC design.

ERRDM-032

(error) For a top level 3DIC design, you cannot create drc errors with layers.

Description

create_drc_error_shapes command cannot be used to specify layers for a top level 3DIC design.

ERRDM-033

(error) At least one of options '-polygons', '-polylines', '-points' or '-endpoints' for create_drc_error_shapes should be specified.

Feedback

Description

create_drc_error_shapes command requires at least one of options: '-polygons', '-polylines', '-points' or '-endpoints' to be specified.

ERRDM-034

(warning) There must be two coordinates given for each endpoint shape.

Description

There must be two coordinates given for each endpoint shape.

ERRDM-035

(error) ERRDM_LOCK_FAIL_ACTION `%s' not one of: `off', `complain', or `die'. Turning off.

Description

This is an internal error. Please report to Synopsys.

What Next

Internal error, please report to Synopsys.

ERRDM-036

(info) lock check failed!.

Description

This is an internal message. Please report to Synopsys.

What Next

Internal message, please report to Synopsys.

ERRDM-037

(error) %s cannot be saved independent of the associated block.

Description

Error data that are attached to a block cannot be saved independent of saving the block.

Feedback

What Next

To save changes to the given error data, call save_block to save the block. Alternatively, you may export the error data to a file using the command write_drc_error_data.

ERRDM-038

(warning) option '-readonly' and '-readwrite' will be ignored when opening error data which is attached with current block.

Description

option '-readonly' and '-readwrite' will be ignored when opening error data which is attached with current block.

ERRDM-039

(error) Use '-endpoints' option with two point coordinates to specify two endpoints for an open error.

Description

Open error accepts only '-endpoints' option with two point coordinates to describe open error shape.

ERRDM-040

(error) Saving to the given version %s is not supported. %s

Description

Provide a version string in the supported range.

ERRDM-041

(error) The drc error data schema version string %s is invalid.

Description

Provide a properly formed version string, <major version number>.<minor version number>, "1.6", for example.

ERRDM-042

(error) The design schema version string %s is invalid.

Feedback

Description

Provide a properly formed version string, <major version number>.<minor version number>, "1.090", for example.

ERRDM-043

(error) The error data %s is closed.

Description

An attempt was made to edit or access data of an error data file which has not been opened.

What Next

Open the error data before editing or accessing its types and violations.

See Also

- open_drc_error_data

ERRDM-044

(error) Unopened error data %s cannot be saved.

Description

An attempt was made to save an error data file which has not been opened.

What Next

Check the error data file input to make sure you specified the correct one.

See Also

- open_drc_error_data

ERRDM-045

(information) Incrementing open_count of error data '%s'.

Description

open_drc_error_data was called for an already opened error data. A reference count was added to the error data. Use close_drc_error_data to decrement the reference count. When the reference count drops to zero, the error data will be closed.

Feedback

See Also

- close_drc_error_data

FILE

FILE-001

(error) Unable to open file '%s' for reading; %s

Description

The file cannot be read for the reason specified.

What Next

Examine the reason given. The file may not exist or may not be readable due to file permissions.

FILE-002

(error) File '%s' cannot be found using search_path of: '%s'.

Description

The file cannot be found on the specified search_path.

What Next

Determine whether the file name or the search_path is incorrect, or whether the file does not exist at all.

FILE-003

(error) Unable to open file '%s' for writing; %s.

Description

The file cannot be opened for writing for the reason specified.

What Next

Examine the reason given. The parent directory may not exist or write permission may be denied.

Feedback

FILE-004

(error) Unable to create directory '%s'; %s.

Description

The directory cannot be created for the reason specified.

What Next

Examine the reason given. The parent directory may not exist or write permission may be denied.

FILE-005

(error) Unable to access directory '%s'; %s

What Next

Check the directory path name.

FILE-006

(error) Unable to remove directory '%s'; %s

Description

The tool was unable to remove the specified directory.

What Next

The directory could not be removed.

FILE-007

(information) Loading %s file '%s'

Description

This informational message shows the full path name and type of a file being read into the application.

What Next

Use the full path name to help understand any problems encountered while reading the file.

Feedback

FILE-008

(error) Directory '%s' already exists

Description

The directory with the specified name already exists.

What Next

Try another name for the new directory.

FILE-009

(error) File '%s' already exists

Description

A file with the specified name already exists.

What Next

Try another name for the new file.

FILE-010

(error) Unable to lock file '%s' for write @%s; %s.

Description

The file cannot be write-locked for the reason specified.

What Next

Examine the reason given. The file may be locked by another process or lock services may not be available on this server.

The reason “No locks available.” indicates a machine error. The ‘lockd’ process (a part of the NFS lock manager, which supports record locking operations on NFS files) is either not running on the server or has malfunctioned. ‘lockd’ may need to be started, or killed and then restarted. In some cases, a server reboot may be needed. These actions typically require the end-user to make a request to their local IT department.

FILE-011

(error) Problem writing to file '%s'; %s.

Feedback

Description

There was an error writing data to the specified file.

What Next

Examine the reason given. The disk may have ran out of space, or there was a system or network event that interrupted the write operation.

FILE-012

(error) Directory '%s' already exists, '%s'.

Description

The directory with the specified name already exists.

What Next

Try another name for the new directory.

FILE-013

(error) Cannot open file '%s' for read.

Description

Unable to open file for read.

What Next

Check that the file exists. Check file/directory for read permissions.

FILE-014

(error) Cannot open file '%s' for write.

Description

Unable to open output file for write.

What Next

Check file/directory for write permissions.

FILE-015

(error) Basenames of original file and new file do not match. Original file: %s New file: %s

Feedback

Description

The given filenames do not have matching basenames.

What Next

This check is done to avoid user error. If this is intended, please run update_cross_probing_files command with -force option to bypass this check.

FILE-016

(error) File %s not found in the set of cross-probing files.

Description

The file being requested for update does not appear to be in the set of Cross-Probing files.

What Next

Run report_cross_probing_files to retrieve the list of files known by Cross-Probing manager.

FILE-017

(error) Unable to retreive the disk space for %s; %s.

Description

The directory cannot be created for the reason specified.

What Next

Examine the reason given. The directory may not exist or permission may be denied.

FILE-018

(error) Unable to get working directory name; %s

Description

The current working directroy name could not be returned. The most common reason is the directory you are in no longer exists.

What Next

Examine the reason given. If your working directory no longer exists, change into a valid directory using absolute path and try again.

Feedback

FILE-019

(error) Decompressing failed; %s.

Description

Unable to decompress the file for the specified reason.

What Next

Check the compressed file.

FILE-020

(error) Command '%s' not executed due to '%s' error.

Description

The command run by you is not successfully executed due to the error message printed.

What Next

Please give a valid command. for example: if there is a directory "dir1" present and if someone creates directory using command "mkdir dir1" then error reported will be "mkdir: cannot create directory ‘dir1’: File exists"

FILE-021

(info) File %s already exists. It will be overwritten.

Description

The command run by you is writing a file that already exists, so it will be overwritten.

FLIB

FLIB-1

(information) %s

Description

This is a general informational message.

What Next

No action required.

Feedback

FLIB-2

(warning) The fusion_lib library '%s' registry file error at line %d. %s

Description

The registry.dat file inside a fusion_lib library (directory) is created and updated by Library Compiler. Note that in the early phase of testing, there may be frequent incompatibility between versions. The following descriptions should help in diagnosing issues.

Bad symbolink link. Most likely the symbolic link points to a file no longer exists.

First line not recognizable. The first line is of a fixed "key" format that users must not modify.

File type not supported. The fusion_lib only supports a limited number of file.

Bad data format. Each line consists of 2 or 3 tokens (fie_type file_name checksum). This line is invalid.

File name already registered. This is most likely a bug as two files cannot have the same name in a given fusion_lib directory.

File missing or not readable. The file has been removed or is not readable.

Bad checksum in registry. The registry checksum in the first line no longer agrees with the checksum generated from the rest of the file. This means a user may have modified the registry.

What Next

If the problem is a bad symbolic link because of a moved file, update the symbolic link. In general, the fusion_lib library needs to be re-checked and saved in order to update the registry. R&D.

FLIB-3

(error) The fusion_lib library '%s' not qualified.

Description

This error message occurs after the fusion_lib checks failed either by check_fusion_lib command or internally called in create_fusion_lib or save_fusion_lib command (equivalent to check_library -logic_vs_physical). The default check is -logic_vs_physical. When it is not qualified by the default check, save_fusion_lib cannot save it as qualified fusion_lib on disk. When there is no frame file, it will print out: No physical library found.

The fusion_lib passing criteria depend on the policy specified by set_early_data_check_policy command:

1) error policy, default mode No missing physical cells reported in LIBCHK-211 and no missing logic or physical signal pins reported in LIBCHK-212.

2) tolerate policy Library data as is, and no severe errors below reported No missing logic or physical signal pins reported in LIBCHK-212.

3) repair policy: Use the same criteria as tolerate policy, and apply check_library -auto_fix

What Next

Check the reported issues in LIBCHK-xxx tables for detail and correct the library accordingly or apply auto fix.

FLIB-4

(error) Failed to save fusion library '%s': %s.

Description

This message indicates that an operation of saving the specified fusion library failed. The reason is given with the message.

What Next

This is just a summary message. Usually there will be other error message(s) before this one to indicate the actual problem. Please refer to those error messages for how to correct the issue.

FLIB-5

(error) Failed to create fusion library '%s': %s.

Description

This message indicates that an operation of creating a fusion library failed. The reason is given with the message.

What Next

Correct the problem and try again.

FLIB-6

(error) Failed to %s ECO file '%s': %s.

Feedback

Description

This message indicates that an operation of specified ECO file failed. The reason is given with the message.

What Next

Correct the problem and try again.

FLIB-7

(error) Failed to save frame '%s' for fusion library '%s'.

Description

This message indicates that saving specified frame of fusion library failed. The reason is given with the message.

What Next

Correct the problem and try again.

FLIB-8

(error) Failed to open fusion library '%s': %s.

Description

This message indicates that an operation of open the specified fusion library failed. The reason is given with the message.

What Next

Correct the problem and try again.

FLIB-9

(information) ECO file '%s' was changed: %s.

Description

This message indicates that the specified ECO file had been changed outside Library Compiler. The actual change and tool's re-action are given with the message.

What Next

Verify whether the change is expected.

Feedback

FLIB-9w

(warning) ECO file '%s' was changed: %s.

Description

This message indicates that the specified ECO file had been changed outside Library Compiler. The actual change and tool's re-action are given with the message.

What Next

Verify whether the change is expected.

FLIB-10

(error) Unable to create a temporary work directory

Description

Library Compiler is unable to create a temporary work directory to store data. If the environment variable TMPDIR is present, please make sure it points to a writable disk location which is not full. If TMPDIR is missing, Library Compiler uses /usr/tmp, please make sure /usr/tmp is writable and not full.

What Next

Fix the problem and run again.

FLIB-11

(information) The fusion_lib %s requires %d number of refresh check(s)

Description

Refresh checks are triggered because the fusion_lib has been copied or moved inappropriately. Although totally harmless, they introduce unnecessary performance overheads. The underlying cause is that some modification time stamps are changed.

When copying using "cp", be sure to specify "-a" (for archive), rather than "-R":

cp -a fusion_lib_dir /destination

When copying using "tar", preserve high-resolution time stamps using posix format.

tar --posix -cf output.tar fusion_lib_dir

Alternatively, you may wish to refresh it using open_fusion_lib & save_fusion_lib commands in Library Compiler

Feedback

FLIB-12

(error) Cannot open fusion library '%s' as it had been changed since last save. Please save it again using Library Compiler first.

Description

This message indicates that the specified fusion library had been changed since last save and cannot be opened. Here, the change means any content or time stamp change of any relavent files in the fusion library.

What Next

Save the fusion library using Library Compiler and try again.

FLIB-13

(error) Frame file using "reflib.ndm" as frame file name is NOT supported.

Description

The "reflib.ndm" is a reserved file name of directory-based ndm library. It usually resides under the ndm library directory. The frame file should be defined using the ndm library directory name.

If it's a file-based ndm file which has schema version prior to 1.200, please avoid using "reflib.ndm" as the file name.

What Next

For directory-based frame libray, please use the parent directory of reflib.ndm as the frame file name. For file-based frame library, please use a different file name as the frame file name.

FLIB-14

(warning) Fusion library '%s' created or saved with inconsistency issues waived.

Description

This message indicates that a fusion library is created or saved with missing or mismatched issues waived between logic and physical libraries. These issues are reported in the library checker in LIBCHK tables above this message line. Please refer to FLIB-3 man page for qualification criteria under each check policy.

Feedback

What Next

Investigate the reported missing or mismatched issues. If those cannot be waived for your design, please fix the library first. You may fix the issues by set_early_data_check_policy -config {repair} or explicitly use set_attribute or other utilities to fix.

FLIB-101

(information) Processing of %s NOT supported. Skipped.

Description

This information indicates a specific command or app option does NOT affect the Fusion Library creation, thus is NOT supported in LM script migration for LC.

What Next

No action required.

FLR

FLR-1

(warning) Variable '%s' cannot be changed once assigned.

Description

This variable cannot be changed once set. Please do not try to set this variable for the second time.

What Next

This particular variable cannot be changed twice. You have to exit from the shell and again run the shell and then use the new value of the variable.

FLT

FLT-002

(information) Errors preprocessing compiled filter.

Feedback

Description

This is a summary message generated after a filter expression has successfully parsed, but unsuccessfully processed because of an unknown identifier, type mismatch in a relation, or invalid operator in a relation.

What Next

Look at previous error messages to determine the problem with the filter expression. Correct the problems, and retry the operation.

FLT-003

(error) while parsing filter expression: %s\n \tat '%s'

Description

A filter expression could not be successfully parsed, typically because of a syntax error. The point in the expression that caused the failure is shown along with the remainder of the expression.

What Next

Look at the man pages for filter expression syntax, and verify that your expression conforms to the syntax. Ensure that supported relation and logical operators are in use, that the expression is constructed of a series of relations separated by logical operations, etc.

FLT-005

(error) Unknown attribute '%s'.

Description

Filters are evaluated within a context. Given the current context, an attribute which you entered is unknown.

A relation in a filter expression is very simple. For example, "area <= 2.4". In this case, the attribute is "area". If you were applying the filter to a pin collection, since "area" is not a valid pin attribute, this error would occur.

What Next

Look at the man pages for the given command, and ascertain the valid values for attributes.

Feedback

FLT-006

(error) Type mismatch between '%s' and '%s'.

Description

A relation in a your filter expression has an identifier and value with inconsistent types. The following simple rules apply:

```
Identifier              Type mismatch
        generates:              when value is:
        ------------------------------------------------
        string                  n/a - never an error
        numeric literal         string, true, false
        boolean                 numeric literal, string
```

Note some important distinctions: the boolean words TRUE and FALSE are interpreted as strings in a string relation, or as boolean in a boolean relation. Similarly, the numeric literal 2.4E-9 is interpreted as a string in a string relation, or as a number in a numeric relation.

What Next

Re-enter the filter with valid identifier/value relations.

FLT-007

(error) Invalid operator '%s' for '%s' and '%s'.

Description

A relation in a your filter expression has an identifier and value with consistent types but an invalid operator. The following simple rules apply:

Type: Invalid operators: ---------- string None. All operators ok. numeric literal =~, !~ boolean =~, !~, <, >, >=, <=

What Next

Re-enter the filter with a valid operator for the failed relation.

FRAM

FRAM-054

(warning) Technology used to create frame-view and current technology have inconsistency: %s.

Feedback

Description

The reported part of the technology are inconsistent between the reference library and the design library.

What Next

Update the library with consistent technology and try again.

GEN

GEN-1

(error) Cell '%s' instance '%s' pin '%s' has same Y coordinate as cell '%s' instance '%s' pin '%s'.

Description

Two pins of the same cell, or different cells in the same column, are found to overlap. This was probably caused by a problem in either the symbol library being used or in schematic generation. Check the identified pins in your symbol library source to see if they are pins of the same cell and if the same Y coordinate has been defined for them. If so, correct the Y coordinates, recompile the symbol library, and rerun the test. If this is not the case, report this as a bug in schematic generation.

GEN-2

(error) Pin '%s' on Cell '%s' does not lie on a grid.

GEN-3

(warning) Creating a symbol for cell '%s' of type '%s'.

Description

This warning is issued when the *gen_show_created_symbols* dc_shell variable is set to "true" and *create_schematic* can not locate the symbol template for a cell in the database or in any of the symbol libraries. In such a case, *create_schematic* automatically generates a rectangular symbol template to use in the schematic. In general, this is done by putting all the input pins on the left side of the symbol and all other pins on the right side. The size of the generated symbol can be controlled by setting the *gen_max_ports_on_symbol_side* variable to an appropriate value.

Feedback

What Next

If this warning is issued for primitive gates, that may indicate that the *symbol_library* or *search_path* variables have not been set properly. This can be resolved by (1) finding the symbol library (a file with a .sdb suffix) to be used and appending it to the *symbol_library* variable, and (2) appending its directory path to the *search_path* variable.

Libraries usually don't have symbol templates for hierarchical cells, so this warning should be ignored for such cells.

GEN-4

(error) Could not find pin: '%s', in cell: '%s' in schematic library '%s'.

GEN-5

(error) Symbol library doesn't have off-sheet connectors.

GEN-6

(warning) Symbol exceeds sheet size.

Description

This warning is issued when one of the symbol templates *create_schematic* creates exceeds the size of the sheet being used. This may be caused by either the sheet being too small or there being too many pins on the symbol.

This message is only issued for symbols that have so many pins that *create_schematic* creates a smaller square symbol with all the pins equally distributed along the four sides, and even then this symbol exceeds the sheet size.

What Next

If this is of concern, use a larger sheet size. Since *create_schematic* will automatically create the smallest symbol possible for the given number of ports when this message is issued, the only way to make the symbol fit the sheet is to use a larger sheet.

GEN-7

(warning) Maximum ports on symbol side limit of '%d' exceeded.

Feedback

GEN-8

(warning) Can't rename off-sheet connector of net '%s'\n to the name of its port '%s'\n because net '%s' already exists.

GEN-10

(warning) Couldn't find all the port symbols in the generic symbol library.

GEN-11

(error) Couldn't find pin name '%s' in ripper symbol '%s'.

GEN-12

(error) Couldn't find a ripper symbol for creating a bussed schematic.

GEN-13

(error) Annotator '%s' has an invalid format specification '%s'.

GEN-14

(error) An unnamed annotator has an invalid format specification '%s'.

GEN-15

(error) Annotator '%s' has more than %d '%%s' specifications \n \tin the format string.

GEN-16

(error) An unnamed annotator has more than %d '%%s' \n \tspecifications in the format string.

GEN-17

(error) Annotator '%s' has an invalid expression '%s'.

Feedback

GEN-18

(error) An unnamed annotator has an invalid expression '%s'.

GEN-19

(warning) The symbol for cell '%s' has a pin off the route grid.\n \tYou may be mixing symbol libraries with different route grids.

Description

This warning is issued when one of the schematic symbols is found to have a pin that is located outside the route grid being used by *create_schematic*, i.e., the pin is somewhere in the middle of the square region defined by the four points around it that represent the intersection of vertical and horizontal grids instead of being on one of the edges or corners. This indicates that the schematic may contain symbols from more than one symbol library and that these libraries specify different route grids. In such a case, *create_schematic* picks up the route grid specified in the first symbol library it runs into, and uses that route grid in the schematic. Any symbols coming from libraries whose route grids do not match the one being used by *create_schematic* are not guaranteed to have their pins aligned with the route grid.

What Next

If this is a problem in transferring the schematic to some external environment, try using symbol libraries with the same route grid. If this is not possible, try modifying the route grids in your symbol libraries to match each other. This is done by editing the .slib file and changing the argument to the *set_route_grid()* specification and then recompiling that library with the *read_lib* command.

GEN-20

(error) One of the pins or port busses is corrupted.

Description

This error is issued when one of the design ports or pins is found to have a corrupt bus structure. This can happen sometimes because of inconsistent bus creation by different tools in the design. In such a case, the port or pin that is found to have a corrupt bus structure will be drawn unbussed in the schematic, i.e. its bus will be ignored by *create_schematic*.

What Next

If there are no other problems with the tool run, this message should be ignored as *create_schematic* automatically ignores the bus objects responsible for corruption.

Feedback

GEN-21

(error) Cell %s's pin %s is on wrong side.

GEN-22

(error) Net %s connects pins of different widths.

GEN-23

(warning) The netlist contains bus-to-bus connections. Any \n\t nets involved in inter-bus connections will be \n\t displayed as disconnected in the no-ripper schematic.

GEN-24

(error) Could not find the type mapper symbol in the \n generic symbol library. The generic symbol library \n is probably old - Please use a new library and \n recreate the schematic.

GEN-25

(warning) All cells are power/ground or have no connection.

Description

Cells in the current design are all power cells or all ground cells. Or the cells have no pins.

GEN-26

(error) member '%d not found in bus '%s' . Only following members present : '%s'. The design is corrupted.

GEN-27

(warning) Creating a very large schematic. \n \tIt is approximately %d wide and %d tall. \n \tMust skip the 'improve' algorithm due to insufficient memory.

Description

You receive this warning when you are trying to create a schematic for a very large design, but there is not sufficient memory available to perform the "improve" algorithm.

Feedback

What Next

You have available three courses of action:

- You can let the schematic creation continue, with the possibility that it will succeed, if there is enough memory.
- You can monitor the performance, using a UNIX utility such as *top*, to see if you are close to running out of address space.
- You can send an interrupt to the application, which terminates the schematic creation at the next check point in the algorithm.

Because large schematics are difficult to work with graphically, consider whether you really want your schematic to be so large. If you have flattened your design, going back to an unflattened design might be more workable and require less address space.

If it is imperative that you produce the schematic, rerun your application using the 64-bit version (if it is available to you), which has a memory address space limit exceeding 4 gigabytes. The process should eventually succeed, providing you have enough swap space on your machine.

GEN-28

(warning) Creating a schematic with an extreme number of sheets. \n \tThe schematic being created has %d sheets. \n \tAborting attempt to create schematic.

Description

You receive this warning because you are trying to create a schematic that has too many sheets, making it impractical to use. The process is terminated.

What Next

You can avoid the issue by choosing a larger sheet size, which will result in fewer sheets: -size A is the smallest sheet size, -size B is larger, and so on, up to -size infinite, which is always just one sheet. For more information about sheet sizes, see the man page for the *create_schematic* command.

GUI

GUI-001

(Error) %s%s '%s' not found.

Feedback

Description

The specified object does not exist.

GUI-002

(Error) %s%s name is empty.

Description

The name for the relevant object type [toolbar|menu|window type|hotkey,..] is empty.

GUI-003

(Error) %sValid %s name cannot consist only of ampersands.

Description

Valid name for specified object type cannot consist only of ampersands. The object type can be a menu, toolbar, window type, hotkey, etc.

GUI-004

(Error) %sTrailing '->' not allowed in menu name '%s'.

Description

Trailing '->' not allow in specified menu name.

GUI-005

(Warning) %sHotkey '%s' is reserved. Please use another hotkey.

Description

Specified hotkey is reserved by application. Please use another hotkey.

GUI-006

(Warning) %sHotkey '%s' is not supported.

Description

Specified hotkey is not supported. Please check spelling or use another hotkey. Shift modifier only work with letter or function hotkey. Thus, "Ctrl+Shift+4" is not supported.

Feedback

GUI-007

(Error) %sHotkey '%s' is invalid. Please check spelling.

Description

Specified hotkey is invalid. Please check spelling.

GUI-008

(Warning) %sMenu item '%s' already exist for %s '%s'.

Description

Specified menu item already exist for specified window type.

GUI-009

(Warning) %sHotkey '%s' will not be set for menu '%s'. Hotkey is in use.

Description

Specified hotkey will not be set for specified menu. It is already in use by another menu item or tcl command.

GUI-010

(Error) %sAnchor offset must be nonzero.

Description

Anchor offset value for specified command must be either a positive or negative integer.

GUI-012

(Warning) %s: Specified dock side '%s' is invalid. Top docking side will be used.

Description

Specified dock side is invalid. Valid values include left|top|right|bottom.

GUI-014

(Error) %s: menu item '%s' not found for window type '%s'.

Feedback

Description

Specified menu item not found for specified window type or default window type if not specified.

GUI-015

(Warning) %s: hotkey '%s' is already set for tcl command '%s'.

Description

Specified hotkey is already set for an existing tcl command.

GUI-016

(Warning) %s: hotkey not set, hotkey '%s' is already set for menu item '%s'.

Description

Specified hotkey has already been used by a menu item. Use -replace option to force hotkey to be set.

GUI-017

(Warning) %s: hotkey '%s' is reserved by system function '%s'.

Description

Specified hotkey has already been used by an internal system function.

GUI-018

(Error) None of the supported browsers %s are in the path

Description

This error message occurs when the application can not find a browser from the list of supported browsers in your environment.

What Next

Please correct the PATH to get one of the supported browsers. Please contact your system administrator to get the location of the browsers.

See Also

- gui_online_browser

Feedback

GUI-019

(Error) The default browser %s of your choice is not supported

Description

The current browser assigned to the variable gui_online_browser is not supported by your online help system.

What Next

Please assign a browser from the the following list %s to the variable gui_online_browser and try to bring up the helpsystem.

See Also

- gui_online_browser

GUI-020

(Info) No %s installation specified with variable %s

Description

The application extension to ICC specified depends on the variable to point to the installation of that tool. The environment variable specified was not set so this extension to ICC will not be loaded.

What Next

If you would like to load the ICC extension for that tool, then please setup the variable to point to the appropriate tool installation before running the ICC GUI.

GUI-021

(Warning) Extension %s not loaded because extension loading is disabled

Description

The loading of application extensions has been disabled. Therefore the specified extension will not be loaded.

What Next

Re-enable extension loading if you want to have extensions loaded.

Feedback

GUI-022

(Error) %s installation directory specified in variable %s is not a directory. Extension can not be loaded from %s

Description

The installation directory for the extension was not a directory, so the extension could not be loaded.

What Next

Correct the setting of the variable to specify the path to the installation of the tool and re-start the ICC GUI to get the extension loaded.

GUI-023

(Warning) The %s installation specified does not contain an ICC extension setup file %s

Description

The installation directory for the extension did not contain the expected ICC extension, so the extension could not be loaded.

What Next

Correct the setting of the variable to specify the path to the installation of the tool and re-run ICC to get the extension loaded. If this version of the application does not support the ICC extension you may need to update to a newer version of this application.

GUI-024

(Info) Loaded %s extension from %s

Description

This message indicates that the ICC extension for the specified application was automatically loaded. The loading of the extension is controlled by the specification of the application installation for this application via a variable.

What Next

There are no additional steps required to use this extension.

GUI-025

(Error) Error sourcing %s extension setup file %s. %s : error_info is: %s

Feedback

Description

There was an error detected when loading the ICC extension for the specified application. Please contact the support staff for the application to get assistance in correcting the problem.

What Next

Please ensure that the application installation specified is correct. If there is an error in the extension then please contact the support staff for that application to get a fix for their ICC extension.

GUI-026

(Info) Visibility is turned %s for cells and cell contents because the task is set to %s

Description

The visibility options for cells and cell contents are turned OFF automatically when the task is set to Design Planning or turned ON automatically when the task is set to Block Implementation or All.

What Next

You can set the preference setVisibilityByTask to turn on or turn off this behavior. For example, to turn off this behavior, use the following command:

gui_set_pref_value -category layout -key setVisibilityByTask -value false

By default, this preference is set to true.

GUI-027

(Error) All menu items may not be deleted from a window type menu

Description

All menu items may be deleted from a menu using the menu root name but not from a window type menu.

What Next

You can use the -root option to specify a menu root.

GUI-028

(Error) A menu root named %s was not found.

Feedback

Description

A menu root with the given name could not be found.

GUI-029

(Error) A menu root named %s was not found.

Description

A menu root with the given name could not be found.

GUI-030

(Error) Specified view, %s, does not exist

Description

A view with the given name does not exist.

GUI-031

(Error) Specified command, %s, does not exist

Description

The given name for the command option is invalid.

GUI-032

(Error) Specified task, %s, does not exist

Description

The given name for the task option is invalid.

GUI-033

(Error) Task item root: %s not found.

What Next

Check and correct the option value of the -item_root option.

Feedback

GUI-034

(Warning) Layers %s have no preferred routing direction.

Description

Congestion data from those layers which have no preferred routing direction will not be displayed in the map.

What Next

If you would like to see the congestion data from those layers, then please setup the preferred routing direction on those layers.

GUI-035

(Warning) Collection size limit reached

Description

The number of objects in the collection created by the gui command has exceeded the size limit.

What Next

Check the command is correct and if necessary increase the size limit.

GUI-036

(Warning) not all objects could be represented as a collection

Description

Some of the selected or highlighted objects could not be returned as they are not representable in a collection.

What Next

Check the objects are correct and if necessary request gui collection support for the missing objects.

GUI-037

(Error) Given color index is greater than max index: %d

Description

The given color index argument is too large.

Feedback

What Next

Please ensure the the given index is no greater than the maximum color index allowed for the current or given Palette.

GUI-038

(Error) Given color name (%s) is not legal.

Description

The given color name is not a legal color name.

What Next

Please ensure the the given color name is a legal name for the current or given Palette.

GUI-039

(Error) %s%s value '%s' is invalid.

Description

Specified filter value is invalid.

GUI-040

(Warning) Anchor toolbar '%s' not found.

Description

Specified name for an anchor toolbar is invalid.

GUI-041

(Warning) Anchor toolbar '%s' not found.

Description

Specified name for an anchor toolbar is invalid.

GUI-042

(Error) Duplicate toolbar item: %s.

Feedback

What Next

Check and correct the menu item name.

GUI-043

(Error) The file %s could not be opened for write.

Description

There was an error while opening the given file for writing.

What Next

Please check permissions for the file path.

GUI-044

(Error) Specified task, %s, does not exist

Description

The given name for the task option is invalid.

GUI-045

(Error) Specified file does not exist: %s.

Description

The given file could not be found or read.

GUI-046

(Error) No tip files found in the given directory %s.

Description

The given directory could not be found or read, or there were no files found with ".html" file extension in the given directory.

GUI-047

(Error) The given file %s already exists.

Feedback

Description

The given output file already exists. Please move or delete the existing file.

GUI-048

(Error) There was an error wrhile writing to %s.

Description

There was an error while writing to the given output file and not all of the document could be written.

GUI-049

(Error) Preset '%s' not found for category '%s'.

Description

Specified preset not found for specified category.

GUI-050

(Error) Performance monitor could not be found.

Description

Performance monitor program executable files could not be found in the Synopsys tool installation.

GUI-051

(Warning) 3D View requires X Server to have %s extension.

Description

3D View uses an OpenGL renderer which requires your X Server to have the GLX and RENDER extensions. Typically this is caused by using a vncserver which is old or not configured to have the GLX or RENDER extensions.

What Next

You can open a shell window in your X Server and run the command xdpyinfo. The list of extensions is listed near the top. You will need to see the following: GLX RENDER

Feedback

GUI-052

(Warning) 3D View requires a valid DISPLAY environment variable.

Description

3D View uses an OpenGL renderer which requires a connection to a valid X Server via the DISPLAY environment variable.

What Next

You can open a shell window in your X Server and run a simple X application like xclock. You can open a shell window in your X Server and run the command xdpyinfo. The list of extensions is listed near the top. You will need to see the following: GLX RENDER

GUI-053

(Warning) 3D View requires a network connection to a X Server.

Description

3D View uses an OpenGL renderer which requires a connection to a valid X Server via the DISPLAY environment variable.

What Next

You can open a shell window in your X Server and run a simple X application like xclock. You can open a shell window in your X Server and run the command xdpyinfo. The list of extensions is listed near the top. You will need to see the following: GLX RENDER

GUI-054

(Warning) 3D View Could not find a compatible X Visual in the X Server. The X Server needs to support 32 bit planes.

Description

3D View requires the X Server to support 32 bit planes. OpenGL requests 24 bit planes PLUS 8 bits of Alpha. If the output of xdpyinfo for the X Server in question does not have at least one entry contianing "32 planes", then the X Server is not supported. That entry must also state "TrueColor

What Next

If the output of xdpyinfo doesn't contain all these lines, then it is incompatible with the OpenGL based 3D view. GLX RENDER 32 planes

Here is an example of an X Visual output by xdpyinfo that is compatible with the OpenGL based 3D view:

default visual id: 0x21 visual: visual id: 0x21 class: TrueColor depth: 24 planes available colormap entries: 256 per subfield red, green, blue masks: 0xff0000, 0xff00, 0xff significant bits in color specification: 8 bits

The output must contain at least one other entry that can support 32 planes:

visual: visual id: 0x47 class: TrueColor depth: 32 planes available colormap entries: 256 per subfield red, green, blue masks: 0xff0000, 0xff00, 0xff significant bits in color specification: 8 bits

---

GUI-055

(Info) 3D View will not run with the -batch option (offscreen mode).

Description

3D View uses an OpenGL renderer which currently does not work in offscreen mode (-batch option).

What Next

Remove the -batch option when running fc_shell or icc2_shell

GUI-056

(Warning) 3D View is missing OpenGL support library: libxcb-glx.so. Check your platform for QSC compliance.

Description

3D View uses an OpenGL renderer which is only supported on platforms compatible with CentOS 7 or greater and Suse 12 or greater.

What Next

Verify that you are running fc_shell or icc2_shell on a QSC-Q platform.

GUI-057

(Warning) 3D View requires the Synopsys version of libGL.so.

Feedback

Description

3D View uses an OpenGL renderer which is built by Synopsys specifically for this product. This error indicates the application is loading a version of libGL.so that wasn't supplied by Synopsys.

What Next

Make sure you are using the version of libGL.so supplied by Synopsys in the product installation. Make sure you don't have a LD_LIBRARY_PATH setting that finds your OS-installed libGL.so

---

GUI-058

(Warning) Given color has been matched to index: %d.

Description

The given color has been matched to index in a current palette.

What Next

Please ensure the the given color name is a legal name for the current or given Palette.

GUI-059

(Warning) View "%s" is being disabled. See previous "3D View" warnings.

Description

3D Views are disabled when the runtime environemnt won't support a particular X Server, or an installation environemnt for OpenGL libraries isn't set up properly according to QSC-S

What Next

Read the "3D View" warnings prior to the message and take the suggested actions.

GUI-060

(Warning) 3D View requires server glx version 1.4.

Description

3D View uses VKT9 which requires a glx version of 1.4.

Feedback

What Next

You can open a shell window in your X Server and run glxinfo (mesa utilities) to determine current version.

GUI-061

(Warning) The total number of visible errors exceed the set maximum for displayed errors.

Description

The maximum errors that are displayed in the layout are set using a preference key and can be changed using the same.

What Next

You can use the command "gui_set_pref_value -category {Globals} -key {gui_error_browser_show_all_max} -value {val}" where val is the number of errors to be displayed in the layout and reload the database. However, increasing this value above the recommended limit (200000) might result in the application displaying slow downs depending on the available computational resources.

GUI-062

(Warning) The application can display slow downs since the gui_error_browser_show_all_max value is greater than the recommended value (%d).

Description

Since a large number of errors are now being loaded into the error browser, the application can display a slow down depending upon the computational resources available.

What Next

Reset the value to the default value.

GUI-063

(Warning) Since the desired value of the preference is out of bounds (minimum %s, maximum %s), it is being reset to the nearest bound.

Description

If the desired value is less than the minimum value of the preference, then the value is set equal to the minimum value. On the contrary, if it is greater than the maximum value of the preference, then the value is set equal to the maximum value.

Feedback

GUI-064

(Warning) Initialization of Tk can prevent use of other application features (See man page for details)

Description

If Tk is initialized then the GUI can no longer support close and reopen of display as Tk does not allow this feature.

That means user cannot call 'gui_stop -close' (to close gui) and then 'gui_start' (to restart gui) for example when switching from offscreen display to normal X11 display.

It also means that save_checkpoint command cannot be used, as that command can only be run when GUI is closed and restore of the closed checkpoint, with the saved Tk state would fail.

GUI-065

(Warning) Failed to find application's associated terminal

Description

The gui will try to find the terminal associated with the application on gui start but may fail depending on the invocation method or terminal X11 support.

If this functionality is needed, and message is output, then please report so specific environment can be investigated.

GUI-998

(Warning) %s

Description

A warning was issued for a non-fatal error when running the command.

What Next

If the error indicates a problem then fix it and re-run the command. If the error is benign then ignore the error.

GUI-999

(Error) %s

Feedback

Description

An error was found when running the command as desribed in the error message.

What Next

Fix the error and re-run the command.

HCEXT

HCEXT-001

(Error) For generated clock: %s, either master clock does not reach the boundary of HyperScale block %s or there are parallel clock source paths (with at least one of them going through sequential logic) from master clock to the boundary pin %s.

Description

If the master clock of a generated clock doesnt reach the boundary of a HyperScale block, there is no way to define the generated clock at block level. In order to fix this, user needs to create a new auxiliary generated clock for each cross-boundary generated clock such that the boundary pin falls in the direct clock network of this new gclock. Now the original generated clock can be defined w.r.t this new generated clock and the boundary pin should be used as the master pin of the original gclock.

Also if there are multiple parallel paths (with at least one of them sequential) from the master source to a block boundary pin, the source latency of generated clock cannot be captured at block level. It is recommended that a unique generated clock is defined for the driver pin of the last sequential element before the block boundary for each of these paths . Then cross-boundary generated clocks can be safely defined w.r.t one or more of these generated clocks.

HCEXT-002

(Error) For generated clock: %s, the source network of this generated clock leaves and reenters the HyperScale block %s too many times.

Description

This error is issued when the source network of generated clock exits the block more than once. Essentially one re-entrance is acceptable but more than one re-entrance is prohibited. User is asked to fix this by creating auxilary generated clocks.

Feedback

HCEXT-003

(Error) For generated clock: %s, master clock does not reach the generated clock source pin %s.

Description

If there are other generated clocks defined between the master clock and the generated clock, the master clock is blocked and cannot reach the source of the generated clock, the waveform cannot be derived from the master clock at block level. It is recommanded that the generated clock use its immediate upstream clock as its master clock.

HCEXT-004

(Error) For generated clock %s inside HyperScale block %s erroneous situations (UITE-461, PTE-075, etc. messages in log file) are encountered.

Description

When a generated clock definition causes any of the following error/warning messages: UITE-461, PTE-004, PTE-023, PTE-024, PTE-025, PTE-075, it implies that there is a problem in definition of the generated clock so the behaviour of the clock would not be as expected. Therefore user needs to fix these erronous situations before extracting consistent block constraints.

What Next

If you are running HyperScale Constraint Extractor flow, please modify the generated clock definition at flat level such that erroneous message are eliminated.

HCEXT-005

(Warning) Definition of %s uses hierarchical pin %s inside HyperScale block: %s, Please move the constraint to the leaf driver or leaf load of the net.

Description

This message is issued when there is a constraint defined on a hierarchical pin inside HyperScale block. Because HyperScale model is a flattened block when instantiated at a top level, these constraints on hierarchical pins will be dropped if used for a top-level run. You need to avoid defining constraints on hierarchical pins or use "*write_script -leaf_pin_transfer*" for moving these constraints to the leaf load/driver pins. Also, it is important to note that this warning is only printed for those hierarchical pins that have leaf load/driver pins.

Feedback

HCEXT-006

(Information) Instance

Description

This message indicates the reference instance of a certain block used for constraint extraction. If the block has multiple instances to be characterized in the same MIM group, the internal constraints will be extracted from the reference instance only.

The reference instance will be the first instance specified by the "*-instances*" option in *characterize_context* command. If "-instances" is not specified, the reference instance will be the first one sorted by name alphabetically. If the MIM instances in the same group are not all merge-able, the reference instance will be chosen from the largest merge-able instance set with the same rules.

HCEXT-007

(Information) Instance "%s" is the reference instance of block "%s" and the merged context will be written.

Description

When using *write_context* command in the HyperScale flow, if the instance is not re-characterized by *characterize_context* command, the merged context including this instance will be written.

What Next

Please make sure you have characterized the right instance that you want to write context.

HCEXT-010

(Warning) Generated clock: %s with source(s) inside block: %s, is a multi-source generated clock. Source latency for this generated clock will be set to 0 by use of explicit set_clock_latency in the block constraints.

Description

PrimeTime assumes source latency of 0 for multi-source generated clocks. To guarantee consistency of block-level constraints, source latency for such generated clocks are explicity set to 0.

Feedback

HCEXT-011

(Warning) SI and Noise constraints are not yet fully supported. These constraints may have to be added manually.

Description

As of 2012.06, the supported SI and Noise constraints include *set_si_delay_analysis*, *set_si_aggressor_exclusion* and *set_si_noise_analysis*; other SI and Noise constraints are not supported. Examples of such constraints are *set_noise_margin*, *set_noise_derate*, etc. Until support for these constraints are added, the user needs to manually apply them to the block runs.

HCEXT-012

(Warning) For generated clock:%s, %s. Master pin will be moved to %s.

Description

This message is printed when the master pin of a generated clock is moved by the HyperScale Constraint Extractor. It might be needed to move the master pin of a generated clock because of one or both of the following reasons: First, if the master pin of generated clock is outside the block(i.e. a cross-boundary generated clock), master pin in this case needs to be moved to be able to define the generated clock at block level. Second, if the generated clock is re-entrant to the block. Master pin in this case needs to be moved to garauntee that the generated clock source network doesnt get broken at block level.

HCEXT-100

(error) %s.

Description

This message is issued when there are errors in hyperscale configuration. Either block/instance names don't match within current design, or the instances of multi-instance block are not merge-able. Please check set_hier_config. If block name is not valid, constraint extraction for that block will be skipped. If instance name is not a valid instance of the corresponding valid block, constraint extraction will ignore the instance for that block, and will extract constraints for the remaining valid instances in the group. If all instances in the group referred by '-instance' are invalid, constraint extraction will be skipped for that block. If both block and instance names are correct, but instances are not merge-able, by default in strict mode, no constraint will be extracted for that block; in normal mode, one reference instance in the group will be chosen for constraint extraction.

Feedback

What Next

Check set_hier_config

HCEXT-101

(Warning) %s.

Description

Generic warning message.

HCEXT-102

(Information) %s.

Description

Generic information message.

HCEXT-103

(Warning) Virtual clock '%s' is defined to lanch or capture timing pathes from/to the block '%s'.

Description

This message is printed when a non-generated clock is defined right on a hierarchical output pin of the target block. The HyperScale Constraint Extractor defines a virtual clock to lanch or capture timing pathes from/to the block.

What Next

It is recommanded to define such clocks on downstream leaf pins outside the block, not on the hierarchical output pins.

HIER

HIER-001

(information) %s.

Description

Generic informational message.

Feedback

What Next

No action is required.

HIER-002

(warning) %s.

Description

Generic warning message.

What Next

No action is required.

HIER-003

(Error) %s is not an abstracted hierarchical instance.

Description

The instance specified in the *report_clock -map* command is not hierarchical or abstracted.

See Also

- report_clock

HIER-004

(error) There are unresolved clocks %s.

Description

In hierarchical timing analysis, clocks from block level have to be mapped to clocks from the top level. If mapping fails for any clock, this error is issued. To view the details of the failed clock mapping, see the clock_mapping sections in the report created with the *report_constraints* command.

What Next

View the details of the failed clock mapping created with the *report_constraints* command.

HIER-005

(error) The option '%s' requires top-level HyperScale analysis.

Feedback

Description

The execution of the command has stopped because the shown command option requires data only available at the top level of the HyperScale analysis.

What Next

Check command options and the analysis settings.

See Also

- report_global_timing
- report_analysis_coverage

HIER-007

(information) Design is successfully linked and the program is setup for hierarchical analysis.

Description

When the *hyperscale_enable_analysis* variable is set to *true* and the hierarchical data configuration setup with the *set_hyperscale_config* command is successfully linked, PrimeTime performs the necessary setup for the automated hierarchical analysis flow.

In this flow, either due to incompatibilities of the feature with the hierarchical analysis flow or as a temporary limitation of the hierarchical analysis flow, the following set of commands are disabled:

```
create_ilm
    identify_interface_logic
    get_ilm_objects
    write_ilm_netlist
    write_ilm_parasitics
    write_ilm_script
    write_ilm_sdf
    create_si_context
    write_arrival_annotations
    characterize_context
    remove_context
    report_context
    write_context
```

The CMD-080 error message is issued if any of these commands are encountered.

What Next

This is an informational message.

Feedback

HIER-008

(Error) Unable to read the database file, %s, due to file format errors.

Description

The database file contains information from a previous run meant to improve the speed and capacity of subsequent PrimeTime runs. If the file has been corrupted, PrimeTime cannot correctly parse it.

What Next

The database file must be manually deleted and the information stored must be regenerated through another PrimeTime run.

HIER-009

(Warning) HyperScale data in %s has been generated using an incompatible version of PrimeTime

Description

HyperScale generated data can only be used by a HyperScale enabled run using a later compatible PrimeTime version.

What Next

Use compatible PrimeTime versions. Regenerate the HyperScale data using the same PrimeTime version used in the current run or use the same PrimeTime version in the current run that was used to generate the HyperScale data.

HIER-010

(warning) Database '%s' of block '%s' is dirty.

Description

This message indicate that the following mismatches have occurred during the block level timing analysis:

```
a. High level hierarchy has pins the low level hierarchy does not have
        b. Bus width mismatch between hierarchies
        c. Pin direction mismatch between hierarchies
```

These problems have to be fixed at the block level.

What Next

Fix these problems at the block level.

Feedback

HIER-012

(information) %s %s.

Description

Generic message.

What Next

This is an informational message.

HIER-013

(Error) %s %s.

Description

This is a generic message with problem as noted.

What Next

If you are running a hierarchical flow, you need to adjust the constraints to be compatible; otherwise, no action is required.

HIER-014

(information) Paths through hierarchical pin '%s' have partially satisfied exception (%s).

Description

In the F-2010.06 release, some exceptions that cross from chip level into hierarchical blocks have been ignored. The timing window at the indicated input port of a hierarchical block is captured conservatively for block level analysis.

What Next

This is only an informational message. No action is required.

See Also

- report_exceptions
- set_false_path
- set_multicycle_path
- set_max_delay

Feedback

- set_min_delay
- reset_path

HIER-015

(Warning) Object '%s' has been skipped for this operation as it is within the boundary of a HyperScale instance, or is marked as "dont_touch".

See Also

- set_dont_touch

HIER-016

(Warning) report_hyperscale %s provides useful information only when invoked after update_timing in a HyperScale block level flow.

HS

HS-001

(information) Loading block timing data for block instance %s.

Description

Updating progress informational message. No action required.

HS-002

(warning) ECO-driven context is generated for block instance %s.

Description

Hyperscale ECO flow warning message. No action required.

HS-003

(error) %s is not an proper HyperScale instance.

Description

The instance specified in is not HyperScale block.

Feedback

What Next

set_hier_config(2).

HS-004

(error) There are unresolved clocks %s.

Description

In HyperScale analysis, clocks from block level have to be mapped to clocks defined at top level in order to properly interpret the timing data and constraints. If this mapping fails for any clock, an error is issued. To see the details of failed clock mapping, please see clock_mapping sections in the report from *report_constraint*.

What Next

report_constraint(2).

HS-005

(error) %s.

Description

This is a severe error that can prevent HyperScale flow from executing properly.

What Next

Check to make sure all the configurations setup for the HyperScale analysi is correct.

For example, you must have at least one valid configuration using *set_hier_config* with neither the *-parent* nor the *-block* options, so it properly configures the storage to write analysis data generated for the current design itself.

See Also

- set_hier_config
- hier_enable_analysis

HS-006

(warning) %s, no data will be loaded from the directory.

Feedback

Description

This warning message is issued when the noted directory cannot be accessed to read necessary data for HyperScale analysis flow.

This message may only be ignored if it is encounted during the initial block level runs. Because the HyperScale context data have not been generated from a prior top level run. In that situation, PrimeTime HyperScale flow will just use the budgetory constraints user provided for the block IO boundary to do the block level run.

What Next

Please check whether the directory name is correctly specified, and ensure the directory exists with proper read permission, etc.

HS-007

(information) Design is successfully linked and set up for HyperScale analysis.

Description

When the *hier_enable_analysis* variable is set to true and the HyperScale data configuration set up with the *set_hier_config* command is successfully linked, the tool prepares for the automated HyperScale analysis flow.

In the HyperScale flow, the following commands are disabled. Using any of them triggers a CMD-080 error message.

```
write_arrival_annotations
    characterize_context
    remove_context
    report_context
    write_context
    write_script
    write_sdc
```

What Next

Please refer to documentation to understand guidelines and recommendations for proper use of HyperScale analysis.

HS-008

(Error) Unable to read %s for block %s, due to file format errors.

Feedback

Description

The HyperScale database contains information saved from a previous run meant to improve the performance and capacity of subsequent PrimeTime runs. If the data has been corrupted and PrimeTime cannot correctly load it, an error is issued.

What Next

The database needs to be manually deleted and the information will needs to be regenerated through the proper PrimeTime HyperScale run.

HS-009

(Error) The database %s configured for block %s was not generated with the expected version of PrimeTime, %s. It was generated using PrimeTime version %s.

Description

The database file contains information from a previous run meant to improve the performance and capacity of subsequent PrimeTime runs. It is required that the database be created with the same PrimeTime version, otherwise, PrimeTime cannot correctly load it.

What Next

The database need to be manually deleted and the information stored need to be regenerated through proper PrimeTime HyperScale run using the current version. An alternative would be to re-run with the PrimeTime version that was used to generate the database, if available.

HS-010

(warning) Database '%s' of block '%s' contains dirty data.

Description

This message indicate that there are following mismatches during the block level timing analysis: a. High level hierarchy has pins the low level hierarchy does not have b. Bus width mismatch between hierarchies c. Pin direction mismatch between hierarchies These problems have to be fixed at block level.

What Next

Fix these problems at block level.

Feedback

HS-011

(warning) Option '%s' requires HyperScale analysis flow.

Description

The command option requires HyperScale analysis flow to be switched on.

What Next

Check command options for correctness.

HS-012

(information) Computing path specific latency for HyperScale block.

Description

information message

HS-013

(Error) %s %s.

Description

This is a generic message for the problem noted.

What Next

If you are running HyperScale flow, please adjust the setup and constraints to be compatible; otherwise, no actions required.

HS-014

(information) Paths through hierarchical pin '%s' have partially satisfied exception (%s).

Description

For the D2010.06 release, some exceptions that cross from chip level into hierarchical blocks have been ignored. Timing window at the indicated input port of a hierarchical block is captured conservatively for block level analysis.

What Next

This is an informational message only. No action is required on your part.

Feedback

See Also

- report_exceptions
- set_false_path
- set_multicycle_path
- set_max_delay
- set_min_delay
- reset_path

HS-015

(warning) %s '%s' is changed by the command%s and it is inside the boundary of a HyperScale block.

Description

The object is changed by the command triggering the warning because the object (or instance of the object in the case of a library object) is found inside a HyperScale block instance. This may result in potential accuracy degradation.

What Next

All commands that alter the timing or structure of HyperScale instances should be performed during the creation of that instance.

See Also

- report_hier_analysis
- hier_enable_analysis

HS-016

(Warning) Victim net '%s' has parasitic mismatch for one or more of its aggressor nets between top level and block level analysis.

See Also

- report_annotated_parasitics

Feedback

HS-017

(error) Clock '%s' referred in the context for instance '%s' at pin '%s' has no equivalent clock found in the context for instance '%s' of the same block.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified. In order to automatically merge the context for two HyperScale block instances of the same block, it is required that the instances must have exact matching clocking scheme. Otherwise, their context data cannot be merged together and analysis must be done seperately to cover each clocking scheme. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the first instance noted.

What Next

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- set_hier_config

HS-018

(information) %d HyperScale block instances are excluded.

Description

This information message shows the number of HyperScale blocks that are excluded when generating the report. No action required.

Feedback

HS-019

(warning) Failed to find a clock that matches top level virtual clock %s, and a virtual clock %s with period %f is created.

Description

In hierarchical timing analysis, when a top level virtual clock does not have a matched block level clock, but this clock is referred in context (e.g., set_input_delay), PrimeTime automatically creates a virtual clock. This can ensure context referring to this clock can be successfully applied at block level.

HS-020

(error) Hierarchy %s has derates on both libcells and itself.

Description

When the old precedence rules (i.e., derates of lib cells have higher precedence than derates of design, and lower precedence than derates of hierarchical cells) are used, a hierarchy cell has a timing derate that is set directly or inherited, and library cells also have timing derates, this error is issued. A hierarchical cell at top level becomes a design at block level, and if the priority of library cell is sandwiched between hierarchical cell and design, a cell in the hierarchical cell has different timing derates at block level and top level. That is why this error is issued. The correct way is to use the new precedence rules by setting *timing_derate_precedence_compatibility* to TRUE.

What Next

Set *timing_derate_precedence_compatibility* to TRUE.

HS-021

(warning) A clock %s wth period %f that is internal at block level is created.

Description

In hierarchical timing analysis, when none of the sources of a block level clock is in interface, and this clock is referred by constraints (e.g., input delay of side pins), this clock will be created as a virtual clock by PrimeTime at top level, and its name is instance_name/clock_name in order to uniquify it.

HS-022

(information) Parasitics reading is skipped in the mode of extracting block constraints.

Feedback

Description

In the constraints extraction mode, parasitics reading is skipped since parasitics does not affect constraints.

HS-023

(Information) Parasitics of HyperScale instance '%s' was already automatically loaded.

Description

Parasitics of HyperScale instances are automatically read by PrimeTime when these instances are instantiated at top level, and user-specified parasitics reading of these instances is automatically skipped. Note that if the *-path* option in *read_parasitics* includes multiple instances among which some are HyperScale instances and the others are not, the parasitics reading for those non-HyperScale instances are not skipped.

See Also

- read_parasitics

HS-024

(error) %s is not a HyperScale block.

Description

Generic message. The instance specified is not a HyperScale block but this command requires it to be a HyperScale block.

HS-025

(Information) Instance '%s' is merged with instance '%s'.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified.

See Also

- set_hier_config

Feedback

HS-026

(error) Case value or set disable timing on pin '%s' in the context for instance '%s' is different from the case value or set disablt timing on pin '%s' in the context for instance '%s' of the same block.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified. In order to automatically merge the context for two HyperScale block instances of the same block, it is required that the instances must have exact matching case values. Otherwise, their context data cannot be merged together and analysis must be done seperately. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the first instance noted.

What Next

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- set_hier_config

HS-027

(warning) Case value or set disable timing on pin '%s' in the context for instance '%s' is different from the case value or set disable timing on pin '%s' in the context for instance '%s' of the same block.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all

Feedback

the instantiation specified. When different case value or disable timing setting found on the same port of different instances, merged context will have the no case value and no disable timing.

What Next

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- set_hier_config

HS-028

(information) Instance '%s' of reference '%s' is the representative instance for scenario '%s' in HyperScale constraint extraction.

Description

When HyperScale block constraints are extracted, multiple instances of same block may share the same scenario, one of these instances is selected as the representative, and extracted block level constraints of this block of this scenario are the constraints related to this instance.

HS-029

(Error) %s.

Description

This error message is issued when the same directory is specified for multiple *set_hier_config* command using the *-path* option, and they are for different design blocks.

What Next

Please make sure you use unique directories to configure for different design blocks. Multiple instances of a same block may use the same directory.

Feedback

HS-030

(warning) The HyperScale block '%s' does not have noise information. Noise analysis for this block is skipped.

Description

This warning message is issued while performing top-level noise analysis using HyperScale blocks that did not receive noise analysis at the block level. Noise analysis for these HyperScale blocks is skipped at the top level. However, noise analysis is still performed on the rest of the top-level logic and on other HyperScale blocks with noise information.

What Next

If you want noise analysis to be performed on a HyperScale block, you need to perform noise analysis at the block level using *update_noise* or *report_noise*, just as you use *update_timing* or *report_timing* at the block level, and write the hierarchical interface data to generate noise information for the block model.

See Also

- set_hier_config
- update_noise
- update_timing
- write_hier_data

HS-031

(warning) %s '%s' referenced by the command%s is inside the boundary of a HyperScale block.

Description

The object (or instance of the object in the case of a library object) is found inside a HyperScale block instance. Altering the characteristics of the object may invalidate the instance of the model

What Next

All commands that alter the timing or structure of HyperScale instances should be performed during the creation of that instance.

Feedback

See Also

- report_hier_analysis
- hier_enable_analysis

HS-032

(Warning) Clock '%s' is an re-entrant clock for block '%s'.

Description

A clock defined inside a block goes outside of the block, and then reaches an input port of that block. This kind of clock is re-entrant clock. This clock should be defined as a multi-source clock at block level: the sources are the source inside the block and that input port.

When clocks are not defined in this way, clock definition scope violations are reported in *report_constraints*.

Sometimes multiple clocks corresponding to this same top level clock are defined at block level. This is not supported in HyperScale. The re-entrant clock has to defined as a multi-source clock at block level.

For example, suppose a clock *CLK* defined at *blk/u1/Z* comes back into the block *blk* at port *clk*, definition at top level:

```
create_clock -name top_CLK -period 10 blk/u1/Z
```

definition at block level:

```
create_clock -name blk_CLK -period 10 {u1/Z clk}
```

When one of the sources is missing at block level, a clock definition scope violation is reported at top level:

```
Clock: top_CLK (mapped to blk_CLK at block level)
    Instance: blk
    block_boundary_clock_definition

    Design   Clock Sources      : { blk/u1/Z blk/clk}
    Instance Clock Sources      : { blk/u1/Z}  (VIOLATED)
```

What Next

Correct the definition of that clock if clock definition scope violations are reported.

HS-033

(error) No corresponding clock for virtual clock '%s' with period %f.

Feedback

Description

When clock network of a clock at top level does not enter a block, but input/output delays on some ports of blocks are referring to it, this clock should be created as virtual clocks at block level. To check which ports are referring to this clock, please check input/output delay scope violations in the *report_constraint* report from top level.

What Next

Add the definition of that clock and its related constraints (e.g., uncertainty, clock groups) into block level constraints.

HS-034

(warning) Instance '%s' inside HyperScale block '%s' referenced to '%s' is resolved as black box in block level run, renamimg the black box reference as '%s'.

Description

In HyperScale top level run, if black box is created and it is carried on from the block level, this message will be issued.

What Next

Check the reference in the block design.

HS-035

(warning) Option '%s' is ignored in HyperScale analysis flow.

Description

The command option is ignored in HyperScale analysis flow.

What Next

Check command options for correctness.

HS-036

(Error) %s %s.

Description

This is a message related to context override at HyperScale block-level analysis.

Feedback

What Next

If you are running the HyperScale flow, adjust the setup and constraints to be compatible; otherwise, no actions are required.

HS-037

(Error) %s %s.

Description

This is a message related to model loading at HyperScale top level analysis.

What Next

If you are running HyperScale flow, please adjust the setup and constraints to be compatible; otherwise, no actions required.

HS-038

(warning) Found net connected to pin '%s' has %s, processing of this boundary pin is skipped.

Description

This is a message related to context capture for HyperScale or HyperScale Constraint Extractor. HyperScale constraint extractor and context capture automatically skip processing unbuffered hierarchical pins (HyperScale block ports) with large number of segments and leaf pins.

HS-039

(warning) The HyperScale %s for block '%s' in current config directory is different from the one used in the saved session, the restored session can only be used to generate reports and not re-perform any timing analysis.

Description

This message will be issued during restore_session if the saved session is a HyperScale session, and the HS block model or top context database for use in the original saved session changed at the time of the restore.It is not recommanded to re-time the design within the restored session if the message is issued.

What Next

Re run the design if timing update is needed.

Feedback

HS-040

(Error) Ignore user set clock mapping for clock '%s', because it doesn't exist in %s.

Description

This message is issued during update_timing after block model or top context is loaded, so that the user set clock mapping can be checked to see whether the clocks exist in block model or top context. If not, the clock map setting for that clcok will be ignored.

What Next

Check the clock names used in "set_clock_map -parent_clock_name/ block_clock_names", make sure the clock does exist in the context or model.

See Also

- set_clock_map

HS-041

(error) Failed writing HyperScale data because %s.

Description

This is a severe error that can prevent HyperScale flow from executing properly.

What Next

Check to make sure all the configurations setup for the HyperScale analysis is correct. And the HyperScale data are updated properly for hierarchical analysis.

For example, if you are trying to write out block session for top level analysis while there are still pending netlist changes in the block, HyperScale block abstraction cannot be written because it may not accurately represent the actual block after implementation and therefore not fully representing the block timing at top level analysis. It is required that users write these changes out and implement them with tools such as IC Compiler to obtain an updated netlist and physical data, perform block level analysis to generate data for further top level analysis.

See Also

- set_hier_config
- hier_enable_analysis

Feedback

HS-042

(error) You must specify at least two subblock instances to -instance option.

Description

ECO-driven context is generated only on HyperScale block ports that are connected to other HyperScale blocks specified in *-instance* option. So at least two HyperScale block instances need to be specified to *-instance* option.

What Next

Specify at least two HyperScale block instances to *-instance* option.

HS-044

(warning) Generated clock '%s' inside block instance '%s' refers to master clock '%s' that can not directly reach the block through boundary pin '%s', recommanded master clock(s) could be %s.

Description

Defining generated clock referring to master clock across other generated clock in between is not recommended. For best results in hierarchical analysis, chain of generated clocks rooted from the same master should be defined in a cascaded style such that each generated clock only refers to the closest clock or generated clock as its master, without cross the source network of other generated clock within the same chain.

What Next

Please update the noted generated clock defintion inside block by change the master to the recommended clock which can directly reach the block, or referring to other suitable generated clock on the same chain inside the same block.

HS-045

(Error) Generated clock '%s' inside block instance '%s' refers to master clock '%s' that can not directly reach the block through boundary pin '%s', no recommanded master clock(s) found on the same chain.

Description

When PrimeTime cannot automatically recommend a candidate master clock(s) on the same chain, it is often because the master clock network passed through sequential elements (e.g. a register cell) before entering the noted block port. This style of generated clock definition requires use of block constraints extracted from PrimeTime, or user must define the clocks with advanced senses to completely model the flat timing behavior. Refer

to *set_sense* command for more details. Alternative is to follow the workaround suggested in the below section.

What Next

After identifying the sequential elements between the closest clock source and block boundary port, there are 2 possible solutions recommended to update the constraints:

1. Move the closest clock (or generated clock) definition after the sequential element so that it can reach the block through only combinational logic.
2. Define an additional clock (or generated clock) after the last sequential element so it can reach the block through only combinational logic.

after either 1. or 2., then redefine the noted generated clock inside the block by referring to this moved or new clock as its master.

HS-046

(warning) Clock '%s' in block instance '%s' is defined on hierarchical pin '%s' that is on the same net of the block boundary pin '%s'.

Description

Defining clocks or generated clocks on hierarchical pins are generally not recommended for PrimeTime. This can potentially introduce timing correlation issues between block and top level analysis.

What Next

When clocks need to be defined on hierarchical pins, it is recommanded that the clock should not be defined on the hierarchical pin between the block boundary port and its connected leaf load pins; instead, please move the clock source pin onto the block boundary pin or the leaf pins.

HS-047

(information) Found clock '%s' reaching block boundary pin '%s' through both combinational and sequential paths.

Description

While characterizing the context around block boundary, it is found that a clock defined outside of the block reaching the specified block port (hierarchical pin) through both combinational logic paths and sequential logic paths. The two types of paths are converging at this same port. This is detected only when there is generated clock(s) downstream. Both the combinational and the sequential paths are considered as the source network for downstream generated clock and used for source latency computation.

This causes potential ambiguity in clock latency and CRPR context captured for the incoming clock outside of the block.

What Next

Check whether the clock network is expected to have both combinational and sequential logic paths converging at the block boundary. If only one of the source latency paths is valid, you can use command 'set_sense' to stop the unneeded propagation paths.

HS-048

(information) Found clock '%s' not used to define generated clocks in the fanout of pin '%s' on block port pin '%s'.

Description

This informational message is triggered by potentially asymmetric leaf branches through the same block boundary clock port. During context characterization around a block boundary, for any block port (hierarchical pin) top level clock enters through and with multiple leaf pin branches inside the block, PrimeTime generally expects these leaf pin branches are equivalent in terms of their fanout logic, such as using the same incoming clock to define generated clock downstream. However, when some branch(es) are used to specify generated clock(s) in their fanout while other branches do not use the incoming clock to specific generated clock(s) in their fanout. PrimeTime issues this message to inform users anout the difference, and check whether this difference among the branches are expected.

What Next

Check the leaf pins on the block port where the clock network enters, whether they are expected to be referred to by different generated clock(s) downstream of the same port.

HS-049

(Warning) These HyperScale data files might have been moved or deleted: "%s" in directory "%s".

Description

Failed to access the HyperScale data file. This may cause information loss.

What Next

Regenerate or retransmit the HyperScale data.

Feedback

HS-050

(Warning) The HyperScale data index file in "%s" is incomplete.

Description

The HyperScale data index file is incomplete. This may cause the HyperScale data file integrity check to be incomplete.

What Next

Regenerate or retransmit the HyperScale data.

HS-051

(Warning) These HyperScale data files might have been modified: "%s" in directory "%s".

Description

The size of HyperScale data file is different from when it was first generated. This change may cause information loss when reading HyperScale data.

What Next

Regenerate or retransmit the HyperScale data.

HS-052

(Warning) The value "%d" of hier_block_interface_model_latch_level is out of range. Please re-apply the value.

Description

This message is issued during HyperScale top level run, when the latch level value set by the user using *set hier_block_interface_model_latch_level* is out of the range. The maximum value depends on *timing_through_path_max_segments* which specifies the muximum number of latches for reporting paths through latches. If the value is larger than the maximum value define by *timing_through_path_max_segments*, Hyperscale will set it as the same value as defined by *timing_through_path_max_segments*. If the value is smaller than 0, Hyperscale will set it as 0.

What Next

Please make sure you have the correct latch level value which falls inside the range.

Feedback

HS-053

Description

This message is issued when PrimeTime detects very complex timing paths propagating through the pin noted, internally each unique class of path is tracked by a separate arrival or required time propagating through the hierarchical pin/port noted. This excessive data can result in large volume of context data captured on these pins, further cause increased memory and slower runtime both in capturing the context at top level and consumption of the context at block level.

The most usual factors can cause this excessive of path analysis complexity include: multiple clocks reaching launch/capture registers, complex reconvergent clock network and CRPR analysis, very large number of exceptions applied in the fanin or fanout of the block boundary, etc.

What Next

Please review the constraints relevant to the pins mentioned.

HS-054

(error) The object_list must be a design when using set_dont_override -include {timing_derate}.

Description

When overriding the timing derate in block level, the object_list must be a design instead of a port.

What Next

Using a design for object_list.

HS-055

(information) boundary_check and boundary_check_include options of report_constraint are invalid when boundary check variable is disabled.

Description

When timing_enable_hier_boundary_check is false, no boundaries can be reported.

What Next

Enable timing_enable_hier_boundary_check to report boundaries.

Feedback

HS-056

(Warning) %s.

Description

This warning message is generated when the HyperScale block MIM instances are re-characterized using *characterize_context* command in the HyperScale top flow. When all the instances are individually re-characterized, no merged context will be generated. Otherwise, the remaining instances which are not re-characterized will be generated in the merged context.

What Next

Please make sure you have characterized the right instance in the HyperScale top flow after linking.

HS-057

(Warning) Instance "%s" is the reference instance of block "%s" and the merged context will be written.

Description

When using *write_context* command in the HyperScale flow, if the instance is not re-characterized by *characterize_context* command, the merged context including this instance will be written.

What Next

Please make sure you have characterized the right instance that you want to write context.

HS-058

(information) Merged latency is the largest window for clock "%s" of port "%s".

Description

When *hier_context_merge_clock_latency_mode* is set to *largest_window*, and the noted clock is asynchronous to other clocks for the block, MIM context merging is using largest window to minimize clock window and pessimism in SI analysis. Also, when total clock latency is merged in the mode *largest_window*, the static latency will be automatically adjusted to use *match_total_latency* mode to ensure consistency.

What Next

No action is required for this informational message. Please check the merge mode if necessary.

Feedback

HS-059

(warning) Merged latency is the default mode min_max_value for clock "%s" of port "%s" because it has at least one synchronous clock.

Description

When *hier_context_merge_clock_latency_mode* is set to *largest_window*, and the noted clock is synchronous to at least one other clock in the block, MIM context merging is expected to use the default mode *min_max_value* to ensure bounding timing and conservative SI analysis at block level.

What Next

No action is required for this informational message. Please check the merge mode and clock domains if necessary.

HS-060

Description

This message is issued when PrimeTime detects no data arrival or required timing context captured on the specified pin. This could be due to unconstrained paths or reduced effort for required propagation due to excessive amount of unique paths (see HS-053).

In the block level run with context, the relevant ports will use the budget input/output delay values from user constraints, since no context is available on them.

What Next

Please review the constraints relevant to the pins mentioned as well as checking for HS-053 messages

HS-061

(warning) Merged latency is forced to use the largest window for clock "%s" of port "%s" while it is synchronous with at least one other clock.

Description

You receive this waning message when *hier_context_merge_clock_latency_mode* is set to *largest_window*, and the noted clock is synchronous to at least one other clocks in the block. It is recommended to use the default *min_max_value* mode to merge the context for different instances of the block in order to ensure the bounding timing analysis at the block level with the merged context, which may include extra pessimism. Also, when total clock latency is merged in the mode *largest_window*, the static latency will be automatically adjusted to use *match_total_latency* mode to ensure consistency.

Feedback

What Next

Please review the clock relationship and the context merge mode variable to ensure it is expected.

HS-062

(Warning) Apply logic value "%d" from context on port "%s", override existing setting "%s" on the port.

Description

This message is issued during HyperScale block level run, when the case value set by the user using *set_case_analysis* is different from the case value from the top context or the port does not have a case value.

What Next

Please make sure you want to override the block case value using top level context or you have a valid case value set.

HS-063

(error) -include model_constraints_data must be used with -netlist option.

Description

When using write_hier_data to write out the block constraints, the option model_constraints_data must be used with -netlist option.

What Next

Use -netlist option combined with -include model_constraints_data.

HS-064

(Warning) Remove logic value "%d" on port "%s", apply arrival data from context.

Description

This message is issued during HyperScale block level run, when the case value set by the user using *set_case_analysis* is different from the case value from the top context.

What Next

Please make sure you want to override the block case value using top level context.

Feedback

HS-065

(error) Found top level clock '%s' is mapped to block level clock '%s', but the top level clock is not reaching the block instance '%s' through the pin '%s'.

Description

When user clock mapping is applied between top level clock and block level clock, if the top level clock is not reaching the block instance, no source latency context will be applied for the block level clock.

What Next

Please check the connection between top level clock and block level clock and apply the right user clock mapping between top and block.

HS-066

(Warning) Found cross boundary data check constraints, ignored in context.

Description

This message is issued when doing the cross boundary required time data check which is currently not supported.

What Next

Please make sure the right data is passed in.

HS-068

(Warning) Found multiple clocks at top or block, not map block clock "%s" to top clock "%s", please use user clock map to map them.

Description

This message is issued when doing clock mapping at block level, there are more than one top clocks or more than one block clocks. We do not map them automatically and will leave for user clock map.

What Next

Please use *set_clock_map* command to manually map the clocks.

HS-070

(Warning) Not map top level clock "%s" to block level clock "%s" since one of them is ideal clock.

Feedback

Description

This message is issued when doing clock mapping at block level, top level clock is not ideal clock while block level clock is ideal clock or top level clock is ideal clock while block level clock is not ideal clock. We do not map them automatically and will leave for user clock map.

What Next

Please use *set_clock_map* command to manually map the clocks.

HS-071

(error) Found '%s' of operation condition loading from different top level contexts are different during HyperScale block level analysis.

Description

During HyperScale block level analysis, when loading different top level contexts for merging, the operation conditions of different top contexts must match.

What Next

Please check that the top level run which generates the top context has the same operation condition.

HS-072

(Warning) Not map top level virtual clock "%s" with block level real clock "%s".

Description

This message is issued when doing clock mapping at block level, top level clock is virtual clock while block level clock is real clock. We do not map them automatically and will leave for user clock map.

What Next

Please use *set_clock_map* command to manually map the clocks.

HS-074

(information) Clock '%s' is merged to clock '%s' in the reference design.

Feedback

Description

This infomation is given during HyperScale top level MIM (multiply instantiated modules) context merging flow, when the clocks (with different sources and clock names but all other attributes are the same) are entering the same port of the MIM instances.

What Next

No action is required.

HS-076

(Information) Set parasitics corner %s for corner domain %s and corner %s on cell %s.

Description

The HyperScale could set parasitics corner implicitly with the *set_hier_config* command.

What Next

No action is required.

See Also

- set_hier_config

HS-100

(information) HyperScale timing context around instance '%s' is successfully merged with instance '%s'.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the timing data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified.

When merge succeeds with this message, the context for the instance noted is covered by a merged context noted. And a single context is written for all successfully merged instances for a single block level analysis.

What Next

No action is required.

Feedback

See Also

- set_hier_config

HS-101

(error) Found clock '%s' propagating to instance '%s' through pin '%s', but no matching clock reaching the equivalent pin on instance '%s' of the same block.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified. In order to automatically merge the context for two HyperScale block instances of the same block, it is required that the instances must have exact matching clocking scheme. Otherwise, their context data cannot be merged together and analysis must be done seperately to cover each clocking scheme. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the first instance noted.

What Next

You can use *report_timing*, or *report_attribute* commands to verify the message.

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- set_hier_config

HS-102

(warning) Found different %s between pin '%s' on instance '%s' and the equivalent pin '%s' on instance '%s' of the same block.

Feedback

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified.

When different case value or disable timing settings are found at the same port of different instances, merged context will have no case value or no disable timing set, and result in a more conservative analysis at block level.

What Next

You can use *report_disable_timing*, or *report_case_analysis* command to verify the message.

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you verify that this conflict is not expected and it represents a constraint setup problem at top level.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- set_hier_config

HS-103

(error) Failed to merge HyperScale timing context around instance '%s' with reference instance '%s'.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified.

In order to automatically merge the context for two HyperScale block instances of the same block, it is required that the instances must be operated in a similar mode and environment, for example, one of the fundamental reqreuirments is that all the instances of the same block must have exactly matching clock and clock topology on the boundary.

Feedback

Otherwise, their context data cannot be merged together and analysis must be done seperately to cover each operating context seperately in order for the top level analysis to remain valid.

It is worth emphasize that ultimately only the users know the design intention and whether or not the different instances of a same physical block are truly operating similarly or equivalently on the same chip under the targeted timing analysis setup.

When merge fails with this error message, the context for the instance noted is discarded and PrimeTime only saves the context covering the reference instance noted. Reference instance is the first instance specified with the same HyperScale config.

What Next

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- set_hier_config

HS-104

(error) Found different %s between pin '%s' on instance '%s' and the equivalent pin '%s' on reference instance '%s' of the same block.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified. In order to automatically merge the context for two HyperScale block instances of the same block, it is required that the instances must have exact matching case values. Otherwise, their context data cannot be merged together and analysis must be done seperately. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the reference instance noted.

Feedback

What Next

You can use *report_disable_timing*, or *report_case_analysis* command to verify the message.

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- set_hier_config

HS-105

(Warning) Cross-boundary %s exceptions are not supported in PrimeTime HyperScale. The exception type will not be captured as part of the context.

Description

Some exception types are not supported in HyperScale across block boundaries in the current release. For supported exception types (false path, multicycle path), cross-boundary exceptions specified during top analysis will be captured during top-level analysis and applied during block-level analysis

This warning may be issued even when the exception cannot be satisfied across the boundary.

What Next

The exception will not be applied to other HyperScale blocks automatically. If this is ok, then no changes need to be performed by the user. If this exception is needed, separate exceptions can be specified during block analysis and during top analysis.

See Also

- set_hier_config

HS-106

(information) Instance '%s' is selected as the reference for context merging, %d other instances can be merged with it.

Feedback

Description

When *set_hier_config* is used to specify a single data storage path and label for multiple top level instances of the same reference block, the timing data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified.

Before merging the context for these instances, a pre-analysis is performed to identify a referece instance to which the most number of instances can be merged together. The criteria used to determine whether contexts for 2 instances are mergable is the 2 instances have the same or equivalent clocks reaching their boundaries.

What Next

No action is required.

See Also

- set_hier_config

HS-107

(Warning) Enabling this variable in HyperScale may reduce performance and/or capacity benefits in top level runs.

Description

When preset/clear arcs are enabled a much larger part of the block becomes part of the interface logic that is of interest for the top level analysis. HyperScale will adjust its block level data to enable a much more thorough top level analysis. This extended top level analysis comes with an decrease in the run time and capacity efficiency.

What Next

No action is required.

HS-108

(Information) Clock '%s' propagating to instance '%s' through pin '%s', the equivalent pin '%' on instance '%s' is constant logic instead.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the

Feedback

instantiation specified. In order to automatically merge the context for two HyperScale block instances of the same block, it is required that the instances must have exact matching clocking scheme by default. However, for specical case of clock port(s) are intentionally fed by or tied to constant logic for some instances without either data or signal propagating through, you can choose to override the exact matching requirement with the variable '*hier_merge_match_clock_with_constant*' to force the context merging.

What Next

Please use *report_timing*, or *report_attribute* commands to verify the message.

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to update the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- set_hier_config

HS-109

(Severe) %s.

This is a severe error that can prevent HyperScale flow from executing properly.

What Next

Check to make sure all the configurations setup for the HyperScale analysis is correct.

See Also

- set_hier_config
- hier_enable_analysis

HS-110

(warning) No corresponding clock for %s clock '%s' with clock '%s' %s due to %s are different: %s, %s.

Feedback

Description

In HyperScale analysis, clocks from block level have to be mapped to clocks defined at top level in order to properly interpret the timing data and constraints. If this mapping fails for any clock, an warning is issued. To see the details of failed clock mapping, please use report_clock -map.

What Next

report_constraint(2). report_clock(2)

HS-111

(Warning) Directory '%s' is already used in configuration for an instance sets of block %s.

Description

This error message is issued when the same directory is specified for multiple *set_hier_config* command using the *-path* option, and they are for a same design block with different instance sets. This may cause failures in finding context data at block level run.

What Next

Please make sure you use unique directories to configure for different instance sets. Multiple instances of a same block using the same directory will not be allowed in a future release.

HS-112

(Error) Command is in conflict with an earlier set_hier_config command for block %s. Command will be ignored.

Description

This error message is issued in two situations:

1. A previous *set_hier_config* command without -instances was already set on a block. This means all instances of that block are represented by the HyperScale data in the same directory. Then a new *set_hier_config* command with -instances option for the same block is entered. Changing the directory for a portion of the instances is not allowed.
2. One or multiple *set_hier_config* commands with -instances options were previously set on a block. Then a new *set_hier_config* command without -instances option for the same block is entered. This is not meaningful and is not supported either.

Feedback

What Next

If you want to change the directory in the a previous *set_hier_config* command, repeat the previous *set_hier_config* with the new directory.

HS-113

(Information) The command overrides previous HyperScale config for some instances or all instances

Description

This message is issued when some or all instances specified or implied by a set_hier_config command have already been configured by previous set_hier_config commands. The new config will override previous ones for these instances.

What Next

No action required.

HS-114

(Error) %s context data at port '%s' because expected pin '%s' is not on the same net.

Description

This message is issued during context override at the HyperScale block level analysis, where there is a netlist mismatch found on the port net between current block design and HyperScale top level context data. A best-effort context override will be applied to the related port.

What Next

No action required. To ensure accurate context override, please use consistent block and top netlist.

HS-115

(Error) Missing capture clock for required context at clock port '%s' because no clock is mapped with '%s'.

Description

This message is issued during context override at the HyperScale block level analysis, where there is no mapped capture clock found on the output port between current block design and HyperScale top level context data. The context override will be failed on this port.

Feedback

What Next

Please use "report_clock -map" to check the clock mapping between HyperScale top and block level analysis. Source the clock_map.pt file from constraint extractor could help solve this problem.

HS-116

(Error) Ignore source latency context for clock '%s' at clock port '%s' because no mapped clock found.

Description

This message is issued during context override at the HyperScale block level analysis, where there is no mapped clock found in current block analysis for the clock lantency context characterized from HyperScale top level analysis. The source lantency context override for this clock will be failed.

What Next

Please use "report_clock -map" to check the clock mapping between HyperScale top and block level analysis. Source the clock_map.pt file from constraint extractor could help solve this problem.

HS-117

(Error) Ignore source latency context for virtual clock '%s' because no mapped clock found.

Description

This message is issued during context override at the HyperScale block level analysis, where there is no mapped clock found in current block analysis for the clock lantency context characterized from HyperScale top level analysis. The source lantency context override for this clock will be failed.

What Next

Please use "report_clock -map" to check the clock mapping between HyperScale top and block level analysis. Source the clock_map.pt file from constraint extractor could help solve this problem.

HS-118

(Error) Missing launch clock for arrival context at clock port %s because no clock is mapped with %s.

Feedback

Description

This message is issued during context override at the HyperScale block level analysis, where there is no mapped lauch clock found for the arrival context on the input port between current block design and HyperScale top level context data. The arrival context override associated with this clock will be failed.

What Next

Please use "report_clock -map" to check the clock mapping between HyperScale top and block level analysis. Source the clock_map.pt file from constraint extractor could help solve this problem.

HS-119

(information) Variable timing_save_pin_arrival_and_slack is set true. This is required for generating ECO-driven context or slack based context margin allocation.

Description

This is a generic message to issue for the change of variable value.

What Next

No action required.

HS-120

(Information) %s %s.

Description

This is a generic message to issue for specially pre-programmed features. In order to ensure QoR consistency of HyperScale block and top level analysis to align with flat timing analysis, selected settings are programmed with fixed value once HyperScale is enabled, such as wire_load_mode and wire_load_model.

```
Information: value 'top' is pre-programmed for command
 'set_wire_load_mode'
                in hierarchical flow enabled with
 'hier_enable_analysis'. (HS-120)

Information: value 'false' is pre-programmed for variable
 'auto_wire_load_selection'
                in hierarchical flow enabled with
 'hier_enable_analysis'. (HS-120)
```

What Next

No action required.

Feedback

HS-121

(Error) Found clock '%s' propagating to instance '%s', but no matching clock with equivalent pins of same '%s' on instance '%s' of the same block is found.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified. In order to automatically merge the context for two HyperScale block instances of the same block, it is required that the instances must have exact matching clocking scheme. Otherwise, their context data cannot be merged together and analysis must be done seperately to cover each clocking scheme. This error message shows which clocking scheme is causing the merging can not proceed. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the first instance noted.

What Next

You can use *report_timing*, or *report_attribute* commands to verify the message.

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level constraints if you ensured that this is a constraint setup problem at top level and the block should have the same clocks and similar contexts when instantiated multiple times.

You can choose to configure for seperate analysis to cover different context for the instances if you ensured that the top level constraint setup is correct and these instances of the same block are assumed to subject to different contexts for timing analysis.

See Also

- HS-101

HS-122

(warning) Command '%s' requires hyperscale or hyperscale constraint extractor enabled.

Description

You received this error message because the hier_characterize_context_mode has been set to full_context and hier_enable_analysis has been set to false while the commend requires at least one of them being enabled.

Feedback

What Next

Determine whether you want to enable hyperscale or hyperscale constraint extractor. If you do, set the hier_characterize_context_mode to constraints_only or hier_enable_analysis to true.

See Also

- hier_characterize_context_mode
- hier_enable_analysis

HS-123

(warning) Library '%s' used to link block '%s' (for example, instance '%s') was either not used or was a different version for linking this top level.

Description

You received this warning message because the library used at hyperscale block level doesn't has a matching library at top level. This could cause the corrsponding objects from hyperscale block model not being correctly linked.

What Next

Check the libraries used at block and top and make sure the library used at hyperscale block is also available at hyperscale top.

See Also

- timing_save_hier_context_data

HS-124

(warning) Cannot find a clock mapping to %s clock '%s' referred %s abstraction data.

Description

In HyperScale analysis, clocks from block level have to be mapped to clocks defined at top level in order to properly interpret the timing data and constraints. An warning is issued on the fail of this mapping for clock with abstraction data. To see the details of failed clock mapping, please use report_clock -map.

What Next

report_constraint(2). report_clock(2)

Feedback

HS-125

(information) Extracting UPF.

Description

In HyperScale flow, block UPF data will be automatically extracted for top level run. If no UPF is present in block, nothing will be extracted. During top level run, the extracted block UPF will be automatically loaded in top level along with HS abstract.

What Next

Please refer to Synopsys Multivoltage Flow User Guide for UPF related issue.

HS-126

(information) Auto loading UPF for HyperScale blocks.

Description

In HyperScale flow, block UPF data will be automatically extracted for top level run. If no UPF is present in block, nothing will be extracted. During top level run, the extracted block UPF will be automatically loaded in top level along with HS abstract.

What Next

Please refer to Synopsys Multivoltage Flow User Guide for UPF related issue.

HS-127

(error) No context to be written while timing_save_hier_context_data is set to false.

Description

In HyperScale top level run, if you set timing_save_hier_context_data to false, no context data will be captured. If using write_hier_data after this variable to false, no context data will be written out.

What Next

Please check the setting of timing_save_hier_context_data and use update_timing to capture context before write_hier_data.

HS-128

(warning) No context to be written while timing_save_hier_context_data is set to false.

Feedback

Description

In HyperScale middle level run, if you set timing_save_hier_context_data to false, no context data will be captured. If using write_hier_data after this variable to false, no context data will be written out, but model data will still be written out.

What Next

Please check the setting of timing_save_hier_context_data and use update_timing to capture context before write_hier_data.

HS-129

(warning) Cannot open directory '%s' for context reading.

Description

This message is issued because the directory given in read_context may not exist, or might have incorrect permissions. The directory in read_context should match the directory given in write_hier_data or write_context in the run from parent design.

What Next

Please check the directory given in read_context exits and contains binary context.

HS-130

(warning) Cannot open context files in directory '%s' for reading.

Description

The context files in the specific directory could not be opened for reading. It may not exist, or might have incorrect permissions.

What Next

Verify the directory name and check context files in the directory.

HS-131

(Information) %s.

Description

PrimeTime found a large boundary net connected to a huge amount of leaf pins

Feedback

HS-132

(warning) Override the previous context margin for %s. Previous context margin: %s

Description

Margin override warning message for 'set_context_margin'.

What Next

set_context_margin(2).

HS-133

(warning) The command overrides previous 'read_context' setting.

Description

Warning message for 'read_context'

What Next

read_context(2).

HS-134

(information) HyperScale block flow enabled for model capturing and writing.

Description

Information message for 'read_context'.

What Next

read_context(2).

HS-135

(warning) HyperScale context data in directory '%s' is written with a different mim_group name '%s'.

Description

Context data written with different mim_group name

HS-136

(warning) HyperScale database is generated by an earlier version.

Feedback

Description

Hyperscale database was generated using an earlier version.

HS-137

(Warning) Not all instances are specified for a MIM instance.

Description

One or more MIM instances are missing for EDC generation.

HS-138

(warning) Old UI has been used, enabling UI compatibility mode to convert to new UI.

Description

Old UI of Hyperscale configuration was used by the users. Converted to new UI internally.

What Next

set_hier_config(2).

HS-139

(Warning) Not in block level analysis flow, command 'set_dont_override' is ignored.

Description

Command '*set_dont_override*' only works for block level flow.

What Next

set_dont_override(2).

HS-140

(error) Specify either '-all' or '-instances'.

Description

Either '-all' or '-instances' option is required.

HS-141

(error) No HyperScale related data to be written, feature not used.

Feedback

Description

Hyperscale flow type is unknown, no data is written.

What Next

write_hier_data(2)

HS-142

(error) 'write_hier_data' command only works after finishing update_timing.

What Next

write_hier_data{2}

HS-143

(error) 'write_hier_data' command only works for HyperScale or Constraint Extractor flow. With additional option specified, it can be used with '-parasitics' only for HyperScale block level run, or '-config' for HyperScale top level run.

What Next

write_hier_data(2)

HS-144

(Error) Instance name '%s' is not a valid name.

What Next

write_hier_data(2).

HS-145

(Error) Instance '%s' is not a hierarchical cell.

What Next

write_hier_data(2).

HS-146

(error) The '-check_block_constraints' option is not compatible with a multi-scenario analysis.

Feedback

What Next

report_constraint(2).

HS-147

(information) Applying path specific latency for HyperScale block.

Description

information message

HS-148

(information) Start using ECO-driven context for timing analysis.

Description

Hyperscale ECO flow information message. No action required.

HS-149

(information) ECO-driven context is not available for current block. Start using normal context for timing analysis.

Description

Hyperscale ECO flow information message. No action required.

HS-150

(information) %s HyperScale data to session directory.

Description

save_session informational message. No action required.

HS-151

(information) ECO-driven context is successfully created.

Description

save_session informational message. No action required.

Feedback

HS-152

(Warning) Port '%s' is connected with both input and output pins, this may impact the accuracy of model data associated with it in HyperScale block abstraction.

Description

You receive this message to warn you that HyperScale detected the noted port is connected with both input and output pins. This happens most often for unbuffered output port with net looping back into timing paths and end points internal to the block. This can result in potential accuracy degradation in in HyperScale block abstraction, because the timing paths looped back into the block are impacted by the port load external to the block; and the net arc delays between the outgoing and loop back branches may be different.

What Next

Please verify the connectivity of the noted port. It is recommended that the port be properly buffered to isolate impact from external loading effects to the internal loop back timing paths.

HS-153

(warning) Could not skip writing parasitics in HyperScale model.

Description

You receive this message to warn you that write_hier_data still generates parasitics files in HyperScale model data. It is not skipped since some parasitics file read in is not SPEF or GPD format.

What Next

Please verify that all parasitics files read in are SPEF or GPD format. Otherwise the parasitics file can not be skipped in HyperScale model.

HS-154

(error) Parasitics file '%s' used to block '%s', instance '%s' was either not read in or was a different version for this top level.

Description

You received this error message because the parasitics file used at hyperscale block level doesn't has a matching parasitics file at top level. This could be caused by that the parasitics in block level is skipped written in model and not being read in at top or top is reading in a different version of file.

Feedback

What Next

Check the parasitics file used at block and top and make sure the parasitics file used at hyperscale block is also available at hyperscale top.

See Also

- write_hier_data

HS-155

%s

Description

You receive this message because '-partition' and '-exclude' options can not be specified at the same time.

What Next

Please modify your setup and re-try

HS-156

%s

Description

You receive this message because '-partition' and '-split' options can not be specified at the same time.

What Next

Please modify your setup and re-try

HS-157

%s

Description

You receive this message because it is already running distributed Flat-like reporting flow, option '-partition' (for analysis flow) will be negelected.

What Next

Please check your setup and re-try

Feedback

HS-158

%s

Description

You receive this message because it is already running distributed analysis flow, option '-session' (for Flat-like reporting flow) will be negelected.

What Next

Please check your setup and re-try

HS-159

%s

Description

You receive this message because it is already running distributed (analysis or reporting) flow. hyperscale analysis specific setup is neglected.

What Next

Please check your setup and re-try

HS-160

(warning) *hier_enable_analysis* is not fully supported by *set_advanced_analysis*.

Description

You receive this message to inform you *hier_enable_analysis* is not fully supported by *set_advanced_analysis*.

What Next

Do not use *set_advanced_analysis* after setting *hier_enable_analysis* to true. Alternatively, user can set timing_enable_auto_mux_clock_exclusivity to false.

HS-161

(information) %s will be made obsolete and is replaced by %s

Description

This is an information message indicating the specified command, option or variable is in the process of being obsoleted and is replaced by the recommended name.

Feedback

HS-162

(warning) Hierarchical pin '%s' is connected with both input and output pins, this may impact the accuracy of context data associated with it in context characterization.

Description

You receive this message to warn you that the noted the hierarchical pin is connected with both input and output pins. This happens most often for unbuffered output pin with net looping back into timing paths and end points internal to the block. This can result in potential accuracy degradation in context characterization, because the timing paths looped back into the block are impacted by the pin load external to the block; and the net arc delays between the outgoing and loop back branches may be different.

What Next

Please verify the connectivity of the noted pin. It is recommended that the pin be properly buffered to isolate impact from external loading effects to the internal loop back timing paths.

HS-163

(Error) write '%s' context is not supported when hier_characterize_context_mode is set to constraints_only.

Description

When hier_characterize_context_mode is set to constraints_only, the gbc format context is not supported in write_context. Besides, the boundary_only option can not be used when it is set to constraints_only. To use these functionalities, please set hier_characterize_context_mode to full_context.

HS-164

(Error) Must specify the '-path' option when '-session' is specified.

Description

User must specify the directory where session is located.

HS-165

(Error) command 'set_hier_config' usage without option '-block' has been made obsolete.

Feedback

HS-166

(Error) Must specify the '-path' option when '-block' is specified.

Description

User must specify the directory where block data is located.

HS-167

(Error) Must specify either '-block' option or '-instance' option when specifying the name for Multi-Instance(MIM) group.

Description

User must specify the block/instances that when creating a MIM group. Note that the number of instances (if specified) should be larger than 1.

HS-168

(Error) Must also specify '-block' option when '-path' option is specified.

Description

User must specify the block/instances for configuration.

HS-169

(Error) Cannot enable hier analysis after hier_characterize_context_mode is set to constraints_only, ignored.

Description

The constraints_only mode in hier_characterize_context_mode and hier analysis are mutually exclusive. You could only enable one of them at a time.

What Next

Disable the constraints_only mode or her analysis so that you could enable the other mode.

HS-170

(Error) Change flow type after timing update is not allowed.

Feedback

Description

HyperScale must be enabled or disabled before update_timing. Change flow type after timing update is not allowed.

What Next

Enable or Disable HyperScale before update_timing.

HS-171

(Warning) By setting this option, user intents to run hierarchical distributed analysis flow. If this is not user's intent, please remove all following options "-partitions", "-split", "-enable_mim" or "-exclude" in your run script and re-try.

HS-172

(Information) Found sense mismatch at pin '%s' for clock '%s'; top-level context expects '%s' sense. Clock sense at pin has been overridden.

Description

When the clock network of a clock at the top level enters a block, the logic between top clock source and the block entry pin can modify the sense of the clock signal, such as inverting the waveform through an odd number of inverters in the clock path.

To perform proper block-level timing analysis, you should specify the clock waveforms observed at the entry pin while maintaining the same period.

What Next

Check the clock definition of the block constraints for the noted clock, or inspect the logic between the top-level clock source and the block entry pin.

HS-173

(Error) Found sense mismatch at pin '%s' for clock '%s'; top-level context expects '%s' sense.

Description

When the clock network of a clock at the top level enters a block, the logic between top clock source and the block entry pin can modify the sense of the clock signal, such as inverting the waveform through an odd number of inverters in the clock path.

To perform proper block level timing analysis, you must specify the clock waveforms observed at the entry pin while maintaining the same period.

Feedback

What Next

Check the clock definition of the block constraints for the noted clock, or inspect the logic between the top-level clock source and the block entry pin.

HS-174

(information) Model data for block '%s' is '%s' '%s' for analysis.

Description

During linking process, although there is a message HS-007 indicates all Hyperscale models are successfully linked when 'hier_enable_analysis' is set to 'true', this message is used for each individual block level that is found and successfully loaded into the HyperScale top analysis. This would help isolate problematic individual HyperScale block models to help isolate the issue faster. Please cross check with the commands such as 'set_hier_config' and 'report_hier_analysis'.

What Next

Please refer to documentation to understand guidelines and recommendations for proper use of HyperScale analysis.

HS-175

(Warning) The pin '%s' is not connected to any port (maybe because of ECO changes); its context %s value will %s.

Description

When applying context, a boundary pin was found to be no longer connected to any I/O port of the block. This situation usually happens after ECO fixing that inserts or removes buffers directly connected to a port. In this case, PrimeTime decides whether to apply the value or discard it, as indicated in the warning message.

What Next

Check whether the netlist change is intended.

HS-176

(Warning) The pin '%s' is no longer connected to port '%s' (usually because of ECO changes on the port); Its context value will be applied to pin '%s' instead.

Feedback

Description

At block, ECO fixing (such as buffer insertion and removal) on I/O ports can sometimes cause the pin that context was initially captured on to no longer exist. In this case, the context value will be applied on the new load pin of the port as informed in the warning message.

What Next

Check whether the netlist change is intended.

HS-177

(error) Found supply net '%s' in instance '%s' has a different supply group than the equivalent supply net '%s' in instance '%s'%s%s of the same block.

Description

When *set_hier_config* is used to specify a single data storage path and scenario for multiple top level instances of the same reference block, the context data internally computed for these instances during HyperScale analysis are automatically merged into a single overall context for the block, this merged context is intended to cover all the instantiation specified. In order to automatically merge the context for two HyperScale block instances of the same block, it is required that the instances must have exact matching PG scheme. Otherwise, their context data cannot be merged together and analysis must be done seperately to cover each PG scheme. When merge fails with this error message, the context for the second instance noted is discarded and PrimeTime only saves the context covering the first instance noted.

What Next

You can use *get_supply_group*, or *report_supply_group* commands to verify the message.

Based on the knowledge and intention of the design and analysis setup, there are several options to deal with failed automatic context merging.

You can choose to modify the top level upf/PG netlist if you ensured that this is a PG setup problem at top level and the block should have the same PG and similar contexts when instantiated multiple times.

See Also

- set_hier_config

Feedback

HS-178

(Warning) '%s'. The timing/noise analysis results regarding the clock '%s' are valid for those matching DVFS scenarios and invalid for other non matching DVFS scenarios.

Description

When performing Hyperscale DVFS analysis, user needs to make sure that the Top and Block clock definitions to be consistent or compatible for all DVFS scenarios in order to have all Context and Model to be correctly applied. When failing to do so, only Context and Model with regard to those matching scenarios will be applied; Therefore the timing or noise results of those non-matching scenarios are unreliable or invalid.

What Next

You can use "report_clock -map" to see how the clocks are mapped with detailed scenario mapping information. Please correct the clock definitions to match all scenarios to acheive valid timing or noise results for all scenarios.

See Also

- set_clock_map
- report_clock
- create_clock

HS-179

(Error) Missing capture clock for required context at data port '%s' because no clock is mapped with '%s'.

Description

This message is issued during context override at the HyperScale block level analysis, where there is no mapped capture clock found on the output port between current block design and HyperScale top level context data. The context override will be failed on this port.

What Next

Please use "report_clock -map" to check the clock mapping between HyperScale top and block level analysis. Source the clock_map.pt file from constraint extractor could help solve this problem.

Feedback

HS-180

(Error) Ignore source latency context for clock '%s' at data port '%s' because no mapped clock found.

Description

This message is issued during context override at the HyperScale block level analysis, where there is no mapped clock found in current block analysis for the clock lantency context characterized from HyperScale top level analysis. The source lantency context override for this clock will be failed.

What Next

Please use "report_clock -map" to check the clock mapping between HyperScale top and block level analysis. Source the clock_map.pt file from constraint extractor could help solve this problem.

HS-182

(Error) Missing launch clock for arrival context at data port %s because no clock is mapped with %s.

Description

This message is issued during context override at the HyperScale block level analysis, where there is no mapped lauch clock found for the arrival context on the input port between current block design and HyperScale top level context data. The arrival context override associated with this clock will be failed.

What Next

Please use "report_clock -map" to check the clock mapping between HyperScale top and block level analysis. Source the clock_map.pt file from constraint extractor could help solve this problem.

HS-184

(Warning) Format SDC %s doesn't support "-preinvert" option. Option blocked for generated clock %s.

Description

You get this message because the -preinvert option is needed to model the generated clock indicated. Since the selected SDC version does not support this option it is being dropped which may lead to unexpected results when the SDC file is consumed.

Feedback

What Next

Please rerun the context or model generation leading to this message without the -sdc option to allow the -preinvert option to be written.

HS-185

(Information) Report exceed contents' limit.

Description

This message is issued when report content reach the limit, rest of contents will skip. For more content, user can extend the limit by 'set hier_pp_report_limit $number'.

What Next

Set bigger limit number if needed. Use 'set hier_pp_report_limit $number'

HS-186

(Warning) Cannot copy data file %s to destination folder in version compatible save session since there is no such file in original MODEL folder.

Description

You get this message because you try to save a version compatible session and copy the data file which is not existing in the orginal MODEL folder.

What Next

Please use the non version compatible save_session or double check the orginal MODEL folder.

ILM

ILM-001

(error) The interface logic on the current design '%s' has not been identified.

Description

You receive this error message because you have not performed the step to identify interface logic on the current design.

Feedback

What Next

Execute the *identify_interface_logic* command on the current design to set the attribute *is_interface_logic_pin* on pins that are part of the interface logic of the current design.

See Also

- identify_interface_logic

ILM-002

(warning) No object has been identified as belonging to the interface logic on the current design '%s'.

Description

You receive this warning message because you have attempted to identify interface logic on the current design. However, no pin has the attribute *is_interface_logic_pin* set to true.

What Next

Verify that the value given to the *-ignore_ports* option when calling the *identify_interface_logic* command does not include all the input and output ports on the design.

See Also

- identify_interface_logic

ILM-003

(warning) Update_timing has already been performed on the current design '%s'. The interface logic identified will be a function of the assertions applied on the design.

Description

You receive this message if you issue the *identify_interface_logic* command after either executing *update_timing* on the specified design, or issuing commands that caused *update_timing* to be executed. The recommended procedure is to execute *identify_interface_logic* before *update_timing*, so that the interface logic is independent of the assertions (*set_disable_timing*, *set_case_analysis*) defined on the design. Thus, you can change *set_disable_timing* and *set_case_analysis* statements without having to regenerate the interface model for the design.

This message warns you that, because update timing has already been performed, the interface logic identified is a function of the assertions applied on the design. In this case, timing arcs on the design could be disabled by the *set_disable_timing* and

Feedback

set_case_analysis commands, so that logic in the fanout/fanin of the disabled timing arcs would not be part of the interface logic on the current design.

What Next

If it is acceptable to you that the interface logic of the current design is a function of the assertions applied on the design, no action is required on your part. Otherwise, execute the *identify_interface_logic* command before executing *update_timing* on the current design.

ILM-004

(warning) No clocks have been defined on the current design '%s'. All clocks must be defined prior to identifying interface logic or extracting model.

Description

You receive this message if you issue the *identify_interface_logic* or *extract_model* command and have not defined any clocks for the current design. You must define all clocks in a design before executing the *identify_interface_logic* command. This message warns you that errors could result in identifying the interface logic on the current design.

What Next

Use the *create_clock* and *create_generated_clock* commands to define all clocks on the current design. Then reissue the *identify_interface_logic* command.

ILM-005

(warning) A wire-load mode other than "top" is set on the current design '%s'. The wire-load mode needs to be set to "top" for timing of the ILM to match the timing of the design.

Description

You have not defined a wire-load mode of "top" on the current design. This needs to be set for the ILM timing to match design timing in a pre-layout design flow. The reason for this is that ILM's are flattened representations of the original design and do not preserve design hierarchy.

What Next

To not encounter verify errors in a pre-layout design flow when comparing the ILM against the original design you need to ensure that a wire-load mode of "top" is set on the original design.

Feedback

ILM-006

(Information) Port '%s' belongs to the ignore list because it fans out to %d%% of the registers on the design.

Description

You receive this message if you execute the *identify_interface_logic* command with the *-auto_ignore* option, and the fanout of the specified input port has a larger percentage of the total number of registers than the percentage specified by the current value of the *ilm_ignore_percentage* variable (default 25). (For example, for the default value of 25, a port's fanout is ignored if the port fans out to 25% or more of the total number of registers in the design.) This message informs you that the specified port's fanout will be ignored.

What Next

This is an informational message only; if it is acceptable to you that the specified port is on the ignore list, no action is required on your part. Otherwise, you can query the current value of the *ilm_ignore_percentage* variable by executing the following:

```
pt_shell printvar ilm_ignore_percentage
```

If you want to set the variable to a higher or lower threshold percentage, execute the following:

```
pt_shell set ilm_ignore_percentage new_value
```

See Also

- identify_interface_logic
- ilm_ignore_percentage

ILM-007

(Warning) -auto_ignore, -context_borrow, -latch_level options do not have any affect while generating a critical pins interface logic model.

Description

You receive this message if you execute the *identify_interface_logic* command with the *-critical_pins* option along with one of *-auto_ignore, -context_borrow or -latch_level* options. These options do not make sense while generating a critical pins interface logic, and will be ignored.

What Next

This is a warning message only, no action is required on your part. To get rid of the warning, rerun *identify_interface_logic* without specifying the above options.

Feedback

See Also

- identify_interface_logic

ILM-008

(Information) The use of -include_all_net_pins option to identify_interface_logic is recommended when you extract a critical pins ILM .

Description

You receive this message if you execute the *identify_interface_logic* command with the *-critical_pins* option (that means you are extracting a critical pins ILM), and did not issue the *-include_all_net_pins* option. This message informs you that the usage of *-include_all_net_pins* option is recommended when extracting a critical pins ILM. There can be certain constraints in the design that do not work properly if you do not give the *-include_all_net_pins* option.

What Next

This is an informational message only; if you know that this option does not affect your design, you can ignore this message. Otherwise, redo the *identify_interface_logic* command by giving the *-include_all_net_pins* option.

See Also

- identify_interface_logic

ILM-009

(Warning) There are some input/output delays defined with respect to an internal clock '%s'.

Description

You receive this message if the *write_ilm_script* command encounters input/output delays defined with respect to an internal (non-ilm) clock. The clock is deleted because none of the sources of the clock are ILOGIC pins.

What Next

Try to fix the input/output delays generated in the script to take care of this problem. Alternatively, rewrite your original delays with respect to ILM clocks.

See Also

- write_ilm_script

Feedback

ILM-010

(Error) -ignore_boundary_pins can only be used with -instances option.

Description

You receive this message if the *create_ilm* command is invoked with *-ignore_boundary_pins* option without using the *-instances* option. The *-ignore_boundary_pins* can be used to ignore the input boundary pins of an instance when an instance ILM is being extracted.

What Next

If you want to extract instance ILM, use the -instances option. Otherwise, drop the *-ignore_boundary_pins* option.

See Also

- create_ilm

ILM-011

(Information) Context for block '%s' has been created in directory %s.

Description

You receive this message to inform you that the create_si_context command has created a context for the block in the specified directory.

What Next

No action required.

See Also

- create_si_context

ILM-012

(Information) ILM for block/design '%s' has been created in directory %s.

Description

You receive this message to inform you that the *create_ilm* command has created an ILM for the block/design in the specified directory.

Feedback

What Next

No action required.

See Also

- create_si_context

ILM-013

(Error) Option -instances must be used along with -top_inst.

Description

You receive this message if you call *create_si_context* command with *-top_inst* argument without specifying the *-instances* option.

What Next

Provide the *-instances* option

See Also

- create_si_context

ILM-014

(Error) No valid instance is found with name '%s'.

Description

You receive this message if the -instances or -top_inst option is used with wrong instance name argument. Either there is no instance with the given name or it refers to a black-box.

What Next

Check the instance name and reissue the command with correct instance names.

See Also

- create_ilm
- create_si_context

ILM-015

(Error) The parent hierarchy of instance '%s' is not '%s'.

Feedback

Description

You receive this message if the *create_ilm* command is issued with inconsitent values to the -top_inst and -instances option. The top instance specified must be the parent hierarchy for all the instances specified via -instances option.

What Next

Check the instance names and reissue the command with correct instance names.

See Also

- create_ilm

ILM-016

(Error) The xtalk_pins option cannot be used for criical pins ILM.

Description

You receive this message if the create_ilm command is issued with -critical_pins and -include {xtalk_pins} options. The xtalk_pins option is not currently supported for critical pins ILM.

What Next

Remove the xtalk_pins option and rerun.

See Also

- create_ilm

ILM-017

(error) Value '%s' for option '-include' is not valid. Specify one of: si_delay_pins, si_noise_pins, net_pins, boundary_cells

Description

You receive this message if the *create_ilm* command is issued with *-include* option and the value provided to *-include* is not valid.

What Next

Rerun the command with one of the specified values for *-include* option.

See Also

- create_ilm

Feedback

ILM-018

(Warning) For the values of '-include' option, 'xtalk_pins' is renamed as 'si_delay_pins' and 'noise_pins' is renamed as 'si_noise_pins'. The old names will work for now but will be obsoleted in future.

Description

You receive this message if the *create_ilm* command is issued with *-include* option and the value provided to -include is either xtalk_pins or noise_pins.

What Next

Update your script to replace 'xtalk_pins' with 'si_delay_pins' and 'noise_pins' with 'si_noise_pins'.

See Also

- create_ilm

ILM-019

(Information) Could not find pin '%s' to write annotation.

Description

You receive this message to inform you that the *write_arrival_annotations* command could not find the specified pin in the design. No annotations are written out for this pin.

What Next

No action required.

See Also

- write_arrival_annotations

ILM-020

(warning) Parasitics on port net %s can not be maintained.

Description

You receive this message to inform you that the create_si_context command cannot create port parasitics for the given net in the block wrapper being generated.

Feedback

What Next

No action required.

See Also

- create_si_context

ILM-021

(warning) Net connected to port %s is eliminated as aggressor in block wrapper.

Description

You receive this message to inform you that the create_si_context command removed the given port net as an aggressor to nets inside the block for which the wrapper is being generated.

What Next

No action required.

See Also

- create_si_context

ILM-022

(error) -validate is used in an old version of modeling.

Description

You receive this message to inform you -validate option is used in an old version of modeling. The version of modeling is specified by variable *hier_modeling_version*. If it is less than 2.0, -validate option cannot be used.

What Next

Set the variable *hier_modeling_version* to 2.0 to allow the automatic model validation.

ILM-023

(Warning) Clock %s in clock group %s is defined at a port. This clock group will be skipped in the instance script.

Feedback

Description

You receive this message to inform you: some clocks in a clock group are defined at ports, and they are assumed to be clocks at the top level, thus this clock group will not be written into the instance script. Users need to use *set_clock_groups* command at the top level to redefine this clock group.

ILM-024

(Warning) The master source pin of generated clock %s is a dangling hierarchical pin. Ignoring this clock.

Description

You receive this message to inform you: the master source pin of that generated clock is a hierarchical pin not connected to any leaf pins; since ILM is flat, this hierarchical pin does not exist in the ILM, and this clock is not created in the instance script of ILM.

ILM-025

(error) *create_ilm* is not supported when *set_advanced_analysis* is executed.

Description

You receive this message to inform you *create_ilm* is not supported when *set_advanced_analysis* is executed.

What Next

Do not execute *set_advanced_analysis* before *create_ilm*.

IMSA

IMSA-001

(error) Command option %s is not supported in IMSA mode.

Description

The command option is not supported in the Interactive Multi-Scenario Analysis (IMSA) mode. You enter this mode by restoring a session saved with the *save_session -only_timing_paths ...* command.

Feedback

What Next

Check your command options and remove the unsupported option. To exit the IMSA mode, use *remove_design command.*

INT

INT-1

(fatal) Unknown interrupt signal '%d' encountered.

INT-2

(information) Interrupting current command.

INT-3

(information) One more interrupt will exit process.

INT-4

(information) Process terminated by interrupt.

INT-5

(information) Preparing to interrupt optimization...

Description

This message indicates that a Control-c (SIGINT) was received by the process during the trials phase of compile, and compile is preparing to either print out a menu (interactive mode) or to write a checkpoint file (background mode). Compile must finish the current transform before the menu or checkpoint file can be written. It may take a few minutes to finish the current transform, so please wait until you see that the checkpoint file has been written before hitting Ctrl-C again.

What Next

No action is required on your part. If you want to abort the current compile, hit Control-c twice.

Feedback

INT-6

(information) Aborting optimization...

Description

This message indicates that two Control-c signals (SIGINT) were received by the process after the Delay Optimization phase of compile, so compile will abort. *compile* will end optimization and return the design in its current state.

What Next

No action is required on your part. If you want to abort the process, press Control-c three times.

INT-7

(information) Ignoring interrupt signal since the design is being mapped. One more interrupt will abort optimization without transferring the design...

Description

This message indicates that one Ctrl-C signal (SIGINT) was received by the process before the Delay Optimization phase of compile. Since the design is being mapped, compile will ignore the first interrupt signal. The second Ctrl-C will abort compile and not write out the design.

If you want to abort the process, then hit Ctrl-C three times in a row.

INT-8

(information) Aborting optimization without transferring the design...

Description

This message indicates that two Ctrl-C signals (SIGINT) were received by the process before the Delay Optimization phase of compile, so compile is going to abort. Compile will end optimization but not return the design in its current state because the design has not been fully mapped.

If you want to abort the process, then hit Ctrl-C three times in a row.

Feedback

INTERCONNECT

INTERCONNECT-001

(error) The field %s (line number %d) has already been specified for the current table. The current table will be ignored and the token will be treated as the begining of a new table.

Description

This error occurs when a field is specified more than once for a given table.

What Next

Correct the table syntax by ensuring that each field is only specified once for a given table.

INTERCONNECT-002

(error) The current table (line number %d) is missing one or more fields.

Description

This error occurs when a table is found without the required number of fields.

What Next

Correct the table syntax by adding the missing fields to the file.

INTERCONNECT-003

(Error) Expected to find a valid field name but found %s (line number %d).

Description

This error occurs when the parser cannot find a valid field name.

What Next

Correct the table syntax by ensuring that each field is specified in the format name: data where name is one of version, corner_name, object_spec, delay_type, layer_name, area, table_min_sigma, table_max_sigma, table_meanshift, table_stdev.

INTERCONNECT-004

(error) Cannot specify '%s' for field '%s' (line number %d).

Feedback

Description

The data found in the interconnect file is not valid for the given field.

What Next

Check the interconnect side-file spec to see allowed values for the field, and update the file appropriately.

INTERCONNECT-005

(error) The version '%s' is not valid. Allowable versions are '%s'

Description

An invalid version number has been specified.

What Next

Check the version number.

INTERCONNECT-006

(error) Size of %s table (%d) does not match the size of %s table (%d).

Description

The size of all tables must match the size of area and/or model_name tables.

What Next

Correct the size of the table.

INTERCONNECT-007

(error) Could not find the specified interconnect file.

Description

The interconnect file could not be found.

What Next

Correct the name and path of the interconnect file.

INTERCONNECT-008

(error) An interconnect file version must be specified.

Feedback

Description

The version number is used for backward compatibility purposes if the interconnect file format changes in the future. It can affect the analysis results.

What Next

Specify the version of the interconnect file on the first line of the interconnect file. For example:

```
version:1.0
```

INTERCONNECT-009

(error) Negative values are not allowed for %s.

Description

Negative values are not allowed for the area, sigma, and stdev tables.

What Next

Remove negative values from the interconnect file.

INTERCONNECT-010

(error) Cannot replace a table read with the new format with a table that has been read with the old format.

Description

Tables read with the new format take precedence over those read with the old format.

What Next

Update the tables to use the new format.

INTERCONNECT-011

(error) The min and max sigma tables must be of the same size and the corresponding area tables must be identical.

Description

Min and Max sigma tables read with the old format must have the same size and the corresponding area tables must be identical.

What Next

Fix the tables, or switch to the new side-file format.

INTERCONNECT-012

(error) The layer map could not be found. Any layer-specific via variation tables will be ignored.

Description

The SPEF's layer-map is needed to map the layer-name to the layer-id.

What Next

Check the SPEF for the missing layer-map.

INTERCONNECT-013

(warning) The layer-name %s could not be found in the layer-map; the corresponding tables will be ignored.

Description

The layer-name in the interconnect side-file must be in the SPEF's layer-map.

What Next

Check the SPEF for the missing layer-name or the interconnect side-file for the incorrect layer-name.

INTERCONNECT-014

(warning) The layer-name %s does not have a corresponding interconnect side-file. The design-level side-file will be used if available.

Description

No interconnect side-file has been read for the specified layer-name in the SPEF's layer-map.

What Next

Check for the missing interconnect side-file for the specified layer-name.

Feedback

INTERCONNECT-015

(error) Via model name %s cannot be mapped to any Via model read from parasitics. Ignoring 'model_name' row of the table.

Description

The Via model names specified in the IVM file should match with the Via model names defined in the parasitics file.

What Next

Check for inconsistency of the model names and fix it.

INTERCONNECT-016

(error) Failed to read IVM table from file '%s'. IVM table refers to via models, but parasitics data has no VIA_MODEL_NAME_MAP.

Description

To use model names in IVM table, the parasitics files read should have VIA_MODEL_NAME_MAP.

What Next

Check if the parasitics files read have VIA_MODEL_NAME_MAPs defined in the correct syntax. Look for any corresponding PARA-XXX errors and fix them.

IR

IR-001

(error) %s is not a valid supply voltage value for net %s

Description

This error indicates that an invalid supply voltage value is assigned to supply net in *-supply_net_voltages* option of *set_update_rail_options* command.

What Next

Please make sure the supply voltage value is a float number.

Feedback

LBDB

LBDB-1

(error) The '%s' function requires %d arguments.

Description

This message indicates that the number of arguments passed to the specified function or the complex attribute is wrong. The Library Compiler expects a specific number of arguments for various functions and complex attributes. For example, the define_cell_area and the capacitive_load_unit require two arguments. A common cause of this error is the argument's syntax definition. For example, the pin_equal complex attribute requires one quoted string as an argument instead of multiple strings

```
pin_equal("Q", "XQ");   wrong
        pin_equal("Q" "XQ");    wrong
        pin_equal("Q XQ");      correct
```

The following example shows an instance where this message occurs:

```
/* Try the wrong number of arguments to these functions. */
  define_cell_area(my_area,pad_slots,extra_junk);
  capacitive_load_unit(1, pf, pf);
```

The following is an example message:

```
Error: Line 23, The 'define_cell_area' function requires 2 arguments.
 (LBDB-1)
```

What Next

Change the technology library to correct the number of arguments. Refer to the "Library Compiler Reference Manual" for the syntax description.

LBDB-2

(error) The value of argument %d of the '%s' function\n \tis of the wrong type. A value of '%s' type is required.

Description

This message indicates that the wrong value type has been set to the specified function argument. A common cause of this error is the alteration of argument order. For example, the capacitive_load_unit attribute expects a floating-point value then a unit of string type.

```
capacitive_load_unit( pf, 1);    wrong
  capacitive_load_unit( 1, pf);    correct
```

Feedback

The following example shows an instance where this message occurs:

```
capacitive_load_unit( pf, 1);
```

In this case, the arguments of the capacitive_load_unit need to be switched.

The following is an example message:

```
Error: Line 17, The value of argument 1 of the 'capacitive_load_unit'
 function
        is of the wrong type. A value of 'floating-point' type is
 required. (LBDB-2)
```

What Next

Change the technology library to correct the arguments. Refer to the "Library Compiler Reference Manual" for the syntax description.

LBDB-3

(error) The '%s' value is invalid for the '%s' attribute.\n \tIts valid values are %s.

Description

This message indicates that the specified string value is not included in the list of accepted values. This error is often caused by a typo in the valid enumerated string value.

The following example shows an instance where this message occurs:

```
default_wire_load_mode : enclose;
```

In this case, the value should be 'enclosed'.

The following is an example message:

```
Error: Line 15, The 'enclose' value is invalid for the
 'default_wire_load_mode'
attribute.
        Its valid values are top, segmented and enclosed. (LBDB-3)
```

What Next

Change the technology library to correct the invalid value.

LBDB-4

(error) The %s '%s' cannot be specified during\n \tthe update_lib command.

Feedback

Description

Only library-level group statements can be added to an existing library using the update_lib command.

This message indicates that an invalid data (function, attribute, or group) has been found in the library to be added.

The following example shows an instance where this message occurs: Existing library

```
default_wire_load_mode      : top;
```

You cannot specify the default_wire_load_mode attribute to be added to an existing library.

The following is an example message:

```
Error: Line 8, The group 'default_wire_load_mode' cannot be specified
 during
        the update_lib command. (LBDB-4)
```

What Next

Check the "Library Compiler User Guide" for valid data that can be added to existing libraries. Change the library to be updated appropriately.

LBDB-5

(error) The library already has a '%s' attribute. It cannot be\n \toverwritten during the update_lib command.

Description

Only library-level group statements can be added to an existing library using the update_lib command.

This message indicates that an attribute has been found in the library to be added.

What Next

Remove the existing attribute from the technology file.

LBDB-6

(error) The library already has a '%s' group; it cannot be\n \toverwritten during the update_lib command because it is permanent.

Description

This message indicates that an existing group is being overwritten in the library; the existing group is permanent. You cannot overwrite existing groups because their

Feedback

definitions might already have affected subsequent group declarations in the library. You can, however, add new ones.

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
        resistance : 0 ;
        capacitance : 1 ;
        area : 0 ;
        slope : 0.186 ;
        fanout_length(1,0.39) ;
    }
```

The following is an example message:

```
Error: Line 1, The library already has a '05x05' group; it cannot be
       overwritten during the update_lib command because it is permanent.
 (LBDB-6)
```

What Next

Change the library file to either remove the group or modify its name.

LBDB-7

(information) A total of %d repeated messages are omitted.

Description

Repeated messages on buses, bundles, pin "collections" have been removed, only those corresponding to the "first" pins are shown. For the following examples:

bus(a) { bus_type : bit7to0; ... }

bundle (b) { member (x, y, z) ... }

pin (c_4 c_3 c_2 c_1) { /* pin "collections" */ ... }

messages will be shown for pins a[7], x, and c_4. This is shown

Line 330, Cell 'fd1', pin 'a[7]', The attribute 'max_transition' is not specified. (LBDB-605)

but this is omitted:

Line 330, Cell 'fd1', pin 'a[6]', The attribute 'max_transition' is not specified. (LBDB-605)

Note that if you use command suppress_message to suppress a certain warning message, that message is not generated at all, and so is not counted here. Lastly, some repeated messages may still show up, but non-repeating messages are never blocked.

Feedback

What Next

To show all repeated messages, set the following variable before read_lib:

set lc_show_repeated_messages TRUE read_lib ...

LBDB-8

(information) The %s '%s' group has been successfully %s\n \tin the library.

Description

The *update_lib* command updates library groups in a given library. This message is for information purposes only and concerns cell and operating_conditions groups. However, if a wire-load model group is updated in a library, designs using that wire-load model must be reassigned a wire-load model.

The following is an example message:

```
Information: Line 1, The operating_conditions 'BCMIL' group has been
 successfully added
             in the library. (LBDB-8)
Information: Line 8, The cell 'lbdb8' group has been successfully added
             in the library. (LBDB-8)
```

What Next

Use *set_wire_load_model* to set the wire-load model on designs using the modified wire-load models.

LBDB-9

(error) The '%s' function requires %s arguments.

Description

This message indicates that the number of arguments passed to the specified function or the complex attribute is wrong. The Library Compiler expects a specific number of arguments for various functions and complex attributes. For example, the define_cell_area and the capacitive_load_unit require two arguments. A common cause of this error is the argument's syntax definition. For example, the pin_equal complex attribute requires one quoted string as an argument instead of multiple strings

```
pin_equal("Q", "XQ");   wrong
        pin_equal("Q" "XQ");    wrong
        pin_equal("Q XQ");      correct
```

Feedback

The following example shows an instance where this message occurs:

```
/* Try the wrong number of arguments to these functions. */
  define_cell_area(my_area,pad_slots,extra_junk);
  capacitive_load_unit(1, pf, pf);
```

The following is an example message:

```
Error: Line 23, The 'define_cell_area' function requires 2 arguments.
 (LBDB-9)
```

What Next

Change the technology library to correct the number of arguments. Refer to the "Library Compiler Reference Manual" for the syntax description.

LBDB-10

(error) Invalid character '%s' is detected in %s name.

Description

This message indicates that you specified an invalid name for the object. For cell, the name cannot contain '/' as it is a reserved character for hierarchy.

What Next

Change the library source file by correcting the name.

LBDB-11

(warning) The same '%s' attribute is defined twice and is ignored the second time.

Description

This message indicates that an attribute has been registered twice. The Library Compiler ignores the second value.

What Next

Make sure that the attribute is defined only once.

LBDB-12

(warning) The '%s' attribute is the wrong type for the '%s' object.

Feedback

Description

This message indicates that an attribute's value had a wrong type. The Library Compiler ignores the value.

What Next

Make sure that the attribute's value is of the correct type.

LBDB-13

(warning) The '%s' enum has been defined twice and is being ignored.

Description

This message indicates that an enumeration value registered with an attribute has been defined twice.

What Next

Make sure that the enumeration value is defined only once.

LBDB-14

(error) The library already has a '%s' group; the library\n \tcannot be overwritten unless the -overwrite option is specified.

Description

This message indicates that a group has already been added by the *update_lib* command, and you are trying to overwrite it using the *update_lib* command again without specifying the -overwrite option.

The following is an example message:

```
Error: Line 2, The library already has a 'lbdb14' group; the library
        cannot be overwritten unless the -overwrite option is specified.
 (LBDB-14)
```

What Next

Either specify the -overwrite option to the update_lib command if you want to overwrite the same group or change the name of the group.

LBDB-15

(warning) an illegal value of '%s' %f is found, it cannot be %s than \ '%s' value '%s %f'.

Feedback

Description

```
This message indicates that the values of capacitance models/attributes
 is not
correct. Note that when you encounter error LBDB-706 as well, then this
 screener
 is one cause for LBDB-706.

the capacitance values should meet the following rule:

Cmiller_rise = miller_cap_rise value
Cmiller_fall = miller_cap_fall value

pin_capacitance = rise_capacitance or fall_capacitance or if missing, use
 pin capacitance

1. Cmiller_rise/fall <= pin_capacitance;
```

The following example shows an instance where this message occurs:

```
pin(I)  {
    direction : input;
    rise_capacitance : 0.00263567;
    ...
    ccsn_first_stage () {
      miller_cap_rise : 0.0477054;
      ...
    }
    ...
  }
```

The following is an example message:

```
Warning: Line 364, Cell 'BUFFD0', pin 'I', an illegal value of
 'miller_cap_rise' 0.047705 is found, it cannot be more than
'capacitance' value '  0.002636'. (LBDB-15)
```

What Next

Change the value of the attributes to meet the screener rules.

LBDB-16

(warning) Found a duplicate %s attribute. Using the latest value.

Description

This message indicates an attribute has been defined twice. The first definition is ignored.

Feedback

The following example shows an instance where this message occurs:

```
pin(Q) {
      direction : output;
      function : "1";
      function : "1";
    }
```

The following is an example message:

```
Warning: Line 59, Found a duplicate function attribute. Using the latest
 value. (LBDB-16)
```

What Next

Remove the duplicate definition of the attribute.

LBDB-17

(error) The library already has a type named '%s'. Type \n \tgroups can never be overwritten.

Description

This message indicates that a type group already exists in the original library, and you are trying to overwrite it using the *update_lib* command again.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

The type named bus2 is defined in the library to be updated and the file used to update.

The following is an example message:

```
Error: Line 1, The Library already has a type named 'bus2'. Type
       groups can never be overwritten. (LBDB-17)
```

What Next

Either remove the type group from the added library or change the name of the group in the file used for update.

Feedback

LBDB-18

(warning) In the '%s' library, the environment attribute \n \t%s's value is out of range.

Description

This message indicates that the nominal source voltage value defined in the library using nom_voltage attribute is less than 0. The library compiler ignores the value and takes the default nominal voltage. For a CMOS library, the default nominal voltage value is 5 volts.

The following example shows an instance where this message occurs:

```
nom_voltage : -5;
```

The following is an example message:

```
Warning: Line 29, In the library 'lbdb18', the environment attribute
        nom_voltage's value is out of range. (LBDB-18)
```

What Next

Change the value of the nom_voltage attribute to be greater than zero.

LBDB-19

(warning) Can't find a pin named '%s' in the '%s' cell.

Description

This message indicates that one of the pin names in the list of the *pin_equal* or *pin_opposite* attribute or *gate_leakage* group is not defined in the cell. This often happens when there is a typo in the pin name.

The following example shows an instance where this message occurs:

```
cell(lbdb19) {
    area : 13;
    pin_opposite("Q","XQ");
    pin(Q, YQ) {
        direction : output;
        function : "1";
    }
  }

cell(lbdb19_1) {
    area : 13;
    pin(Q, YQ) {
        direction : input;
        function : "1";
    }
    leakage_current() {
```

Feedback

```
        gate_leakage(XQ) {
          input_high_value : 7.1;
          input_low_value : -8.7;
        }
    }
  }
```

The following is an example message:

```
Warning: Line 28, Can't find a pin named 'XQ' in the 'lbdb19' cell.
 (LBDB-19)
Warning: Line 218, Can't find a pin named 'XQ' in the 'lbdb19_1' cell.
 (LBDB-19)
```

What Next

Check to see if there is a typo in the pin name. Otherwise, declare the pin in the technology library.

LBDB-20

(warning) Cannot process 'pin_opposite' for the '%s' cell.

Description

This message indicates that the pins used in the list of the *pin_opposite* attribute are not found in the cell.

The following example shows an instance where this message occurs:

```
cell(lbdb20) {
    area : 13;
    pin_opposite("Q","XQ");
    pin(Q, YQ) {
        direction : output;
        function : "1";
    }
    pin(YQ) {
        direction : output;
        function : "0";
    }
  }
```

In this case, the pins defined in the cell are 'Q' and 'YQ'. However, the pins listed in the pin_opposite attribute are 'Q' and 'XQ'.

The following is an example message:

```
Warning: Line 28, Can't process 'pin_opposite' for the 'lbdb20' cell.
 (LBDB-20)
```

Feedback

What Next

Fix the pin names in the list of the pin_opposite attribute.

LBDB-23

(error) There is a missing timing arc between pins '%s' and\n \t'%s' in the '%s' cell.

Description

This message indicates there is a missing timing arc from an input or inout pin to an output pin.

For a combinational cell, the Library Compiler checks that

```
* An output port with a function statement has timing arcs to
          all functionally related inputs
        * An output port with a three_state attribute has timing arcs
          to all three_state related inputs
        * If all timing arcs are conditional, a default timing arc
          without any condition is required.
```

The following example shows an instance where this message occurs:

```
cell(lbdb23) {
    area : 1;
    pin(A) {
      direction : input;
      capacitance : 1;
    }
    pin(B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "(A B)'";
      timing() {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A";
      }
    }
  }
```

In this case, a timing arc is missing between the pin 'Z' and 'B'. To fix the problem, add the following timing group:

```
timing() {
        intrinsic_rise : 1.0;
```

Feedback

```
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "B";
      }

The following is an example message:
Error: Line 12, There is a missing timing arc between pins 'A' and
        'Z' in the 'lbdb23' cell. (LBDB-23)
```

What Next

Add the missing timing group between the two pins.

LBDB-23w

(warning) There is a missing timing arc between pins '%s' and\n \t'%s' in the '%s' cell.

Description

This message indicates there is a missing timing arc from an input or inout pin to an output pin.

For a combinational cell, the Library Compiler checks that

```
* An output port with a function statement has timing arcs to
          all functionally related inputs
        * An output port with a three_state attribute has timing arcs
          to all three_state related inputs
        * If all timing arcs are conditional, a default timing arc
          without any condition is required.
```

The following example shows an instance where this message occurs:

```
cell(lbdb23) {
    area : 1;
    pin(A) {
      direction : input;
      capacitance : 1;
    }
    pin(B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "(A B)'";
      timing() {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
```

Feedback

```
        related_pin : "A";
      }
    }
  }
```

In this case, a timing arc is missing between the pin 'Z' and 'B'. To fix the problem, add the following timing group:

```
timing() {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "B";
      }

The following is an example message:
Warning: Line 12, There is a missing timing arc between pins 'A' and
        'Z' in the 'lbdb23' cell. (LBDB-23w)
```

What Next

Add the missing timing group between the two pins.

LBDB-24

(warning) The '%s' symbol is used but is not defined.

Description

This message indicates that in a symbol library, you assigned an undefined symbol name to a special symbol.

The following example shows an instance where this message occurs:

```
logic_1_symbol : "mylogic_1";
```

In this example, the symbol 'my_logic_1' is not defined. To fix the problem, define the symbol:

```
symbol(mylogic_1) {
    line(0,0,0,1.5);
    line(0,1.5,.5,2);
    line(0,1.5,-.5,2);
    pin(a,0,0,RIGHT);
  }
```

The following is an example message:

```
Warning: Line 38, The 'mylogic_1' symbol is used but is not defined.
 (LBDB-24)
```

Feedback

What Next

Either define the symbol assigned to the special symbol, or correct the name if it is wrong.

LBDB-27

(error) An invalid attribute '%s' is found.

Description

This error message occurs when a bus *function*, *three_state*, or *state_function* attribute value is not valid.

This message is also used to notify you that it is not allowed to specify related_power_power or related_group_pin when a pin is short-pin and doesn't drive any timing arc in the cell.

This message is also used to notify you when the *level_shifter_enable_pin* attribute is not specified for the input pin of a level shifter cell, or when the *isolation_cell_enable_pin* attribute is not specified for the input pin of an isolation cell.

This message is also used to show that the attribute "antenna_diode_related_power_pins" and "antenna_diode_related_ground_pins" specify one or more pg pins that don't exist.

This message is also used to show that the *max_input_delta_overdrive_high* or *max_input_delta_underdrive_high* attribute is not specified for the input or inout pin, or is not specified for power switch, level shifter, macro(memory) or pad cell.

What Next

Correct the value of the attribute and rerun the command.

LBDB-27w

(warning) An invalid attribute '%s' is found.

Description

This warning message occurs when a bus *function*, *three_state*, or *state_function* attribute value is not valid.

This message is also used to notify you that it is not allowed to specify related_power_power or related_group_pin when a pin is short-pin and doesn't drive any timing arc in the cell.

This message is also used to notify you when the *level_shifter_enable_pin* attribute is not specified for the input pin of a level shifter cell, or when the *isolation_cell_enable_pin* attribute is not specified for the input pin of an isolation cell.

Feedback

This message is also used to show that the attribute "antenna_diode_related_power_pins" and "antenna_diode_related_ground_pins" specify one or more pg pins that don't exist.

This message is also used to show that the *max_input_delta_overdrive_high* or *max_input_delta_underdrive_high* attribute is not specified for the input or inout pin, or is not specified for power switch, level shifter, macro(memory) or pad cell.

What Next

Correct the value of the attribute and rerun the command.

LBDB-28

(error) The '%s' attribute is supplied with %d arguments.\n \tOnly %d arguments are expected.

Description

This message indicates that a command or an attribute got the wrong number of arguments.

The following example shows an instance where this message occurs:

```
define("lbdb28", "library", "string", "integer");
```

The following is an example message:

```
Error: Line 61, The 'define' attribute is supplied with 4 arguments.
        Only 3 arguments are expected. (LBDB-28)
```

What Next

Fix the arguments of the attribute.

LBDB-29

(information) The '%s' attribute for %s group is official liberty syntax/already defined, this user define syntax is ignored.

Description

This message indicates that the user's defined attribute has been already defined or it is reserved by Library Compiler. The Library Compiler ignores the second definition. If the attribute has already supported by Library Compiler, the information can be ignored.

The following example shows an instance where this message occurs:

```
define("lbdb29", "pin", "string");
  define("lbdb29", "pin", "integer");
  define("area", "cell", "float");
```

Feedback

The following is an example message:

```
Information: Line 62, The 'lbdb29' attribute for pin group is official
 liberty syntax/already defined, this user define syntax is ignored.
 (LBDB-29)
Information:Line 100, The 'area' attribute for cell group is official
 liberty syntax/already defined, the user define syntax is ignored
 (LBDB-29)
```

What Next

Users can ignore this information safely. or remove the redudant definition to eliminate the message.

LBDB-30

(warning) There is a sequential timing arc with the\n \t%s non-clock pin for a related_pin attribute.

Description

This message warns you if you specified any setup, hold, skew, removal, or edge-triggered timing arcs relative to a nonclock signal.

The following example shows an instance where this message occurs:

```
cell(lbdb30) {
    area : 9;
    pin(D) {
      direction : input;
      capacitance : 1;
      min_pulse_width_high : 1.0;
      min_pulse_width_low : 1.0;
      timing () {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CD";
      }
    }
    pin(CP) {
      direction : input;
      capacitance : 1;
    }
    pin(CD) {
      direction : input;
      capacitance : 1;
    }
    ff("IQ","IQN") {
      next_state : "D";
```

Feedback

```
      clocked_on : "CP";
      clear   : "CD'";
    }
  }
```

The following is an example message:

```
Warning: Line 1828, There is a sequential timing arc with the
        'CP' non-clock pin for a related_pin attribute. (LBDB-30)
```

What Next

Make sure the related_pin value is a clock pin, or modify the timing group.

LBDB-31

(information) The %s group has been successfully %s\n \tin the library.

Description

This message informs you that a group has been successfully added or overwritten in a library using the *update_lib* command.

The following is an example message:

```
Information: Line 1, The type group has been successfully added
        in the library. (LBDB-31)
```

What Next

No action is required.

LBDB-32

(warning) The '%s' group has been defined multiple times in\n \tthe '%s' library. Using the last definition encountered.

Description

The library contains more than one definition of a group. The Library Compiler issues this error message, ignores the previous definitions, and takes into consideration the last definition encountered.

The following example shows an instance where this message occurs:

```
wire_load_selection(lbdb32) {
    wire_load_from_area(27,100,"10x10");
    wire_load_from_area(10,25,"05x05");
  }
  wire_load_selection(lbdb32) {
    wire_load_from_area(27,10,"10x10");
```

Feedback

```
    wire_load_from_area(27,100,"10x10");
    wire_load_from_area(0,28,"05x05");
    wire_load_from_area(2,10,"15x10");
  }
```

The following is an example message:

```
Warning: Line 50, The 'lbdb32' group has been defined multiple times in
         the 'lib' library. Using the last definition encountered.
 (LBDB-32)
```

What Next

Change the group name if it is wrong, or delete the second definition.

LBDB-34

(error) There is a syntax error in the related_bus_pins attribute's value.

Description

This message indicates there is a syntax error in the value of the related_bus_pins attribute. This might be caused by a typo.

The following example shows an instance where this message occurs:

```
related_bus_pins : {ADDR} ;
```

In this case, the 'ADDR' name is between parentheses. To fix the error, place the name between quotes.

The following is an example message:

```
Error: Line 164, There is a syntax error in the related_bus_pins
 attribute's value. (LBDB-34)
```

What Next

Check the "Library Compiler User Guide" for the correct syntax of the value, and fix the technology library source file.

LBDB-35

(warning) Missing a timing arc of timing_type 'three_state_disable'\n \tbetween '%s' and '%s' pins in the '%s' cell.

Description

To describe the transition from 0->Z or 1->Z, use the timing arc with timing_type of *three_state_disable* for the pin with a three_state attribute.

Feedback

The following example shows an instance where this message occurs:

```
cell(BTS4)  {
        area : 3.0;
    pin(Z)  {
      direction : output;
      function : "A";
      three_state : "E";
      timing()  {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A";
      }
      timing()  {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "E";
      }
    }
    pin(A)  {
      direction : input;
        capacitance : 1.0;
    }
    pin(E)  {
      direction : input;
        capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Warning: Line 110, Missing a timing arc of timing_type
 'three_state_disable'
        between 'E' and 'Z' pins in the 'lbfb35' cell. (LBDB-35)
```

What Next

Add the missing timing group between the two pins.

LBDB-36

(error) The '%s' specifies wrong incorrect names.

Description

This error message occurs when incorrect variable names are specified for a ff, ff_bank, latch, latch_bank, or a statetable group. This message also occurs when the number of variables is either less or more than the required number.

Feedback

Examples of incorrect variable names include the following:

- `The group name`

- `An empty string`

The following example shows an instance where this message occurs: The following example causes an error because it uses the variable group name and an empty string:

```
statetable("A", "statetable") {
ff("IQ", "") {

Error: Line 213, The 'statetable' specifies wrong variable names.
 (LBDB-36)
```

What Next

Check the *Library Compiler User Guide* for the correct syntax, and fix the variable names of the group in the technology library.

LBDB-37

(warning) The '%s' layer is defined multiple times:\n \tDeleting the old definition.

Description

The symbol library contains more than one definition of a layer. The Library Compiler issues this warning message, deletes the previous definition, and takes into consideration the last definition encountered.

The following example shows an instance where this message occurs:

```
library("ds.sdb") {

  layer(lbdb37_layer) {
    set_font ("1_25.font");
    visible : TRUE ;
    line_width : 1 ;
    red : 65000 ;
    green : 33000 ;
    blue : 0 ;
  }

  layer(lbdb37_layer) {   /* A duplicate layer. */
    set_font ("1_25.font");
    visible : TRUE ;
    line_width : 1 ;
    red : 65000 ;
    green : 33000 ;
    blue : 0 ;
```

```
  }
 }
```

The following is an example message:

```
Warning: Line 32, The 'lbdb37_layer' layer is defined multiple times:
        Deleting the old definition. (LBDB-37)
```

What Next

In the symbol library file, change the layer name if it is wrong, or delete the second definition.

LBDB-39

(error) The '%s' symbol is defined multiple times.

Description

The symbol library contains more than one definition of a symbol. The Library Compiler issues this error message and deletes all the definitions.

The following example shows an instance where this message occurs:

```
symbol(lbdb39_dot) {
    line( -.25,-.25,.25,-.25);
    line(.25,.25,.25,-.25);
    line(.25,.25,-.25,.25);
    line( -.25,.25,-.25,-.25);
    line( -.25,-.25,.25,.25);
    line(.25,-.25,-.25,.25);
  }

  symbol(lbdb39_dot) {
    line( -.25,-.25,.25,-.25);
    line(.25,.25,.25,-.25);
    line(.25,.25,-.25,.25);
    line( -.25,.25,-.25,-.25);
    line( -.25,-.25,.25,.25);
    line(.25,-.25,-.25,.25);
  }
```

The following is an example message:

```
Error: Line 58, The 'lbdb39_dot' symbol is defined multiple times.
 (LBDB-39)
```

What Next

Change the symbol name if it is wrong, or delete the second definition.

Feedback

LBDB-40

(error) In the '%s' symbol, the '%s' and '%s' pins both\n \thave the '%s' direction and the same Y location.

Description

The symbol library contains more than one pin with the same direction and the same Y location.

The following example shows an instance where this message occurs:

```
symbol("lbdb40") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 1000, 10000, LEFT);
    pin("P1", 8000, 10000, LEFT);
    pin("P2", 8000, 10000, LEFT);
    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
  }
```

The following is an example message:

```
Error: Line 15, In the 'lbdb40' symbol, the 'P2' and 'P0' pins both
        have the 'LEFT' direction and the same Y location. (LBDB-40)
```

What Next

Change the direction or the Y location of any of the pins.

LBDB-41

(error) In the '%s' symbol, the '%s' and '%s' pins both\n \thave the '%s' direction and the same X location.

Description

The symbol library contains more than one pin with the same direction and the same X location.

The following example shows an instance where this message occurs:

```
symbol("lbdb41") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 10000, 1000, DOWN);
    pin("P1", 10000, 8000, DOWN);
    pin("P2", 10000, 8000, DOWN);
    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
```

```
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
  }
```

The following is an example message:

```
Error: Line 15, In the 'lbdb41' symbol, the 'P2' and 'P0' pins both
        have the 'DOWN' direction and the same X location. (LBDB-41)
```

What Next

Change the direction or the X location of any of the pins.

LBDB-42

(error) In the '%s' symbol, the '%s' pin '%s' and\n \tthe '%s' pin '%s' are uncorrectly positioned.

Description

This error indicates that one of the problems is encountered:

```
- Both pin P1 and P2 have same direction and same X and Y locations.
        - The pin P1 has a LEFT direction, the pin P2 has RIGHT
          direction, and P1 and P2 have the same Y location. However
          the X location of P2 is less or equal than to the X location
          of P1.
        - The pin P1 has a UP direction, the pin P2 has DOWN
          direction, and P1 and P2 have the same X location. However
          the Y location of P2 is greater or equal than to the Y location
          of P1.
```

The following example shows an instance where this message occurs:

```
symbol("lbdb41") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 10000, 1000, DOWN);
    pin("P1", 10000, 8000, DOWN);
    pin("P2", 10000, 8000, DOWN);
    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
  }
```

The following is an example message:

```
Error: Line 41, In the symbol 'lbdb42', the 'DOWN' pin 'P2' and
        the 'DOWN' pin 'P1' are uncorrectly positioned. (LBDB-42)
```

Feedback

What Next

Change the direction or the locations of any of the pins.

LBDB-43

(error) The '%s' pin is defined multiple times in the '%s' symbol.

Description

The symbol library contains more than one definition of a pin in the specified symbol. The Library Compiler issues this error message and deletes all the definitions.

The following example shows an instance where this message occurs:

```
symbol("lbdb43") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 10000, 1000, DOWN);
    pin("P0", 10000, 1000, DOWN);
    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
  }
```

The following is an example message:

```
Error: Line 44, The 'P0' pin is defined multiple times in the 'lbdb43'
 symbol. (LBDB-43)
```

What Next

Change the pin name if it is wrong, or delete the second definition.

LBDB-46

(error) Found an invalid rotation.

Description

This message indicates that the specified string value for the pin's rotation is not included in the list of accepted values. This error is often caused by a typo in the valid enumerated string value.

What Next

Change the symbol library to correct the invalid rotation value. The valid values of the rotation are ANY_ROTATION, LEFT, RIGHT, UP, or DOWN.

Feedback

LBDB-47

(error) The '%s' cell's pin '%s' has a timing arc that has\n \t%d matched timing arcs on the scaled_cell(%s,%s).

Description

Each timing arc in the regular cell should have a matched timing arc on the same pin in the scaled_cell group. This message indicates that more than one such matching timing arc has been found in the library source.

The following example shows an instance where this message occurs:

```
library(lbdb47) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
    }

    cell(AND) {
      area : 1;
      pin(A B) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A B";
        timing() {
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          slope_rise : 0.0;
          slope_fall : 0.0;
          related_pin : "A B";
        }
      }
    }

    scaled_cell(AND,WCCOM) {
      area : 1;
      pin(A B) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A B";
        timing() {
```

Feedback

```
            intrinsic_rise : 0.1;
            intrinsic_fall : 0.1;
            rise_resistance : 0.1;
            fall_resistance : 0.1;
            slope_rise : 0.0;
            slope_fall : 0.0;
            related_pin : "A";
          }
          timing() {
            intrinsic_rise : 0.3;
            intrinsic_fall : 0.3;
            rise_resistance : 0.3;
            fall_resistance : 0.3;
            slope_rise : 0.0;
            slope_fall : 0.0;
            related_pin : "A ";
          }
        }
      }
    }
```

In this case, The timing arc between 'Z' and 'A' is defined once in the 'AND' cell and twice in the 'AND' scaled_cell. To fix the problem, remove one the timing arcs.

The following is an example message:

```
Error: Line 42, The 'AND' cell's pin 'Z' has a timing arc that has
       2 matched timing arcs on the scaled_cell(AND,WCCOM). (LBDB-47)
```

What Next

Find the duplicate timing group you do not need, and delete it.

LBDB-48

(error) The '%s' pin has a %s group whose related_pin\n \tis the port itself.

Description

It is not possible to have a timing arc or a power table whose starting point and ending point are the same.

The following example shows an instance where this message occurs:

```
cell(lbdb48) {
      area : 1.0;
      pin ( O ) {
        direction : output;
        function : "1";
        timing() {
          timing_sense : non_unate;
          related_pin : "O";
```

```
            rise_resistance : 0.1;
            fall_resistance : 0.1;
            intrinsic_rise : 5.0;
            intrinsic_fall : 0.0;
          }
        }
      }
```

The following is an example message:

```
Error: Line 43, The 'O' pin has a timing group whose related_pin
       is the port itself. (LBDB-48)
```

What Next

Check the timing arc or the internal power group, and make the appropriate correction.

LBDB-49

(error) No '%s' attribute has been specified for the\n \tlibrary. This attribute is needed in %s libraries.

Description

This message indicates that you did not specify any of the following attributes in the physical library.

```
* distance_unit
        * capacitance_unit
        * resistance_unit
```

The following example shows an instance where this message occurs: Add any of the following examples of attributes to the library:

```
distance_unit : "1um";
```

The following is an example message:

```
Warning: No 'distance_unit' attribute has been specified for the
         library. This attribute is needed in technology libraries.
 (LBDB-49)
```

What Next

Add the missing attribute to the library source file.

LBDB-50

(error) In the '%s' cell, the '%s' input pin has a 'function' attribute.

Feedback

Description

This message indicates that a pin declared as an input, implicitly by omitting the direction or explicitly where the direction is set to input, has a function attribute. Only output and inout ports can have a function attribute.

The following example shows an instance where this message occurs:

```
pin(Q) {
        function : "1";
    }
```

In this case, the direction of 'Q' is set implicitly to 'input' and 'Q' has a function statement defined. To fix the problem, either set the direction explicitly to 'output' or 'inout', or delete the function attribute.

The following is an example message:

```
Error: Line 55, In the 'lbdb50' cell, the 'Q' input pin has a 'function'
 attribute. (LBDB-50)
```

What Next

Either change the direction of the port or remove the function attribute.

LBDB-51

(warning) No '%s' attribute has been specified for the\n \t%s library. It is set to default value '%s'.

Description

This message indicates that you did not specify any of the following attributes in the physical library. And a default value has been assigned.

```
* time_unit
```

The following example shows an instance where this message occurs: Add any of the following examples of attributes to the library:

```
distance_unit : 1um ;
```

The following is an example message:

```
Warning: No 'time_unit' attribute has been specified for the
         library. It is set to default value '1ns'. (LBDB-51)
```

What Next

Make sure the default value is the desired value.

Feedback

LBDB-53

(error) The '%s' attribute, which expects values of %s type,\n \tis being supplied a value of %s type.

Description

This message indicate that the attribute has been supplied with the wrong value. Library Compiler ignores the value.

The following example shows an instance where this message occurs:

```
dont_touch : 1;
```

In this case, the 'dont_touch' attribute expects a boolean value such as true or false.

The following is an example message:

```
Error: Line 53, The 'dont_touch' attribute, which expects values of
 boolean  type,
       is being supplied a value of integer type. (LBDB-53)
```

What Next

Check the "Library Compiler User Guide" for the correct type of attribute, and change the value accordingly.

LBDB-54

(error) The define attribute has an invalid '%s' type.\n \tThe valid types are 'string', 'integer', 'float', and 'boolean'.

Description

This message indicates that an invalid type is specified for the define attribute. Library Compiler ignores the invalid type.

The following example shows an instance where this message occurs:

```
library(lbdb54) {
  define( "glorp","library","my_type" );
}
```

The following is an example message:

```
Error: Line 2, The define attribute has an invalid 'my_type' type.
       The valid types are 'string', 'integer', 'float', and 'boolean'.
 (LBDB-54)
```

Feedback

What Next

Change the type to string, integer, float, or boolean in the library.

LBDB-55

(error) The '%s' technology license is not installed.

Description

This message indicates that the specified technology license is missing during a read_lib command. Given the technology, the missing license feature is matched as follows:

```
* CMOS technology needs a Design-Compiler feature.
        * FPGA technology needs an FPGA-Compiler feature.
```

If your site is without a valid technology license, the library is read in, and all functional information is removed. All cells are black boxes, and optimization with this library is disabled.

The following is an example message:

```
Error: Line 2, The 'cmos' technology license is not installed. (LBDB-55)
```

What Next

Make sure that you have a license and that the license is properly installed before next trying to read the specified technology library.

LBDB-57

(error) The 'generic' technology can only be read by Synopsys.

Description

The generic technology library supplies simple combinational and sequential cells that are useful for technology-independent component instantiation. This message indicates that you specified 'generic' as the technology type in the technology library source file. This technology type is reserved for Synopsys generic technology library. Only Synopsys is allowed to compile a generic technology library.

What Next

Do not use 'generic' as the technology type in your technology library source. Choose the correct technology type from current supporting types, for example, CMOS or FPGA.

Feedback

LBDB-58

(warning) The '%s' pin is a multicell_pad_pin, but\n \tit has no connection_class information.

Description

This message indicates that you have a pin in a multicell pad with the multicell_pad_pin attribute defined but the connection_class attribute is missing.

If your library uses multicell pads, Design Compiler needs to know which pins on the various cells to connect to implement the pad properly. Two attributes give this information:

```
* The multicell_pad_pin attribute identifies the pins to
          connect to create a working multicell pad. Use this
          attribute to flag all the pins to connect on a pad or an
          auxiliary pad cell.
        * The connection_class attribute indicates the pins
          to be connected to pins on other cells.
```

The following example shows an instance where this message occurs:

```
cell (lbdb58) {
      pad_cell : true;
      area : 0.0;
      pin (A) {
        direction : input;
        capacitance : 1.0;
        fanout_load : 1.0;
      }
      pin (GZ) {
        direction : input;
        capacitance : 1.0;
        fanout_load : 1.0;
      }
      pin(Y) {
        direction : output;
        capacitance : 1.0;
        driver_type : open_drain;
        is_pad : true;
        multicell_pad_pin : true;
        slew_control : low;
        drive_current : 1.0;
        output_voltage  : STD_CMOS;     /* defined in the library */
        function : "A";
        three_state : "GZ";
        timing () {
          intrinsic_rise   : 0.0;
          rise_resistance  : 0.0;
          intrinsic_fall   : 1.0;
          fall_resistance  : 0.1;
          related_pin      : "A";
```

Feedback

```
        }
        timing () {
          intrinsic_rise   : 0.0;
          rise_resistance  : 0.0;
          intrinsic_fall   : 1.0;
          fall_resistance  : 0.1;
          related_pin      : "GZ";
        }
        max_transition : 0.1;
      }
    }
```

In this case, the 'Y' pin has the multicell_pad_pin attribute defined. To fix the problem, add the connection_class attribute.

The following is an example message:

```
Warning: Line 41, The 'Y' pin is a multicell_pad_pin, but
         has no connection_class information. (LBDB-58)
```

What Next

Add the connection_class attribute to the specified pin.

LBDB-59

(error) The '%s' found in the %s\n \tattribute is invalid.

Description

This message indicates that the specified pin, bus, or bundle name defined in a related_inputs or related_outputs attribute does not exist in the library.

The following example shows an instance where this message occurs:

```
/* Specify non-existence output pin */
  internal_power(lbdb59) {
    values("0.1, 1.2, 0.3, 0.4");
    related_outputs : "X";
  }
```

The following is an example message:

```
Error: Line 46, The 'X' found in the related_inputs or related_outputs
        attribute is invalid. (LBDB-59)
```

What Next

Add the port definition if it is missing in the library, or fix the name if it is a typographical error.

Feedback

LBDB-60

(warning) The wire_load or wire_load_table '%s' group has no\n \t'%s'. Using the default value of (%d, %3.1f).

Description

This message indicates that the specified attribute is not specified in the wire_load or wire_load_table group. The default value of the attribute is used. The missing attribute can be

```
* A fanout_length
        * A fanout_capacitance
        * A fanout_resistance
        * A fanout_area
```

The following example shows an instance where this message occurs:

```
wire_load_table("lbdb60") {
      fanout_length(1, 0.2) ;
      fanout_resistance(1, 0.17) ;
      fanout_area(1, 0.2) ;
    }
```

In this case, the fanout_capacitance is missing in the wire_load_table. If you do not want the default value, add the following attribute:

```
fanout_capacitance(1, 0.15);
```

The following is an example message:

```
Warning: Line 10, The wire_load or wire_load_table 'lbdb60' group has no
        'fanout_capacitance'. Using the default value of (1, 0.0).
 (LBDB-60)
```

What Next

If you do not want to apply the default to the attribute indicated in the warning message, specify the attribute in the indicated group.

LBDB-61

(warning) Template '%s' is defined in old library syntax.

Description

This message indicates that a special symbol in the symbol library file is written using an old library syntax.

Feedback

What Next

Check the "Library Compiler User Guide" for the correct syntax of symbols.

LBDB-62

(error) The '%s' symbol is a duplicate '%s' template.

Description

This message indicates that the specified symbol is a duplicate symbol in the symbol library file. Library Compiler ignores the duplicate symbol.

What Next

Remove the duplicate symbol from the symbol library, or change the name if it is a typo.

LBDB-66

(error) The '%s' attribute cannot be supplied a \n \tnonpositive value (%f).

Description

This message indicates that the specified attribute cannot have a nonpositive value.

The following example shows an instance where this message occurs:

```
capacitive_load_unit( -1,pf );
```

The following is an example message:

```
Error: Line 18, The 'capacitive_load_unit' attribute cannot be supplied a
       nonpositive value (-1.000000). (LBDB-66)
```

What Next

Change the value of the attribute to positive in the technology library file.

LBDB-69

(error) Missing a %s name.

Description

This message indicates that a group name is missing in the technology or symbol library file. The Library Compiler ignores the library.

Feedback

The following example shows an instance where this message occurs:

```
cell() {
    area : 9;
  }
```

The following is an example message:

```
Error: Line 63, Missing a cell name. (LBDB-69)
```

What Next

Add the group name to the technology or symbol library file.

LBDB-70

(Information) The '%s' group under %s group is official liberty syntax/already defined, this user define syntax is ignored.

Description

The technology library contains more than one definition of a define_group attribute with the same name. or the group has already supported by Library Compiler. The Library Compiler issues this information message and deletes all the definitions.

The information can be ignored if the group has already supported by Library Compiler.

The following example shows an instance where this message occurs:

```
define_group(lbdb70, cell);
    define_group(lbdb70, cell);
```

The following is an example message:

```
Information: Line 58, The 'lbdb70' group under cell group is official
 liberty syntax / already defined, this user define syntax is ignored.
 (LBDB-70)
```

What Next

Users can ignore this information safely. or remove the redudant definition to eliminate the message.

LBDB-72

(error) Undefined module_pin '%s' referenced in pin_association\n \t'%s' in %s '%s'.

Description

The name given to a pin_association group within a binding group or a state group names a pin that must be defined by a pin group within the module. This error arises when the

Feedback

name given to the pin_association group does not have a corresponding pin group on the module. For example, in the following synthetic library, the pin_association group named 'MY_B' attempts to bind the operator pin 'B' to the module pin 'MY_B'. However, the pin 'MY_B' is not defined for the module, which causes an error to occur.

```
library (example.sldb) {
   module (my_module) {
      design_library : "MYLIB";
      parameter(width) {
         hdl_parameter : TRUE;
      }
      pin (MY_A) {
         direction : input;
         bit_width : "width";
      }
      pin (MY_Z) {
         direction : output;
         bit_width : "width";
      }
      binding (b1) {
         bound_operator : "ADD_UNS_OP";
         pin_association(MY_A) { oper_pin : A ; }

         /* The following line creates an error: */
         pin_association(MY_B) { oper_pin : B ; }

         pin_association(MY_Z) { oper_pin : Z ; }
      }
   }
}
```

In this case you can fix the error by adding a pin group to the module:

```
pin (MY_B) {
         direction : input;
         bit_width : "width";
      }
```

What Next

Remove the pin_association group that refers to the nonexistent module pin. Alternately, you can add a module pin group with the name of the referenced pin in the pin_association group.

LBDB-73

(error) The '%s' cell has more than one sequential \n \tfunction (seq, latch, or ff) declaration.

Feedback

Description

This message indicates there is more than one declaration of a sequential function group.

What Next

Leave only one sequential function group declaration; remove the rest of the declarations.

LBDB-74

(error) The %s value, '%s', is either not defined or it is defined after this line.

Description

This error message occurs when the *default_operating_conditions* or *default_wire_load* attribute refers to an undefined the operating_conditions or wire_load group name in the library.

This message can also report the *related_power_rail* attribute references and the undefined power_rail values in the power_supply group.

The following example shows the 05x05 wire_load group defined after the *default_wire_load* attribute and the resulting error message:

```
default_wire_load : 05x05;
  wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

Error: Line 57, The default_wire_load value, '05x05',
has not been defined or it is defined after this line. (LBDB-74)
```

What Next

Check your library to determine if you have defined the group name. If the group name exists in the library, make sure it is defined before it is used.

LBDB-75

(warning) There is an extra timing arc between '%s' and \n \t'%s' pins in the '%s' cell.

Description

Timing arcs are allowed for pins that are related to each other. To be related to each other, the input pin has to be in the *function* or *three_state* attribute of the output/input pin. This message is issued if the timing arc identified between pins does not fall into the

Feedback

categories described previously. Certain output transitions cannot result from a single input pin change when *function*, *three_state*, and *x_function* share input pin, because the x_function takes highest priority. This message is issued when such situation happens.

The following example shows an instance where this message occurs:

```
pin(Z) {
      direction : output;
      function : "B";
      timing() {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A";
      }
   }
```

In this case, you defined a timing arc between the 'A' and 'Z pins, even though the 'A' pin is not functionally related to the 'Z' pin. Either remove the timing arc or change the function statement of 'Z' to include 'A'.

This is another example involving x_function:

```
pin(out) {
      direction : output ;
      function : "a0&s0 | a1&s1 | a2&s2" ;
      max_capacitance : 0.09 ;
      min_capacitance : 0.01 ;
      output_voltage : default ;
      x_function : "!(s0&!s1&!s2|!s0&s1&!s2|!s0&!s1&s2)" ;

      timing() {
        related_pin : "s0" ;
        sdf_cond : "a0===1'b0 && a1===1'b0 && a2===1'b1" ;
        timing_sense : negative_unate ;
        timing_type : combinational ;
        when : "!a0&!a1&a2" ;
      }
```

In this case, 's0', 's1' and 's2' are used in both function and x_function, no isolated change on 's0' can cause 01 or 10 transition on 'out', a timing arc from 's0' to 'out' requires simontaneous change of 's1' or 's2', LBDB-75 will warn on a timing arc from 's0' to 'out', and similarly, warn on timing arc from 's1' or 's2' as well.

The following is an example message:

```
Warning: Line 73, There is an extra timing arc between 'A' and
        'Z' pins in the 'lbd75' cell. (LBDB-75)
```

Feedback

What Next

Check your library to see whether you have generated the timing group by mistake, whether the related_pin field is wrong or the function attribute value is not recognized.

LBDB-76

(error) The '%s' %s cannot be specified here.

Description

This message indicates that you specified an attribute outside its context. When processing the current context, Library Compiler flags invalid attributes.

It can also be used to indicate that you have specified an attribute/groups which conflicts with the other attributes/groups of the object. For example, if you specify 'io_type' attribute on a cell in the FPGA library which is based on fpga_isd information, the LBDB-76 will be issues and the 'io_type" attribute should be removed.

Another example is when ocv_centile_cell_rise|fall, ocv_centile_rise|fall_transition defined under a timing group, "sigma_type" attribute can NOT be defined for ocv_sigma_cell_rise|fall and ocv_sigma_rise|fall_transition under the same timing group.

The following example shows an instance where this message occurs:

```
pin(D) {
      direction : input;
      capacitance : 1.0;
      current_unit : "1mA";
    }
```

In this case, the 'current_unit' attribute is defined at the pin level. To fix the problem, move the attribute to the library context.

The following is an example message:

```
Error: Line 69, The 'current_unit' attribute cannot be specified here.
 (LBDB-76)
```

What Next

Change the technology library source file to either delete the specified attribute or move the attribute to its correct context.

LBDB-79

(error) The 'ripped_pin' name is not defined.

Feedback

Description

This message indicates that you specified an undefined pin name for the ripped_pin attribute in a symbol library file.

The following example shows an instance where this message occurs:

```
symbol("lbdb79") {
         ripped_pin : "bus_pin" ;
         ripped_bits_property : "EDIF_property" ;
         line(0 , 50, 50, 0);
         line(50, 0, 0, -50);
         line(-50, 0 , 100, 0);
         pin("wire_pin", 100 , 0 , ANY_ROTATION);
  }
```

In this case, the 'bus_pin' pin is not defined.

The following is an example message:

```
Error: Line 69, The 'ripped_pin' name is not defined. (LBDB-79)
```

What Next

Change the symbol library to either define the pin name before you use it in the ripped_pin attribute or fix the pin name if it is a typo.

LBDB-80

(error) The '%s' port name is either undefined or \n \tits group definition is invalid.

Description

This message indicates that the specified port name is either not defined in the library source file or Library Compiler did not read the port group definition successfully. This might often be caused by a problem in the pin bus or a bundle group definition.

The following example shows an instance where this message occurs:

```
cell (lbdb80) {
    area : 3.0;
    bus (D) {
      bus_type : BUS4;
      direction : input;
      capacitance : 1.0;
    }
    pin (CK) {
      direction : input;
      capacitance : 1.0;
    }
    ff_bank (IQ,IQN,4) {
      next_state : "D" ;
```

```
      clocked_on : "CK";
    }
    pin (Q) {
      direction : output ;
      function : "D[0] CK" ;
    }
  }
```

In this case, the 'BUS4' type is not defined in the library. Thus, the 'D' bus is not recognized, and the next_state value is considered to be not defined. Fix the problem by adding the 'BUS4' type group definition.

The following is an example message:

```
Error: Line 186, The 'D' port name is either undefined or
        its group definition is invalid. (LBDB-80)
```

What Next

Change the library source file to define the port.

LBDB-81

(error) The base type in the type group is invalid.

Description

This message indicates that the specified base_type name in the type group is invalid. This might be caused by a typo in the name. Library Compiler only supports the *array* base_type.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : afrray;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

In this case, there is a typo in the base_type value. change afrray to *array*.

The following is an example message:

```
Error: Line 30, The base type in the type group is invalid. (LBDB-81)
```

What Next

Check the "Library Compiler User Guide" and fix the name of the base_type.

Feedback

LBDB-82

(error) The data type in the type group is invalid.

Description

This message indicates that the specified data_type name in the type group is invalid. This might be caused by a typo in the name. Library Compiler only supports the *bit* data_type.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : array;
    data_type : int;    /* wrong */
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

In this case, the data_type value is invalid. change int to *bit*.

The following is an example message:

```
Error: Line 30, The data type in the type group is invalid. (LBDB-82)
```

What Next

Check the "Library Compiler User Guide" and fix the name of the data_type.

LBDB-83

(warning) The width value in the type group is invalid.\n \tIt is corrected.

Description

This message indicates that the specified *bit_width* value in the type group is invalid. This might be caused by a typo in the value. The Library Compiler ignores the invalid value and computes the real value from the bit_from and bit_to fields.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 3;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

Feedback

In this case, the bit_width value is 3. To fix the problem, change it to 2 (bit_to - bit_from + 1).

The following is an example message:

```
Error: Line 30, The width value in the type group is invalid.
        It is corrected. (LBDB-82)
```

What Next

Change the library file, and fix the value of the bit_width.

LBDB-86

(warning) The downto value in the type group is invalid.\n \tIt is corrected.

Description

This message indicates that the specified *downto* value in the type group is invalid. This might be caused by a typo in the value. The Library Compiler ignores the invalid value and computes the real value from the bit_from and bit_to fields.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : ffalse;
  }
```

In this case, the downto value has a typo, ffalse. To fix the problem, change ffalse to false. The Library Compiler corrects the value by setting to false bit_from value is less than the bit_to value. Otherwise, it is set to true.

The following is an example message:

```
Warning: Line 35, The downto value in the type group is invalid.
        It is corrected. (LBDB-86)
```

What Next

Change the library file, and fix the value of the downto field.

LBDB-87

(error) The type group is missing its 'data_type' field.

Feedback

Description

This message indicates that the data_type field is missing in the type group.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : array;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

To fix the problem, add the data_type statement to the type group.

```
data_type : bit;
```

The following is an example message:

```
Error: Line 28, The type group is missing its 'data_type' field.
 (LBDB-87)
```

What Next

Change the library file, and add the data_type field to the type group.

LBDB-88

(error) The type group is missing its 'base_type' field.

Description

This message indicates that the base_type field is missing in the type group.

The following example shows an instance where this message occurs:

```
type(bus2) {
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

To fix the problem, add the base_type statement to the type group.

```
base_type : array;
```

The following is an example message:

```
Error: Line 28, The type group is missing its 'base_type' field.
 (LBDB-88)
```

Feedback

What Next

Change the library file, and add the base_type field to the type group.

LBDB-89

(error) The '%s' library attribute must be defined\n \tto specify a %s value.

Description

This message indicates that an attribute needed by another group is missing in the library. Examples of attributes are

```
* The input_voltage value needs the voltage_unit attribute
          defined.
        * The slew_control value needs the time_unit attribute
          defined.
        * The drive_current value needs the current_unit attribute
          defined.
```

The following example shows an instance where this message occurs:

```
input_voltage(CMOS) {
    vil          : 0.8 ;
    vih          : 2.0 ;
    vimin        : -0.3 ;
    vimax        : VDD + 0.3 ;
   }
    cell(lbdb89) {
      area : 0.0;
      dont_touch : false;
      dont_use   : false;
      pad_cell : true;
      pin(PAD ) {
        is_pad : true;
        input_voltage : CMOS;
        direction   : input;
        capacitance : 3.0;
        fanout_load : 0.0;
      }
      pin(Y ) {
        direction   : output;
        function    : "PAD";
        max_fanout  : 16.0;
        timing() {
          intrinsic_fall  : 4.0;
          intrinsic_rise  : 4.0;
          fall_resistance : 0.0;
          rise_resistance : 0.0;
          related_pin  :"PAD ";
        }
```

```
      }
    }
```

In this case, add the voltage_unit to the library as follows:

```
voltage_unit : "1V";
```

The following is an example message:

```
Error: Line 14, The 'voltage_unit' library attribute must be defined
       to specify a input_voltage value. (LBDB-89)
```

What Next

Add the missing attribute to the library.

LBDB-90

(error) The type group is defined multiple times.

Description

This message indicates that the type group is defined multiple times in the technology library. This might be caused by a typo.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
  type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 1;
    bit_to : 0;
    downto : true;
  }
```

In this case, rename the second type group to bus2_down.

The following is an example message:

```
Error: Line 36, The type group is defined multiple times. (LBDB-90)
```

Feedback

What Next

Change the library file by either removing the multiple definitions but one or renaming the type groups.

LBDB-91

(warning) The bus naming style format is invalid.\n \tUsing the default format.

Description

This message indicates that you specified an invalid bus_naming_style format. The value must include %s and %d. Library Compiler ignores the invalid value and uses the default style "%s[%d]".

The following example shows an instance where this message occurs:

```
bus_naming_style : "%s$%s";
```

The following is an example message:

```
Warning: Line 28, The bus naming style format is invalid.
        Using the default format. (LBDB-91)
```

What Next

Check the "Library Compiler User Guide" for the correct format of the bus_naming_style and fix the value.

LBDB-92

(error) The bus subscript is out of bounds.

Description

This message indicates that you specified a bus element whose index value falls outside the declared index range of the bus type.

The accessed bus element with an index outside the bus bounds is specified in function, three_state, ff, or latch statements.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
```

Feedback

```
}
cell (lbdb92) {
  area : 31.0;
  bus (D) {
    bus_type : bus2;
    direction : input ;
    capacitance : 1.0 ;
  }
  pin (CK) {
    direction : input ;
    capacitance : 1.0 ;
  }
  ff_bank (IQ,IQN,2) {
    next_state : "D[3]" ;
    clocked_on : "CK" ;
  }
  bus (SO) {
    bus_type : bus2;
    direction : output ;
    function : "IQ" ;
  }
}
```

In this case, the 'D[3]' value assigned to next_state falls outside the bus2 range.

The following is an example message:

```
Error: Line 186, The bus subscript is out of bounds. (LBDB-92)
```

What Next

Either change the bounds of the bus definition so that all subelements that are accessed fall within the range, or correct any bus indexing errors in the source library.

LBDB-93

(error) The bus type is invalid.

Description

This message indicates that you specified a bus name whose bus_type is invalid. This might be caused by an invalid base_type in the type group or a typo in the name. Library Compiler only supports the *array* base_type for bus groups.

The following example shows an instance where this message occurs:

```
type(bus2) {
    base_type : list;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
```

Feedback

```
    downto : false;
  }
  cell (lbdb93) {
    area : 31.0;
    bus (D) {
      bus_type : bus2;
      direction : input ;
      capacitance : 1.0 ;
    }
    pin (CK) {
      direction : input ;
      capacitance : 1.0 ;
    }
  }
```

In this case, the 'list' base_type of the 'bus2' type is invalid. Fix the problem by changing the 'list' to 'array'.

The following is an example message:

```
Error: Line 177, The bus type is invalid. (LBDB-93)
```

What Next

Check the "Library Compiler User Guide" and fix the name of the base_type in the type group, or change the bus type name.

LBDB-94

(warning) The ':' character is used in this bus naming style;\n \tthis makes it impossible to specify ranges of buses using ':'.

Description

This message indicates that you specified a ':' in the string of the bus_naming_style. Library Compiler gets confused because the ':' is used to specify ranges of buses.

The following example shows an instance where this message occurs:

```
bus_naming_style : "%s:%d";
```

The following is an example message:

```
Warning: Line 28, The ':' character is used in this bus naming style;
         this makes it impossible to specify ranges of buses using ':'.
 (LBDB-94)
```

What Next

Change the value of the bus_naming_style attribute in the technology library.

Feedback

LBDB-95

(error) Buses have incompatible widths.

Description

This message indicates that you specified a function or a three_state attribute of a group of buses with a different width.

The following example shows an instance where this message occurs:

```
cell (lbdb95) {
    area : 3.0;
    bus (D) {
      bus_type : bus2;
      direction : input;
      capacitance : 1.0;
    }
    pin (CK) {
      direction : input;
      capacitance : 1.0;
    }
    ff_bank (IQ,IQN,4) {
      next_state : "D";
      clocked_on : "CK";
    }
    pin (SO) {
      direction : output;
      function : "D[0] CK";
    }
  }
```

In this case, the number of bits in the ff_bank, which is 4, is different from the width of the 'D' bus, which is 2. Make sure that both values are the same.

The following is an example message:

```
Error: Line 186, Buses have incompatible widths. (LBDB-95)
```

What Next

Change the library source file to make sure that all buses have the same width.

LBDB-96

(error) The bus type name is missing.

Description

This message indicates that you specified a bus with an invalid a bus_type.

Feedback

What Next

Check the library source file, and correct the bus_type to the bus in the library.

LBDB-97

(error) The bus type of a subelement is missing.

Description

This message indicates that you specified a subelement whose parent is missing a bus type.

What Next

Change the library, and fix the bus type.

LBDB-98

(error) The type group name is not defined.

Description

This message indicates that you specified a bus group with an undefined bus_type name in the technology library. This might be caused by a typo.

The following example shows an instance where this message occurs:

```
cell (lbdb98) {
    area : 3.0;
    bus (D) {
      bus_type : bus2;
      direction : input;
      capacitance : 1.0;
    }
   }
```

In this case, the 'bus2' is not defined in the library. To fix the problem, add the following type group:

```
type(bus2) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 0;
    bit_to : 1;
    downto : false;
  }
```

Feedback

The following is an example message:

```
Error: Line 177, The type group name is not defined. (LBDB-98)
```

What Next

Change the library file by adding the named type group.

LBDB-99

(error) The pin direction is inconsistent with the bus or\n \tthe bundle parent direction.

Description

This message indicates that you specified a member of a bus or a bundle whose direction is different from its parent's direction.

The following example shows an instance where this message occurs:

```
bundle(nets) {
      members(n0, n1, n2, n3);
      direction : inout;
      pin (n0) {
        direction : output;
      }
    }
```

In this case, the 'nets' direction is 'inout', but the 'n0' direction is 'output'.

The following is an example message:

```
Error: Line 199, The pin direction is inconsistent with the bus or
        the bundle parent direction. (LBDB-99)
```

What Next

Change the library to fix the direction of the element, the bus, or the bundle.

LBDB-101

(error) The piece number in piecewise linear mode is negative.

Description

This message indicates that you specified a negative piece number in either delay intercept attributes or pin resistance attributes in CMOS piecewise linear delay model library.

Feedback

The following example shows an instance where this message occurs:

```
piece_define("0 8 15");
        ...
  rise_delay_intercept(-11, "2.2");
```

In this case, the -11 piece number is invalid. To fix the problem, make the piece number 0, 1, or 2 as defined by the piece_define attribute.

The following is an example message:

```
Error: Line 172, The piece number in piecewise linear mode is negative.
 (LBDB-101)
```

What Next

Modify the piece number to match the number of ranges in the piece_define attribute.

LBDB-102

(warning) The '%s' piece is multiply\n \tdefined. Using the first one encountered.

Description

This message indicates that you specified either delay intercept attributes or pin resistance attributes for the same piece number multiple times in a CMOS piecewise linear delay model library. Library Compiler ignores the later definitions.

The following example shows an instance where this message occurs:

```
rise_delay_intercept(1, "2.2");
        rise_delay_intercept(1, "2.2");
```

The following is an example message:

```
Warning: Line 173, The 'rise_delay_intercept(1)' piece is multiply
        defined. Using the first one encountered. (LBDB-102)
```

What Next

Modify the piece number if it is a typo, or remove the second definition.

LBDB-103

(warning) The piece number is greater than the number\n \tdefined with piece_define.

Description

This message indicates that in a CMOS piecewise-linear delay model library you specified a piece number in either delay intercept attributes or pin resistance attributes greater than the number defined in the piece_define attribute.

Feedback

The following example shows an instance where this message occurs:

```
piece_define("0 8 15");
        ...
  rise_delay_intercept(3, "2.2");
```

In this case, the 3 piece number is invalid. To fix the problem, make the piece number 0, 1, or 2 as defined by the piece_define attribute.

The following is an example message:

```
Warning: Line 174, The piece number is greater than the number
        defined with piece_define. (LBDB-103)
```

What Next

Modify the piece number to match the number of ranges in the piece_define attribute.

LBDB-104

(warning) The piecewise linear model is multiply defined.\n Using the first one encountered.

Description

This message indicates that you specified the *piece_define* attribute multiple times in a CMOS piecewise linear delay model library. Library Compiler ignores the later definitions.

The following example shows an instance where this message occurs:

```
piece_define("0 8 15");
  piece_define("0 8 15 25");
```

The following is an example message:

```
Warning: Line 13, The piecewise linear model is multiply defined.
        Using the first one encountered. (LBDB-104)
```

What Next

Remove the second definition of the attribute.

LBDB-105

(warning) The timing arc has a negative %s\n \tspecified. Using the default value.

Description

This message indicates that you specified a negative drive resistance value of pin resistance attributes in a CMOS piecewise linear delay model library. Library Compiler

assigns the *default_rise_pin_resistance* or the *default_fall_pin_resistance* value to the timing arc or the value 0.0 if no default value exists.

The following example shows an instance where this message occurs:

```
rise_pin_resistance(0, "-11.1");
```

The following is an example message:

```
Warning: Line 183, The timing arc has a negative rise_pin_resistance(0)
        specified. Using the default value. (LBDB-105)
```

What Next

Make the drive resistance value positive in the pin resistance attribute.

LBDB-107

(warning) The %s '%s' is defined multiple times\n \tin the library. Using the last one encountered.

Description

This message indicates that the same name has been used for more than one object (for example, cells in a library or pins in a cell). Each object must have a unique name within its scope. In the case of a name conflict, Library Compiler ignores all except the last name encountered during the compilation. The compiled database contains the last object only.

The following example shows an instance where this message occurs:

```
statetable ( "D GN", "Q QB") {
        table : "L/H L : - - : L/H H/L,\
            -   H : - - : N   N";
      }

      statetable ( "D GN", "Q QB") {
        table : "L/H L : - - : L/H H/L,\
            -   H : - - : N   N";
      }
```

The following is an example message:

```
Warning: Line 987, The group 'statetable' is defined multiple times
        in the library. Using the last one encountered. (LBDB-107)
```

What Next

Update the library to give each object a unique name within its scope. Quite often, a typo is responsible for the name conflict.

Feedback

LBDB-110

(warning) In the piecewise linear model, the first piece must\n \thave 0 length.

Description

This message indicates that you specified the first piece range, in the piece_define attribute, not starting from zero. Library Compiler ignores the value, and resets it to zero.

The following example shows an instance where this message occurs:

```
piece_define("1 8 15");
```

The following is an example message:

```
Warning: Line 12, In the piecewise linear model, the first piece must
        have 0 length. (LBDB-110)
```

What Next

Change the first piece range to zero.

LBDB-111

(warning) In the piecewise linear model, a piece length\n \tsmaller than that of the previous piece has been found.

Description

This message indicates that in the piece_define attribute you specified a piece length smaller than the previous one. The Library Compiler ignores the value and resets it to the previous value.

The following example shows an instance where this message occurs:

```
piece_define("0 18 15");
```

The following is an example message:

```
Warning: Line 12, In the piecewise linear model, a piece length
        smaller than that of the previous piece has been found.
 (LBDB-111)
```

What Next

Change the piece ranges to be in ascending order.

Feedback

LBDB-112

(error) The timing arc has only one segment of\n \t'%s'. It must have at least two if \n\ \tpiece_define has more than one piece.

Description

This message indicates that in a CMOS piecewise linear delay model library you specified only one segment in either delay intercept attributes or pin resistance attributes. However, the *piece_define* defines more than one piece.

The following example shows an instance where this message occurs:

```
piece_define("0 8 15");
        ...
        rise_delay_intercept(0, "2.2");
```

In this case, only one rise_delay_intercept attribute is defined. To fix the problem, add two more rise_delay_intercept for piece 1 and 2.

```
rise_delay_intercept(1, "3.3");
        rise_delay_intercept(2, "4.4");
```

The following is an example message:

```
Error: Line 169, The timing arc has only one segment of
       'rise_delay_intercept'. It must have at least two if
        piece_define has more than one piece. (LBDB-112)
```

What Next

Modify the piece number to match the number of ranges in the piece_define attribute.

LBDB-117

(error) A list does not belong here.

Description

This message indicates that you specified a list to an attribute whose type is not a list.

The following example shows an instance where this message occurs:

```
library(lbdb117) {
  cell(c) {
    area : 1.0;
    pin( a ) {
      direction : input;
      capacitance : 1.0;
    }
    pin( b ) {
```

Feedback

```
      direction : output;
      timing() {
        intrinsic_rise : 0.48;
        intrinsic_fall : 0.77;
        rise_resistance : 0.1443;
        fall_resistance : {0.0523,0.0523};
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "a";
      }
    }
  }
}
```

In this case, the 'fall_resistance' attribute has a value of type list. Fix the problem by assigning a single value to the attribute.

The following is an example message:

```
Error: Line 14, A list does not belong here. (LBDB-117)
```

What Next

Correctthe value of the specified attribute.

LBDB-119

(error) The '%s' pin on the %s could not be found on\n \tthe %s. There must be a one-to-one match.

Description

Each pin in the regular cell needs a matched pin in the scaled_cell group. This message indicates that a pin could not be matched in the library source.

The following example shows an instance where this message occurs:

```
library(lbdb119) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
    }
    cell(AND) {
      area : 1;
      pin(A B) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
```

Feedback

```
        function : "A B";
        timing() {
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          slope_rise : 0.0;
          slope_fall : 0.0;
          related_pin : "A B";
        }
      }
    }

    scaled_cell(AND,WCCOM) {
      area : 1;
      pin(A B C) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A B";
        timing() {
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          slope_rise : 0.0;
          slope_fall : 0.0;
          related_pin : "A B";
        }
      }
    }
  }
```

In this case, the 'C' pin exists in the scaled_cell but not in the parent cell.

The following is an example message:

```
Error: Line 100, The 'C' pin on the scaled_cell could not be found on
       the parent cell. There must be a one-to-one match. (LBDB-119)
```

What Next

Add the missing pin in the regular cell, or remove the extra pin in the scaled_cell.

LBDB-120

(warning) Layers are ignored inside symbols.

Feedback

Description

For a symbol library, Library Compiler ignores layer information within a symbol.

The following example shows an instance where this message occurs:

```
symbol(lbdb-120) {
    line( - flag_width / 2, - flag_height / 2, \
       - flag_width / 2, flag_height / 2) ;
    line( - flag_width / 2, flag_height / 2, \
         flag_width / 2, flag_height / 2) ;
    line( flag_width / 2, flag_height / 2, \
         flag_width / 2, - flag_height / 2) ;
    line( flag_width / 2, - flag_height / 2, \
         - flag_width / 2, - flag_height / 2) ;
    text( "Area", - string_length / 2 - char_width / 3, \
         - 0.75 / 2, "constraint_layer") ;
  }
```

In this case, the constraint_layer is used in the symbol.

The following is an example message:

```
Warning: Line 3453, Layers are ignored inside symbols. (LBDB-120)
```

What Next

Remove the layer information from the symbol.

LBDB-121

(error) The '%s' must be defined in a macro cell.

Description

This message is reported when the specified group is defined in a cell not of type macro.

The group pg_setting_definition must be defined in macro cell.

The following is an example message:

```
Error: Line 546, There 'pg_setting_definition" must be defined in a macro
 cell.(LBDB-121)
```

What Next

Change the cell type to macro.

LBDB-122

(error) The %s '%s' is missing required values.

Feedback

Description

This error indicates that the specified group is missing required attribute/group: 1) For a voltage_state_range_list group, at least one voltage_state_range is needed; 2) For a pg_setting_definition group, at least one pg_setting_value is needed; 3) For a pg_setting_definition group, default_pg_setting is needed; 4) For a pg_setting_value group, either pg_pin_condition or pg_setting_condition is needed; 5) For a pg_setting_transition group, either start_setting or end_setting is needed; 6) For a site group, width and height is needed; 7) For a routing_blockage group, either rectangle or polygon is needed; 8) For a routing_blockage group, layer_name is needed; 9) For a base_layer_density_view group, saved_layers is needed. 10) For a derived_layer group, one of and, or, xor, not and resize attribute is needed.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  pg_setting_definition(read) {
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The pg_setting_definition 'read' is missing required
 values. (LBDB-122)
```

What Next

Define the missing group/attribute.

LBDB-123

(error) The state '%s' could not be found for the %s '%s'.

Description

This message indicates that the specified state for pg_pin or pg_setting could not be found in the library.

The following example shows an instance where this message occurs:

```
/* Specify non-existence pg pin state */
  pg_setting_value(lbdb59) {
    pg_pin_active_state(VDD, none);
  }
```

The following is an example message:

```
Error: Line 46, The state 'none' could not be found for the pg pin 'VDD'.
 (LBDB-123)
```

Feedback

What Next

Add the required state for the voltage name of the pg pin if it is missing in the library, or the pg setting in the cell, or fix the name if it is a typographical error.

LBDB-124

(error) The pg setting instance pg_setting(%s, %s) is invalid.

Description

The pg setting instance delaration must be referring to a pg_setting_definition and one of its pg_setting_value.

The following example shows an instance where this message occurs: The following example shows an incorrect pg setting instance:

```
cell(CGNP) {
  area : 1;
  pg_setting_definition(rw) {
    pg_setting_value(read) {
      ...
    }
  }
  mode_definition(rw) {
    mode_value(read) {
      ...
    }
    mode_value(write) {
        pg_setting(rw, write);
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The pg setting instance pg_setting(rw, write) is
 invalid. (LBDB-124)
```

What Next

Check for consistency between mode group and pg setting definitions, and pg setting instance declarations.

LBDB-125

(warning) The %s '%s' in group %s is ignored.

Feedback

Description

This message indicates that you specified a redundant attribute or group in the specified group.

The following example shows an instance where this message occurs: The following example shows a redundant pg_pin_active_state for VBP in this pg_setting_value group.

```
cell (CC) {
    pg_setting_definition(PD) {
        pg_setting_value(PV) {
            pg_pin_condition : "VDD * !VSS" ;
            pg_pin_active_state(VDD, on);
            pg_pin_active_state(VBP, pon);
        }
    }
}
```

The following is an example message:

```
Warning: Line 639, The pg_pin_active_state VBP in group pg_setting_value
 is ignored. (LBDB-125)
```

What Next

Remove the redundant attribute from the parent group and rerun the command.

LBDB-126

(error) The '%s' construct is not valid\n \tin '%s' libraries.

Description

This message indicates that the specified construct is not valid in the specified library. In Library Compiler, certain constructs are valid only in certain types of libraries. For example, pin resistances are not valid when specified on timing arcs in nonlinear (table_lookup) libraries.

The following example shows an instance where this message occurs:

```
library(lbdb126) {
  delay_model : "generic_cmos";
  piece_define("0 8 15");

  cell(INVERTER) {
    area : 5.0;
    cell_power : 1.0;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
```

Feedback

```
  }
}
```

In this case, the 'cell_power' construct is not valid in piecewise_cmos libraries.

The following is an example message:

```
Error: Line 155, The 'cell_power' construct is not valid
        in 'piecewise_cmos' libraries. (LBDB-126)
```

What Next

Remove the invalid construct from the library source file

LBDB-127

(error) The %s contains invalid variable '%s'.

Description

This message indicates that the Boolean condition contains invalid operand. For pg_pin_condition, only pg pin and signal pin are allowed; For pg_setting_condition, only other pg_setting_definition and signal pin are allowed;

The following example shows an instance where this message occurs: The following example shows an incorrect pg_pin_condition in this pg_setting_value group, while X is neither a pg pin nor pin of the cell.

```
cell (CC) {
    pg_setting_definition(PD) {
        pg_setting_value(PV) {
            pg_pin_condition : "VDD * !VSS * X" ;
            pg_pin_active_state(VDD, on);
        }
    }
}
```

The following is an example message:

```
Warning: Line 639, The pg_pin_condition contains incorrect variable 'X'.
 (LBDB-127)
```

What Next

Check the Boolean condition and remove invalid variable.

LBDB-128

(error) The '%s' and '%s' attributes are both defined for this\n \t%s group.

Feedback

Description

This error indicates some attributes are specified together in one group.

derived_layers groups require specification of either 1. and 2. or 3. not 4. xor 5. resize However, it is an error to specify more than one of them.

pg_setting_value groups require specification of either 1. pg_pin_condition and pg_pin_active_state 2. pg_setting_condition and pg_setting_active_state

However, it is an error to mix both the styles.

The following example shows an instance where this message occurs:

```
cell (CC) {
    pg_setting_definition(PD) {
        pg_setting_value(PV) {
            pg_pin_condition : "VDD * !VSS" ;
            pg_setting_condition : "PD1 * PD2";
        }
    }
}
```

The following is an example message:

```
Error: Line 104, The 'pg_pin_condition' and 'pg_setting_condition'
 attributes are both defined for this
       pg_setting_value group. (LBDB-128)
```

What Next

Check the library source file to make sure that the previous requirement is met.

LBDB-129

(error) The pg_setting_value '%s' contains circular pg_setting_active_state.

Description

The pg_setting_active_state in the pg_setting_value has circular reference. A circular reference occurs when an pg_setting_value is related to itself through other pg_setting_value. Under this situation, the pg_setting_condition can never be resolved. Therefore, Library Compiler flags them with errors.

The following example shows an instance where this message occurs:

```
cell(lbdb140) {
        pg_setting_definition(PD) {
            ...
        }
        pg_setting_definition(PD_1) {
            ...
```

Feedback

```
        }
        pg_setting_definition(PD_2) {
            ...
        }
        pg_setting_definition(PD_3) {
            pg_setting_value(PV8) {
                pg_setting_condition : "PD_4 + PD_1" ;
                pg_setting_active_state(PD_4, PV1);
                pg_setting_active_state(PD_1, PV1);
            }
        }
        pg_setting_definition(PD_4) {
            pg_setting_value(PV1) {
                pg_setting_condition : "PD * !PD_3" ;
                pg_setting_active_state(PD, PV1);
                pg_setting_active_state(PD_3, PV8);
            }
        }

    }
```

The following is an example message:

```
Warning: Line 263, The pg_setting_value 'PV8' contains circular
 pg_setting_active_state. (LBDB-129)
```

What Next

Check the library source file, and verify the questionable circular pg_setting_value.

LBDB-130

(error) The pg_setting_condition of '%s' is always %s.

Description

This error message indicates that the pg_setting_condition is always true or false, which means the pg_setting_value is always active or never active.

The following example shows an instance where this message occurs:

```
cell(lbdb140) {
        pg_setting_definition(PD) {
            pg_setting_value(PV1) {
                pg_pin_condition : "!VDD + VSS" ;
            }
        }
        pg_setting_definition(PD_2) {
            pg_setting_value(PV1) {
                pg_pin_condition : "VDD * !VSS" ;
            }
        }
```

Feedback

```
        pg_setting_definition(PD_3) {
            pg_setting_value(PV8) {
                pg_setting_condition : "PD_2 * PD" ;
                pg_setting_active_state(PD_2, PV1);
                pg_setting_active_state(PD, PV1);
            }
        }

    }
```

The following is an example message:

```
Warning: Line 263, The pg_setting_condition of 'PV8' is always false.
 (LBDB-130)
```

What Next

Check the Boolean condition, and verify the problematic expression.

LBDB-131

(error) The required state of %s with name '%s' has not been defined in the %s, or it is invalid.

Description

This message indicates that the pg_pin_active_state or pg_setting_active_state of the specified object is not defined in the group, or it's an invalid state.

The following is an example message:

```
Error: Line 57, The required state of pg pin with name 'VDD" has not been
 defined in the pg_setting_value, or it is invalid.(LBDB-131)
```

What Next

Add the correct state for this object.

LBDB-132

(error) In the '%s' cell, the %s pin '%s' cannot have\n \ta '%s' attribute.

Description

This message indicates that you specified a *clock* or a *prefer_tied* attribute on a inout pin.

The following example shows an instance where this message occurs:

```
cell(lbdb132) {
    area : 1;
    pin(A B C) {
```

Feedback

```
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : inout;
      function : "A B";
      three_state : "C";
      clock : true;
      timing() {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A B C";
      }
      timing() {
        timing_type : three_state_disable;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C";
      }
    }
  }
```

In this case, the 'Z' pin whose direction is inout has a clok attribute set.

The following is an example message:

```
Error: Line 219, In the 'lbdb132' cell, the inout pin 'Z' cannot have
        a 'clock' attribute. (LBDB-132)
```

What Next

Remove the specified attribute, or change the direction of the pin to input.

LBDB-135

(error) The attribute '%s' is required for at least one output pin as the related PG pin has attribute '%s'.

Description

For a macro cell, if output pins' PG pin has attribute 'permit_power_down', it is a requirement that at least one output pin associated to the PG pin has attribute 'alive_during_partial_power_down'.

The following example shows an instance where this message occurs:

```
cell(els) {
      is_macro_cell : true;
```

Feedback

```
    pg_pin (VDD) {
      pg_type : primary_power;
      voltage_name : VDD;
    }
    pg_pin (VDDL) {
      pg_type : primary_power;
      permit_power_down : true;
      voltage_name : VDDL;
    }
    pg_pin (VSS) {
      pg_type : primary_ground;
      voltage_name : VSS;
    }

    pin(EN) {
      direction : input;
      related_power_pin : VDDL;
      related_ground_pin : VSS;
    }
    pin(Y1) {
      direction : output;
      related_power_pin : VDDL;
      related_ground_pin : VSS;
    }
    pin(Y2) {
      direction : output;
      related_power_pin : VDDL;
      related_ground_pin : VSS;
    }
  }
```

In this case, all the output pins' related PG pins have the attribute 'permit_power_down', but there is no attribute 'alive_during_partial_power_down' in output pins ('Y1' and 'Y2').

The following is an example message:

```
Error: Line 326, Cell 'els', The attribute
 'alive_during_partial_power_down' is required for at least one output
 pin as the related PG pin has attribute 'permit_power_down' (LBDB-135)
```

What Next

Add required attribute to the output signal pin.

LBDB-136

(warning) The '%s' attribute on the '%s' pin in\n \tthe '%s' cell is not valid on %s pins.\n \tThe attribute is ignored.

Feedback

Description

This message indicates that the attribute on the specified pin is invalid. The attribute is ignored.

The following example shows an instance where this message occurs:

```
cell(lbdb136) {
      area : 9;
      pin(D) {
        direction : input;
        capacitance : 1;
      }
      pin(CP) {
        direction : input;
        capacitance : 1;
      }
      pin(CD) {
        direction : input;
        capacitance : 2;
      }
      ff("IQ","IQN") {
        next_state : "D";
        clocked_on : "CP";
        clear   : "CD'";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        min_period : 0;
      }
```

In this case, the min_period attribute is defined for an output pin.

The following is an example message:

```
Warning: Line 1848, The  'min_period'  attribute on the 'Q' pin in
        the 'lbdb136' cell is not valid on output pins.
        The attribute is ignored. (LBDB-136)
```

What Next

Refer to the "Library Compiler User Guide" to determine the reason why the attribute is not valid. Make the correction.

LBDB-137

(error) The attribute '%s' is required as its related PG pin has attribute '%s'.

Feedback

Description

This message indicates that the required attribute on the specified pin is missing, since the related PG pin of the pin has specified attribute.

For an isolation cell, or macro cell with isolation enable pin, if the PG pin has attribute 'permit_power_down', it is a requirement that the output pin and isolation cell enable pin associated to the PG pin has attribute 'alive_during_partial_power_down'.

The following example shows an instance where this message occurs:

```
cell(els) {
      pg_pin (VDD) {
        pg_type : primary_power;
        voltage_name : VDD;
      }
      pg_pin (VDDL) {
        pg_type : primary_power;
        permit_power_down : true;
        voltage_name : VDDL;
      }
      pg_pin (VSS) {
        pg_type : primary_ground;
        voltage_name : VSS;
      }

      pin(EN) {
        isolation_cell_enable_pin : true;
        direction : input;
        related_power_pin : VDDL;
        related_ground_pin : VSS;
      }
      pin(Y) {
        direction : output;
        related_power_pin : VDDL;
        related_ground_pin : VSS;
      }
    }
```

In this case, the alive_during_partial_power_down is missing in pin EN and Y.

The following is an example message:

```
Error: Line 326, Cell 'els', pin 'EN', The attribute
 'alive_during_partial_power_down' is required as its related PG pin has
 attribute 'permit_power_down'. (LBDB-137)
Error: Line 346, Cell 'els', pin 'Y', The attribute
 'alive_during_partial_power_down' is required as its related PG pin has
 attribute 'permit_power_down'. (LBDB-137)
```

What Next

Add required attribute to the signal pin.

Feedback

LBDB-138

(warning) The timing arc is missing the piecewise data value\n \tfor '%s'. The value is interpolated if possible.\n \tOtherwise, the default value is used if it exists.

Description

This message indicates that you did not specify the definition of either delay intercept attributes or pin resistance attributes of piece number in a CMOS piecewise linear delay model library.

The following example shows an instance where this message occurs:

```
library(test) {
  delay_model : "generic_cmos";
  piece_define("0 8 15");

  cell(lbdb138) {
    area : 5.0;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Z) {
      direction : output;
      function : "A'";

      timing() {
        intrinsic_rise : 5.0;
        intrinsic_fall : 2.0;
        slope_rise : 1.0;
        slope_fall : 2.0;

        rise_delay_intercept(0, "1.1");
        rise_delay_intercept(1, "2.2");
        rise_delay_intercept(2, "3.3");

        fall_delay_intercept(0, "1.1");
        fall_delay_intercept(1, "2.2");
        fall_delay_intercept(2, "3.3");

        rise_pin_resistance(0, "1.1");
        rise_pin_resistance(1, "2.2");

        fall_pin_resistance(0, "4.4");
        fall_pin_resistance(1, "4.4");

        related_pin : "A";
      }
    }
  }
}
```

Feedback

In this case, the value of the rise_pin_resistance attribute is missing for index 2.

The following is an example message:

```
Warning: Line 165, The timing arc is missing the piecewise data value
        for 'rise_pin_resistance(2)'. The value is interpolated if
 possible
        Otherwise, the default value is used if it exists. (LBDB-138)
```

What Next

Add the missing attribute to the specified piece number.

LBDB-139

(error) Invalid delay model for the given technology.

Description

This message indicates that you specified an invalid value in the delay_model attribute.

The following example shows an instance where this message occurs:

```
delay_model : "lbdb139";
```

The following is an example message:

```
Error: Line 3, Invalid delay model for the given technology. (LBDB-139)
```

What Next

Refer to the "Library Compiler User Guide" for supported delay models. Change the value of the delay_model attribute to a valid one.

LBDB-140

(warning) The '%s' cell contains circular timing arcs.\n \tThe '%s' pin is in one of the cycles.

Description

The pin in the library cell has circular timing arcs. A circular timing arc occurs when an inout or output pin is related to itself through other inout or output pins. A change in one pin belonging to a circular timing arc continually loops around.

Circular timing arcs do not make sense and are probably mistakes. Therefore, the Library Compiler flags them with warnings.

The following example shows an instance where this message occurs:

```
cell(lbdb140) {
      area : 9;
```

Feedback

```
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(CP) {
      direction : input;
      capacitance : 1;
    }

    ff("IQ","IQN") {
      next_state : "D";
      clocked_on : "CP";
    }
    pin(Q) {
      direction : output;
      function : "IQ";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CP";
      }
    }
    pin(Q2) {
      direction : output;
      function : "IQ";
      timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "Q3";
      }
    }
    pin(Q3) {
      direction : output;
      function : "IQ";
      timing() {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "Q2";
      }
    }
  }
```

The following is an example message:

```
Warning: Line 263, The 'lbdb140' cell contains circular timing arcs.
        The 'Q2' pin is in one of the cycles. (LBDB-140)
```

Feedback

What Next

Check the library source file, and verify the questionable circular timing arcs.

LBDB-141

(warning) The timing arc is missing the piecewise data value for\n \t'%s'. The default value is used if it exists.

Description

This message indicates that you did not specify the definition of either delay intercept attributes or pin resistance attributes of the piece number defined in the piece_define in a CMOS piecewise linear delay model library.

The following example shows an instance where this message occurs:

```
library(test) {
  delay_model : "generic_cmos";
  piece_define("0");

  cell(lbdb138) {
    area : 5.0;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Z) {
      direction : output;
      function : "A'";

      timing() {
        intrinsic_rise : 5.0;
        intrinsic_fall : 2.0;
        slope_rise : 1.0;
        slope_fall : 2.0;

        rise_delay_intercept(0, "1.1");

        rise_pin_resistance(0, "1.1");
        fall_pin_resistance(0, "4.4");

        related_pin : "A";
      }
    }
  }
```

In this case, the value of the fall_delay_intercept attribute is missing for index 2.

Feedback

The following is an example message:

```
Warning: Line 170, The timing arc is missing the piece wise data value
 for
        'fall_delay_intercept(0)'. The default value is used if it
 exists. (LBDB-141)
```

What Next

Add the missing attribute to the specified piece number.

LBDB-142

(error) '%s' is an invalid value for the '%s'\n \tenumerated type attribute.

Description

This message indicated that you specified a value that is not part of the enumerated literals for the specified attribute.

The following example shows an instance where this message occurs:

```
voltage_unit : "1";
```

The following is an example message:

```
Error: Line 19, '1' is an invalid value for the 'voltage_unit'
        enumerated type attribute. (LBDB-142)
```

What Next

Refer to the "Library Compiler User Guide", and fix the invalid value.

LBDB-143

(error) An invalid string is provided. The invalid string is\n \teither a blank string or a string that begins with a digit\n \tthat is unquoted.

Description

A string begining with a digit must be enclosed in double quotes (""). In addition, blank strings are not valid in Library Compiler.

The following example shows an instance where this message occurs:

```
type(111) {
    base_type : array;
    data_type : bit;
    bit_width : 2;
    bit_from : 1;
    bit_to : 0;
```

Feedback

```
    downto : true;
  }
```

In this case, the 111 type name starts with a digit. To fix the problem, add quotes.

The following is an example message:

```
Error: Line 29, An invalid string is provided. The invalid string is
        either a blank string or a string that begins with a digit
        that is unquoted. (LBDB-143)
```

What Next

Check the library and correct the string. If the string begins with a digit, enclose the string in quotes. Remove any blank strings. For details on Library Compiler string rules, refer to the "Library Compiler Reference Manual".

LBDB-144

(error) The '%s' pin name does not match the '%s' bus name.

Description

This message indicates that you specified a bus element name different from the bus name given in the bus_naming_style. Library Compiler cannot extract the element name properly.

What Next

Make sure that the bus_naming_style string matches the specified bus name.

LBDB-145

(warning) The 'direction' attribute is missing in the %s '%s'.

Description

This message indicates that the direction attribute is missing in the bus or bundle group.

The following example shows an instance where this message occurs:

```
bundle(Q) {
      members(XQ, Q1);
/*      direction : output; */
      function : "1";
    }
```

The following is an example message:

```
Warning: Line 53, The 'direction' attribute is missing in the 'Q' bundle.
 (LBDB-145)
```

Feedback

What Next

Add the direction attribute to the bus or bundle port in the technology library.

LBDB-146

(error) The value for the update attribute must be "true" or "false".

Description

This message indicates that, in a symbol library, you specified an invalid value to the *update* attribute in either an *annotate_symbol* or an *annotate* group. This might be caused by a typo because the Library Compiler expects a quoted string.

The following example shows an instance where this message occurs:

```
annotate_symbol() {
      value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
      format : "sheet:  %s of %s" ;
      x : RIGHT_X ;
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
      update : true;
    }
```

The following is an example message:

```
Error: Line 95, The value for the update attribute must be "true" or
 "false". (LBDB-146)
```

What Next

Check your symbol library file, and correct the value of the update attribute.

LBDB-147

(error) A value must be specified for the annotate or\n \tthe annotate_symbol group.

Description

This message indicates that, in a symbol library, you did not specify a value to either the *annotate* or the *annotate_symbol* group.

The following example shows an instance where this message occurs:

```
annotate_symbol() {
      format : "sheet:  %s of %s" ;
      x : RIGHT_X ;
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
    }
```

Feedback

In this case, the value attribute is missing. To fix the problem, add the attribute,

```
value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
```

The following is an example message:

```
Error: Line 89, A value must be specified for the annotate or
        the annotate_symbol group. (LBDB-147)
```

What Next

Check your symbol library file, and add the value attribute.

LBDB-148

(error) The '%s' pin is not found in the annotate_symbol group.

Description

This message indicates that, in a symbol library, you specified an invalid pin_name value for the *pin_name* attribute in an *annotate_symbol*. This might be caused by a typo.

The following example shows an instance where this message occurs:

```
symbol("lbdb148") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 10000, 1000, DOWN);

    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
    annotate_symbol() {
      value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
      pin_name : "P2";
      format : "sheet:  %s of %s" ;
      x : RIGHT_X ;
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
    }

  }
```

In this case, the 'P2' name does not exist in the 'lbdb148' symbol. Change the name to P0.

The following is an example message:

```
Error: Line 89, The 'P2' pin is not found in the annotate_symbol group.
 (LBDB-148)
```

Feedback

What Next

Check your symbol library file, and correct the value of the pin_name attribute.

LBDB-149

(error) The X value is invalid in the annotate or\n \tthe annotate_symbol group.

Description

This message indicates that, in a symbol library, you specified an invalid value to the *X* attribute in either an *annotate* or *annotate_symbol* group. This might be caused by a typo.

The following example shows an instance where this message occurs:

```
symbol("lbdb148") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 10000, 1000, DOWN);

    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
    annotate_symbol() {
      value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
      format : "sheet:  %s of %s" ;
      x : "";
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
    }

  }
```

The following is an example message:

```
Error: Line 89, The X value is invalid in the annotate or
        the annotate_symbol group. (LBDB-149)
```

What Next

Check your symbol library file, and correct the value of the X attribute.

LBDB-150

(error) The format specification cannot have more than %d %%s specifications.

Description

This message indicates that, in a symbol library, the format attribute has more than 10 string specifications. Library Compiler accepts only 10.

Feedback

The following example shows an instance where this message occurs:

```
annotate_symbol() {
      value( "A1","A2","A3","A4","A5","A6","A7","A8","A9","A10" ) ;
      format : "sheet:  %s of %s %s of %s %s of %s %s of %s %s of %s %s
 of %s " ;
      x : RIGHT_X ;
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
    }
```

The following is an example message:

```
Error: Line 101, The format specification cannot have more than 10 %s
 specifications. (LBDB-150)
```

What Next

Check your symbol library file, and reduce the number of specification in the format attribute.

LBDB-151

(error) The format specification has %d %%s specification(s),\n \tbut only %d value(s) is/are specified.

Description

This message indicates that, in a symbol library, the format specification does not match the number of values provided to either the *annotate* or the *annotate_symbol* group. This might be caused by a typo.

The following example shows an instance where this message occurs:

```
annotate_symbol() {
      value( "ANN_PAGE_NUM") ;
      format : "sheet:  %s of %s" ;
      x : RIGHT_X ;
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
    }
```

In this case, the value attribute has only the string value, but the format refers to two %s. To fix the problem, either add the second string value in the value attribute or remove the second %s in the format attribute.

The following is an example message:

```
Error: Line 89, The format specification has 2 %s specification(s),
        but only 1 value(s) is/are specified. (LBDB-151)
```

Feedback

What Next

Check your symbol library file, and correct the value of either the value attribute or the format attribute.

LBDB-152

(error) The '%s' object type is invalid in the annotate\n \tor the annotate_symbol group.

Description

This message indicates that, in a symbol library, you specified an invalid object type for the *object_type* attribute in either an *annotate* or *annotate_symbolgroup. This might be caused by a typo. Library Compiler accepts the following object types:*

```
* pin
        * design
        * port
        * cell
        * net
```

The following example shows an instance where this message occurs:

```
symbol("lbdb152") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 10000, 1000, DOWN);

    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
    annotate_symbol() {
      value( "ANN_PAGE_NUM", "ANN_NUM_PAGES") ;
      format : "sheet:  %s of %s" ;
      x : "RIGHT_X";
      y : LOW_Y ;
      layer_name : "template_text_layer" ;
      object_type : "library";
    }

  }
```

The following is an example message:

```
Error: Line 89, The 'library' object type is invalid in the annotate
        or the annotate_symbol group. (LBDB-152)
```

What Next

Check your symbol library file, and correct the value of the object_type attribute.

Feedback

LBDB-153

(error) A syntax error is found before the library or phys_library group.\n \tThe compilation is terminated.

Description

This message follows lexical and syntax error messages issued when reading a library.

The following example shows an instance where this message occurs:

```
related_bus_pins : { ADDR";
```

In this case, a lexical error is encountered in the related_bus_pins value. Substitute the '{' for a "".

The following is an example message:

```
Error: A syntax error is found before the library or phys_library group.
        The compilation is terminated. (LBDB-153)
```

What Next

Fix all lexical and syntax errors.

LBDB-155

(warning) The %s_cell for the '%s' cell with '%s'\n \toperating_conditions is defined multiple times in the library.\n \tUsing the last one encountered.

Description

This message indicates that a scaled_cell with the same operating_conditions is defined multiple times in the library. This might be caused by a typo in the name of the operating_conditions. Library Compiler uses the last cell encountered.

The following example shows an instance where this message occurs:

```
library(lbdb155) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
    }
    cell(IVV) {
      area : 1;
      pin(A) {
        direction : input;
        capacitance : 1;
      }
```

Feedback

```
    pin(Z) {
      direction : output;
      function : "A'";
      timing() {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "A";
      }
    }
  }

  scaled_cell(IVV,WCCOM) {
    area : 1;
    pin(A) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A'";
      timing() {
        intrinsic_rise : 0.3;
        intrinsic_fall : 0.3;
        rise_resistance : 0.3;
        fall_resistance : 0.3;
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "A";
      }
    }
  scaled_cell(IVV,WCCOM) {
    area : 1;
    pin(A) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A'";
      timing() {
        intrinsic_rise : 0.3;
        intrinsic_fall : 0.3;
        rise_resistance : 0.3;
        fall_resistance : 0.3;
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "A";
      }
    }
```

```
    }
  }
```

The following is an example message:

```
Warning: Line 327, The scaled_cell for the 'AND' cell with 'WCCOM'
         operating_conditions is defined multiple times in the library.
         Using the last one encountered. (LBDB-155)
```

What Next

Delete all the redundant scaled_cell groups, or fix the library if it is a typo.

LBDB-156

(error) The LSI rounding digit and cutoff attributes\n \thave incompatible values.

Description

This message indicates that you specified invalid values for either the *lsi_rounding_digit* or the *lsi_rounding_cutoff* attribute. Library Compiler issues this error when the lsi_rounding_digit value is greater than the lsi_rounding_cutoff value multiplied by 10.01 or the lsi_rounding_cutoff value is greater than the lsi_rounding_digit value.

The following example shows an instance where this message occurs:

```
lsi_rounding_digit : 0.1;
   lsi_rounding_cutoff : 0.003;
```

In this case, the lsi_rounding_digit 0.1 is greater than (0.003 * 10.01). To fix the problem, assign the value 0.01 to lsi_rounding_digit.

```
lsi_rounding_digit : 0.01;
```

The following is an example message:

```
Error: Line 10, The LSI rounding digit and cutoff attributes
        have incompatible values. (LBDB-156)
```

What Next

Check the library, and fix either the value of the lsi_rounding_digit or the lsi_rounding_cutoff attribute.

LBDB-157

(error) The '%s' cell name defined in the scaled_cell is not found.

Feedback

Description

This message indicates that the technology library has a scaled_cell defined without a parent cell defined. Library Compiler uses the scaled_cell group to supply an alternate set of values for an existing cell. The choice is based on the set of operating conditions used.

The following example shows an instance where this message occurs:

```
library(lbdb157) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
    }

cell(IV) {
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
scaled_cell(IVV,WCCOM) {    /* Typo in the cell name. */
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.3;
      intrinsic_fall : 0.3;
      rise_resistance : 0.3;
      fall_resistance : 0.3;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
```

```
    }
  }
}
}
```

The following is an example message:

```
Error: Line 101, The 'IVV' cell name defined in the scaled_cell is not
 found. (LBDB-157)
```

What Next

Add the parent cell for the scaled_cell, or fix the scaled_cell name if it is a typo.

LBDB-158

(error) The '%s' operating conditions is not found.

Description

This message indicates that the technology library has a scaled_cell with an undefined operating conditions.

The following example shows an instance where this message occurs:

```
library(lbdb158) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
    }

cell(IV) {
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
```

Feedback

```
}
scaled_cell(IV,WCCOM1) {    /* Typo in the operating_conditions name. */
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.3;
      intrinsic_fall : 0.3;
      rise_resistance : 0.3;
      fall_resistance : 0.3;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}
```

The following is an example message:

```
Error: Line 305, The 'WCCOM1' operating conditions is not found.
 (LBDB-158)
```

What Next

Add the operating_conditions group if it is missing, or fix the operating_conditions name if it has a typo.

LBDB-159

(error) Incomplete EDIF properties are specified in the '%s' symbol.\n \tSpecify 'edif_cell_name', 'edif_view_name', and 'edif_name_property'.

Description

This message indicates that, in a symbol library, you specified incomplete attributes of the view identifier properties of the symbol for a cell. These attributes are *edif_cell_name*, *edif_view_name*, and *edif_name_property*. If Library Compiler encounters a symbol with any of these attributes, it must have all three of them declared.

The following example shows an instance where this message occurs:

```
symbol("lbdb159") {
    set_minimum_boundary(0 , 0 , 8000, 12000);
    pin("P0", 10000, 1000, DOWN);
```

Feedback

```
    line(0, 0, 0, 12000);
    line(0, 12000, 8000, 12000);
    line(8000, 12000, 8000, 0);
    line(8000, 0, 0, 0);
    edif_cell_name : "edifcell";
    edif_name_property : " edifproperty";
  }
```

In this case, the edif_view_name attribute is missing. To fix the problem, add

```
edif_view_name : "edifview";
```

The following is an example message:

```
Error: Incomplete EDIF properties are specified in the 'lbdb159' symbol.
       Specify 'edif_cell_name', 'edif_view_name', and
 'edif_name_property'. (LBDB-159)
```

What Next

Change the symbol definition for the cell in the source text file of the symbol library. Either delete the view identifier property attributes that are there so that the symbol has none of those attributes or add appropriate view identifier property attributes, so that the symbol has all three of those attributes.

LBDB-160

(error) It is not acceptable to set the technology to\n \t'%s' after it has been set to '%s'. The two\n \ttechnologies are incompatible.

Description

This message indicates that you specified incompatible values for the technology attribute and the delay_model attribute.

The following example shows an instance where this message occurs:

```
library(lbdb160) {
    /* wrong technology and delay model combination */
    technology("cmos");
    delay_model : generic_ecl;
}
```

The following is an example message:

```
Error: Line 4, It is not acceptable to set the technology to
        'generic_ecl' after it has been set to 'cmos'. The two
        technologies are incompatible. (LBDB-160)
```

Feedback

What Next

Check The Library Compiler User Guide Manual for compatible combinations, and fix either the value of the technology or the delay_model attribute.

LBDB-161

(error) The '%s' bus needs to have its bus_type specified first.\n \tThe %s '%s' was found before the bus_type.

Description

This message indicates that you specified a bus without its bus_type attribute, or Library Compiler rejected the bus_type value and considered it as not defined.

The following example shows an instance where this message occurs:

```
bus (D) {
/*    bus_type : bus2; */       /* remove the comment to fix the problem
 */
      direction : input;
      capacitance : 1.0;
    }
```

The following is an example message:

```
Error: Line 179, The 'D' bus needs to have its bus_type specified first.
       The attribute 'direction' was found before the bus_type.
 (LBDB-161)
```

What Next

Add the bus_type attribute to the library, or fix the value of the attribute.

LBDB-162

(error) An invalid area range is found in the wire_load_from_area attribute.

Description

This message indicates that you specified an invalid area range. The problem is caused by any of these reasons:

```
* The min_area value is greater than the max_area value.
        * The min_area value is less than zero.
        * The max_area value is less or equal to zero.
```

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
    resistance : 0 ;
```

Feedback

```
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }
  wire_load_selection(test) {
    wire_load_from_area(27,10,"10x10");          /* problem */
    wire_load_from_area(27,100,"10x10");
    wire_load_from_area(0,28,"05x05");
    wire_load_from_area(2,10,"15x10");
  }
```

In this case, the minimum area value 27 is greater than the maximum area value 10.

The following is an example message:

```
Error: Line 51, An invalid area range is found in the wire_load_from_area
 attribute. (LBDB-162)
```

What Next

Check the area values, and fix the problem.

LBDB-163

(warning) The '%s' attribute value is\n \t %s (%3.1f). Using %3.1f instead.

Description

This message indicates that you specified an attribute value that is out of the accepted range. The value is either less than the minimum value or greater than the maximum value.

The following example shows an instance where this message occurs:

```
k_volt_internal_power : -111.0;
```

In this case, the k_volt_internal attribute's value -111.0 is less than the minimum accepted value -100.0.

The following is an example message:

```
Warning: Line 9, The 'k_volt_internal_power attribute' attribute value is
         less than the minimum allowed  (-100.0). Using 0.0 instead.
 (LBDB-163)
```

What Next

Change the attribute value to satisfy the value range.

Feedback

LBDB-164

(error) The 'wire_load_from_area' range overlaps\n \tthe range in line %d.

Description

This message indicates that you specified an overlapping area range in two *wire_load_from_area* attributes.

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

  wire_load_selection(test) {
    wire_load_from_area(0,20,"05x05");
    wire_load_from_area(10,25,"05x05");
  }
```

In this case, the area range [0,20] overlaps the area range [10,25].

The following is an example message:

```
Error: Line 12, The 'wire_load_from_area' range overlaps
        the range in line 13. (LBDB-164)
```

What Next

Change the area range in the second *wire_load_from_area* attribute.

LBDB-165

(warning) A range gap is found in the 'wire_load_selection'.\n \tThe 'min_area' is extended from %f to %f.

Description

The wire_load_selection specified in this library has a gap. It means that two adjacent selector items are not overlapped. Library Compiler uses its built-in algorithm to fill the gap. It extends the lower bound of the selector that covers the bigger area toward the upper bound of the other selector item.

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
    resistance : 0 ;
```

```
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

  wire_load_selection(test) {
    wire_load_from_area(0,20,"05x05");
    wire_load_from_area(25,50,"05x05");
  }
```

In this case, there is a gap in area range from 20 to 25. Library Compiler corrects the problem as if you had the declaration

```
wire_load_from_area(20,50,"05x05");
```

The following is an example message:

```
Warning: Line 13, A range gap is found in the 'wire_load_selection'.
        The 'min_area' is extended from 25.000000 to 20.000000.
 (LBDB-165)
```

What Next

Ignore the warning if the Library Compiler's algorithm satisfies your modeling requirement. Otherwise, fix the library source code to match your wire_load_selection model.

LBDB-166

(warning) A range does not start with 0.0 in the 'wire_load_selection'.\n \tThe 'min_area' is extended from %f to 0.0.

Description

The min_area value in the specified wire_load_selection attribute in this library does not start with 0.0. Library Compiler extends the lower bound of the selector to 0.0.

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

  wire_load_selection(test) {
    wire_load_from_area(10,25,"05x05");
  }
```

Feedback

The following is an example message:

```
Warning: Line 48, A range does not start with 0.0 in the
 'wire_load_selection'.
        The 'min_area' is extended from 10.000000 to 0.0. (LBDB-166)
```

What Next

Fix the library source code to set the min_area to 0.0.

LBDB-167

(error) The '%s' scaling factors group is not found.

Description

The message indicates that you specified an invalid name for the scaling_factors group. This might be caused either by a typo in the name or by the group not being defined.

The following example shows an instance where this message occurs:

```
scaling_factors("IO_PAD_SCALING") {
        k_volt_intrinsic_rise : 0.846 ;
    }
    cell (lbdb167) {
       area : 0 ;
       scaling_factors : IO_PAD_SCALE ;
    }

In this case, there is a typo in the name.

The following is an example message:
Error: Line 20, The 'IO_PAD_SCALE' scaling factors group is not found.
 (LBDB-167)
```

What Next

Add the scaling_factors group to the library, or correct the value of the scaling_factors if it is a typo.

LBDB-168

(error) The %s timing constraint has only one value.\n \tOnly one 'intrinsic_rise' or 'intrinsic_fall' can be specified.

Description

You specified invalid values for intrinsic_rise and intrinsic_fall in a timing group that describes a *recovery* or *removal* timing constraint. Library Compiler complains if each of these two constraints has

Feedback

```
* Both intrinsic_rise and intrinsic_fall values are assigned to zero.
        * Both intrinsic_rise and intrinsic_fall values are not
 specified.
        * Both intrinsic_rise and intrinsic_fall values are not zero.
```

The following example shows an instance where this message occurs:

```
pin(CD) {
      direction : input;
      capacitance : 2;
      timing() {
        timing_type : recovery_rising;
        /* both values are 0.0 */
        intrinsic_rise : 0.0;
        intrinsic_fall : 0.0;
        related_pin : "CP";
      }
      timing() {
        timing_type : removal_rising;
        /* both values not specified */
        related_pin : "CP";
      }
    }
```

The following is an example message:

```
Error: Line 56, The Recovery timing constraint has only one value.
        Only one 'intrinsic_rise' or 'intrinsic_fall' can be specified.
 (LBDB-168)
```

What Next

Inspect the datasheet of the cell in question. If the asynchronous control signal is high-active, define the recovery and the removal constraints as the intrinsic_fall. If the asynchronous control signal is low-active, define the recovery and the removal constraints as the intrinsic_rise. Remove the other field (intrinsic_rise or intrinsic_fall) from the library source file.

LBDB-169

(error) An invalid 'three_state_disable' timing type appears\n \ton the timing arc. Its parent output pin has no 'three_state' attribute.

Description

This message indicates that you specified a *three_state_disable* timing_arc on a port that has no *three_state* attribute.

Feedback

The following example shows an instance where this message occurs:

```
cell(AND) {
    area : 1;
    pin(A B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
      timing() {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A B" ;
      }
      timing() {
        timing_type : three_state_disable;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A";
      }
    }
  }
```

The following is an example message:

```
Error: Line 44, An invalid 'three_state_disable' timing type appears
        on the timing arc. Its parent output pin has no 'three_state'
 attribute. (LBDB-169)
```

What Next

Either delete the timing arc or correct the port group definition to add the three_state attribute.

LBDB-170

(warning) The '%s' attribute's value is\n \t%s (%3.1f). Removing it.

Description

This message indicates that you specified an attribute value that is out of the accepted range. The value is either less than the minimum value or greater than the maximum value. Library Compiler ignores the value because it does not find a default value to replace it.

Feedback

The following example shows an instance where this message occurs:

```
pin(A) {
      direction : input;
      capacitance : 1;
      min_fanout : -1;
    }
```

In this case, the min_fanout attribute's value -1 is less than the minimum accepted value 0.0.

The following is an example message:

```
Warning: Line 283, The 'min_fanout' attribute value is
         less than the minimum allowed (0.0). Removing it. (LBDB-170)
```

What Next

Change the attribute value to satisfy the value range.

LBDB-171

(error) The '%s' wire load model is not defined, or \n \tit is defined after this line.

Description

This message indicates that you specified a "wire_load_from_area" that refers to a "wire_load" group that is not defined or has been defined in the library after the current line.

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

  wire_load_selection(test) {
    wire_load_from_area(27,100,"10x10");
    wire_load_from_area(10,25,"05x05");
  }
```

The following is an example message:

```
Error: Line 47, The '10x10' wire load model is not defined, or
        it is defined after this line. (LBDB-171)
```

Feedback

What Next

Check your library to see if you have defined the group. If you have done that, also check its position within the library to make sure it is defined before it is used.

LBDB-172

(warning) The '%s' attribute is not specified. Using %4.2f.

Description

This message indicates that an attribute is missing, and Library Compiler is reporting the default floating point or integer value it is setting. This message affects attributes with default values.

The following example shows an instance where this message occurs:

```
pin(D) {
      direction : input;
    }
```

The following is an example message:

```
Warning: Line 52, The 'capacitance' attribute is not specified. Using
 0.00. (LBDB-172)
```

What Next

Either add the missing attribute to the technology library or ignore the message.

LBDB-173

(error) The '%s' group requires one or more names.

Description

This message indicates you specified no name for a group that requires at least one name.

The following example shows an instance where this message occurs:

```
pin() {
      direction : input;
      capacitance : 1.0;
   }
```

In this case, a pin name is required.

The following is an example message:

```
Error: Line 286, The 'pin' group requires one or more names. (LBDB-173)
```

Feedback

What Next

Change your library to add the group name.

LBDB-174

(error) The '%s' group requires %s names.

Description

This error message occurs when a group is specified without its required number of names. This might be caused by a typographical error.

The following example shows an instance where this message occurs: In the following example, the ff group requires 2 names. To fix the problem, either remove the last element 2, or if it is a typographical error, change ff to ff_bank.

```
ff(IQ,IQN, 2)
```

What Next

See the *Library Compiler User Guide* for the correct syntax of the specified group, and match the number of group names.

LBDB-175

(warning) The bus_naming_style contains characters that\n \tare also used as delimiters in function, three_state, and related_pin\n \tattributes. Be sure to put spaces around the characters in the [%s] set\n \twhen supplying values for attributes of the types mentioned. \n \tAlso, surround subscripted pin names with double quotes in pin groups.

Description

This message indicates that you specified delimiter characters in the *bus_naming_style* attribute such as "() +*|&!^'".

The following example shows an instance where this message occurs:

```
bus_naming_style : %s&%d;
```

The following is an example message:

```
Warning: Line 28, The bus_naming_style contains characters that
        are also used as delimiters in function, three_state, and
 related_pin
        attributes. Be sure to put spaces around the characters in the
 [&] set
        when supplying values for attributes of the types mentioned.
        Also, surround subscripted pin names with double quotes in pin
 groups. (LBDB-175)
```

Feedback

What Next

Change the delimiter character, or follow the rules specified in the message.

LBDB-176

(error) Invalid bus syntax is detected in '%s'.

Description

This message indicates that you specified an invalid bus element. Library Compiler fails to extract the bus element information using the bus_naming_style attribute value.

What Next

Change the library by either fixing the bus_naming_style value or fixing the bus element representation.

LBDB-177

(warning) The attribute '%s' is not specified Using '%s'.

Description

This message indicates that an attribute is missing, and Library Compiler is reporting the default string value it is setting. This message affects attributes with default values.

What Next

Either add the missing attribute to the technology library or ignore the message.

LBDB-178

(error) Duplicated %s group. A group with similar '%s' attribute value is found at line %u

Description

This message indicates that this group conflicts with an earlier group because the attribute indicated has similar value in both of them.

The following example shows an instance where this message occurs:

```
receiver_capacitance() {
        receiver_capacitance_rise {
          segment : 1;
          ...
        }
        receiver_capacitance_rise {
          segment : 1;
```

```
        ...
      }
      receiver_capacitance_rise {
        segment : 3;
        ...
      }
      ...
    }
```

In this case, the second receiver_capacitance_rise group is in error because its 'segment' attribute conflicts with the first group.

The following is an example message:

```
Error: Line 20014, Duplicated 'receiver_capacitance_rise' group. A group
 with
similar 'segment' attribute value is found at line 19876
```

What Next

Change the library file by modify the indicated attribute.

LBDB-179

(error) The '%s' group requires the '%s' attribute.\n \tEither the attribute is missing or the attribute has an invalid value.

Description

This message indicates you specified a group without one of its required attributes. Library Compiler rejects the attribute definition if the attribute exists and has an invalid value.

The following example shows an instance where this message occurs:

```
memory() {
        type : random;
        address_width : 10;
        word_width : 8;
      }
```

In this case, the 'type' has an invalid value. To fix the problem, assign 'rom' or 'ram' to the type.

The following is an example message:

```
Error: Line 27, The 'memory' group requires the 'type' attribute.
        Either the attribute is missing or the attribute has an invalid
 value. (LBDB-179)
```

What Next

Change the library file by adding the missing attribute to the group.

Feedback

LBDB-180

(error) The '%s' attribute requires both\n \t'clear' and 'preset' attributes.

Description

This message indicates that you specified the 'clear_preset_var1' or the 'clear_preset_var2' attribute or both in a sequential model group without specifying both the 'clear' and the 'preset' attributes.

The following example shows an instance where this message occurs:

```
ff("IQ","IQN") {
        next_state : "D";
        clocked_on : "CP";
        clear : "CD'";
        clear_preset_var1: "L";
      }
```

In this case, the 'preset' attribute is missing in the ff group.

The following is an example message:

```
Error: Line 98, The 'clear_preset_var1' attribute requires both
        'clear' and 'preset' attributes. (LBDB-180)
```

What Next

Add the missing attribute to the group.

LBDB-181

(error) The '%s' group, with both 'clear' and 'preset' attributes,\n \trequires 'clear_preset_var1' and/or 'clear_preset_var2' attributes.

Description

This message indicates that you specified both the 'clear' and the 'preset' attribute in a sequential model group without specifying both the 'clear_preset_var1' or the 'clear_preset_var2' attributes.

The following example shows an instance where this message occurs:

```
ff("IQ","IQN") {
        next_state : "D";
        clocked_on : "CP";
        preset : "SD'";
        clear : "CD";
```

In this case, the 'clear_preset_var1' and or 'clear_preset_var2' attributes are missing.

Feedback

The following is an example message:

```
Error: Line 93, The 'ff' group, with both 'clear' and 'preset'
 attributes,
         requires 'clear_preset_var1' and/or 'clear_preset_var2'
 attributes. (LBDB-181)
```

What Next

Add either 'clear_preset_var1' or 'clear_preset_var2' to the sequential group.

LBDB-182

(error) Invalid %s name '%s' is detected. This name must be\n \tunique among all pin names, bus names, bundle names, and rail connection names.

Description

This message indicates a duplicate pin, bus, bundle, a rail_connection, or a voltage_state_range name in the library.

The following example shows an instance where this message occurs:

```
pin(D) {
      direction : input;
      capacitance : 1.0;
    }
    pin(D) {
      direction : input;
      capacitance : 1.0;
    }
```

The following is an example message:

```
Error: Line 56, Invalid pin name 'D' is detected. This name must be
        unique among all pin names, bus names, and bundle names.
 (LBDB-182)
```

What Next

Change the name of the pin, bus, bundle, rail_connection, voltage_state_range in the technology library.

LBDB-183

(error) Missing '%s' group with '%s' attribute of '%s' value.

Feedback

Description

This message indicates that a group with a specific attribute value is missing. This problem is associated with certain type of information that requires data to be given in a series of groups. These groups are "tagged" with a specific attribute with a consecutive value.

The following example shows an instance where this message occurs:

```
receiver_capacitance() {
        receiver_capacitance_rise {
          segment : 1;
          ...
        }
        receiver_capacitance_rise {
          segment : 3;
          ...
        }
        receiver_capacitance_rise {
          segment : 4;
          ...
        }
        ...
      }
```

In the example above, receiver_capacitance_rise with segment = 2 is missing.

The following is an example message:

```
Error: Line 20073, Missing 'receiver_capacitance_rise' group with
 'segment' attribute of value '2'.
```

What Next

Fix the library by adding the missing group.

LBDB-186

(error) Invalid '%s' pin name is detected in the '%s' bundle.

Description

This message indicates that you specified an invalid pin name in a bundle group.

What Next

Change the library source file by correcting the pin name.

Feedback

LBDB-187

(error) The '%s' bundle needs to have its 'members' specified first.\n \tThe '%s' %s is found before a 'members'.

Description

This message indicates that you specified the members attribute in a bundle group after another attribute. The *members* attribute has to be first in the bundle group.

The following example shows an instance where this message occurs:

```
bundle (DD) {
        direction : input;
        members(D1, D2);
        capacitance : 1;
      }
```

The following is an example message:

```
Error: Line 94, The 'DD' bundle needs to have its 'members' specified
 first.
       The 'direction' attribute is found before a 'members'. (LBDB-187)
```

What Next

Change the library source file by specifying the members attribute first in the bundle group.

LBDB-188

(error) The 'members' attribute is defined multiple times.

Description

This message indicates that you specified the *members* attribute in a bundle group more than once. Library Compiler expects only one *members* attribute in the bundle group.

The following example shows an instance where this message occurs:

```
bundle (DD) {
        direction : input;
        members(D1, D2);
        members(D3, D4);
        capacitance : 1;
      }
```

The following is an example message:

```
Error: Line 95, The 'members' is defined multiple times. (LBDB-188)
```

Feedback

What Next

Change the library source file by specifying only one members attribute in a bundle group.

LBDB-189

(warning) Level shifters are required for this library.\n \tA level shifter is a buffer or inverter with differing\n \tconnection_class values specified between input and output\n \tpins. Design Compiler cannot produce valid designs using this\n \tlibrary if a level shifter component is not provided.

Description

This warning message occurs when your library contains connection classes that cannot be used without level shifters. Design Compiler uses these components to shift a net from one connection class to another and does so to remove connection class violations from your design. Multi-input or multi-output cells with differing connection classes on inputs and outputs are not considered level shifters. Following this warning message, a list appears of those connection classes that do not have valid shifters between them.

This warning alerts you to situations where Design Compiler might not be able to validate your design for connection class. For example, suppose that Library Compiler warns that you are missing a level shifter with an input connection class of "a" and an output connection class of "b". If there is a pin or port in your design with a connection class of "b" connected to a driver with a connection class of "a", Design Compiler might be unable to validate this connection without a level shifting component that converts voltage levels from an input connection class of "a" to an output connection class of "b".

There are cases where this message can be too restrictive. For example, consider the case where you, the designer, know that all inputs to your design will only have connection class "a" and that all outputs will only have connection class "c". Meanwhile, for the purposes of our example, assume that all "internal" logic in the design will have connection class "b". If you defined a library with two level shifters (one with "a" on the input and "b" on the output, and the other with "b" on the input and "c" on the output), Design Compiler can validate the design because it can convert voltage levels from the inputs at level "a" to internal logic at level "b", and from internal logic at level "b" to the outputs at level "c". In this case, the warnings that you receive about missing level shifters would be too restrictive. However, you have an output that is at level "a", and is driven by internal logic at level "b", Design Compiler is not be able to validate the design unless it can replace the component driving the output port with a component that has level "a" on its output pin.

Be aware of the current limitations in the connection class validation and be advised that you can construct a library with connection rule restrictions that are too difficult for Design Compiler to solve. Future versions of the software might remove these restrictions, but Library Compiler currently informs you of the limitations on validating a design for connection class violations.

Feedback

The following example shows an instance where this message occurs:

```
cell(lbdb189) {
      /* Should only be connected to IO Cells only */
      area : 0.0;
      dont_touch : false;
      dont_use   : false;
      pad_cell : true;
      pin(PAD ) {
        is_pad : true;
        input_voltage : CMOS;
        direction   : input;
        capacitance : 1.0;
        fanout_load : 0.0;
      }
      pin(Y ) {
        connection_class : "iopcl";
        direction   : output;
        function    : "PAD";
        max_fanout  : 1.0;
        timing() {
          intrinsic_fall  : 1.0;
          intrinsic_rise  : 1.0;
          fall_resistance : 0.0;
          rise_resistance : 0.0;
          related_pin  :"PAD ";
        }
      }
    }
```

The following is an example message:

```
Warning: Line 1, Level shifters are required for this library.
        A level shifter is a buffer or inverter with differing
        connection_class values specified between input and output
        pins. Design Compiler cannot produce valid designs using this
        library if a level shifter component is not provided. (LBDB-189)
```

What Next

If this message appeared because you omitted some level shifting components from your library, add the components.

LBDB-190

(warning) %s level shifter with input connection class '%s' \n and output connection class '%s' is needed.

Feedback

Description

This message indicates that a (noninverting or inverting) level shifter is needed between the two connection classes. See the man page for error LBDB-189 for more information on how this message can occur.

The following example shows an instance where this message occurs:

```
cell(IOPCLBUF) {
      /* Should only be connected to IO Cells only */
      area : 0.000000;
      dont_touch : false;
      dont_use   : false;
      pad_cell : true;
      pin(PAD ) {
        is_pad : true;
        input_voltage : CMOS;
        direction   : input;
        capacitance : 35.000000;
        fanout_load : 0.000000;
      }
      pin(Y ) {
        connection_class : "iopcl";
        direction   : output;
        function    : "PAD";
        max_fanout  : 16.000000;
        timing() {
          intrinsic_fall  : 3.925000;
          intrinsic_rise  : 3.925000;
          fall_resistance : 0.000000; /* delay included in intrinsic */
          rise_resistance : 0.000000; /* delay included in intrinsic */
          related_pin  :"PAD ";
        }
      }
    }
```

The following is an example message:

```
Warning: Line 1, Noninverting level shifter with input connection class
 'iopcl'
and output connection class 'default' is needed. (LBDB-190)
```

What Next

If you obtained this message because you omitted a level shifting component from your library, add the level shifting component.

LBDB-191

(error) The inout '%s' pin, bus, or bundle has\n \tno 'three_state' function.

Feedback

Description

The pin whose direction is specified as 'inout' has only a 'function' statement. The 'three_state' statement is also required by an "inout" pin.

The following example shows an instance where this message occurs:

```
pin(Z) {
      direction : inout;
      function : "A B";
    }
```

The following is an example message:

```
Error: Line 356, The inout 'Z' pin, bus, or bundle has
        no 'three_state' function. (LBDB-191)
```

What Next

If the pin is actually an output pin, change the direction attribute to 'output'. Otherwise, add the 'three_state' statement to the pin.

LBDB-192

(error) Illegal interdependence data specified in pin "%s".

Description

timing arc with "interdependence_id" attribute is treated as interdependence data in pin. they are used for setup/hold pessimism reduction. There are some rules to specified the id for interdependence data (These rules applies to timing arcs with same condition):

1. Interdependece data can not be the first timing arc in this pin. This it to prevent potential backward compatibility issue.
2. Interdependece data should be in pair. That is, if there is a setup_rising interdependence data with id = 1 in the pin, a hold_rising interdependence data with same id = 1 is needed. Same case for timing type = setup_falling / hold_falling.
3. For one timing_type arcs, the interdependence id should be unique. E.g. If there are two setup_rising interdependence data with same id = 1, this error is issued.
4. The interdependence id starts from 1, and if multiple interdependence data defined for the pin, the id should be consecutive. E.g. id = 1,2,3 is okay, but 1, 2, 4 is not.

The following example shows an instance where this message occurs:

```
pin(D) {
        direction : input;
        timing() {
            timing_type : setup_rising;
```

Feedback

```
            fall_constraint("template") {
            ...
            }
            rise_constraint("template") {
            ...
            }
            related_in: "CLK";
        }
        timing() {
            timing_type : setup_rising;
            interdependence_id : 1;
            fall_constraint("template") {
            ...
            }
            rise_constraint("template") {
            ...
            }
            related_in: "CLK";
        }
        timing() {
            timing_type : hold_rising;
            fall_constraint("template") {
            ...
            }
            rise_constraint("template") {
            ...
            }
            related_in: "CLK";
        }
        timing() {
            timing_type : hold_rising;
            interdependence_id : 2;
            fall_constraint("template") {
            ...
            }
            rise_constraint("template") {
            ...
            }
            related_in: "CLK";
        }
    }
```

The following is an example message:

```
Error: Line 356, Illegal interdependence data specified in pin
 "D".(LBDB-192)
```

What Next

Check the id value for interdependence data in the pin group, make sure all above requirments are satisfied.

Feedback

LBDB-193

(error) Interdependence data is defined for wrong timing type arc in pin "%s".

Description

Timing group with "interdependence_id" attribute is treated as interdependence data in pin. they are used to for setup/hold pessimism reduction. For now, It's only supported for these timing types: setup_rising, hold_rising, setup_falling, hold_falling.

The following example shows an instance where this message occurs:

```
pin(D) {
        direction : input;
        timing() {
            timing_type : setup_rising;
            fall_constraint("template") {
            ...
            }
            rise_constraint("template") {
            ...
            }
            related_in: "CLK";
        }
        timing() {
            timing_type : skew_rising; // not support type
            interdependence_id : 1;
            fall_constraint("template") {
            ...
            }
            rise_constraint("template") {
            ...
            }
            related_in: "CLK";
        }
        timing() {
            timing_type : hold_rising;
            fall_constraint("template") {
            ...
            }
            rise_constraint("template") {
            ...
            }
            related_in: "CLK";
        }
        timing() {
            timing_type : hold_rising;
            interdependence_id : 2;
            fall_constraint("template") {
            ...
            }
            rise_constraint("template") {
```

```
            ...
            }
            related_in: "CLK";
        }
    }
```

The following is an example message:

```
Error: Line 356, Interdependence data is defined for wrong timing type
 arc in pin "D".(LBDB-193)
```

What Next

Check the interdependence data in the pin group, make sure they are defined for constraint arcs with right timing type.

LBDB-200

(error) The cell has both the 'pad_cell' and the 'auxiliary_pad_cell' attributes.

Description

This message indicates that you specified both the *pad_cell* and the *auxiliary_pad_cell* attributes in the same cell.

The following example shows an instance where this message occurs:

```
cell(lbdb200){
      area : 0.000000;
      pad_cell : true;
      auxiliary_pad_cell : true;
    }
```

The following is an example message:

```
Error: Line 3577, The cell has both the 'pad_cell' and the
 'auxiliary_pad_cell' attributes. (LBDB-200)
```

What Next

Remove either the pad_cell attribute or the auxiliary_pad_cell attribute.

LBDB-201

(error) A nonpad '%s' cell has a '%s' attribute.

Description

This message indicates that you specified a pad_type attribute in a nonpad cell.

Feedback

The following example shows an instance where this message occurs:

```
cell(lbdb201){
      area : 0.0;
      pad_type : clock;
      pin(Z)  {
        direction : output
        function : "A"
      }
      pin(A) {
        direction : input;
        capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Error: Line 3577, A nonpad 'lbdb201' cell has a 'pad_type' attribute.
 (LBDB-201)
```

What Next

Check the "Library Compiler User Guide" for information on pad cells. Either remove the invalid attribute or add the pad_type, the pad_cell, or the auxiliary_pad_cell attribute.

LBDB-202

(error) A nonpad '%s' cell has a '%s' pin/pg_pin with a '%s' attribute.

Description

This error message occurs when a pad pin/pg_pin attribute is specified in a nonpad cell.

The following example shows an instance where this message occurs: In the following example, there is an *is_pad* attribute at the pin level, but there is no pad attribute at the cell level, so the *read_lib* command issues the error message:

```
cell(lbdb202){
      area : 0.0;
      pin(Z)  {
        is_pad : true;
        direction : output
        drive_current : 2.0;
        function : "A"
      }
      pin(A) {
        direction : input;
        capacitance : 1.0;
    }
  }
```

Feedback

The following is an example message: The following is an example of the error message:

```
Error: Line 3581, A nonpad 'lbdb202' cell has a 'Z' pin/pg_pin
       with a 'is_pad' attribute. (LBDB-202)
```

What Next

Either remove the invalid attribute or add the *pad_cell* attribute. See the Library Compiler documentation for information on pad cells.

See Also

- read_lib

LBDB-203

(error) The nonpad '%s' pin has a '%s' attribute.

Description

This message indicates that you specified a pad cell with pad_type and pad_cell attributes defined and a nonpad pin with a hysteresis attribute.

The following example shows an instance where this message occurs:

```
cell(lbdb203){
    area : 0.0;
    pad_type : clock;
    pad_cell : true;
    pin(Z)  {
      direction : output;
      hysteresis : true;
      function : "A";
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Error: Line 3584, The nonpad 'Z' pin has a 'hysteresis' attribute.
 (LBDB-203)
```

What Next

Refer to the "Library Compiler User Guide" for information on pad cells. Either remove the pad cell attributes or add the pad pin attributes.

Feedback

LBDB-204

(error) The '%s' %s pin cannot have a '%s' attribute.

Description

This message indicates that you specified a pad pin attribute on a pin with an invalid direction.

The following example shows an instance where this message occurs:

```
cell(lbdb204){
    area : 0.0;
    pad_cell : true;
    pin(Z)  {
      direction : output;
      is_pad : true;
      hysteresis : true;
      function : "A";
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Error: Line 3584, The 'Z' output pin cannot have a 'hysteresis'
 attribute. (LBDB-204)
```

What Next

Refer to the "Library Compiler User Guide" for information on pad cells. Either change the pin's direction or move the attribute to the correct pin.

LBDB-205

(warning) The '%s' pad pin is missing a '%s' attribute.

Description

This message indicates that you specified an output or inout pad pin without a *drive_current* attribute.

The following example shows an instance where this message occurs:

```
cell(lbdb205){
    area : 0.0;
    pad_cell : true;
    pin(Z)  {
```

```
      direction : output;
      is_pad : true;
      hysteresis : true;
      function : "A";
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Warning: Line 3596, The 'Z' pad pin is missing a 'drive_current'
 attribute. (LBDB-205)
```

What Next

Refer to the "Library Compiler User Guide" for information on pad cells and pins. Add the missing attribute to the pin.

LBDB-206

(error) The '%s' pad cell has no pad pins.

Description

This message indicates that you specified a pad cell with pad_type and pad_cell attributes defined but you did not specify pad pin attributes associated with any pin in the cell.

The following example shows an instance where this message occurs:

```
cell(lbdb206){
    area : 0.0;
    pad_type : clock;
    pad_cell : true;
    pin(Z)  {
      direction : output
      function : "A"
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Error: Line 3575, The 'lbdb206' pad cell has no pad pins. (LBDB-206)
```

Feedback

What Next

Refer to the "Library Compiler User Guide" for information on pad cells. Remove either the pad cell attributes or add the pad pin attributes.

LBDB-207

(warning) The '%s' pad cell has more than one pad pin. \n

Description

This message indicates that you specified more than one pad pin in a pad cell.

The following example shows an instance where this message occurs:

```
cell(lbdb207) {
    area : 0.0;
    pad_cell : true;
    bond_pads : 1;
    driver_sites : 1;
    pin(PAD ) {
      direction : input;
      is_pad : true;
      input_voltage : CMOS;
      capacitance : 1.0;
    }
    pin(PAD1 ) {
      direction : input;
      is_pad : true;
      input_voltage : CMOS;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction : output;
      function : "PAD PAD1";
      timing() {
        intrinsic_fall : 1.0;
        intrinsic_rise : 1.0;
        fall_resistance : 0.50;
        rise_resistance : 0.50;
        related_pin :"PAD PAD1";
      }
    }
  }
```

In this case, there are two pad pins: 'PAD' and 'PAD1'.

The following is an example message:

```
Warning: Line 33, The 'lbdb207' pad cell has more than one pad pin.
 (LBDB-207)
```

Feedback

What Next

Refer to the "Library Compiler User Guide" for information on pad cells.

LBDB-208

(error) The %s '%s' pad cell cannot be a 'clock' pad.

Description

This message indicates you specified an output pad pin with the is_pad attribute on a clock pad. Library Compiler accepts clock pads only on input pins.

The following example shows an instance where this message occurs:

```
cell(lbdb208) {
    area : 0.0;
    pad_cell : true;
    pad_type : clock;
    pin(PAD ) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction : output;
      is_pad : true;
      function : "PAD";
      output_voltage : CMOS_OUT;
      timing() {
        intrinsic_fall : 1.0;
        intrinsic_rise : 1.0;
        fall_resistance : 0.0;
        rise_resistance : 0.0;
        related_pin :"PAD";
      }
    }
  }
```

The following is an example message:

```
Error: Line 65, The output 'lbdb208' pad cell cannot be a 'clock' pad.
 (LBDB-208)
```

What Next

Refer to the "Library Compiler User Guide" for information on pad cells. Check the library source file, and specify the is_pad attribute to an input pin.

Feedback

LBDB-209

(error) A '%s' attribute cannot be specified on a\n \tpin unless a pull_up or pull_down driver_type is specified.

Description

This message indicates that you specified a *pulling_resistance* or a *pulling_current* attribute on a pin without specifying the pullup or pulldown driver type.

The following example shows an instance where this message occurs:

```
pin(A) {
      direction : output;
      pulling_resistance : 100;
      ...
    }
```

In this case, the driver_type is missing. To fix the problem, add the statement,

```
driver_type : pull_up;
```

The following is an example message:

```
Error: Line 355, A 'pulling_resistance' attribute cannot be specified on
 a
       pin unless a pull_up or pull_down driver_type is specified.
 (LBDB-209)
```

What Next

Change the library file by either adding the driver_type attribute to the specified pin or removing the pulling_resistance or pulling_current attribute.

LBDB-210

(error) The pulling_current value cannot be 0.0.

Description

This message indicates that you specified a zero value for the *pulling_current* attribute.

The following example shows an instance where this message occurs:

```
pulling_current : 0.0;
```

The following is an example message:

```
Error: Line 357, The pulling_current value cannot be 0.0. (LBDB-210)
```

Feedback

What Next

Change the value of the attribute to a nonzero value.

LBDB-211

(error) The '%s' driver_type cannot be specified on a\n \tpin that already has a %s driver_type specified.

Description

This message indicates that you specified an incompatible set of driver types on a pin. Library Compiler fails if the driver_type value includes the following combinations:

```
* pull_up and pull_down
        * pull_up and bus_hold
        * pull_down and bus_hold
        * open_drain and open_source
        * open_drain and bus_hold
        * open_source and bus_hold
```

The following example shows an instance where this message occurs:

```
cell(lbdb211) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Z2) {
      direction : output;
      function : "A";
      driver_type : "pull_up pull_down";
      timing() {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        related_pin : "A";
      }
    }
  }
```

The following is an example message:

```
Error: Line 84, The 'pull_down' driver_type cannot be specified on a
       pin that already has a 'pull_up' driver_type specified. (LBDB-211)
```

What Next

Refer to the "Library Compiler User Guide" for driver_type information. Remove the incompatible values of the driver_type attribute.

Feedback

LBDB-212

(error) The 'open_%s' driver_type cannot be specified on\n \tan input pin.

Description

This message indicates that you specified an invalid *open_source* or *open_drain* driver_type value on an input_pin.

The following example shows an instance where this message occurs:

```
cell(lbdb212) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;
      driver_type : "open_drain";
    }
    pin(Z2) {
      direction : output;
      function : "A";
      timing() {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        related_pin : "A";
      }
    }
  }
```

The following is an example message:

```
Error: Line 78, The 'open_drain' driver_type cannot be specified on
       an input pin. (LBDB-212)
```

What Next

Refer to the "Library Compiler User Guide" for driver_type information. Remove the invalid value of the driver_type attribute.

LBDB-213

(error) The '%s' area attribute cannot be specified\n \ton a pin of a cell that is not a pad cell.

Description

This message indicates that you specified a user-defined cell area value for pad cells and applied it to a nonpad cell.

Feedback

The following example shows an instance where this message occurs:

```
define_cell_area(my_area,pad_slots);

    cell(NON_PAD_CELL) {
      area : 1;
      my_area : 10;
    }
```

The following is an example message:

```
Error: Line 29, The 'my_area' area attribute cannot be specified
       on a pin of a cell that is not a pad cell. (LBDB-213)
```

What Next

Change the library file, and either make the cell a pad cell or remove the pad information from the cell.

LBDB-214

(error) The '%s' area attribute of '%s' type\n \tcannot be specified on a pin of a cell that is not a pad cell\n \tor an auxiliary pad cell.

Description

This message indicates that you specified a user-defined cell area value for pad cells or auxiliary pad cells and applied it to a nonpad cell.

The following example shows an instance where this message occurs:

```
define_cell_area(your_area,pad_driver_sites);

    cell(NON_PAD_CELL) {
      area : 1;
      your_area : 10;
    }
```

The following is an example message:

```
Error: Line 29, The 'your_area' area attribute of 'pad_driver_sites' type
       cannot be specified on a pin of a cell that is not a pad cell
       or an auxiliary pad cell. (LBDB-214)
```

What Next

Change the library file and either make the cell a pad cell or remove the pad information from the cell.

Feedback

LBDB-215

(error) The '%s' attribute cannot be specified\n \ton the '%s' input pin.

Description

This message indicates that you specified an invalid attribute on an input pin. Library Compiler fails if the following attributes are associated with an input pin.

```
* A driver_type attribute whose value is bus_hold
        * A slew_control attribute
        * An edge_rate_rise attribute
        * An edge_rate_fall attribute
        * An edge_rate_rise_load attribute
        * An edge_rate_fall_load attribute
        * A reference_resistance attribute
```

The following example shows an instance where this message occurs:

```
pin(B) {
            direction : input;
            capacitance : 1.0;
            fanout_load : 1.0;

            edge_rate_breakpoint_r0 : 0.000;
            edge_rate_breakpoint_f0 : 0.000;
            edge_rate_breakpoint_r1 : 0.010;
            edge_rate_breakpoint_f1 : 0.010;

            edge_rate_rise : 1.0;
            edge_rate_load_rise : 1.0;
            edge_rate_fall     : 1.0;
            edge_rate_load_fall : 1.0;
         }
```

The following is an example message:

```
Error: Line 110, The 'edge_rate_rise' attribute cannot be specified
       on the 'B' input pin. (LBDB-215)
```

What Next

Check the library source file, and delete the invalid attribute from the input pin.

LBDB-216

(error) The '%s' scaled_cell's '%s' pin has a different\n \tnumber of timing arcs than the corresponding pin on the '%s' cell.

Feedback

Description

This message indicates that a timing group is missing in one of the output pins of either the specified cell or the scaled_cell.

The following example shows an instance where this message occurs:

```
library(lbdb216) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
    }
    cell(IVV) {
      area : 1;
      pin(A) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A'";
        timing() {
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          slope_rise : 0.0;
          slope_fall : 0.0;
          related_pin : "A";
        }
      }
    }

    scaled_cell(IVV,WCCOM) {
      area : 1;
      pin(A) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A'";
      }
    }
  }
```

In this case, add the following timing group to the 'Z' pin in the scaled_cell to fix the problem.

```
timing() {
          intrinsic_rise : 0.3;
```

```
          intrinsic_fall : 0.3;
          rise_resistance : 0.3;
          fall_resistance : 0.3;
          slope_rise : 0.0;
          slope_fall : 0.0;
          related_pin : "A";
        }
```

The following is an example message:

```
Error: Line 40, The 'WCCOM' scaled_cell's 'Z' pin has a different
       number of timing arcs than the corresponding pin on the 'IVV'
 cell. (LBDB-216)
```

What Next

Add the missing timing group to the specified output pin in either the cell or the scaled_cell.

LBDB-217

(error) The '%s' cell's '%s' pin has a timing arc without\n \ta counterpart on the scaled_cell(%s,%s).

Description

Each timing arc in the regular cell needs a matched timing arc on the same pin in the scaled_cell group. This message indicates that a matching timing arc is not found in the library source file.

The following example shows an instance where this message occurs:

```
library(lbdb217) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
    }
    cell(AND) {
      area : 1;
      pin(A B) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A B";
        timing() {
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
```

```
            rise_resistance : 0.1;
            fall_resistance : 0.1;
            slope_rise : 0.0;
            slope_fall : 0.0;
            related_pin : "A B";
          }
        }
      }

      scaled_cell(AND,WCCOM) {
        area : 1;
        pin(A B) {
          direction : input;
          capacitance : 1;
        }
        pin(Z) {
          direction : output;
          function : "A B";
          timing() {
            intrinsic_rise : 0.1;
            intrinsic_fall : 0.1;
            rise_resistance : 0.1;
            fall_resistance : 0.1;
            slope_rise : 0.0;
            slope_fall : 0.0;
            related_pin : "A";
          }
          timing() {
            intrinsic_rise : 0.3;
            intrinsic_fall : 0.3;
            rise_resistance : 0.3;
            fall_resistance : 0.3;
            slope_rise : 0.0;
            slope_fall : 0.0;
            related_pin : "A ";
          }
        }
      }
    }
```

In this case, The timing arc between 'Z' and 'A' is defined once in the 'AND' cell and twice in the 'AND' scaled_cell. To fix the problem, remove one of the timing arcs.

The following is an example message:

```
Error: Line 42, The 'AND' cell's 'Z' pin has a timing arc without
       a counterpart on the scaled_cell(AND,WCCOM). (LBDB-217)
```

What Next

Find the missing timing group in the scaled_cell and add it, or remove one of the extra timing groups in the cell.

Feedback

LBDB-218

(warning) The 'direction' of the '%s' scaled_cell pin \n \tdoes not match that of the same pin name on the '%s' cell.\n \tResetting the scaled_cell pin's direction to match both directions.

Description

This message indicates that a direction attribute of a scaled_cell pin is different from the same pin on the primary cell. Library Compiler matches the direction of the scaled_cell pin to the direction of the primary pin.

The following example shows an instance where this message occurs:

```
cell(AND) {
    area : 1;
    pin(A B C) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : inout;
      function : "A B";
      three_state : "C";
      timing() {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A B C";
      }
      timing() {
        timing_type : three_state_disable;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C";
      }
    }
    }
    scaled_cell(AND,WCCOM) {
      area : 1;
      pin(A B C) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A B";
        timing() {
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
```

```
            rise_resistance : 0.1;
            fall_resistance : 0.1;
            slope_rise : 0.0;
            slope_fall : 0.0;
            related_pin : "A B";
          }
        }
    }
```

The following is an example message:

```
Warning: Line 313, The 'direction' of the 'Z' scaled_cell pin
         does not match that of the same pin name on the 'AND' cell.
         Resetting the scaled_cell pin's direction to match both
 directions. (LBDB-218)
```

What Next

Check the library source file, and make sure the directions are the same.

LBDB-219

(error) The (%s,%s) scaled_cell has duplicate\n \ttiming arcs for the '%s' pin. It is unclear\n \twhich arc corresponds to the arcs in the '%s' cell.

Description

This message indicates that a scaled_cell has duplicate timing arcs between two pins. Library Compiler fails to recognize the equivalent timing arc in the primary cell.

What Next

Check the library source file, and remove the second timing arc.

LBDB-220

(error) The '%s' %s_voltage group has no '%s' attribute\n \tspecified. This attribute is essential in defining valid voltages.

Description

This message indicates that an input_voltage or an output_voltage group has one of its attributes missing. For an input_voltage group, Library Compiler fails if any of the vil, vih, vimin, or vimax attributes is missing. For an output_voltage group, Library Compiler fails if any of the vol, voh, vomin, or vomax attributes is missing.

The following example shows an instance where this message occurs:

```
output_voltage(CMOS_OUT) {
    vil : 1.5;
```

```
    vih : 3.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }
```

In this case, either there is a typo where the output_voltage is specified instead of input_voltage, or the vol, voh, vomin, and vomax are not specified for the output_voltage.

The following is an example message:

```
Error: Line 31, The 'CMOS_OUT' output_voltage group has no 'vol'
 attribute
       specified. This attribute is essential in defining valid voltages.
 (LBDB-220)
```

What Next

Check the library source file, and add the missing attribute to the voltage group.

LBDB-221

(warning) The '%s' %s_voltage group has a %s value,\n \twhich is %s %s.

Description

This message indicates that an *input_voltage* or an *output_voltage* has inconsistent values for its attributes. Library Compiler issues warnings in these cases:

```
* vil value is less than vimin value.
        * vih value is greater than vimax value.
        * vol value is less than vomin value.
        * voh value is greater than vomax value.
```

The following example shows an instance where this message occurs:

```
input_voltage(CMOS) {
    vil : -1.5;
    vih : 3.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }
```

In this case, the vil value is less than the vimin value.

The following is an example message:

```
Warning: Line 25, The 'CMOS' input_voltage group has a vil value,
        which is less than vimin. (LBDB-221)
```

Feedback

What Next

Change the specified attribute value to be consistent with the minimum or the maximum values.

LBDB-222

(error) The fpga_family attribute is required when\n \tthe fpga_cell_type attribute is specified.

Description

This message indicates that in an fpga cell you specified an *fpga_cell_type* attribute without the *fpga_family* attribute.

The following example shows an instance where this message occurs:

```
cell( lbdb222 ) {
        area : 1;
        fpga_cell_type : CLB;

        pin( K ) {
            direction : input;
            capacitance : 0.0;
        }
        ...
    }
```

In this case, to fix the problem, add the statement to the cell.

```
fpga_family : "x4000";
```

The following is an example message:

```
Error: Line 28, The fpga_family attribute is required when
        the fpga_cell_type attribute is specified. (LBDB-222)
```

What Next

Add the missing fpga_family attribute to the cell.

LBDB-223

(error) The fpga_cell_type attribute is required when\n \tthe fpga_family attribute is specified.

Description

This message indicates that in an fpga cell you specified an *fpga_family* attribute without the *fpga_cell_type* attribute.

The following example shows an instance where this message occurs:

```
cell(lbdb223) {
        area : 1;
        fpga_family : "x4000";

        pin( K ) {
            direction : input;
            capacitance : 0.0;
        }
        ...
    }
```

In this case, to fix the problem, add the statement to the cell.

```
fpga_cell_type : CLB;
```

The following is an example message:

```
Error: Line 28, The fpga_cell_type attribute is required when
        the fpga_family attribute is specified. (LBDB-222)
```

What Next

Add the missing fpga_cell_type attribute to the cell.

LBDB-224

(error) The fpga_timing_type is required on all arcs \n \twhen fpga_cell_type and fpga_family are specified.

Description

This message indicates that you did not specify *fpga_timing_type* groups in a cell with the *fpga_family* and the *fpga_cell_type* attributes.

The following example shows an instance where this message occurs:

```
cell(INV) {
      fpga_family : "x4000";
      fpga_cell_type : CLB;
      area : 1;
      pin(X) {
        function : "A'";
        direction : output;
        timing() {
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
        }
```

```
      }
      pin(A) {
        direction : input;
        capacitance :  0.1;
        fanout_load :  0.1;
      }
    }
```

To fix the problem, add the attribute to the timing group.

```
timing() {
          fpga_timing_type : ICK;
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
        }
```

The following is an example message:

```
Error: Line 208, The fpga_timing_type is required on all arcs
        when fpga_cell_type and fpga_family are specified. (LBDB-224)
```

What Next

Add the missing fpga_timing_type groups to all the pins of the cell.

LBDB-225

(error) The fpga_timing_type is invalid when the fpga_cell_type\n \tand the fpga_family attributes are not defined on a cell.

Description

This message indicates that you specified fpga_timing_type in a timing group of a pin without defining the fpga_family and the fpga_cell_type attributes at the cell level.

The following example shows an instance where this message occurs:

```
cell(lbdb225) {
      area : 1;
      pin(X) {
        function : "A'";
        direction : output;
        timing() {
          fpga_timing_type : ICK;
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
```

```
        }
      }
      pin(A) {
        direction : input;
        capacitance :  0.1;
        fanout_load :  0.1;
      }
    }
```

To fix the problem, add the sample statements at the cell level.

```
fpga_family : "x4000";
      fpga_cell_type : CLB;
```

The following is an example message:

```
Error: Line 30, The fpga_timing_type is invalid when the fpga_cell_type
        and the fpga_family attributes are not defined on a cell.
 (LBDB-225)
```

What Next

Add the missing attribute to the library file.

LBDB-226

(error) The FPGA CLB cell type from the x2000 family requires\n \tA, B, C, D, K, X, and Y pins.

Description

This message indicates that you specified an incomplete CLB FPGA cell with missing pins from the x2000 family.

The following example shows an instance where this message occurs:

```
cell(lbdb226) {
      fpga_family : "x2000";
      fpga_cell_type : CLB;
      area : 1;
      pin(X) {
        function : "A'";
        direction : output;
        timing() {
          fpga_timing_type : ICK;
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
        }
      }
```

Feedback

```
      pin(A) {
        direction : input;
        capacitance :  0.1;
        fanout_load :  0.1;
      }
    }
```

The following is an example message:

```
Error: Line 22, The FPGA CLB cell type from the x2000 family requires
        A, B, C, D, K, X, and Y pins. (LBDB-226)
```

What Next

Add the missing pins to the cell.

LBDB-227

(error) The FPGA IOB cell type from the x2000 family requires\n \tO, T, K, I, and PAD pins.

Description

This message indicates that you specified an incomplete IOB FPGA cell with missing pins from the x2000 family.

The following example shows an instance where this message occurs:

```
cell(lbdb227) {
      fpga_family : "x2000";
      fpga_cell_type : IOB;
      area : 1;
      pin(X) {
        function : "A'";
        direction : output;
        timing() {
          fpga_timing_type : ICK;
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
        }
      }
      pin(A) {
        direction : input;
        capacitance :  0.1;
        fanout_load :  0.1;
      }
    }
```

Feedback

The following is an example message:

```
Error: Line 22, The FPGA IOB cell type from the x2000 family requires
        O, T, K, I, and PAD pins. (LBDB-227)
```

What Next

Add the missing pins to the cell.

LBDB-228

(error) The FPGA CLB cell type from the x3000 family requires \n \tA, B, C, D, E, K, EC, DI, RD, X, Y, and GSR pins.

Description

This message indicates that you specified an incomplete CLB FPGA cell with missing pins from the x3000 family.

The following example shows an instance where this message occurs:

```
cell(lbdb228) {
      fpga_family : "x3000";
      fpga_cell_type : CLB;
      area : 1;
      pin(X) {
        function : "A'";
        direction : output;
        timing() {
          fpga_timing_type : ICK;
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
        }
      }
      pin(A) {
        direction : input;
        capacitance :  0.1;
        fanout_load :  0.1;
      }
    }
```

The following is an example message:

```
Error: Line 22, The FPGA CLB cell type from the x3000 family requires
        A, B, C, D, E, K, EC, DI, RD, X, Y, and GSR pins. (LBDB-228)
```

What Next

Add the missing pins to the cell.

Feedback

LBDB-229

(error) The FPGA IOB cell type from the x3000 family requires \n \tO, T, IK, OK, I, Q, PAD, and GSR pins.

Description

This message indicates that you specified an incomplete IOB FPGA cell with missing pins from the x3000 family.

The following example shows an instance where this message occurs:

```
cell(lbdb229) {
      fpga_family : "x3000";
      fpga_cell_type : IOB;
      area : 1;
      pin(X) {
        function : "A'";
        direction : output;
        timing() {
          fpga_timing_type : ICK;
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
        }
      }
      pin(A) {
        direction : input;
        capacitance :  0.1;
        fanout_load :  0.1;
      }
    }
```

The following is an example message:

```
Error: Line 22, The FPGA IOB cell type from the x3000 family requires
        O, T, IK, OK, I, Q, PAD, and GSR pins. (LBDB-229)
```

What Next

Add the missing pins to the cell.

LBDB-230

(error) The FPGA CLB cell type from the x4000 family requires\n \tF1-F4, G1-G4, C1-C4, K, X, Y, XQ, YQ, GSR, CIN, and COUT pins.

Feedback

Description

This message indicates that you specified an incomplete CLB FPGA cell with missing pins from the x4000 family.

The following example shows an instance where this message occurs:

```
cell(lbdb230) {
      fpga_family : "x4000";
      fpga_cell_type : CLB;
      area : 1;
      pin(X) {
        function : "A'";
        direction : output;
        timing() {
          fpga_timing_type : ICK;
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
        }
      }
      pin(A) {
        direction : input;
        capacitance :  0.1;
        fanout_load :  0.1;
      }
    }
```

The following is an example message:

```
Error: Line 22, The FPGA CLB cell type from the x4000 family requires
        F1-F4, G1-G4, C1-C4, K, X, Y, XQ, YQ, GSR, CIN, and COUT pins.
 (LBDB-230)
```

What Next

Add the missing pins to the cell.

LBDB-231

(error) The FPGA IOB cell type from the x4000 family requires\n \tO, T, IK, OK, I1, I2, PAD, and GSR pins.

Description

This message indicates that you specified an incomplete IOB FPGA cell with missing pins from the x4000 family.

Feedback

The following example shows an instance where this message occurs:

```
cell(lbdb231) {
      fpga_family : "x4000";
      fpga_cell_type : IOB;
      area : 1;
      pin(X) {
        function : "A'";
        direction : output;
        timing() {
          fpga_timing_type : ICK;
          intrinsic_rise  : 0.1;
          intrinsic_fall  : 0.1;
          rise_resistance : 1.0;
          fall_resistance : 1.0;
          related_pin : "A";
        }
      }
      pin(A) {
        direction : input;
        capacitance :  0.1;
        fanout_load :  0.1;
      }
    }
```

The following is an example message:

```
Error: Line 22, The FPGA IOB cell type from the x4000 family requires
        O, T, IK, OK, I1, I2, PAD, and GSR pins. (LBDB-231)
```

What Next

Add the missing pins to the cell.

LBDB-232

(error) The attribute '%s' cannot be %s while the pin has %s.

Description

The first specified attribute in the pin cannot be the value with the second specified attribute on the same pin has been defined.

For example, the *is_unconnected* attribute cannot be specified on a pin with *related_power_pin* or *related_ground_pin* attribute, or the pin is a feedthrough pin, i.e. in a *short* path.

The following example shows an instance where this message occurs:

```
cell(Block) {
    area : 2;
    pin(A) {
```

Feedback

```
      direction : input;
      capacitance : 1.0;
      related_power_pin : VDD ;
      related_ground_pin : VSS ;
      is_unconnected : true ;
    }
    ...

  }
```

The following is an example message:

```
Error: Line 84, The  attribute 'is_unconnected' cannot be true while
 the pin has related_power_pin/related_groud_pin or is feedthrough.
 (LBDB-232)
```

What Next

Check the specification of the cell, remove the attribute that incorrecly defined.

LBDB-233

(warning) The attribute '%s' should be defined while\n \tthe pin has no power supply and is not a feedthrough pin.

Description

The specified attribute in the pin should be defined when the pin has no related_power_pin/related_ground_pin and is not a feedthrough pin if it should be unconnected.

Library Compiler will derive the attribute automatically during read_lib.

The following example shows an instance where this message occurs:

```
cell(Block) {
    area : 2;

    pin(Z) {
      direction : output;
      function : "A";
    }
  }
```

The following is an example message:

```
Warning: Line 84, The attribute 'is_unconnected' should be defined while
     the pin has no power supply and is not a feedthrough pin. (LBDB-233)
```

What Next

Adding related power/ground pin if the pin should not be unconnected.

Feedback

LBDB-235

(error) This %s voltage or power supply group is not defined.

Description

This message indicates the specified voltage or the power supply associated with the signal level is not defined in the library source file. The voltage can either be input or output.

The following example shows an instance where this message occurs:

```
pin(PAD ) {
        is_pad : true;
        input_voltage : lbdb235;
        direction   : input;
        capacitance : 35.000000;
        fanout_load : 0.000000;
      }
      pin(PAD1 ) {
        is_pad : true;
        input_signal_level : VDD1;
        direction   : input;
        capacitance : 35.000000;
        fanout_load : 0.000000;
      }
```

In this case, the 'lbdb235' input_voltage is not defined. To fix the problem, add the following input_voltage:

```
input_voltage(lbdb235) {
    vil         : 0.8 ;
    vih         : 2.0 ;
    vimin       : -0.3 ;
    vimax       : VDD + 0.3 ;
   }
```

In addition, the 'VDD1' input_signal_level is not defined. To fix the problem, add the following power_supply group:

```
power_supply() {
    default_power_rail : VDD0;
    power_rail (VDD1, 5.0);
   }
```

The following is an example message:

```
Error: Line 23, This input voltage or power supply group is not defined.
 (LBDB-235)
Error: Line 30, This input voltage or power supply group is not defined.
 (LBDB-235)
```

Feedback

What Next

Add the missing voltage or the power supply to the library file.

LBDB-236

(error) An %s pin cannot specify an %s attribute.

Description

This message indicates that there is a mismatch between the direction of a pin and the voltage attribute. Library Compiler fails if you specify an input_voltage to an output pin and an output_voltage to an input pin.

The following example shows an instance where this message occurs:

```
cell(lbdb236) {
    area : 0.0;
    pad_cell : true;
    pad_type : clock;
    pin(PAD ) {
      direction : input;
      is_pad : true;
      input_voltage : CMOS;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction : output;
      is_pad : true;
      function : "PAD";
      input_voltage : CMOS;
      timing() {
        intrinsic_fall : 1.0;
        intrinsic_rise : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin :"PAD";
      }
    }
  }
```

In this case, the 'Y' pin has an input_voltage specified. To fix the problem, change the voltage to an output_voltage attribute.

The following is an example message:

```
Error: Line 71, An output pin cannot specify an input_voltage attribute.
 (LBDB-236)
```

Feedback

What Next

Check the library source file, and fix the invalid attribute, either the direction of the pin or the voltage attribute.

LBDB-236w

(warning) An %s pin cannot specify an %s attribute.

Description

This message indicates that there is a mismatch between the direction of a pin and the voltage attribute. Library Compiler fails if you specify an input_voltage to an output pin and an output_voltage to an input pin.

The following example shows an instance where this message occurs:

```
cell(lbdb236) {
    area : 0.0;
    pad_cell : true;
    pad_type : clock;
    pin(PAD ) {
      direction : input;
      is_pad : true;
      input_voltage : CMOS;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction : output;
      is_pad : true;
      function : "PAD";
      input_voltage : CMOS;
      timing() {
        intrinsic_fall : 1.0;
        intrinsic_rise : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin :"PAD";
      }
    }
  }
```

In this case, the 'Y' pin has an input_voltage specified. To fix the problem, change the voltage to an output_voltage attribute.

The following is an example message:

```
Warning: Line 71, An output pin cannot specify an input_voltage
 attribute. (LBDB-236w)
```

What Next

Check the library source file, and fix the invalid attribute, either the direction of the pin or the voltage attribute.

LBDB-238

(warning) No '%s' attribute has been specified for the\n \tlibrary. This attribute is needed in %s libraries.

Description

This message indicates that you did not specify any of the following attributes in the technology library.

```
* time_unit
        * capacitance_load_unit
        * pulling_resistance_unit
        * voltage_unit
        * current_unit
        * leakage_power_unit
```

The following example shows an instance where this message occurs: Add any of the following examples of attributes to the library:

```
capacitive_load_unit(0.042000,pf) ;
    voltage_unit  : "1V";
    current_unit  : "1mA";
    pulling_resistance_unit : "1kohm";
    time_unit : "1ns";
    leakage_power_unit : "1nW";
```

The following is an example message:

```
Warning: No 'capacitive_load_unit' attribute has been specified for the
         library. This attribute is needed in technology libraries.
 (LBDB-238)
```

What Next

Add the missing attribute to the library source file.

LBDB-239

(error) The '%s' driver_type cannot coexist\n \twith the '%s' attribute on the '%s' pin.

Feedback

Description

The *driver_type* specified in the pin cannot coexist with the attribute on the same pin. For example, a pin with a *bus_hold driver_type* is tied to a DC source. A function attribute or *three_state* attribute cannot be specified on a *bus_hold* pin.

The following example shows an instance where this message occurs:

```
cell(lbdb239) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
    pin(Z2) {
      direction : output;
      function : "A";
      driver_type : "bus_hold";
      timing() {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        related_pin : "A";
      }
    }
  }
```

The following is an example message:

```
Error: Line 84, The  'bus_hold' driver_type cannot coexist
        with the 'function' attribute on the 'Z2' pin. (LBDB-239)
```

What Next

Check the specification of the cell, and make the appropriate change to the *driver_type* attribute or other attributes in the faulty pin group.

LBDB-240

(error) The '%s' cell area attribute has already been defined.

Description

This message indicates that the user-defined cell area is specified twice.

The following example shows an instance where this message occurs:

```
define_cell_area(my_area,pad_slots);
    define_cell_area(my_area,pad_slots);
```

Feedback

The following is an example message:

```
Error: Line 24, The 'my_area' cell area attribute has already been
 defined. (LBDB-240)
```

What Next

Remove the second definition of the cell area attribute.

LBDB-241

(warning) Multiple cell area definitions (%s, %s) map\n \tonto the same '%s' area. Using the last one encountered.

Description

This message indicates that you specified multiple defined_cell_area attributes with the same area kind. Library Compiler uses the last one encountered.

The following example shows an instance where this message occurs:

```
define_cell_area(my_area,pad_slots);
    define_cell_area(your_area,pad_slots);
```

The following is an example message:

```
Warning: Line 24, Multiple cell area definitions (your_area, my_area) map
        onto the same 'pad_slots' area. Using the last one encountered.
 (LBDB-241)
```

What Next

Delete the redundant define_cell_area definitions.

LBDB-242

(warning) This '%s' timing arc has the same timing_type and\n \trelated_pin attributes as the timing arc on the line %d.

Description

This message indicates that on the same pin you defined two timing groups with the same timing_type and related_pin attributes. Design Compiler considers the timing arcs as two separate arcs.

The following example shows an instance where this message occurs:

```
pin(QN) {
    direction : output;
    function : "IQN";
    timing() {
```

Feedback

```
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 2.0;
      intrinsic_fall : 2.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP P";
    }
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
```

In this case, the 'QN' pin has the 'CP' related_pin and the 'rising_edge' timing_type multiply defined.

The following is an example message:

```
Warning: Line 591, This 'QN' timing arc has the same timing_type and
         related_pin attributes as the timing arc on the line 583.
 (LBDB-242)
```

What Next

If it is a typo, change the library file, and delete the redundant timing groups.

LBDB-243

(warning) The '%s' combinational cell has a '%s' pin with\n \ta sequential timing arc containing the '%s' timing_type.

Description

This message indicates that you specified one of the cell's timing arcs as sequential, while the function of this cell is combinational. Library Compiler warns you if any of the following timing types is defined on a combinational cell:

```
* rising_edge
       * falling_edge
```

```
        * preset
        * clear
        * setup_rising
        * setup_falling
        * hold_rising
        * hold_falling
        * recovery_rising
        * recovery_falling
        * skew_rising
        * skew_falling
        * removal_rising
        * removal_falling
```

The following example shows an instance where this message occurs:

```
cell(lbdb243) {
    area : 1;
    pin(A B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A B";
      }
    }
  }
```

In this case, the 'Z' pin has an invalid 'rising_edge' timing_type.

The following is an example message:

```
Warning: Line 84, The 'lbdb243' combinational cell has a 'Z' pin with
         a sequential timing arc containing the 'rising_edge'
 timing_type. (LBDB-243)
```

What Next

Change the library source file, and fix the timing_type of the specified pin.

LBDB-246

(warning) The default_wire_load_selection is not defined.\n \tBy default, the '%s' wire_load_selection group is used.

Feedback

Description

The *default_wire_load_selection* attribute is undefined in this library. The *default_wire_load_selection* attribute is required when multiple wire_load_selection groups are specified in a library. If there is only one wire_load_selection group defined in a library, Library Compiler automatically sets the *default_wire_load_selection* attribute to the only available wire_load_selection group.

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }
  wire_load_selection(test) {
    wire_load_from_area(27,10,"10x10");
    wire_load_from_area(27,100,"10x10");
    wire_load_from_area(0,28,"05x05");
    wire_load_from_area(2,10,"15x10");
  }
```

The following is an example message:

```
Warning: Line 50, The default_wire_load_selection is not defined.
        By default, the 'test' wire_load_selection group is used.
 (LBDB-246)
```

What Next

Set the *default_wire_load_selection* attribute to avoid this warning message, or ignore this message.

LBDB-247

(error) The default_wire_load_selection is not defined.\n \tThe default_wire_load_selection attribute is required when more than one\n \twire_load_selection group is specified.

Description

The *default_wire_load_selection* attribute is undefined in this library. Library Compiler requires this attribute because there is more than one wire_load_selection group specified.

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
```

```
    slope : 0.186 ;
    fanout_length(1,0.39) ;
  }

  wire_load_selection(test) {
    wire_load_from_area(0,25,"05x05");
  }
  wire_load_selection(test1) {
    wire_load_from_area(0,27,"05x05");
  }
```

To fix the problem, add this statement to the library:

```
default_wire_load_selection : test;
```

The following is an example message:

```
Error: Line 0, The default_wire_load_selection is not defined.
        The default_wire_load_selection attribute is required when more
 than one
        wire_load_selection group is specified. (LBDB-247)
```

What Next

Set the *default_wire_load_selection* attribute to be one of the wire_load_selection groups.

LBDB-250

(warning) The '%s' pin already has a 'pulling_resistance' value.\n \tThe 'pulling_current' causes the 'pulling_resistance' value to be overwritten.

Description

This message indicates you specified both the *pulling_resistance* and the *pulling_current* attributes on the same pin. Library Compiler uses the pulling_current value and the nominal voltage to overwrite the pulling_resistance value.

The following example shows an instance where this message occurs:

```
pin(Y) {
        direction : output;
        capacitance : 1.0;
        driver_type : pull_up;
        is_pad : true;
        slew_control : low;
        drive_current : 1.0;
        output_voltage  : CMOS_OUT;
        function : "A";
        three_state : "GZ";
        pulling_resistance : 1000;
        pulling_current : 10;
     }
```

Feedback

The following is an example message:

```
Warning: Line 93, The 'Y' pin already has a 'pulling_resistance' value.
        The 'pulling_current' causes the 'pulling_resistance' value to be
 overwritten. (LBDB-250)
```

What Next

If you do not want the pulling_resistance value overwritten, delete the pulling_current attribute.

LBDB-251

(warning) The '%s' pin has a 'hysteresis' attribute but\n \tno 'input_voltage' attribute. Both attributes are needed.

Description

This message indicates that you specified the hysteresis attribute, but you did not specify the input_voltage attribute in a pad cell.

The following example shows an instance where this message occurs:

```
pin(PAD ) {
      direction : input;
      is_pad : true;
      hysteresis : true;
      capacitance : 1.0;
    }
```

To fix the problem, add this statement to the 'PAD' pin:

```
input_voltage : CMOS; /* CMOS is defined in the library */
```

The following is an example message:

```
Warning: Line 53, The 'PAD' pin has a 'hysteresis' attribute but
        no 'input_voltage' attribute. Both attributes are required.
 (LBDB-251)
```

What Next

Add the input_voltage attribute to the pin in the pad cell.

LBDB-252

(error) The '%s' %s group already exists and\n \tcannot be overwritten.

Feedback

Description

This message indicates that you multiply defined either an input_voltage or an output_voltage group. Library Compiler does not allow the overwriting of existing voltage groups.

The following example shows an instance where this message occurs:

```
input_voltage(CMOS) {
    vil : 1.5;
    vih : 3.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }

  input_voltage(CMOS) {
    vil : 2.5;
    vih : 4.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }
```

The following is an example message:

```
Error: Line 31, The 'CMOS' input_voltage group already exists and
       cannot be overwritten. (LBDB-252)
```

What Next

Delete the second specification of the voltage group.

LBDB-253

(error) The '%s' pin does not have all the %s slew rate attributes\n \tdefined. The '%s' attribute is missing.\n \tAll %s slew-rate attributes must be specified together as a group.

Description

This message indicates that not all slew rate attributes are specified in a pin. Library Compiler expects the following rise slew rate attributes defined together:

```
* rise_current_slope_before_threshold
        * rise_time_before_threshold
        * rise_current_slope_after_threshold
        * rise_time_after_threshold
```

and the following fall slew rate defined together:

```
* fall_current_slope_before_threshold
        * fall_time_before_threshold
        * fall_current_slope_after_threshold
        * fall_time_after_threshold
```

Feedback

The following example shows an instance where this message occurs:

```
cell(lbdb253) {
    area : 0.0;
    pad_cell : true;
    bond_pads : 1;
    driver_sites : 1;
    pin(PAD) {
      is_pad : true;
      direction : output;
      output_voltage : CMOS_OUT;
      function : "Y ";
      drive_current : 1.0;
      slew_control : high;
      rise_time_before_threshold : 1.0;
      rise_current_slope_after_threshold : -0.1;
      rise_time_after_threshold : 1.0;
      fall_current_slope_before_threshold : -0.1;
      fall_time_before_threshold : 1.0;
      fall_current_slope_after_threshold : 0.1;
      fall_time_after_threshold : 1.0;
      timing() {
        intrinsic_fall : 1.0;
        intrinsic_rise : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin :"Y";
      }
    }
    pin(Y ) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

In this case, the 'rise_current_slope_before_threshold' attribute is not specified for the 'PAD' pin.

The following is an example message:

```
Error: Line 88, The 'PAD' pin does not have all the rise slew rate
 attributes
        defined. The 'rise_current_slope_before_threshold' attribute is
 missing.
        All rise slew-rate attributes must be specified together as a
 group. (LBDB-253)
```

What Next

Check the library source file, and add the missing slew rate attribute.

Feedback

LBDB-254

(error) The '%s' edge rate related attribute \n \tcannot be specified on the '%s' output pin.

Description

This message indicates that you specified an edge rate attribute on an output pin.

The following example shows an instance where this message occurs:

```
pin(Z) {
            direction : output;
            function : "(A & B)";
            max_fanout : 25;

            edge_rate_breakpoint_r0 : 0.0;
            edge_rate_breakpoint_f0 : 0.0;
            edge_rate_breakpoint_r1 : 0.1;
            edge_rate_breakpoint_f1 : 0.1;

            edge_rate_rise : 1.0;
            edge_rate_load_rise : 1.0;
            edge_rate_fall : 0.1;
            edge_rate_load_fall : 1.0;
        }
```

The following is an example message:

```
Error: Line 120, The 'edge_rate_breakpoint_r0' edge rate related
 attribute
        cannot be specified on the 'Z' output pin. (LBDB-254)
```

What Next

Delete the attribute from the output pin group.

LBDB-255

(error) The 'vhdl_name' attribute of '%s' is invalid VHDL or\n \tconflicts with another 'vhdl_name' attribute.

Description

This message indicates that the cell or port *vhdl_name* attribute is either invalid VHDL (reserved VHDL name) or another cell or port has already been set to the same name.

The following example shows an instance where this message occurs:

```
cell(lbdb255) {
    area : 2;
    pin(A) {
```

```
      vhdl_name : "pinvhdl";
      direction : input;
      capacitance : 1;
    }
    pin(B) {
      vhdl_name : "pinvhdl" ;
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A^B";
      timing() {
        timing_sense : positive_unate;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A";
      }
      timing() {
        timing_sense : non_unate;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A B";
      }
    }
  }
```

In this case, both the 'A' and 'B' pin have the same value in the vhdl_name attribute.

The following is an example message:

```
Error: Line 93, The 'vhdl_name' attribute of 'pinvhdl' is invalid VHDL or
        conflicts with another 'vhdl_name' attribute. (LBDB-255)
```

What Next

If the attribute is invalid VHDL, change the library by fixing the value of the vhdl_name attribute. If the value of the attribute is redundant, either delete the second attribute or change its value.

LBDB-256

(warning) The 'vhdl_name' attribute of '%s' is invalid VHDL or\n \tconflicts with another 'vhdl_name' attribute. Renamed to '%s'.

Feedback

Description

This message indicates that the cell or port 'vhdl_name' attribute is either invalid VHDL or another cell or port has already been set to the same name.

Because this is an update_lib cell, the name is automatically renamed to a valid one.

The following example shows an instance where this message occurs:

```
cell (lbdb256) {
  area : 1;
  pin(IN) {
    vhdl_name : "port_X";
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    vhdl_name : "port_X";       /* rename after warning */
    direction : output;
    function : "IN'";
    timing () {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "IN";
    }
  }
}
```

The following is an example message:

```
Warning: Line 9, The 'vhdl_name' attribute of 'port_X' is invalid VHDL or
        conflicts with another 'vhdl_name' attribute. Renamed to
 'port_Xb'. (LBDB-256)
```

What Next

Change the file to update by changing the value of the vhdl_name attribute if you are not satisfied with the renamed value.

LBDB-257

(warning) The '%s' wire_load_selection group has been specified\n \twhile the default_wire_load_mode is %s 'top'. This causes \n \tthe 'wire_load_selection' group to work only for the top-level design.

Description

The 'default_wire_load_mode' is defined as, or defaults to, 'top', which causes the 'wire_load_selection' group to only work for the top-level design.

Feedback

The following example shows an instance where this message occurs:

```
default_wire_load_mode : 'top';
  wire_load_selection(test) {
    wire_load_from_area(27,100,"10x10");
    wire_load_from_area(10,25,"05x05");
  }
```

The following is an example message:

```
Warning: The 'test' wire_load_selection group has been specified
        while the default_wire_load_mode is default to 'top'. This causes
        the 'wire_load_selection' group to work only for the top-level
 design. (LBDB-257)
```

What Next

Set the default_wire_load_mode to 'segmented' or 'enclosed' modes to work with wire_load_selection group.

LBDB-258

(error) The '%s' driver_type cannot be specified\n \ton a inout pin without a three_state attribute.

Description

This message indicates that you specified a pull_up or a pull_down driver_type on an inout pin lacking a three_state attribute.

The following example shows an instance where this message occurs:

```
pin(A) {
      direction : inout;
      driver_type : pull_up;
      capacitance : 1;
      pulling_resistance : 100;
    }
```

The following is an example message:

```
Error: Line 354, The 'pull_up' driver_type cannot be specified
        on a inout pin without a three_state attribute. (LBDB-258)
```

What Next

Either delete the driver_type or add the three_state attribute.

LBDB-259

(error) The '%s' refers to a nonexistent or empty '%s'.

Feedback

Description

This message indicates that you specified a nonexistent or empty template group on a propagation delay in a nonlinear delay library.

The following example shows an instance where this message occurs:

```
fall_propagation(lbdb259_template) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

To fix the problem, add the following group to the library file,

```
lu_table_template(lbdb259_template) {
        variable_1 : input_net_transition;
        variable_2 : output_net_length;
        index_1 ("0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

The following is an example message:

```
Error: Line 111, The 'lbdb259_template' refers to a nonexistent or empty
 'lu_table_template'. (LBDB-259)
```

What Next

Check the library source file, and either add the lu_table_template group if it is missing or correct the template name if it is a typo.

LBDB-259w

(warning) The '%s' refers to a nonexistent or empty '%s'.

Description

This message indicates that you specified a nonexistent or empty template group on a propagation delay in a nonlinear delay library.

The following example shows an instance where this message occurs:

```
fall_propagation(lbdb259_template) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

To fix the problem, add the following group to the library file,

```
lu_table_template(lbdb259_template) {
        variable_1 : input_net_transition;
        variable_2 : output_net_length;
```

```
        index_1 ("0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

The following is an example message:

```
Warning: Line 111, The 'lbdb259_template' refers to a nonexistent or
 empty 'lu_table_template'. (LBDB-259w)
```

What Next

Check the library source file, and either add the lu_table_template group if it is missing or correct the template name if it is a typo.

LBDB-260

(error) The '%s' in '%s' and '%s' \n \tin '%s' of the '%s' lu_table_template represent \n \tthe same unallowable meaning.

Description

This message indicates that the two variables in the lu_table_template represent the same unallowable meaning. Library Compiler fails if both the values of variable_1 and variable_2 are from the following set:

```
* total_output_net_capacitance
        * output_net_length
        * output_net_wire_cap
        * output_net_pin_cap
```

The following example shows an instance where this message occurs:

```
lu_table_template(lbdb260) {
        variable_1 : output_net_length;
        variable_2 : total_output_net_capacitance;
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

The following is an example message:

```
Error: Line 57, The 'output_net_length' in variable_1 and
 'total_output_net_capacitance'
        in variable_2 of the 'lbdb260' lu_table_template represent
        the same unallowable meaning. (LBDB-260)
```

What Next

Check the lu_table_template, and make the correction to either variable_1 or variable_2.

Feedback

LBDB-261

(error) The %s has already been specified for '%s'%s. A duplicate is not allowed.

Description

This message indicates that attribute or group information is specified multiple times. Library Compiler does not allow duplicate information.

What Next

Check the library source file, and, if there is a duplicate, change either name of duplicated group or delete one group/attribute.

Examples

The following example shows an instance where this message occurs:

```
lu_table_template(lbdb261_template) {
        variable_1 : constrained_pin_transition;
        variable_2 : related_pin_transition;
        index_1 ("0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

Examples

```
Error: Line 43, The 'index_2' has already been specified for
 'lbdb261_template' at line 30. A duplicate is not allowed.(LBDB-261)
```

LBDB-261w

(warning) The %s has already been specified for '%s'%s. Using the last definition encountered.

Description

This message indicates that attribute or group information is specified multiple times. Library Compiler does not allow duplicate information and use last definition.

What Next

Check the library source file, and, if there is a duplicate, change either name of group/attribute or delete one group/attribute.

EXMAPLES

The following example shows two function definition are same

Feedback

```
pin(Q) {
             direction : output;
             function : "1";
             function : "1";
        }
```

Examples

```
Warning: Line 43, The  attribute 'function'  has already been specified
 for group 'pin' at line 58. Using the last definition encountered.
 (LBDB-261w)
```

LBDB-262

(error) The '%s' attribute has an invalid sequence of\n \tdata '%f , %f'. The values must be in\n \tmonotonically increasing order.

Description

This message indicates that the set of data is not specified in monotonically increasing order.

The following example shows an instance where this message occurs:

```
lu_table_template(one_dimension) {
        variable_1 : input_net_transition;
        variable_2 : output_net_length;
        index_1 ("0.1");
        /* index does not in monotically increasing order */
        index_2 ("0.1, 4.2, 2.3, 3.4");
  }
```

The following is an example message:

```
Error: Line 22, The 'index_2' attribute has an invalid sequence of
        data '4.200000 , 2.300000'. The values must be in
        monotonically increasing order. (LBDB-262)
```

What Next

Check your library and correct the order of the values. If the message shows identical values and the library file reveals tiny differences, you hit the resolution limit of single-precision floating-point numbers. Consider increasing the spacing between data points.

Feedback

If the error happens inside an output_current_rise or output_current_fall group, please refer to the latest version of "CCS Timing Library Characterization Guidelines" and try the following:

1. Reduce or set tstart = 0 (see Figure 4 in the Guidelines), and re-characterize the library.
2. If that does not work, further reduce the reference_time value. Subtract the same amount from all entries in index_3 (time) in the same vector group. Apply the same modifications to all vector groups having the same input_net_transition value (index_1 or index_2), within the same output_current_rise or output_current_fall group. Make sure no adjusted numbers become negative.

LBDB-262w

(warning) The '%s' attribute has an invalid sequence of\n \tdata '%f , %f'. The values must be in\n \tmonotonically increasing order.

Description

This message indicates that the set of data is not specified in monotonically increasing order.

The following example shows an instance where this message occurs:

```
lu_table_template(one_dimension) {
        variable_1 : input_net_transition;
        variable_2 : output_net_length;
        index_1 ("0.1");
        /* index does not in monotically increasing order */
        index_2 ("0.1, 4.2, 2.3, 3.4");
  }
```

The following is an example message:

```
Warning: Line 22, The 'index_2' attribute has an invalid sequence of
        data '4.200000 , 2.300000'. The values must be in
        monotonically increasing order. (LBDB-262w)
```

What Next

Check your library and correct the order of the values. If the message shows identical values and the library file reveals tiny differences, you hit the resolution limit of single-precision floating-point numbers. Consider increasing the spacing between data points.

Feedback

If the warning happens inside an output_current_rise or output_current_fall group, please refer to the latest version of "CCS Timing Library Characterization Guidelines" and try the following:

1. Reduce or set tstart = 0 (see Figure 4 in the Guidelines), and re-characterize the library.
2. If that does not work, further reduce the reference_time value. Subtract the same amount from all entries in index_3 (time) in the same vector group. Apply the same modifications to all vector groups having the same input_net_transition value (index_1 or index_2), within the same output_current_rise or output_current_fall group. Make sure no adjusted numbers become negative.

LBDB-263

(error) The '%s' attribute has a value '%f',\n which is less than '%f', the minimum required value of this attribute.

Description

The value specified is less than the required minimum value for this attribute.

The following example shows an instance where this message occurs:

```
lu_table_template(invalid_template) {
        variable_1 : constrained_pin_transition;
        variable_2 : output_net_length;
        /* index value can not be less than zero */
        index_1 ("-0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

The following is an example message:

```
Error: Line 35, The 'index_1' attribute has a value '-0.100000',
        which is less than '0.000000', the minimum required value
        of this attribute. (LBDB-263)
```

What Next

Check the library source file and correct the problem. Find the minimum value for this attribute in the error message or in the Library Compiler reference manual.

LBDB-264

(error) The '%s' is invalid in this look-up table.

Feedback

Description

This message indicates that the specified index is not allowed in the current table because the current table is one dimensional.

The following example shows an instance where this message occurs:

```
lu_table_template(lbdb264) {
        variable_1 : constrained_pin_transition;
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

To fix the problem, change index_2 to index_1.

The following is an example message:

```
Error: Line 46, The 'index_2' is invalid in this delay look-up table.
 (LBDB-264)
```

What Next

Check the library source file to determine whether you have the *variable_2* attribute specified before *index_2* or whether you are specifying *index_2* in a one-dimensional table or template.

LBDB-265

(error) You cannot mix a cell delay table with\n \ta propagation delay table in the same timing group.

Description

You can define cell delay table or propagation delay table within a timing group, but you cannot mix them together. For example, *cell_rise* and *propagation_fall* cannot be defined in a timing group. The same applies to *cell_fall* and *propagation_fall*.

The following example shows an instance where this message occurs:

```
cell (INVB) {
    area : 0.1;
    pin(Q) {
      direction : output;
      function :  "!A";
      timing() {
        related_pin : "A";
        rise_transition(fivebyfive) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          index_2("0.100,0.200,0.300,0.400,0.500");
          values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
```

Feedback

```
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
        }
        cell_rise(fivebyfive_prime) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          values("-0.100000, -0.200000, 0.300000, 0.400000, 0.500000");
        }
        rise_propagation(fivebyfive_prime) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          values("-0.100000, -0.200000, 0.300000, 0.400000, 0.500000");
        }
        fall_transition(fivebyfive) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          index_2("0.100,0.200,0.300,0.400,0.500");
          values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
        }
        cell_fall(fivebyfive) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          index_2("0.100,0.200,0.300,0.400,0.500");
          values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
            "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
        }
      }
      max_transition : 1.0;
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Error: Line 1110, You cannot mix a cell delay table with
        a propagation delay table in the same timing group. (LBDB-265)
```

What Next

Make your selection, and use either a cell delay table or a propagation delay table.

LBDB-266

(error) The '%s' attribute is needed in the specification.\n No default can be applied to this attribute.

Feedback

Description

This error message occurs when the identified attribute is missing in the specification.

What Next

Check your library, add the missing attribute, and run the command again.

For example, the *index_1* attribute is missing from the following specification:

```
lu_table_template(lbdb266_template) {
        variable_1 : constrained_pin_transition;
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

In the following example, since the *va_rise_constraint* is referring to a template that contains the *related_out_total_output_net_capacitance* related output loading variable, the *related_output_pin* attribute is required under the timing group.

```
lu_table_template(va_sup_hld_1) {
   variable_1 : related_out_total_output_net_capacitance;
   index_1("2.0, 3.0");
   variable_2 : constrained_pin_transition;
   index_2("3.0, 4.0");
 }
 ...
    timing () {
       timing_based_variation() {
         va_parameters(var1, var2);
         nominal_va_values(10.0, 20.0);
         va_rise_constraint(va_sup_hld_1) {
                        va_values(10.0, 19.0);
               ...
         }
   ...}
  ...}
 ...
```

LBDB-266w

(warning) The '%s' attribute is needed in the specification.\n No default can be applied to this attribute.

Description

This warning message occurs when the identified attribute is missing in the specification.

What Next

Check your library, add the missing attribute, and run the command again.

Feedback

For example, the *index_1* attribute is missing from the following specification:

```
lu_table_template(lbdb266_template) {
        variable_1 : constrained_pin_transition;
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

In the following example, since the *va_rise_constraint* is referring to a template that contains the *related_out_total_output_net_capacitance* related output loading variable, the *related_output_pin* attribute is required under the timing group.

```
lu_table_template(va_sup_hld_1) {
   variable_1 : related_out_total_output_net_capacitance;
   index_1("2.0, 3.0");
   variable_2 : constrained_pin_transition;
   index_2("3.0, 4.0");
 }
 ...
    timing () {
       timing_based_variation() {
         va_parameters(var1, var2);
         nominal_va_values(10.0, 20.0);
         va_rise_constraint(va_sup_hld_1) {
                        va_values(10.0, 19.0);
               ...
         }
   ...}
  ...}
 ...
```

LBDB-267

(error) The '%s' is missing for this timing arc.

Description

All four delay look-up tables

```
* rise_propagation/cell_rise
        * fall_propagation/cell_fall
        * rise_transition
        * fall_transition
```

are required in the timing arc if the *delay_model* is *table_lookup*. If the *timing_type* is 'clear', define both fall tables. Defining the rise tables is optional. If the *timing_type* is 'preset', define both rise tables. Defining the fall tables is optional.

The following example shows an instance where this message occurs:

```
pin ( Y )    {
      direction : output;
      function : " (A+B)' ";
```

Feedback

```
      timing ()      {
        related_pin : A ;
        rise_propagation(prop) {
          values("0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000");
        }
        rise_transition(tran) {
          values("0.000000, 0.10000");
        }
        fall_transition(tran) {
          values("0.000000, 0.100000");
        }
      }
    }
```

To fix the problem, add the attribute to the timing group,

```
fall_propagation(prop) {
          values("0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000");
        }
```

The following is an example message:

```
Error: Line 144, The 'fall_propagation' is missing for this timing arc.
 (LBDB-267)
```

What Next

Check the library source file to see if you missed the look-up table or put it in the wrong place.

LBDB-268

(error) The '%s' cannot be specified in a timing arc with\n \tthe '%s' timing_type.

Description

This message indicates that the timing arc with the indicated timing_type is not compatible with a *table_lookup* delay model.

The following example shows an instance where this message occurs:

```
rise_constraint(basic_template) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
```

```
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

The following is an example message:

```
Error: The 'rise_constraint' cannot be specified in a timing arc with
        the 'combinational' timing_type. (LBDB-268)
```

LBDB-269

(error) You have both '%s' and '%s'\n \tspecified in this timing group.

Description

You cannot specify both cell delay and propagation delay information in a timing group as indicated in the error message. For example, *cell_rise* and *propagation_fall* cannot be defined in a timing group. The same applies to *cell_fall* and *propagation_fall*.

You can use *intrinsic_rise* and *intrinsic_fall* to define default delay values when the delay model is a table_lookup.

The following example shows an instance where this message occurs:

```
cell (INVB) {
    area : 0.1;
    pin(Q) {
      direction : output;
      function :  "!A";
      timing() {
        related_pin : "A";
        rise_transition(fivebyfive) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          index_2("0.100,0.200,0.300,0.400,0.500");
          values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
        }
        cell_rise(fivebyfive_prime) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          values(\
                 "-0.100000, -0.200000, 0.300000, 0.400000, 0.500000");
        }
        rise_propagation(fivebyfive_prime) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          values(\
                 "-0.100000, -0.200000, 0.300000, 0.400000, 0.500000");
        }
        fall_transition(fivebyfive) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          index_2("0.100,0.200,0.300,0.400,0.500");
```

Feedback

```
          values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
        }
        cell_fall(fivebyfive) {
          index_1("0.000,0.200,0.400,0.600,0.800");
          index_2("0.100,0.200,0.300,0.400,0.500");
          values("0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000", \
                 "0.100000, 0.100000, 0.100000, 0.100000, 0.100000");
        }
      }
      max_transition : 1.0;
    }
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Error: Line 1110, You have both 'rise_propagation' and 'cell_rise'
        specified in this timing group. (LBDB-269)
```

What Next

Make your selection to use either a cell delay table or a propagation delay table.

LBDB-270

(error) The '%s' has a count of %d, which does not match\n \tthe size %d specified.

Description

The specification of the index implied the size of each axis of the look-up table. The syntax of *values* complex attribute should be organized in groups of floating-point values equal to the size of index_2. The total number of groups should be equal to the size of index_1. For a one-dimensional table, the size of index_2 is *1*.

The following example shows an instance where this message occurs:

```
lu_table_template(basic_template) {
        variable_1 : input_net_transition;
        variable_2 : output_net_length;
        index_1 ("0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

Feedback

```
rise_propagation(basic_template) {
      values ("1, 2, 3, 4", "5, 6, 7, 8", \
              "9, 10, 11", "13, 14, 15, 16");
}
```

The following is an example message:

```
Error: Line 160, The 'values' have a count of 3, which does not match
        the size 4 specified. (LBDB-270)
```

What Next

Check the library source file, and correct the problem by grouping the values together in the required format.

LBDB-271

(error) The '%s' has zero elements.

Description

This message indicates that one of the lu_table_template index complex attributes contains no value.

The following example shows an instance where this message occurs:

```
lu_table_template(missing_index) {
        variable_1 : output_net_length;
        index_1("");
  }
```

The following is an example message:

```
Error: Line 64, The 'index_1' has zero elements. (LBDB-271)
```

What Next

Check the library source file, and either add the missing value to the index attribute or delete the attribute if it is not used.

LBDB-272

(warning) The '%s' attribute has a '%f' value,\n \twhich is less than '%f' the minimum recommended value of this attribute.

Description

This message indicates that the value assigned for the specified attribute is lower than the recommended minimum value. However, Library Compiler will maintain the values as is.

Feedback

The following example shows an instance where this message occurs:

```
lu_table_template(basic_template) {
        variable_1 : input_net_transition;
        variable_2 : output_net_length;
        index_1 ("0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
  ...
        fall_transition(basic_template) {
                values ("-1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

The following is an example message:

```
Warning: Line 123, The 'values' attribute has a '-1.000000' value,
        which is less than '0.000000' the minimum recommended value of
        this attribute. (LBDB-272)
```

What Next

Check the library source file, and make sure the value is correct. Refer to the "Library Compiler Reference Manual" for the attribute value requirements.

LBDB-273

(error) The fanout_length complex attribute allows only 2\n \tor 5 arguments, and you specified %d arguments.

Description

This message indicates that the *fanout_length* complex attribute has an invalid number of arguments. The attribute can have either the two standard arguments,

```
* fanout
        * length
```

or five arguments created automatically from the back-annotation information,

```
* fanout
        * length
        * average capacitance
        * standard deviation
        * number of nets
```

The following example shows an instance where this message occurs:

```
wire_load("05x05") {
    resistance : 0 ;
    capacitance : 1 ;
    area : 0 ;
```

Feedback

```
    slope : 0.186 ;
    fanout_length(1,0.39, 0.1) ;
  }
```

The following is an example message:

```
Error: Line 43, The fanout_length complex attribute allows only 2
        or 5 arguments, and you specified 3 arguments. (LBDB-273)
```

What Next

Refer to the "Library Compiler User Guide" manual for more information about the fanout_length attribute. Check the library source file, and correct the format of the attribute.

LBDB-274

(warning) The '%s' attribute has a '%f' value,\n \twhich is less than '%f' the minimum required value of this attribute.\n \tThe value is changed to the minimum value.

Description

This message indicates that the value assigned for the specified attribute is lower than the required minimum value. Therefore, Library Compiler uses the minimum value for the attribute.

The following example shows an instance where this message occurs:

```
lu_table_template(basic_template) {
        variable_1 : output_pin_transition;
        variable_2 : connect_delay;
        index_1 ("0, 1");
        index_2 ("0, 1");
  }
  ...
        fall_transition_degradation(basic_template) {
                values ("-1, 2", "5, 8");
        }
```

The following is an example message:

```
Warning: Line 123, The 'values' attribute has a '-1.000000' value,
        which is less than '0.000000' the minimum required value of
        this attribute. The value is changed to the minimum value.
 (LBDB-274)
```

What Next

Check the library source file, and correct the value if the minimum value is not acceptable. Refer to the "Library Compiler Reference Manual" for the attribute value requirements.

Feedback

LBDB-275

(warning) The '%s' attribute has size 1, which is not \n \tused for any purpose with its associated variable.

Description

This message indicates that the size of one of the *lu_table_template* attributes has size 1. Library Compiler expects the size of each dimension to be larger than *1*.

The following example shows an instance where this message occurs:

```
lu_table_template(lbdb275) {
        variable_1 : input_net_transition;
        variable_2 : output_net_length;
        index_1 ("0.1");
        index_2 ("0.1, 0.2, 0.3, 0.4");
  }
```

The following is an example message:

```
Warning: Line 20, The 'index_1' attribute has size 1, which is not
        used for any purpose with its associated variable. (LBDB-275)
```

What Next

Check the library source file, and delete this dimension if it is not needed.

LBDB-276

(error) The '%s' refers to an invalid '%s'.

Description

This message indicates that the specified name refers to an invalid *lu_table_template* group. First, Library Compiler issues all the errors that make the group invalid and issues this message when the template is used.

The following example shows an instance where this message occurs:

```
lu_table_template(lbdb276_template) {
        variable_1 : constrained_pin_transition;
        variable_2 : output_net_length;
        index_1 ("-0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }

          rise_transition(invalid_template) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12");
          }
```

Feedback

```
In this case, the index_1 value is less than zero, so the look-up
table becomes invalid. The rise_transition timing information refers
to an invalid table.
```

The following is an example message:

```
Error: Line 165, The 'lbdb276_template' refers to an invalid
 'lu_table_template'. (LBDB-276)
```

What Next

Check the library source file, and correct the errors in the look-up table template to which this table refers.

LBDB-278

(error) The 'timing' group with '%s' timing_type \n \tneeds at least one look-up table.

Description

This message indicates that in a nonlinear delay library, you did not specify a look-up table (rise_constraint or fall_constraint) for timing checks in a timing group. To be complete, Library Compiler expects at least one look-up table for the timing check groups.

The following example shows an instance where this message occurs:

```
pin ( D )    {
      direction : input;
      capacitance : 1;
      timing ()      {
        related_pin : CK ;
        timing_type : setup_rising ;
      }
  }
```

To fix the problem, define the template group and the rise_constraint group to the timing group,

```
lu_table_template(constraint) {
    variable_1 : constrained_pin_transition;
    index_1("0, 1, 2, 3, 4");
    variable_2 : related_pin_transition;
    index_2("0, 1, 2, 3, 4");
  }
  pin ( D )    {
      direction : input;
      capacitance : 1;
      timing () {
        related_pin : CK ;
        timing_type : setup_rising ;
        rise_constraint(constraint) {
```

Feedback

```
          values("1.0000, 1.0000, 1.0000, 1.0000, 1.0000",  \
                 "1.0000, 1.0000, 1.0000, 1.0000, 1.0000",  \
                 "1.0000, 1.0000, 1.0000, 1.0000, 1.0000",  \
                 "1.0000, 1.0000, 1.0000, 1.0000, 1.0000",  \
                 "1.0000, 1.0000, 1.0000, 1.0000, 1.0000");
        }
      }
  }
```

The following is an example message:

```
Error: Line 63, The 'timing' group with 'setup_rising' timing_type
        needs at least one look-up table. (LBDB-278)
```

What Next

Check the library source file, and correct the timing group. Add either a rise_constraint or fall_constraint table to the group.

LBDB-279

(error) The 'timing' group with '%s' timing_type \n \tneeds one look-up table.

Description

This message indicates that you specified more than one table for the specified timing group. This group needs only one table, either *constraint_rise* or *constraint_fall*.

The following example shows an instance where this message occurs:

```
pin(cd) {
      direction : input;
      capacitance : 0.065
      timing() {
        related_pin : "cp";
        timing_type : recovery_rising;
        rise_constraint(constraint_template) {
          values("1, 2", "3, 4");
        }
        fall_constraint(scalar) {
          values("1");
        }
      }
    }
```

In this case, the 'cd' pin has both the rise_constraint and fall_constraint attribute. To fix the problem, delete the fall_constraint table.

The following is an example message:

```
Error: Line 61, The 'timing' group with 'recovery_rising' timing_type
        needs one look-up table. (LBDB-279)
```

Feedback

What Next

Check the library source file, and correct the timing group. Delete from the group either the *constraint_rise* table or the *constraint_fall* table.

LBDB-280

(error) The '%s' look-up table cannot use\n \t'%s' as its template. The look-up table is not\n \tcompatible with the template.

Description

This message indicates that the specified look-up table is not compatible with the specified template. Variable types described in a look-up table template must be compatible with the usage of that template. For example, a template references variable types used for constraint checking ('related_pin_transition' and 'constrained_pin_transition') cannot be referenced in a cell delay description ('cell_rise' or 'cell_fall').

The following example shows an instance where this message occurs:

```
lu_table_template(basic_template) {
    variable_1 : input_net_transition;
    index_1("0, 1, 2, 3, 4");
    variable_2 : output_net_length;
    index_2("0, 1, 2");
  }
  lu_table_template(constraint) {
    variable_1 : constrained_pin_transition;
    index_1("0, 1, 2, 3, 4");
    variable_2 : related_pin_transition;
    index_2("0, 1, 2, 3, 4");
  }

        rise_constraint(basic_template) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

To fix the problem, change the template value of the rise_constraint group from basic_template to constraint.

The following is an example message:

```
Error: Line 126, The 'rise_constraint' look-up table cannot use
        'basic_template' as its template. The look-up table is not
        compatible with the template. (LBDB-280)
```

Feedback

What Next

Refer to the "Library Compiler User Guide" for more information about look-up tables. Change the library source file by referencing a different template in the look-up table description.

LBDB-281

(error) The '%s' template has variables which\n \tshould not be used together.

Description

This message indicates that you specified two incompatible variables in the same template.

The following example shows an instance where this message occurs:

```
lu_table_template(invalid_template) {
        variable_1 : constrained_pin_transition;
        variable_2 : output_net_length;
        index_1 ("0.1, 0.2, 0.3, 0.4");
        index_2 ("0.1, 0.2, 0.3, 0.4");
  }
```

The following is an example message:

```
Error: Line 32, The 'invalid_template' template has variables which
        should not be used together. (LBDB-281)
```

What Next

Refer to the "Library Compiler User Guide" for more information on defining CMOS nonlinear timing model templates. Check the library source file to see if you made a mistake when you entered the variables strings.

LBDB-282

(error) The '%s' attribute has a '%f' value\n \tthat is larger than the maximum allowed value of '%f'.

Description

This message indicates that for the specified attribute, you defined a value that is larger than the maximum allowed value. The error message includes the maximum value for this attribute.

The following example shows an instance where this message occurs:

```
default_min_porosity : 91.0;
```

Feedback

The following is an example message:

```
Error: Line 53, The 'default_min_porosity' attribute has a '91.000000'
 value
        that is larger than the maximum allowed value of '90.000000'.
 (LBDB-282)
```

What Next

Refer to the "Library Compiler User Guide" for the maximum value required for the attribute, and correct the value in the library source file.

LBDB-283

(error) The '%s' layer name is invalid.

Description

This message indicates that you specified an invalid name for the current attribute or function. The name should match a name previously defined in the resource group.

If the value is in the related_layer attribute and the layer is not valid. It may be because it is not one of the neighboring contact layer.

The following example shows an instance where this message occurs:

```
same_net_min_spacing(dummy, metal1, 0.1, TRUE);
```

The following is an example message:

```
Error: Line 104, The 'dummy' layer name is invalid.  (LBDB-283)
```

What Next

Check your library to see if you have an error in either previous layer definition or the current attribute / function.

LBDB-284

(error) Missing 'routing_layers' attribute for this library\n \twhich is needed for specifying 'routing_track'.

Description

This message indicates that you specified a *routing_track* group without specifying the *routing_layers* attribute. Library Compiler expects the *routing_layers* complex attribute to be defined before you can specify the *routing_track* group. The *routing_track* group has a name to refer to a specific routing layer in the *routing_layers* complex attribute.

Feedback

The following example shows an instance where this message occurs:

```
routing_track(metal2) {
        tracks : 2;
        total_track_area : 0.2;
   }
```

To fix the problem, add the attribute to the library,

```
routing_layers(metal1,metal2);
```

The following is an example message:

```
Error: Line 65, Missing 'routing_layers' attribute for this library,
        which is needed for specifying 'routing_track'. (LBDB-284)
```

What Next

Check the library source file to see if you are missing the *routing_layers* attribute, which should be placed in the library before the *routing_track* group can be identified.

LBDB-285

(error) In this 'routing_track' group, 'tracks' is 0 and\n \t'total_track_area' is %f, which is inconsistent.

Description

This message indicates that for a *routing_track* group, you specified the *total_track_area* attribute without specifying the *tracks* attribute. If you do not have tracks in a routing layer, you cannot have *total_track_area* for that layer either.

The following example shows an instance where this message occurs:

```
routing_layers(metal1,metal2);

   routing_track(metal2) {
        /* missing tracks */
        total_track_area : 1.5;
   }
```

To fix the problem, add the tracks attribute to the routing_track group,

```
tracks : 1;
```

The following is an example message:

```
Error: Line 266, In this 'routing_track' group, 'tracks' is 0 and
        'total_track_area' is 1.500000, which is inconsistent. (LBDB-285)
```

Feedback

What Next

Check your library to see if it is missing the *tracks* attribute in this group. Do not have the *total_track_area* other than '0', or this group is not needed.

LBDB-286

(error) No 'routing_track' information in the '%s' library.

Description

This message indicates that, in the library, you specified the *default_min_porosity* attribute without specifying the *routing_track* group in any of the cells.

The following is an example message:

```
Error: Line 1, No 'routing_track' information in the 'lbdb286' library.
 (LBDB-286)
```

What Next

Remove the *default_min_porosity* attribute or add *routing_track* information into the library.

LBDB-287

(warning) No routability information in the '%s' %s.

Description

This message indicates that one of the two cases occurred:

```
* You have the routing_layers attribute in a library and
          do not have routing_track group in the cell.
        * You have the default_min_porosity attribute in a
          library and do not have the routing_track information
          in a cell.
```

The following example shows an instance where this message occurs:

```
default_min_porosity : 0.0;
    routing_layers(metal1,metal2);

cell(AN2) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
```

```
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "A";
    }
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "B";
    }
  }
}
```

In this case, The library has the *default_min_porosity* attribute, but the 'AN2' cell has no *routing_track* information.

The following is an example message:

```
Warning: Line 63, No routability information in the 'AN2' cell.
 (LBDB-287)
```

What Next

Check the library source file to remove the *routing_layers* attribute if the warning fits the first case. For the second case, check the cell to make sure it does not have any *routing_track* information on all routing layers (all of them are completely obstructed in this cell) when you have the *default_min_porosity* attribute.

LBDB-288

(error) The '%f' 'total_track_area' value is larger than\n \tthe '%f' cell area value.

Description

This message indicates that you specified a larger value for the *total_track_area* than the *cell area* value. The *total_track_area* value of a particular routing layer cannot be larger than the *cell area* value.

The following example shows an instance where this message occurs:

```
cell(IVP) {
  area : 1;
   routing_track(metal2) {
```

Feedback

```
        tracks : 1;
        total_track_area : 1.5;
    }
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
```

The following is an example message:

```
Error: Line 242, The 1.500000 'total_track_area' value is larger than
        the '1.000000' cell area value. (LBDB-288)
```

What Next

Check to see if you have entered the wrong information for either of these two attributes.

LBDB-289

(error) '%s' has been used more than one time in the\n \tspecification.

Description

This message indicates that you specified the same routing layer name more than once in the routing_layers attribute. Library Compiler expects unique names.

The following example shows an instance where this message occurs:

```
routing_layers(metal2,metal2);
```

The following is an example message:

```
Error: Line 55, 'metal2' has been used more than one time in the
        specification. (LBDB-289)
```

What Next

Check to see if you entered the wrong information for this attribute.

Feedback

LBDB-290

(error) '%s' should have at least one entry in it.

Description

This message indicates that you specified an attribute without any entries. This complex attribute must contain at least one entry.

The following example shows an instance where this message occurs:

```
routing_layers();
```

The following is an example message:

```
Error: Line 18, 'routing_layers' should have at least one entry in it.
 (LBDB-290)
```

What Next

Check to see if you have entered the required information for this complex attribute.

LBDB-291

(warning) No routability information for the '%s' layer.\n \tIt is assumed to be completely obstructed.

Description

The *routing_track* group of the indicated layer is not in the cell. It is assumed to be completely obstructed.

The following example shows an instance where this message occurs:

```
library(small_cmos1) {
    default_min_porosity : 0.0;
    routing_layers(metal1,metal2);

    cell(AN2) {
       area : 2;
       routing_track(metal2) {
         tracks : 2;
         total_track_area : 0.2;
       }
       pin(A) {
         direction : input;
         capacitance : 1;
       }
       pin(B) {
         direction : input;
         capacitance : 1;
```

```
        }
        pin(Z) {
          direction : output;
          function : "A B";
          timing() {
             intrinsic_rise : 0.1;
             intrinsic_fall : 0.1;
             rise_resistance : 0.1;
             fall_resistance : 0.1;
             related_pin : "A";
          }
          timing() {
             intrinsic_rise : 0.1;
             intrinsic_fall : 0.1;
             rise_resistance : 0.1;
             fall_resistance : 0.1;
             related_pin : "B";
          }
        }
    }
}
```

In this case, 'metal1' is not used in any routing_track group.

The following is an example message:

```
Warning: Line 240, No routability information for the 'metal1' layer.
        It is assumed to be completely obstructed. (LBDB-291)
```

What Next

If the previous statement is not true, enter the *routing_track* information for the indicated layer. Otherwise, it is all right.

LBDB-292

(error) The '%s' should be the %d%s attribute in the library.

Description

This message indicates that you specified the technology and delay_model in unacceptable order. For the Library Compiler to work correctly, the defined attribute must appear in this library at the indicated place in the error message.

The following example shows an instance where this message occurs:

```
library(lib) {
  technology : "cmos";
  delay_model : "generic_cmos";
}
```

Feedback

In this case, the delay_model attribute comes after the technology attribute. To fix the problem, switch the order of definition of the two attributes.

The following is an example message:

```
Error: Line 5, The 'delay_model' should be the 1st attribute in the
 library. (LBDB-292)
```

What Next

Modify the library source file to move the defined attribute to the correct place, as indicated in the error message.

LBDB-292w

(warning) The '%s' should be the %d%s attribute in the library.

Description

This message indicates that you specified the technology and delay_model in unacceptable order. For the Library Compiler to work correctly, the defined attribute must appear in this library at the indicated place in the warning message.

The following example shows an instance where this message occurs:

```
library(lib) {
  technology : "cmos";
  delay_model : "generic_cmos";
}
```

In this case, the delay_model attribute comes after the technology attribute. To fix the problem, switch the order of definition of the two attributes.

The following is an example message:

```
Warning: Line 5, The 'delay_model' should be the 1st attribute in the
 library. (LBDB-292w)
```

What Next

Modify the library source file to move the defined attribute to the correct place, as indicated in the warning message.

LBDB-293

(error) In this 'routing_track' group, the 'tracks' value\n \tis %d and the 'total_track_area' value is '0.0'. This is\n \tinconsistent.

Feedback

Description

This message indicates that you specified the *tracks* attribute without specifying the *total_track_area* attribute in a *routing_track* group. If you have tracks in a routing layer, you need to have the *total_track_area* for that layer too.

The following example shows an instance where this message occurs:

```
routing_track(metal2) {
        tracks : 2;
        /* missing total_track_area */
   }
```

The following is an example message:

```
Error: Line 205, In this 'routing_track' group, the 'tracks' value
        is 2 and the 'total_track_area' value is '0.0'. This is
        inconsistent. (LBDB-293)
```

What Next

Check the library source file to see if it is missing the *total_track_area* attribute in this group, and add it. Otherwise, set the *tracks* value to 0 or remove the routing_track group.

LBDB-294

(warning) The UP or DOWN X pin coordinate does not lay on a grid.

Description

This warning message appears when the library symbol has a pin that is not on a grid and is off by 0.01.

The following example shows an instance where this message occurs:

```
library(lbdb294) {
 SCALE = 1.0 / 8.0;

  symbol("gndsym") {
    set_minimum_boundary(0 * SCALE, 0 * SCALE, 40 * SCALE, 40 * SCALE);
    line(5 * SCALE, 10 * SCALE, 35 * SCALE, 10 * SCALE);
    line(0 * SCALE, 20 * SCALE, 40 * SCALE, 20 * SCALE);
    line(15 * SCALE, 2 * SCALE, 25 * SCALE, 2 * SCALE);
    line(20 * SCALE, 20 * SCALE, 20 * SCALE, 40 * SCALE);
    pin("gnd", 20 * SCALE, 40 * SCALE, ANY_ROTATION);
  }
}
```

In this case, the "gnd" pin has the Y coordinate off the grid.

Feedback

The following is an example message:

```
Warning: Line 24, The UP or DOWN X pin coordinate does not lay on a grid.
 (LBDB-294)
```

What Next

Check the symbol library file, and correct the X coordinate.

LBDB-295

(warning) The LEFT or RIGHT Y pin coordinate does not lay on a grid.

Description

This warning message appears when the library symbol has a pin that is not on a grid and is off by 0.01.

The following example shows an instance where this message occurs:

```
library(lbdb295) {
 SCALE = 1.0 / 8.0;

  symbol("gnd") {
    set_minimum_boundary(0 * SCALE, 0 * SCALE, 40 * SCALE, 40 * SCALE);
    line(5 * SCALE, 10 * SCALE, 35 * SCALE, 10 * SCALE);
    line(0 * SCALE, 20 * SCALE, 40 * SCALE, 20 * SCALE);
    line(15 * SCALE, 2 * SCALE, 25 * SCALE, 2 * SCALE);
    line(20 * SCALE, 20 * SCALE, 20 * SCALE, 40 * SCALE);
    pin("Z", 128 * SCALE, 4 * SCALE, ANY_ROTATION);
    pin("gnd", 20 * SCALE, 40 * SCALE, ANY_ROTATION);
  }
}
```

In this case, the "Z" pin has the Y coordinate off the grid.

The following is an example message:

```
Warning: Line 24, The LEFT or RIGHT Y pin coordinate does not lay on a
 grid. (LBDB-295)
```

What Next

Check the symbol library file, and correct the Y coordinate.

LBDB-296

(warning) The '%s' pin of the '%s' auxiliary pad cell\n \tshould not have a function attribute.

Feedback

Description

This message indicates that you specified a function attribute on a auxiliary pad cell.

Cells with a 'auxiliary_pad_cell' attribute are used together with other cells with a 'pad_cell' attribute to build a logical pad. They can also provide the pull-up, pull-down, buffer, or inverter functionality. They should not have real 'logic'. Design Compiler will not work correctly if you decompose your pad cell this way.

The following example shows an instance where this message occurs:

```
cell(lbdb296) {
      auxiliary_pad_cell : true;
      area : 1;
      general_drivers : 0;
      input_drivers : 8;
      pin(A) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A'";
        timing() {
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "A";
        }
      }
    }
```

The following is an example message:

```
Warning: Line 64, The 'Z' pin of the 'lbdb296' auxiliary pad cell
        should not have a function attribute. (LBDB-296)
```

What Next

Check the technology source library. Either

```
1. remove the 'function' attribute from the cell under the
      following conditions:
        * If the cell is a buffer, no action is required.
        * If the cell is an inverter, invert the functionality of your
          'pad_cell', which is to be connected to this cell to form a
          pad cell, accordingly.
or
   2. remove the 'auxiliary_pad_cell' attribute, and model this cell
      as a regular cell but with the right 'connection_class' on the
      pin so it can be connected to the 'pad_cell' to form a pad as
      intended.
```

Feedback

LBDB-297

(error) The '%s' pin is reserved and should not be used as a pin name.

Description

Library Compiler uses several keywords internally for a sequential cell. The keywords are

```
* next_state
        * clocked_on
        * clocked_on_also
        * data_in
        * enable
        * enable_also
        * preset
        * clear
        * force_00
        * force_01
        * force_10
        * force_11
        * the variable1 and variable2 used in ff/latch/ff_bank/latch_bank

The following example shows an instance where this message occurs:
  pin(preset) {
    direction : input;
    capacitance : 1;
  }
```

The following is an example message:

```
Error: Line 182, The 'preset' pin is reserved and should not be used as a
 pin name. (LBDB-297)
```

What Next

Modify your library to change the name of the pin.

LBDB-298

(error) The '%s' attribute has a value %d, which is\n \tless than the minimum required value of this attribute %d.

Description

This message indicates that the value specified is less than the required minimum value for this attribute.

Feedback

The following example shows an instance where this message occurs:

```
wire_load_table("40x40") {
      fanout_area(-11, 0.1);
   }
```

The following is an example message:

```
Error: Line 84, The 'fanout_area' attribute has a value -11, which is
        less than the minimum required value of this attribute 1.
 (LBDB-298)
```

What Next

Check the library source file, and correct the value of the attribute. If the minimum value for this attribute is not displayed in the error message, refer to the *Library Compiler User Guide Manual* for minimum attribute values.

LBDB-299

(error) The library is missing 'operating_conditions' groups and 'default_operating_conditions' attribute.

Description

This error message occurs when the *default_operating_conditions* is undefined and there is no operating_conditions groups defined.

What Next

If you do not want Library Compiler to create the default operating_conditions for you, please check your library to define the relative operating_condition group and set it as the default_operating_conditions with the library-level attribute "default_operating_conditions".

LBDB-300

(error) The '%s' related_outputs for the internal_power group has\n \tbeen specified. A duplicate is not allowed.

Description

This message indicates that you include the same output pin in more than one internal_power group.

The following example shows an instance where this message occurs:

```
internal_power(test_input) {
    values("0.1, 1.2, 2.3, 3.4");
    related_outputs : "Z";
   }
```

```
   internal_power(test_input) {
    values("0.1, 1.2, 2.3, 3.4");
    related_outputs : "Z";
   }
```

The following is an example message:

```
Error: Line 41, The 'Z' related_outputs for the internal_power group has
        been specified. A duplicate is not allowed. (LBDB-300)
```

What Next

Check the library source file, and delete the duplicate information from one of the internal_power groups.

LBDB-301

(information) No internal_power information for the '%s' cell.

Description

This message indicates that you did not define an internal_power group for the specified cell. Library Compiler expects at least one internal_power group so the internal power of the cell can be calculated.

The following example shows an instance where this message occurs:

```
cell(lbdb301) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
}
```

Feedback

In this case, the 'lbdb301' cell is missing the internal_power group. To fix the problem, add this statement:

```
internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \
            " 1.000000 ,  5.000000 ,  0.000000 ", \
            " 0.000000 ,  0.000000 ,  0.000000 ");
     related_outputs : "Z";
     related_inputs : "A B";
  }
```

The following is an example message:

```
Information: Line 191, No internal_power information for the 'lbdb301'
 cell. (LBDB-301)
```

What Next

If you want to include the internal power of this cell in your design, add the required information into the library.

LBDB-302

(error) The '%s' specified in the '%s' is an\n \t%s pin.

Description

This message indicates that you specified either an input pin in a *related_outputs* attribute or an output pin in a *related_inputs* attribute.

The following example shows an instance where this message occurs:

```
cell(lbdb302) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
```

```
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
  internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \
            " 1.000000 ,  5.000000 ,  0.000000 ", \
            " 0.000000 ,  0.000000 ,  0.000000 ");
     /* bad related port */
     related_outputs : "A";
     related_inputs : "Z B";
  }
}
```

In this case, both the related_outputs and the related_inputs attributes have a wrong pin name. To fix the problem, change the name from 'A' to 'Z' in the related_outputs attribute and 'Z' to 'A' in the related_inputs attribute.

The following is an example message:

```
Error: Line 272, The 'A' specified in the 'related_outputs' is an
        input pin. (LBDB-302)
Error: Line 273, The 'Z' specified in the 'related_inputs' is an
        output pin. (LBDB-302)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-303

(error) You cannot specify more than one input pin or one bit\n \tof a bus or bundle input pin in the 'related_input'.

Description

This message indicates that you specified more than one input pin or one bit of an input pin, in the case of bus and bundle groups, in the *related_input* attribute. Library Compiler allows only one input pin or one bit of a bus or bundle in the attribute.

The following example shows an instance where this message occurs:

```
cell(lbdb303) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
```

Feedback

```
  }
  pin(Z) {
    direction : output;
    function : "A+B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
  internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \
            " 1.000000 ,  5.000000 ,  0.000000 ", \
            " 0.000000 ,  0.000000 ,  0.000000 ");
     related_outputs : "Z";
     /* more than one related input */
     related_input : "A B";
  }
}
```

In this case, the related_input attribute has two 'A' and 'B' input pins.

The following is an example message:

```
Error: Line 315, You cannot specify more than one input pin or one bit
        of a bus or a bundle input pin in the 'related_input'. (LBDB-303)
```

What Next

Check the "Library Compiler User Guide" for more information on power analysis, and correct the problem. Make sure that the related_input attribute has only one input pin or one bit of an bus or bundle input pin and the related_inputs attribute has more than one pin.

LBDB-304

(error) You can specify '%s'\n but not both, because they are mutually exclusive.

Description

This message indicates that you specified a *related_input* attribute with a *related_outputs* attribute in an internal_power group. Library Compiler allows either a *related_input* attribute or the pair *related_outputs*, *related_inputs* attributes, but not both, since the

Feedback

information provided is mutually exclusive. Library Compiler supports the related_input, related_inputs, and the related_outputs attributes in the table as follows:

```
* A one dimensional table uses only related_outputs.
        * A one dimensional table uses only related_input.
        * A one dimensional table uses both related_inputs and
          related_outputs.
        * A two dimensional table uses both related_inputs and
          related_outputs.
```

The following example shows an instance where this message occurs:

```
cell(lbdb304) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A+B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
  internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \
            " 1.000000 ,  5.000000 ,  0.000000 ", \
            " 0.000000 ,  0.000000 ,  0.000000 ");
     related_outputs : "Z";
     related_input : "A B";
  }
}
```

In this case, there is a typo. To fix the problem, add the character s to the related_input attribute name.

The following is an example message:

```
Error: Line 309, You can specify 'related_outputs/related_inputs or
 related_input'
        but not both, because they are mutually exclusive. (LBDB-304)
```

Feedback

What Next

Check the library and correct the related_inputs attribute if it is a typo or delete the unnecessary information from the library.

LBDB-305

(error) In the context, the '%s' valid value of the\n \t'%s' template is '%s'.\n \tYou specified '%s'.

Description

This message indicates that you specified an invalid value for the variable_1 in the power_lut_template given the specified information in the internal_power group. Library Compiler expects

```
* A related_input attribute in an internal_power group for a
          input_transition_time value in variable_1 of the corresponding
          power_lut_template
        * A related_outputs attribute in an internal_power group for a
          total_output_net_capacitance value in variable_1 of the
          corresponding power_lut_template
```

The following example shows an instance where this message occurs:

```
power_lut_template(lbdb305_input) {
    variable_1 : input_transition_time;
    index_1 ("1.0, 2.0");
  }

cell(lbdb305) {
  internal_power(lbdb305_input) {
    index_1("1.0, 2.0");
    values("1.0, 2.0");
    related_outputs : "Z";
  }
}
```

The following is an example message:

```
Error: Line 27, In the context, the 'variable_1' valid value of the
        'lbdb305_input' template is 'total_output_net_capacitance'.
        You specified 'input_transition_time'. (LBDB-305)
```

What Next

Refer to the "Library Compiler Reference Manual Volume 1" for more information on power modeling and analysis. Correct the attribute's value or its reference in the library.

Feedback

LBDB-306

(warning) The '%s' preferred input voltage does not exist in this library.

Description

This message indicates that you specified a input_voltage name to the *preferred_input_pad_voltage* attribute that is not described in the library or is defined after this attribute.

The following example shows an instance where this message occurs:

```
preferred_input_pad_voltage : "lbdb306";
  input_voltage(lbdb306) {
    vil : 1.5;
    vih : 3.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }
```

in this case, the 'lbdb306' input_voltage is defined after the preferred_input_pad_voltage attribute.

The following is an example message:

```
Warning: Line 25, The 'lbdb306' preferred input voltage does not exist in
 this library. (LBDB-306)
```

What Next

Check the preferred input pad voltage to be sure it is correct. If the input_voltage exists, make sure that the attribute is defined before the preferred_input_pad_voltage attribute. Otherwise, add the preferred input pad voltage to the library description.

LBDB-307

(warning) The '%s' preferred output voltage does not exist in this library.

Description

This message indicates that you specified an output_voltage name to the *preferred_output_pad_voltage* attribute that is not described in the library or is defined after this attribute.

The following example shows an instance where this message occurs:

```
preferred_output_pad_voltage : "lbdb307" ;
  output_voltage(lbdb307) {
    vol : 1.5;
    voh : 3.5;
    vomin : -0.3;
```

Feedback

```
    vomax : VDD + 0.3;
  }
```

in this case, the 'lbdb307' output_voltage is defined after the preferred_output_pad_voltage attribute.

The following is an example message:

```
Warning: Line 24, The 'lbdb307' preferred output voltage does not exist
 in this library. (LBDB-307)
```

What Next

Check the preferred output pad voltage to be sure it is correct. If the output_voltage exists, make sure that the attribute is defined before the preferred_output_pad_voltage attribute. Otherwise, add the preferred output pad voltge to the library description.

LBDB-308

(warning) Incomplete set of pads to support the '%s'\n \tpreferred output pad slew rate control.

Description

This message indicates that in the library you specified the *preferred_output_pad_slew_rate_control* attribute but you did not define a complete set of pads to support it. Library Compiler expects at least one of the following set of pad cells in the library with the given slew rate control value:

```
* One output pad
        * One bidirectional pad
        * One three state pad
```

The following example shows an instance where this message occurs:

```
library (lbdb308) {
  preferred_output_pad_slew_rate_control : high;
  output_voltage(GENERAL) {
    vol          : 0.33 ;
    voh          : 3.7 ;
    vomin        : -0.3 ;
    vomax        : VDD + 0.3 ;
  }
  cell(OUTBUF) {
    area : 0.000000;
    dont_touch : false;
    dont_use   : false;
    pad_cell : true;
    pin(D ) {
      direction   : input;
      capacitance : 1.0;
```

Feedback

```
    }
    pin(PAD ) {
      is_pad : true;
      output_voltage : GENERAL;
      drive_current : 4.0;
      slew_control : high;
      direction   : output;
      function    : "D";
      timing() {
        intrinsic_fall  : 1.0;
        intrinsic_rise  : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin  :"D";
      }
    }
  }
  cell(BBHS) {
    area : 0.000000;
    dont_touch : false;
    dont_use   : false;
    pad_cell : true;
    pin(E D ) {
      direction   : input;
      capacitance : 1.0;
    }
    pin(Y ) {
      direction   : output;
      timing() {
        intrinsic_fall  : 1.0;
        intrinsic_rise  : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin  :"PAD ";
      }
    }
    pin(PAD ) {
      is_pad : true;
      input_voltage : CMOS;
      output_voltage : GENERAL;
      drive_current : 4.0;
      slew_control : high;
      direction   : inout;
      function    : "D";
      three_state : "E'";
      timing() {
        intrinsic_fall  : 1.0;
        intrinsic_rise  : 1.0;
        fall_resistance : 0.1;
        rise_resistance : 0.1;
        related_pin  :"E D";
      }
    }
```

```
  }
}
```

In this case, the 'lbdb308' library has an output pad cell and a bidirectional pad cell, but it is missing a three_state pad cell.

The following is an example message:

```
Warning: Line 2, Incomplete set of pads to support the 'high'
        preferred output pad slew rate control. (LBDB-308)
```

What Next

Check the preferred output pad slew rate control to be sure it is correct, and add pads to the library containing the preferred output pad slew rate control value.

LBDB-309

(warning) In the '%s' gate, cannot degenerate the \n \t'%s' output due to excessive function size.

Description

This message appears when the Library Compiler has determined that degenerating the given output is potentially too difficult. This determination is based on an evaluation of the function complexity at this output port.

What Next

Either remove the *fpga_complex_degenerate* attribute from the library cell in question, or set the *fpga_degenerate_output* attribute to FALSE on this particular output. In either case, these actions delete the warning; they do not cause the degeneration software to attempt to degenerate the gate.

LBDB-310

(information) Degenerating %d-input gates from '%s' component\n \tof the '%s' output.

Description

This message indicates that the Library Compiler is starting to create degenerate functions based on the component named.

The following example shows an instance where this message occurs:

```
cell(lbdb310) {
    area : 1.0;
    fpga_complex_degenerate : true ;
    pin(D0 D1 D2 D3 S00 S01 S10 S11) {
      direction   : input;
```

```
      capacitance : 1.0;
    }
    pin(Y) {
      direction : output;
      function :
 "(D0!(S00&S01)+D1(S00&S01))!(S10+S11)+(D2!(S00&S01)+D3(S00&S01))(S10+S11
)";
      timing() {
        rise_resistance : 0.5;
        fall_resistance : 0.5;
        related_pin  :  "D0 D1 D2 D3 S00 S01 S10 S11" ;
      }
    }
  }
```

The following is an example message:

```
Information: Degenerating 2-input gates from the 'lbdb310' component
        of the 'Y' output. (LBDB-310)
```

What Next

No action is required.

LBDB-311

(information) Degenerated %d %d-input gates from the '%s' component.\n \tA total of %d components have been degenerated from the '%s' output.

Description

This message indicates that the Library Compiler has finished creating n-input degenerate functions based on the component and output named. The message tells you how the library size is growing and how long the degeneration process is taking.

The following example shows an instance where this message occurs:

```
cell(lbdb311) {
    area : 1.0;
    fpga_complex_degenerate : true ;
    pin(D0 D1 D2 D3 S00 S01 S10 S11) {
      direction   : input;
      capacitance : 1.0;
    }
    pin(Y) {
      direction   : output;
      function :
 "(D0!(S00&S01)+D1(S00&S01))!(S10+S11)+(D2!(S00&S01)+D3(S00&S01))(S10+S11
)";
      timing() {
        rise_resistance : 0.5;
        fall_resistance : 0.5;
```

Feedback

```
        related_pin  :  "D0 D1 D2 D3 S00 S01 S10 S11" ;
      }
    }
  }
```

The following is an example message:

```
Information: Degenerated 2 1-input gates from the 'lbdb311' component.
        A total of 2 components have been degenerated from the 'Y'
 output. (LBDB-311)
```

What Next

No action is required.

LBDB-312

(warning) Unable to do fpga complex degeneration on the '%s' gate because it %s.

Description

This message occurs when you have defined *fpga_complex_degenerate* on a component for which this feature is not currently supported. Library Compiler issues this message for the following cells:

```
* Sequential devices: latches and flip flops
        * I/O pads
        * Cells with dont_use attribute
        * Cells with three_state attribute
```

What Next

Remove the *fpga_complex_degenerate* attribute for this component, or set the attribute to FALSE.

LBDB-315

(error) The '%s' attribute is incorrectly specified in the context.

Description

The attribute indicated in the error message is not valid, because it is not compatible with the template to which this internal_power group refers. For example, the *related_input* attribute cannot be specified in a two-dimensional table.

The following example shows an instance where this message occurs:

```
power_lut_template(output_by_cap_and_trans) {
  variable_1 : total_output_net_capacitance;
  variable_2 : input_transition_time;
```

Feedback

```
  index_1 ("0.0, 5.0, 20.0");
  index_2 ("0.1, 1.00, 5.00");
}

cell(lbdb315) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A+B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  cell_leakage_power : 1;
  internal_power(output_by_cap_and_trans) {
     values(" 5.000000 ,  15.000000 ,  0.300000 ", \
            " 1.000000 ,  5.000000 ,  0.000000 ", \
            " 0.000000 ,  0.000000 ,  0.000000 ");
     related_outputs : "Z";
     related_input : "A";
  }
}
```

The following is an example message:

```
Error: Line 315, The 'related_input' attribute is incorrectly specified
 in the context. (LBDB-315)
```

What Next

Refer to the Library Compiler manuals and the Design Power Reference manual for power modeling and analysis. Modify the library to correct the problem.

LBDB-316

(error) Arithmetic overflow or exception is encountered\n \ton the '%s' attribute with the '%s' value.

Feedback

Description

This message indicates that you specified an attribute's value that causes an arithmetic overflow or an exception. Library Compiler cannot handle the value.

The following example shows an instance where this message occurs:

```
fall_propagation ( table4x6 ) {
   index_1 ("2.00e+02 2.50e+02 3.50e+02 4.00e+02 ") ;
   index_2 ("4.48e-02 8.96e-02 1.34e-01 1.79e-01 2.24e-01 2.69e-01 ");
   values ("7.45e+01 9.56e+01 1.15e+02 1.34e+02 1.52e+02 1.71e+02 ", \
           "9.38e+01 1.20e+02 1.45e+02 1.67e+02 1.89e+02 2.10e+02 ", \
           "1.01e+02 1.32e+02 1.58e+02 1.83e+02 2.07e+02 2.29e+02 ", \
           "1.04e+02 1.43e-93 1.43e-93 1.43e-93 2.75e+226 9.30e+254 " ) ;
}
```

The following is an example message:

```
Error: Line 85, Arithmetic overflow or exception is encountered
        on the 'values' attribute with the '2.75e+226' value. (LBDB-316)
```

What Next

Check the library source file, and correct the problem.

LBDB-317

(error) It is invalid to specify the '%s' attribute\n \ton a pin within the bus or bundle group.

Description

This message indicates that you specified a function attribute on a pin within a bus or a bundle group.

The following example shows an instance where this message occurs:

```
bundle (qn) {
    members(qn2);
    direction : output;
    function : "iq";
    pin (qn2) {
      function : "q2";
    timing() {
       related_pin   : "q2";
       intrinsic_rise :  0.1;
       intrinsic_fall :  0.1;
       rise_resistance : 1.0;
       fall_resistance : 1.0;
    }
  }
```

The following is an example message:

```
Error: Line 67, It is invalid to specify the 'function' attribute
        on a pin within the bus or bundle group. (LBDB-317)
```

What Next

Check the library source file, and correct the problem.

LBDB-318

(warning) the user specified timing sense '%s' is different \n \tfrom the function calculated timing_sense '%s'.

Description

```
In timing group of a pin, timing_sense should match the function of the
 pin.
```

The following example shows an instance where this message occurs:

```
cell(INV) {
  pin (Y) {
    timing () {
      related_pin : "A";
      timing_sense : positive_unate;
    }
    function : "!A"
  }
  ...
}
```

If timing_sense is specified, the Library Compiler calculates the value for it from the pin's logic function. And issues this warning if specified timing_sense is different from the calculated one. The user sepcified timing_sense will be stored in .db.

For example, the value calculated for an AND gate is positive_unate, the value for a NAND gate is negative_unate, and the value for an XOR gate is non_unate. For the above example, the value for an INV is negative_unate.

If timing_sense is not specified, the Library Compiler calculates and derives the value for it from the pin's logic function. The derived timing_sense will be stored in .db.

A function is unate if a rising (or falling) change on a positive unate input variable causes the output function variable to rise (or fall) or not change. A rising (or falling) change on a negative unate input variable causes the output function variable to fall (or rise) or not change. For a nonunate variable, further state information is required to determine the effects of a particular state transition.

The following is an example message:

```
Warning: Line 123, Cell 'INV', pin 'Y', the user specified timing sense
'positive_unate' is different from the function calculated timing_sense
'negative_unate'. (LBDB-318)
```

What Next

Correct the value of the timing_sense.

LBDB-319

(Information) Voltage '%s' is used but not declared. A legacy value of '%g' is assumed.

Description

This message indicates that the Voltage 'VDD'(or 'VCC', 'VSS') is used in the expression, but not declared in voltage_map. Thus a legacy value of '5'(or '5', '0') is assumed.

The following example shows an instance where this message occurs:

```
library (lbdb319) {
    voltage_map ( IOVDD1, 1.32 );
    voltage_map ( COREVDD1, 0.875 );
    voltage_map ( IOCOREGND1, 0 );
    input_voltage(cmos11) {
        vil : 0.35 * VDD ;
        vih : 0.65 * VDD ;
        vimin : -0.3 ;
        vimax : 1.32 ;
    }
}
```

The following is an example message:

```
Information: Line 34, Voltage 'VDD' is used but not declared. A legacy
 value of '5' is assumed. (LBDB-319)
```

What Next

No action is required.

LBDB-353

(warning) A nonsequential timing arc is specified with\n \trespect to the '%s' clock pin.

Description

The cell has the *interface_timing* attribute set to TRUE. The interface timing policy requires that all timing arcs defined with respect to a clock pin be sequential (noncombinational) in nature.

Feedback

The following example shows an instance where this message occurs:

```
cell (lbdb353) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
        timing_type : setup_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall :  1.0;
        related_pin : "CLK";
      }
      timing () {
        timing_type : hold_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "CLK";
      }
    }
    pin (CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      clock : true;
      timing () {
        timing_type : skew_rising;
        intrinsic_rise : 1.0;
        related_pin : "CLK1";
      }
    }

    pin (CLK1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
        timing_type : skew_falling;
        intrinsic_rise : 1;
        related_pin : "CLK";
      }
    }
    pin(Q){
      direction   :   output;
      timing () {
        intrinsic_rise   : 1.0;
        rise_resistance  : 0.1;
        intrinsic_fall   : 1.0;
        fall_resistance  : 0.1;
        related_pin      : "CLK";
      }
```

```
    }
  }
```

In this case, the 'Q' pin is missing the timing_type attribute in its timing group.

The following is an example message:

```
Warning: Line 62, A nonsequential timing arc is specified with
        respect to the 'CLK' clock pin. (LBDB-353)
```

What Next

Make sure that all arcs with a clock pin as a related_pin are sequential.

LBDB-354

(warning) A sequential timing arc is specified with respect\n \tto the '%s' nonclock pin.

Description

The cell has the *interface_timing* attribute set to TRUE. The interface timing policy requires that all sequential timing arcs (except for clear and preset) be defined with respect to a pin that is labeled as a clock.

The following example shows an instance where this message occurs:

```
cell (lbdb354) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
        timing_type : setup_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall :  1.0;
        related_pin : "CLK";
      }
      timing () {
        timing_type : hold_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "CLK";
      }
    }
    pin (CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      clock : true;
      timing () {
```

```
        timing_type : skew_rising;
        intrinsic_rise : 1.0;
        related_pin : "CLK1";
      }
    }

    pin (CLK1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
        timing_type : skew_falling;
        intrinsic_rise : 1;
        related_pin : "CLK";
      }
    }
    pin(Q){
      direction   :   output;
      timing () {
        intrinsic_rise   : 1.0;
        rise_resistance  : 0.1;
        intrinsic_fall   : 1.0;
        fall_resistance  : 0.1;
        related_pin      : "CLK";
      }
    }
  }
```

In this case, the 'CLK' pin has a timing group with a timing_group value skew_rising related to the 'CLK1' pin.

The following is an example message:

```
Warning: Line 40, A sequential timing arc is specified with respect
        to the 'CLK1'  nonclock pin. (LBDB-354)
```

What Next

Make sure that all sequential arcs are defined with respect to a clock pin.

LBDB-355

(warning) A skew constraint is specified for the nonclock '%s' pin.

Description

A skew constraint is specified for a pin that is not a clock. All clock pins must have the *clock* attribute set to TRUE.

Feedback

The following example shows an instance where this message occurs:

```
cell (lbdb355) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
        timing_type : setup_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall :  1.0;
        related_pin : "CLK";
      }
      timing () {
        timing_type : hold_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "CLK";
      }
    }
    pin (CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      clock : true;
      timing () {
        timing_type : skew_rising;
        intrinsic_rise : 1.0;
        related_pin : "CLK1";
      }
    }

    pin (CLK1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
        timing_type : skew_falling;
        intrinsic_rise : 1;
        related_pin : "CLK";
      }
    }
    pin(Q){
      direction   :   output;
      timing () {
        intrinsic_rise   : 1.0;
        rise_resistance  : 0.1;
        intrinsic_fall   : 1.0;
        fall_resistance  : 0.1;
        related_pin      : "CLK";
      }
```

```
    }
  }
```

In this case, the 'CLK1' pin has skew constraint timing group on the nonclock 'CLK' pin. Because Library Compiler failed to recognize the 'CLK' pin.

The following is an example message:

```
Warning: Line 52, A skew constraint is specified for the nonclock 'CLK1'
 pin. (LBDB-355)
```

What Next

Make sure that skew constraints are defined for clock pins only. Check the library source file, and either set the *clock* attribute to TRUE on the pin, or remove the skew constraint.

LBDB-356

(warning) Multiple %s constraints are specified between\n \tthe '%s' pin and the '%s' clock pin.

Description

Design Compiler takes the worst case constraint when multiple constraints are specified.

The following example shows an instance where this message occurs:

```
cell (lbdb356) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      timing () {
        timing_type : setup_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "CLK";
      }
      timing () {
        timing_type : hold_rising;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "CLK";
      }
      timing () {
        timing_type : hold_falling;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "CLK";
      }
```

Feedback

```
    }
    pin (CLK)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      clock : true;
    }
    pin(Q){
      direction   :   output;
      timing () {
        timing_type      : rising_edge;
        intrinsic_rise   : 1.0;
        rise_resistance  : 0.1;
        intrinsic_fall   : 1.0;
        fall_resistance  : 0.1;
        related_pin      : "CLK";
      }
    }
  }
```

In this case, the 'I1' pin has two hold constraints.

The following is an example message:

```
Warning: Line 31, Multiple setup or hold constraints are specified
        between the 'I1' pin and the 'CLK' clock pin. (LBDB-356)
```

What Next

PrimeTime supports multiple setup/hold constraints.

LBDB-357

(warning) The '%s' cell has the interface_timing attribute,\n \tbut has no clock pin.

Description

According to interface timing specification policy, a library cell with the interface timing attribute set to TRUE must have at least one pin labeled as a clock.

The following example shows an instance where this message occurs:

```
cell (lbdb357) {
    area    :   0.0;
    interface_timing : TRUE;
    pin (I1)    {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
    }
    pin(Q){
      direction   :   output;
```

Feedback

```
      function : "I1'";
      timing () {
        intrinsic_rise   : 1.0;
        rise_resistance  : 0.1;
        intrinsic_fall   : 1.0;
        fall_resistance  : 0.1;
        related_pin      : "I1";
      }
    }
  }
```

The following is an example message:

```
Warning: Line 6, The 'combo' cell has the interface_timing attribute,
        but has no clock pin. (LBDB-357)
```

What Next

If the cell is combinational, remove the *interface_timing* attribute set on the cell. If the cell is sequential in nature, add the *clock* attribute to all clock pins of the cell. If the cell does not have a clock pin (like a RAM), choose the control pin with respect to which setups and holds are measured, and label it as a clock.

LBDB-358

(error) It is not legal to specify the attribute '%s' in\n \tthe '%s' group in this context.

Description

The indicated attribute cannot be specified in the indicated group because of the context. This situation can arise if the group can have several types and the attribute can only appear when the group is of specific type.

What Next

Check your library to see if you have specified the wrong information for the group or if the attribute should be deleted from the group.

LBDB-366

(warning) The '%s' attribute in char_config group is required for NLPM library. \n No default can be applied to this attribute.

Description

From 2017.06 release, user will see LBDB-366 Warning when the library contains internal_power group, but NO internal_power_calculation attribute defined in library-level char_config group.

Feedback

The internal_power_calculation attribute takes enumerated values:

```
exclude_switching_on_rise
  exclude_switching_on_rise_and_fall
  include_switching
```

This attribute is critical for tools like PTPX to determine the meaning of internal_power table values.

What Next

Please define internal_power_calculation attribute in library-level char_config group when library contains NLPM data.

LBDB-370

(error) The library contains a '%s' group,\n \tbut has no contain '%s' group.

Description

This message indicates that you specified only one transition degradation table in the library. Libraries that contain transition degradation tables must have tables for both rise and fall transitions.

The following example shows an instance where this message occurs:

```
rise_transition_degradation(trans_deg) {
        values("0.0, 0.6", \
               "1.0, 1.6");
}
```

In this case, the 'fall_transition_degradation' group is missing. To fix the problem, add this group to the library,

```
fall_transition_degradation(trans_deg) {
        values("0.0, 0.8", \
               "1.0, 1.8");
}
```

The following is an example message:

```
Error: Line 46, The library contains a 'rise_transition_degradation'
 group,
        but has no 'fall_transition_degradation' group. (LBDB-370)
```

What Next

Add the missing table group to the library description.

Feedback

LBDB-371

(error) The '%s' lut group is missing the mandatory '%s' attribute.

Description

This message indicates that you specified a lut group without the input_pins attribute in a FPGA library.

The following example shows an instance where this message occurs:

```
cell(lut5) {
    area : 1.0;
    lut(lbdb371) {
      /*      input_pins : "a b c d e"; */
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "lbdb371";
      timing() {
        related_pin : "a b c d e";
      }
    }
  }
```

The following is an example message:

```
Error: Line 98, The 'lbdb371' lut group is missing the mandatory
 'input_pins' attribute. (LBDB-371)
```

What Next

Check the library source file, and add the missing attribute.

LBDB-372

(error) The '%s' lut group attribute has an invalid '%s' value.

Description

This message indicates that you specified a lut group with an invalid value for the input_pins attribute in a FPGA library.

The following example shows an instance where this message occurs:

```
cell(lut5) {
    area : 1.0;
```

Feedback

```
    lut(R) {
    input_pins : "";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e";
      }
    }
  }
```

The following is an example message:

```
Error: Line 98, The 'input_pins' lut group attribute has an invalid ''
 value. (LBDB-372)
```

What Next

Check the library source file, and correct the value of the input_pins attribute.

LBDB-373

(error) The '%s' cell has more than one lut group defined.

Description

This message indicates that you specified more than one lut group in the FPGA library.

The following example shows an instance where this message occurs:

```
cell(lbdb373) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e";
    }
    lut(R1) {
      input_pins : "a b c d e";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e";
```

```
      }
    }
  }
```

The following is an example message:

```
Error: Line 96, The 'lbdb373' cell has more than one lut group defined.
 (LBDB-373)
```

What Next

Check the library source file, and delete the extra lut groups.

LBDB-374

(error) The '%s' input port is not in the '%s' lut.

Description

This message indicates that you did not specify an input port in lut group.

The following example shows an instance where this message occurs:

```
cell(lbdb374) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e";
    }
    pin(a b c d e f) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e";
      }
    }
  }
```

The following is an example message:

```
Error: Line 101, The 'f' input port is not in the 'lbdb374' lut.
 (LBDB-374)
```

What Next

Check the library source file, and either add the input port to the lut group or delete the port.

Feedback

LBDB-375

(error) The '%s' port is incorrectly listed as an input in the\n \t'%s' lut.

Description

This message indicates that you specified a noninput port in the lut group.

The following example shows an instance where this message occurs:

```
cell(lbdb375) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e o";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e";
      }
    }
  }
```

The following is an example message:

```
Error: Line 98, The 'o' port is incorrectly listed as an input in the
        'lbdb375' lut. (LBDB-375)
```

What Next

Check the library source file, and delete the noninput port from the lut group.

LBDB-376

(error) The '%s' port is invalid in a cell containing a lut group.

Description

This message indicates that you specified an invalid port in a cell containing a lut group. Ports in a cell with a lut are either input or output.

The following example shows an instance where this message occurs:

```
cell(lbdb376) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e ";
```

Feedback

```
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(f) {
      direction : inout;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e";
      }
    }
  }
```

The following is an example message:

```
Error: Line 105, The 'f' port is invalid in a cell containing a lut
 group. (LBDB-376)
```

What Next

Check the library source file, and correct the direction of the port.

LBDB-377

(error) The '%s' lut group is invalid in a multiple output cell.

Description

This message indicates that you specified more than one output port in a cell containing a lut group.

The following example shows an instance where this message occurs:

```
cell(lbdb377) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e ";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(f) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e";
```

```
      }
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e";
      }
    }
  }
```

In this case, both 'f' and 'o' are output ports.

The following is an example message:

```
Error: Line 98, The 'R' lut group is invalid in a multiple output cell.
 (LBDB-377)
```

What Next

Check the library source file, and delete the extra output ports.

LBDB-378

(error) The '%s' lut group is invalid in a cell with no outputs.

Description

This message indicates that you did not specify any output port in a cell containing a lut group.

The following example shows an instance where this message occurs:

```
cell(lbdb378) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e ";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
  }
```

In this case, the 'lbdb378' has no output port.

The following is an example message:

```
Error: Line 98, The 'R' lut group is invalid in a cell with no outputs.
 (LBDB-378)
```

Feedback

What Next

Check the library source file, and either add the output port or delete the lut group.

LBDB-379

(error) The '%s' output port on the '%s' cell has no\n \tfunction attribute, or the function attribute is invalid with\n \tthe lut group on this cell.

Description

This message indicates that either you specified an invalid function attribute on the output port a cell containing a lut group, or you did not define the function attribute.

The following example shows an instance where this message occurs:

```
cell(lbdb379) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e ";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      timing() {
        related_pin : "a b c d e";
      }
    }
  }
```

In this case, The function attribute is missing in the 'o' port. To fix the problem, add the statement

```
function : "R";
```

The following is an example message:

```
Error: Line 113, The 'o' output port on the 'lbdb379' cell has no
        function attribute, or the function attribute is invalid with
        the lut group on this cell. (LBDB-379)
```

What Next

Check the library source file, and either add or correct the function attribute.

Feedback

LBDB-380

(error) The '%s' name is invalid for a lut group in the '%s'\n \tcell because a port on the design has the same name.

Description

This message indicates that there is a name conflict between the specified lut group name and a port name. The names of the lut groups must be unique and must not conflict with existing port names.

The following example shows an instance where this message occurs:

```
cell(lbdb380) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e";
    }
    pin(a b c d e) {
      direction : input;
      capacitance : 0.0;
    }
    pin(R) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e";
      }
    }
  }
```

The following is an example message:

```
Error: Line 98, The 'R' name is invalid for a lut group in the 'lbdb380'
        cell because a port on the design has the same name. (LBDB-380)
```

What Next

Change the name of the lut group so that it is unique.

LBDB-381

(error) The '%s' lut cell has %d input port(s). A lut\n \tcell must have at least 1 but no more than 9 input ports.

Description

This message indicates that the specified lut cell has either too many or too few input ports. lut cells must have at least 1 but not more than 9 input ports.

Feedback

The following example shows an instance where this message occurs:

```
cell(lbdb381) {
    area : 1.0;
    lut(R) {
      input_pins : "a b c d e f g h i j";
    }
    pin(a b c d e f g h i j) {
      direction : input;
      capacitance : 0.0;
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "a b c d e f g h i j";
      }
    }
  }
```

The following is an example message:

```
Error: Line 98, The 'lbdb381' lut cell has 10 input port(s). A lut
        cell must have at least 1 but no more than 9 input ports.
 (LBDB-381)
```

What Next

Edit the lut cell description in your library so that the cell has at least 1 but not more than 9 input ports.

LBDB-382

(error) The '%s' cell is an invalid lut cell. Only\n \tsimple combinational cells are valid.

Description

This message indicates that the specified cell is not a simple combinational cell, which is the only valid type of lut cell.

The following example shows an instance where this message occurs:

```
cell(lbdb382) {
    area : 1.0;
    lut(R) {
      input_pins : "D CP";
    }
    pin(D CP ) {
      direction : input;
      capacitance : 0.0;
    }
    ff("IQ","IQN") {
```

Feedback

```
      next_state : "D";
      clocked_on : "CP";
    }
    pin(o) {
      direction : output;
      function : "R";
      timing() {
        related_pin : "D CP";
      }
    }
  }
```

The following is an example message:

```
Error: Line 96, The 'lbdb382' cell is an invalid lut cell. Only
        simple combinational cells are valid. (LBDB-382)
```

What Next

Remove the lut construct from this cell description, or modify the cell so that it is a simple combinational cell.

LBDB-383

(error) The '%s' attribute is invalid on\n \tthe '%s' lut cell.

Description

This message indicates that the specified attribute is not valid on the specified lut cell.

The following example shows an instance where this message occurs:

```
cell(lbdb383) {
    area : 1.0;
    fpga_lut_output : true;
    lut(R) {
      input_pins : "A B C D";
    }
    pin(A B C D) {
        direction : input;
        capacitance : 0.0;
    }
    pin(Z) {
        direction : output;
        function : "R";
        timing() {
            intrinsic_rise : 5.0;
            intrinsic_fall : 5.0;
            related_pin : "A B C D";
        }
    }
}
```

The following is an example message:

```
Error: Line 25, The 'fpga_lut_output' attribute is invalid on
        the 'lbdb383' lut cell.  (LBDB-383)
```

What Next

Remove the offending attribute from the lut cell.

LBDB-384

(error) The lut marker cell attribute\n \t'%s' is invalid on the '%s' cell.

Description

This message indicates that a lut marker cell attribute has been found on the specified cell, identifying it as a lut marker cell. However, the cell is not a valid candidate for a lut marker cell because it is not a single output buffer cell with 0 area.

Lut marker cells delimit the boundaries of luts and must be single-output buffer cells with 0 area.

The following example shows an instance where this message occurs:

```
cell(lbdb384) {
    area : 0.0;
    fpga_lut_insert_before_sequential : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z) {
      direction : output;
      function : "A";
      timing() {
        intrinsic_rise : 0.0;
        intrinsic_fall : 0.0;
        related_pin : "A";
      }
    }
  }
```

The following is an example message:

```
Error: Line 126, The lut marker cell attribute
        'fpga_lut_insert_before_sequential' is invalid on the 'lbdb384'
 cell. (LBDB-384)
```

What Next

Either remove the lut marker cell attribute from the cell, or edit the cell description to make it a valid marker cell; that is, a single output buffer cell with 0 area.

Feedback

LBDB-385

(error) The lut marker '%s' cell is functionally invalid.\n \tLut marker cells must be single output buffers.

Description

This message indicates that the specified marker cell is not a single output buffer, which is the only valid lut marker cell type.

The following example shows an instance where this message occurs:

```
cell(lbdb385) {
    area : 0.0;
    fpga_lut_output : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z1) {
      direction : output;
      function : "A";
      timing() {
        intrinsic_rise : 0.0;
        intrinsic_fall : 0.0;
        related_pin : "A";
      }
    }
    pin(Z2) {
      direction : output;
      function : "A";
      timing() {
        intrinsic_rise : 0.0;
        intrinsic_fall : 0.0;
        related_pin : "A";
      }
    }
  }
```

In this case, there are two output ports in the cell.

The following is an example message:

```
Error: Line 143, The lut marker 'lbdb385' cell is functionally invalid.
        Lut marker cells must be single output buffers. (LBDB-385)
```

What Next

Remove the marker cell attribute from the cell, or change the cell's functionality so that it is a single output buffer.

Feedback

LBDB-386

(warning) The lut marker '%s' cell has a nonzero\n \t'%s' attribute. Marker cells must have \n \tzero area and zero delay.

Description

This message indicates that the specified area or delay value in the library is nonzero, which is invalid for lut marker cells.

The following example shows an instance where this message occurs:

```
cell(lbdb386) {
    area : 0.0;
    fpga_lut_output : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z) {
      direction : output;
      function : "A";
      timing() {
        intrinsic_rise : 1.0;
        intrinsic_fall : 0.0;
        related_pin : "A";
      }
    }
  }
```

In this case, the 'intrinsic_rise' value is 1.0. Change the value to zero to fix the problem.

The following is an example message:

```
Warning: Line 169, The lut marker 'lbdb386' cell has a nonzero
        'intrinsic rise delay' attribute. Marker cells must have
        zero area and zero delay. (LBDB-386)
```

What Next

Change the offending nonzero value (area or delay, as appropriate) to zero.

LBDB-387

(warning) The '%s' library has more than one lut output marker cell.

Description

This message indicates that the specified library has too many lut output marker cells. Each library can have only one lut output marker cell.

Feedback

The following example shows an instance where this message occurs:

```
library(lbdb387) {
  ...
  cell(marker1) {
    area : 0.0;
    fpga_lut_output : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z) {
      direction : output;
      function : "A";
      timing() {
        intrinsic_rise : 0.0;
        intrinsic_fall : 0.0;
        related_pin : "A";
      }
    }
  }

  cell(marker2) {
    area : 0.0;
    fpga_lut_output : true;
    pin(A) {
      direction : input;
      capacitance : 0.0;
    }
    pin(Z) {
      direction : output;
      function : "A";
      timing() {
        intrinsic_rise : 0.0;
        intrinsic_fall : 0.0;
        related_pin : "A";
      }
    }
  }
}
```

The following is an example message:

```
Warning: Line 56, The 'lbdb387' library has more than one lut output
 marker cell. (LBDB-387)
```

What Next

Check the library source file, and remove the duplicate output marker cells.

Feedback

LBDB-388

(error) The '%s' attribute cannot be specified in a\n \ttiming arc that is not a timing constraint.

Description

This message indicates that an attribute has been incorrectly specified. The specified attribute is allowed only on timing arcs that are timing constraints (for example, setup and hold).

The following example shows an instance where this message occurs:

```
pin(Q) {
      direction : output;
      function : "IQ";
      timing() {
        timing_type : falling_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        when_end : "D0";
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CK2";
      }
    }
```

In this case, the 'falling_edge' timing_type value is not a constraint.

The following is an example message:

```
Error: Line 94, The 'when_end' attribute cannot be specified in a
        timing arc that is not a timing constraint. (LBDB-388)
```

What Next

Check the library source file, and make the appropriate correction. For example, change the timing type to be a timing constraint.

LBDB-389

(error) This timing arc has either '%s' or '%s'\n \tattribute but not both.

Description

This message indicates that in a timing group, you defined only one attribute from the following sets:

```
* when attribute and sdf_cond attribute
        * when_start attribute and sdf_cond_start attribute
        * when_end attribute and sdf_cond_end attribute
```

Feedback

To define a state dependent timing arc, Library Compiler expects both attributes defined.

The following example shows an instance where this message occurs:

```
pin(Z) {
        direction : output;
        function : "A^B";
        timing() {
          when : "B'";
          timing_sense : positive_unate;
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "A";
        }
```

In this case, only the 'when' attribute is specified. To fix the problem, add the statement,

```
sdf_cond : "!B";
```

The following is an example message:

```
Error: Line 88, This timing arc has either 'when' or 'sdf_cond'
        attribute but not both. (LBDB-389)
```

What Next

Complete your specification by adding appropriate attributes to the timing group.

LBDB-390

(warning) The when and/or sdf_cond attributes in this\n \ttiming arc are ignored.

Description

This message indicates that you specified, in addition to the *when_start*, *when_end*, *sdf_cond_start*, or *sdf_cond_end* attributes in the timing (constraint) group, the *when* and *sdf_cond* attributes. Library Compiler ignores the *when* and *sdf_cond* attributes.

The following example shows an instance where this message occurs:

```
timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      sdf_edges : start_edge;
      when : " CD * SD ";
      sdf_cond : " SIG_2 == 1'b1 ";
      when_end : " CD * SD * Q' ";
      sdf_cond_end : " SIG_0 == 1'b1";
```

Feedback

```
      related_pin : "CP";
    }
```

In this case, both the when and sdf_cond pair and the when_end and sdf_cond_end are specified.

The following is an example message:

```
Warning: Line 836, The when and/or sdf_cond attributes in this
        timing arc are ignored. (LBDB-390)
```

What Next

Remove the redundant *when* and/or *sdf_cond* attributes from the timing group.

LBDB-391

(warning) The '%s' attribute on pin '%s' is not valid.\n \tThe attribute is ignored.

Description

This message indicates that the attribute on the specified pin is invalid. The attribute is ignored. This situation occurs when other information specified on the same pin is incompatible with the attribute. For example, the *min_period* attribute is ignored if the *minimum_period* group is also specified on the same pin.

The following example shows an instance where this message occurs:

```
pin (CLK) {
    direction : input ;
    capacitance : 0 ;
    min_pulse_width_low  : 3 ;
    min_pulse_width_high : 3 ;
    min_period : 5.0;
    minimum_period() {
      constraint : 1.0;
      when : "D PRE";
      sdf_cond : "cond_1 == 1'b1";
    }
  }
```

The following is an example message:

```
Warning: Line 183, The 'min_period' attribute on the 'CLK' pin is not
 valid.
        The attribute is ignored. (LBDB-391)
```

What Next

Refer to the *Library Compiler Reference Manual* to determine the reason why the attribute is not valid. Change the library source file and make the correction.

Feedback

LBDB-392

(error) The ECL Technology is obsolete with v3.4b. Compilation terminated abnormally.

Description

This error occurs when the ECL Technology is used. This technology is supported up to v3.4a but not for subsequent releases.

The following example shows an instance where this message occurs:

```
library(lbdb392) {
  technology(ecl);
  delay_model : "generic_ecl" ;
}
```

The following is an example message:

```
Error: The ECL Technology is obsolete with v3.4b. Compilation terminated
 abnormally. (LBDB-392)
```

What Next

Use the supported technologies.

LBDB-393

(error) Too many values entered for the driver_type attribute.

Description

This error occurs when more than two values entered for a driver_type attribute in defining a simple attribute.

The following example shows an instance where this message occurs:

```
pin(y) {
      direction : inout;
      function : 1;
      three_state : "a";
      driver_type : "open_source pull_down resistive";
      timing() {
        timing_type : three_state_disable;
        related_pin : "a";
      }
      timing() {
        related_pin : "a";
      }
    }
```

In the driver_type line, three driver_types are specified for this pin.

Feedback

The following is an example message:

```
Error: Line 458, Too many values entered for the driver_type attribute.
 (LBDB-393)
```

What Next

Only inout pin allows for two driver_type values. Other pins can have only one value. During passing, we first catch the case where more than two are entered.

LBDB-394

(error) The driver type %s is incompatible with the %s pin %s.

Description

Valid driver-type (programmable or non-programmable) and pin combinations (Y means valid):

non-programmable input output inout programmable
==========
pull_up Y Y Y pull_up_function pull_down Y Y Y pull_down_function open_drain N Y Y open_drain_function open_source N Y Y open_source_function bus_hold N N Y bus_hold_function resistive N Y Y resistive_function resistive_0 N Y Y resistive_0_function resistive_1 N Y Y resistive_1_function open_drain_with_pull_up N N Y open_drain_with_pull_down N N Y open_source_with_pull_up N N Y open_source_with_pull_down N N Y
==========

The following example shows an instance where this message occurs:

```
pin(a) {
      direction : input;
      capacitance : "1";
      driver_type : "open_source pull_up";
    }
```

The following is the example message:

```
Error: Line 177, The driver type open_source_with_pull_up is incompatible
        with the input pin a. (LBDB-394)
```

The following example shows another instance where this message occurs followed by the example message:

```
pin(A3) {
  direction : input;
  pull_up_function : "!A1 * !A2 * !A3";
  pull_down_function : "A1 * A2 * !A3";
  bus_hold_function : "A1 * !A2 * !A3";
  open_drain_function : "!A1 * A2 * !A3";
```

Feedback

```
  open_source_function : "!A1 * !A2 * A3";
  resistive_function : "A1 * A2 * A3";
  resistive_0_function : "A1 * !A2 * A3";
  resistive_1_function : "!A1 * A2 * A3";
  ...
 }
```

In this case, only pull_up_function and pull_down_function can be specified under an input pin. To avoid the error, please remove the rest of 6 programmable driver types.

The following is the example message:

```
Error: Line 217, The driver type open_drain_function is incompatible with
 the input pin A3. (LBDB-394)
```

What Next

When single pull_up/down applys to an inout pin, it is for the input behavior; other single types applying to an inout pin are for the output behavior. Always comply with the above rules.

LBDB-395

(warning) The timing arc with timing_type '%s'\n can only be specified on a pin with 'input' or 'inout' direction.

Description

The timing_type non_seq_setup_rising, non_seq_setup_falling, non_seq_hold_rising and non_seq_hold_falling can only be specified on a timing arc on the input or the inout pins.

The following example shows an instance where this message occurs:

```
pin(Z) {
          direction : output;
          timing() {
            timing_type : non_seq_setup_rising;
            ...
          }
        }
```

The following is an example message: Warning: Line 144, The timing arc with timing_type 'non_seq_setup_rising' can only be specified on a pin with 'input' or 'inout' direction. (LBDB-395)

What Next

Check the timing arc and make the correction to either the direction of the pin or delete the timing arc or move it to the appropriate place.

Feedback

LBDB-396

(warning) The 'related_output_pin' attribute is only needed\n when the delay table refers to a template which uses the\n output loading of the related_output_pin in one of its dimension.

Description

This can happen when the 'related_output_pin' is not needed in this timing arc or the template name used by this table is wrong or the template itself should use the output loading of the related_output_pin in one of its dimension.

The following example shows an instance where this message occurs:

```
lu_table_template(prop) {
          variable_1 :  output_net_length;
          index_1 ("1, 5, 10");
        }

        cell(A) {

          pin(O) {
            timing() {
              related_output_pin : "Z";
              rise_propagation(prop) {
                ...
              }
            }
          }
        }
```

The following is an example message: Warning: Line 144, The 'related_output_pin' attribute is only needed when the delay table refers to a template which uses the output loading of the related_output_pin in one of its dimension. (LBDB-396)

The timing arc is a rise_propagation table which refers to the template 'prop'. In the template, the only variable it depends on is the loading of the output pin. There is not dependency on the loading of pin 'Z' and there is no need to put the 'related_output_pin' in the timing group.

What Next

Check the table or the template to see if the related_output_pin attribute is actually needed here. If not, just delete the attribute.

LBDB-397

(error) There can only be one pin in the 'related_output_pin'\n attribute and the pin should be single bit.

Feedback

Description

The "related_output_pin" attribute is used for figuring out the output loading to index into the table. It is not possible to determine which output pin to use for this purpose if there is more than one pin specified in the attribute. Multiple bits specification also have the same problem.

The following example shows an instance where this message occurs:

```
timing() {
          related_output_pin : "Z1 Z2";
          ...
        }
```

The following is an example message: Error: Line 144, There can only be one pin in the 'related_output_pin' attribute and the pin should be single bit. (LBDB-397)

There are two pins, Z1 and Z2, in the related_output_pin attribute. It is not possible to figure out which pin should be used to figuring out the loading to index into the timing table.

What Next

Check the 'related_output_pin' attribute and make the correction according to the real electrical characteristics.

LBDB-398

(error) The pin '%s' specified in the 'related_output_pin'\n attribute is not an output or inout pin.

Description

The pin specified in the 'related_output_pin' attribute should have the direction 'output' or 'inout'.

The following example shows an instance where this message occurs:

```
pin(A) {
          direction : input;
          ...
        }
        pin(B) {
          timing() {
            related_output_pin : "A";
            ...
          }
        }
```

The following is an example message: Error: Line 144, The pin 'A' specified in the 'related_output_pin' attribute is not an output or inout pin. (LBDB-398)

Feedback

Pin 'A' is an input pin and cannot be put into the 'related_output_pin' attribute.

What Next

Check the 'related_output_pin' attribute to see if you have put the wrong pin in it or you forgot to put the correct pin direction on the pin specified in the 'related_output_pin' attribute.

LBDB-399

(error) The timing_type '%s' is not supported\n with the 'related_output_pin' attribute.

Description

The timing_type supported with the 'related_output_pin' attribute are: 'setup_rising', 'setup_falling', 'hold_rising', 'hold_falling', 'non_seq_setup_rising', 'non_seq_setup_falling', 'non_seq_hold_rising', 'non_seq_hold_falling', 'skew_rising', 'skew_falling', 'removal_rising', 'removal_falling', 'recovery_rising' and 'recovery_falling'.

The following example shows an instance where this message occurs:

```
timing() {
          timing_type : rising_edge;
          related_output_pin : "A";
          ...
        }
```

The following is an example message: Error: Line 144, The timing_type 'rising_edge' is not supported with the 'related_output_pin' attribute.. (LBDB-399)

What Next

You may either put the wrong timing_type for the timing group or delete the timing group if it is not supported or the 'related_output_pin' attribute is not needed.

LBDB-400

(warning) The '%s' operating condition has been defined \n \tmultiple times in the '%s' library. \n \tDesign Compiler will use the first definition only.

Description

The library contains more than one definition of an operating condition. Library Compiler issues this error message, records all definitions, but Design Compiler will only use the first definition encountered.

The following example shows an instance where this message occurs:

```
operating_condition(P1V1) {
    ...
```

Feedback

```
  }
  operating_condition(P1V1) {
    ...
  }
```

The following is an example message:

```
Warning: Line 50, The 'P1V1' operating condition has been defined
        multiple times in the 'sample-library' library.
        Design compiler will use the first one only. (LBDB-400)
```

What Next

Change the operating condition name if it is wrong, or delete all extra definitions.

LBDB-401

(error) The '%s' is missing for this timing check.

Description

Both rise and fall constraint values are required in the nochange timing check.

The following example shows an instance where this message occurs:

```
pin ( EN )    {
      direction : input;
      timing ()      {
        timing_type : nochange_high_high;
        related_pin : CP ;
        rise_constaint(cons) {
          values("0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000");
        }
      }
    }
```

To fix the problem, add the attribute to the timing group,

```
fall_constraint(cons) {
          values("0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000",  \
                 "0.100000, 0.100000, 0.100000");
        }
```

Feedback

The following is an example message:

```
Error: Line 104, The 'fall_constraint' is missing for this timing check.
 (LBDB-401)
```

What Next

Check the library source file to see if you missed the rise or fall constraint value. Otherwise, use setup or hold check instead.

LBDB-402

(error) The '%s' is missing for this internal_power group.

Description

Internal_power groups require specification of either (1) both the rise_power and fall_power attributes; or (2) the power attribute.

The following example shows an instance where this message occurs:

```
pin ( EN )    {
      direction : input;
      internal_power ()      {
        rise_power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
      }
    }
```

To fix the problem, add the attribute to the internal_power group.

```
fall_power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
```

The following is an example message:

```
Error: Line 104, The 'fall_power' is missing for this internal_power
 group. (LBDB-402)
```

What Next

Check the library source file to see if you missed the rise_power, fall_power, or power attribute.

LBDB-403

(error) The '%s' and '%s' attributes are both defined for this\n \tinternal_power group.

Feedback

Description

Internal_power groups require specification of either 1 both the rise_power and fall_power attributes; or 2. the power attribute.

However, it is an error to mix both the specifications.

The following example shows an instance where this message occurs:

```
pin ( EN )    {
      direction : input;
      internal_power ()      {
        power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
        rise_power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
      }
    }
```

To fix the problem, remove the rise_power attribute from the internal_power group, or remove power attribute and add the following fall_power attribute from the internal_power group.

```
fall_power(power_1d_temp) {
          values("0.100000, 0.100000, 0.100000");
        }
```

The following is an example message:

```
XXX
Error: Line 104, The 'rise_power' and 'power' attributes are both defined
 for this
       internal_power group. (LBDB-403)
```

What Next

Check the library source file to make sure that the previous requirement is met.

LBDB-404

(error) The '%s' lookup table in the input-associated\n \tinternal_power group cannot use '%s' as its template.

Description

The rise_power, fall_power, or power lookup tables in a input-associated internal_power group must use 1-dimensional template with input_transition_time as its variable.

Feedback

The following example shows an instance where this message occurs:

```
power_lu_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  power_lu_template(err_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }

        power(err_temp) {
                values ("1, 2, 3, 4");
        }
```

To fix the problem, change the template value of the power attribute from err_temp to ok_temp.

The following is an example message:

```
Error: Line 126, The 'power' lookup table in the input-associated
       internal_power group cannot use 'err_temp' as its template.
 (LBDB-404)
```

What Next

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

LBDB-405

(error) The 1-dimensional '%s' lookup table in the\n \tinout-associated internal_power group cannot use '%s' as its template.

Description

The 1-dimensional rise_power, fall_power, or power lookup tables in an inout-associated internal_power group must use a template with input_transition_time or total_output_net_capacitance as its variable.

The following example shows an instance where this message occurs:

```
power_lu_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  power_lu_template(ok2_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }
```

Feedback

```
power_lu_template(err_temp) {
  variable_1 : output_net_length;
  index_1("0, 1, 2, 3");
}

      power(err_temp) {
              values ("1, 2, 3, 4");
      }
```

To fix the problem, change the template value of the power attribute from err_template to ok_temp or ok2_temp.

The following is an example message:

```
Error: Line 126, The 1-dimensional 'power' lookup table in the
       inout-associated internal_power group cannot use
       'basic_template' as its template. (LBDB-405)
```

What Next

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

LBDB-406

(error) The 1-dimensional '%s' lookup table in the\n \t%s-associated internal_power group cannot use '%s' as its template.

Description

The 1-dimensional rise_power, fall_power, or power lookup tables in an output- associated internal_power group must use a template with total_output_net_capacitance as its variable.

The following example shows an instance where this message occurs:

```
power_lu_template(err_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  power_lu_template(ok_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }

      power(err_temp) {
              values ("1, 2, 3, 4");
      }
```

To fix the problem, change the template value of the power attribute from err_template to ok_temp.

The following is an example message:

```
Error: Line 126, The 1-dimensional 'power' lookup table in the
        output-associated internal_power group cannot use 'err_temp' as
 its template. (LBDB-406)
```

What Next

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

LBDB-407

(error) The 2-dimensional '%s' lookup table in the\n \t%s-associated internal_power group cannot use '%s' as its template.

Description

The 2-dimensional rise_power, fall_power, or power lookup tables in an output-associated internal_power group must use a template with input_transition_time and total_output_net_capacitance as its variables.

The following example shows an instance where this message occurs:

```
power_lu_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
    variable_2 : total_output_net_capacitance;
    index_2("0, 1, 2, 3");
  }
  power_lu_template(err_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
    variable_2 : constrained_pin_transition;
    index_2("0, 1, 2, 3");
  }

        power(err_temp) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

To fix the problem, change the template value of the power attribute from err_temp to ok_temp.

Feedback

The following is an example message:

```
Error: Line 126, The 2-dimensional 'power' lookup table in the
        output-associated internal_power group cannot use 'err_temp' as
 its template. (LBDB-407)
```

What Next

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

LBDB-408

(error) The 3-dimensional '%s' lookup table in the\n \t%s-associated internal_power group cannot use '%s' as its template.

Description

The 3-dimensional rise_power, fall_power, or power lookup tables in an output-associated internal_power group must use a template with input_transition_time, total_output_net_capacitance and equal_or_opposite_output_net_capacitance as its variables.

The following example shows an instance where this message occurs:

```
power_lu_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2");
    variable_2 : total_output_net_capacitance;
    index_2("0, 1, 2");
    variable_3 : equal_or_opposite_output_net_capacitance;
    index_3("0, 1, 2");
  }
  power_lu_template(err_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2");
    variable_2 : constrained_pin_transition;
    index_2("0, 1, 2");
    variable_3 : equal_or_opposite_output_net_capacitance;
    index_3("0, 1, 2");
  }

        power(err_temp) {
                values ("1,  2,  3",  "4,  5,  6",  "7, 8, 9", \
                      "10, 11, 12", "13, 14, 15", "16, 17, 18", \
                       "19, 20, 21", "22, 23, 24", "25, 26, 27");
        }
```

To fix the problem, change the template value of the power attribute from err_temp to ok_temp.

Feedback

The following is an example message:

```
Error: Line 126, The 3-dimensional 'power' lookup table in the
        output-associated internal_power group cannot use 'err_temp' as
 its template. (LBDB-408)
```

What Next

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

LBDB-409

(error) The %d-dimensional template used in '%s' lookup table\n \tis incompatible with the template used in '%s' lookup table.

Description

Both rise_power and fall_power lookup tables must have the same dimension. One exception is when the internal_power is an arc from a tri-state pin (that is related_pin is a tri-state pin), the dimension of rise_power and fall_power can be different.

The following example shows an instance where this message occurs:

```
power_lu_template(1d_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");

  power_lu_template(2d_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
    variable_2 : total_output_net_capacitance;
    index_2("0, 1, 2, 3");
  }

        rise_power(1d_temp) {
                values ("1, 2, 3, 4");
        }
        fall_power(2d_temp) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

To fix the problem, use 1-dimensional or 2-dimensional lookup tables on both rise_power and fall_power attributes.

Feedback

The following is an example message:

```
Error: Line 126, The %d-dimensional template used in '%s' lookup table
        is incompatible with the template used in '%s' lookup table.
 (LBDB-409)
```

What Next

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

LBDB-410

(error) The '%s' attribute is missing from the internal_power\n \tgroup.

Description

The related_pin or related_bus_pins attributes are required in an internal_power group with a 2-dimensional or 3-dimensional lookup table. The equal_or_opposite_output attribute is required in an internal_power group with a 3-dimensional look-up table.

The following example shows an instance where this message occurs:

```
internal_power() {
        power(power_2d) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
    }
```

To fix the problem, add the following line into the internal_power group.

```
related_pin : "A";
```

The following is an example message:

```
Error: Line 126, The 'related_pin or related_bus_pins' attribute is
 missing
        from the internal_power group. (LBDB-410)
```

What Next

Change the library source file by specifying related_pin, related_bus_pins, or equal_or_opposite_output attribute in the internal_power group as needed.

LBDB-411

(error) The internal_power group associated with pin '%s'\n \tcannot coexist with the cell-associated internal_power group in line %d.

Feedback

Description

It is not allowed to use cell-associated and pin-associated internal_power group for the same pin.

The following example shows an instance where this message occurs:

```
cell(AN2) {
        internal_power(power_1d_temp) {
            related_input : "A";
            values("0.100000, 0.100000, 0.100000");
        }
        pin (A) {
            direction : input;
            internal_power () {
                power(power_1d_temp) {
                    values("0.100000, 0.100000, 0.100000");
                }
            }
        }
        ...
    }
```

To fix the problem, remove internal_power group associated with cell group or pin group.

The following is an example message:

```
Error: Line 126, The internal_power group associated with pin 'A'
        cannot co-exist with the cell-associated internal_power group in
 line 120. (LBDB-411)
```

What Next

Refer to the *Library Compiler User Guide* for more information about power modeling. Change the library source file by using either the cell-associated style or pin-associated style internal_power on the specified pin.

LBDB-412

(error) There is a missing internal_power relation between\n \tpins '%s' and '%s' in the '%s' cell.

Description

This message indicates there is a missing internal_power relation from an input or inout pin to an output pin.

For a combinational cell, the Library Compiler checks that

```
* An output port with a function statement has internal_power relation
          to all functionally related inputs
```

Feedback

```
        * An output port with a three_state attribute has timing arcs
          to all three_state related inputs
```

However, Library Compiler will not check if internal_power information is completely missing in this output.

The following example shows an instance where this message occurs:

```
cell(AN2) {
    pin(A, B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
      internal_power () {
        power (power_2d_temp) {
            values ("1, 2, 3, 4", "5, 6, 7, 8", \
                    "9, 10, 11, 12", "13, 14, 15, 16");
        }
        related_pin : "A";
      }
      timing() {
        ...
      }
    }
  }
```

In this case, an internal_power group is missing between the pin 'Z' and 'B'. To fix the problem, add the following internal_power group:

```
internal_power () {
        power (power_2d_temp) {
            values ("1, 2, 3, 4", "5, 6, 7, 8", \
                    "9, 10, 11, 12", "13, 14, 15, 16");
        }
        related_pin : "B";
      }

The following is an example message:
Error: Line 12, There is a missing internal_power relation between
        pins 'B' and 'Z' in the 'AN2' cell. (LBDB-412)
```

What Next

Add the missing internal_power group between the two pins.

Feedback

LBDB-413

(error) There is an extra internal_power group between '%s' and\n \t'%s' pins in the '%s' cell.

Description

Internal_power groups are allowed for pins that are related to each other. To be related to each other, the input pin has to be in the *function* or *three_state* attribute of the output or input pin. This message is issued if the internal_power group identified between pins does not fall into the categories previously described.

The following example shows an instance where this message occurs:

```
pin(Z) {
      direction : output;
      function : "B";
      internal_power () {
        power (power_2d_temp) {
            values ("1, 2, 3, 4", "5, 6, 7, 8", \
                    "9, 10, 11, 12", "13, 14, 15, 16");
        }
        related_pin : "A B";
      }
      timing() {
        ...
      }
   }
```

In this case, you defined a internal_power group between the 'A' and 'Z pins, even though the 'A' pin is not functionally related to the 'Z' pin. Remove the internal_power group or change the function statement of 'Z' to include 'A'.

The following is an example message:

```
Warning: Line 73, There is an extra internal_power group between 'A' and
        'Z' pins in the 'AN2' cell. (LBDB-413)
```

What Next

Check your library to see whether you have generated the internal_power group by mistake, whether the related_pin field is wrong, or the function attribute value is not recognized.

LBDB-414

(error) In this internal_power group, the '%s' output pin in\n \tthe '%s' attribute is not functionally equivalent or opposite to the '%s' pin.

Feedback

Description

If an output is specified in the related_pin, related_bus_pins, or equal_or_opposite_output attributes, this output must be functionally equivalent or opposite of the output pin which owns the internal_power.

The following example shows an instance where this message occurs:

```
cell(AN2) {
    pin(A, B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
      internal_power () {
        power (power_3d_temp) {
                values ("1, 2, 3", "4, 5, 6", "7, 8, 9", \
                        "10, 11, 12", "13, 14, 15", "16, 17, 18"\
                        "19, 20, 21", "22, 23, 24", "25, 26, 27");
        }
        related_pin : "A B";
        equal_or_opposite_output : "Y";
      }
      timing() {
        ...
      }
    }
    pin(Y) {
      direction : output;
      function : "A + B";
      timing() {
        ...
      }
    }
  }
```

To fix the problem, remove equal_or_opposite_output attribute from the internal_power group and use 2-dimensional lookup table; or make sure 'Y' is functionally equivalent or opposite to 'Z'.

The following is an example message:

```
Error: Line 126, In this internal_power group, the 'Y' output pin in
        the 'equal_or_opposite_output' attribute is not functionally
 equivalent
        or opposite to the 'Z' pin. (LBDB-414)
```

Feedback

What Next

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

LBDB-415

(error) The '%s' attribute cannot be specified in this\n \tinternal_power group.

Description

This message indicates you specified an attribute outside its context.

```
(1) An internal_power group with 1-dimensional look-up tables cannot
 specify
    related_pin, related_bus_pins, or equal_or_opposite_output
 attributes.
(2) An internal_power group with 2-dimensional look-up tables cannot
 specify
    an equal_or_opposite_output attribute.
```

One exception is when the internal_power is an arc from a tri-state pin (that is related_pin is a tri-state pin), the checker is diabled.

The following example shows an instance where this message occurs:

```
internal_power() {
        power(power_1d_temp) {
                values ("1, 2, 3, 4");
        }
        related_pin : "A";
    }
```

In this case, the 'related_pin' attribute is not allowed in 1-dimensional lookup table. To fix the problem, remove the related_pin attribute from internal_power group.

The following is an example message:

```
Error: Line 69, The 'related_pin or related_bus_pins' attribute cannot be
        specified in this internal_power group. (LBDB-415)
```

What Next

Change the technology library source file to delete the specified attribute or move the attribute to its correct context.

LBDB-416

(error) The '%s' cell is missing cell_leakage_power attribute.

Feedback

Description

This message indicates there is one or more state-dependent leakage_power attribute, but no cell_leakage_power attribute specified as default value. When at least one state-dependent leakage power is specified in a cell, the cell must have also cell_leakage_power attribute defined.

The following example shows an instance where this message occurs:

```
cell(AN2) {
      leakage_power () {
        when : "A";
        value : 1.0;
      }
      ...
  }
```

In this case, a cell_leakage_power attribute is missing. To fix the problem, add the following attribute to the cell group:

```
cell_leakage_power : 0.5;

The following is an example message:
Error: Line 12, The 'AN2' cell is missing cell_leakage_power attribute.
 (LBDB-416)
```

What Next

Add the missing timing group between the two pins.

LBDB-417

(error) Pin '%s' has a timing arc that appears on only one of\n \tthe scaled cell (%s,%s) and the cell '%s'.

Description

Timing arcs with the same pin pair and type must match by number between the scaled cell and the regular cell.

The following example shows an instance where this message occurs:

```
library(alib) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
    }
    cell(AND) {
      area : 1;
```

Feedback

```
    pin(A B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      function : "A B";
      timing() {
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "A B";
      }
    }
  }

  scaled_cell(AND,WCCOM) {
    area : 1;
    pin(A) {
      direction : input;
      capacitance : 1;
    }
    pin(B) {
      direction : input;
      capacitance : 1;
      timing() {
        intrinsic_rise : 0.3;
        intrinsic_fall : 0.3;
        rise_resistance : 0.3;
        fall_resistance : 0.3;
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "A";
      }
    }
    pin(Z) {
      direction : output;
      function : "A B";
      timing() {
        intrinsic_rise : 0.3;
        intrinsic_fall : 0.3;
        rise_resistance : 0.3;
        fall_resistance : 0.3;
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "A B";
      }
    }
  }
}
```

In this case, The timing arc between 'B' and 'A' is defined only on the 'AND' scaled cell and not on the 'AND' scaled_cell. To fix the problem, remove one of the timing arcs.

The following is an example message:

```
Error: Ling 30, Pin 'A' has a timing arc that appears on only one of
        the scaled cell (AND,WCCM) and the cell 'AND'. (LBDB-417)
```

What Next

Find the timing group in the scaled_cell and remove the extra timing groups or add more timing groups in the parent cell.

LBDB-418

(warning) The cell_degradation constraint is missing\n \tin this timing group in cell '%s'.

Description

This message informs the user that Library Compiler finds the cell_degradation constraint being described in at least one, but not all, timing arcs of the cell. If the cell_degradation constraint is specified in a cell, all timing arcs of the following types should specify cell_degradation constraint: combinational rising_edge falling_edge clear preset three_state_enable However, the cell_degradation constraint should not be defined in timing groups of the following timing types: setup_rising setup_falling hold_rising hold_falling recovery_rising recovery_falling removal_rising removal_falling skew_rising skew_falling non_seq_setup_rising non_seq_setup_falling non_seq_hold_rising non_seq_hold_falling nochange_high_high nochange_high_low nochange_low_high nochange_low_low

The following example shows an instance where this message occurs:

```
cell (DFF) {
  pin (D) {
    direction : input;
    ...
    timing () {  /* no warning */
      timing_type : setup_rising;
      related_pin : CP;
      rise_constraint (constr) {
        ...
      }
      rise_constraint (constr) {
        ...
      }
    }
  }
  pin (CP) {
    direction : input;
    ...
```

Feedback

```
  }
  pin (Q) {
    direction : output;
    timing () {  /* cell_degradation is defined */
      related_pin : CP;
      timing_type : rising_edge;
      cell_degradation (celldeg) {
        ...
      }
      cell_rise (delay) {
        ...
      }
      cell_fall (delay) {
        ...
      }
      ...
    }
    ...
  }
  pin (QN) {
    direction : output;
    timing () {  /* cell_degradation is NOT defined  --- LIBG-206 --- */
      related_pin : CP;
      timing_type : rising_edge;
      cell_rise (delay) {
        ...
      }
      cell_fall (delay) {
        ...
      }
      ...
    }
    ...
  }
  ...

}
```

In this case, the warning message will be issued on CP-to-QN timing arc.

The following is an example message:

```
Warning: Line 202, The cell_degradation constraint is missing
         in this timing group in cell 'DFF'. (LBDB-418)
```

What Next

Do either one of the following modification to the cell description: (1) Remove all cell_degradation constraints specified in the cell. (2) Make sure all delay arcs of the above timing types specify cell_degradation constraints.

Feedback

LBDB-419

(warning) Found the obsolete and unsupported 'state' group in the'%s' cell;\n \tplease use 'ff' group or 'latch' group or 'statetable' instead.

Description

The *state* group is not supported after v3.0. Instead, the sequential function should now be described in *ff* or *latch* group or *statetable*.

The following is an example message:

```
Warning: Line 159, Found the obsolete and unsupported 'state' group in
 the 'lbdbl419' cell;
        please use 'ff' group or 'latch' group or 'statetable' instead.
 (LBDB-419)
```

What Next

If you have access to the technology library source file change the *state* group to *ff* or *latch* group. Otherwise contact the vendor and inform them about the problem.

LBDB-420

(error) The index number '%d' must be less than\n \tthe address width '%d'.

Description

This message indicates an index in the column_address or row_address attribute is greater than the address_width value.

The following example shows an instance where this message occurs:

```
memory() { /* Indicate this is a memory cell */
        type : ram;
        address_width : 4;
        word_width : 2;
        column_address : "0 6 "; /* index 6 > addr_width 4 */
      }
```

The following is an example message:

```
Error: Line 127, The index number '6' must be less than
        the address width '4'.  (LBDB-420)
```

What Next

Correct the index in the technology library.

Feedback

LBDB-421

(error) The column or row address width '%d' must be less than\n \tor equal to the address width '%d'.

Description

This message indicates the width of the column_address or row_address attribute is greater than the address_width value.

The following example shows an instance where this message occurs:

```
memory() { /* Indicate this is a memory cell */
        type : ram;
        address_width : 4;
        word_width : 2;
        column_address : "0:4 "; /* col width 5 > addr_width 4 */
      }
```

The following is an example message:

```
Error: Line 127, The column/row address width '5' must be less than or
        equal to the address width '4'.  (LBDB-421)
```

What Next

Reduce the number of indices in the column_address or row_address or correct the address_width value in the technology library.

LBDB-423

(error) Address pins are not all used by column_address and row_address attributes.

Description

This message indicates not all indices in the column_address and row_address attributes are used.

The following example shows an instance where this message occurs:

```
memory() { /* Indicate this is a memory cell */
        type : ram;
        address_width : 4;
        word_width : 2;
        column_address : "0 1";
        row_address : "3";              /* missing the index 2 */
      }
```

Feedback

The following is an example message:

```
Error: Line 122, Address pins are not all used by column_address and
 row_address attributes. (LBDB-423)
```

What Next

Correct the index in the technology library.

LBDB-424

(warning) The number of address pins that overlap between column and row is '%d'.

Description

This message indicates that there are overlapping indices in the column_address and row_address attributes.

The following example shows an instance where this message occurs:

```
memory() { /* Indicate this is a memory cell */
        type : ram;
        address_width : 4;
        word_width : 2;
        column_address : "0:2";
        row_address : "2:3";            /* the index 2 is overlapping */
      }
```

The following is an example message:

```
Warning: Line 122, The number of address pins that overlap between column
 and row is 1. (LBDB-424)
```

What Next

Correct the index overlapping in the technology library.

LBDB-425

(warning) Removing duplicate indices in the attribute.

Description

This message indicates an index in the column_address or row_address attribute is duplicated.

The following example shows an instance where this message occurs:

```
memory() { /* Indicate this is a memory cell */
        type : ram;
        address_width : 4;
```

Feedback

```
        word_width : 2;
        column_address : "0 3 3";
      }
```

The following is an example message:

```
Warning: Line 126, Removing duplicate indices in the attribute.
 (LBDB-425)
```

What Next

Correct the index in the technology library.

LBDB-426

(error) The '%s' is missing for this inout pin.

Description

Both input_signal_level and the output_signal_level values are required in an inout pin.

The following example shows an instance where this message occurs:

```
pin ( BIDIR )    {
      direction : inout;
      input_signal_level : VDD1;
      }
    }
```

To fix the problem, add the attribute to the pin group,

```
output_signal_level : VDD2;
```

The following is an example message:

```
Error: Line 104, The 'output_signal_level' is missing for this inout pin.
 (LBDB-426)
```

What Next

Check the library source file to see if you missed the input_signal_level or the output_signal_level attributes. Otherwise, change the direction of the pin to input or output.

LBDB-426w

(warning) The '%s' is missing for this inout pin.

Description

Both input_signal_level and the output_signal_level values are required in an inout pin.

Feedback

The following example shows an instance where this message occurs:

```
pin ( BIDIR )    {
      direction : inout;
      input_signal_level : VDD1;
      }
    }
```

To fix the problem, add the attribute to the pin group,

```
output_signal_level : VDD2;
```

The following is an example message:

```
Warning: Line 104, The 'output_signal_level' is missing for this inout
 pin. (LBDB-426w)
```

What Next

Check the library source file to see if you missed the input_signal_level or the output_signal_level attributes. Otherwise, change the direction of the pin to input or output.

LBDB-427

(error) All power supplies defined in the power_supply group\n \tmust exist in this operating_conditions group.

Description

This message indicates that one or more power_rail attributes are missing in an operating_conditions group even though they were defined in the power_supply group.

The following example shows an instance where this message occurs:

```
power_supply() {
        default_power_rail : VDD0;
        power_rail(VDD1, 5.0);
        power_rail(VDD2, 3.3);
    }


    operating_conditions(MPSS) {
        process : 1.5 ;
        temperature : 70 ;
        voltage : 4.75 ;
        tree_type : "worst_case_tree" ;
        power_rail(VDD2, 2.9);
    }
```

To fix the problem, add the attribute to the operating_conditions group,

```
power_rail(VDD1, 4.9);
```

Feedback

The following is an example message:

```
Error: Line 14, All power supplies defined in the power_supply group
        must exist in this operating_conditions group. (LBDB-427)
```

What Next

Check the library source file to see if you missed a power_rail attribute and correct it.

LBDB-428

(error) All the pins in the '%s' cell with multiple power supplies\n \tmust have signal level attributes.

Description

Either the input_signal_level or the output_signal_level attribute is missing in a pin within a multiple power supply cell.

The following example shows an instance where this message occurs:

```
power_supply() {
        default_power_rail : VDD0;
        power_rail(VDD1, 5.0);
        power_rail(VDD2, 3.3);
    }

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  rail_connection(PV1, VDD1);
  rail_connection(PV2, VDD2);
  pin(A) {
    direction : input;          /* missing input_signal_level attribute
 */
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A";
    output_signal_level : VDD2;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
```

Feedback

```
}
}
```

To fix the problem, add the attribute to the 'A' pin group,

```
input_signal_level : VDD1;
```

The following is an example message:

```
Error: Line 96, All the pins in the 'lbdb428' cell with multiple power
 supplies
       must have signal level attributes. (LBDB-428)
```

What Next

Check the library source file to see if you missed the input_signal_level or the output_signal_level attributes.

LBDB-429

(warning) The timing arc from '%s' to '%s' is dormant.

Description

A timing arc from an input pin to an output pin is dormant if the signal change on the input pin can never cause the change on the output without simultaneous changes on any other input pins.

The following example shows an instance where this message occurs:

```
cell(a_cell) {
    pin(y) {
      function : "!a b"
      three_state : "!a !b | a b"
      timing() {
        related_pin : a;
      }
    }
  }
```

In this example, if only pin 'a' is changed, pin 'y' will not have the signal transitions between '0' and '1'. The combinational timing arc between 'a' and 'y' is dormant.

The following is an example message:

```
Warning: Line 50000, The timing arc from 'a' to 'y' is dormant.
 (LBDB-429)
```

Feedback

What Next

This is caused by the input sharing between 'function', 'three_state', and 'x_function'. The signal transition is not physically possible and generally the timing arc should not be specified.

LBDB-430

(error) The '%s' rail_connection in a cell with multiple power\n \tsupplies is missing an internal_power table.

Description

This error message indicates that an output pin, regardless of the output_signal_level value, is missing an internal_power table for designated rail_connection.

The following example shows an instance where this message occurs:

```
power_supply() {
        default_power_rail : VDD0;
        power_rail(VDD1, 5.0);
        power_rail(VDD2, 3.3);
    }

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  rail_connection(PV1, VDD1);
  rail_connection(PV2, VDD2);
  pin(A) {
    direction : input;
    capacitance : 1;
    input_signal_level : VDD1;
    internal_power () {
      power_level : VDD1;
      power(power_out1_d) {
        values (" 0.693418, 0.691911, 0.689730, 0.691771, 0.695229,
 0.696524");
      }
    }
  }
  pin(Z) {
    direction : output;
    function : "A";
    output_signal_level : VDD2;
    internal_power () {
      power_level : VDD2;
      power(power_out1_d) {
        values (" 0.693418, 0.691911, 0.689730, 0.691771, 0.695229,
 0.696524");
      }
```

Feedback

```
    }
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}
```

To fix the problem, add the internal_power to the 'Z' pin.

```
internal_power () {
      power_level : VDD1;
      power(power_out1_d) {
        values (" 0.693418, 0.691911, 0.689730, 0.691771, 0.695229,
 0.696524");
      }
    }
```

The following is an example message:

```
Error: Line 96,  The 'VDD1' rail_connection in a cell with multiple power
        supplies is missing an internal_power table. (LBDB-430)
```

What Next

Check the library source file to see if you missed the power_level attribute or there is a typo in the name of the power_supply.

LBDB-431

(error) The value for attribute '%s' is empty.

Description

This error message indicates that an value field is null or empty.

The following example shows an instance where this message occurs:

```
cell(GND_G_A) {
  area             : 1 ;
  cell_footprint   : GND_G ;
  dont_touch       : true ;
  dont_use         : true ;
  cell_leakage_power : 0.00;

  pin(PAD) {
```

Feedback

```
    direction             : output ;
    function              : "0" ;
    capacitance           : 0.000000 ;

    max_capacitance       : 999.989990 ;
  }

  internal_power(POWER_IO_A) {
    values ("0.00000  ,0.00000  ",\
           "0.00000  ,0.00000  ");
    related_inputs  : "";
    related_outputs : "PAD";
  }
}
```

To fix the problem, fill up value for related_inputs or remove related_inputs.

```
internal_power () {
      values ("0.00000  ,0.00000  ",\
           "0.00000  ,0.00000  ");
        related_inputs  : "";
        related_outputs : "PAD";
      }
```

The following is an example message:

```
Error: Line 722,  The value for attribute 'related_outputs' is
        empty. (LBDB-431)
```

What Next

Check the library source file to see if you missed giving the value. If so, fill it up with appropriate value.

LBDB-432

(error) The non-Zero %d scalar value is not allowed in internal_power\n \tgroup within a cell group.

Description

This error message indicates that a non zero scalar value was defined in an internal_power group within a cell group.

The following example shows an instance where this message occurs:

```
cell(LBDB-432) {
  area             : 1 ;

  internal_power(scalar) {
        values("2.0");
        related_input : "";
```

Feedback

```
  }

   ....
}
```

To fix the problem, change the values to zero or move the internal_power to a pin group.

```
internal_power (scalar) {
      values ("0.00000");
        related_input  : "";
      }
```

The following is an example message:

```
Error: Line 174, The non-Zero 2.0 scalar value is not allowed in
 internal_power
        group within a cell group. (LBDB-432)
```

What Next

Check the library source file to see if it was a typo. If so, change the value to zero for no power consumption or move the internal power to a pin group.

LBDB-433

(error) The '%s' integrated gated clock cell has a '%s' pin with\n \ta combinational timing arc containing the '%s' timing_type.

Description

This message indicates that you specified one of the cell's timing arcs as combinational, which should be sequential. While the function of this cell is integrated clock gated cell, the timing arc on the clock gate enable pin from the clock gate clock pin should be sequential timing type setup, hold or nochnage.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "none_posedge";
  dont_use : true;
  pin(EN) {
    direction : input;
    capacitance : 0.017997;
    clock_gate_enable_pin : true;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
```

Feedback

```
      slope_fall : 0.0;
      related_pin : "EN";
    }
    timing() {
      intrinsic_rise : 0.22;
      intrinsic_fall : 0.22;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 0.031419;
    clock_gate_clock_pin : true;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    function : "CP + EN'";
    max_capacitance : 0.500;
    clock_gate_out_pin : true;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "EN";
    }
    timing() {
      intrinsic_rise : 0.22;
      intrinsic_fall : 0.22;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "CP";
    }
    internal_power (){
      rise_power(li4X3){
        index_1("0.0150, 0.0400, 0.1050, 0.3550");
        index_2("0.050, 0.451, 1.501");
        values("0.141, 0.148, 0.256",\
        "0.162, 0.145, 0.234",\
        "0.192, 0.200, 0.284",\
        "0.199, 0.219, 0.297");
      }
      fall_power(li4X3){
        index_1("0.0150, 0.0400, 0.1050, 0.3550");
```

Feedback

```
        index_2("0.050, 0.451, 1.500");
        values("0.117, 0.144, 0.246",\
        "0.133, 0.151, 0.238",\
        "0.151, 0.186, 0.279",\
        "0.160, 0.190, 0.217");
      }
      related_pin : "CP EN" ;
    }
  }
}
```

The following is an example message:

```
Error: Line 206, The 'CGNP' integrated gated clock cell has a 'EN' pin
 with
        a combinational timing arc containing the 'combinational'
 timing_type. (LBDB-433)
```

What Next

Change the library source file, and fix the timing_type of the specified pin.

LBDB-434

(error) The '%s' integrated gated clock cell has a '%s' pin with\n \ta sequential timing arc containing the '%s' timing_type.

Description

This message indicates that you specified one of the cell's timing arcs as sequential, which should be combinational. While the function of this cell is integrated clock gated cell, the timing arc on the clock gate output pin from the clock gate clock/enable/test pin should be combinational timing type.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "none_posedge";
  dont_use : true;
  pin(EN) {
    direction : input;
    capacitance : 0.017997;
    clock_gate_enable_pin : true;
    timing() {
      timing_type : nochange_high_low;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
    timing() {
```

Feedback

```
      timing_type : nochange_low_low;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 0.031419;
    clock_gate_clock_pin : true;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    function : "CP + EN'";
    max_capacitance : 0.500;
    clock_gate_out_pin : true;
    timing() {
      timing_type : nochange_high_low;
      intrinsic_rise : 0.4;
      intrinsic_fall : 0.4;
      related_pin : "CP";
    }
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "EN";
    }
    timing() {
      intrinsic_rise : 0.22;
      intrinsic_fall : 0.22;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "CP";
    }
    internal_power (){
      rise_power(li4X3){
        index_1("0.0150, 0.0400, 0.1050, 0.3550");
        index_2("0.050, 0.451, 1.501");
        values("0.141, 0.148, 0.256",\
        "0.162, 0.145, 0.234",\
        "0.192, 0.200, 0.284",\
        "0.199, 0.219, 0.297");
      }
      fall_power(li4X3){
        index_1("0.0150, 0.0400, 0.1050, 0.3550");
        index_2("0.050, 0.451, 1.500");
```

Feedback

```
        values("0.117, 0.144, 0.246",\
        "0.133, 0.151, 0.238",\
        "0.151, 0.186, 0.279",\
        "0.160, 0.190, 0.217");
      }
      related_pin : "CP EN" ;
    }
  }
}
```

The following is an example message:

```
Error: Line 206, The 'CGNP' integrated gated clock cell has a 'Z' pin
 with
        a sequential timing arc containing the 'nochange_high_low'
 timing_type. (LBDB-434)
```

What Next

Change the library source file, and fix the timing_type of the specified pin.

LBDB-435

(error) The '%s' integrated gated clock cell has a '%s' pin without\n \tspecified timing arcs.

Description

This message indicates that you specified one of the cell's pin without timing arcs, while the function of this cell is integrated clock gated cell.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "none_posedge";
  dont_use : true;
  pin(EN) {
    direction : input;
    capacitance : 0.017997;
    clock_gate_enable_pin : true;
  }
  pin(CP) {
    direction : input;
    capacitance : 0.031419;
    clock_gate_clock_pin : true;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    function : "CP + EN'";
    max_capacitance : 0.500;
    clock_gate_out_pin : true;
```

Feedback

```
      timing() {
        timing_type : nochange_high_low;
        intrinsic_rise : 0.4;
        intrinsic_fall : 0.4;
        related_pin : "CP";
      }
      timing() {
        timing_type : nochange_low_low;
        intrinsic_rise : 0.4;
        intrinsic_fall : 0.4;
        related_pin : "CP";
      }
      timing() {
        intrinsic_rise : 0.48;
        intrinsic_fall : 0.77;
        rise_resistance : 0.1443;
        fall_resistance : 0.0523;
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "EN";
      }
      timing() {
        intrinsic_rise : 0.22;
        intrinsic_fall : 0.22;
        rise_resistance : 0.1443;
        fall_resistance : 0.0523;
        slope_rise : 0.0;
        slope_fall : 0.0;
        related_pin : "CP";
      }
      internal_power (){
        rise_power(li4X3){
          index_1("0.0150, 0.0400, 0.1050, 0.3550");
          index_2("0.050, 0.451, 1.501");
          values("0.141, 0.148, 0.256",\
          "0.162, 0.145, 0.234",\
          "0.192, 0.200, 0.284",\
          "0.199, 0.219, 0.297");
        }
        fall_power(li4X3){
          index_1("0.0150, 0.0400, 0.1050, 0.3550");
          index_2("0.050, 0.451, 1.500");
          values("0.117, 0.144, 0.246",\
          "0.133, 0.151, 0.238",\
          "0.151, 0.186, 0.279",\
          "0.160, 0.190, 0.217");
        }
        related_pin : "CP EN" ;
      }
    }
  }
```

Feedback

The following is an example message:

```
Error: Line 206, The 'CGNP' integrated gated clock cell has a 'Z' pin
 without
        specified timing arcs. (LBDB-435)
```

What Next

Change the library source file, and add the missing timing arc of the specified pin.

LBDB-436

(error) Illegal timing_model_type value '%s'.

Description

Currently the timing_model_type attribute can only take the value "stamp".

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  timing_type_model : stml;
  ...
}
```

The following is an example message:

```
Error: Line 206, Illegal timing_model_type value 'stml'. (LBDB-436)
```

What Next

Change or delete the attribute.

LBDB-437

(warning) The generated_clock(%s) group is defined \n \tmultiple times.

Description

This message indicates that you specified the same generated_clock group multiple times. Only the last one is retained.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;

  generated_clock(clock_A) {
    ...
  }
```

```
  generated_clock(clock_A) {
    ...
  }
  ...
}
```

The following is an example message:

```
Warning: Line 206, The generated_clock(clock_A) group is defined
        multiple times. (LBDB-437)
```

What Next

Change the group name, or delete the duplicated group.

LBDB-438

(error) The master pin is not specified in the generated_clock\n \tgroup.

Description

The master_pin attribute must be specified for a generated clock.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    clock_pin : CK;
    divided_by : 2;
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The master pin is not specified in the generated_clock
        group. (LBDB-438)
```

What Next

Add the master_pin attribute.

LBDB-439

(error) The clock pin is not specified in the generated_clock\n \tgroup.

Description

The clock_pin attribute must be specified for a generated clock.

Feedback

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    master_pin : CK;
    divided_by : 2;
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The clock pin is not specified in the generated_clock
        group. (LBDB-439)
```

What Next

Add the clock_pin attribute.

LBDB-440

(error) The generated_clock divisor is less than 1.

Description

The divisor in the generated_clock group must be an integer greater than or equal to 1.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    clock_pin : CLK1;
    master_pin : CLK;
    divided_by : 0;
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The generated_clock divisor is less than 1. (LBDB-440)
```

What Next

Change the divisor value.

LBDB-441

(error) The generated_clock multiplier is less than 1.

Feedback

Description

The multiplier in the generated_clock group must be an integer greater than or equal to 1.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    clock_pin : CLK1;
    master_pin : CLK;
    multiplied_by : 0;
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The generated_clock multiplier is less than 1.
 (LBDB-441)
```

What Next

Change the multiplier value.

LBDB-442

(error) The generated_clock edge is less than 0.

Description

The edge1, edge2, and edge3 parameter in the edges complex attribute in the generated_clock group must be non-negative integers.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  generated_clock(clockA) {
    clock_pin : CLK1;
    master_pin : CLK;
    edges(-1, 2, 3);
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The generated_clock edge is less than 0. (LBDB-442)
```

Feedback

What Next

Change the violating edge value.

LBDB-443

(warning) The mode_definition(%s) group is defined\n \tmultiple times.

Description

This message indicates that you specified the same mode_definition group multiple times. Only the last one is retained.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;

  mode_definition(rw) {
    ...
  }
  mode_definition(rw) {
    ...
  }
  ...
}
```

The following is an example message:

```
Warning: Line 206, The mode_definition(rw) group is defined
        multiple times. (LBDB-443)
```

What Next

Change the group name, or delete the duplicated group.

LBDB-444

(error) The mode definition '%s' has no values defined.

Description

A mode_definition group must have at least one mode value defined.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  mode_definition(read) {
  }
```

Feedback

```
  ...
}
```

The following is an example message:

```
Error: Line 206, The mode definition 'read' has no values defined.
 (LBDB-444)
```

What Next

Define the mode values.

LBDB-445

(warning) The mode_value(%s) group is defined\n \tmultiple times.

Description

This message indicates that you specified the same mode_value group multiple times. Only the last one is retained.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;

  mode_definition(rw) {
    mode_value(read) {
      when : R;
      sdf_cond : "R == 1";
    }
    mode_value(read) {
      when : !R;
      sdf_cond : "R == 0";
    }
  }
}
```

The following is an example message:

```
Warning: Line 206, The mode_value(read) group is defined
        multiple times. (LBDB-445)
```

What Next

Change the group name, or delete the duplicated group.

LBDB-446

(error) The sdf_cond attribute is not specified for the\n \tmode condition.

Feedback

Description

This message indicates that you specified the when condition for the mode value, but did not specify the sdf_cond attribute.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  mode_difinition(rw) {
    mode_value(read) {
      when : R;
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The sdf_cond attribute is not specified for the
        mode condition. (LBDB-446)
```

What Next

Add the missing sdf_cond attribute.

LBDB-447

(information) The %s is defined multiple times for %s. All of them are kept.

Description

This message indicates that you specified multiple attribute or group information. All of the attributes or group information are kept in db.

What Next

Please make sure that it is your real intention to have multiple attribute or group information.

EXMAPLES

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;

  pin (y) {
    timing() {
      mode(rw, read);
      mode(rw, write);
    }
```

Feedback

```
  }
}
```

Examples

```
Information: Line 206, The mode is defined multiple times for timing. All
 of them are kept (LBDB-447)
```

LBDB-448

(error) The Boolean condition overlaps with the condition\n \tspecified at line %d.

Description

The two Boolean conditions must be mutually exclusive.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      when : R;
      sdf_cond : "R == 1";
    }
    mode_value(write) {
      when : R;
      sdf_cond : "R == 1";
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The Boolean condition overlaps with the condition
        specified at line 202. (LBDB-448)
```

What Next

Check the conditions and make them mutually exclusive.

LBDB-449

(error) The mode instance mode(%s, %s) is invalid.

Description

The mohe instance delaration must be referring to a mode_definition and one of its mode_value

Feedback

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      ...
    }
    mode_value(werite) {
      ...
    }
  }
  pin (y) {
    timing () {
      mode(rw, latching);
      ...
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The mode instance mode(rw, latching) is invalid.
 (LBDB-449)
```

What Next

Check for consistency between mode group and mode value definitions, and mode instance declarations.

LBDB-450

(error) Mismatched quotes in the sdf_cond string.

Description

In the sdf_cond string, a double quoting is mismatched.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      when : R;
      sdf_cond : "R == 1 && C ==
    }
  }
  ...
}
```

Feedback

The following is an example message:

```
Error: Line 206, Mismatched quotes in the sdf_cond string. (LBDB-450)
```

What Next

Add the missing quote or delete the extra quote.

LBDB-451

(error) Undefined variable '%s'.

Description

The variable in the sdf_cond string must be a port or bus name.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      when : R;
      sdf_cond : "read == 1";
    }
  }
  pin (R) {
    ...
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, Undefined variable 'read'. (LBDB-451)
```

What Next

Eliminate undefined varibable.

LBDB-452

(error) Fewer than two ports are specified in the\n \tshort list.

Description

A short complex attribute must have more than one parameter.

The following example shows an instance where this message occurs:

```
cell (c) {
  ...
```

Feedback

```
  short(A);
  pin (A) {...}
  pin (Y) {...}
}
```

The following is an example message:

```
Error: Line 206, Fewer than two ports are specified in the
        short list. (LBDB-452)
```

What Next

Add the missing port names.

LBDB-453

(error) The parameter '%s' in the short list is not a\n \tport or bus name.

Description

The short complex attribute must take port or bus name as parameters.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  short(R, T);

  pin(R) {...}
  ...
}
```

The following is an example message:

```
Error: Line 206, The parameter 'T' in the short list is not a
        port or bus name. (LBDB-453)
```

What Next

Eliminate undefined varibable.

LBDB-454

(error) Unequal bus widths in the short list. \tspecified timing arcs.

Description

All members of a short list must be of the same width. That is, they must all be simple ports, or all be buses of the same width.

Feedback

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  short(A, B);
  bus(A) {
    bus_type : bus4;
  }
  bus(B) {
    bus_tyep : bus8;
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, Unequal bus widths in the short list. (LBDB-454)
```

What Next

Use the same width members.

LBDB-455

(error) Multiple drive arcs are defined on port %s.

Description

A port can have at most one drive arc defined.

The following example shows an instance where this message occurs:

```
pin(Y) {
  timing () {
    drive_arc : true;
    ...
  }
  timing () {
    drive_arc : true;
    ...
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, Multiple drive arcs are defined on port Y. (LBDB-455)
```

What Next

Eliminate the extra ones.

Feedback

LBDB-456

(error) The drive arc is not combinational.

Description

Drive arc must be combinational.

The following example shows an instance where this message occurs:

```
pin(Z) {
    direction : output;
    timing() {
        timing_type : nochange_high_low;
        drive_arc : true;
        ...
    }
    ...
}
```

The following is an example message:

```
Error: Line 206, The drive arc is not combinational. (LBDB-456)
```

What Next

Change the drive arc to combinational or delete it.

LBDB-457

(error) Related pin is found on the drive arc.

Description

Drive arc cannot have related pins.

The following example shows an instance where this message occurs:

```
pin(Z) {
    direction : output;
    timing() {
        timing_type : nochange_high_low;
        drive_arc : true;
        related_pin : A;
        ...
    }
    ...
}
```

The following is an example message:

```
Error: Line 206, Related pin is found on the drive arc. (LBDB-457)
```

Feedback

What Next

Remove the related_pin attribute or unlabel the timing arc.

LBDB-458

(error) Cell rise or fall table is missing on the\n \tdrive arc.

Description

Drive arc requires cell rise and fall tables.

The following example shows an instance where this message occurs:

```
pin(Z) {
    direction : output;
    timing() {
        timing_type : nochange_high_low;
        drive_arc : true;
        cell_rise(table1) {
          ...
        }
    }
    ...
}
```

The following is an example message:

```
Error: Line 206, Cell rise or fall table is missing on the
        drive arc. (LBDB-458)
```

What Next

Add the missing tables.

LBDB-459

(error) The drive arc has tables that are not 1-D function\n \tof total_output_capacitance.

Description

Drive arc requires delay tables to be 1-D function of total output capacitance.

The following example shows an instance where this message occurs:

```
pin(Z) {
    direction : output;
    timing() {
        timing_type : nochange_high_low;
        drive_arc : true;
        cell_rise(table2D) {
```

```
            values("0.1, 0.2", "0.5, 0.8");
          }
      }
      ...
}
```

The following is an example message:

```
Error: Line 206, The drive rc has tables that are not 1-D function
        of total_output_capacitance. (LBDB-459)
```

What Next

Add the missing tables.

LBDB-460

(error) Multiple tlatch groups are defined on\n \tpin '%s'.

Description

This message indicates that you specified multiple tlatch groups on a pin.

The following example shows an instance where this message occurs:

```
pin(D) {

  tlatch(EN) {
    ...
  }
  tlatch(E) {
    ...
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, Muliple tlatch groups are defined on
        pin 'D'.  (LBDB-460)
```

What Next

Delete the duplicated group.

LBDB-461

(error) The edge type is not specified for the tlatch.

Feedback

Description

A tlatch group must have the edge_type attribute specified.

The following example shows an instance where this message occurs:

```
pin(D) {

  tlatch(EN) {
    tdisable : TRUE;
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The edge tyep is not specified for the tlatch.
 (LBDB-461)
```

What Next

Add the missing attribute.

LBDB-462

(error) Pin '%s' referred to in tlatch does not exist.

Description

The tlatch group name must be the name of an existing enable pin.

The following example shows an instance where this message occurs:

```
cell (c) {
  pin(D) {
    tlatch(EN) {
      edge_type : rising;
    }
  }
  ...
  /* No such pin as EN */
}
```

The following is an example message:

```
Error: Line 206, Pin 'EN' referred to in tlatch does not exist.
 (LBDB-462)
```

What Next

Add the missing attribute.

Feedback

LBDB-463

(warning) The related pin '%s' for the non-sequential\n \tsetup/hold timing check is labeled a clock.

Description

If the related pin for the non-sequential constraint arc is labeled a clock, then timing analysis will not propagate a clock signal through the cell.

The following example shows an instance where this message occurs:

```
cell (c) {
  pin(D) {
    timing() {
      timing_type : non_seq_setup_falling;
      related_pin : OSC;
      ...
    }
  }
  pin(OSC) {
    clock : true;
    ...
  }
}
```

The following is an example message:

```
Warning: Line 206, The related pin 'OSC' for the non-sequential
        setup/hold timing check is labeled a clock. (LBDB-463)
```

What Next

Delete the "clock : true;" declaration in the pin group.

LBDB-464

(error) The '%s' cell is a non-pad cell with x_function,\n \twhich is not supported by Library Compiler.

Description

Library Compiler only supports x_function on pad cells. Library Compiler issues this error message if a non-pad cell defines x_function on one or more ports.

The following example shows an instance where this message occurs:

```
cell (lbdb464) {
    area    :   0.0;
    pin (D, CLK)    {
      direction   :   input;
```

Feedback

```
      capacitance :   1.0;
      fanout_load :   1.0;
    }
    pin(Q){
      direction   :   output;
      function : "IQ";
      x_function : CLK';
      timing () {
        timing_type : rising_edge;
        intrinsic_rise   : 1.0;
        rise_resistance  : 0.1;
        intrinsic_fall   : 1.0;
        fall_resistance  : 0.1;
        related_pin      : "CLK";
      }
    }
    ff (IQ, IQN) {
      next_state : D;
      clocked_on : CLK;
    }
  }
```

The following is an example message:

```
Error: Line 6, The 'lbdb464' cell is a non-pad cell with x_function,
 which is not supported by Library Compiler.(LBDB-464)
```

What Next

Remove the x_function attribute defined for any output pin of the cell.

LBDB-465

(error) The '%s' attribute is missing\n \tfrom the electromigration group.

Description

The *related_pin* or *related_bus_pins* attribute is required in an electromigration group with a two-dimensional lookup table.

The following example shows an instance where this message occurs:

```
electromigration() {
        em_max_toggle_rate(em_2d) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
    }
```

To fix the problem, add the following line into the electromigration group:

```
related_pin : "A";
```

The following is an example message:

```
Error: Line 126, The 'related_pin or related_bus_pins' attribute is
 missing
        from the electromigration group. (LBDB-465)
```

What Next

Change the library source file by specifying the *related_pin* or the *related_bus_pins* attribute in the electromigration group as needed.

LBDB-466

(error) The '%s' attribute cannot be\n \tspecified in this electromigration group.

Description

This message indicates that you specified an attribute outside its context. An electromigration group with one-dimensional lookup tables cannot specify *related_pin* or *related_bus_pins* attributes.

The following example shows an instance where this message occurs:

```
electromigration() {
        em_max_toggle_rate(em_1d_temp) {
                values ("1, 2, 3, 4");
        }
        related_pin : "A";
    }
```

In this case, the *related_pin* attribute is not allowed in the one-dimensional lookup table. To fix the problem, remove the *related_pin* attribute from the electromigration group.

The following is an example message:

```
Error: Line 69, The 'related_pin or related_bus_pins' attribute cannot be
        specified in this electromigration group. (LBDB-466)
```

What Next

Change the technology library source file to delete the specified attribute or move the attribute to its correct context.

LBDB-467

(error) The '%s' lookup table in the input-associated\n \telectromigration group cannot use '%s' as its template.

Feedback

Description

The em_max_toggle_rate lookup table in an input-associated electromigration group must use a one-dimensional template with *input_transition_time* as its variable.

The following example shows an instance where this message occurs:

```
em_lut_template(ok_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  em_lut_template(err_temp) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }

        em_max_toggle_rate(err_temp) {
                values ("1, 2, 3, 4");
        }
```

To fix the problem, change the template value of the *em_max_toggle_rate* attribute from *err_temp* to *ok_temp*.

The following is an example message:

```
Error: Line 126, The 'em_max_toggle_rate' lookup table in the
 input-associated
       electromigration group cannot use 'err_temp' as its template.
 (LBDB-467)
```

What Next

For more information about lookup tables, see the *Library Compiler User Guide*. Change the library source file by referencing a different template in the lookup table description.

LBDB-468

(error) The one-dimensional '%s' lookup table in the\n \tinout-associated electromigration group cannot use '%s' as its template.

Description

The one-dimensional em_max_toggle_rate lookup table in an inout-associated electromigration group must use a template with *input_transition_time* or *total_output_net_capacitance* as its variable.

The following example shows an instance where this message occurs:

```
em_lut_template(ok_template) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
```

Feedback

```
  }
  em_lut_template(ok2_template) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }
  em_lut_template(err_template) {
    variable_1 : output_net_length;
    index_1("0, 1, 2, 3");
  }

        em_max_toggle_rate(err_template) {
                values ("1, 2, 3, 4");
        }
```

To fix the problem, change the template value of the *em_max_toggle_rate* attribute from err_template to ok_template or ok2_template.

The following is an example message:

```
Error: Line 126, The 1-dimensional 'em_max_toggle_rate' lookup table in
 the
        inout-associated electromigration group cannot use
        'err_template' as its template. (LBDB-468)
```

What Next

For more information about lookup tables, see the *Library Compiler User Guide*. Change the library source file by referencing a different template in the lookup table description.

LBDB-469

(error) The one-dimensional '%s' lookup table in the\n \t%s-associated electromigration group cannot use '%s' as its template.

Description

The one-dimensional em_max_toggle_rate lookup table in an output-associated electromigration group must use a template with *total_output_net_capacitance* as its variable.

The following example shows an instance where this message occurs:

```
em_lut_template(err_template) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }
  em_lut_template(ok_template) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
  }
```

Feedback

```
        em_max_toggle_rate(err_template) {
                values ("1, 2, 3, 4");
        }
```

To fix the problem, change the template value of the *em_max_toggle_rate* attribute from *err_template* to *ok_template*.

The following is an example message:

```
Error: Line 126, The 1-dimensional 'em_max_toggle_rate' lookup table in
 the
        output-associated electromigration group cannot use
 'err_template' as its template. (LBDB-469)
```

What Next

For more information about lookup tables, see the *Library Compiler User Guide*. Change the library source file by referencing a different template in the lookup table description.

LBDB-470

(error) The two-dimensional '%s' lookup table in the\n \t%s-associated electromigration group cannot use '%s' as its template.

Description

The two-dimensional em_max_toggle_rate lookup table in an output-associated electromigration group must use a template with *input_transition_time* and *total_output_net_capacitance* as its variables.

The following example shows an instance where this message occurs:

```
em_lut_template(ok_template) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
    variable_2 : total_output_net_capacitance;
    index_2("0, 1, 2, 3");
  }
  em_lut_template(err_template) {
    variable_1 : total_output_net_capacitance;
    index_1("0, 1, 2, 3");
    variable_2 : constrained_pin_transition;
    index_2("0, 1, 2, 3");
  }

        em_max_toggle_rate(err_template) {
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
```

To fix the problem, change the template value of the *em_max_toggle_rate* attribute from err_template to ok_template.

The following is an example message:

```
Error: Line 126, The 2-dimensional 'em_max_toggle_rate' lookup table in
 the
        output-associated electromigration group cannot use
 'err_template' as its template. (LBDB-470)
```

What Next

Refer to the *Library Compiler User Guide* for more information about lookup tables. Change the library source file by referencing a different template in the lookup table description.

LBDB-471

(warning) The current_type cannot be the same as the one on line\n \t%d which is under the same electromigration() group. Using the last\n \tem_max_toggle_rate group encountered.

Description

Library Compiler considers em_max_toggle_rate groups with same current_type value attribute as duplicate group. If both em_max_toggle_rate groups don't specify the current_type attribue, they are also considered duplicate. Library Compiler ignores all duplicate em_max_toggle_rate groups except the last one encountered during the compilation. The compiled database contains the last one only.

The following example shows an instance where this message occurs:

```
pin(Q){
       ...
       electromigration() {
         em_max_toggle_rate(em_2d) {
                 current_type : average ;
                 values ("1, 2, 3, 4", "5, 6, 7, 8", \
                         "9, 10, 11, 12", "13, 14, 15, 16");
         }
         em_max_toggle_rate(em_2d) {
                 current_type : average ;
                 values ("21, 22, 23, 24", "25, 26, 27, 28", \
                         "29, 30, 31, 32", "33, 34, 35, 36");
         }
          related_pin : "A";
       }
  }
```

To fix the problem, remove one of the em_max_toggle_rate tables.

Feedback

```
pin(Q){
      ...
      electromigration() {
        em_max_toggle_rate(em_2d) {
                current_type : average ;
                values ("1, 2, 3, 4", "5, 6, 7, 8", \
                        "9, 10, 11, 12", "13, 14, 15, 16");
        }
        related_pin : "A";
      }
  }
```

The following is an example message:

```
Error: Line 11, The current_type cannot be the same as the one on line
      6 which is under the same electromigration() group.  Using the last
      em_max_toggle_rate group encountered. (LBDB-471)
```

What Next

Change the library source file by removing any extra em_max_toggle_rate tables within the electromigration group.

LBDB-472

(warning) The timing type of the timing arc from '%s' to\n \t'%s' is changed from '%s' to\n \t'%s'.

Description

The functional relationships between the pin and the related pin(s) dictate that this timing arc is non-rising or non-falling. This is due to the input sharing between function, three_state, and x_function.

The following example shows an instance where this message occurs:

```
pin(io){
      direction : output;
      function : "!ap & !an";
      three_state : "ap & !an";
      x_function : "!ap & an";

      timing() {
        related_pin : "ap an";
        timing_type : three_state_disable;
        ...
      }
      ...
  }
```

To fix, change functions or change timing_types.

Feedback

```
pin(io){
      ...
      timing() {
        related_pin : "ap an";
        timing_type : three_state_disable_rise;
        ...
      }
      ...
  }
```

The following is an example message:

```
Warning: Line 9, The timing type of the timing arc from 'ap' to
        'io' is changed from 'three_state_disable' to
        'three_state_disable_rise'. (LBDB-472)
```

What Next

Change the library source file so that expected timing types are entered. In case of an error, change the functional description.

LBDB-473

(error) The timing label '%s' is already used for \n \tanother timing arc in the same cell.

Description

You receive this error message when the given timing label is invalid because it was already used by another timing arc in the cell. Duplicate timing labels are not allowed within a cell.

What Next

Edit the timing label list so that there is not a label in the list that is used in another timing group in the cell.

LBDB-474

(error) The timing group has incorrect number of labels.

Description

You receive this error message when the timing group at the specified line has either too many or too few specified labels.

What Next

Edit the timing label list in your library so that the timing group has the right number of labels specified.

Feedback

LBDB-475

(error) The port '%s' is missing the attribute '%s'.

Description

You receive this error message when the *rise_capacitance* attribute or the *fall_capacitance* attribute for a port is missing and the other attribute is specified. Both or neither of the attributes must be specified.

What Next

Specify the missing attribute or remove the specified attribute.

LBDB-476

(warning) The port '%s' does not have the attribute '%s' specified. The value %f will be assigned to the attribute.

Description

You receive this error message when the *rise_capacitance* and *fall_capacitance* attributes are specified for a port, and the *capacitance* attribute is not. The maximum value between *rise_capacitance* and *fall_capacitance* will be assigned to the attrribute.

What Next

If you accept the value assigned to the attribute referenced in the error message, no action is required on your part. If not, assign a value to the attribute.

LBDB-477

(error) The table %s has invalid intermediate_values \n \tentry.

Description

This message indicates that a intermediate_values table contain invalid values. The values have to be between zero and the corresponding values from the values table attribute.

What Next

Edit the intermediate_values table so that it no longer contains invalid values.

LBDB-478

(error) The intermediate_values cannot be used with \n \tcurrent setting of output delay threshold voltages.

Feedback

Description

This message indicates that the output delay threshold voltages are not valid for the intermediate_values table. The intermediate_values table values are used to specify the values from first slew point to the output delay point. The assumption is that the output delay point lies between the two slew points. This error message is issued when Library Compiler detects that the output delay point does not lie between the two slew points and intermediate_values table was used.

What Next

Stop using the intermediate_values table or edit the library-level attributes for threshold voltages (for delay and slew).

LBDB-479

(error) when '%s' is specified '%s' has to be \n \t given as well.

Description

This message indicates that a rise net delay table was given without a fall net delay table (or vice versa). Both tables are expected by the wire delay estimator.

What Next

Edit the library source file to add the missing table or delete the incomplete table for the file to compile.

LBDB-480

(error) Missing a timing arc of timing_type 'three_state_disable' between the '%s' and '%s' pins in the '%s' cell.

Description

To describe the transition from 0->Z or 1->Z, use the timing arc with a timing_type of *three_state_disable* for the pin with a *three_state* attribute.

The following example shows an instance where this message occurs:

```
cell(BTS4)  {
        area : 3.0;
    pin(Z)  {
      direction : output;
      function : "A";
      three_state : "E";
      timing()  {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
```

```
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "A";
      }
      timing()  {
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "E";
      }
    }
    pin(A)  {
      direction : input;
        capacitance : 1.0;
    }
    pin(E)  {
      direction : input;
        capacitance : 1.0;
    }
  }
```

The following is an example message:

```
Error: Line 110, Missing a timing arc of timing_type
 'three_state_disable'
        between 'E' and 'Z' pins in the 'lbfb35' cell. (LBDB-480)
```

What Next

Add the missing timing group between the two pins. To change the message to a warning, set the environment variable *timing_check_all_errors* to 0.

LBDB-481

(warning) Port %s has multiple default timing arcs.\n \tOnly one arc is used as the default arc.

Description

You receive this message because a port has multiple default timing arcs in the case of State Dependent Timing. This is probably due to two conditions: First, a timing arc with no WHEN statement has been given as a default arc. Second, one timing arc with a condition has been specified as a default timing arc by having its *default_timing* attribute set for the arc.

What Next

Examine the library source file, and remove all but one default timing arc.

Feedback

LBDB-482

(error) Port %s has multiple timing \n \tarcs with default_timing attribute set.

Description

You receive this message because a port has multiple timing arcs with the *default_timing* attribute set. A port with State Dependent Timing should have only one timing arc. A library with this error does not compile.

What Next

Examine the library source file, and reset all but one timing arc of the *default_timing* attribute for the port.

LBDB-483

(error) Cannot find include file '%s',%s.

Description

You receive this message because one of the following: The *include()* attribute has been used to include a file but the file could not be located in the search path.

The file exists but it also includes another library file.

What Next

Add the missing include file or do not use "nested" include file.

LBDB-484

(error) No variables statement is specified in the '%s' poly_template.

Description

You receive this message because you did not define a variables statement in the specified poly_template group. Library Compiler expects you to define one variables statement there.

The following example shows an instance where this message occurs: The following example shows a poly_template named *p1* that is missing a variables statement:

```
poly_template(p1) {
  variable_1_range("1,2");
  variable_2_range("3,4");
}
```

Feedback

To correct the problem in the example above, insert the following statement in the *p1* poly_template group:

```
variables("temperature, total_output_net_capacitance");
```

The following is an example message:

```
Error: Line 191, No variables statement is specified in the 'p1'
 poly_template. (LBDB-484)
```

What Next

Define a variables statement for the specified poly_template.

LBDB-485

(error) Incompatible variable '%s' is used in the '%s' \n \tpoly_template.

Description

You receive this message because you defined an invalid variable in the variables statement in the poly_template group.

The following example shows an instance where this message occurs: In the following example, the *whatever* variable value is not valid in the *p1* poly_template.

```
poly_template(p1) {
  variables("whatever, total_output_net_capacitance");
  variable_1_range("1,2");
  variable_2_range("3,4");
}
```

To correct the problem in the example above, insert the following statement in the *p1* poly_template group:

```
variables("temperature, total_output_net_capacitance");
```

The following is an example message: Error: Line 191, Incompatible variable 'whatever' is used in the 'p1' poly_template. (LBDB-485)

What Next

Define a variable name for the specified poly_template.

LBDB-486

(warning) Variable range outside variable \n \tdimension is defined in '%s' poly_template.

Feedback

Description

You receive this message because you have defined a variable range outside the dimension of the poly_template.

The following example shows an instance where this message occurs: The following example shows a *variable_2_range* variable value that cannot be used in the *p1* poly_template.

```
poly_template(p1) {
  variables("total_output_net_capacitance");
  variable_1_range("1,2");
  variable_2_range("3,4");
}
```

Correct it by removing the *variable_2_range* statement.

The following is an example message: Warning: Line 191, Variable range outside variable dimension is defined in 'p1' poly_template. (LBDB-486)

What Next

Remove the statement for the variable range that is not in use.

LBDB-487

(error) No range information defined for variable_%d in\n\ \t'%s' poly_template.

Description

You receive this message because you have not defined the range for one of the variables used in the poly_template.

The following example shows an instance where this message occurs: The following example shows a *p1* poly_template that is missing the *variable_1_range* statement.

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_2_range("3,4");
}
```

Correct it by adding the following statement in the poly_template group:

```
variable_1_range("1,2");
```

The following is an example message: Error: Line 191, No range information defined for variable_1 in 'p1' poly_template. (LBDB-487)

What Next

Add the *variable_n_range* statement for the specified variable.

Feedback

LBDB-488

(error) No variables statement specified in '%s' \n \tdomain of '%s' poly_template.

Description

You receive this message because you have not defined a variables statement in this domain of the poly_template group.

The following example shows an instance where this message occurs: The following example shows a domain named *d1* in a poly_template named *p1* that is missing the variables statement:

```
poly_template(p1) {
  ......
  domain (d1) {
    variable_1_range("1,2");
    variable_2_range("3,4");
  }
}
```

Correct it by adding the following statement in the poly_template group:

```
variables("temperature, total_output_net_capacitance");
```

The following is an example message:

```
Error: Line 191, No variables statement specified in 'd1' domain of 'p1'
 poly_template. (LBDB-488)
```

What Next

Define a variables statement for this domain in the poly_template.

LBDB-489

(error) Incompatible variable '%s' used '%s' domain \n \tof '%s' poly_template.

Description

You receive this message because you defined an invalid variable in the variables statement of this domain in the poly_template.

The following example shows an instance where this message occurs: The following example shows an invalid variable named *whatever* in the *p1* poly_template.

```
poly_template(p1) {
  ......
  domain(d1) {
    variables("whatever, total_output_net_capacitance");
    variable_1_range("1,2");
```

Feedback

```
    variable_2_range("3,4");
  }
}
```

Correct it by adding the following statement in the domain group:

```
variables("temperature, total_output_net_capacitance");
```

The following is an example message:

```
Error: Line 191, Incompatible variable 'whatever' used in 'd1' domain of
 'p1' poly_template. (LBDB-489)
```

What Next

Examine the name of the specified variable to determine the cause.

LBDB-490

(warning) Variable range outside variable \n \tdimension is defined in '%s' domain of '%s' poly_template.

Description

You receive this message because you have defined a variable range outside the dimension of the specified domain of the poly_template.

The following example shows an instance where this message occurs: The following example shows a *variable_2_range* statement that is useless in the *d1* domain of the *p1* poly_template.

```
poly_template(p1) {
  ......
  domain(d1) {
    variables("total_output_net_capacitance");
    variable_1_range("1,2");
    variable_2_range("3,4");
  }
}
```

Correct it by removing the *variable_2_range* statement.

The following is an example message: Warning: Line 191, Variable range outside variable dimension is defined in 'd1' domain of 'p1' poly_template. (LBDB-490)

What Next

Remove the variable range statement not in use.

Feedback

LBDB-491

(error) No range information defined for variable_%d in\n \t'%s' domain of '%s' poly_template.

Description

You receive this message because you have not defined a range for the specified variable used in this domain of the poly_template.

The following example shows an instance where this message occurs: The following example shows the *d1* domain of the *p1* poly_template with the *variable_1_range* statement missing.

```
poly_template(p1) {
  ......
  domain(d1) {
    variables("temperature, total_output_net_capacitance");
    variable_2_range("3,4");
  }
}
```

Correct it by adding the following statement:

```
variable_1_range("1,2");
```

The following is an example message: Error: Line 191, No range information defined for variable_1 in 'd1' domain of 'p1' poly_template. (LBDB-491)

What Next

Add a *variable_n_range* statement (substituting the specified variable number for *n*).

LBDB-492

(error) Power rail mapping information missing in\n \t'%s' poly_template.

Description

You receive this message because you have not defined the power rail mapping information for the *voltage2* variable in the poly_template.

The following example shows an instance where this message occurs: The following example shows the *p1* poly_template with the mapping statement missing.

```
poly_template(p1) {
  variables("temperature, voltage2, total_output_net_capacitance");
  ......
}
```

Feedback

Correct it by adding the following statement:

```
mapping("voltage2, VDD");
```

The following is an example message: Error: Line 191, Power rail mapping information missing in 'p1' poly_template. (LBDB-492)

What Next

Add the mapping statement in the poly_template.

LBDB-493

(error) Power rail mapping information missing in\n \t'%s' domain of '%s' poly_template.

Description

You receive this message because you have not defined the power rail mapping information for the voltage2 variable in the specified domain of the specified poly_template.

The following example shows an instance where this message occurs: The following example shows the *d1* domain of the *p1* poly_template with the mapping statement missing.

```
poly_template(p1) {
  ......
  domain(d1) {
    variables("temperature, voltage2, total_output_net_capacitance");
    ......
  }
}
```

Correct it by adding the following statement:

```
mapping("voltage2, VDD");
```

The following is an example message: Error: Line 191, Power rail mapping information missing in 'd1' domain of 'p1' poly_template. (LBDB-493)

What Next

Add the mapping statement in this domain of the poly_template.

LBDB-495

(error) Invalid number of dimensions in '%s' \n \t poly_template.

Feedback

Description

You receive this message because the number of variables you have defined in the poly_template is invalid.

The following example shows an instance where this message occurs: The following example shows a variables statement that defines the wrong number of variables in the *p1* poly_template.

```
poly_template(p1) {
  variables("");
  ......
}
```

Correct it by changing the variables statement in the poly_template group to the following:

```
variables("temperature, total_output_net_capacitance");
```

The following is an example message: Error: Line 191, Invalid number of dimensions in 'p1' poly_template. (LBDB-495)

What Next

Examine the variables statement to determine why the number of variables is invalid.

LBDB-496

(error) Invalid number of dimensions in '%s' \n \t domain of '%s' poly_template.

Description

You receive this message because the number of variables you have defined in the specified domain of the specified poly_template is invalid.

The following example shows an instance where this message occurs: The following example shows a variables statement that defines the wrong number of variables in the *d1* domain of the *p1* poly_template.

```
poly_template(p1) {
  ......
  domain (d1) {
    variables("");
    ......
  }
}
```

Correct it by changing the variables statement in this domain of the poly_template group to the following:

```
variables("temperature, total_output_net_capacitance");
```

Feedback

The following is an example message: Error: Line 191, Invalid number of dimensions in 'd1' domain of 'p1' poly_template. (LBDB-496)

What Next

Examine the variables statement to determine why the number of variables is invalid.

LBDB-497

(error) Incomplete range of variable in '%s' \n \t poly_template.

Description

You receive this message because the variable statement of the specified poly_template has an incomplete range.

The following example shows an instance where this message occurs: The following example shows the *p1* poly_template with an incomplete *variable_1_range* statement.

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_1_range("1");
  ......
}
```

Correct it by changing the *variable_1_range* statement in the poly_template group to the following:

```
variable_1_range("1,2");
```

The following is an example message: Error: Line 191, Incomplete range of variable in 'p1' poly_template. (LBDB-497)

What Next

Examine all *variable_n_range* statements (substituting each existing variable number for *n*) of the specified poly_template to determine those that have an incomplete range.

LBDB-498

(error) Incomplete range of variable in '%s' \n \t domain of '%s' poly_template.

Description

You receive this message because the variable statement in the specified domain of the specified poly_template has an incomplete range.

The following example shows an instance where this message occurs: The following example shows *d1* domain of the *p1* poly_template with an incomplete *variable_1_range* statement.

Feedback

```
poly_template(p1) {
  ......
  domain (d1) {
    variables("temperature, total_output_net_capacitance");
    variable_1_range("1");
    ......
  }
}
```

Correct it by changing the *variable_1_range* statement in the *d1* domain of the poly_template group to the following:

```
variable_1_range("1,2");
```

The following is an example message: Error: Line 191, Incomplete range of variable in 'd1' domain of 'p1' poly_template. (LBDB-498)

What Next

Examine all *variable_n_range* statements (substituting each existing variable number for *n*) in the specified domain of the specified poly_template to determine those that have an incomplete range.

LBDB-499

(error) No orders information defined for the polynomial.

Description

You receive this message because you have not defined the *orders* statement for the polynomial.

The following example shows an instance where this message occurs: The following example shows a poly timing group with a missing *orders* statement.

```
rise_constraint(constraint) {
    coefs("1.2095, 0.2281, 0.0225, -0.0001, 0.0678, -0.0002, 0.0000,
 0.0000");
  }
```

Correct it by adding the following statement before the *coefs* statement:

```
orders("1,1,1");
```

The following is an example message: Error: Line 191, No orders information defined for the polynomial. (LBDB-499)

What Next

Add the *orders* statement before the *coefs* statement.

Feedback

LBDB-500

(error) No orders information defined for '%s' \n \t domain of the polynomial.

Description

You receive this message because you have not defined the *orders* statement for this domain of the polynomial.

The following example shows an instance where this message occurs: The following example shows the *d1* domain of a poly timing group with a missing *orders* statement.

```
rise_constraint(constraint) {
    ......
    domain (d1) {
      coefs("1.2095, 0.2281, 0.0225, -0.0001, 0.0678, -0.0002, 0.0000,
 0.0000");
    }
  }
```

Correct it by adding the following statement before the *coefs* statement:

```
orders("1,1,1");
```

The following is an example message: Error: Line 191, No orders information defined for 'd1' domain of the polynomial. (LBDB-500)

What Next

Add the *orders* statement before the *coefs* statement.

LBDB-501

(error) No coefs information defined for the polynomial.

Description

You receive this message because you have not defined the *coefs* statement for the polynomial.

The following example shows an instance where this message occurs: The following example shows a poly timing group with a missing *coefs* statement.

```
rise_constraint(constraint) {
    orders("1,1,1");
  }
```

Correct it by adding the following statement after the *orders* statement:

```
coefs("1.2095, 0.2281, 0.0225, -0.0001, 0.0678, -0.0002, 0.0000,
 0.0000");
```

Feedback

The following is an example message: Error: Line 191, No coefs information defined for the polynomial. (LBDB-500)

What Next

Add the *coefs* statement after the *orders* statement.

LBDB-502

(error) No coefs information defined for '%s' \n \t domain of the polynomial.

Description

You receive this message because you have not defined the *coefs* statement for the specified domain of the polynomial.

The following example shows an instance where this message occurs: The following example shows the *d1* domain of a poly timing group with a missing *coefs* statement.

```
rise_constraint(constraint) {
    ......
    domain (d1) {
      orders("1,1,1");
    }
  }
```

Correct it by adding the following after the *orders* statement:

```
coefs("1.2095, 0.2281, 0.0225, -0.0001, 0.0678, -0.0002, 0.0000,
 0.0000");
```

The following is an example message: Error: Line 191, No coefs information defined for 'd1' domain of the polynomial. (LBDB-502)

What Next

Add the *coefs* statement for the specified domain after the *orders* statement.

LBDB-503

(Error) The low range setting is equal to or greater than the high range setting in %s.

Description

This warning message tells you that the values specified for the variable range setting statement are incorrect. Only temperature, voltages, and generic parameters can have the same low range and high range.

The following example shows an instance where this message occurs: The following example shows the p1 poly_template with an incomplete variable_1_range statement.

Feedback

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_1_range("100,1");
  ......
}
```

Correct it by changing the variable_1_range statement in the poly_template group to the following:

```
variable_1_range("1,100");
```

The following is an example message: Error: Line 191, The low range setting is equal to or greater than the high range setting in variable_1_range. (LBDB-503)

LBDB-504

(warning) Range setting in domain at variable_%d_range conflicts with template setting. Use the template setting instead.

Description

This warning tells you that the variable range setting statement has a range that conflicts with the range set previously in the template.

The following example shows an instance where this message occurs: The following example shows the p1 poly_template with an incorrect variable_1_range statement in the domain.

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_1_range("1,50");
  domain (d1) {
    variable_1_range("2,100");
  }
  ......
}
```

Correct it by changing the variable_1_range statement in the domain to the following:

```
variable_1_range("2,40");
```

The value 40 can be any number less than or equal to 50.

The following is an example message: Warning: Line 191, Range setting conflicts with template setting. (LBDB-504)

What Next

Examine all variable_*n*_range statements. Substitute each existing variable number for *n* in the specified poly_template to determine the statements that conflict with each other.

Feedback

LBDB-505

(error) Variable %s is not a voltage. Can only map voltages to a power rail.

Description

This error message tells you that the first variable in mapping is not a voltage. Only voltages can be mapped to a power rail.

The following example shows an instance where this message occurs: The following example shows the p1 poly template with an incorrect mapping statement.

```
poly_template(p1) {
  variables("temperature, voltage,total_output_net_capacitance");
  variable_1_range("20,150");
  variable_2_range("1.2,3.2");
  variable_3_range("10,30");
  mapping(temperature,VDD1);
  ......
}
```

Fix the mapping statement by changing the variable_1_range statement in the domain to the following:

```
mapping(voltage,VDD1);
```

The following is an example message: Error: Line 191, Variable temperature is not a voltage (LBDB-505).

What Next

Check the variables in the mapping and replace the first variable with a voltage.

LBDB-506

(error) Variable %s is not defined in the %s.

Description

This error message tells you that the first variable in mapping is not defined in the template.

The following example shows an instance where this message occurs: The following example shows the p1 poly_template with an incorrect mapping statement.

```
poly_template(p1) {
  variables("temperature, voltage,total_output_net_capacitance");
  variable_1_range("20,150");
  variable_2_range("1.2,3.2");
  variable_3_range("10,30");
  mapping(voltage1,VDD1);
```

```
  ......
}
```

Correct it by changing the variable_1_range statement in the domain to the following:

```
mapping(voltage,VDD1);
```

The following is an example message: Error: Line 191, Variable voltage1 is not defined in the template (LBDB-506).

What Next

Define the variable in the template, or change the variable_1_range statement in the domain.

LBDB-507

(error) Attempting to map to %s, which is defined in power_supply group. However, power_supply group is missing.

Description

This error message tells you that you have not defined a power_supply group before using its information.

The following example shows an instance where this message occurs: The following example shows the p1 poly_template with the mapping statement missing.

```
poly_template(p1) {
  variables("temperature, voltage2, total_output_net_capacitance");
  mapping("voltage2, VDD");
  ......
}
```

Correct it by adding the following statement before the template:

```
power_supply() {
    default_power_rail : VDD ;
  }
```

The following is an example message: Error: Line 191, Power_supply group missing but trying to map to %s, which is supposed to be defined in a power_supply group. (LBDB-507)

What Next

Add a power_supply group before the templates.

Feedback

LBDB-508

(error) The '%s' port has hyperbolic low groups. Only input pin or bidirectional pin can have hyperbolic low groups.

Description

Library Compiler issues this error message if one hyperbolic low group is defined within an output pin.

The following example shows an instance where this message occurs:

```
pin(Q){
      direction : output;
      ...
      hyperbolic_noise_low() {
        ...
      }
  }
```

To correct the problem, remove one of the hyperbolic low groups.

```
pin(Q){
      direction : output;
      ...
  }
```

The following is an example message:

```
Error: Line 6, The 'Q' port has hyperbolic groups.
        Only input pin or bidirectional pin can have hyperbolic low
 groups. (LBDB-508)
```

What Next

Change the library source file by removing the hyperbolic low groups within the output pin group.

LBDB-509

(error) The '%s' port has hyperbolic high groups.\n \tOnly input pin or bi-directional pin can have hyperbolic high groups.

Description

Library Compiler issues this error message if one hyperbolic high group is defined within a output pin.

Feedback

The following example shows an instance where this message occurs:

```
pin(Q){
      direction : output;
      ...
      hyperbolic_noise_high() {
      }
  }
```

To fix the problem, remove one of the hyperbolic high groups.

```
pin(Q){
      direction : output;
      ...
  }
```

The following is an example message:

```
Error: Line 6, The 'Q' port has hyperbolic groups.
        Only input pin or bi-directional pin can have hyperbolic high
 groups. (LBDB-509)
```

What Next

Change the library source file by removing the hyperbolic high groups within the output pin group.

LBDB-510

(error) The '%s' port has hyperbolic above_high groups.\n \tOnly input pin or bi-directional pin can have hyperbolic above_high groups.

Description

Library Compiler issues this error message if one hyperbolic above_high group is defined within a output pin.

The following example shows an instance where this message occurs:

```
pin(Q){
      direction : output;
      ...
      hyperbolic_noise_above_high() {
      }
  }
```

To fix the problem, remove one of the hyperbolic above_high groups.

```
pin(Q){
      direction : output;
      ...
  }
```

The following is an example message:

```
Error: Line 6, The 'Q' port has hyperbolic groups.
        Only input pin or bi-directional pin can have hyperbolic
 above_high groups. (LBDB-510)
```

What Next

Change the library source file by removing the hyperbolic above_high groups within the output pin group.

LBDB-511

(error) The '%s' port has hyperbolic below_low groups.\n \tOnly input pin or bi-directional pin can have hyperbolic below_low groups.

Description

Library Compiler issues this error message if one hyperbolic below_low group is defined within a output pin.

The following example shows an instance where this message occurs:

```
pin(Q){
      direction : output;
      ...
      hyperbolic_noise_below_low() {
      }
  }
```

To fix the problem, remove one of the hyperbolic below_low groups.

```
pin(Q){
      direction : output;
      ...
  }
```

The following is an example message:

```
Error: Line 6, The 'Q' port has hyperbolic groups.
        Only input pin or bi-directional pin can have hyperbolic
 below_low groups. (LBDB-511)
```

What Next

Change the library source file by removing the hyperbolic below_low groups within the output pin group.

Feedback

LBDB-512

(error) The '%s' port has noise hyperbolic groups.\n \tOnly one input/bi-directional port can have noise hyperbolic groups.

Description

Library Compiler issues this error message if more than one noise hyperbolic is defined within a timing.

The following example shows an instance where this message occurs:

```
pin(Q){
      direction : output;
      ...
      noise_hyperbolic_low() {
        ...
      }
  }
```

To fix the problem, remove one of the noise hyperbolic groups.

```
pin(Q){
      direction : output;
      ...
  }
```

The following is an example message:

```
Error: Line 6, The 'Q' port has noise hyperbolic groups.
        Only input/bi-directional ports can have noise hyperbolic groups.
 (LBDB-512)
```

What Next

Change the library source file by removing any extra noise hyperbolic groups within the pin group.

LBDB-513

(error) The '%s' port has repeated noise hyperbolic groups. Only one such group is allowed.

Description

Library Compiler issues this error message if more than one of the same noise hyperbolic group is defined within a timing.

Feedback

The following example shows an instance where this message occurs:

```
pin(Q){
      ...
      noise hyperbolic_low() {
        ...
      }
      noise hyperbolic_low() {
        ...
      }
  }
```

To correct the problem, remove extra noise hyperbolic groups.

```
pin(Q){
      ...
      noise hyperbolic_low() {
        ...
      }
  }
```

The following is an example message:

```
Error: Line 6, The 'Q' port has repeated noise hyperbolic groups.
        Only one such group is allowed. (LBDB-513)
```

What Next

Change the library source file by removing any extra noise hyperbolic groups within the timing group.

LBDB-514

(error) The constraint timing arc has noise immunity groups.\n \tOnly non-constraint timing arc can specify such info.

Description

Library Compiler issues this error message if noise immunity info is defined within a constraint timing arc.

The following example shows an instance where this message occurs:

```
pin(Q){
      direction : output;
      ...
      timing() {
         timing_type: setup_rising;
         ...
         noise_immunity_low() {
           ...
         }
```

```
      }
  }
```

To fix the problem, remove the noise immunity tables/polys.

```
pin(Q){
      direction : output;
      ...
      timing() {
         timing_type: setup_rising;
         ...
      }
  }
```

The following is an example message:

```
Error: Line 6, The timing arc has noise immunity groups.
        Only non-constraint timing arc can specify such info. (LBDB-514)
```

What Next

Remove the noise immunity tables/polys.

LBDB-515

(error) The '%s' port has repeated noise immunity groups inside timing group. Only one such group is allowed.

Description

Library Compiler issues this error message if more than one noise immunity is defined within a timing group.

The following example shows an instance where this message occurs:

```
pin(Q){
      ...
      timing() {
         ...
         noise_immunity_low() {
           ...
         }
         noise_immunity_low() {
           ...
         }
      }
  }
```

To correct the problem, remove extra noise immunity groups.

```
pin(Q){
      ...
```

Feedback

```
      timing() {
      ...
        noise_immunity_low() {
        ...
        }
      }
  }
```

The following is an example message:

```
Error: Line 6, The 'Q' port has repeated noise immunity groups inside
 timing group.
        Only one such group is allowed. (LBDB-515)
```

What Next

Change the library source file by removing any extra noise immunity tables or polys within the timing group.

LBDB-516

(error) The '%s' group uses\n \ttemplate '%s' which does not contain 'iv_output_voltage' as its variable.

Description

The iv characteristics group must use a 1-d iv characteristics template with *iv_output_voltage* as its variable.

The following example shows an instance where this message occurs:

```
iv_lut_template(ok_temp){
        variable_1 : iv_output_voltage;
        index_1("0.5,1.0,1.5,2.0,2.5");
    }
    iv_lut_template(err_temp){
        variable_1 : input_transition_time;
        index_1("0.5,1.0,1.5,2.0,2.5");
    }
    ...
         steady_state_current_high(err_temp) {
                values("1.385,2.554,3.722,4.891,6.059");;
        }
```

To fix the problem, change the template value of the *steady_state_current_high* attribute from *err_temp* to *ok_temp*.

The following is an example message:

```
Error: Line 126, The 'steady_state_current_high' group in the timing
       group cannot use 'err_temp' as its template. (LBDB-516)
```

Feedback

What Next

Change the library source file by including 'iv_output_voltage' in the template.

LBDB-517

(error) The '%s' lookup table in the\n \ttiming group cannot use '%s' as its template.

Description

The noise characteristics group must use a 2-d noise characteristics template with *input_noise_width, total_output_net_capacitance* as its variables.

The following example shows an instance where this message occurs:

```
noise_lut_template(ok_temp){
        variable_1 : input_noise_width;
        variable_2 : total_output_net_capacitance;
        index_2("1.0,2.0,4.0,6.0,10.0");
        index_2("0.5,1.0,1.5,2.0,2.5");
    }
    noise_lut_template(err_temp){
        variable_1 : input_net_transition;
        variable_2 : total_output_net_capacitance;
        index_2("1.0,2.0,4.0,6.0,10.0");
        index_2("0.5,1.0,1.5,2.0,2.5");
    }
    ...
         noise_immunity_high(err_temp) {
                values("0.733,1.073,1.412,1.752,2.092",\
                           "0.873,1.214,1.554,1.894,2.234",\
                           "1.095,1.442,1.787,2.132,2.477",\
                           "1.298,1.648,1.996,2.343,2.691",\
                           "1.703,2.060,2.414,2.766,3.119");
        }
```

To fix the problem, change the template value of the *noise_immunity_high* attribute from *err_temp* to *ok_temp*.

The following is an example message:

```
Error: Line 126, The 'noise_immunity_high' lookup table in the timing
       group cannot use 'err_temp' as its template. (LBDB-517)
```

What Next

Change the library source file by including 'input_noise_width' and 'total_output_net_capacitance' in the template.

Feedback

LBDB-519

(error) The timing arc has steady_state_resistance_low/high/above_high/below_low attribute specified.\n \tOnly combo, enable, disable, rising_edge, falling_edge, clear and preset timing arc can specify such attributes.

Description

Library Compiler issues this error message if any steady_state_resistance_low/high/above_high/below_low attribute is defined within a timing arc which is not combo, disable or enable.

The following example shows an instance where this message occurs:

```
pin(Q){
       ...
       timing() {
         timing_type : setup_rising;
         ...
         steady_state_resistance_high() {
            ...
         }
       }
  }
```

To fix the problem, remove the steady_state_resistance attributes.

```
pin(Q){
       ...
       timing() {
         timing_type : setup_rising;
         ...
       }
  }
```

The following is an example message:

```
Error: Line 6, The timing arc has
 steady_state_resistance_low/high/above_high/below_low attribute
 specified.
        Only combo, enable, disable, rising_edge, falling_edge, clear and
 preset timing arc can specify such attributes. (LBDB-519)
```

What Next

Change the library source file by removing such attributes inside the timing() group.

LBDB-520

(error) The timing arc has steady_state_current_high/low specified.\n \tOnly combo, rising_edge, falling_edge, preset and clear timing arcs can specify such info.

Feedback

Description

Library Compiler issues this error message if any steady_state_current_high/low group is defined within a timing group which is not combo, disable or enable.

The following example shows an instance where this message occurs:

```
pin(Q){
      ...
      timing() {
        timing_type : setup_rising;
        ...
        steady_state_current_high(iv1x5) {
           ...
        }
      }
  }
```

To fix the problem, remove the steady_state_current_high group.

```
pin(Q){
      ...
      timing() {
        timing_type : setup_rising;
        ...
      }
  }
```

The following is an example message:

```
Error: Line 6, The timing arc has steady_state_current_high/low
 specified.
       Only combo, rising_edge, falling_edge, preset and clear timing
 arcs can specify such info. (LBDB-520)
```

What Next

Change the library source file by removing such groups inside the timing() group.

LBDB-521

(error) The timing arc has steady_state_current_tristate specified.\n \tOnly enable or disable timing arc can specify such info.

Description

Library Compiler issues this error message if any steady_state_current_tristate group is defined within a timing group which is not disable or enable.

Feedback

The following example shows an instance where this message occurs:

```
pin(Q){
      ...
      timing() {
        timing_type : setup_rising;
        ...
        steady_state_current_tristate(iv1x5) {
           ...
        }
      }
  }
```

To fix the problem, remove the steady_state_current_tristate group.

```
pin(Q){
      ...
      timing() {
        timing_type : setup_rising;
        ...
      }
  }
```

The following is an example message:

```
Error: Line 6, The timing arc has steady_state_current_tristate
 specified.
        Only enable or disable timing arc can specify such info.
 (LBDB-521)
```

What Next

Change the library source file by removing such groups inside the timing() group.

LBDB-522

(error) The '%s' group in the\n \ttiming arc cannot use '%s' as its template.

Description

The noise characteristics group must use a 3-d noise characteristics template with *input_noise_width, input_noise_height, total_output_net_capacitance* as its variables.

The following example shows an instance where this message occurs:

```
...
    propagation_lut_template(ok_temp){
        variable_1 : input_noise_width;
        variable_2 : input_noise_height;
        variable_3 : total_output_net_capacitance;
        index_1("1.0,2.0,4.0,6.0,10.0");
        index_2("0.5,1.0,1.5,2.0,2.5");
```

Feedback

```
        index_3("0.5,1.0,1.5,2.0,2.5");
    }
    noise_lut_template(err_temp){
        variable_1 : input_net_transition;
        variable_2 : input_noise_height;
        variable_3 : total_output_net_capacitance;
        index_1("1.0,2.0,4.0,6.0,10.0");
        index_2("0.5,1.0,1.5,2.0,2.5");
        index_3("0.5,1.0,1.5,2.0,2.5");
    }
    ...
         propagation_noise_width_high(err_temp) {
                values("0.733,1.073,1.412,1.752,2.092",\
                           "0.873,1.214,1.554,1.894,2.234",\
                           "1.095,1.442,1.787,2.132,2.477",\
                           "1.298,1.648,1.996,2.343,2.691",\
                           ...
                           "1.703,2.060,2.414,2.766,3.119");
        }
```

To fix the problem, change the template value of the *propagation_noise_width_high* attribute from *err_temp* to *ok_temp*.

The following is an example message:

```
Error: Line 126, The 'propagation_noise_width_high' group in the timing
       arc cannot use 'err_temp' as its template. (LBDB-522)
```

What Next

Change the library source file by including 'input_noise_width', 'input_noise_height' and 'total_output_net_capacitance' in the template.

LBDB-523

(error) The related '%s' group is not specified for\n \tthe %s' group in the timing arc.

Description

The noise propagation width and height group must coexist for the same region(low, high, below_low, above_high).

The following example shows an instance where this message occurs:

```
...
        timing() {
                propagation_noise_width_high(ok_temp) {
                values("0.733,1.073,1.412,1.752,2.092",\
                           "0.873,1.214,1.554,1.894,2.234",\
                           "1.095,1.442,1.787,2.132,2.477",\
                           "1.298,1.648,1.996,2.343,2.691",\
                           ...
```

Feedback

```
                    "1.703,2.060,2.414,2.766,3.119");
                }
                propagation_noise_width_low(ok_temp) {
                values("0.733,1.073,1.412,1.752,2.092",\
                    "0.873,1.214,1.554,1.894,2.234",\
                    "1.095,1.442,1.787,2.132,2.477",\
                    "1.298,1.648,1.996,2.343,2.691",\
                    ...
                    "1.703,2.060,2.414,2.766,3.119");
                propagation_noise_height_low(ok_temp) {
                values("0.733,1.073,1.412,1.752,2.092",\
                    "0.873,1.214,1.554,1.894,2.234",\
                    "1.095,1.442,1.787,2.132,2.477",\
                    "1.298,1.648,1.996,2.343,2.691",\
                    ...
                    "1.703,2.060,2.414,2.766,3.119");
        }
        ...
```

To fix the problem, add the *propagation_noise_width_high* group in the timing group.

The following is an example message:

```
Error: Line 126, The related 'propagation_noise_height_high' group is not
 specified
        for the 'propagation_noise_width_high' group in the timing arc.
 (LBDB-523)
```

What Next

Add the missiong propagation group in the timing group.

LBDB-524

(error) Invalid variable '%s' is used in the '%s' \n \tpoly_template refered by %s group.

Description

You receive this message because you defined an invalid variable in the variables statement in the poly_template group refered by leakage_power or pin_capacitance group. The valid variables can only be temperature voltage, and power_rails.

The following example shows an instance where this message occurs: In the following example, the *whatever* variable value is not valid in the *p1* poly_template.

```
poly_template(p1) {
  variables("temperature, total_output_net_capacitance");
  variable_1_range("1,2");
  variable_2_range("3,4");
}
```

Feedback

To correct the problem in the example above, insert the following statement in the *p1* poly_template group:

```
variables("temperature, voltage");
```

The following is an example message: Error: Line 191, Invalid variable 'total_output_net_capacitance' is used in the 'p1' poly_template refered by leakage_power group.(LBDB-524)

What Next

Define a variable name for the specified poly_template.

LBDB-525

(error) Only polynomial format is supported for '%s' group.

Description

You receive this message because you defined an non-polynomial group, such as pin_capacitance() group, leakagage_power() group.

What Next

Please redefine these groups using polynomials.

LBDB-526

(warning) The always on cell has no always on pin related to backup power or ground.

Description

If the cell is an always_on buffer/invertor cell, then backup power/ground is the preferred related pg pin.

This message is showed up when the cell has backup power/ground, but there is no singal pin related to backup pg pins.

The following example shows an instance where this message occurs:

```
cell(test) {
   always_on : TRUE;
   pg_pin(PWR) {
   voltage_name : VDD;
   pg_type : primary_power;
   }
   pg_pin(GND) {
   voltage_name : VSS;
   pg_type : primary_ground;
   }
```

Feedback

```
    pg_pin(GND1) {
    voltage_name : VSS1;
    pg_type : backup_ground;
    }
    pg_pin(VDDI) {
    voltage_name : VDDH;
    pg_type : backup_power;
    }
    ...
    pin(A) {
         direction : input;
         related_power_pin : PWR;
         related_ground_pin : GND;
       ...
    }
    pin(Z) {
         direction : output;
         function : A;
         related_power_pin : VDD;
         related_ground_pin : GND;
      ...
    }
    ...
}
```

Both input pin A and output pin Z should connect to backup PG.

The following is an example message:

```
Warning: Line 335, Cell "test", The always on cell has no always on pin
 related to backup power or ground. (LBDB-526)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-527

(warning) is_clock_isolation_cell attribute is not supported. It's marked as dont_use, dont_touch.

Description

Currently if an isolation cell is modeled using the is_clock_isolation_cell attribute, it can not be auto inferred by Galaxy design tools (e.g. Power Compiler). Thus the cell is being marked as dont_touch and dont_use during read_lib.

The following is an example message:

```
Warning: Line 1023, Cell 'A', is_clock_isolation_cell attribute is not
 supported. (LBDB-527)
```

Feedback

What Next

Warning only. No action is required.

LBDB-530

(error) The pin '%s' used in\n \t%s '%s' cannot specify the '%s' %s.

Description

This error message occurs when the pin with "is_isolated" attribute is used in the expression of isolation_enable_condition.

The following example shows an instance where this message occurs: The following is an example of incorrect input that causes this error message:

```
cell (lbdb530) {
    ...
    pin (EN) {
      direction   :   input;
      capacitance :   1.0;
      fanout_load :   1.0;
      is_isolated :   true;
    }
    pin(Q0){
        direction   :   output;
        function : "I1";
        is_isolated :   true;
        isolation_enable_condition : "EN";

    }
    ...
  }
```

In this case, pin EN used in the attribute isolation_enable_condition of pin Q0 has been specified with is_isolated attribute. To fix the error, remove is_isolated attribute from pin EN.

The following is an example message:

```
Error: Line 179, Cell 'lbdb530', pin 'Q0', The pin 'EN' used in
        attribute 'isolation_enable_condition' cannot specify the
 'is_isolated' attribute. (LBDB-530)
```

What Next

Check the library source file and remove is_isolated attribute from the pin, or don't use the pin in the expression of isolation_enable_condition.

Feedback

LBDB-541

(error) The pin '%s' in the short list is not an 'inout' pin.

Description

The port in "short" attribute must be direction "inout".

The following example shows an instance where this message occurs:

```
cell (c) {
  ...
  short(A, Y);
  pin (A) {
    direction : input ;
    ...
  }
  pin (Y) {
    direction : input ;
    ...
  }
}
```

The following is an example message:

```
Error: Line 145, Cell 'c', The pin 'A' in the short list is not an
 'inout' pin. (LBDB-541)
```

What Next

Correct the port direction.

LBDB-542

(error) The pin '%s' in the short list is missing pin capacitance attribute.

Description

The port in "short" attribute must be specified with "capacitance" (or "rise_capacitance/ fall_capacitance") attribute.

The following example shows an instance where this message occurs:

```
cell (c) {
  ...
  short(A, Y);
  pin (A) {
    ...
  }
  pin (Y) {
    capacitance : 0.01 ;
    ...
```

```
  }
}
```

The following is an example message:

```
Error: Line 145, Cell 'c', The pin 'A' in the short list is missing pin
 capacitance attribute. (LBDB-542)
```

What Next

Add the pin capacitance attribute on the port.

LBDB-543

(error) Found an inconsistant pin capacitance for the shorted pin.

Description

The ports in same “short” attribute must be specified with identical "capacitance" (or “rise_capacitance/fall_capacitance”) attribute.

The following example shows an instance where this message occurs:

```
cell (c) {
  ...
  short(A, Y);
  pin (A) {
    capacitance : 0.01 ;
    ...
  }
  pin (Y) {
    capacitance : 0.02 ;
    ...
  }
}
```

The following is an example message:

```
Error: Line 145, Cell 'c', Pin 'Y', Found an inconsistant pin capacitance
 for the shorted pin. (LBDB-543)
```

What Next

Correct the pin capacitance attribute on the port.

LBDB-544

(error) The "retention_equivalent_cell" attribute can not be specified in a retention cell.

Feedback

Description

This message indicates that both attribute "retention_cell" and "retention_equivalent_cell" are specified on the cell. The "retention_equivalent_cell" is for a non-retention cell to point to its retention equivalent cell. So it can only be specified on a non retention cell.

The following example shows an instance where this message occurs:

```
cell (ret_cell) {

    retention_cell : test;
    retention_equivalent_cell : my_ret_cell;

    ...

  }
```

The following is an example message:

```
Error: Line 149, Cell 'ret_cell', The "retention_equivalent_cell"
 attribute can not be specified in a retention cell. (LBDB-544)
```

What Next

Check the library source file, remove the retention_equivalent_cell attribute.

LBDB-545

(error) The "retention_equivalent_pin" attribute can not be specified in cell without "retention_equivalent_cell" attribute.

Description

This message indicates that the pin has attribute "retention_equivalent_pin", but no cell level attribute "retention_equivalent_cell" specified. "retention_equivalent_pin" can only be used together with "retention_equivalent_cell" to describe the pin name.

The following example shows an instance where this message occurs:

```
cell (cell) {

    /* retention_equivalent_cell : my_ret_cell; */

    pin(D) {
      retention_equivalent_pin : DD;
      ...
    }

    ...

  }
```

Feedback

The following is an example message:

```
Error: Line 149, Cell 'ret_cell', Pin 'D', The "retention_equivalent_pin"
 attribute can not be specified in cell without
 "retention_equivalent_cell" attribute. (LBDB-545)
```

What Next

Check the library source file, add the retention_equivalent_cell attribute.

LBDB-546

(warning) The "retention_equivalent_cell" can not be specified in a non-black-box cell.

Description

This message indicated that cell is not a black-box cell, but is specified with "retention_equivalent_cell" attribute. The "retention_equivalent_cell" is desired for complex cell, so the cell should be black-box.

What Next

Check the library source file, remove the retention_equivalent_cell attribute.

LBDB-547

(warning) The cell referenced by "retention_equivalent_cell" attribute must be a retention cell.

Description

This message indicates that the cell referenced by "retention_equivalent_cell" is not a retention cell, it is missing the "retention_cell" attribute, or the attribute is pointing to a wrong cell.

The following example shows an instance where this message occurs:

```
cell (cell) {

    retention_equivalent_cell : my_ret_cell;

    ...

  }

  cell (my_ret_cell) {

    /* retention_cell : test; */

    ...
```

Feedback

```
}
```

The following is an example message:

```
Warning: Line 149, Cell 'my_ret_cell', The cell referenced by
 "retention_equivalent_cell" attribute must be a retention cell.
 (LBDB-547)
```

What Next

Check the library source file, add the retention_cell attribute, or correct the retention_equivalent_cell attribute.

LBDB-548

(warning) The cell referenced by "retention_equivalent_cell" attribute can't have dont_use attribute.

Description

This message indicates that the cell referenced by "retention_equivalent_cell" is a dont_use cell. This is wrong for optimization tools.

The following example shows an instance where this message occurs:

```
cell (cell) {

    retention_equivalent_cell : my_ret_cell;

    ...

  }

  cell (my_ret_cell) {

    dont_use: true;

    ...

  }
```

The following is an example message:

```
Error: Line 149, Cell 'my_ret_cell', The cell referenced by
 "retention_equivalent_cell" attribute can't have dont_use attribute.
 (LBDB-548)
```

What Next

Check the library source file, remove the dont_use attribute, or correct the retention_equivalent_cell attribute.

Feedback

LBDB-549

(warning) The cell referenced by "retention_equivalent_cell" attribute has inconsistent bias pg_pin setting with non-retention cell.

Description

If non-retention cell has bias pg_pin, its retention equivalent cell should also have bias pg_pin; If non-retention cell has no bias pg_pin, its retention equivalent cell should also have no bias pg_pin; This message indicates that the non-retention cell and its retention equivalent cell have different bias pg_pin setting.

The following example shows an instance where this message occurs:

```
cell (cell) {

    retention_equivalent_cell : my_ret_cell;

    /*
    pg_pin(VBP) {
      pg_type: pwell;
    }
    */
    ...

  }

  cell (my_ret_cell) {

    pg_pin(VBP) {
      pg_type: pwell;
    }

    ...

  }
```

The following is an example message:

```
Error: Line 149, Cell 'my_ret_cell', The cell referenced by
 "retention_equivalent_cell" attribute has inconsistent bias pg_pin
 setting with non-retention cell. (LBDB-549)
```

What Next

Check the library source file, correct the bias pg_pin setting.

LBDB-550

(warning) %s should be consistent with %s.

Feedback

Description

This message occurs when 2 or more related LVF table values should be consistent with each other.

```
The rules are issuing Warning when:
  Rule 1: mean_shift * skewness  < 0 (obsolete)
  Rule 2: skewness * (sigma_late - simga_early) < 0
  Rule 3: (std_dev - sigma_early) * (std_dev - sigma_late) > 0
```

For example, the corresponding values of skewness * (sigma_late - simga_early) should be negative.

The following example shows the inconsistent ocv_sigma_cell_fall early/late value and ocv_skewness_cell_fall table(ocv_std_dev_cell_fall value):

```
lu_table_template("del_1_8_7") {
    variable_1 : "input_net_transition" ;
    index_1("1, 2, 3, 4, 5, 6, 7, 8");
    variable_2 : "total_output_net_capacitance" ;
    index_2("1, 2, 3, 4, 5, 6, 7");
  }
 ...
 timing() {
   ...
    ocv_skewness_cell_fall(del_1_8_7) {
          index_1("0.004626, 0.009397, 0.01909, 0.03877, 0.07875, 0.16,
 0.3249, 0.66");
          index_2("0.000253, 0.0007021, 0.001949, 0.005408, 0.01501,
 0.04166, 0.1156");
          values("0.0003315, 0.0004154, 0.0006503, 0.001309, 0.003135,
 0.008191, 0.02237",\
                 "0.0003667, 0.0004518, 0.000687, 0.001345, 0.003174,
 0.008257, 0.02242",\
                 "0.0005104, 0.0005502, 0.0007653, 0.001423, 0.003261,
 0.00832, 0.0224",\
                 "0.0009744, 0.0009964, 0.001041, 0.001585, 0.003421,
 0.008503, 0.02259",\
                 "0.001875, 0.001913, 0.001975, 0.002119, 0.00375,
 0.008838, 0.02296",\
                 "0.003633, 0.003697, 0.003811, 0.004024, 0.004596,
 0.009506, 0.02362",\
                 "0.007095, 0.007179, 0.007403, 0.007758, 0.008299,
 0.01093, 0.02499",\
                 "0.01384, 0.0141, 0.01444, 0.01506, 0.01599, 0.01718,
 0.0278");
       }
   ...
 }

Warning: Line 1912, Cell 'STN_INV_1', pin 'X', related_pin 'A',
 when '', Rule 2, ocv_std_dev_cell_fall value [0.02237], the
 ocv_skewness_cell_fall value [0.02237] should be consistent with
```

Feedback

```
ocv_sigma_cell_fall early/late value [0.02411/-0.001501] (place: 6).
(LBDB-550)
```

What Next

Check the charaterization data which form the distribution and fix the values. These checks could be skipped if thresholds defined by global variable: - lc_lvf_skewness_threshold# if abs(skewness)<lc_lvf_skewness_threshold, then any skewness related checks will be skipped - lc_lvf_sigma_threshold#if abs(sigma_early-sigma_late)<lc_lvf_sigma_threshold, then any sigma related checks will be skipped - lc_lvf_normalized_skewness_threshold# if abs(skewness/std_dev)^3)<lc_lvf_normalized_skewness_threshold, then any skewness related checks will be skipped

See more on UIL-550 man page.

LBDB-551

(warning) The cell referenced by "retention_equivalent_cell" attribute can not be a non-black-box cell.

Description

This message indicated that retention equivalent cell is not a black-box cell. The cell referenced by "retention_equivalent_cell" is desired for a complex retention cell, so the cell should be black-box.

What Next

Check the library source file, correct the retention_equivalent_cell attribute.

LBDB-552

(warning) Can't find pin '%s' in the retention_equivalent_cell '%s'.

Description

For the non-retention cell with retention_equvialent_cell attribute, if any pin has no retention_equvialent_pin attribute, then the pin with same name should be exist in the referenced retention equivalent cell

For the retention equivalent pin referenced by retention_equvialent_pin attribute, the specified pin name should be existed in the retention equivalent cell

The following example shows an instance where this message occurs:

```
cell (cell) {

    retention_equivalent_cell : my_ret_cell;
```

Feedback

```
    pin(D) {
      ...
    }
    pin(E) {
      retention_equivalent_pin : EE;
      ...
    }

    ...

  }

  cell (my_ret_cell) {

    /*
    pin(D) {
      ...
    }
    pin(EE) {
      ...
    }
    */

    ...

  }
```

The following is an example message:

```
Warning: Line 139, Cell 'my_ret_cell', Pin 'D', Can't find pin 'D' in the
 retention_equivalent_cell 'my_ret_cell' (LBDB-552)
Warning: Line 149, Cell 'my_ret_cell', Pin 'E', Can't find pin 'EE'in the
 retention_equivalent_cell 'my_ret_cell' (LBDB-552)
```

What Next

Check the library source file, correct the retention_equivalent_pin attribute.

LBDB-553

(warning) The '%s' %s should not coexist with the '%s' %s.

Description

The first specified attribute/group should not coexist with the second specified attribute/group on the same group. For example, the *char_when_rise* attribute should not be specified with *char_when* attribute on the same timing group.

Feedback

The following example shows an instance where this message occurs:

```
cell(lbdb553) {
      Pin (Y) {
         timing () {
          related_pin : "IN";
            when : "A";
            char_when : "A*B";
            char_when_rise : "A*B";
            ...
         }
         ...
      }
      ...
   }
```

The following is an example message:

```
Warning: Line 2181, Cell 'lbdb553', pin 'Y', The 'char_when_rise'
 attribute should not coexist with the 'char_when' attribute. (LBDB-553)
```

What Next

Check the library source file, and remove the redundant one.

LBDB-555

(Error) The %s attribute is not defined for the library when %s is defined.

Description

This is for when a default attribute is required to be defined for the library but is not defined when certain attribute or group is defined.

The following is an example message:

```
Error: Line 10, The distance_unit attribute is not defined for the
 library when
default_ocv_derate_distance_group or ocv_derate_distance_group is
 defined. (LBDB-555)
```

What Next

Check the library source file, define the default attribute for the library.

LBDB-556

(Error) The '%s' ocv_derate group referenced by %s contains non-distance-based tables.

Feedback

Description

This is for when a default_ocv_derate_distance_group/ocv_distance_group attribute referenced an ocv_derate group, at least one ocv_derate_factor in that ocv_derate group used ocv_table_template that has "variable_1 : path_depth;" defined.

The following is an example message:

```
Error: Line 110, The 'ocv' ocv_derate group referenced by
 ocv_derate_group contains non-distance-based tables. (LBDB-556)
```

What Next

Check the library source file, use ocv_derate group that contain only distance-based tables.

LBDB-557

(error) The '%s' is missing in '%s' group.

Description

Required content is missing for the group.

The following example shows an instance where this message occurs:

```
cell ( test_cell )    {
      ocv_derate(ocv) {
        /* require ocv_derate_factors defined here */
      }
      ... ...
    }
```

The following is an example message:

```
Error: Line 144, The 'ocv_derate_factors' is missing in 'ocv_derate'
 group. (LBDB-557)
```

What Next

Check the library source file to see if you missed the required content for the specified group.

LBDB-558

(error) The '%s' %s group referenced by %s attribute is not found.

Feedback

Description

This message indicates that the attribute cross-referenced by its value an undefined group with specific name.

The following example shows an instance where this message occurs:

```
library(lbdb158) {
cell(IV) {
  ocv_derate_group : a_ocv_derate_not_defined;
  area : 1;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A'";
    timing() {
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}
```

The following is an example message:

```
Error: Line 35, The 'a_ocv_derate_not_defined' ocv_derate group
 referenced by ocv_derate_group attribute
is not found. (LBDB-558)
```

What Next

Add the group if it is missing, or fix the attribute value if it has a typo.

LBDB-559

(warning) The '%s' table used different indices from the '%s' table.

Description

This message occurs when a look-up table used different indices from its master table. Using same indices between the tables is prefered.

Feedback

The following example shows the ocv_sigma_cell_rise table used different indices from cell_rise table:

```
lu_table_template(del_0_2_2) {
  variable_1 : input_net_transition;
  index_1("7.500000,325.000000");
  variable_2 : total_output_net_capacitance;
  index_2("1.100,10.000");
 }
 lu_table_template(del_1_2_2) {
  variable_1 : input_net_transition;
  index_1("17.500000,25.000000");
  variable_2 : total_output_net_capacitance;
  index_2("3.518,12.418");
 }
 ...
 timing() {
   ...
   ocv_sigma_cell_rise(del_1_2_2) {
     values( " 95.492787, 104.196860",\
             " 221.983170, 258.953160");
   }
   cell_rise(del_0_2_2) {
     values( " 95.492787, 104.196860",\
             " 221.983170, 258.953160");
   }
   ...
 }

Warning: Line 191, The 'ocv_sigma_cell_rise' table used different indices
 from the 'cell_rise' table. (LBDB-559)
```

What Next

Charaterize the library using same indices for the look-up tables.

LBDB-560

(error) The pin '%s' specified in the '%s' attribute is not a(n) %s pin.

Description

This error message occurs when a pin specified by this attribute has direction not of required type.

The following example shows an instance where this message occurs: The following example shows the attribute which needs a internal pin.

```
mode_value ( A2I ) {
    mode_value_internal_pin : A1 ;
    when : "EN" ;
```

Feedback

```
    sdf_cond : "EN=1" ;
}
```

The following is an example message:

```
Error: Line 191, The pin 'A1' specified in the 'mode_value_internal_pin'
 attribute is not a(n) internal pin. (LBDB-560)
```

What Next

Specify a correct pin for this attribute.

LBDB-561

(error) The event instance event(%s, %s) is invalid.

Description

The event instance delaration must be referring to a mode_definition and one of its event_defintion.

The following example shows an incorrect event instance:

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      ...
    }
    mode_value(write) {
      ...
    }
    event_definition (I2A) {
        start_mode : "read" ;
        end_mode : "write" ;
    }

  }
    dynamic_current () {
      event(rw, latching);
      ...
    }
  ...
}
```

The following is an example message:

```
Error: Line 206, The event instance event(rw, latching) is invalid.
 (LBDB-561)
```

Feedback

What Next

Check for consistency between mode group and event definitions, and event instance declarations.

LBDB-562

(error) '%s' only allows single pin Boolean-expression.

Description

This error message occurs when Boolean expression contains multiple pins defined for the specified attribute.

The following example shows an incorrect Boolean expression.

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    mode_value(read) {
      ...
    }
    mode_value(write) {
      ...
    }
    event_trigger () {
        trigger_transition : "clock + EN";
    }
  }
  ...
}
```

The following is an example message:

```
Error Line 272, "trigger_transition" only allows single pin
 Boolean-expression. (LBDB-562)
```

What Next

Check the Boolean expression.

LBDB-563

(error) The '%s' must be defined within a mode_defintion group with mutually_exclusive_mode_values is true.

Description

This error message occurs when specified attribute defined within a mode_defintion group which has no attribute mutually_exclusive_mode_values or its value is false.

Feedback

The following example shows an instance where this message occurs: The following example shows an incorrect mode_defintion group.

```
cell(CGNP) {
  area : 1;
  mode_definition(rw) {
    default_mode : "read" ;
    mode_value(read) {
      ...
    }
    mode_value(write) {
      ...
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 540, The 'default_mode' must be defined within a
 mode_defintion
group with mutually_exclusive_mode_values is true. (LBDB-563)
```

What Next

Add mutually_exclusive_mode_values : true or remove the attribute in the mode_defintion group.

LBDB-564

(information) The event instance is defined multiple times for the same group.

Description

This message indicates that you specified multiple event instances for a power group. All the event instances will be retained.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;

  dynamic_current () {
      event(rw, A2I);
      event(rw, I2S);
  }
}
```

The following is an example message:

```
Information: Line 206, The event instance is defined multiple times
        for the same group. (LBDB-564)
```

Feedback

What Next

Please make sure that it is your real intention to have multiple events that apply to the power group.

LBDB-566

(warning) the macro cell has the switch_cell_type: coarse_grain. It is marked as dont_touch and dont_use.

Description

If macro cell has switch_cell_type, it should be fine_grain. This message means that this macro cell has the switch_cell_type: coarse_grain, it is marked as dont_touch and dont_use, it can not be auto inferred by galaxy design tools (e.g. ICC1/ICC2 router).

The following example shows an instance where this message occurs:

```
cell(A) {
    is_macro_cell : true;
    switch_cell_type : coarse_grain;
  }
```

The following is an example message:

```
Warning: Line 1023, Cell 'A', the macro cell has the switch_cell_type:
 coarse_grain. It is marked as dont_touch and dont_use. (LBDB-566)
```

What Next

Correct the "switch_cell_type" to fine_grain for the macro cell.

LBDB-567

(error) The swing of the slew/transition is more than 100% which is not possible.

Description

This error message occurs when (slew_upper_threshold_pct_rise - slew_lower_threshold_pct_rise) / slew_derate_from_library > 100 or (slew_upper_threshold_pct_fall - slew_lower_threshold_pct_fall) / slew_derate_from_library > 100. If a slew after considering the slew_derate factor is more than 100%, such a waveform slew for any characterization waveform points to waveform going beyond the rail to rail swing which is not possible.

The following example shows an instance where this message occurs:

```
library( MyLib ) {
  slew_derate_from_library : 0.5;
  slew_lower_threshold_pct_rise : 20.0;
```

Feedback

```
  slew_upper_threshold_pct_rise : 80.0;
  ...
}
```

From the above information the slew/transition has a swing of more than 100% which is not possible.

The following is an example message:

```
Error: Line 140, The swing of the slew/transition is more than 100% which
 is not possible. (LBDB-567)
```

What Next

correct the slew thresholds or slew derate such that its swing is less than rail-to-rail.

LBDB-567w

(warning) The swing of the slew/transition is more than 100% which is not possible.

Description

This warning message occurs when (slew_upper_threshold_pct_rise - slew_lower_threshold_pct_rise) / slew_derate_from_library > 100 or (slew_upper_threshold_pct_fall - slew_lower_threshold_pct_fall) / slew_derate_from_library > 100. If a slew after considering the slew_derate factor is more than 100%, such a waveform slew for any characterization waveform points to waveform going beyond the rail to rail swing which is not possible.

The following example shows an instance where this message occurs:

```
library( MyLib ) {
  slew_derate_from_library : 0.5;
  slew_lower_threshold_pct_rise : 20.0;
  slew_upper_threshold_pct_rise : 80.0;
  ...
}
```

From the above information the slew/transition has a swing of more than 100% which is not possible.

The following is an example message:

```
Warning: Line 140, The swing of the slew/transition is more than 100%
 which is not possible. (LBDB-567w)
```

What Next

correct the slew thresholds or slew derate such that its swing is less than rail-to-rail.

Feedback

LBDB-568

(warning) Cell '%s' has %d async signal pins, user must specify one async signal pin for level shifter cell or isolation cell with more than 3 pins. It's marked as dont_use, dont_touch.

Description

This warning message occurs when the level shifter or isolation cell has more than 3 pins, but the number of async signal pin is not 1. The cell will be marked as dont_use, dont_touch except one condition for level shift with more than 3 pins. The condition is: isDifferentLS is true, and including 3 input pins, 1 output pin, 1 level shifter enable pin.

The following is an example message:

```
Warning: Line 191, Cell 'LS', Cell 'LS' has 0 async signal pins, user
 must
specify one async signal pin for level shifter cell or isolation cell
 with
more than 3 pins. It's marked as dont_use, dont_touch.
```

What Next

This is only a warning message. No action is required.

You could correct the modeling in the previous example to specify the cell with exact 1 async signal pin.

LBDB-569

(warning) The std cell has the switch_cell_type: fine_grain. It is marked as dont_touch and dont_use.

Description

If std cell has switch_cell_type, it should be coarse_grain. This message means that this std cell has the switch_cell_type: fine_grain, it is marked as dont_touch and dont_use, it can not be auto inferred by galaxy design tools (e.g. ICC1/ICC2 router).

The following example shows an instance where this message occurs:

```
cell(A) {
    switch_cell_type : fine_grain;
  }
```

The following is an example message:

```
Warning: Line 1023, Cell 'A', The std cell has the switch_cell_type:
 fine_grain. It is marked as dont_touch and dont_use. (LBDB-569)
```

Feedback

What Next

Correct the "switch_cell_type" to coarse_grain for the std cell.

LBDB-580

(error) This retention cell is not a valid sequential device in normal mode.

Description

```
When retention pin disable values are appied, the sequential elements do
 not function.
This may be due to user was intended to model a zero-pin retention cell
 but put a wrong
retention_pin attribute on the clock signal.
```

The following example shows an instance where this message occurs:

```
library(test) {
 ...
  cell (zpr) {
    ...
    pin(clk) {
      direction : input ;
      related_ground_pin : vss ;
      related_power_pin : vcc_in ;
      retention_pin(save_restore, 1); /* wrong attribute, should be
 removed */
      ...
    }

    latch(IQ1,IQN1) {
      enable : "!clk" ;
      data_in : "d" ;
      power_down_function : "!vcc+vss" ;
    }
    latch(IQ2,IQN2) {
      enable : "clk" ;
      data_in : "IQ1" ;
      power_down_function : "!vcc_in+vss" ;
    }

    retention_condition() {
      required_condition : "!clk";
      power_down_function : "!vcc+vss" ;
    }

    ...
  }
}
```

The following is an example message:

```
Error: Line 3, Cell 'zpr', This retention cell is not a valid sequential
 device in normal mode.
```

What Next

```
Remove the "retention_pin" attribute in this cell.
```

LBDB-581

(warning) The '%s' pg_pin '%s' is using '%s' logic in power_down_function.

Description

```
The pg_pin specified as power pg_type should have negative logic in
 power_down_function;
The pg_pin specified as ground pg_type should have positive logic in
 power_down_function.

This message indicate that the pg_pin logic in the power_down_function is
 wrong.
```

The following example shows an instance where this message occurs:

```
library(test) {
 ...
  cell (a) {
    ...
    pg_pin(vdd) {
      pg_type : primary_power;
      ...
    }
    pg_pin(vss) {
      pg_type : primary_ground;
      ...
    }

    pin(out) {
      power_down_function : "vdd+vss" ;
      ...
    }

    ...
  }
}
```

The following is an example message:

```
Error: Line 300, Cell 'a', pin 'out', The 'power' pg_pin 'vdd' is using
 'positive' logic in power_down_function.
```

Feedback

What Next

Correct the pg_pin logic in power_down_function.

LBDB-582

(error) The 'true' is_pass_gate attribute is conflicting with \n \tthe 'true' is_inverting attribute for the '%s' group.

Description

This message indicates you specified 'true' is_pass_gate attribute and 'true' is_inverting attribute simltaneously for the same CCB (i.e., the same ccsn_first_stage, ccsn_last_stage, input_ccb or output_ccb group), which causes conflict.

The following example shows an instance where this message occurs.

```
library (test) {
   ...
   cell(inv) {
     ...
     pin(A) {
       direction : input;
       input_ccb(iccb) {
         is_inverting : true;
         is_pass_gate : true;
         ...
       }
       ...
    }
    ...
 }
```

The following is an example message:

```
Error: Line 74, Cell 'inv', pin 'A', The 'true' is_pass_gate attribute is
 conflicting with
the 'true' is_inverting attribute for the 'input_ccb' group. (LBDB-582)
```

What Next

Change the library file by either remove the is_pass_gate attribute from the CCB or specify 'false' is_inverting attribute for the CCB.

LBDB-586

(error) This timing group is missing NLDM '%s' data to work with 'propagating_ccb' attribute at line %u.

Feedback

Description

In the referenced ccs noise data modeling (hereinafter "ccb modeling"), there is a synergy between NLDM delay data and input_ccb/output_ccb data referenced by the attribute propagating_ccb. However, a required data (cell_rise, cell_fall, rise_transition, fall_transition) is not found, as indicated by the message.

Examples

Error: Line 1564, Cell 'INV_X8M_A9TL', pin 'Y', This timing group is missing NLDM 'cell_rise' data to work with 'propagating_ccb' attribute at line 2815. (LBDB-586)

What Next

Add missing data.

LBDB-587

(warning) attribute '%s'. Input slew (vector/index_1) not matching between '%s' at line %u of 'input_ccb' stage (line %u) and '%s' at line %u of 'output_ccb' stage (line %u). Mismatch %s.

Description

In a two-stage propagation_ccb usage, both referenced ccb stages must have the same set of input slew values (vector/index_1 of respective output_voltage_rise/fall groups), matching in size and values.

Warning: Line 5085, Cell 'AND2_X2M_A9TL', pin 'Y', attribute 'propagating_ccb'.
Input slew (vector/index_1) not matching between 'output_voltage_rise' at line 3118 of 'input_ccb' stage (line 3017) and 'output_voltage_fall' at line 6424 of 'output_ccb' stage (line 6382). Mismatch in size. (LBDB-587)

What Next

Correct characterization procedure.

LBDB-588

(error) attribute '%s'. The referenced '%s' stage at line %u has more than one load value in its 'vector/index_2' of '%s' at line %u.

Description

The issue is related to a two-stcge input_ccb/output_ccb configuration. The input_ccb stage has more than one index_2 value ("total_output_net_capacitance") among the vectors of its output_voltage_rise/fall group. However, this stage drives a fixed internal oad

Feedback

(i.e. the output ccb stage), no internal load variation is currently supported. Hence there can only be one index_2 value.

This problem may be caused by the use of the same input_ccb in a single-stage propagating_ccb of another timing group.

Examples

Error: Line 7492, Cell 'custom_cell_xwy', pin 'nx2', attribute 'propagating_ccb'. The referenced 'input_ccb' stage at line 488 has more than one load value in its 'vector/index_2' of 'output_voltage_rise' at line 561. (LBDB-588)

What Next

Correct the characterization procedure.

LBDB-589

(warning) The voltage value of middle 3 points should be consistent with that of delay/slew measure points in %s group.

Description

In referenced CCB noise modeling, the voltage value of middle three points (stored in attribute "values") in each vector group of output_voltage_rise group should be slew_lower_threshold_pct_rise, output_threshold_pct_rise, slew_upper_threshold_pct_rise of Vdd, and for output_voltage_fall group, slew_upper_threshold_pct_fall, output_threshold_pct_fall, slew_lower_threshold_pct_fall of Vdd.

The following example shows an instance where this message occurs:

```
library("test_library") {
  ...
  output_threshold_pct_fall : 50 ;
  output_threshold_pct_rise : 50 ;
  slew_lower_threshold_pct_fall : 30 ;
  slew_lower_threshold_pct_rise : 30 ;
  slew_upper_threshold_pct_fall : 70 ;
  slew_upper_threshold_pct_rise : 70 ;
  voltage_map(VDD, 0.765);
  ...

  cell(BUFX0P5BV0LI35P) {
    ...
    pin(A) {
      ...
      related_power_pin : VDD ;

      input_ccb(INVX1BV0LI35P__nco_0_FR_RF:a:z) {
```

Feedback

```
        ...
        output_voltage_fall() {

          vector(ccsn_wf1x1x5) {
            index_1("0.001000");
            index_2("0.000500");
            index_3("0.00430831, 0.00566391, 0.00721167, 0.00889193,
 0.0114251");
            values("0.688500, 0.535500, 0.482500, 0.229500, 0.076500");
          }
          ...
        }
        ...
      }
      ...
    }
    ...
  }
  ...
}
```

The following is an example message:

```
Warning: Line 1193, Cell 'BUFX0P5BV0LI35P', pin 'A', The voltage value of
 middle
 3 points should be consistent with that of delay/slew measure points in
output_voltage_fall group. (LBDB-589)
```

What Next

Fix the mistake. In the example above, the middle value should be: 0.382500.

LBDB-590

(warning) There is only %d index value(s) in '%s' for this %s table.

Description

To be able to calculate value that not on grid, there's minimal index values requirement on specific tables.

For pg_current in dynamic_current, the indices except time (the last index) in all vectors will be grouped and checked. If it has only one index, which usually is input_net_transition, at least three index values are needed. If it has multiple indices, then for each index, at least two index values are needed.

The following example has only one input_net_transition value of 5.1 in the pg_current table, and two total_output_net_capacitance values of 0.1 and 0.3.

```
pg_current(V2) {
        vector(test_2) {
```

Feedback

```
          reference_time : 93.2;
          index_1("5.1");
          index_2("0.1");
          index_3("8.2 8.3 9.0");
          values("3.78 92.4 100.1");
         }
        vector(test_2) {
          reference_time : 93.2;
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
         }
```

```
The following is an example message:
Warning: Line 518, Cell 'OR2', There is only 1 index value(s) in
 'input_net_transition' for this pg_current table. (LBDB-590)
```

What Next

Add more index values.

LBDB-591

(warning) The pg_current values are irregular, peak point is at beginning or end.

Description

This message is issued since the current waveform("values(...)") in the pg_current vector is abnormal, it has the peak value at beginning or end. Note: peak is the largest absolute value. This constraint will only be applied while output is switching, and if the peak value is under 1uA, which is closing to leakage current, the constraint is not needed.

The following example has the peak value at end.

```
vector(test_1) {
     reference_time : 23.7;
     index_1("0.8");
     index_2("0.7");
     index_3("10.4");
     index_4("8.2 8.5 9.1 9.4 9.8");
     values("0.7 34.6 3.78 92.4 100.1");
    }
```

The following is an example message:

```
Warning: Line 520, Cell 'OR2', The pg_current values are irregular, peak
 point is at beginning or end. (LBDB-591)
```

What Next

Check the characterization data.

Feedback

LBDB-592

(warning) Too few value points in this vector, at least '%d' values needed.

Description

This message is issued since the current waveform("values(...)") in the pg_current vector has too few points. At least three points are needed. The only exception is that all current values are under the threshold (1uA), which is closing to leakage current, then the requirement is not needed.

The following example has the peak value at end.

```
vector(test_1) {
     reference_time : 23.7;
     index_1("0.8");
     index_2("0.7");
     index_3("10.4");
     index_4("8.2 8.5");
     values("0.7 34.6");
    }
```

The following is an example message:

```
Warning: Line 520, Cell 'OR2', Too few value points in this vector, at
 least '3' values needed. (LBDB-592)
```

What Next

Check the characterization data.

LBDB-593

(error) value list of '%s' attribute not full range, or not monotonically %s.

Description

The value list of this attribute is either not full range or monotonic. The values are required to:

start at 0.0, and increase monotonically to 100.0, or

start at 100.0, and decrease monotonically to 0.0

The following example has two issues: the 3rd value is less than the 2nd, and the last one is not 100.0;

```
receiver_trip_threshold_pct_rise(0.0, 40.0, 30.0, 60.0, 75.0,
 85.0, 99.0);
```

Feedback

The following is an example message:

```
Error: Line 74, value list of 'receiver_trip_threshold_pct_rise'
 attribute not full range, or not monotonically increasing.
```

What Next

Fix the problem.

LBDB-594

(error) Unnamed CCB stage.

Description

All input_ccb & output_ccb groups must be given names. Named ccsn stages are placed only at pin group level. They are referenced, if needed, in acitve_input_ccb, active_output_ccb, & propagating_ccb attributes at timing group level.

The following "input_ccb" example does not have a name.

```
library (test) {
   ...
   cell(inv) {
      ...
     pin(A) {
       direction : input;
       input_ccb() {
         ...
       }
       ...
    }
    ...
 }
```

The following is an example message:

```
Error: Line 74, Cell 'inv', pin 'A', Unnamed CCB stage. (LBDB-594)
```

What Next

Add name to the input_ccb or output_ccb group.

LBDB-595

(error) CCB stage name '%s' already used by the %s group at line %u.

Feedback

Description

The name shown in the message is already used by another input_ccb or output_ccb group in the same pin group. Please replace it with a unique name, and update affected active_input_ccb, active_output_ccb, and propagating_ccb attributes.

The following example shows an instance where this message occurs. The CCB stage name *b* is used twice under pin b:

```
pin(b) {
     direction : inout;
     input_ccb(b) {
       ...
     }
     output_ccb(b) {
       ...
     }
     ...
   }
```

The following is an example message:

```
Error: Line 1813, Cell 'dup_names', pin 'I', CCB stage name 'b' already
used by the input_ccb group at line 1476. (LBDB-595)
```

What Next

Modify to make sure names are unique. For example:

```
pin(b) {
     direction : inout;
     input_ccb(b_in) {
       ...
     }
     output_ccb(b_out) {
       ...
     }
     ...
   }
```

LBDB-596

(error) The value of min_capacitance is greater than that of max_capacitance.

Description

This information occurs when the value of min_capacitance is greater than that of max_capacitance.

Feedback

The following example shows an instance where this message occurs:

```
pin (Z) {
  direction : "output";
  function : "A";
  output_signal_level : "VDD";
  max_capacitance : 0.057841;
  min_capacitance : 0.557841;
 }
```

The following is an example message:

```
Error: Line 258, Cell 'BUFX1', pin 'Z', The value of min_capacitance is
 greater than that of max_capacitance. (LBDB-596)
```

What Next

Make sure the value of min_capacitance is not greater than that of max_capacitance.

LBDB-597

(error) CCB group '%s' has been utilized by attribute '%s' at line %u.

Description

For a given timing group, a particular CCB stage group may only be referenced once among attributes propagating_ccb, active_input_ccb, and active_output_ccb. It is an error to be referenced more than once.

The following example shows an instance where this message occurs. The input_ccb group *ccb_a* is referenced twice in the same timing group.

```
library(test) {
    cell test(inv) {
      pin(a) {
        direction : in;
          input_ccb(ccb_a) {
          ...
          }
        ...
      }
      pin(out) {
        direction : out;
        output_ccb(ccb_out) {
          ...
          }
        timing () {
          related_pin : in;
          active_input_ccb("ccb_a");
          propagating_ccb("ccb_a", "ccb_out");
        }
      }
```

Feedback

```
    }
  }
```

The following is an example message:

```
Error: Line 3209, Cell 'inv', pin 'ZN', CCB group 'ccb_a' has been
 utilized by attribute 'propagating_ccb' at line 3210. (LBDB-597)
```

What Next

Remove the incorrect usage.

LBDB-598

(error) CCB group '%s' referenced by attribute '%s' not found in pin '%s' at line %u.

Description

A CCB stage referenced in attributes propagating_ccb, active_input_ccb, and active_output_ccb must be located at the input pin (related_pin) or the output pin, depending on the context.

The following example shows an instance where this message occurs:

```
library(test) {
    cell test(and2) {
      pin(a) {
        direction : in;
        input_ccb(ccb_a) {
        ...
        }
      ...
      }
      pin(b) {
        direction : in;
        input_ccb(ccb_b) {
        ...
        }
      ...
      }
      pin(o1) {
        direction : out;
        output_ccb(ccb_o1) {
          ...
          }
        ...
      }
      pin(o2) {
        direction : out;
        output_ccb(ccb_o2) {
          ...
          }
```

Feedback

```
        timing () {
          related_pin : a;
          propagating_ccb("ccb_a", "ccb_o1");
        }
      }
    }
  }
```

The following is an example message:

```
Error: Line 759, Cell 'and2', pin 'o2', CCB group 'ccb_o1' referenced by
 attribute 'propagating_ccb' not found in pin 'o2' at line 70. (LBDB-598)
```

What Next

Fix the mistake. In the example above, attribute propagating_ccb should be specified as:

```
propagation("ccb_a", "ccb_o2");
```

LBDB-599

(error) In attribute '%s', ccb '%s' referenced is of the wrong type.

Description

The ccb referenced is not of the correct type for one of the following reasons:

1. The 1st parameter of propagating_ccb, or all parameters in active_input_ccb must reference a input_ccb of the related pin, not a output_ccb.
2. The 2nd parameter of propagating_ccb, if present, must reference a output_ccb in the current (output/inout) pin, not a input_ccb.
3. Finally, note that only one ccb can drive the output. If the attribute mentioned is 'active_output_ccb', remove the offending output_ccb because:

1. Another output_ccb has already been given in the same attribute. In fact, the only one valid possibility of more than 1 output_ccb's being referenced is the two output_ccb's in which one has the stage_type:pull_up and the other has the stage_type:pull_down.
2. The 'propagating_ccb' attribute is present.

The following example shows an instance where this message occurs:

```
library(test) {
    cell test(complex) {
      pin(a) {
        direction : inout;
        input_ccb(ccb_a_in) {
        ...
        }
        output_ccb(ccb_a_out) {
```

```
        ...
        }
      ...
      }
      pin(out) {
        direction : out;
        output_ccb(ccb_o2) {
          ...
          }
        timing () {
          related_pin : a;
          active_input_ccb("ccb_a_out");
        }
      }
    }
  }
```

The following is an example message:

```
Error: Line 3175, Cell 'complex', pin 'out', In attribute
 'active_input_ccb', CCS noise stage 'ccb_a_out' referenced is of the
 wrong type. (LBDB-599)
```

What Next

Fix the mistake.

LBDB-600

(error) The '%s' direction cannot be specified on a\n \tpin.

Description

This message indicates that you specified an incompatible direction value on a pin. Library Compiler fails if the direction value includes the following combinations:

```
* tristate
```

The following example shows an instance where this message occurs:

```
cell(lbdb600) {
    area : 2;
    pin(A) {
      direction : tristate;
      capacitance : 1.0;
    }
    ...
  }
```

Feedback

The following is an example message:

```
Error: Line 84, The 'tristate' direction cannot be specified on a
       pin. (LBDB-600)
```

What Next

Refer to the "Library Compiler User Guide" for direction information. Remove the incompatible values of the direction attribute.

LBDB-601

(error) related_pin is illegal in the timing group. \ Timing arc info is missing.

Description

This message indicates that you specified an illegal related_pin in a timing group.

The following example shows an instance where this message occurs:

```
timing() {
                /* noise immunity */
                noise_immunity_high(noise5x5){
                    index_2("0.362,0.725,1.087,1.449,1.812");
                    values("0.733,1.073,1.412,1.752,2.092",\
                           "0.873,1.214,1.554,1.894,2.234",\
                           "1.095,1.442,1.787,2.132,2.477",\
                           "1.298,1.648,1.996,2.343,2.691",\
                           "1.703,2.060,2.414,2.766,3.119");
                }
                related_pin: "a";
            }
```

The following is an example message:

```
Error: Line 120, related_pin is illegal in the timing group. \
 Timing arc info is missing.  (LBDB-601)
```

What Next

Refer to the "Library Compiler User Guide" for related_pin information.

LBDB-602

(warning) The units of time, capacitance, voltage and current are not consistent.

Description

This message indicates that you specified an inconsistent units in the library.

Feedback

The following example shows an instance where this message occurs:

```
library (mi333) {
    ...
   time_unit                    : "1ns";
   voltage_unit                 : "1mV";
   current_unit                 : "1mA";
   pulling_resistance_unit      : "1kohm";
   capacitive_load_unit  (1, pf);
    ...
```

The following is an example message:

```
Warning: Line 120, The units of time, capacitance, voltage and current
 are not consistent. (LBDB-602)
```

What Next

Refer to the "Library Compiler User Guide" for unit information. Modify the realted unit values to make them consistent.

LBDB-603

(error) The '%s' attribute cannot be supplied a \n \tnonpositive value (%d).

Description

This message indicates that the specified attribute cannot have a nonpositive value.

The following example shows an instance where this message occurs:

```
orders ( 0, 2, 3 );
```

The following is an example message:

```
Error: Line 18, The 'orders' attribute cannot be supplied a
       nonpositive value (0) (LBDB-603)
```

What Next

Change the value of the attribute to positive in the technology library file.

LBDB-604

(error) '%s' attribute should be less than '%s' attribute.

Description

This message indicates that the specified attributes are not consistent.

Feedback

The following example shows an instance where this message occurs:

```
slew_lower_threshold_pct_rise: 80.0
   slew_upper_threshold_pct_rise: 20.0
```

The following is an example message:

```
Error: Attribute 'slew_lower_threshold_pct_rise' should be less
       than 'slew_upper_threshold_pct_rise'. (LBDB-604)
```

What Next

Change the value of the attributes to be consistent in the technology library file.

LBDB-605

(warning) The attribute '%s' is not specified.

Description

This message indicates that an attribute is missing.

The following example shows an instance where this message occurs:

```
slew_lower_threshold_pct_rise: 20.0
```

The following is an example message:

```
Warning: Line 18, The attribute 'slew_lower_threshold_pct_rise' is not
 specified. (LBDB-605)
```

What Next

Either add the missing attribute to the technology library or ignore the message.

LBDB-606

(error) The invalid '%s' value is encountered\n \ton the '%s' attribute.

Description

This message indicates that you specified an invalid attribute's value

The following example shows an instance where this message occurs:

```
fall_propagation ( table4x6 ) {
   index_1 ("2.00e+02 2.50e+02 3.50e+02 4.00e+02 ") ;
   index_2 ("4.48e-02 8.96e-02 1.34e-01 1.79e-01 2.24e-01 2.69e-01 ");
   values ("Look.here 9.56e+01 1.15e+02 1.34e+02 1.52e+02 1.71e+02 ", \
           "9.38e+01 1.20e+02 1.45e+02 1.67e+02 1.89e+02 2.10e+02 ", \
           "1.01e+02 1.32e+02 1.58e+02 1.83e+02 2.07e+02 2.29e+02 ", \
```

Feedback

```
            "1.04e+02 1.43e-93 1.43e-93 1.43e-93 2.75e+226 9.30e+254 " ) ;
}
```

The following is an example message:

```
Error: Line 85, The invalid 'Look.here' value is encountered
        on the 'values' attribute. (LBDB-606)
```

What Next

Check the library source file, and correct the problem.

LBDB-607

(warning) The pin '%s' does not have a internal_power group.

Description

For a signal pin, it should have one internal_power table.

The following example shows an instance where this message occurs:

```
cell ( cell1 ) {
    pg_pin (VDD) {
      pg_type : "primary_power";
      related_bias_pin : "VDDB";
      voltage_name : "VDD";
    }
    pg_pin (VDDB) {
      pg_type : "nwell";
      physical_connection : "device_layer";
      voltage_name : "VDDB";
    }
    pg_pin (VSS) {
      pg_type : "primary_ground";
      related_bias_pin : "VSSB";
      voltage_name : "VSS";
    }
    pg_pin (VSSB) {
      pg_type : "pwell";
      physical_connection : "device_layer";
      voltage_name : "VSSB";
    }
     pin(A) {
        ...
     }
     pin(B) {
        ...
     }
     pin ( CP ) {
        direction : input ;
        related_bias_pin : "VDDB VSSB";
```

Feedback

```
        related_ground_pin : "VSS";
        related_power_pin : "VDD";

         ...
      }
      ...
```

To fix the problem, add internal_power group under pin CP.

```
internal_power () {
        related_pg_pin : "VDD";
        when : "(!A&B)";
        power ("power_1") {
          index_1("0.002, 0.0263908, 0.0995546, 0.2215, 0.392218,
 0.611718, 0.88");
          values("0.0002916, 0.0005488, 0.0015848, 0.0024696, 0.0029070,
 0.0031031, 0.0032115");
        }

}
```

The following is an example message:

```
Warning: Line 126, The pin 'CP' does not have a internal_power group.
 (LBDB-607)
```

What Next

Add the internal_power table.

LBDB-608

(Warning) Library cell '%s' has a valid function-id,\n \tbut it has also been annotated with the user_function_class\n \tattribute. Resolving this conflict by ignoring the\n \tuser_function_class attribute for this library cell.

Description

The specified cell has been annotated with the *user_function_classr* attribute even though it has a valid function-id. Library Compiler can generate a function-id for most cells in a technology library. However, there may be a few complex sequential or combinational cells that Library Compiler cannot successfully generate a function-id for. In addition, some black-box cells in the library do not have any function information. The *user_function_class* attribute is intended for such cells that otherwise would not have a function-id. The *user_function_class* attribute is not intended for library cells that already have a valid function-id.

Feedback

What Next

This warning message indicates that the *user_function_class* attribute for this library cell will be ignored. No further action is required. To turn off this warning message in the future, make sure that a *user_function_class attribute* is not set on this library cell.

LBDB-609

(Warning) Library cells '%s' and '%s' have\n \tdifferent pin information, but they have been assigned the\n \tsame user_function_class. Resolving this conflict by ignoring\n \tthe user_function_class attribute on the latter library cell.

Description

Two library cells that are assigned the same *user_function_class* attribute should have the exact same pin information. That is, they must have the same number of pins and the same pin names. This requirement is necessary so that Design Compiler can establish pin-to-pin correspondence between two cells in the same *user_function_class* when it replaces a reference to one library cell by a reference to the other library cell.

This warning message indicates that an inconsistency was found between the pin information of two library cells in the same *user_function_class*. To resolve this conflict, the *user_function_class* attribute for the second library cell will be ignored.

What Next

This warning message indicates that the *user_function_class* attribute for the second library cell will be ignored. No further action is required. To turn off this warning message in the future, make sure that all library cells in a given *user_function_class* attribute have the same pin information.

LBDB-610

(warning) The units of %s are not consistent.

Description

This message indicates that you specified an inconsistent units in the library.

The following example shows an instance where this message occurs:

```
library (mi333) {
    ...
   time_unit                    : "1ns";
   voltage_unit                 : "1V";
   current_unit                 : "1mA";
   resistance_unit              : "1kohm";
   capacitive_load_unit  (1, pf);
    ...
```

Feedback

The following is an example message:

```
Warning: Line 120, The units of time, capacitance, resistance are not
 consistent. (LBDB-610)
```

What Next

Refer to the "Library Compiler User Guide" for unit information. Modify the realted unit values to make them consistent.

LBDB-611

(warning) The '%s' %s group is not used by any %s pin in the library.

Description

This message indicates that the library pins does not use the defined input/output voltage groups.

The following example shows an instance where this message occurs:

```
input_voltage(CMOS) {
    vil : 1.5;
    vih : 3.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }

  input_voltage(CMOS) {
    vil : 2.5;
    vih : 4.5;
    vimin : -0.3;
    vimax : VDD + 0.3;
  }
```

The following is an example message:

```
Error: Line 31, The 'CMOS' input_voltage  group is not used by any input
 pin in the library. (LBDB-611)
```

What Next

For input_voltage group, add "input_voltage" attrribute to input library pins. For output_voltage group, add "output_voltage" attrribute to output library pins.

LBDB-612

(information) The '%s' attribute value is\n \t %s (%3.1f).

Feedback

Description

This message indicates that you specified an attribute value that maybe out of the accepted range. The value is either less than the minimum value or greater than the maximum value. Unlike LBDB-163, it does not reset the value.

The following example shows an instance where this message occurs:

```
height_coefficient : -0.01;
```

In this case, the height_coefficient's value -0.01 is less than the minimum accepted value 0.0. However, it is not reset.

The following is an example message:

```
Warning: Line 109, The 'height_coefficient' attribute value is
         less than 0.0. (LBDB-612)
```

LBDB-612w

(warning) The '%s' attribute value (%g) is\n \t %s (%g).

Description

This message indicates that you specified an attribute value that maybe out of the accepted range. The value is either less than the minimum value or greater than the maximum value. Unlike LBDB-163, it does not reset the value.

The following example shows an instance where this message occurs:

```
voltage_map(VDDL, 1.00) ;
  ...
  cell (A) {
    ...
    pin(I)  {
      ...
      input_voltage_range (0.4, 3.3);
      related_power_pin : VDDL;
      max_input_delta_overdrive_high : 0.05;
      max_input_delta_underdrive_high : 0.8;
    }
  }
```

In this case, the max_input_delta_underdrive_high's value (0.8) is greater than the input_voltage_range allowed (0.6, which is the difference of voltage value between related_power_pin and the lower bound of input_voltage_range). However, it is not reset.

The following is an example message:

```
Warning: Line 79, The 'max_input_delta_underdrive_high' attribute value
 (0.8) is
         greater than the input_voltage_range allowed (0.6). (LBDB-612w)
```

Feedback

What Next

Change the attribute value to satisfy the value range.

LBDB-613

(error) The '%s' group requires the '%s' %s.\n \tEither the attribute(or group) is missing or the attribute(or group) has an invalid value.

Description

This message indicates a group is missing, or you specified a group without one of its required attributes(or groups, or vectors). Library Compiler rejects the attribute(group) definition if the attribute(group) is missing, or exists but has an invalid value.

The following example shows an instance where this message occurs:

```
memory() {
        type : random;
        address_width : 10;
        word_width : 8;
      }
```

In this case, the 'type' has an invalid value. To fix the problem, assign 'rom' or 'ram' to the type.

The following is an example message:

```
Error: Line 27, The 'memory' group requires the 'type' attribute.
 Either the attribute(or group) is missing or the attribute(or group)has
 an invalid value. (LBDB-613)
```

Here is another example shows where this message occurs:

```
ccsn_last_stage() {
          output_voltage_fall () {
          }
          propagated_noise_low () {
          }
          propagated_noise_high () {
          }
 }
```

In this case, 'output_voltage_rise' group is missing. In addition, 'vector' data tables are also missing for output_voltage_fall, propagated_noise_low, propagated_noise_high. These need to be added to fix the problem.

The following is an example message.

```
Error: Line 54, The 'ccsn_last_stage' group requires the
 'output_voltage_rise' group.
```

```
 Either the attribute(or group) is missing or the attribute(or group)has
 an invalid value. (LBDB-613)
Error: Line 54, The 'ccsn_last_stage' group requires the
 'output_voltage_fall' group.
 Either the attribute(or group) is missing or the attribute(or group)has
 an invalid value. (LBDB-613)
Error: Line 54, The 'ccsn_last_stage' group requires the
 'propagated_noise_low' group.
 Either the attribute(or group) is missing or the attribute(or group)has
 an invalid value. (LBDB-613)
Error: Line 54, The 'ccsn_last_stage' group requires the
 'propagated_noise_high' group.
 Either the attribute(or group) is missing or the attribute(or group)has
 an invalid value. (LBDB-613)
```

What Next

Change the library file by adding the missing attribute(or group, or vector) to the group.

LBDB-614

(error) The '%s' has a count of %d, which does not match\n \tthe number of "%s" specified.

Description

The specification of the variables implied the number of indices of a template (or template domain).

The following example shows an instance where this message occurs:

```
lu_table_template(basic_template) {
        variable_1 : input_net_transition;
        index_1 ("0.1, 1.2, 2.3, 3.4");
        index_2 ("0.1, 1.2, 2.3, 3.4");
  }
```

The following is an example message:

```
Error: Line 160, The 'index_*' have a count of 2, which does not match
        the number of 'varible_*' specified. (LBDB-614)
```

What Next

Check the library source file, and make the number of variables and indices to\n \tthe same.

LBDB-615

(warning) Connect pin '%s' to the default_power_supply '%s'\n \tdefined in the power_supply() group in library.

Feedback

Description

Either the input_signal_level or the output_signal_level attribute is missing in a pin within a multiple power supply cell. By default, LC connect this pin to the default_power_supply defined in the power_supply() group in library.

The following example shows an instance where this message occurs:

```
power_supply() {
        default_power_rail : VDD0;
        power_rail(VDD1, 5.0);
        power_rail(VDD2, 3.3);
    }

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  rail_connection(PV1, VDD1);
  rail_connection(PV2, VDD2);
  pin(A) {
    direction : input;          /* missing input_signal_level attribute,
 will use default VDD0 */
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A";
    output_signal_level : VDD2;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
}
```

The following is an example message:

```
Warning: Line 96, Connect pin 'A' to the default_power_supply 'VDD0'
       defined in the power_supply() group in library. (LBDB-615)
```

What Next

Check the library source file to see if you missed the input_signal_level or the output_signal_level attributes.

Feedback

LBDB-616

(error) Found the timing arc '%s' has lookup table or poly template \n \twhich is more than %s dimensional in a '%s' timing group in the library

Description

The related_pin and constraint_pin are the same in the specified timing group; therefore, there cannot be a two-dimension or more lookup table/poly template based on related_pin_transition and constraint_pin_transition because they are the same pin and one pin cannot have two different values at the same time.

Note that the min_pulse_width timing group can be one- or two-dimensional, because the arc can be indexed by the output load.

The following example shows an instance where this message occurs:

```
lu_table_template  (table_2)   {
   variable_1  :  constrained_pin_transition  ;
   variable_2  :  related_pin_transition  ;
   index_1 ("0.00, 0.25, 0.50") ;
   index_2 ("0.00, 0.50, 2.00") ;
}

 ...

    timing() {
      related_pin : CP ;
      timing_type : min_pulse_width ;
      rise_constraint(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (
                  "4.0, 5.0, 6.0"
                  "4.2, 5.2, 6.2"
                  "4.4, 5.4, 6.4"
          );
      }
      fall_constraint(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (
                  "4.0, 5.0, 6.0" \
                  "4.2, 5.2, 6.2" \
                  "4.4, 5.4, 6.4" \
          );
      }
```

Feedback

The following is an example message:

```
Error: Line 160, Found the timing arc 'rise_constraint' has lookup table
 or poly template which is more than one dimensional in a min_pulse_width
 timing group in the library (LBDB-616)
```

What Next

Modify the timing arc based on a one-dimensional lookup table or poly template.

LBDB-617

(warning) The related pin in a '%s' timing group is specified as '%s', not \n \t the pin '%s' itself. It is reset to pin '%s'.

Description

In the timing group reported, since the related_pin and constraint_pin are the same, the related_pin attribute is optional and has be to set to the pin itself.

The following example shows an instance where this message occurs:

```
pin(CP) {
   ...
    timing() {
      related_pin : D ;
      timing_type : min_pulse_width ;
      rise_constraint(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
                  "4.2, 5.2, 6.2"\
                  "4.4, 5.4, 6.4"\
          );
      }
      fall_constraint(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
                  "4.2, 5.2, 6.2"\
                  "4.4, 5.4, 6.4"\
          );
      }
  }

need to delete related_pin attribute or set it as
related_pin : CP ;
```

Feedback

The following is an example message:

```
Warning: Line 160, The related pin in a min_pulse_width timing group
 is specified as 'D', not the pin 'CP' itself. It is reset to pin 'CP'.
 (LBDB-617)
```

What Next

Either delete the related_pin attribute or set the attribute to the pin's name.

LBDB-618

(error) The min/max_clock_tree_path timing arc contains illegal rise/fall_propagation group.

Description

In a min/max_clock_tree_path timing arc, only cell_rise group or cell_fall group or both are allowed

The following example shows an instance where this message occurs:

```
pin(CP) {
   ...
    timing() {
      related_pin : CLK ;
      timing_type : min_clock_tree_path ;
      rise_propagation(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
          );
      }
      fall_propagation(table_2) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
          );
      }
  }

need to delete both rise_propagation and fall_propagation lookup table
 and replace with
cell_rise and cell_fall lookup tables
```

The following is an example message:

```
Warning: Line 160, the min/max_clock_tree_path timing arc containts
 illegal rise/fall_progagation group (LBDB-618)
```

Feedback

What Next

Delete the illegal rise/fall_propagation group

LBDB-619

(error) The '%s' attribute cannot be specified on the %s %s.

Description

This error message occurs when you specify an invalid attribute for an object. As shown in the following example, the *output_signal_level_high* attribute is invalid for a pin object, causing the error message:

```
cell(lbdb600) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;
      output_signal_level_high : 1.2;
      ...
    }
    ...
  }

Error: Line 84, The 'output_signal_level_high' attribute cannot be
 specified on the
       pin 'A'. (LBDB-619)
```

What Next

Remove the attribute from the pin and rerun the command.

LBDB-619w

(warning) The '%s' attribute cannot be specified on the %s %s.

Description

This warning message occurs when you specify an invalid attribute for an object. As shown in the following example, the *output_signal_level_high* attribute is invalid for a pin object, causing the warning message:

```
cell(lbdb600) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;
      output_signal_level_high : 1.2;
      ...
```

```
    }
    ...
  }
```

```
Warning: Line 84, The 'output_signal_level_high' attribute cannot be
 specified on the
       pin 'A'. (LBDB-619w)
```

What Next

Remove the attribute from the pin and rerun the command.

LBDB-620

(warning) The lookup table domain '%s' is defined multiple times\n \twithin '%s'. Using the last one encountered.

Description

This message indicates that the same lookup table domain has been defined for multiple times within one timing/power arc. In the case of a domain conflict, Library Compiler ignores all except the last domain encountered during the compilation. The compiled database contains the last domain only.

The following example shows an instance where this message occurs:

```
cell_rise(li7X7){
     domain(D1) { ... }
     domain(D1) { ... }
     domain(D2) { ... }
   }
```

The following is an example message:

```
Warning: Line 987, The lookup table domain 'D1' is defined multiple times
         within 'cell_rise'. Using the last one encountered. (LBDB-620)
```

What Next

Make sure that only define one lookup table for each domain for each timing/power arc.

LBDB-621

(error) Invalid calc_mode '%s' is detected. This name must be\n \tunique among domains within one lu_table_template.

Description

This message indicates a duplicate calc_mode defined among domains within one lu_table_template.

Feedback

The following example shows an instance where this message occurs:

```
lu_table_template(li7X7){
    domain(D1) {
      calc_mode : "CM1";
      . . .
    }
    domain(D2) {
      calc_mode : "CM1";
      . . .
    }
  }
```

The following is an example message:

```
Error: Line 56, Invalid calc_mode 'CM1' is detected. This name must be
        unique among domains within one lu_table_template. (LBDB-621)
```

What Next

Change the name of the pin, bus, bundle, rail_connection in the technology library.

LBDB-622

(error) The '%s' attribute is missing for the %s %s.

Description

This error message occurs because either the *max_input_noise_width* or the *min_input_noise_width* attribute is missing when both attributes are required.

This message also occurs when *input_signal_level* and *output_signal_level* are not defined in the input/output pin of a level shifter or isolation cell.

What Next

Check the library source file, and add the missing attribute.

LBDB-623

(error) The '%s' attribute is larger than the %s '%s' %sfor the %s %s.

Description

This error message occurs when the *min_input_noise_width* attributed value is larger than the *max_input_noise_width* attribute value. Library Compiler requires that the *min_input_noise_width* value be no larger than the *max_input_noise_width* value.

The following example shows *min_input_noise_width* set at a higher value than *max_input_noise_width* and the resulting error message.

Feedback

```
pin(S) {
  min_input_noise_width : 2.0;
  max_input_noise_width : 1.0;
  ...
  }

Error: Line 18, The 'min_input_noise_width' attribute is larger than
the 'min_input_noise_width' attribute for the pin '%s'.  (LBDB-623)
```

This error message also occurs when any of the following are true:

- The value of **output_signal_level_high** is greater than **output_signal_level_low**.
- The value of **output_signal_level_high** is greater than **output_signal_level**.
- The value of **input_signal_level_high** is greater than **input_signal_level_low**.
- The value of **input_signal_level_high** is greater than **input_signal_level**.

What Next

Change all related values to conform to the requirement and rerun the command.

LBDB-624

(error) The output/inout pin '%s' has illegal 'tied-off' timing arcs.

Description

If a output pin is not tied to "high"(the function attribute is set to "1") or "low"(the function attribute is set to "0"), its time arcs should not set the 'tied-off' attribute to true.

The following example shows an instance where this message occurs:

```
pin(S) {
   function : "A B";
   ...
    timing() {
      tied_off : true;
      steady_state_current_high(table_1) {
          index_1 ("0.00, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
                  ...
          );
      }
      ...
  }
```

Feedback

```
need to delete the 'tied-off' attribute.
```

The following is an example message:

```
Warning: Line 160,  The output pin 'S' has illegal 'tied-off' timing
 arcs. (LBDB-624)
```

What Next

Delete the 'tied-off' attribute.

LBDB-625

(error) The output/inout pin '%s' has a 'tied-off' timing arc containing illegal '%s' %s.

Description

If a output pin is tied to "high"(the function attribute is set to "1"), only steady_state_current_high group is allowed in its timing arc whose 'tied_off' attribute is set to true.

The following example shows an instance where this message occurs:

```
pin(S) {
   function : "1";
   ...
    timing() {
      tied_off : true;
      steady_state_current_high(table_1) {
          index_1 ("0.00, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
                  ...
          );
      }
      ...
  }

need to delete the 'steady_state_current_high' table.
```

The following is an example message:

```
Warning: Line 160,  The output pin 'S' has a 'tied-off' timing arc
 containing illegal 'steady_state_current_high' group.  (LBDB-625)
```

What Next

Delete the illegal noise_immunity/noise_propagation groups.

Feedback

LBDB-626

(error) The 'tied-off' timing arc contains illegal noise_immunity/noise_propagation group.

Description

In a timing arc whose tied_off attribute is set to true, for noise information, only steady_state_current_low group or steady_state_current_high group is allowed

The following example shows an instance where this message occurs:

```
pin(CP) {
   ...
    timing() {
      tied_off : true;
      noise_immunity_high(table_1) {
          index_1 ("0.00, 1.00, 2.50") ;
          index_2 ("0.00, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
                  ...
          );
      }
      ...
  }

need to delete the 'noise_immunity_high' table.
```

The following is an example message:

```
Warning: Line 160, the 'tied-off' timing arc containts illegal
 noise_immunity/noise_propagation group (LBDB-626)
```

What Next

Delete the illegal noise_immunity/noise_propagation groups.

LBDB-627

(error) The '%s' group of the '%s' timing arc\n \tis not referencing the compatible template.

Description

In the specified min_pulse_width timing arc, the only valid templates are as follows:

1. "constrained_pin_transition" (one-dimensional)
2. "related_pin_transition" (one-dimensional)
3. "constrained_pin_transition" + "related_out_total_output_net_capacitance"
4. "related_pin_transition" + "related_out_total_output_net_capacitance"

Feedback

The following example shows an instance where this message occurs:

```
lu_table_template  (table_1)   {
   variable_1  :  related_pin_transition  ;
   index_1 ("0.10, 0.25, 0.50") ;
}
lu_table_template  (table_2)   {
   variable_1  :  related_out_total_output_net_capacitance;
   index_1 ("0.10, 0.25, 0.50") ;
}

 ...

    timing() {
      related_pin : CP ;
      timing_type : min_pulse_width ;
      rise_constraint(table_2) {
          index_1 ("0.50, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
          );
      }
      fall_constraint(table_1) {
          index_1 ("0.50, 1.00, 2.50") ;
          values (\
                  "4.0, 5.0, 6.0"\
          );
      }
```

change the template table_2 to

```
lu_table_template  (table_2)   {
   variable_1  :  constrained_pin_transition  ;
   index_1 ("0.10, 0.25, 0.50") ;
}
```

The following is an example message:

```
Error: Line 160, The 'rise_constraint' group of the 'min_pulse_width'
 timing arc\n
\tis not referencing the compatible template.  (LBDB-627)
```

What Next

Change the variable in the template accordingly.

LBDB-628

(error) The value of timing_sense attribute is invalid for \n \tthe timing arc whose timing_sense should be '%s' instead.

Feedback

Description

The timing arc with feed_through_type attribute must have 'positive_unate' timing_sense.

The following example shows an instance where this message occurs:

```
...
        pin(Z) {
          direction : inout;
          timing() {
            feed_through_type : short;
            timing_sense : negative_unate;
            ...
          }
        }
        ...
```

In this case, the timing sense should be "positive_unate".

The following is an example message:

```
Error: Line 256, The value of timing_sense attribute is invalid for the
        timing arc whose timing_sense should be 'positive_unate' instead.
 (LBDB-628)
```

What Next

Check the timing arc and make the correction accordingly.

LBDB-629

(error) The parent '%s' of the user-defined attribute is not defined.

Description

For define(name, parent, type), parent must be the name of a user-defined group or a predefined library group.

The following example shows an instance where this message occurs:

```
library(test) {
        define(a, test, string);
        ...
    }
```

Since "test" is not defined, we can define a new user-defined group call "test" by adding the following statement: define_group(test, library);

The following is an example message:

```
Error: Line 256, The parent 'test' of the user-defined attribute is not
 defined. (LBDB-629)
```

Feedback

What Next

Either change the parent name or define a new user-defined group with the parent name.

LBDB-630

(error) The 'user_parameters' group is not specified.

Description

This message indicates that the 'user_parameters' group is not specified. Library Compiler errors out because some generic parameters(parameter1..5) are used in either poly_template or power_poly_template, and the 'user_parameters' must be defined to contain the definition of those generic parameters.

The following example shows an instance where this message occurs:

```
user_parameters() {
      parameter1 : 0.80;
    }
```

The following is an example message:

```
Error: Line 52, The 'user_parameters' group is not specified. (LBDB-630)
```

What Next

Add the missing attribute to the 'user_parameters' group. the message.

LBDB-631

(error) The '%s' attribute in the 'user_parameters' group is not specified.

Description

This message indicates that an attribute is missing, and Library Compiler errors out because this attribute is used in either poly_template or power_poly_template.

The following example shows an instance where this message occurs:

```
user_parameters() {
      parameter1 : 0.80;
    }
```

The following is an example message:

```
Error: Line 52, The 'parameter2' attribute in  the 'user_parameters'
 group is not specified. (LBDB-631)
```

Feedback

What Next

Add the missing attribute to the 'user_parameters' group. the message.

LBDB-632

(error) The power rail name '%s' is invalid.

Description

This message indicates that you specified an invalid name for the current power rail. The name should not conflict with the generic parameters(parameter1..paramter5).

The following example shows an instance where this message occurs:

```
power_supply() {
          default_power_rail : VDD0;
          power_rail(parameter1, 4.95);
 }
```

The following is an example message:

```
Error: Line 104, The power rail name 'parameter1' layer name is invalid.
 (LBDB-632)
```

What Next

User a different name that is not conflicting with parameter1..paramter5.

LBDB-633

(error) The %s value, '%s', has not been\n \tdefined in the %s.

Description

This message indicates that the referred value is undefined in the library.

The following example shows an instance where this message occurs:

```
part(a) {
    valid_speed_grades ("A","B","C");
    valid_step_levels ("step0","step1","step3");
    default_step_level : "step0";
    speed_grade("D") {
        step_level("step0");
    }
  }
```

In this case, the "D" valid_speed_grade is not defined.

Feedback

The following is an example message:

```
Error: Line 57, The valid_speed_grade value, 'D',
       has not been defined in the part. (LBDB-74)
```

What Next

Add the referred value in the library.

LBDB-634

(error) The "variables" definition is conflicting with the main template.

Description

This message indicates that you specified an invalid 'variables' for the current poly template domain. It's required that a poly template define the same 'variables' as that of its main poly template.

The following example shows an instance where this message occurs:

```
poy_template(T3) {
       variables (input_net_transition, voltage, temperature);
       . . .
    domain(D1) {
       variables (input_net_transition, voltage);
       . . .
    }
 }
```

The following is an example message:

```
Error: Line 124, The "variables" definition is conflicting with its main
 template. (LBDB-634)
```

What Next

User the same 'variables' definition as that of its main poly template.

LBDB-635

(error) The 'tied-off' timing arc contains illegal related_pin attribute.

Description

In a timing arc whose tied_off attribute is set to true, related_pin attribute is not allowed.

The following example shows an instance where this message occurs:

```
pin(CP) {
   ...
```

Feedback

```
    timing() {
      tied_off : true;
      ...
      related_pin : A;
      }
      ...
  }
```

```
need to delete the 'related_pin' attribute.
```

The following is an example message:

```
Warning: Line 160, the 'tied-off' timing arc containts illegal
 related_pin attribute. (LBDB-635)
```

What Next

Delete the related_pin attribute.

LBDB-636

(error) The '%s' attribute value is invalid for the timing arc.

Description

This message indicates for a timing arc that the attribute value is invalid. For example, clock_gate_check attribute can only be defined to "true" for the setup/hold/nochange timing arcs.

What Next

Remove the attribute from the timing arc.

LBDB-637

(error) The %s-associated '%s' lookup table\n \tcannot use '%s' as its template.

Description

This message can be used as generic error message template. For frequency-base max_cap, it means that: 1. the max_cap lookup table in an input-associated max_cap group must use a one-dimensional template with *frequency* as its variable. 2. the max_cap lookup table in an ouput-associated max_cap group must use a one-dimensional template with *frequency* as its variable, or a two-dimensional template with *frequency* and *total_output_net_capacitance* as its variables with *frequency* being the first variable.

The following example shows an instance where this message occurs:

```
maxcap_lut_template(ok_temp) {
    variable_1 : frequency;
```

Feedback

```
    index_1("0, 1, 2, 3");
  }
  maxcap_lut_template(err_temp) {
    variable_1 : input_transition_time;
    index_1("0, 1, 2, 3");
  }

        max_cap(err_temp) {
                values ("1, 2, 3, 4");
        }
```

To fix the problem, change the template value of the *max_cap* attribute from *err_temp* to *ok_temp*.

The following is an example message:

```
Error: Line 126, The input-associated 'max_cap' lookup table
       cannot use 'err_temp' as its template. (LBDB-637)
```

What Next

For more information about lookup tables, see the *Library Compiler User Guide*. Change the library source file by referencing a different template in the lookup table description.

LBDB-638

(error) It is invalid to specify the '%s' %s \n \ton an %s pin.

Description

This message indicates that you specified a invalid group on a pin.

The following example shows an instance where this message occurs:

```
pin (p) {
    direction : input;
    ...
    max_cap (test) {
      ...
    }
    ...
  }
```

The following is an example message:

```
Error: Line 67, It is invalid to specify the 'max_cap' group
        on an input pin. (LBDB-638)
```

What Next

Check the library source file, and correct the problem.

Feedback

LBDB-639

(warning) The '%s' %s in this timing arc are ignored.

Description

This message indicates that you specified a redundant attribute or group for the sequential half-nate timing arcs.

In the following example, both the cell_fall group and the fall_transition group are redundant for the sequential half-unate timing arc.

```
timing() {
  timing_type : rising_edge;
  timing_sense : positive_unate;
  cell_rise( f_ocap ){
    index_1 ( "0.0000, 1.0000, 512.0000, 7999.9995, 15999.9990,
 31999.9980, 63999.9961");
    values ( "25.0000, 35.0000, 5145.0000, 80024.9922, 160024.9844,
 320024.9688, 640024.9375");
  }
  rise_transition( f_ocap ){
    index_1 ( "0.0000, 1.0000, 512.0000, 7999.9995, 15999.9990,
 31999.9980, 63999.9961");
    values ( "15.0000, 25.0000, 5135.0000, 80014.9922, 160014.9844,
 320014.9688, 640014.9375");
  }
  cell_fall( f_ocap ){
    index_1 ( "0.0000, 1.0000, 512.0000, 7999.9995, 15999.9990,
 31999.9980, 63999.9961");
    values ( "25.0000, 35.0000, 5145.0000, 80024.9922, 160024.9844,
 320024.9688, 640024.9375");
  }
  fall_transition( f_ocap ){
    index_1 ( "0.0000, 1.0000, 512.0000, 7999.9995, 15999.9990,
 31999.9980, 63999.9961");
    values ( "15.0000, 25.0000, 5135.0000, 80014.9922, 160014.9844,
 320014.9688, 640014.9375");
  }
}

Warning: Line 639, The cell_fall group in this
   timing arc are ignored. (LBDB-390)
Warning: Line 639, The fall_transition group in this
   timing arc are ignored. (LBDB-390)
```

What Next

Remove the redundant groups from the timing arc and rerun the command.

Feedback

LBDB-640

(error) The '%s' attribute %s \n \tin this %s group.

Description

This message indicates you need to specify or remove an attribute from the group according to the template it references as follows: 1. 1-dimentional template does not allow the 'related_pin' attribute. 2. 2-dimentional template requires the 'related_pin' attribute.

The following example shows an instance where this message occurs:

```
max_cap(maxcap_1d_template) {
                values ("1, 2, 3, 4");
                related_pin : "A";
        }
```

In this case, the 'related_pin' attribute is not allowed in 1-dimensional lookup table. To fix the problem, remove the related_pin attribute from the max_cap group.

The following is an example message:

```
Error: Line 69, The 'related_pin' attribute cannot be specified
        in this max_cap group. (LBDB-640)
```

What Next

Change the technology library source file to add or delete the specified attribute.

LBDB-641

(error) The '%s' %s has some %s groups \n \tmissing the %s attribute.

Description

This message indicates there is one or more leakage_power(internal) groups without the power_level attribute. When at least one leakage_power(internal_power) is specified with the power_level attribute in a cell(pin), all the leakage_power(internal_power) in the cell must also have the power_level attribute defined.

It can also be used to notify a user that teh related_pg_pin attribute is missing in the leakage_power/internal_power groups.

The following example shows an instance where this message occurs:

```
cell(AN2) {
      leakage_power () {
        power_level : VDD1;
        value : 1.0;
      }
```

```
      leakage_power () {
        /* power_level : VDD2; */
        value : 2.0;
      }
      ...
  }
```

In this case, the power_level attribute is missing for the 2nd leakage_power. To fix the problem, add the attribute to the leakage_power group:

```
cell(AN2) {
      leakage_power () {
        power_level : VDD1;
        value : 1.0;
      }
      leakage_power () {
        power_level : VDD2;
        value : 2.0;
      }
      ...
  }
```

The following is an example message:

```
Error: Line 12, The 'AN2' cell has some leakage_power groups
        missing the power_level attribute. (LBDB-641)
```

What Next

Add the missing attribute for the leakage_power group.

LBDB-642

(warning) The group '%s' is defined multiple times\n \tin group '%s'. Using the last one encountered.

Description

Some groups require that no more than one same group be defined in their scope.

Some groups require when statement, and only one of them can be defined without when statement in their scope.

The following example shows an instance where this message occurs:

```
pin_capacitance ()  {
     rise_capacitance_range() { ... }
     rise_capacitance_range() { ... }
   }
```

Feedback

The following is the example message:

```
Warning: Line 987, The group 'rise_capacitance_range' is defined multiple
 times
        in group 'pin_capacitance'. Using the last one encountered.
 (LBDB-642)
```

The following example shows another instance where this message occurs:

```
cell(test) {
   ...
   leakage_current ()  {
     when : A;
     pg_current(VDD) {
       value : 5.3;
     }
   }
   leakage_current ()  {
     when : A1;
     pg_current(VDD) {
       value : 15.3;
     }
   }
   ...
   leakage_current ()  {
     pg_current(VDD) {
       value : 0.3;
     }
   }
   leakage_current ()  {
     pg_current(VDD) {
       value : 8.3;
     }
   }
   ...
Only one of leakage_current groups with no 'when' statement can be
defined under a cell.  If there are more than one group with no
'when' statement defined, then they are duplicated groups.
```

The following is the example message:

```
Warning: Line 138, The group 'leakage_current' is defined multiple times
        in group 'cell'. Using the last one encountered. (LBDB-642)
```

What Next

Remove the extra objects.

LBDB-643

(error) '%s' is used more than once inside cell '%s'.

Feedback

Description

This error message occurs when unique *power_gating_pin* attribute value is specified more than once within a cell.

The following example shows power_pin_1 specified twice within a cell and the resulting error message:

```
cell (BUF) {
    pin(A) {
      power_gating_pin (power_pin_1, "0") ;
      direction : input;
    }
    pin(B) {
      power_gating_pin (power_pin_1, "0") ;
      direction : output;
    }
  }

Error: Line 56, 'power_pin_1' is used more than once inside cell 'BUF'.
(LBDB-643)
```

What Next

Make sure that each unique *power_gating_pin* value is specified only once.

LBDB-644

(warning) The cell_leakage_power attribute of the '%s' cell is redundant\n \tand not used in the leakage_power modeling.

Description

This message indicates one of the following two cases are true: 1. there is power_level specific leakage_power groups in the cell 2. the cell has no power_level specific leakage_power groups, and it has default leakage_power group(leakage_power group without 'when' statement).

The following example shows an instance where this message occurs:

```
cell(AN2) {
      cell_leakage_power : 0.5;
      leakage_power () {
        power_level : VDD1;
        when : "A";
        value : 1.0;
      }
      ...
  }
```

Feedback

In this case, the cell has power_level specific leakage_power groups, thus the cell_leakage_power attribute is redundant. To fix the problem, remove the attribute from the cell group.

The following example shows another instance where this message occurs:

```
cell(AN2) {
      cell_leakage_power : 0.5;
      leakage_power () {
        when : "A";
        power(LKP_T) {
           orders ("1, 1");
           coefs  ("1, 1, 1, 1");
           domain (D1) {
                 orders ("1, 1");
                 coefs  ("1, 1, 1, 1");
           }
        }
      }
      ...
  }
```

In this case, a cell_leakage_power attribute is redundant. To fix the problem, remove the attribute from the cell group:

Warning: Line 12, The cell_leakage_power attribute of the 'AN2' cell is redundant and not used in the leakage_power modeling. (LBDB-644)

What Next

Remove the 'cell_leakage_power' from the cell.

LBDB-645

(error) Cannot find the '%s' %s in the %s.

Description

This error message occurs when a power_rail name attached to a *related_power_rail* or *rail_value* attribute does not exist in the power_supply.

This error message also occurs when the *default_power_rail* attribute is not defined in the power_supply group.

The following code does not contain VDD4 in the power_supply, which results in the error message.

```
library(libg5) {
    ...
    power_supply(pw) {
      default_power_rail : VDD;
```

```
        power_rail (VDD1, 2.0);
        power_rail (VDD2, 2.5);
        power_rail (VDD3, 3.0);
        power_rail (VSS1, 3.0);
        power_rail (VSS2, 3.0);

        mapping(VSS1) {
                related_power_rail : "VDD1 VDD2";
        }
        mapping(VSS2) {
                related_power_rail : "  VDD4 VDD3       ";
        }
      }

 }

Error: Line 403, Cannot find the 'VDD4' power_rail in the power_supply.
(LBDB-645)
```

What Next

Check your library for an incorrect power_rail name, correct the name, and run the command again.

LBDB-646

(error) No %s information is defined before the %s '%s'.

Description

This error message occurs when you have not defined the power_supply statement for the power_level.

This message also occurs when the power_supply group is missing for a cell rail_connections because some pins of the cell do not define the *input_signal_level* (for an input pin) or the *output_signal_level* (for an output pin).

The following example shows a library with a missing power_supply statement before the cell containing the power_level attribute and the resulting error message.

```
library(lib) {
  ...
  cell (A)
    ...
    leakage_power() {
        power_level : "VDD";
        ...
    }
    ...
 }
```

Feedback

```
Error: Line 191, No power_supply information is defined before the
power_level 'VDD'. (LBDB-646)
```

What Next

Add the power_supply statement before the cell statement that contains the power_level, as shown in the following example:

```
power_supply() {
        default_power_rail : VDD;
        power_rail (VDD, 2.0);
        ...
  }
```

LBDB-647

(warning) Found the obsolete and unsupported '%s' %s in the '%s' cell; use '%s' instead.

Description

The *rail_connection* attribute is not supported after 2004.12 Beta version. Instead, the information should now be described in the power_pin group.

The following is an example of the error message:

```
Warning: Line 159, Found the obsolete and unsupported 'rail_connection'
attribute in the 'sample' cell; use 'power_pin' group instead. (LBDB-647)
```

What Next

If you have access to the technology library source file, change the *rail_connection* attribute to power_pin group. Otherwise, contact the vendor and inform them of the problem.

LBDB-648

(error) The power_pin definitions of cell '%s' do not follow the mapping rules specified in the power_supply group.

Description

This error message occurs when the definitions of the power_pins do not follow the mapping rules in the power_supply group. The following is an example of this error message:

```
Warning: Line 159, The power_pin definitions of cell '%s' do not follow
the mapping rules in the power_supply group. (LBDB-648)
```

Feedback

What Next

Either change the mapping rules in the power_supply group or redefine the power_pins and run the command again.

LBDB-649

(error) The '%s' domain's power rail mapping information conflicts with its main template.

Description

This error message occurs when the power rail mapping information is incorrectly defined in the domain of the poly_template. The information in poly_template domain must be exactly the same as the poly_template.

The following example shows the *d1* domain of the *p1* poly_template with the incorrect mapping statement and the resulting error message:

```
poly_template(p1) {
  ...
  mapping(voltage1, VDD1);
  mapping(voltage, VDD0);
  ...
  domain(d1) {
    ...
    mapping(voltage1, VDD2);
    mapping(voltage, VDD0);
    ...
  }
}

Error: Line 191, The 'd1' domain's power rail mapping information
conflicts with its main template. (LBDB-649)
```

What Next

Modify the mapping statements in this domain of the poly_template to match those of the poly_template.

The following example shows the correct *d1* domain mapping statements:

```
mapping(voltage1, VDD1);
    mapping(voltage, VDD0);
```

LBDB-650

(error) The '%s' cell is not a valid %s.

Feedback

Description

This error message occurs when the level shifter, isolation cell or clock isolation cell is incorrectly modeled. A level shifter or an isolation cell must satisfy one of the following sets of conditions:

- It has 3 pins, including 1 input pin, 1 level_shifter_enable_pin/ isolation_cell_enable_pin, 1 output pin.
- It has 2 pins, including 1 input pin and 1 output pin.

A clock isolation cell must satisfy:

- It has 3 pins, including 1 clock_isolation_cell_clock_pin, 1 isolation_cell_enable_pin, 1 output pin.

  The following example shows the level shifter with the incorrect modeling and the resulting error message:

```
cell(LS) {
 is_level_shifter : true;
 ...
 pin(a) {
        ...
 }
 pin(b) {
        ...
 }
 pin(c) {
        ...
 }
 pin(d) {
        ...
 }
}
Error: Line 191, The 'LS' cell is not a valid level shifter.
 (LBDB-650)
```

What Next

Correct the modeling information of the level shifter or isolation cell to satisfy the requirements.

You could correct the modeling in the previous example by removing one of the pins specified in the cell.

LBDB-651

(error) The %s%s '%s' contains the \n \tconflicting '%s'/'%s' values.

Feedback

Description

This error message occurs when the *input_signal_level* and *output_signal_level* values are modeled incorrectly for the level shifter or isolation cell.

For a level shifter, *input_signal_level* in input pin can't be the same as *output_signal_level* in output pin. Meaning that the rail names can't be the same in a level shifter.

For an isolation cell, the value of *input_signal_level* in input pin can't be different from the value of *output_signal_level* in output pin. Meaning that the rail values can't be difference in an isolation cell.

The following example shows the level-shifter with the incorrect modeling and the resulting error message:

```
cell(LS) {
 is_level_shifter : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDD2
 }
 pin(out) {
        ...
        output_signal_level : VDD2
 }
}

Error: Line 191, The pins of level shifter 'LS' contain the
conflicting 'input_signal_level'/'output_signal_level' values. (LBDB-651)
```

The following example shows the isolation cell with the incorrect modeling and the resulting error message:

```
library(libdb651) {
  ...
  /* operation conditions */
  operating_conditions(5v_1v) {
    ...
    power_rail (VDDH, 5);    /* high power */
    power_rail (VDDL, 1);    /* low power */
    ...
  }
  ...
  default_operating_conditions : 5v_1v;

  ...
cell(ISO) {
 is_isolation_cell : true;
 ...
 pin(in) {
        ...
```

```
        input_signal_level : VDDH
 }
 pin(out) {
        ...
        output_signal_level : VDDL
 }
}

Error: Line 191, The pins of isolation cell 'ISO' contain the
conflicting 'input_signal_level'/'output_signal_level' values. (LBDB-651)
```

What Next

For the first example, modify the modeling information of the level shifter to meet the requirements.

To correct the modeling of the example above, make the *input_signal_level* string "VDD1" of the input pin different from the *output_signal_level* string "VDD2" of the output pin as follows:

```
cell(LS) {
 is_level_shifter : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDD1
 }
 pin(out) {
        ...
        output_signal_level : VDD2
 }
}


For the second example, modify the modeling information of the isolation
 cell
to meet the requirements.

To correct the modeling of the example above, make the
input_signal_level value "5" of the input pin
same as the output_signal_level value "1" of the
output pin.  You can assiged both to the same pin like
"VDDH", so that both will refer to same value "5" in
operating_conditions as follows.

library(libdb651) {
  ...
  /* operation conditions */
  operating_conditions(5v_1v) {
    ...
    power_rail (VDDH, 5);    /* high power */
    power_rail (VDDL, 1);    /* low power */
```

Feedback

```
    ...
  }
  ...
  default_operating_conditions : 5v_1v;

  ...
cell(ISO) {
 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDH
 }
 pin(out) {
        ...
        output_signal_level : VDDH
 }
}
```

LBDB-652

(error) The %s '%s' has incompatible '%s' and '%s'.

Description

This error message occurs when the user specified attributes are incompatible. For example, specifying both *pulse_clock* and *generated_clock* inside a cell.

```
Error: Line 159, The cell 'A' has incompatible 'pulse_clock'
and 'generated_clock'.  (LBDB-652)
```

What Next

Either remove the *pulse_clock*attribute or the *generated_clock* group for the cell.

LBDB-653

(error) The index of '%s' can define only one value.

Description

This error message occurs because the specified index cannot contain more than one value. This restriction applies to the dimension input_net_transition, and total_output_net_capacitance in the vector group.

The following example shows an index with more than one value and the resulting error message.

```
output_current_template(CCS_T) {
    variable_1 : input_net_transition;
```

Feedback

```
    variable_2 : total_output_net_capacitance;
    variable_3 : time;
  }
  vector(CCS_T) {
        reference_time : 0.5;
        index_1 ("0.12");
        index_2 ("0.1, 1.2");
        index_3 ("0.01, 0.02, 0.03");
        values (" ... ");
  }

Error: Line 46, The index of 'total_output_net_capacitance' can
only define one value. (LBDB-653)
```

To correct the error, change index_2 to ("0.1");

What Next

Check the library source file and remove the extra values in the index definition.

LBDB-654

(error) The values of '%s' and '%s' are not consistent in %s '%s'.

Description

This error message occurs when the values of the *reference_time* and *input_net_transition* attributes are inconsistent inside the output_current_rise or output_current_fall group. Inside each output_current_rise or output_current_fall group, only the same pair of *reference_time* and *inout_net_transition* values is allowed.

Note: In 2007.03 release, the message is enhanced to also report inconsistent input_voltage_range and output_voltage_range values in a level shifter. Assuming that a level shifter defines the following information: level_shifter_type : <lst_val>; input_voltage_range(<<ivrl_val>, <ivrh_val>); output_voltage_range(<ovrl_val>, <ovrh_val>); then it must satisfy the following requirements: - if <lst_val> = HL, then <ivrh_val> > <ovrl_val>. - if <lst_val> = LH, then <ivrl_val> < <ovrh_val>. Otherwise, LC will issue LBDB-654 error.

The following is an example of inconsistent *reference_time* and *input_net_transition* values and the resulting error message:

```
output_current_template(CCT) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
  variable_3 : time;
 }
 . . .
 output_current_rise() {
   vector(CCT) {
```

Feedback

```
      reference_time : 0.11; <=== reference_time = 0.11 with
 input_net_transition = 0.1
      index_1 ("0.1");
      index_2 ("1");
      index_3 ("1, 2, 3");
      values ("1, 2, 3");
   }
    vector(CCT) {
      reference_time : 0.12; <=== reference_time = 0.12 with
 input_net_transition = 0.1
      index_1 ("0.1");
      index_2 ("2");
      index_3 ("1, 2, 3");
      values ("1, 2, 3");
   }
 }

Error: Line 98, The values of 'reference_time' are not consistent in
group 'output_current_rise'. (LBDB-654)
```

What Next

Check the library source file, and correct the values of the *reference_time* attribute.

LBDB-655

(error) The vectors are not dense in group '%s'.

Description

This error message occurs because Library Compiler requires a "complete grid" of vector groups inside each output_current_rise or output_current_fall group. The vector groups must form a dense MxN grid, with M unique input_net_transition values, and N unique total_output_net_capacitance values. The vector groups should have exact MxN number and any duplicate input_net_transition and total_output_net_capacitance pair will cause this error.

A similar dense grid requirement is also imposed on the output_voltage_rise and output_voltage_fall groups of input_ccb and output_ccb. (This requirement does not apply to those of ccsn_first_stage and ccsn_last_stage).

The following example shows an output_current_rise group without a dense vector and resulting error message.

```
output_current_template(CCT) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
  variable_3 : time;
 }
 . . .
 output_current_rise() {
```

Feedback

```
   vector(CCT) {
      reference_time : 0.11;
      index_1 ("0.1");
      index_2 ("1");
      index_3 ("1, 2, 3");
      values ("1, 2, 3");
   }
    vector(CCT) {
      reference_time : 0.11;
      index_1 ("0.2");
      index_2 ("2");
      index_3 ("1, 2, 3");
      values ("1, 2, 3");
   }
   /* need vectors for (0.1, 2) and (0.2, 1) */
 }

Error: Line 198, The vectors are not dense in group
 'output_current_rise'.
(LBDB-655)
```

What Next

Check the library source file and add a vector for each input_net_transition and total_output_net_capacitance pair.

LBDB-656

(error) The lu_table_template '%s' referred by '%s' in line %d is invalid.

Description

This error message occurs because the variable of the referred lu_table_template can only include the *input_net_transition* variable for the pin based receiver model. For the timing arc based receiver model, the variable of the referred lu_table_template can include *input_net_transiton* and *total_output_net_capacitance*.

The following example shows an invalid lu_table_template reference and the resulting error message:

```
lu_table_template(T1) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
  . . .
 }
 . . .
 pin(A) {

 receiver_capacitance() {
   receiver_capacitance1_rise(T1) {
      index_1 ("0.1, 0.1");
```

Feedback

```
      index_2 ("1, 2");
      values ("1, 2", "2.5, 3");
   }
   . . .
 }
```

```
Error: Line 298, The lu_table_template 'T1' referred by
 'receiver_capacitance1_rise' in line 1239 is invalid. (LBDB-656)
```

What Next

Check the library source file, and correct the variable(s) of the corresponding lu_table_template.

LBDB-657

(error) Conflicting receiver model found in pin '%s' (pin-based) and in timing arc '%s-%s' (arc-based).

Description

This error message occurs because when an input (or inout) pin A defines a receiver_capacitance() group, then no timing arc whose from pin is A, can define receiver_capacitance1_rise/receiver_capacitance1_fall/ receiver_capacitance2_rise/ receiver_capacitance2_fall.

The following is an example of an incorrect definition and the resulting error message:

```
pin(A) {
   direction : input;
   receiver_capacitance() { . . .}
   . . .
 }
 pin(Y) {
   direction : output;
   timing() {
     receiver_capacitance1_rise(T1) { . . .}
     receiver_capacitance1_fall(T1) { . . .}
     receiver_capacitance2_rise(T1) { . . .}
     receiver_capacitance2_fall(T1) { . . .}
     . . .
   }
   . . .
 }
```

Error: Line 398, Conflicting receiver model found in pin 'A' (pin-based) and in timing arc 'A-Y' (arc-based). (LBDB-657)

Feedback

What Next

Check the library source file and remove the duplicated receiver model. Usually it is best practice to use the timing arc based receiver model.

LBDB-658

(error) Both variable and range of poly_template '%s' should be defined before domain '%s' is defined.

Description

You receive this message a domain can't be defined because either the variable or range statement of the main poly_template is missing.

The following example shows an instance where this message occurs: The following example shows the *p1* poly_template is missing both variable and range information.

```
poly_template(p1) {
 poly_template(PT)  {
  domain(D1)  {
    variables("temperature, total_output_net_capacitance");
    variable_1_range(0, 40);
    variable_2_range(1, 2);
  }
  ......
}
```

Correct it by add *variables, variable_1_range and variable_2_range statement in the poly_template group.*

The following is an example message: Error: Line 191, Both variable and range of poly_template 'PT' should be defined before domain 'D1' is defined. (LBDB-658)

What Next

Make sure that *variables* and all *variable_n_range* statements exist before defining domains.

LBDB-659

(error) The %s %s cannot coexist\n \twith the '%s' %s on the '%s' pin.

Description

The first specified attribute/group in the pin cannot coexist with the second specified attribute/group on the same pin. For example, the *is_three_state* attribute cannot be specified on a pin with *three_state* attribute.

Feedback

The following example shows an instance where this message occurs:

```
cell(lbdb239) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;
    }
    ...

    pin(Z) {
      direction : output;
      function : "A";
      three_state : "B"

      is_three_state : false; /* error */
      ...
    }
  }
```

The following is an example message:

```
Error: Line 84, The  "false" 'is_three_state' attribute cannot coexist
        with the 'three_state' attribute on the 'Z' pin. (LBDB-659)
```

What Next

Check the specification of the cell, and make the appropriate change to the *driver_type* attribute or other attributes in the faulty pin group.

LBDB-660

(error) It is invalid to specify the '%s' %s on the '%s' %s%s.

Description

This message indicates that you have specified an invalid attribute or group for a cell.

The following example shows an instance where this message occurs:

```
cell (p) {
    clocked_cell : rising_edge;
    pin(clk) {
      clock : true;
    }

    pin(out) {
      function : "clk";
    }
  }
```

To correct the error, add at least 1 combinational timing arc between the *clk* and *out* pins.

Feedback

The following is an example message:

```
Error: Line 67, It is invalid to specify the 'clocked_cell' attribute on
 the 'p' cell. (LBDB-660)
```

What Next

Check the library source file, and ensure that the following conditions are met:

- The *is_isolated attribute* is specified only on the macro-cell pins.
- When the *clocked_cell* attribute is specified, the corresponding cell has
  - only 1 clock-pin, with the *clock* attribute set to *true*.
  - at least 1 timing arc between the clock pin and an output pin.

LBDB-661

(error) The 'generic' integrated clock gating cell should not define the 'statetable' group without 'ff/latch' group.

Description

This message indicates that you specified the 'generic' integrated gating clock cell with 'statetable' definition without 'ff/latch' group definition. You should define 'statetable' group with 'ff' or 'latch' group.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";

  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,\
               L  H  : - : H ,\
               H  -  : - : N ";
  }
  ...
}

The modified cell description should be :

cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";

  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,\
               L  H  : - : H ,\
               H  -  : - : N ";
```

Feedback

```
  }
  latch("IQ","IQN") {
    enable : "CP'";
    data_in : "EN";
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The 'generic' integrated clock gating cell should not
 define the 'statetable' group without 'ff/latch' group.(LBDB-661)
```

What Next

Change the library source file, add 'ff' group or 'latch' group definition.

LBDB-662

(warning) The %s is not defined. operating_conditions "nom_pvt" is created \n \tand set as the default_operating_conditions.

Description

This warning message occurs when the *default_operating_conditions* is undefined and there is eith no operating_conditions groups defined or multiple operating_conditions defined.

What Next

If you do not want Library Compiler to create the default operating_conditions for you, please check your library to define the relative operating_condition group and set it as the default_operating_conditions with the library-level attribute "default_operating_conditions".

LBDB-663

(warning) The %s is not defined. operating_conditions '%s' is set\n \tas the default_operating_conditions.

Description

This warning message occurs when the *default_operating_conditions* is undefined and there is extactly 1 operating_conditions group defined in the library.

What Next

If you do not want Library Compiler to automatically set the default operating_conditions for you, please check your library to define the relative operating_condition group

Feedback

and set it as the default_operating_conditions with the library-level attribute "default_operating_conditions".

LBDB-664

(error) The '%s' attribute of the '%s' has a value '%g',\n \twhich should be %s for the %s.

Description

The value specified is equal to a threshold value 0.0 for the attribute.

The following example shows an instance where this message occurs:

```
output_current_rise() {
        vector(current_template_8x7) {
           reference_time : 0.0140609;
           index_1("0");
           index_2("0.019368");
           index_3("0.1462, 0.175, 0.19, 0.205, 0.235, 0.25, 0.265,
 0.275, 0.29, 0.305, 0.32, 0.35, 0.406591");
           values("0.0, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1,
 1.2, 1.3");
        }
      }
```

The following is an example message:

```
Error: Line 1897, Cell 'A', pin 'X', The 'values' attribute of the
 'vector' has a value '0',
       which should be non-zero for the output_current_rise vector.
 (LBDB-664)
```

What Next

Check the library source file and correct the problem.

LBDB-665

(error) The %s value of the '%s' attribute of the '%s' is the peak value.

Description

The frist value specified in the specified attribute is a peak value, i.e., the maximun value for the values attribute of the vector of an output_current_rise group, or the minimum value for the values attribute of the vector of an output_current_fall group.

The following example shows an instance where this message occurs:

```
output_current_rise(current_template_8x7) {
        vector(current_template_8x7) {
           reference_time : 0.0140609;
```

Feedback

```
          index_1("0");
          index_2("0.019368");
          index_3("0.1462, 0.175, 0.19, 0.205, 0.235, 0.25, 0.265,
 0.275, 0.29, 0.305, 0.32, 0.35, 0.406591");
          values("1.8, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1,
 1.2, 1.3");
       }
     }
```

The following is an example message:

```
Error: Line 35, The first value of the 'values' attribute of the 'vector'
 is the peak value. (LBDB-665)
```

What Next

Check the library source file and correct the problem.

LBDB-666

(warning) The '%s' has the same %s %g as the '%s' at line %d, \n \tbut the %s does not increase(from %g to %g) \n \twith increasing %s (from %g to %g).

Description

For a timing arc, within each output_current_rise/fall group. for a given total_output_net_capacitance(load), teh reference_times should increase with the increasing input_transition_time(slew). This check is only useful for the signoff timing analysis with the 2004.12 and the relative sevice pack releases of PrimeTime.

The following example shows an instance where this message occurs:

```
output_current_rise(current_template) {
               ...
              vector(current_template) {
                 reference_time : 0.0140609;
                 index_1("0.1"); /* load */
                 index_2("0.019368"); /* slew */
                 index_3("0.1462, 0.175, 0.19, 0.205, 0.235, 0.25,
 0.265, 0.275, 0.29, 0.305, 0.32, 0.35, 0.406591");
                 /* LBDB-664 */
                 values("0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9,
 1.0, 1.1, 1.2, 1.3");
              }
              vector(current_template) {
                 reference_time : 0.0319875;
                 index_1("0.1"); /* load */
                 index_2("0.049573"); /* slew */
                 index_3("0.160795, 0.185, 0.2, 0.23, 0.24, 0.255, 0.27,
 0.285, 0.295, 0.31, 0.325, 0.34, 0.355, 0.37, 0.4
175");
```

Feedback

```
                values("0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9,
 1.0, 1.1, 1.2, 1.3");
              }
               ...
        }
```

The following is an example message:

```
Warning : Line 357, The 'vector' has the same
 total_output_net_capacitance 0.000000 as the 'vector' at line 364,
        but the reference_time does not increase(from 0.031987 to
 0.026168)
        with increasing input_net_transition (from 0.049573 to 0.094881).
 (LBDB-666)
```

What Next

Check the library source file and correct the problem.

LBDB-667

(warning) This '%s' group has a value (%g) in 'vector/index_1' that does not match any values of 'index_1' in '%s' at line %u. Parent '%s' is at line %u.

Description

In the referenced ccs noise data modeling, output_voltage_rise and output_voltage_fall are characterized in ways to be closer to timing characterization. Their "input slew" (vector/index_1) and "output load" (vector/index_2) values form a 2D grid, similar to various timing lookup tables.

To best match timing behavior, "input slew" values of all CCB's should match points given in index_1 of respective driver waveform. See also LBDB-979 for additional checks on CCB's involved in propagating noise.

The following example shows an instance where this message occurs:

```
library(test) {
  ...
  normalized_driver_waveform(ndw1) {
    driver_waveform_name : "driver_waveform_default_fall" ;
    index_1("0.003209, 0.0133113, 0.033516, 0.0726625, 0.152218");
    ...
  }
  ...
  cell (flop) {
    ...
    pin(A) {
      ...
      driver_waveform_fall : driver_waveform_default_fall ;
      ...
```

Feedback

```
        input_ccb(ccb1) {
          ...
          output_voltage_fall() {
            vector(vec1) {
              index_1("0.013209,...");
              ...
          }
          ...
        }
        ...
      }
      ...
    }
}
```

Examples

Warning: Line 28818, Cell 'ICG', pin 'SE', This 'output_voltage_fall' group has a value (0.00863453) in 'vector/index_1' that does not match any values of 'index_1' in 'normalized_driver_waveform' at line 261. Parent 'input_ccb' is at line 28776. (LBDB-667)

What Next

Correct the characterization procedure.

LBDB-668

(warning) related_pin '(%s)', when '(%s)', slew/load '(%g/%g)', The final signal voltage of the %s is %g, which does not reach within the 5 percent of the rail voltage %g.

Description

For each output_current_rise/fall vector, the final signal voltage must be within the 5% of the final rail voltage. This can be described with the following formulas:

If output_signal_level_low and output_signal_level_high are specified, volt_low = output_signal_level_low; volt_high = output_signal_level_high; Else volt_low = VSS; volt_high = VDD;

1. For the output_current_rise vector, Vfinal = volt_low + (0.5/Cout)*(I2+I1)*(T2-T1)+... +(0.5/Cout)*(In+In-1)*(Tn-Tn-1) and fabs(Vfinal - volt_high) must NOT be greater than 0.02 (volt_high - volt_low) 2. For the output_current_fall vector, Vfinal = volt_high + (0.5/Cout)*(I2+I1)*(T2-T1)+...+(0.5/Cout)*(In+In-1)*(Tn-Tn-1) and fabs(Vfinal - volt_low) must NOT be greater than 0.02 (volt_high - volt_low)

The following is an example message:

```
Error : Line 373, cell 'TEST', pin 'Q', related_pin '(CP)', when '(!D)',
 slew/load '(0.0088/0.0012)', The final signal voltage of the vector is
 1.200000, which does not reach within the 5 percent of the rail voltage
 1.000000. (LBDB-668)
```

Feedback

What Next

Check the library source file and correct the problem.

LBDB-669

(error) The final signal voltage of the %s is %g and it does not reach beyond the 2nd \n \tslew threshold voltage, which is %g for the %s.

Description

For each output_current_rise/fall vector, the final signal voltage must reach the 2nd slew threshold(i.e., the maximum of the slew thresholds for the output_current_rise vectors, and the minimum of the slew thresholds for the output_current_fall vectors) This can be described with the following formulas:

If output_signal_level_low and output_signal_level_high are specified, volt_low = output_signal_level_low; volt_high = output_signal_level_high; Else volt_low = VSS; volt_high = VDD;

1. For the output_current_rise vector, Vfinal = volt_low + (0.5/Cout)*(I2+I1)*(T2-T1)+... +(0.5/Cout)*(In+In-1)*(Tn-Tn-1) Verr = volt_low + MAX(slew_lower_threshold_pct_rise, slew_upper_threshold_pct_rise, output_threshold_pct_rise) * (volt_high-volt_low) * 0.01

Vfinal must NOT be less than Verr. 2. For the output_current_fall vector, Vfinal = volt_high + (0.5/Cout)*(I2+I1)*(T2-T1)+...+(0.5/Cout)*(In+In-1)*(Tn-Tn-1) Verr = volt_low + MIN(slew_lower_threshold_pct_fall, slew_upper_threshold_pct_fall, output_threshold_pct_fall) * (volt_high-volt_low) * 0.01

Vfinal must NOT be greater than Verr.

The following is an example message:

```
Error : Line 373, The final signal voltage of the vector is 0.800000 and
 it does not reach beyond the 2nd
        slew threshold voltage, which is 1.000000 for the
 output_current_fall vector. (LBDB-669)
```

What Next

Check the library source file and correct the problem.

LBDB-670

(information) The '%s' has '%s' %s, \n \twhich has less than %d significant digits.

Feedback

Description

The values in the current/receiver_capacitance tables should have at least 4 significant digits. The value of intrinsic_resistance and intrinsic_capacitance should have at least 2 significant digits if there is no off channel resistance (i.e. greater than 1Mohm) in the library.

The following example shows an instance where this message occurs:

```
output_current_rise(current_template) {
        ...
        vector(current_template) {
           reference_time : 0.0961844;
           index_1("0");
           index_2("0.170393");
           index_3("0.254379, 0.295, 0.31, 0.325, 0.34, 0.355, 0.385,
 0.4, 0.415, 0.43, 0.445, 0.475, 0.543056");
           values("0.1234, 0.2345, 0.3456, 0.4567, 0.5678, 0.6789,
 0.7890, 0.7891, 0.0001, 0.7892, 0.7893, 0.7894, 0.7895");
        }
        ...
    }
```

The following is an example message:

```
Information : Line 373, The 'vector' has 'values' 0.4,
        which has less than 4 significant digits. (LBDB-670)
```

What Next

Check the library source file and correct the problem.

LBDB-671

(warning) The '%s' has %s adjacent '%s' (%.8g, %.8g).

Description

The adjacent 'values' in the vectors fo the outpur_current_rise/fall tables are identical.

The following example shows an instance where this message occurs:

```
output_current_rise(current_template) {
        ...
        vector(current_template) {
           reference_time : 0.0961844;
           index_1("0");
           index_2("0.170393");
           index_3("0.254379, 0.295, 0.31, 0.325, 0.34, 0.355, 0.385,
 0.4, 0.415, 0.43, 0.445, 0.475, 0.543056");
           values("0.1234, 0.2345, 0.2345, 0.4567, 0.5678, 0.6789,
 0.7890, 0.7891, 0.0001, 0.7892, 0.7893, 0.7894, 0.7895");
```

```
        }
        ...
    }
```

The following is an example message:

```
Error : Line 373, The 'vector' has identical adjacent 'values' (0.2345,
 0.2345). (LBDB-671)
```

What Next

Check the library source file and correct the problem.

LBDB-672

(information) There are more than 1 operating_conditions defined in the library.

Description

The message is to notify users that there are more than 1 operating_conditions defined in the library. For each library, only 1 operating_condtions group is necessary since it defined the pvt used for characterizing the library, and this operating_condtion is also the "default_operating_conditions" of the library.

LBDB-673

(warning) The timing arc does not have full receiver modeling information.

Description

This message indicates that the timing arc does not have all the following receiver modeling information: receiver_capacitance1_rise, receiver_capacitance1_fall, receiver_capacitance2_rise, receiver_capacitance2_fall

Although it is usually valid to specify only half of the receiver modeling information for the half-nate timing arcs. However, in some corner cases, we may need the full receiver modeling information.

In the following example,the receiver_capacitance1_fall group and the receiver_capacitance2_fall group are not specified for the half-unate timing arc.

```
timing() {
  timing_type : rising_edge;
  timing_sense : positive_unate;
  ...
  receiver_capacitance1_rise(basic_template_8x7) {
              index_1 ("0, 0.00081298, 0.0188997, 0.0460298, 0.0912466,
 0.18168, 0.452981, 0.905149");
              index_2 ("0.019368, 0.049573, 0.0948806, 0.170393,
 0.321418, 0.774494, 1.52962");
```

```
                values ("0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038");
  }
  receiver_capacitance2_rise(basic_template_8x7) {
                index_1 ("0, 0.00081298, 0.0188997, 0.0460298, 0.0912466,
 0.18168, 0.452981, 0.905149");
                index_2 ("0.019368, 0.049573, 0.0948806, 0.170393,
 0.321418, 0.774494, 1.52962");
                values ("0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038", \
                   "0.00165664, 0.00165664, 0.00165936, 0.00166126,
 0.00166211, 0.00166425, 0.00167038");
  }
  ...
}
```

```
Warning: Line 673, The timing arc does not have full receiver modeling
 information. (LBDB-390)
```

What Next

If possoble, add the missing receiver modeling information in the library.

Feedback

LBDB-674

(information) The 1st pair of (%s, %s) index of timing arc\n \t'%s' is (%g, %g) which is larger than recommended (%g, %g).

Description

This information occurs when the 1st index values of the timing arc are larger than the recommended values.

The following example shows an instance where this message occurs:

```
cell_rise(template) {
      index_1("1.0 ,2.0,4.0,6.0,10.0"); /* total_output_net_capacitance
 */
      index_2("0.362,0.725,1.087,1.449,1.812"); /* input_transition_time
 */
      ...
  }
```

The following is an example message:

```
Information: Line 20068, The 1st pair of
 (total_output_net_capacitance,input_transition_time) index of timing arc
       'cell_rise' is (1.0, 0.362) which is larger than recommended (0,
 0).  (LBDB-674)
```

What Next

Make sure the 1st index values are not larger than the recommended.

LBDB-675

(information) The 1st %s index of timing arc\n \t'%s' is %g, which is larger than recommended %g.

Description

This information occurs when the 1st index value of the timing arc is larger than the recommended value.

The following example shows an instance where this message occurs:

```
cell_rise(template) {
      index_1("1.0 ,2.0,4.0,6.0,10.0"); /* total_output_net_capacitance
 */
      ...
  }
```

The following is an example message:

```
Information: Line 20068, The 1st total_output_net_capacitance index of
 timing arc
        'cell_rise' is 1.0, which is larger than recommended 0.
 (LBDB-675)
```

What Next

Make sure the 1st index value is not larger than the recommended.

LBDB-676

(information) The significant digits of values in timing arc '%s' is %d,\n \twhich is less than recommended %d.

Description

This information occurs when the significant digits of values in the specified table is less than the recommended number.

The following example shows an instance where this message occurs:

```
cell_rise(template) {
      ...
      values("0.459,0.651,0.843,1.034,1.225",\
      ...);
  }
```

The following is an example message:

```
Information: Line 454, The significant digits of values in timing arc
 'cell_rise' is 4,
        which is less than recommended 5. (LBDB-676)
```

What Next

Make sure the significant digits is not less than the recommended.

LBDB-677

(warning) The table size of timing arc '%s' is %dx%d,\n \twhich is less than recommended %dx%d.

Description

This information occurs when the table size is less than the recommended number.

Feedback

The following example shows an instance where this message occurs:

```
cell_rise(template) {
      index_1("1.0 ,2.0,4.0,6.0,10.0"); /* total_output_net_capacitance
 */
      index_2("0.362,0.725,1.087,1.449,1.812"); /* input_transition_time
 */
      ...
  }
```

The following is an example message:

```
Warning: Line 446, The table size of timing arc 'cell_rise' is 5x5,
        which is less than recommended 7x7. (LBDB-677)
```

What Next

Make sure the table size is not less than the recommended.

LBDB-678

(warning) The table size of timing arc '%s' is %d,\n \twhich is less than recommended %d.

Description

This information occurs when the table size is less than the recommended number.

The following example shows an instance where this message occurs:

```
cell_rise(template) {
      index_1("1.0 ,2.0,4.0,6.0,10.0"); /* total_output_net_capacitance
 */
      ...
  }
```

The following is an example message:

```
Warning: Line 446, The table size of timing arc 'cell_rise' is 5,
        which is less than recommended 7. (LBDB-678)
```

What Next

Make sure the table size is not less than the recommended.

LBDB-679

(error) Can not find the %s of the %spin%s.

Feedback

Description

This information occurs when pin's max_capacitance/min_capacitance or the related_pin's max_transition information can not be found.

The following example shows an instance where this message occurs:

```
cell ( INV ) {
    area : 1 ;
    pin ( A ) {
      direction : input ;
      capacitance : 1 ;
      fanout_load : 1 ;
      ...
    }
    pin ( Z ) {
      related_pin :  A ;
      direction : output ;
      capacitance : 1 ;
      fanout_load : 1 ;
      ...
    }
  }
```

The following is an example message:

```
Error: Line 446, Can not find the max_transition of the input pin 'A'.
 (LBDB-679)
Error: Line 446, Can not find the min_capacitance of the  pin 'Z'.
 (LBDB-679)
Error: Line 446, Can not find the max_capacitance of the  pin 'Z'.
 (LBDB-679)
```

What Next

Make sure the max_transition/max_capacitance/min_capacitance information are defined in the source .lib file.

LBDB-680

(warning) The max value of %s index of group '%s' is %g,\n \twhich is less than max %s of pin '%s', %g.

Description

This information occurs when the max value of the specified index is less than the max constraint for the pin.

Feedback

In 10nm library, the index of input_net_transition of CCS receiver model will be checked using these ways in order of priority:

1) If driver waveform is defined, choose driver waveform matching the max_transition of related input pin, masure the transition time used in characterization of C1/C2 respectively from driver waveform, then use the restored transition time as constraint.

2) If driver waveform is NOT defined, use 80% of the max_transition value of related input pin as constraint.

The following example shows an instance where this message occurs:

```
pin(y) {
     direction   : input;
     min_capacitance : 0.361;
     max_capacitance : 1.813;
     max_transition : 0.5;
     cell_rise(template) {
       index_2("0.362,0.725,1.087,1.449,1.812"); /* total_out_net_cap  */
       ...
     }
     ...
   }
```

The following is an example message:

```
Warning: Line 762, The max value of total_out_net_cap index of timing arc
 'cell_rise' is 1.812,
        which is less than max total_out_net_cap of pin 'y', 1.813.
 (LBDB-680)

Warning: Line 1117, Cell 'dfnrb4', The max value of 1st index of group
 'receiver_capacitance1_fall' is 1755.58,
        which is less than max transition restored from driver_waveform
 of pin 'CP', 2369.48. (LBDB-680)

Warning: Line 78450, Cell 'r0hd_eln20_cbgclnbt06p00', The max value of
 1st index of group 'receiver_capacitance1_rise' is 0.4035,
        which is less than max transition with a 20.0 percent tolerance
 of pin 'root_clk_off', 1.2. (LBDB-680)
```

What Next

Make sure the max index value is not less than the constraint.

LBDB-681

(warning) The min value of %s index of timing arc '%s' is %g,\n \twhich is bigger than min %s of pin '%s', %g.

Feedback

Description

This information occurs when the min value of the specified index is larger than the min constraint for the pin.

The following example shows an instance where this message occurs:

```
pin(y) {
     direction   : input;
     min_capacitance : 0.361;
     max_capacitance : 1.813;
     max_transition : 0.5;
     cell_rise(template) {
       index_2("0.362,0.725,1.087,1.449,1.812"); /* total_out_net_cap  */
       ...
     }
     ...
   }
```

The following is an example message:

```
Warning: Line 762, The min value of total_out_net_cap index of timing arc
 'cell_rise' is 0.362,
        which is larger than min total_out_net_cap of pin 'y', 0.361.
 (LBDB-681)
```

What Next

Make sure the min index value is not larger than the constraint.

LBDB-682

(warning) The values in timing arc '%s' are nonmonotonic %g, %g,\n \twhen %s = %g.

Description

This information appears when the delay values in the specified table do not increase monotonically with the increasing capacitance.

The following example shows an instance where this message occurs:

```
cell_rise(template) {
      index_1("1.0 ,2.0,4.0,6.0,10.0"); /* input_transition_time */
      index_2("0.362,0.725,1.087,1.449,1.812"); /*
 total_output_net_capacitance */
      values ("1.405, 1.116...")
  }
```

Feedback

The following is an example message:

```
Warning: Line 762, The values in timing arc 'cell_rise' are non monotonic
 1.405, 1.116,
        when input_net_transition = 1.    (LBDB-682)
```

What Next

Make sure that the delay values increase monotonically with the increasing capacitance.

LBDB-683

(warning) The table is a load independent table.

Description

This information occurs when the template of one table do not have the total_output_net_capacitance index where it is needed.

The following example shows an instance where this message occurs:

```
lu_table_template(transition1x5){
    variable_1 : input_net_transition;
    index_1("0.5,1.0,1.5,2.0,2.5");
 }
 ...
 cell (AND) {
   pin(y) {
      ...
      cell_rise(transition1x5) {
        index_1("0.362,0.725,1.087,1.449,1.812"); /* input_net_transition
 */
        ...
      }
      ...
   }
   ...
 }
```

The following is an example message:

```
Warning: Line 762, The table is a load independent table. (LBDB-683)
```

What Next

Make sure the table use the correct template which is with total_output_net_capacitance index.

LBDB-684

(warning) The table is a scalar table.

Feedback

Description

This information occurs when the template of one table do not have any index where it is needed.

The following example shows an instance where this message occurs:

```
lu_table_template(scalar_template){
 }
 ...
 cell (AND) {
   pin(y) {
     ...
     cell_rise(scalar_template) {
        values ("...");
     }
     ...
   }
   ...
 }
```

The following is an example message:

```
Warning: Line 762, The table is a scalar table. (LBDB-684)
```

What Next

Make sure the table use the correct template which is with index.

LBDB-685

(warning) The voltage range of %s is %g->%g,\n \twhich is less than recommended %g->%g.

Description

This information occurs when the range of voltage index for IV curves is less than the recommended.

The following example shows an instance where this message occurs:

```
...
   iv_lut_template ("LUT_TEMPLATE_13570_t") {
        variable_1 : "iv_output_voltage";
        index_1("-1.500000, -0.611850, -0.019800, 0.009900, 0.246750,
 0.868350, 1.016400, 1.578900, 2.526300, 3.000000");
   }
     ...
    timing () {
      steady_state_current_low ("LUT_TEMPLATE_13570_t") {
                    values("-1.500000, -0.611850, -0.019800, 0.009900,
 0.246750, 0.868350, 1.016400, 1.578900, 2.526300, 3.000000");
```

Feedback

```
      }
    }
```

The following is an example message:

```
Warning: Line 780, The voltage range of steady_state_current_low is
 -1.5->3,
        which is less than recommended -5->10. (LBDB-685)
```

What Next

Make sure the voltage range is not less than the recommended.

LBDB-686

(warning) There is potential extrapolation problem\n \t%s[%g, %g, %g]=%g (> %g).

Description

This information occurs when the noise value extrapolated with the boundary values is larger than the recommended zero value.

The following example shows an instance where this message occurs:

```
propagated_noise_width_below_low(my_noise_propagation){
      index_1("0.00250, 0.00500, 0.01000, 0.01500, 0.02500, 0.03750,
 0.05000"); /*total_output_net_capacitance*/
      index_2("0.400,1.000,1.500,2.000"); /*input_noise_width*/
      index_3("0.36000,0.54000,0.72000,0.90000");
      values("0.025, 0.024, 0.010, 0.013",\
             "1.071, 0.342, 0.121, 0.222",\
             "0.489, 0.565, 0.789, 0.750",\
             "0.282, 0.021, 0.279, 0.118",\
             "0.034, 0.042, 0.009, 0.015",\
             "1.068, 0.346, 0.121,...);
  }
```

The following is an example message:

```
Warning: Line 215, There is potential extrapolation problem
        Width[0.05, 1, 0]=0.376 (> 0.1). (LBDB-686)
```

What Next

Make sure the boundary values in the table correct.

LBDB-687

(warning) There is potential extrapolation problem\n \t%s[%g, %g]=%g (> %g).

Feedback

Description

This information occurs when the noise value extrapolated with the boundary values is larger than the recommended zero value.

The following example shows an instance where this message occurs:

```
propagated_noise_width_below_low(my_noise_propagation){
      index_1("0.400,1.000,1.500,2.000"); /*input_noise_width*/
      index_2("0.36000,0.54000,0.72000,0.90000");
      values("0.025, 0.024, 0.010, 0.013",\
             "1.071, 0.342, 0.121, 0.222",\
             "0.489, 0.565, 0.789, 0.750",\
             "0.282, 0.021, 0.279, 0.118");
  }
```

The following is an example message:

```
Warning: Line 215, There is potential extrapolation problem
        Width[1, 0]=2.529 (> 0.1). (LBDB-687)
```

What Next

Make sure the boundary values in the table correct.

LBDB-688

(warning) The curve is curling upwards at the end.\n \twhen total_output_net_capacitance=%g.

Description

This information occurs when the immunity curve curls upwards at the end of the curve.

The following example shows an instance where this message occurs:

```
noise_immunity_high (my_noise_reject) {
    values ("1.3, 0.8, 0.7, 0.6, 0.55", \
            "1.5, 0.9, 0.8, 0.65, 0.6", \
            "1.5, 0.9, 0.8, 0.65, 0.6", \
            "1.5, 0.9, 0.8, 0.65, 0.6", \
            "-1.5, 1.9, 0.8, 0.65, 0.6") ;
  }
```

The following is an example message:

```
Warning: Line 178, The curve is curling upwards at the end.
        when total_output_net_capacitance=0.1. (LBDB-688)
```

Feedback

What Next

Make sure each last 2 values with the same total_output_net_capacitance index are almost identical.

LBDB-689

(warning) The curve is not leveling off at the end.\n \twhen total_output_net_capacitance= %g.

Description

This information occurs when the immunity curve is not leveling off at the end.

The following example shows an instance where this message occurs:

```
noise_immunity_high (my_noise_reject) {
    values ("1.3, 0.8, 0.7, 0.6, 0.55", \
            "1.5, 0.9, 0.8, 0.65, 0.6", \
            "1.5, 0.9, 0.8, 0.65, 0.6", \
            "1.5, 0.9, 0.8, 0.65, 0.6", \
            "-1.5, 1.9, 0.8, 0.65, 0.6") ;
  }
```

The following is an example message:

```
Warning: Line 178, The curve is not leveling off at the end.
        when total_output_net_capacitance=0. (LBDB-689)
```

What Next

Make sure each last 2 values with the same total_output_net_capacitance index are almost identical.

LBDB-690

(error) The current polarity is reversed.

Description

This information occurs when the current polarity is reversed.

The following example shows an instance where this message occurs:

```
steady_state_current_low(my_current_low) {
    values("0.1, 0.05, 0, -0.1, -0.25, -1, -1.8");
  }
```

The following is an example message:

```
Error: Line 198, The current polarity is reversed. (LBDB-690)
```

Feedback

What Next

Make sure the skew of the current at middle point is correct.

LBDB-691

(error) There is negative or zero values in the table.

Description

This information occurs when the value in the table is negative or zero where it should be positive.

The following example shows an instance where this message occurs:

```
propagated_noise_height_below_low(my_noise_propagation){
  ...
          values ("-1.4 ..");
```

The following is an example message:

```
Error: Line 198, There is negative values in the table. (LBDB-691)
```

What Next

Make sure the values in the table are positive.

LBDB-692

(warning) The max height of the noise table %s is %g,\n \twhich is less than recommended %g.

Description

This information occurs when the max height of the noise table is less than the recommended.

The following example shows an instance where this message occurs:

```
propagated_noise_height_below_low(my_noise_propagation){
                index_1("0.00250, 0.00500, 0.01000, 0.01500, 0.02500,
 0.03750, 0.05000");
                index_2("0.400,1.000,1.500,2.000");

 index_3("0.36000,0.54000,0.72000,0.90000"); /*input_noise_height*/
```

The following is an example message:

```
Warning: Line 248, The max height of the noise table
 propagated_noise_height_below_low is 0.9,
        which is less than recommended 5. (LBDB-692)
```

Feedback

What Next

Make sure the max height is not less than the recommended.

LBDB-693

(warning) The max width of the noise table %s is %g,\n \twhich is less than recommended %g.

Description

This information occurs when the max width of the noise table is less than the recommended.

The following example shows an instance where this message occurs:

```
propagated_noise_height_below_low(my_noise_propagation){
                index_1("0.00250, 0.00500, 0.01000, 0.01500, 0.02500,
 0.03750, 0.05000");
                index_2("0.400,1.000,1.500,2.000"); /*input_noise_width*/
                index_3("0.36000,0.54000,0.72000,0.90000");
```

The following is an example message:

```
Warning: Line 281, The max width of the noise table
 propagated_noise_width_low is 2,
        which is less than recommended 4. (LBDB-693)
```

What Next

Make sure the max width is not less than the recommended.

LBDB-694

(warning) The width range of %s is %g->%g,\n \twhich is less than recommended %g->%g.

Description

This information occurs when the width index does not have enough range.

The following example shows an instance where this message occurs:

```
noise_immunity_above_high (my_noise_reject_outside_rail) {
    index_1("0, 0.1, 2"); /*input_noise_width*/
    values ("1, 0.8, 0.5", \
            "1, 0.8, 0.5", \
            "1, 0.8, 0.5");
  }
```

Feedback

The following is an example message:

```
Warning: Line 192, The width range of noise_immunity_above_high is 0->2,
        which is less than recommended 2->4. (LBDB-694)
```

What Next

Make sure the width index have the enough range.

LBDB-695

(error) The pin '%s' misses DC noise margin.

Description

This information occurs when one pin does not DC noise margin information.

The following example shows an instance where this message occurs:

```
pin(a) {
            direction   : input;
            capacitance : 1.000;
        }
```

The following is an example message:

```
Error: Line 794, The pin 'a' misses DC noise margin. (LBDB-695)
```

What Next

Make sure there is DC noise margin information defined in one pin if no other noise information.

LBDB-696

(warning) The timing arc misses noise %s information.

Description

This information occurs when the timing arc does not have specified noise information.

The following is an example message:

```
Warning: Line 137, The timing arc misses noise
 propagated_noise_width_high information. (LBDB-696)
```

What Next

Make sure there is complete noise information defined in the timing arc.

Feedback

LBDB-697

(warning) The timing arc %s->%s misses noise %s_%s information.

Description

This information occurs when the timing arc does not have specified noise information.

The following is an example message:

```
Warning: Line 137, The timing arc DA[0]->QB[0] misses noise
 propagated_noise_width_above_high information. (LBDB-697)
```

What Next

Make sure there is complete noise information defined in the timing arc.

LBDB-698

(warning) The values in noise table '%s' are non monotonous\n \t%g, %g, when %s = %g, %s = %g.

Description

This information occurs when the delay values in specified table do not decrease monotonously with increasing capacitance.

The following example shows an instance where this message occurs:

```
propagated_noise_width_below_low(my_noise_propagation){
                index_1("0.00250, 0.00500, 0.01000, 0.01500, 0.02500,
 0.03750, 0.05000");
                index_2("0.400,1.000,1.500,2.000");
                index_3("0.36000,0.54000,0.72000,0.90000");
                values("0.000, 0.024, 0.010, 0.013",\
                       "1.071, 0.342, 0.121, 0.222",\
                       "0.489, 0.565, 0.789, 0.750",\
                       "0.282, 0.021, 0.279, 0.118",\
                       "1.000, 0.042, 0.009, 0.015",\
                       "1.068, 0.346, 0.121, 0.248",\
                       "0.497, 0.584, 0.786, 0.777",\
                       "0.271, 0.029, 0.281, 0.120",\
                       "0.055, 0.074, 0.008, 0.017",\
                       "1.076, 0.356, 0.121, 0.306",\
                       "0.481, 0.612, 0.783, 0.778",\
                       "0.257, 0.045, 0.288, 0.103",\
                       "0.072, 0.102, 0.006, 0.018",\
                       "1.098, 0.367, 0.121, 0.359",\
                       "0.506, 0.646, 0.779, 0.770",\
                       "0.248, 0.057, 0.295, 0.105",\
                       "0.102, 0.161, 0.002, 0.018",\
```

```
                        "1.162, 0.392, 0.118, 0.437",\
                        "0.571, 0.707, 0.775, 0.763",\
                        "0.238, 0.076, 0.311, 0.107",\
                        "0.142, 0.202, 0.002, 0.059",\
                        "0.389, 0.426, 0.102, 0.541",\
                        "0.673, 0.775, 0.772, 0.768",\
                        "0.235, 0.094, 0.329, 0.109",\
                        "0.180, 0.246, 0.005, 0.071",\
                        "0.434, 0.463, 0.090, 0.644",\
                        "0.705, 0.835, 0.758, 0.783",\
                        "0.235, 0.108, 0.345, 0.111");
            }
```

The following is an example message:

```
Warning: Line 248, The values in noise table
 'propagated_noise_height_below_low' are non monotonous
        0.025, 1.000, when input_noise_width = 0.4, input_noise_height =
 0.36. (LBDB-698)
```

What Next

Make sure the delay values decrease monotonously with increasing capacitance.

LBDB-699

(error) The 'generic' integrated clock gating cell '%s' should only have at most 1 inout/output pin with \n \tattribute 'clock_gate_out_pin' set to true.

Description

This message indicates that you specified the 'generic' integrated gating clock cell can only have 1 inout/output pin with 'clock_gate_out_pin : true'.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";
  ...
  pin(O1) {
                direction : output;
                clock_gate_out_pin : true;
                ...
  }
  pin(O2) {
                direction : output;
                clock_gate_out_pin : true;
                ...
  }
  ...
}
```

Feedback

```
The modified cell description can be :

cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";
  ...
  pin(O1) {
                direction : output;
                clock_gate_out_pin : true;
                ...
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The 'generic' integrated clock gating cell 'CGNP' should
 only have at most 1 inout/output pin with \n
        attribute 'clock_gate_out_pin' set to true. (LBDB-699)
```

What Next

Change the library source file.

LBDB-700

(error) The pin '%s' of the 'generic' integrated clock gating cell '%s' can not define\n \t attribute 'state_function'. It should use attribute 'function" instead.

Description

This message indicates that you specified attribute 'state_function' in the 'generic' integrated gating clock cell. It should be changed as 'function'.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  clock_gating_integrated_cell : "generic";
  ...
  pin(O1) {
                direction : output;
                state_function : "!(IQ + SE) * CP_IN"
                ...
  }
  ...
}

The modified cell description can be :

cell(CGNP) {
```

Feedback

```
  area : 1;
  clock_gating_integrated_cell : "generic";
  ...
  pin(O1) {
                direction : output;
                function : "!(IQ + SE) * CP_IN"
                ...
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The pin 'O1' of the 'generic' integrated clock gating
 cell 'CGNP' can not define attribute 'state_function'. It should use
 attribute 'function" instead. (LBDB-700)
```

What Next

Change the library source file by replacing "state_function" to "function".

LBDB-701

(error) The %scell '%s' can not define pin functions of both '%s' and '%s'.

Description

Assume the integrated clock gating cell is modeled as :

... clock_gating_integrated_cell : "generic"; latch("IQ", "IQN") { data_in : "EN1 * EN2" ; enable : "CLK"' ; } ...

This message indicates that you specified pin functions for either one of the following 2 cases, which is invalid: 1. the same pin function with both IQ and IQN. for example, pin(Y1) { function : "IQ * (A + IQN)"; ... }

1. the different pin functions involved with IQ and IQN. for example, pin(Y1) { function : "IQ * A"; ... } pin(Y2) { function : "IQN * A"; ... }

The following is an example message:

```
Error: Line 206, The integrated clock gating cell '%s' can not define pin
 functions of both '%s' and '%s'. (LBDB-701)
```

What Next

Change the library source file by replacing "IQN" to "IQ"'.

Feedback

LBDB-702

(error) The cell should not define the 'statetable' group. \n \tIt should use 'ff' group or 'latch' group instead.

Description

This message indicates that you specified statetable and the pin function of "...IQ..." or "...IQN..."(excluding "IQ" and IQN", where IQ and IQN are the outptut of sequential element. You should define 'ff/latch' group instead.

The following example shows an instance where this message occurs:

```
cell(A) {
  area : 1;
  ...
  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,\
               L  H  : - : H ,\
               H  -  : - : N ";
  }

  pin(Y) {
        function : "IQ * CP";
        ...
  }
  ...
}

The modified cell description should be :

cell(A) {
  area : 1;

  latch("IQ","IQN") {
    enable : "CP'";
    data_in : "EN";
  }
  ...
  pin(Y) {
        function : "IQ * CP";
        ...
  }
}
```

The following is an example message:

```
Error: Line 206, The cell should not define the 'statetable' group.
        It should use 'ff' group or 'latch' group instead. (LBDB-702)
```

Feedback

What Next

Change the library source file, and replace the statetable group with the ff/latch group of the specified cell.

LBDB-703

(error) An invalid %s '%s' is found in the '%s' group.

Description

The message is to notify users that either the attribute/group should not be defined in the relative parent group, or the value of the attribute/group need to be corrected.

What Next

Remove the attribute/group or correct the value of the attribute/group and rerun the command.

LBDB-704

(warning) The standard cells '%s' and '%s' does not have the same pg_pin configuration.

Description

The message is to notify users that all the standard cells(cells having 1 primary_power pg_pin and 1 primary_ground pg_pin) should have exactly the same pg_pin configuration: - all the primrary_power pg_pins of these cells have the same "voltage_name" - all the primrary_ground pg_pins of these cells have the same "voltage_name"

What Next

Correct the "voltage_name" attribute values of the pg_pins of the standard cells and rerun the command.

LBDB-705

(warning) The '%s' %s group has been defined multiple times in\n \tthe '%s' %s group. Using the last definition encountered.

Description

The library contains more than one definition of a group. The Library Compiler issues this error message, ignores the previous definitions, and takes into consideration the last definition encountered.

Feedback

The following example shows an instance where this message occurs:

```
cell(sample) {
        ...
        pg_pin(A) {
          ...
        }
        pg_pin(A) {
          ...
        }
        ...
    }
```

The following is an example message:

```
Warning: Line 50, The 'A' pg_pin group has been defined multiple times in
        the 'sample' cell group. Using the last definition encountered.
 (LBDB-705)
```

What Next

Change the group name if it is wrong, or delete the second definition.

LBDB-706

(error) %s analysis failed during CCS or CCB Noise compilation

Description

This error message reports that the ccsn_first_stage, ccsn_last_stage, input_ccb, or output_ccb at the line indicated cannot be compiled successfully. The analysis of an output_voltage_rise/fall data set fails.

If there is an LBDB-953 warning also associated with this stage, please consult the man page on LBDB-953 on how to debug the dc_current table.

If there is an LBDB-15 (or LBDB-954w, LBDB-955 specifically for N10) warning also associated with this stage, please consult the corresponding man page on how to correct the miller capacitance values.

If the cell is a level shifter, or has multiple pg_pins (primary_power, backup_power, or internal_power) of different voltages, LDBD-706 is likely to occur on those low-to-high level-shifting ccs noise stages. Please look for LBDB-939 warning to get more details.

Otherwise, make sure all capacitance values (miller_cap_rise/fall, and total_output_net_capacitance) are reasonable. Look for an LBDB-955 warning on miller_cap_rise/fall. Check to make sure index_2 (total_output_net_capacitance) values of all vector groups within the output_voltage_rise/fall group are smaller than the largest output load of delay and slew lookup tables.

Finally, examine index_1 (input_net_transition) values of all vector groups within the output_voltage_rise/fall group. They should not be smaller than the second smallest index_1 (input_net_transition) values of delay and slew lookup tables.

What Next

Correct the CCS or CCB Noise data accordingly.

LBDB-706w

(warning) %s analysis failed during CCS or CCB Noise compilation

Description

This warning message reports that the ccsn_first_stage, ccsn_last_stage, input_ccb, or output_ccb at the line indicated cannot be compiled successfully. The analysis of an output_voltage_rise/fall data set fails.

If there is an LBDB-953 warning also associated with this stage, please consult the man page on LBDB-953 on how to debug the dc_current table.

If there is an LBDB-15 (or LBDB-954w, LBDB-955 specifically for N10) warning also associated with this stage, please consult the corresponding man page on how to correct the miller capacitance values.

If the cell is a level shifter, or has multiple pg_pins (primary_power, backup_power, or internal_power) of different voltages, LDBD-706w is likely to occur on those low-to-high level-shifting ccs noise stages. Please look for LBDB-939 warning to get more details.

Otherwise, make sure all capacitance values (miller_cap_rise/fall, and total_output_net_capacitance) are reasonable. Look for an LBDB-955 warning on miller_cap_rise/fall. Check to make sure index_2 (total_output_net_capacitance) values of all vector groups within the output_voltage_rise/fall group are smaller than the largest output load of delay and slew lookup tables.

Finally, examine index_1 (input_net_transition) values of all vector groups within the output_voltage_rise/fall group. They should not be smaller than the second smallest index_1 (input_net_transition) values of delay and slew lookup tables.

What Next

Correct the CCS or CCB Noise data accordingly.

LBDB-707

(information) Compiling CCS Noise data --- %%d...

Feedback

Description

This message is for information purposes only and it is to show the process of compiling CCS noise data.

The following is an example message:

```
Information: Compiling CCS Noise data --- 10%... (LBDB-707)
Information: Compiling CCS Noise data --- 20%... (LBDB-707)
 ...
Information: Compiling CCS Noise data --- 100%... (LBDB-707)
```

LBDB-708

(error) The timing arc has '%s' timing_sense, which is not consistent with \n \tthe "is_inverting" attribute value(s) of its %s group(s).

Description

```
In the following descriptions, "input ccb" stands for input_ccb in new
 noise
model or ccsn_first_stage in old noise model, and "output ccb" stands for
output_ccb in new noise model or ccsn_last_stage in old noise model.

This message is to indicate that the "is_inverting" attribute value of
 the
"input ccb"/"output ccb" group(s) defined in the timing arc is not
 consistent
with the timing_sense of the arc.

The correct configuration should be:
1. If the timing sense is "positive_unate", then it can only contain
 either 1
"input ccb" with "FALSE" "is_inverting" attribute,
or 1 "input ccb" with "TRUE" "is_inverting" attribute and 1 "output ccb"
 with
"TRUE" "is_inverting" attribute,
or 1 "input ccb" with "FALSE" "is_inverting" attribute and 1 "output ccb"
 with
"FALSE" "is_inverting" attribute.
2. If the timing sense is "negative_unate", then it can only contain
 either 1
"input ccb" with "TRUE" "is_inverting" attribute,
or 1 "input ccb" with "TRUE" "is_inverting" attribute and 1 "output ccb"
 with
"FALSE" "is_inverting" attribute,
or 1 "input ccb" with "FALSE" "is_inverting" attribute and 1 "output ccb"
 with
"TRUE" "is_inverting" attribute.
```

Feedback

The following is an example message:

```
Error: Line 50, The timing arc has 'negative_unate' timing_sense, which
 is not
consistent with the "is_inverting" attribute values of its
 input_ccb/output_ccb
group(s). (LBDB-708)
```

LBDB-709

(error) '%s' cannot be used in the timing arc.

Description

This particular timing arc cannot have the aforementioned group or attribute because it is not a delay arc, or its timing sense is not positive or negative unate. (Non-unate timing sense typically occurs in sequential arcs.)

The following is an example message:

Error: Line 2077, Cell 'LL_SSYNCCFD1QSX010', pin 'Q', 'ccsn_first_stage' cannot be used in the timing arc.

What Next

correct the timing type or sense. Or remove the group or attribute.

LBDB-710

(error) The table size of '%s' is %dx%d,\n \twhich is less than the required %dx%d.

Description

This information occurs when the table size is less than the required number.

The following example shows an instance where this message occurs:

```
dc_current(template) {
      index_1("1.0") ; /* input_voltage */
      index_2("0.362"); /* output_voltage */
      ...
  }
```

The following is an example message:

```
Warning: Line 446, The table size of 'dc_current' is 5x5,
        which is less than the required 6x6. (LBDB-710)
```

What Next

Make sure the table size is not less than the recommended.

Feedback

LBDB-711

(error) a %s pin cannot specify the '%s' %s.

Description

This error message occurs when there is a mismatch between the direction of a pin and the CCS Noise data. Library Compiler fails if the following rules are not satisfied:

```
1. An input pin can only specify at least 1 ccsn_first_stage group.

2. An inout pin can specify both ccsn_first_stage group and
 ccsn_last_stage group.

3. An output pin can only specify ccsn_last_stage group.
```

The following example shows an instance where this message occurs: The following is an example of incorrect input that causes this error message:

```
cell(lbdb711) {
    ...
    pin(Y ) {
      direction : output;
      ...
      ccsn_first_stage() {
        ...
      }
    }
  }
```

In this case, the Y pin has the ccsn_first_stage group specified. To fix the error, change ccsn_first_stage to ccsn_last_stage.

What Next

Check the library source file and fix either the invalid CCS Noise data, or the direction of the pin.

LBDB-712

(warning) an %s pin should either specify at least one non-static\n \t'%s' in the pin group or specify noise data for all of its timing arcs.

Description

This warning message occurs because: 1. an inout or input pin should have: 1.1 at least one non-static ccsn_first_stage group in the pin group or define non-static ccs noise first stage data for all of its timing groups for CCSN modeling. 1.2 at least one non-static input_ccb group in the pin group for referenced CCSN modeling. 2. an inout or output pin should have: 2.1 at least one non-static ccsn_last_stage group in the pin group or define

Feedback

non-static ccs noise last stage data for all of its timing groups for CCSN modeling. 2.2 at least one non-static output_ccb group in the pin group for referenced CCSN modeling.

A static CCS noise model captures the behaviors of a static CCB (channel connected block). A static CCB refers to a CCB that does not have any input terminal or the voltage level at the input terminal does not affect the output current of the CCB. For example, a static CCS noise model can be characterized for a CMOS NAND gate when both inputs are tied to ground. Such static CCS noise models can be used in noise analysis with case analysis, but they cannot be used for propagating crosstalk delay or noise waveforms through the cell under study. See the *Make CCS Noise User Guide* for detailed information.

The following example shows an instance where this message occurs: In the following example, the Y pin does not have the ccsn_last_stage group specified, so the tool issues this warning message. To fix the problem, add the ccsn_last_stage group into the pin group.

```
cell(good) {
    ...
    pin(Y ) {
      direction : output;
      ...
      ccsn_last_stage() {
        ...
      }
      }
    }
  }
  cell(lbdb712) {
    ...
    pin(Y ) {
      /* no ccs noise information inside the pin group */
      direction : output;
      ...
      /* not all timing arcs inside the pin group has ccs noise data */
    }
  }
```

What Next

This is only a warning message. No action is required.

Feedback

However, you can do any of the following:

- Check the library source file and fix either the invalid CCS Noise data, or the direction of the pin.
- Safely ignore this warning if the following three categories of cells are identified in a library:
  - inverters: A cell always has 1 input pin and 1 output pin with the function as "!input" or "input'"
  - NAND: A cell always has 2 input or more and 1 output pin with the function as "!(input1 * input2 * ... input(n))" or "(input1 * input2 * ... input(n))'"
  - NOR: A cell always has 2 input or more and 1 output pin with the function as "!(input1 + input2 + ... input(n))" or "(input1 + input2 + ... input(n))'"

LBDB-713

(error) The '%s' group with %s '%s' attribute cannot specify following CCS or CCB Noise data: %s.

Description

This message indicates that if a ccsn_first_stage, ccsn_last_stage, input_ccb, or output_ccb group has 'is_needed' attribute set to FALSE, then it is not valid to specify the following noise data:

stage_type, is_inverting, miller_cap_rise, miller_cap_fall, dc_current, output_voltage_rise, output_voltage_fall, propagated_noise_low, propagated_noise_high.

The following example shows an instance where this message occurs:

```
cell(bad) {
    ...
    pin(Y ) {
      direction : output;
        ...
        ccsn_last_stage() {
                is_needed : FALSE;
                stage_type : both
                ...
        }
      }
    }
  }
```

Feedback

The following is an example message:

```
Error: Line 71, The 'ccsn_last_stage' group with FALSE 'is_needed'
 attribute
cannot specify following CCS or CCB Noise data: 'stage_type'. (LBDB-713)
```

What Next

Check the library source file, and remove the redundant CCS/CCB Noise data.

LBDB-714

(error) The '%s' group cannot specify the '%s' attribute with value '%s'.

Description

This message can be used to indicate that the output pin of a tie-off cell(pin function= "1" | "0", or driver_type = "pull_up" | "pull_down") specify incorrect value for the stage_type attribute of the ccsn_first_stage/ccsn_last_stage groups defined on the pin, which must satisfy the following rules: 1. If the driver pin with driver_type = pull_up or function = "1", then its ccsn_first_stage/ccsn_last_stage group must have the stage_type attribute with value "PULL_UP". 2. If the driver pin with driver_type = pull_down or function = "0", then its ccsn_first_stage/ccsn_last_stage group must have the stage_type attribute with value "PULL_DOWN".

The following example shows an instance where this message occurs:

```
cell(bad) {
    ...
    pin(Y ) {
        direction : output;
        function : 1;
        driver_type : "pull_up";
        ...
        ccsn_last_stage() {
                is_needed : FALSE;
                stage_type : "pull_down";
                ...
        }
      }
    }
  }
```

In this case, the 'Y' pin specify 'pull_down' stage_type attribute in its 'ccsn_last_stage' group. To fix the problem, change the 'pull_down' to 'pull_up'.

The following is an example message:

```
Error: Line 71, The 'ccsn_last_stage' group cannot specify the
 'stage_type' attribute with value 'PULL_DOWN'. (LBDB-714)
```

Feedback

What Next

Check the library source file, and correct the incorrect 'stage_type' value.

LBDB-716

(error) The %s %g of '%s' attribute is %s %s = %g.

Description

This message indicates that the first/last/some value of the specific attribute is greater than the upper bound value, or lower than the lower bound value.

What Next

Check your library and correct the value.

LBDB-717

(error) The value %g of '%s' attribute is %s %g.

Description

This message indicates that the value of the specific attribute is greater than the upper bound value, or less than the lower bound value.

What Next

Check your library and correct the value.

LBDB-718

(warning) The %s %g of '%s' attribute is %s %s = %g.

Description

This message indicates that the first/last/some value of the specific attribute is greater than the upper bound value, or lower than the lower bound value. Note that this is just a warning, not an error.

What Next

Check your library and correct the value.

LBDB-719

(error) The cell must have at least 1 'primary_ground' pg_pin and at least 1 'primary_power' pg_pin. It's being marked as dont_use, dont_touch.

Feedback

Description

This error message occurs when a primary_ground pg_pin or a primary_power pg_pin is missing. Cell in the following list could occurs this message, if it doesn't have at least 1 primary_ground pg_pin and at least 1 primary_power pg_pin. (1) The cell is a macro cell. (2) The cell has function info. (except for tie-off cell) (3) The cell has timing/noise/power info.

What Next

Add the missing primary_ground pg_pin or primary_power pg_pin and run the command again.

LBDB-720

(error) The '%s' %s cannot be specified in the library\n \tbased on pg_pin.

Description

This message indicates that you specified the syntax(power_supply, rail_connection, input/output_signal_level, power_level, etc.) which is incompatible with the syntax based on pg_pin such as voltage_map, pg_pin, related_power/ground_pin, related_pg_pin).

The following example shows an instance where this message occurs:

```
cell(lbdb720) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;

      input_signal_level : VDD;

      related_power_pin : VDD;
      related_ground_pin : VSS;

    }
    ...
  }
```

The following is an example message:

```
Error: Line 84, The 'input_signal_level' attribute cannot be specified in
 the library
        based on pg_pin. (LBDB-720)
```

Feedback

What Next

Refer to the "Library Compiler User Guide" for related information and emove the incompatible values,

---

LBDB-720w

(warning) The '%s' %s cannot be specified in the library\n \tbased on pg_pin.

Description

This message indicates that you specified the syntax(power_supply, rail_connection, input/output_signal_level, power_level, etc.) which is incompatible with the syntax based on pg_pin such as voltage_map, pg_pin, related_power/ground_pin, related_pg_pin).

The following example shows an instance where this message occurs:

```
cell(lbdb720) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1.0;

      input_signal_level : VDD;

      related_power_pin : VDD;
      related_ground_pin : VSS;

    }
    ...
  }
```

The following is an example message:

```
Warning: Line 84, The 'input_signal_level' attribute cannot be specified
 in the library
        based on pg_pin. (LBDB-720w)
```

What Next

Refer to the "Library Compiler User Guide" for related information and emove the incompatible values,

---

LBDB-721

(warning) The value %f of 'nom_voltage' is not the same as the value\n \t%f of 'voltage' of the default operating_conditions '%s'.

Feedback

Description

This message indicates that the nom_voltage valye is not equal to the value of "voltage" attribute of the default operating_conditions group of the library.

The following example shows an instance where this message occurs:

```
nom_voltage     : 1.09;

  operating_conditions(sample) {
    process     : 1;
    temperature : 85;
    voltage     : 1.08;
    tree_type   : balanced_tree
  }
```

The following is an example message:

```
Warning: Line 52, The value 1.09 of 'nom_voltage' is not the same as the
 value
        1.08 of 'voltage' of the default operating_conditions '%s'.
 (LBDB-721)
```

What Next

Correct the nominal_voltage value to make it the same as the value of the voltage attribute of the default operating_conditions group.

LBDB-722

(error) The voltage value %f of the 1st voltage_map '%s' is not the same as\n \tthe value of 'voltage' of the default operating_conditions '%s'.

Description

This message indicates the 1st specified voltage_map attribute specifiy the different voltage value from that of the 'voltage' of the default operating_consitions group if there are only two voltage_map specified in library. They should be equal.

The following example shows an instance where this message occurs:

```
voltage_map(VDD, 1.2);
      voltage_map(VSS, 0);
      operating_conditions(sample) {
        process     : 1;
        temperature : 85;
        voltage     : 1.08;
        tree_type   : balanced_tree
      }
      default_operating_conditions : sample;
```

Feedback

In this case, there are two voltage_map specified, and the voltage value of the 1st voltage_map 'VDD1' voltage_map is 1.2, while the voltage value of default operating_conditions 'sample' is 1.08. To Fix the problem, update the voltage_map 'VDD' as follows:

```
voltage_map(VDD, 1.08);
      voltage_map(VSS, 0);
      operating_conditions(sample) {
        process     : 1;
        temperature : 85;
        voltage     : 1.08;
        tree_type   : balanced_tree
      }
      default_operating_conditions : sample;
```

The following is an example message:

```
Error: Line 23, The voltage value 1.2 of the 1st voltage_map 'VDD' is not
 the same as\n
\tthe value of 'voltage' of the default operating_conditions 'sample'.
 (LBDB-722)
```

What Next

Correct the voltage value of the 1st voltage_map.

LBDB-723

(error) The last variable '%s' is '%s',\n \twhich is wrong. The value must be "time".

Description

This message indicates that the value of the last variable can only be "time" in pg_current_template. pg_current_template can have one variable up to 4 variables, and input_net_transition, time, and total_output_net_capacitance are 3 avaiable values can be assigned. No matter what size of template is, the last variable must be "time".

The following example shows an instance where this message occurs:

```
pg_current_template(basic_template) {
    variable_1 : input_net_transition;
    variable_2 : time;
    variable_3 : total_output_net_capacitance;
    variable_4 : total_output_net_capacitance;
  }
```

To fix the problem, exchange the values between variable_2 and variable_4.

Feedback

The following is an example message:

```
Error: Line 388, The last variable variable_4 is
 total_output_net_capacitance,
        which is wrong.  The value must be "time". (LBDB-723)
```

What Next

If the last variable is not "time", change the variable, which is assigned to "time", to the last.

LBDB-724

(error) There is no voltage_map defined for ground voltage value 0.

Description

This message indicates the library does not define the voltage_map for the ground voltage value 0. In the libraries based on the new power modeling syntax (voltage_map, pg_pin, ..., etc.), this condition myst be satisfied.

The following example shows an instance where this message occurs:

```
voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);

      operating_conditions(sample) {
        process     : 1;
        temperature : 85;
        voltage     : 1.08;
        tree_type   : balanced_tree
      }
      default_operating_conditions : sample;
```

In this case, there is no voltage_map defined for ground voltage value 0. To fix the problem, add the following voltage_map attribute at the library level:

```
voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);
      voltage_map(VSS, 0);

      operating_conditions(sample) {
        process     : 1;
        temperature : 85;
        voltage     : 1.08;
        tree_type   : balanced_tree
      }
      default_operating_conditions : sample;
```

Feedback

The following is an example message:

```
Error: Line 23, There is no voltage_map defined for ground voltage value
 0. (LBDB-724)
```

What Next

Add the voltage_map for the ground voltage value 0.

LBDB-725

(warning) Connect pin '%s' to the default %s pg_pin '%s'.

Description

Either the related_power_pin or the related_ground_pin attribute is missing in a pin. By default, LC connect this pin to the default related_power_pin/related_ground_pin.

The following example shows an instance where this message occurs:

```
voltage_map(VDD0, 1.8);
   voltage_map(VDD1, 1.9);
   voltage_map(VDD2, 23);
   voltage_map(VSS, 0);

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  pg_pin(PV1) {
    voltage_name : VDD1;
    pg_type : primary_power;
  }
  pg_pin(PV2) {
    voltage_name : VDD2;
    pg_type : primary_power;
  }
  pg_pin(VSS) {
    voltage_name : VSS;
    pg_type : primary_ground;
  }
  pin(A) {
    direction : input;
    capacitance : 1;
    /* missing related_power_pin attribute, will use default PV1 */
    related_ground_pin : VSS;
  }
  pin(Z) {
    direction : output;
    function : "A";
    related_power_pin : PV1;
    related_ground_pin : VSS;
    timing() {
```

Feedback

```
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
```

The following is an example message:

```
Warning: Line 96, Connect pin 'A' to the default power pg_pin 'PV1'.
 (LBDB-725)
```

What Next

Check the library source file to see if you missed the related_power_pin or the related_ground_pin attributes.

LBDB-726

(error) All the pins in the '%s' cell with more than 2 %s pg_pins\n \tmust have '%s' attribute.

Description

The related_power_pin (or the related_ground_pin) attribute is missing in a pin within a cell with more than 2 power pg_pins (or ground pg_pins) respectively.

The following example shows an instance where this message occurs:

```
voltage_map(VDD0, 1.8);
   voltage_map(VDD1, 1.9);
   voltage_map(VDD2, 23);
   voltage_map(VSS, 0);

cell(lbdb428) {
  area : 2;
  pad_cell : true;
  pg_pin(PV1) {
    voltage_name : VDD1;
    pg_type : primary_power;
  }
  pg_pin(PV2) {
    voltage_name : VDD2;
    pg_type : primary_power;
  }
  pg_pin(VSS) {
    voltage_name : VSS;
    pg_type : primary_ground;
  }
```

Feedback

```
  pin(A) {
    direction : input;
    capacitance : 1;
    /* missing related_power_pin attribute, will use default PV1 */
    related_ground_pin : VSS;
  }
  pin(Z) {
    direction : output;
    function : "A";
    related_power_pin : PV1;
    related_ground_pin : VSS;
    timing() {
      intrinsic_rise : 0.48;
      intrinsic_fall : 0.77;
      rise_resistance : 0.1443;
      fall_resistance : 0.0523;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A";
    }
  }
}
```

To fix the problem, add the attribute to the 'A' pin group,

```
related_power_pin : VDD1;
```

The following is an example message:

```
Error: Line 96, All the pins in the 'lbdb726' cell with more than 2 power
 pg_pins
        must have 'related_power_pin' attribute. (LBDB-726)
```

What Next

Check the library source file to see if you missed the related_power_pin or the related_ground_pin attributes.

LBDB-727

(error) The %s%s '%s' contains the conflicting %s \n \t'%s' for pin '%s' and %s '%s' for pin '%s'.

Description

This error message occurs when the *input_signal_level*, *output_signal_level*, or *related_power_pin* values is modeled incorrectly for the level shifter or isolation cell. See detail checking as described below.

Liberty supports two kinds of PG syntax: old and new.

Feedback

Rule for a level shifter in the old syntax:

The rail name of *input_signal_level* in input pin cannot be the same as rail name of *output_signal_level* in output pin.

Rule for a level shifter in the new syntax:

If *input_signal_level* and *related_power_pin* both present in input pin, then Library Compiler will choose the value of *input_signal_level* for comparison. Either *input_signal_level* or *related_power_pin* in input pin cannot refer to the same voltage name as what *related_power_pin* refers to in output pin.

Rule for an isolation cell in the old syntax:

The rail value of *input_signal_level* in input pin shall be the same as the rail value of *output_signal_level* in output pin.

Rule for an isolation cell in the new syntax:

The value of either *input_signal_level* or *related_power_pin* in input pin shall refer to the same voltage value as what *related_power_pin* refers to in output pin.

The following example shows a level shifter with incorrect modeling and the resulting error message in the new PG syntax:

```
library (test) {
 ...
 voltage_map( VSS, 0.0);
 voltage_map( VDDH, 0.9);
 voltage_map( VDDL, 0.7);
 ...
 cell(LS) {
 ...
 pg_pin(GND) {
 voltage_name : VSS;
 pg_type : primary_ground;
 }
 pg_pin(VDD2) {
 voltage_name : VDDH;
 pg_type : primary_power;
 }
 pg_pin(VDD1) {
 voltage_name : VDDL;
 pg_type : primary_power;
 }

 is_level_shifter : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDL;
        related_power_pin : VDD1;  /* discard */
```

```
        related_ground_pin : GND;
 }
 pin(out) {
        ...
        related_power_pin: VDD1;
        related_ground_pin : GND;
 }
}
```

In this case, input_signal_level "VDDL", which is the same voltage name as what related_power_pin "VDD1" is referring to.

```
Error: Line 191, The level shifter 'LS' contain the conflicting
 input_signal_level
        'VDDL' for pin 'in' and related_power_pin 'VDD1' for pin 'out'.
 (LBDB-727)
```

The following example shows the isolation cell with the incorrect modeling and the resulting error message in new pg syntax:

```
library (libdb727) {
 ...
 voltage_map( VDD, 0.7);
 voltage_map(VDDH, 0.80); /* high power */
 voltage_map(VDDL, 0.4); /* low power */
 voltage_map(VSS, 0.0);   /* primary ground */
 ...
 cell(ISO) {
 ...
 pg_pin(VDD1) {
 voltage_name : VDDH;
 pg_type : primary_power;
 }
 pg_pin(VDD2) {
 voltage_name : VDDL;
 pg_type : primary_power;
 }

 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        related_power_pin : VDD1;
        related_ground_pin : GND;
 }
 pin(out) {
        ...
        related_power_pin: VDD2;
        related_ground_pin : GND;
 }
}
```

Feedback

In this case, related_power_pin 'VDD1' is referred to voltage value 0.8 and related_power_pin 'VDD2' is referred to voltage value 0.4. So, the valtage value 0.8 in input pin is different from valtage value 0.4 in output pin, which is wrong.

```
Error: Line 191, The isolation cell 'ISO' contain the conflicting
 related_power_pin
        'VDD1' for pin 'in' and related_power_pin 'VDD2' for pin 'out'.
 (LBDB-727)
```

The following example shows the level shifter with the incorrect modeling and the resulting error message in the old PG syntax:

```
cell(LS) {
 is_level_shifter : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDD2

 }
 pin(out) {
        ...
        output_signal_level : VDD2

 }
}

Error: Line 191, The level shifter 'LS' contain the conflicting
 input_signal_level 'VDD2' for pin 'in' and output_signal_level 'VDD2'
 for pin 'out'. (LBDB-727)
```

The following example shows the isolation cell with the incorrect modeling and the resulting error message in old pg syntax:

```
library(libdb727) {
  ...
  /* operation conditions */
  operating_conditions(5v_1v) {
    ...
    power_rail (VDDH, 5);    /* high power */
    power_rail (VDDL, 1);    /* low power */
    ...
  }
  ...
  default_operating_conditions : 5v_1v;

  ...
cell(ISO) {
 is_isolation_cell : true;
 ...
 pin(in) {
        ...
```

```
        input_signal_level : VDDH
 }
 pin(out) {
        ...
        output_signal_level : VDDL
 }
}

Error: Line 191, The isolation cell 'ISO' contain the conflicting
 input_signal_level 'VDDH' for pin 'in' and output_signal_level 'VDDL'
 for pin 'out'. (LBDB-727)
```

What Next

For the first example, modify the modeling information of the level shifter to meet the requirements.

To correct the modeling of the example above, make the *input_signal_level* value of the input pin different from the *related_power_pin* value of the output pin as follows:

```
cell(LS) {
 is_level_shifter : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDL;
        related_power_pin: VDD1;
        related_ground_pin : GND;
 }
 pin(out) {
        ...
        related_power_pin: VDD2;
        related_ground_pin : GND;
 }
}


For the second example, modify the modeling information of the isolation
 cell to meet
the requirements.

To correct the modeling of the example above, make the
related_power_pin value of the input pin
same as the related_power_pin
value of the output pin as follows:

library (libdb727) {
 ...
 voltage_map( VDD, 0.7);
 voltage_map(VDDH, 0.80); /* high power */
 voltage_map(VDDL, 0.4); /* low power */
 voltage_map(VSS, 0.0);   /* primary ground */
 ...
```

Feedback

```
 cell(ISO) {
 ...
 pg_pin(VDD1) {
 voltage_name : VDDH;
 pg_type : primary_power;
 }
 pg_pin(VDD2) {
 voltage_name : VDDL;
 pg_type : primary_power;
 }

 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        related_power_pin : VDD1;
        related_ground_pin : GND;
 }
 pin(out) {
        ...
        related_power_pin: VDD1;
        related_ground_pin : GND;
 }
}
```

For the third example, modify the modeling information of the level shifter to meet the requirements.

To correct the modeling of the example above, make the *input_signal_level* string of the input pin different from the *output_signal_level* string "VDD2" of the output pin as follows:

```
cell(LS) {
 is_level_shifter : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDD1
 }
 pin(out) {
        ...
        output_signal_level : VDD2
 }
}
```

```
For the fourth example, modify the modeling information of the isolation
 cell
to meet the requirements.

input_signal_level 'VDDH' is referred to voltage value
'5' and output_signal_level 'VDDL' is referred to
voltage value '1'.  The voltage value is '5' in input
pin and the voltage value is '1' in output pin, which
```

Feedback

```
is wrong.

To correct it, you can assiged both to the same voltage
like "VDDH", so that both will refer to same value "5"
in operating_conditions as follows.


library(libdb727) {
  ...
  /* operation conditions */
  operating_conditions(5v_1v) {
    ...
    power_rail (VDDH, 5);    /* high power */
    power_rail (VDDL, 1);    /* low power */
    ...
  }
  ...
  default_operating_conditions : 5v_1v;

  ...
cell(ISO) {
 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDH
 }
 pin(out) {
        ...
        output_signal_level : VDDH

 }
}
```

LBDB-728

(error) You can not specify the same pin '%s' twice\n \tin '%s'.

Description

This message indicates that you specified the same pin more than one in either *related_inputs* or *related_outputs*. Each pin can be only specifed once.

The following example shows an instance where this message occurs:

```
cell(lbdb728) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
```

Feedback

```
    direction : input;
    capacitance : 1;
  }

  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
     ...
    }
  }
  dynamic_current() {
    when : "A";
    related_inputs : "B B";
    related_outputs : "Z Z"
    typical_capacitances(0.3 0.4);
    switching_group() {
     ...
    }
  }
  ...
}
```

In this case, both related_outputs and related_inputs, have specified the same pin name twice. To fix the problems, change the name from 'Z Z' to 'Z' in the related_outputs, change the name from 'B B' to 'B' in the related_inputs.

The following is an example message:

```
Error: Line 272, You can not specify the same pin 'Z' twice
        in 'related_outputs'. (LBDB-728)
Error: Line 572, You can not specify the same pin 'B' twice
        in 'related_inputs'. (LBDB-728)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-729

(warning) You can't specify the same pin '%s' in different\n \trelated_output attributes which are under the same intrinsic_parasitic group.

Description

If there are more than one *intrinsic_resistance* group under a *intrinsic_parasitic* group, then no *related_output* can have the same pin. However, the rule does not apply to closed channel, where the value specified in *intrinsic_resistance* group is greater than 1M Ohm.

Feedback

The following example shows an instance where this message occurs:

```
library(my) {
  /* unit attributes */
  time_unit : "1ns";
  capacitive_load_unit (1.0,pf);
  ...
 cell(lbdb729) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }
  intrinsic_parasitic() {
    /* default state */
    intrinsic_resistance(<pg_name>) {
       related_output : "ZN";
       value : 9.0;
    }
    intrinsic_resistance(<pg_name>) {
       related_output : "ZN";
       value : 920.0;
    }
    intrinsic_resistance(<pg_name>) {
       related_output : "ZN";
       value : 1001.0;
    }
    intrinsic_capacitance(<pg_name>) {
       value : 8.2;
    }
  }
  ...
 }
}
```

Based on timing and capacitance unit, we know the resistance unit is kilo. In this case, all intrinsic_resistance groups under a intrinsic_parasitic have same related_output 'ZN'. To fix the problem, change the name 'ZN' to 'Z' in either the group which has value '9.0' or the group which has value '920.0' because both are opened channel. No need to change the

name in the group which has value '1001.0' because it is greater than 1M ohm, which is closed channel.

The following is an example message:

```
Warning Line 272, You can't specify the same pin 'ZN' in different
        related_output attributes which are under the same
 intrinsic_parasitic group. (LBDB-729)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-730

(error) The pin '%s' specified in the '%s' is neither\n \tan %s pin nor an inout pin.

Description

This message indicates that direction of the pin you specified in a *related_inputs*, *related_outputs*, *related_output*, *index_output* or *gate_leakage* is wrong.

The following example shows an instance where this message occurs:

```
cell(lbdb730) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  leakage_current() {
     when : "A & !B & Z";
     pg_current(V1) {
      ...
     }
```

Feedback

```
      ...
      gate_leakage(Z) {  /* must be input or inout pin */
        input_high_value : 2.1;
        input_low_value : -1.7;
      }
    }
    dynamic_current() {
      when : "A";
      related_inputs : "Z";
      related_outputs : "B"
      typical_capacitances(0.3);
      switching_group() {
        input_switching_condition(fall);
        output_switching_condition(rise);
        pg_current(<pg_name>) {
          vector(<lu_template_name>) {
            reference_time : 93.2;
            index_output : "A";
            index_1("5.1");
            index_2("0.3");
            index_3("8.2 9.4 9.8");
            values("1.78 12.4 110.1");
          }
        }
      ...
      }
    }
    intrinsic_parasitic() {
      /* default state */
      intrinsic_resistance(<pg_name>) {
         related_output : "B";
         value : 9.0;
      }
      intrinsic_capacitance(<pg_name>) {
         value : 8.2;
      }

    }
    ...
}
```

In this case, all related_output, related_outputs, related_inputs, index_output and gate_leakage have a wrong pin name. To fix the problems, change the name from 'Z' to either 'A' or 'B' in the related_inputs, change the name from 'B' to 'Z' in the related_outputs, change the name from 'A' to 'Z' in the index_output, change the name from 'B' to 'Z' in the related_output and change the name from 'Z' to either 'A' or 'B' in the gate_leakage.

The following is an example message:

```
Error: Line 272, The pin 'Z' specified in the 'related_inputs' is neither
        an input pin nor an inout pin. (LBDB-730)
```

Feedback

```
Error: Line 471, The pin 'B' specified in the 'related_outputs' is
 neither
        an output pin nor an inout pin. (LBDB-730)
Error: Line 526, The pin 'A' specified in the 'index_output' is neither
        an output pin nor an inout pin. (LBDB-730)
Error: Line 890, The pin 'B' specified in the 'related_output' is neither
        an output pin nor an inout pin. (LBDB-730)
Error: Line 749, The pin 'Z' specified in the 'gate_leakage' is neither
        an input pin nor an inout pin. (LBDB-730)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-731

(error) The pin '%s' specified in the '%s' can not\n \tbe found in '%s'.

Description

Whatever the pin you specified in *index_output* must be matched to one of pins that you specified in *related_outputs*.

This message indicates that the pin you specified in a *index_output* is wrong because it can not be found in *related_outputs* which is defined under the same dynamic_current group as where *index_output* is defined.

The following example shows an instance where this message occurs:

```
cell(lbdb731) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }
  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z"
    typical_capacitances(0.3);
```

Feedback

```
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise);
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "ZN";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
      }
     ...
    }
  }
  ...
}
```

In this case, index_output have a wrong pin 'ZN' because it does not match the pin 'Z', which is specified in related_outputs. To fix the problem, change the name from 'ZN' to 'Z' in index_output.

The following is an example message:

```
Error: Line 272, The pin 'ZN' specified in the 'index_output' can not
        be found in 'related_outputs'. (LBDB-731)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-732

(error) You cannot specify more than one output pin or one bit\n \tof a bus or bundle output pin in the '%s'.

Description

Only single output pin is allowed to be specified in a *index_output* and a *related_output*.

This message indicates that you specified multiple pins either in a *index_output* or in a *related_output*.

The following example shows an instance where this message occurs:

```
cell(lbdb732) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
```

Feedback

```
    pin(B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      ...
    }
    pin(ZN) {
      direction : output;
      ...
    }

    dynamic_current() {
      when : "A";
      related_inputs : "B";
      related_outputs : "Z ZN"
      typical_capacitances(0.3 0.4);
      switching_group() {
        input_switching_condition(fall);
        output_switching_condition(rise fall);
        pg_current(<pg_name>) {
          vector(<lu_template_name>) {
            reference_time : 93.2;
            index_output : "Z ZN";
            index_1("5.1");
            index_2("0.3");
            index_3("8.2 9.4 9.8");
            values("1.78 12.4 110.1");
          }
        }
       ...
      }
    }
    ...
    intrinsic_parasitic() {
      /* default state */
      intrinsic_resistance(<pg_name>) {
         related_output : "Z ZN";
         value : 9.0;
      }
      intrinsic_capacitance(<pg_name>) {
         value : 8.2;
      }

    }

}
```

In this case, index_output and related_output have specified "Z ZN" which is wrong. To fix the problem, remove either 'Z' or 'ZN' from "Z ZN".

Feedback

The following is an example message:

```
Error: Line 272, You cannot specify more than one output pin or one bit
        of a bus or bundle output pin in the 'index_output'. (LBDB-732)
Error: Line 262, You cannot specify more than one output pin or one bit
        of a bus or bundle output pin in the 'related_output'. (LBDB-732)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-733

(error) An unbuffered %s pin '%s' should specify at least 1 'ccsn_first_stage' group.

Description

This message indicates that the following rule is not satisfied: If is_unbuffered is set to true on an inout/output pin, there should be at least 1 ccsn_first_stage group in the pin group.

The following example shows an instance where this message occurs:

```
cell(LAQM1RA) {
    ...
    pin (Q) {
      is_unbuffered : true;
      direction : "output";
      function : "IQ";
      ...
    }
  }
```

In this case, is_unbuffered of output pin 'Q' is true but the pin 'Q' has no 'ccsn_first_stage' group specified. To fix the problem, add the 'ccsn_first_stage' group into the pin 'Q'.

The following is an example message:

```
Error: Line 1620, Cell 'LAQM1RA', pin 'Q', An unbuffered output pin 'Q'
 should specify at least 1 'ccsn_first_stage' group. (LBDB-733)
```

What Next

Check the library source file, and add ccsn_first_stage or change the value of is_unbuffered.

LBDB-734

(warning) an %s pin should specify at least 1 non-static '%s' groups.

Feedback

Description

This warning message occurs when an input or inout pin does not have non-static ccsn_first_stage (or input_ccb for referenced CCSN modeling) group in the pin group and there are no related timing arcs referring this pin as the related_pin.

A static CCS noise model captures the behaviors of a static CCB (channel connected block). A static CCB refers to a CCB that does not have any input terminal or the voltage level at the input terminal does not affect the output current of the CCB. For example, a static CCS noise model can be characterized for a CMOS NAND gate when both inputs are tied to ground. Such static CCS noise models can be used in noise analysis with case analysis, but they cannot be used for propagating crosstalk delay or noise waveforms through the cell under study. See the *Make CCS Noise User Guide* for detailed information.

The following example shows an instance where this message occurs: The following is an example of incorrect input that causes this warning message:

```
cell(sample) {
    ...
    pin (A) {
        direction : input;
    }

    pin(Y ) {
      direction : output;
      ...
      ccsn_last_stage() {
        ...
      }

    }
  }
```

In this example, the A pin does not have the ccsn_first_stage group specified, and there are no associated timing arcs specifying ccs_first_stage groups. To fix the problem, add the non-static ccsn_first_stage group into pin A.

What Next

Check the library source file and fix either the invalid CCS Noise data, or the direction of the pin.

LBDB-735

(error) '%s' can't be specified in '%s' if power cell type is macro.

Feedback

Description

Currently in Liberty syntax, we support two power cell types for CCS power model. One is 'stdcell' and another is 'macro'. For a 'macro' cell type, there is one restriction. You can not specify *related_outputs* in *dynamic_current* group and *output_switching_condition* in *switching_group* group if cell type in CCS power is 'macro'.

This message indicates that you either specified *related_outputs* or *output_switching_condition* when cell type is 'macro'.

The following example shows an instance where this message occurs:

```
cell(lbdb735) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
    ...
  power_cell_type : macro;
  dynamic_current() {
    ...
    related_outputs : "Z ZN";                /* remove this */
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall); /* remove this */
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
        ...
        }
        ...
      }
     ...
    }
  }
  ...
}
```

In the case above, related_outputs and output_switching_condition are sepcified when cell type is 'macro', which is wrong. To fix the problem, we shall remove both attributes.

The following is an example message:

```
Error: Line 272, 'related_outputs' can't be specified in
 'dynamic_current' if power cell type is macro. (LBDB-735)
Error: Line 292, 'output_switching_condition' can't be specified in
 'switching_group' if power cell type is macro. (LBDB-735)
```

Feedback

What Next

Check the library source file, and make the necessary correction. You can remove *output_switching_condition* or *related_outputs* attribute to avoid the error if you specify any of them.

LBDB-736

(error) Size of '%s' must be the same as size of related_outputs.

Description

Size of *output_switching_condition* specified in *switching_group* and size of *related_outputs* specified in *dynamic_current*, they must be identical, which is the same for *typical_capacitances*. Meaning that size of *typical_capacitances* specified in *dynamic_current* must be the same size as what *related_outputs* has.

This message indicates that either size is different between *related_outputs* and *typical_capacitances* or size is different between *related_outputs* and *output_switching_condition*.

The following example shows an instance where this message occurs:

```
cell(lbdb736) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z";
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
      pg_current(<pg_name>) {
```

```
          vector(<lu_template_name>) {
            ...
        }
       ...
     }
   }
   ...
   }
}
```

In this case, size of related_outputs is 1 ("Z"), but size of typical_capacitances is 2 (0.3 and 0.4) and size of output_switching_condition is 2 (rise and fall) as well. To fix the problem, you can increase size of related_outputs to 2. You can change "Z" to "Z ZN".

The following is an example message:

```
Error: Line 272, Size of 'typical_capacitances' must be the same as size
 of related_outputs. (LBDB-736)
Error: Line 282, Size of 'output_switching_condition' must be the same as
 size of related_outputs. (LBDB-736)
```

What Next

Check the library source file, and make the necessary correction. Size of *output_switching_condition*, *related_outputs* and *typical_capacitances* must be identical.

LBDB-737

(error) '%s' is required in '%s' if index_output is specified\n \tin one of pg_current groups.

Description

For expanded ccs power, if *index_output* is specified in one of *vector* groups, then all of the *vector* groups under the same *pg_current* group must define an *index_output*.

For compact ccs power, if *index_output* is specified in one of *compact_ccs_power* groups, then all of the *compact_ccs_power* groups under the same *pg_current* group must define an *index_output*.

In the case like this, *typical_capacitances* attribute is required in *dynamic_current* group.

This message indicates that there no *typical_capacitances* attribute can be found in *dynamic_current* when *index_output* is defined.

The following example shows an instance where this message occurs:

```
cell(lbdb737) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
```

Feedback

```
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z ZN"
    switching_group() {
      ...
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "Z";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
        ...
      }
     ...
    }
  }
  ...
}
```

In this case, index_output is specified, but no typical_capacitances attribute is specified. To fix the problem, add the line like this typical_capacitances(0.1); in the dynamic_current group.

The following is an example message:

```
Error: Line 272, 'typical_capacitances' is required in 'dynamic_current'
 if index_output is specified
       in one of pg_current groups. (LBDB-737)
```

What Next

Check the library source file, and make the necessary correction. Add *typical_capacitances* attribute to avoid the error.

Feedback

LBDB-738

(error) In '%s' group, size of '%s' must be larger than one\n \tif index_output is defined in one of pg_current groups.

Description

For expanded ccs power, if *index_output* is specified in one of *vector* groups, then all of the *vector* groups under the same *pg_current* group must define an *index_output* attribute.

For compact ccs power, if *index_output* is specified in one of *compact_ccs_power* groups, then all of the *compact_ccs_power* groups under the same *pg_current* group must define an *index_output* attribute.

In the case like this, the size of *related_outputs* must be larger than 1.

This message indicates that the size of *related_outputs* is less than 2, when *index_output* is defined.

The following example shows an instance where this message occurs:

```
cell(lbdb738) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
    related_outputs : "Z"
    ...
    switching_group() {
      ...
      pg_current(<pg_name>) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "Z";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
```

Feedback

```
          values("1.78 12.4 110.1");
        }
        ...
      }
    ...
```

In this case, size of related_outputs is 1 ("Z"), when index_output is defined, which is wrong. To fix problem, we shall increase size of related_outputs. We can change "Z" to "Z ZN".

The following is an example message:

```
Error: Line 272, In 'dynamic_current' group, size of 'related_outputs'
 must be larger than one
       if index_output is defined in one of pg_current groups. (LBDB-738)
```

What Next

Check the library source file, and make the necessary correction. Increase the size of *related_outputs* up to at least 2 to avoid the error.

LBDB-739

(error) '%s' attribute is required for this '%s' group.

Description

For expanded ccs power, all *vector* groups under the same *pg_current* group must specify the same template. If there is no any *index_output* attribute specified in these *vector* groups and template used for these *vector* groups contains only one total_output_net_capacitance, then *related_outputs* attribute is required in *dynamic_current*.

For expanded ccs power, all *compact_ccs_power* groups under the same *pg_current* group must specify the same template. If there is no any *index_output* attribute specified in these *compact_ccs_power* groups and template used for these *compact_ccs_power* groups contains only one total_output_net_capacitance, then *related_outputs* attribute is required in *dynamic_current*.

This message indicates that you must specify *related_outputs* attribute in *dynamic_current* because the above rule is applied.

The following example shows an instance where this message occurs:

```
pg_current_template(test_2) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : time;
    index_1("0.6 0.9");
    index_2("0.6 0.9");
```

Feedback

```
    index_3("0.3 4.7");
  }
  ...
  cell(lbdb739) {
    area : 2;
    pin(A) {
      direction : input;
      capacitance : 1;
    }
    pin(B) {
      direction : input;
      capacitance : 1;
    }
    pin(Z) {
      direction : output;
      ...
    }
    pin(ZN) {
      direction : output;
      ...
    }

    dynamic_current() {
      when : "A";
      related_inputs : "B";
      ...
      switching_group() {
        input_switching_condition(fall);
        output_switching_condition(rise fall);
        pg_current(<pg_name>) {
          vector(test_2) {
            reference_time : 93.2;
            index_1("5.1");
            index_2("0.3");
            index_3("8.2 9.4 9.8");
            values("1.78 12.4 110.1");
          }
          ...
        }
       ...
      }
    }
    ...
  }
```

In this case, there is no index_output specified in any vector under a pg_current group. Also, the template (test_2) that vector referred to contains only one total_output_net_capacitance (variable_2). In the case like this a related_outputs attribute is required to be defined in dynamic_current group. To fix the problem, we need to add a related_outputs attribute within a dynamic_current group.

Feedback

The following is an example message:

```
Error: Line 272, 'related_outputs' attribute is required for this
 'dynamic_current' group. (LBDB-739)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-740

(error) Size of '%s' in this '%s' group must be two.

Description

For expanded ccs power, all *vector* groups under the same *pg_current* group refer to the same *pg_current_template*.

For compact ccs power, a *compact_ccs_power* group refers to a *compact_lut_template*.

In the pg_current_template or compact_lut_template, if there are two total_output_net_capacitance, then size of *related_outputs* in *dynamic_current* must be two.

This message indicates that the size of *related_outputs* is not two.

The following example shows an instance where this message occurs:

```
pg_current_template(test_1) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : total_output_net_capacitance;
    variable_4 : time;
    index_1("0.6 0.9");
    index_2("0.6 0.9");
    index_3("0.3 4.7");
    index_4("4.5 6.7 7.2");
 }
 ...
 cell(lbdb740) {
   area : 2;
   pin(A) {
     direction : input;
     capacitance : 1;
   }
   pin(B) {
     direction : input;
     capacitance : 1;
   }
   pin(Z) {
     direction : output;
     ...
```

Feedback

```
}
pin(ZN) {
  direction : output;
  ...
}

dynamic_current() {
  when : "A";
  related_inputs : "B";
  related_outputs : "Z"
  switching_group() {
    ...
    pg_current(<pg_name>) {
      vector(test_1) {
        reference_time : 93.2;
        index_1("5.1");
        index_2("0.3");
        index_3("0.3");
        index_4("8.2 9.4 9.8");
        values("1.78 12.4 110.1");
      }
      ...
    }
   ...
```

In this case, template 'test_1' contains two total_output_net_capacitance values, but size of related_outputs is 1 ("Z"), which is wrong. To fix the problem, you might want to increase size of related_outputs to two. You can change "Z" to "Z ZN".

The following is an example message:

```
Error: Line 262, Size of 'related_outputs' in this 'dynamic_current'
 group must be two. (LBDB-740)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-741

(error) Two switching_group groups in line %d and %d are\n \toverlapping.

Description

If either min_input_switching_count or max_input_switching_count specified in switching groups, and the switching count number they covered are overlapping, then these *switching_group* groups are considered overlapped.

If there is no min_input_switching_count or max_input_switching_count, then two *switching_group* groups are considered overlapped if both *input_switching_condition* and *output_switching_condition* are overlapped.

Feedback

If one of followings are true, then *output_switching_condition* is considered to be overlapping condition : + *output_switching_condition* is undefined on both *switching_group* groups. + *output_switching_condition* is defined on both *switching_group* groups and values of them are indentical.

If one of followings are true, then *input_switching_condition* is considered to be overlapping condition : + *input_switching_condition* is undefined on both *switching_group* groups. + *input_switching_condition* is defined on both *switching_group* groups and values of them are indentical. + values of them are difference, but one *input_switching_condition* is undefined, and another has value either "rise" or "fall".

This message indicates that two *switching_group* groups are overlapped because *input_switching_condition* and *output_switching_condition* both are in overlapping condition.

The following example shows an instance where this message occurs:

```
cell(lbdb741) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }
  power_cell_type : stdcell;
  dynamic_current() {
    when : "A";
    related_inputs : "B";
    related_outputs : "Z ZN"
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
     ...
    }
    switching_group() {
      output_switching_condition(rise fall);
     ...
    }
```

Feedback

```
  }
  ...
```

In this case, both switching_group have same output_switching_condition, and one input_switching_condition has value "fall" and another is undefined. input_switching_condition is overlapping and which is same as output_switching_condition, so two switching_group groups are overlapped. To fix the problem, you might want to change the value to "fall fall" in one of output_switching_condition groups.

```
type(bus6) {
  base_type : array ;
  data_type : bit ;
  bit_width : 6 ;
  bit_from : 5 ;
  bit_to : 0 ;
  downto : true ;
}

cell(lbdb741) {
  bus(sel) {
    bus_type : bus6 ;
    direction : input ;
    capacitance : 2 ;
    related_power_pin : V1;
    related_ground_pin : G1;
  }

  bundle(C) {
    members(Cx, Cy, Cz);
    direction : input;
    capacitance : 2 ;
    related_power_pin : V1;
    related_ground_pin : G1;

  }
  area : 2;
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
     pg_type : backup_ground;
```

Feedback

```
  }
  power_cell_type : macro;
  dynamic_current() {
    related_inputs : "C sel";
    switching_group() {
      min_input_switching_count : 1;
      max_input_switching_count : 6;
      ...
    }
    switching_group() {
      min_input_switching_count : 5;
      max_input_switching_count : 9;
      ...
    }
    ...
  }
}

In this case, the min_input_switching_count and max_input_switching_count
 are
specified in "macro" cell type.  If that is the case, we need to check if
 the number
they covered are overlapping.  We don't worry about
 input_switching_condition or
output_switching_condition here because these attributes can't be
 sepcified
if either min_input_switching_count or max_input_switching_count is
 sepcified.

'C' is 6 bits bus and 'sel' is 3 bits bundle.  The total bits are 9.
For the first switching_group, the switching count is from 1 to 6, and
 for the
second switching_group, the switching count is from 5 to 9.  The number 5
 and 6
are covered in both groups, which means the two groups are overlapping.
 To fix the
problem, please change number 5 to 7 in the second switching_group or
 change number
6 to 4 in the first switching_group.
```

SH EXAMPLE MESSAGE

```
Error: Line 100, Two switching_group groups in line 170 and 189 are
       overlapping. (LBDB-741)
```

What Next

Check the library source file, and make the necessary correction.

Feedback

LBDB-742

(error) Only one total_output_net_capacitance is allowed for the\n \ttemplate specified in this %s.

Description

For expanded ccs power, if *index_output* is specified in one of *vector* groups, then all of the *vector* groups under the same *pg_current* group must define an *index_output* attribute.

For compact ccs power, if *index_output* is specified in one of *compact_ccs_power* groups, then all of the *compact_ccs_power* groups under the same *pg_current* group must define an *index_output* attribute.

In the case like this, the template , which these *vector*/*compact_ccs_power* groups referred to, must contains only one total_output_net_capacitance.

This message indicates that the template contains either more than one or less than one total_output_net_capacitance.

The following example shows an instance where this message occurs:

```
pg_current_template(test_1) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : total_output_net_capacitance;
    variable_4 : time;
    index_1("0.6 0.9");
    index_2("0.6 0.9");
    index_3("0.3 4.7");
    index_4("4.5 6.7 7.2");
 }

 pg_current_template(test_2) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : time;
    index_1("0.6 0.9");
    index_2("0.6 0.9");
    index_3("0.3 4.7");
 }
 ...
 cell(lbdb742) {
   area : 2;
   pin(A) {
     direction : input;
     capacitance : 1;
   }
   pin(B) {
     direction : input;
     capacitance : 1;
   }
```

Feedback

```
pin(Z) {
  direction : output;
  ...
}
pin(ZN) {
  direction : output;
  ...
}

dynamic_current() {
  when : "A";
  related_inputs : "B";
  related_outputs : "Z ZN";
  typical_capacitances(0.3 0.4);
  switching_group() {
    input_switching_condition(fall);
    output_switching_condition(rise fall);
    pg_current(<pg_name>) {
      vector(test_1) {
        reference_time : 93.2;
        index_output : "Z";
        index_1("5.1");
        index_2("0.3");
        index_3("0.3");
        index_4("8.2 9.4 9.8");
        values("1.78 12.4 110.1");
      }
    }
   ...
```

In this case, index_output is specified in vector, and the vector is referred to template 'test_1', which contains two total_output_net_capacitance values. That is wrong. To fix the problem, we can change referred template to 'test_2'.

The following is an example message:

```
Error: Line 272, Only one total_output_net_capacitance is allowed for the
       template specified in this vector. (LBDB-742)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-743

(error) All %s under a pg_current group must specify\n \tsame template.

Description

All *vector* or *compact_ccs_power* groups under the same *pg_current* group must specify the same template.

Feedback

This message indicates that you specified different templates in /fBvector or *compact_ccs_power* groups, which are all under same *pg_current*.

The following example shows an instance where this message occurs:

```
pg_current_template(test_1) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : total_output_net_capacitance;
    variable_4 : time;
    index_1("0.6 0.9");
    index_2("0.6 0.9");
    index_3("0.3 4.7");
    index_4("4.5 6.7 7.2");
 }

 pg_current_template(test_2) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : time;
    index_1("0.6 0.9");
    index_2("0.6 0.9");
    index_3("0.3 4.7");
 }
 ...
 cell(lbdb743) {
   area : 2;
   ...
   dynamic_current() {
      ...
     switching_group() {
       ...
       pg_current(<pg_name>) {
         vector(test_2) {
           reference_time : 93.2;
           index_1("5.1");
           index_2("0.3");
           index_3("8.2 9.4 9.8");
           values("1.78 12.4 110.1");
         }
         vector(test_1) {
           reference_time : 93.2;
           index_1("5.1");
           index_2("0.3");
           index_3("0.3");
           index_4("8.2 9.4 9.8");
           values("1.78 12.4 110.1");
         }
         ...
       }
      ...
```

In this case, two vectors refer to different templates, one is 'test_1', and another is 'test_2'. This is wrong. To fix the problem, change 'test_1' to 'test_2' in second vector.

The following is an example message:

```
Error: Line 272, All vectors under a pg_current group must specify
       same template. (LBDB-743)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-744

(error) index_output is required for all %s in this\n \tpg_current group.

Description

For expanded ccs power, if *index_output* is specified in one of *vector* groups, then all of the *vector* groups under the same *pg_current* group must define an *index_output* attribute.

For compact ccs power, if *index_output* is specified in one of *compact_ccs_power* groups, then all of the *compact_ccs_power* groups under the same *pg_current* group must define an *index_output* attribute.

This message indicates that *index_output* attribute is not defined in all *vector*/*compact_ccs_power* groups under a *pg_current*.

Also to see, LBDB-737, LBDB-738, and LBDB-742.

The following example shows an instance where this message occurs:

```
cell(lbdb744) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }

  dynamic_current() {
```

```
    when : "A";
    related_inputs : "B";
    related_outputs : "Z ZN"
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
      pg_current(VDD) {
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "ZN";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
         vector(<lu_template_name>) {
          reference_time : 93.2;
          index_output : "Z";
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
        vector(<lu_template_name>) {
          reference_time : 93.2;
          index_1("5.1");
          index_2("0.3");
          index_3("8.2 9.4 9.8");
          values("1.78 12.4 110.1");
        }
      }
     ...
    }
  }
  ...
```

In this case, index_output is not specified in third vector, which is wrong. All vectors under pg_current(VDD) must specify index_output, because index_output has beed defined in one of vectors. To fix the problem, add index_output attribute to the third vector.

The following is an example message:

```
Error: Line 272, index_output is required for all vectors in this
       pg_current group. (LBDB-744)
```

What Next

Check the library source file, and make the necessary correction.

Feedback

LBDB-745

(error) Under this dynamic_current, pin '%s' is specified in\n \t'%s' and '%s'.

Description

/fBwhen, *related_outputs*, and *related_inputs* can't specify the same pin if they are under the same *dynamic_current* group.

This message indicates that you specified the same pin for two of following attributes : /fBwhen, *related_outputs*, and *related_inputs*

The following example shows an instance where this message occurs:

```
cell(lbdb745) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    ...
  }
  pin(ZN) {
    direction : output;
    ...
  }
  pin(ZN1) {
    direction : output;
    ...
  }
  dynamic_current() {
    when : "B + ZN'";
    related_inputs : "B";
    related_outputs : "Z ZN"
    typical_capacitances(0.3 0.4);
    switching_group() {
  ...
}
```

In this case, pin B is specified in both when and related_inputs, which is wrong. Same for pin ZN, which is specified in both when and related_outputs. To fix the problem, change "B" to "A" in related_inputs, and change "Z ZN" to "Z ZN1" in related_outputs.

Feedback

The following are example messages:

```
Error: Line 272, Under this dynamic_current, pin 'B' is specified in
 'related_inputs' and 'when'. (LBDB-745)

Error: Line 272, Under this dynamic_current, pin 'ZN' is specified in
 'related_outputs' and 'when'. (LBDB-745)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-746

(error) The %s of cell '%s'\n \tshould be specified before the %s '%s' is defined.

Description

You receive this message because the switch_cell_type is not defined before specifying the attributes related to switch cells.

The following example shows an instance where this message occurs: The following example shows the *switch_cell_type* is missing.

```
cell(sample) {
 pin(Y)  {
        switch_function : "sp";
        ...
 }
  ......
}
```

Correct it by add *fBswitch_cell_type attribute in the cell group.*

The following is an example message: Error: Line 191, The switch_cell_type attribute of cell 'sample' should be specified before the switch_function 'sp' is defined. (LBDB-746)

What Next

Make sure that *switch_cell_type* attribute exists before defining other attributes related switch cells.

LBDB-747

(warning) %s on input pin and %s on output pin\n \thave same power rail value but different rail name.

Description

This message will only be applied for an isolation cell.

Feedback

In Liberty, we support two kinds (old and new) of pg syntax. If *input_signal_level* and *related_power_pin* both presented in new syntax, then *input_signal_level* will be chosen, and *related_power_pin* will be discarded.

If you are in new pg syntax, the message indicates that voltage name of either *input_signal_level* or *related_power_pin* in input pin is different from voltage name of *related_power_pin* in ouput pin, but both are referring to the same voltage value.

If you are in old pg syntax, the message indicates that rail name of *input_signal_level* in input pin is different from rail name of utput_signal_level *in ouput pin, but both rail names are referring to the same voltage value.*

The following example shows an instance where this message occurs:

```
/* This is an example of old pg syntax. */
library(libdb747) {
 ...
   power_supply() {
        default_power_rail : VDD;
        power_rail (VDDH, 3); /* high power */
        power_rail (VDDL, 3); /* low power */
        power_rail (VSS, 0.0);   /* primary ground */
  }
  ...
  /* operation conditions */
  nom_process   : 1;
  nom_temperature       : 25;
  nom_voltage   : 1.0;
  operating_conditions(3v_3v) {
    process     : 1;
    temperature : 25;
    voltage     : 1.0;
    tree_type   : balanced_tree
    power_rail (VDDH, 3);    /* high power */
    power_rail (VDDL, 3);    /* low power */
    power_rail (VSS, 0.0);   /* primary ground */
  }
  default_operating_conditions : 3v_3v;

 ...
cell (LVLHLEHX2M) {
  ...
  rail_connection (VDD, VDDL);
  area : 2.600000;
  is_isolation_cell : true;
  pin(A) {
    direction : input;
    input_signal_level : VDDH;
    capacitance : 0.1859;
    internal_power() {
    ...
  }
```

Feedback

```
 pin(Y) {
   direction : output;
   output_signal_level : VDDL;
   capacitance : 0.0;
   function : "(A & EN)";
   internal_power() {
     power_level : VDDL;
  ...
```

In this case, input_signal_level in input pin "A" is specified "VDDH" as power rail, which is different from "VDDL" specified in output_signal_level in output pin "Y". However, both "VDDH" and "VDDL" are referring to same voltage value "3" as defined in operating_conditions group.

The following is the example message:

```
Warning: Line 100, input_signal_level on input pin and
 output_signal_level on output pin
        have same power rail value but different rail name. (LBDB-747)
```

The following example shows another instance where this message occurs:

```
/* This is an example of new pg syntax */
library (libdb747) {
 ...
 voltage_map( VDD, 0.7);
 voltage_map(VDDH, 0.8); /* high power */
 voltage_map(VDDL, 0.8); /* low power */
 voltage_map(VSS, 0.0);   /* primary ground */
 ...
 cell(ISO) {
 ...
 pg_pin(VDD1) {
 voltage_name : VDDH;
 pg_type : primary_power;
 }
 pg_pin(VDD2) {
 voltage_name : VDDL;
 pg_type : primary_power;
 }

 is_isolation_cell : true;
 ...
 pin(in) {
        ...
        input_signal_level : VDDH;
        related_power_pin : VDD1;  /* discard */
        related_ground_pin : GND;
 }
 pin(out) {
        ...
        related_power_pin: VDD2;
        related_ground_pin : GND;
```

Feedback

```
 }
}

In this case, input_signal_level 'VDDH' is referred to voltage value 0.8
 and
related_power_pin 'VDD2' is referred to voltage value 0.8, too.  The
 voltage
value 0.8 in input pin is same as valtage value in output pin, but their
voltage names are different, one is VDDH, and the other is VDDL.

The following is the example message:
Warning: Line 100, input_signal_level on input pin and related_power_pin
 on output pin
        have same power rail value but different rail name. (LBDB-747)
```

What Next

Check the library source file, and make the necessary correctiorn if it is needed.

LBDB-748

(error) There are less than 4 vectors specified in group '%s'.

Description

This error message occurs because Library Compiler requires at least 4 vectors inside each output_current_rise or output_current_fall group.

The following example shows an output_current_rise group without a dense vector and resulting error message.

```
output_current_template(CCT) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
  variable_3 : time;
 }
 . . .
 output_current_rise() {
   vector(CCT) {
      reference_time : 0.11;
      index_1 ("0.1");
      index_2 ("1");
      index_3 ("1, 2, 3");
      values ("1, 2, 3");
   }
   /* need at least additional 3 vectors to compile */
 }

Error: Line 198, There are less than 4 vectors specified in group
 'output_current_rise'.  (LBDB-748)
```

Feedback

What Next

Check the library source file and add additional vectors.

LBDB-749

(error) The size of %s should be at least %d.

Description

The specification of the size of the index is less than the minim index size.

The following example shows an instance where this message occurs:

```
lu_table_template(basic_template) {
        variable_1 : input_net_transition;
        index_1 ("1");
  }

          receiver_capacitance1_rise(basic_template) {
                index_1 ("500");
                values ("1.3401");
          }
```

The following is an example message:

```
Error: Line 160, The size of index_1 should be at least 2. (LBDB-749)
```

What Next

Check the library source file, and correct the problem by inceasing the size of the specified index.

LBDB-750

(warning) Overwrite '%s' by default '%s' value %f defined\n \tin 'operating_conditions'.

Description

There are two pg pin syntaxes in liberty: one is old syntax such as power_rail or rail_connection, another is new syntax such as voltage_map or pg_pin.

If new pg_pin syntax has been defined in .lib file , all PVT (process, voltage and temperature) defined in default_operating_conditions will be copied over to nom PVT.

For .lib/.db file without pg pin syntaxes, all PVT (process, voltage and temperature) defined in default_operating_conditions will be copied over to nom PVT.

The warning message indicates that whatever default nom PVT values you defined have been overwritten by values of default_operating_conditions.

Feedback

The following example shows an instance where this message occurs:

```
library(libdb750) {
 ...
  nom_process : 1.3
  nom_temperature : 20.0;
  nom_voltage : 4.0;

  operating_conditions ( TYPICAL ) {
    process : 1.0 ;
    temperature : 22.0 ;
    voltage : 3.0 ;
    tree_type : balanced_tree ;
  }
  default_operating_conditions :  TYPICAL;
   ...
  voltage_map(VDD1, 4.0); /* new pg pin syntax */
  voltage_map(VDD2, 4.5);
   ...
  cell (and2) {
   ...
  pg_pin(V1) { /* new pg pin syntax */
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  ...
```

In this case, nom_process will be overwritten by "process" value 1.0, which is defined in default operating_conditions group. nom_temperature will be overwritten by "temperature" value 22.0, which is defined in default operating_conditions group. nom_voltage will be overwritten by "voltage" value 3.0, which is defined in default operating_conditions group.

The following is an example message:

```
Warning: Line 100, Overwrite 'nom_process' by default 'process' value 1.0
 defined
        in 'operating_conditions'. (LBDB-750)
Warning: Line 100, Overwrite 'nom_temperature' by default 'temperature'
 value 22.0 defined
        in 'operating_conditions'. (LBDB-750)
Warning: Line 100, Overwrite 'nom_voltage' by default 'voltage' value 3.0
 defined
        in 'operating_conditions'. (LBDB-750)
```

LBDB-751

(error) The %s group with name '%s', has not been defined in the %s.

Feedback

Description

This message indicates that the referred group name is undefined in the library.

The following is an example message:

```
Error: Line 57, The base_curves group with name 'AND2",
       has not been defined in the library.(LBDB-751)
```

What Next

Add the referred group in the library. Or remove the reference

---

LBDB-752

(error) The '%s' attribute is missing in compressed_lut_template '%s'.

Description

This message indicates that the attribute is not defined in the compressed_lut_template group.

The following is an example message:

```
Error: Line 58, The 'base_curves_group' attribute is missing in
 compressed_lut_template 'LTT3'.(LBDB-752)
```

What Next

Add the attribute in compressed_lut_template.

LBDB-753

(error) The '%s' base curve parameter is missing in compressed_lut_template '%s' index_3.

Description

For ccs timing base curves, these six elementary curve parameters are must needed: init_current, peak_current, peak_voltage, peak_time, left_id, right_id. Additional parameters are also allowed, the index_3 value list can contains more than six parameters.

The following example shows an instance where this message occurs:

```
compressed_lut_template(LTT3) {
        variable_1 : input_net_transition;
        variable_2 : total_output_net_capacitance;
        variable_3 : curve_parameters;
        index_1 ("0.1, 0.2");
        index_2 ("1.0, 1.2");
```

Feedback

```
        index_3 ("init_current, peak_current, peak_voltage, left_id,
 right_id");
    }
```

The following is an example message:

```
Error: Line 60, The 'peak_time' base curve parameter is missing in
 compressed_lut_template 'LTT3' index_3.(LBDB-753)
```

What Next

Add the missing elementary curve parameter in compressed_lut_template index_3.

LBDB-754

(error) Redudant curve_x defined in base_curves '%s'.

Description

In a base_curves group, only one curve_x definition is allowed, otherwise it brings confusing to users.

The following example shows an instance where this message occurs:

```
base_curves(AND2_BC) {
        base_curve_type : ccs_timing_half_curve;
        curve_x ("0.1, 0.5, 0.9");
        curve_x ("0.2, 0.5, 0.8");
        curve_y (1, "0.8, 0.5, 0.2");
        curve_y (2, "0.85, 0.5, 0.15");
        ...
    }
```

The following is an example message:

```
Error: Line 62, Redudant curve_x defined in base_curves
 'AND2_BC'.(LBDB-754)
```

What Next

Remove redudant curve_x definition in base curves group, left one curve_x is enough.

LBDB-755

(error) Illegal base curve data is specified in '%s'.

Feedback

Description

The syntax of base_curves group:

```
base_curves("name") {
    base_curve_type : ccs_half_curve;
    curve_x ("float..., float");
    curve_y (curve_id, "float..., float";
    ...
}
```

Following are rules for base curve data: For curve data specified in curve_x: 1. At least 3 points are specified; 2. The value should between 0 and 1; 3. The values should be monotonic increasing;

For curve_data specified in curve_y: 1. number of points should be same as that in curve_x; 2. curve_y should be defined after curve_x; 3. valid boundary is [-inf, 1] for both compact CCS timing and compact CCS power.

The following example shows an instance where this message occurs:

```
base_curves(AND2_BC) {
        base_curve_type : ccs_timing_half_curve;
        curve_x ("0.1, 0.5, 1.1");
        curve_y (1, "0.8, 0.5, 0.2, 0.1");
        curve_y (2, "0.85, 0.5, 0.15");
        ...
    }
```

The following is an example message:

```
Error: Line 63, Illegal base curve data is specified in
 'curve_x'.(LBDB-755)
Error: Line 64, Illegal base curve data is specified in
 'curve_y'.(LBDB-755)
```

What Next

Check base curve data according these rules, fix error.

LBDB-756

(error) No curve_x definition found before curve_y in the base_curves '%s'.

Description

In a base_curves group, Only and Must have one curve_x defined before curve_y.

The following example shows an instance where this message occurs:

```
base_curves(AND2_BC) {
        base_curve_type : ccs_timing_half_curve;
```

Feedback

```
        curve_y (1, "0.8, 0.5, 0.2");
        curve_y (2, "0.85, 0.5, 0.15");
        ...
    }
```

The following is an example message:

```
Error: Line 65, No curve_x definition found before curve_y in the
 base_curves 'AND2_BC'.(LBDB-756)
```

What Next

Add the curve_x definition before the curve_y, otherwise, the base curve data is incomplete.

LBDB-757

(error) No curve_y definition found in the base_curves '%s'.

Description

In a base_curves group, base curves are demonstrated by curve_x and curve_y together. curve_y can't be absent.

The following example shows an instance where this message occurs:

```
base_curves(AND2_BC) {
        base_curve_type : ccs_timing_half_curve;
        curve_x ("0.1, 0.5, 0.9");
    }
```

The following is an example message:

```
Error: Line 63, No curve_y definition found in the base_curves
 'AND2_BC'.(LBDB-757)
```

What Next

Add the curve_y definition after the curve_x, in the base curves group.

LBDB-758

(error) Duplicate or negative curve_id '%d' is specified.

Description

In a base_curves group, the curve_id in curve_y should satisfy following rules: 1. curve_id should be an interger that greater than 0; 2. curve_id should be unique in the base_curves group;

Feedback

The following example shows an instance where this message occurs:

```
base_curves(AND2_BC) {
        base_curve_type : ccs_timing_half_curve;
        curve_x ("0.1, 0.5, 1.1");
        curve_y (-1, "0.8, 0.5, 0.2, 0.1");
        curve_y (2, "0.85, 0.5, 0.15");
        curve_y (4, "0.8, 0.5, 0.2, 0.1");
        curve_y (4, "0.85, 0.5, 0.15");
        ...
    }
```

The following is an example message:

```
Error: Line 63, Duplicate or negative curve_id '-1' is
 specified.(LBDB-758)
Error: Line 60, Duplicate or negative curve_id '4' is
 specified.(LBDB-758)
```

What Next

Check rules above, correct the curve_id data in curve_y.

LBDB-759

(error) Bad init_current value '%g' is specified in '%s'.

Description

Init_current is one of six parameters to model compressed ccs timing base curve. In compressed_ccs_rise group, the init_current values should >= 0; And in compressed_ccs_fall group, the init_current values should <= 0;

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
```

Feedback

```
    index_3 ("init_current, peak_current, peak_voltage, peak_time,
 left_id, right_id");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
        timing() {
            compressed_ccs_rise("LTT3") {
              values("0, 0.5, 0.6, 0.8, 1, 3", \
                     "-0.15, 0.55, 0.65, 0.85, 2, 4", \
                     "0.2, 0.6, 0.7, 0.9, 3, 2", \
                     "0.25, 0.65, 0.75, 0.95, 4, 1");
            } /* end of compressed_ccs_rise */
        }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1163, Bad init_current value '-0.15' is specified in
 'compressed_ccs_rise'.(LBDB-759)
```

What Next

According the rule above, correct the init_current value.

LBDB-760

(error) Bad peak_current value '%g' is specified in '%s'.

Description

peak_current is one of six parameters to model compressed ccs timing base curve. In compressed_ccs_rise group, the peak_current values should > 0; And in compressed_ccs_fall group, the peak_current values should < 0;

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
```

Feedback

```
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time,
 left_id, right_id");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
        timing() {
            compressed_ccs_rise("LTT3") {
              values("0.1, 0, 0.6, 0.8, 1, 3", \
                     "0.15, -0.55, 0.65, 0.85, 2, 4", \
                     "0.2, 0.6, 0.7, 0.9, 3, 2", \
                     "0.25, 0.65, 0.75, 0.95, 4, 1");
            } /* end of compressed_ccs_rise */
        }
    }
  }
  ...
}
```

The following are example messages:

```
Error: Line 1163, Bad peak_current value '0' is specified in
 'compressed_ccs_rise'.(LBDB-760)
Error: Line 1163, Bad peak_current value '-0.55' is specified in
 'compressed_ccs_rise'.(LBDB-760)
```

What Next

According the rule above, correct the peak_current value.

LBDB-761

(error) Non-integer base curve id '%s' is specified in '%s'.

Description

Curve_id should be integers because it is defined with integer data type.

For compact ccs timing, curve_id is the data corresponding to left_id or right_id in compressed_ccs_rise/compressed_ccs_fall group.

For compact ccs power, curve_id is the data corresponding to bc_id* in compact_ccs_power group.

Feedback

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time,
 left_id, right_id");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
        timing() {
            compressed_ccs_rise("LTT3") {
              values("0.1, 0, 0.6, 0.8, 1, 3", \
                     "0.15, -0.55, 0.65, 0.85, 2, 4", \
                     "0.2, 0.6, 0.7, 0.9, 3, 2", \
                     "0.25, 0.65, 0.75, 0.95, 4, 1");
            } /* end of compressed_ccs_rise */
        }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1163, Non-integer curve_id(lef_id/right_id) '3.5' is
 specified in 'compressed_ccs_rise'.(LBDB-761)
Error: Line 1163, Non-integer curve_id(lef_id/right_id) '2.0' is
 specified in 'compressed_ccs_rise'.(LBDB-761)
```

What Next

According the rule above, correct the left_id/right_id value in compressed_ccs_rise/ compressed_ccs_fall group, or the bc_id* value in compact_ccs_power group.

Feedback

LBDB-762

(error) Undefined base curve id '%d' is referenced in '%s'.

Description

Curve_id must be predefined in previous base_curve group.

For compact ccs timing, curve_id is the data corresponding to left_id or right_id in compressed_ccs_rise/compressed_ccs_fall group.

For compact ccs power, curve_id is the data corresponding to bc_id* in compact_ccs_power group.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time,
 left_id, right_id");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
        timing() {
            compressed_ccs_rise("LTT3") {
              values("0.1, 0, 0.6, 0.8, 1, 31", \
                     "0.15, -0.55, 0.65, 0.85, 7, 4", \
                     "0.2, 0.6, 0.7, 0.9, 3, 2", \
                     "0.25, 0.65, 0.75, 0.95, 4, 1");
            } /* end of compressed_ccs_rise */
        }
    }
  }
  ...
}
```

Feedback

The following is an example message:

```
Error: Line 1163, Undefined curve_id(lef_id/right_id) '31' is referenced
 in 'compressed_ccs_rise'.(LBDB-762)
Error: Line 1163, Undefined curve_id(lef_id/right_id) '7' is referenced
 in 'compressed_ccs_rise'.(LBDB-762)
```

What Next

According the rule above, correct the left_id/right_id value in compressed_ccs_rise/ compressed_ccs_fall group, or the bc_id* value in compact_ccs_power group.

LBDB-763

(error) Incompatible %s data specified in %s.

Description

For ccs timing and power data, there are two models that can be used. One is expanded model, the other is compact model.

Expanded ccs timing model is specified by output_current_{rise|fall}. Compact ccs timing model is specified by compact_ccs_{rise|fall}. Expanded ccs power model is specified by vector under pg_current group. Compact ccs power model is specified by compact_ccs_power under pg_current group.

Currently, only one model is supported in one library. If both of them are used in the library, the error is issued.

Users can't specify expanded ccs timing/power model for some cells in the library, while compact ccs timing/power model for other cells.

The following example shows an instance where this message occurs:

```
library(name) {
  ...

  cell(cell_name1) {
    pin(pin_name) {
        timing() {
            output_current_rise() {
              vector("CT3") {
                ...
              }
              ...
            }
            output_current_fall() {
              vector("CT3") {
                ...
              }
              ...
```

Feedback

```
            }
        }
    }
  }
  cell(cell_name2) {
    pin(pin_name) {
        timing() {
            compact_ccs_rise("LTT3") {
              values("..."..., "...");
            }
            compact_ccs_fall("LTT3") {
              values("..."..., "...");
            }
        }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1, Un-Compatible CCS timing data specified in timing
 arc.(LBDB-763)
```

What Next

Keep only one ccs timing/power model in the library.

LBDB-764

(error) Redundant base_curves group '%s' with '%s' type defined in library.

Description

Since the compressed ccs data (for the time being, it only support compressed ccs timing) is consumed by PT, to ensure the performance of PT, guarantee the ccs accuracy and ease the implementation of PT support and implementation, we only support one base curve group with specific base curve type.

The following example shows an instance where this message occurs:

```
library(name) {
  ...

  base_curves(bct1) {
    base_curve_type : ccs_timing_half_curve;
    curve_x ("0.1, 0.5, 0.9");
    curve_y (1, "0.2, 0.5, 0.8");
    ...
  }
  base_curves(bct2) {
    base_curve_type : ccs_timing_half_curve;
```

Feedback

```
    curve_x ("0.1, 0.5, 0.9");
    curve_y (1, "0.33, 0.55, 0.88");
    ...
  }
  ...
}
```

The following is an example message:

```
Error: Line 165, Redundant base_curves group 'bct2' with
 'ccs_timing_half_curve' type defined in library.(LBDB-764)
```

What Next

Remove the base_curves group or combine same base curve type groups into one base_curves group if possible. Leave only one base_curves group with the base curve type.

LBDB-765

(error) Bad peak_voltage value '%g' is specified in '%s',\n \tLegal vale should be in range of [%g, %g].

Description

peak_voltage is one of six parameters to model compact ccs timing base curve. In [va_]compact_ccs_rise/fall group, the peak_voltage values should less than Vdd of this port.

Note that the ways to define VDD are different between pg pin library, power-rail library, non-pg pin library. details may need to refer to application notes for pg pin supporting.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  operating_conditions(typical) {
    process     : 1;
    temperature : 25;
    voltage     : 1.0;
    tree_type   : balanced_tree
  }
  default_operating_conditions : typical;

  base_curves (ctbct1){
    base_curve_type : ccs_timing_half_curve;
    curve_x("0.2, 0.5, 0.8");
    curve_y(1, "0.8, 0.5, 0.2");
    curve_y(2, "0.75, 0.5, 0.35");
    curve_y(3, "0.85, 0.5, 0.15");
    curve_y(4, "0.85, 0.5, 0.15");
```

Feedback

```
  }
  compressed_lut_template(LTT3) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 ("0.1, 0.2");
    index_2 ("1.0, 2.0");
    index_3 ("init_current, peak_current, peak_voltage, peak_time,
 left_id, right_id");
    base_curves_group: "ctbct1";
  }

  cell(cell_name) {
    pin(pin_name) {
        timing() {
            compact_ccs_rise("LTT3") {
              values("0.1, 0, 0.6, 0.8, 1, 3", \
                     "0.15, 1.55, 0.65, 0.85, 2, 4", \
                     "0.2, 0.6, 0.7, 0.9, 3, 2", \
                     "0.25, 0.65, 0.75, 0.95, 4, 1");
            } /* end of compressed_ccs_rise */
        }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1163, Bad peak_voltage value '1.55' is specified in
 'compact_ccs_rise',
        Legal value should be in range of [0, 1.0].(LBDB-765)
```

What Next

According the rule above, correct the peak_voltage value.

LBDB-766

(warning) The '%s' attribute of %s '%s' overwrites the value specified \tin the '%s' attrbiute.

Description

This message indicates that the latest value overwrites the previous value defined for the same attribute.

The following is an example message:

```
Error: Line 100, The 'retention_pin' attribute of pin 'A' overwrites the
 value specified
        in the 'map_to_logic' attrbiute. (LBDB-766)
```

Feedback

What Next

Make sure that it is what have been expected.

LBDB-767

(error) No mandatory attribute '%s' defined in sensitization group '%s'.

Description

sensitization group is to describe the complete state patterns (by vector attributes) for a specific list of pins (by pin_names attribute). vector and pin_names are mandatory attributes in the group.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, Y");
  }

  ...
}
```

The following is an example message:

```
Error: Line 11, No mandatory attribute 'vector' defined in sensitization
 group 'my_sensitization'.(LBDB-767)
```

What Next

According to message, add pin_names or vector to make the sensitization group complete.

LBDB-768

(error) Duplicate pin name '%s' specified in '%s'.

Description

This error is issued when duplicate pin name specified in sensitization group pin_names, or cell/timing group pin_name_map attribute. Pin names in the attribute are used to generate stimuli from sensitization group for timing arc.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  sensitization (my_sensitization){
```

Feedback

```
    pin_names("A, B, B, Y");
    vector (0, "0 0 0 0");
    vector (1, "0 0 0 1");
    ...
  }

  ...
}
```

The following is an example message:

```
Error: Line 12, Duplicate pin name 'B' specified in
 'pin_names'.(LBDB-768)
```

What Next

Correct the duplicate pin name definition, if the number of pin is changed because of the fix, other sensitization related attributes may also need to be updated.

LBDB-769

(error) %s id (%d) specified sensitization vector.

Description

This error is issued when duplicate or negative vector id specified in vector attribute. The vector attribute is composed by: vector(vector_id, vector_string); The vector id should greater than or equal to zero, and unique in current sensitization group.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C, Y");
    vector (0, "0 0 0 0");
    vector (1, "0 0 0 1");
    vector (1, "0 0 1 1");
    vector (-1, "0 0 1 0");
    ...
  }

  ...
}
```

The following is an example message:

```
Error: Line 14, Duplicate id (1) specified in sensitization
 vector.(LBDB-769)
Error: Line 15, Negative id (-1) specified in sensitization
 vector.(LBDB-769)
```

Feedback

What Next

Correct the vector id in the vector attribute, according to the rule above.

LBDB-770

(error) No pin_names attribute defined before the vector.

Description

In sensitization group, pin_names attribute should be declared before all vectors. The error is issued when processing vector but find no pin_names attribute defined before in the sensitization group.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  sensitization (my_sensitization){
    vector (0, "0 0 0 0");
    pin_names("A, B, C, Y");
    vector (1, "0 0 0 1");
    vector (2, "0 0 1 0");
    vector (3, "0 0 1 1");
    ...
  }

  ...
}
```

The following is an example message:

```
Error: Line 13, No pin_names attribute defined before the
 vector.(LBDB-770)
```

What Next

Add pin_names attribute if it's missing, or reorder the pin_names attribute to the first declaration in the sensitization group.

LBDB-771

(error) Number of elements in the vector string (%d) is different from number of pin (%d).

Description

This error is issued when the number of elements in vector string is different the number of pins defined in pin_names attribute. The vector attribute is composed by: vector(vector_id, vector_string);

Feedback

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C, Y");
    vector (0, "0 0 0 0");
    vector (1, "0 0 0 1");
    vector (2, "0 0 1 0");
    vector (3, "0 1 1");
    ...
  }

  ...
}
```

The following is an example message:

```
Error: Line 17, Number of elements in the vector string (3) is different
 from number of pins (4).(LBDB-771)
```

What Next

Correct the vector string in the vector attribute, make it's elements number equal to number of pin in pin_names.

LBDB-772

(error) Number of pins (%d) in the %s pin_name_map \tis different from that (%d) in sensitization master '%s'.

Description

This error is issued when run into following situations: 1. Number of pin in cell->pin_name_map is different from that in cell->sensitization_master->pin_names. 2. Number of pin in timing->pin_name_map is different from that in timing->sensitization_master->pin_names. 3. When there is timing->pin_name_map defined, but there is only cell->sensitization_master attribute, Number of pin in timing->pin_name_map is different from that in cell->sensitization_master->pin_names.

When there is pin_name_map defined in cell or timing, pins in the attribute is used to generate stimuli for characterization, instead of pin_names in sensitization master. but the number of pins should be the same, otherwise vectors in the sensitization_master can not be mapped to these pins properly.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C, Y");
```

Feedback

```
    vector (0, "0 0 0 0");
    vector (1, "0 0 0 1");
    vector (2, "0 0 1 0");
    vector (3, "0 0 1 1");
    ...
  }

  cell (my_cell) {
    sensitization_master : my_sensitization;
    pin_name_map("A, B, Z");
    pin (A) {
        ...
    }
    ...
  }
  ...
}
```

The following is an example message:

```
Error: Line 1170, Number of pins (3) in the cell pin_name_map
        is different from that (4) in sensitization master
 'my_sensitization'.(LBDB-772)
```

What Next

Correct the vector string in the vector attribute, make it's elements number equal to number of pin in pin_names.

LBDB-773

(error) Illegal pin name '%s' specified in %s level sensitization attribute.

Description

This error is issued when pin name specified in cell/timing level sensitizaiotn attribute is an illegal(undefined) pin in the cell: This screener rule checks following pin names: 1. pin names specified in cell->pin_name_map attribute. 2. when there is no cell->pin_name_map, pin_names in cell->sensitization_master. 3. pin names in timing->pin_name_map attribute. 4. when there is no timing->pin_name_map, pin_names in timing->sensitization_master.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C");
    vector (0, "0 0 0");
    vector (1, "0 0 1");
    vector (2, "0 1 0");
```

Feedback

```
    vector (3, "0 1 1");
    ...
  }

  cell (my_cell) {
    sensitization_master : my_sensitization;
    pin_name_map("A, B, Z");
    pin (A) {
        ...
    }
    pin (B) {
        ...
    }
    pin (Y) {
        ...
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1170, Illegal pin name 'Z' specified in cell level
 sensitization attribute.(LBDB-773)
```

What Next

Check pin names in the sensitization attributes(pin_name_map, or pin_names in sensitization_master), make sure all pin names are real pin in the cell.

LBDB-774

(error) Incomplete sensitization info in the timing arc.

Description

This error is issued when there is wave_rise/wave_fall attribute defined in the timing group, but none of following attributes found: 1. pin_name_map attribute in current timing group. 2. sensitization_master attribute in current timing group. 3. pin_name_map attribute in current cell. 2. sensitization_master attribute in current cell.

Since there is no way to get the pin names for the wave_rise/wave_fall, the sensitization information for the timing is incomplete.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  sensitization (my_sensitization){
    pin_names("A, B, C");
    vector (0, "0 0 0");
```

```
    vector (1, "0 0 1");
    vector (2, "0 1 0");
    vector (3, "0 1 1");
    ...
  }

  cell (my_cell) {
    ...
    pin (A) {
        timing() {
            wave_rise (1, 3);
            wave_fall (2, 0);
            /* other timing arc data */
        }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1170, Incomplete sensitization info in the timing
 arc.(LBDB-774)
```

What Next

Define pin_name_map or sensitization_master attribute either in the timing arc or in the cell, make sure the sensitization information in this timing group is complete.

LBDB-775

(warning) No sensitization_master defined, sensitization vector is derived from vector id in the timing arc.

Description

This warning is issued when there is wave_rise/wave_fall attribute defined in the timing group, But no sensitization_master attribute defined either in the timing group or current cell.

This is a simplified usage model of sensitization, that sensitization vector used to get from sensitization group by vector id, but is derived from vector id and number of pin in pin_name_map by binary scale directly in such cases.

Example:

```
timing() {
    pin_name_map("A, B, C, Z");
    wave_rise (5, 8, 15);
}
```

Here '5' implies vector string of "0 1 0 1", '8' implies vector string of "1 0 0 0", and so on.

The following example shows an instance where this message occurs:

```
library(name) {
  ...

  cell (my_cell) {
    ...
    pin (A) {
        timing() {
            pin_name_map("A, B, Y");
            wave_rise (1, 3);
            wave_fall (2, 0);
            /* other timing arc data */
        }
    }
  }
  ...
}
```

The following is an example message:

```
Warning: Line 1170, No sensitization_master defined, sensitization vector
 is derived from vector id in the timing arc.(LBDB-775)
```

What Next

If this is what the users wanted, just ignore this warning. otherwise, specify valid sensitization_master attribute in the timing group or current cell.

LBDB-776

(error) Vector id (%d) in '%s' is undefined in sensitization group '%s'.

Description

When there is sensitization master defined for the timing arc, Vector id specified in wave_rise and wave_fall should be predefined in the sensitization group, otherwise, this error is issued.

The following example shows an instance where this message occurs:

```
library(name) {
  sensitization (my_sensitization){
    pin_names("A, B, C");
    vector (0, "1 0 0");
    vector (1, "0 0 1");
    vector (2, "1 1 0");
    vector (3, "0 1 1");
  }
  ...
```

Feedback

```
  cell (my_cell) {
    ...
    pin (A) {
        timing() {
            sensitization_master : my_sensitization;
            pin_name_map ("A, B, Y");
            wave_rise (1, 3);
            wave_fall (2, 4);
            /* other timing arc data */
        }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1181, Vector id (4) in 'wave_fall' is undefined in
 sensitization group 'my_sensitization'(LBDB-776)
```

What Next

Modify vector id in the wave_rise/wave_fall, make sure every vector id is predefined in sensitization master group.

LBDB-777

(error) Vector id (%d) for implied vector string in '%s' is out of range (0~%d).

Description

When there is no sensitization master defined either in the timing group or current cell, Vector string is implied by vector id and number of pin in pin_name_map. So the vector id should greater than or equal to zero, and less than 2^(number of pin in pin_name_map).

For example:

```
timing() {
    pin_name_map("A, B, C, Z");
    wave_rise (5, 8, 17);
}
```

Here number of pin in pin_name_map is 4, the vector id should < (2^4 = 16), so the vector id = 17 is out of range, and is not allowed.

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  cell (my_cell) {
    ...
```

Feedback

```
    pin (A) {
        timing() {
            sensitization_master : my_sensitization;
            pin_name_map ("A, B, Y");
            wave_rise (1, 7);
            wave_fall (2, 8);
            /* other timing arc data */
        }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1181, Vector id (8) for implied vector string in 'wave_fall'
 is out of range (0~7)(LBDB-777)
```

What Next

Modify vector id in the wave_rise/wave_fall, make sure every vector id is in the legal range.

LBDB-778

(error) index (%d) specified in '%s' is out of range (1~%d).

Description

The wave_rise_sampling_index/wave_fall_sampling_index is to define from which transition, (instead of default last transition) to the transition of the output pin, the delay is measured.

If the number of elements in wave_rise/wave_fall is N, then The index value should between (1 ~ N-1).

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  cell (my_cell) {
    ...
    pin (A) {
        timing() {
            sensitization_master : my_sensitization;
            pin_name_map ("A, B, Y");
            wave_rise (1, 4, 7);
            wave_fall (2, 5, 8);
            wave_rise_sampling_index : 3;
            /* other timing arc data */
        }
    }
```

Feedback

```
  }
  ...
}
```

The following is an example message:

```
Error: Line 1181, index (3) specified in 'wave_rise_sampling_index' is
 out of range (1~2)(LBDB-778)
```

What Next

Modify sampling index accordingly, make sure it's in the legal range.

LBDB-779

(error) Number of elements (%d) specified in '%s' is out of range (1~%d).

Description

The wave_rise_timing_interval/wave_fall_timing_interval attributes are for special cases that customers want to control the time interval between transitions. which is used to characterize some special-purpose cells and pessimistic timing characterization.

If the number of elements in wave_rise/wave_fall is N, then Number of elements in these two attributes should between (1 ~ N-1);

The following example shows an instance where this message occurs:

```
library(name) {
  ...
  cell (my_cell) {
    ...
    pin (A) {
        timing() {
            sensitization_master : my_sensitization;
            pin_name_map ("A, B, Y");
            wave_rise (1, 4, 7);
            wave_fall (2, 5, 8);
            wave_rise_timing_interval(0.0, 0.5, 1.0);
            /* other timing arc data */
        }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 1181, Number of elements (3) specified in
 'wave_rise_sampling_index' is out of range (1~2)(LBDB-779)
```

Feedback

What Next

Modify the wave_rise_timing_interval/wave_fall_timing_interval attribute values, accordingly to the rule above.

LBDB-780

(error) The '%s' %s is not %s '%s' %s.

Description

This error message occurs when you specify an invalid 'std_cell_main_rail' pg_pin in a level shifter not satisfying one of the following constraints: - the pg_pin must be a 'primary_power' or 'primary_ground' pg_pin. - if the pg_pin is 'primary_power', the pg_pin must be specified as the "related_power_pin" of one of the signal pins of the level shifter. - if the pg_pin is 'primary_ground', the pg_pin must be specified as the "related_ground_pin" of one of the signal pins of the level shifter.

As shown in the following example, the 'VDD' pg_pin is invalid because it is not a 'primary power' pg_pin.

```
cell(ls) {
    is_level_shifter : true;

    pg_pin(VDD) {
        voltage_name : VDDL;
        pg_type : backup_power;

        std_cell_main_rail : true;
    }
    ...
  }

Error: Line 84, The 'VDD' pg_pin is not a 'primary_power' pg_pin.
 (LBDB-780)
```

What Next

Modify the cell accordingly to satisfy the constraints.

LBDB-781

(error) The timing arc with feed_through_type '%s'\n \t%s specify the CCS Timing Current waveform vectors.

Description

The timing arc with feed_through_type attribute must satisfy the following requirements: 1. if the feed_through_type attribute is "short", then the timing arc must not have CCS Timing

Feedback

current waveform vectors. 2. if the feed_through_type attribute is "wire" or "gate", then the timing arc must have CCS Timing current waveform vectors.

The following example shows an instance where this message occurs:

```
pin(Z) {
          direction : output;
          timing() {
            /* no ccs information defined in the timing arc */
            feed_through_type : wire;
            ...
          }
        }
```

The following is an example message: Error: Line 144, The timing arc with feed_through_type 'short' cannot specify the CCS Timing Current waveform vectors. (LBDB-781)

What Next

Check the timing arc and make the correction accordingly.

LBDB-782

(error) The pin '%s' should be an 'inout' pin because of the associated \n \ttiming arc with feed_through_type attribute.

Description

The timing arc with feed_through_type attribute can only be specified between inout pins.

The following example shows an instance where this message occurs:

```
pin (A) {
          direction : output;
          ...
        }
        pin(Z) {
          direction : output;
          timing() {
            feed_through_type : short;
            ...
            related_pin : "A";
          }
        }
```

The following is an example message: Error: Line 144, The pin 'A' should be an 'inout' pin because of the associated timing arc with feed_through_type attribute. (LBDB-782) Error: Line 148, The pin 'Z' should be an 'inout' pin because of the associated timing arc with feed_through_type attribute. (LBDB-782)

Feedback

What Next

Check the timing arc and make the correction accordingly.

LBDB-783

(error) In cell '%s', the %s timing arc from pin '%s' to '%s' with feed_through_type '%s'\n \tdoes not have the required timing arc from pin '%s' to '%s' of the same timing_type\n \t, timing_sense and feed_though_type.

Description

The timing arc with feed_through_type attribute 'short' or 'wire' must have the relative backward timing arc with the same timing_type and feed_through_type for the same cell.

The following example shows an instance where this message occurs:

```
cell(T) {
        ...
        pin(Z) {
          direction : output;
          /* no timing arc Z->A with timing_type = combinational and
 feed_through_type= wire exists in the cell T */
          timing() {
            timing_type : combinational;
            feed_through_type : wire;
            ...
            related_pin "A";
          }
        }
        ...
     }
```

The following is an example message: Error: Line 144, In cell 'T', the combinational timing arc from pin 'A' to 'Z' with feed_through_type '%s' does not have the required timing arc from pin 'Z' to 'A' of the same timing_type, timing_sense and feed_though_type. (LBDB-783)

What Next

Check the timing arcs and make the correction accordingly.

LBDB-784

(error) The %s value of the '%s' attribute is %g,\n \twhich is %s the required value %g.

Description

The minimum/maximum value of the attribute is less/greater than the required value.

Feedback

The following example shows an instance where this message occurs:

```
...
  current_unit : "1mA" ;
  ...
  dc_current (ccsn_dc_29x29) {
        index_1 ("...");
        index_2 ("...");
        /* current unit = 1mA, and the max value = 0.005 */
        values ("0.0005, ...., 0.00091);
  }
```

The following is an example message:

```
Error: Line 35, The maximum value of the 'values' attribute is 0.0005,
        which is less than required value 0.001. (LBDB-784)
```

What Next

Check the library source file and correct the problem.

LBDB-785

(warning) The '%s' attribute is not defined in the library. \n \tUsing %f as the default value.

Description

You receive this message because the relative attribute is not defined in the library, so LC will create the attribute with the predefined default value.

The following is an example message: Warning: Line 85, The 'nom_voltage' attribute is not defined in the library. Using 5 as the default value. (LBDB-785)

What Next

Examine the library source file, and add the correct value for the attribute.

LBDB-786

(error) The attribute valus is not a switch pin.

Description

The value of related_switch_pin must be referring to either a switch pin or an internal pin as defined below.

switch pin : switch_pin attribute is set to "true" within a pin. internal pin : related_pin attribute is referred to a switch pin.

The following example shows an instance where this message occurs:

```
dc_current (ccsn_dc_29x29) {
    related_switch_pin : D;
    ...
 }
 pin(CTL) { /* this is a switch pin as switch_pin is set to "true" */
    capacitance : 0.5;
    direction : input;
    switch_pin : true;
    ...
 }
 pin(int_1) { /* this is an internal pin, which refers to a switch pin by
                 related_pin attribute */
    direction : internal;
    timing () {
      related_pin : CTL;
      ...
    }
    ...
 }
 pin(D) {
    capacitance : 0.5;
    direction : input;
    ...
  }
```

In this case, related_switch_pin is pointing to pin "D", which is not either an internal pin or a switch pin. The way to correct it is to specify related_switch_pin to either pin "CTL" or pin "int_1".

The following is an example message:

```
Error Line 272, The attribute valus is not a switch pin. (LBDB-786)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-787

(error) Cell(%s): The 'internal_node' in the '%s' port\n \tcan't be specified because no statetable is allowed in generic type\n \tof clock gating integrated cell.

Description

If attribute 'clock_gating_integrated_cell' is generic, then no statetable is allowed. 'internal_node' attribute must match one of the internal node names in statetable. Since there is no statetable is allowed, there is no 'internal_node' attribute can be specified in a port, either.

Feedback

The following example shows an instance where this message occurs:

```
cell(ldbd-787) {
    ...
  cell_leakage_power : 0.023529479 ;
  clock_gating_integrated_cell : "generic" ;
    ...

  pin(Q) {
    direction : internal;
    internal_node : "Q1";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
}
```

In this case, Q1 in internal_node attribute shall not be specified because there is no statetable in the cell.

The following is an example message:

```
Error: Line 139, Cell(lbdb-787): The 'internal_node' in the 'Q' port
        can't be specified because no statetable is allowed in generic
 type
        of clock gating integrated cell. (LBDB-787)
```

What Next

Remove the internal_node attribute to fix the problem.

LBDB-788

(warning) No default '%s" group defined in '%s'.

Description

This warning is issued when there is some default group is missing in library, but no default can be assumed to it.

For example, if there is no default driver waveform specified, This warning will be reported.

The following is an example message:

```
Warning Line 10, No default 'normalized_driver_waveform" group defined in
 'library'.(LBDB-788)
```

Feedback

What Next

Check the library source file, add default group.

LBDB-789

(warning) The '%s' attribute in the '%s' table has\n \tless than %d '%s" points,that is point between %g to %g.

Description

The values of the corresponding attribute has no enough type of points.

For example, the normalized voltage points for driver waveform need at lease 1 start points(0~0.05) and end points(0.95~1.0) for accuracy.

The following example shows an instance where this message occurs:

```
normalized_driver_waveform (dw01) {
    index_1 ("1.0");    /* input net transition */
    index_2 ("0.1, 0.3, 0.5, 0.7, 0.9"); /* normalized voltage*/
    ...
 }
```

In this case, the index_2 of normalized_driver-waveform is normalized_voltage, It would be better to supply at leat one start points and end points for accuracy purpose.

The following is an example message:

```
Warning Line 27, The 'index_2' attribute in the
 'normalized_driver_waveform' table
       has less than 1 'start" points, that is between '0' to '0.05'.
 (LBDB-789)
Warning Line 27, The 'index_2' attribute in the
 'normalized_driver_waveform' table
       has less than 1 'end" points, that is between '0.95' to '1.0'.
 (LBDB-789)
```

What Next

Check the library source file, add some example points for the attribute.

LBDB-790

(error) '%s' only allows single %s pin name.

Description

Only one single pg pin name can be specified in intrinsic_resistance, intrinsic_capacitance and pg_current or only one single pin name can be specified in gate_leakage.

Feedback

The following example shows an instance where this message occurs:

```
pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
     pg_type : backup_ground;
  }

 pin(A1) {
  direction : input;
  ...
   }
 pin(A2) {
  direction : input;
  ...
   }
 pin(A3) {
  direction : input;
  ...
   }
 pin(ZN1) {
  direction : output;
  ...
 }
 pin(ZN) {
  direction : output;
  ...
 }
 ...
  dynamic_current() {
    when : "A1";
    related_inputs : "A2 A3";
    related_outputs : "ZN ZN1";
    typical_capacitances(0.3 0.4);
    switching_group() {
      input_switching_condition(fall);
      output_switching_condition(rise fall);
      pg_current(V2 G1) {
        vector(test_2) {
          reference_time : 193.2;
          index_output : "ZN1";
          index_1("15.1");
```

Feedback

```
          ...
        }
      ...
    }
   ...
 }

leakage_current() {
   pg_current(V1) {
     value : 4.5;
   }
   pg_current(G1 G2) {
     value : -4.5;
   }
  ...
   gate_leakage(A2 A3) {
     input_high_value : 1.0;
     input_low_value : -10.0;
   }
   gate_leakage() {
     input_high_value : 3.0;
     input_low_value : -40.0;
   }


}
intrinsic_parasitic() {
  when : "A1 & A2 & ZN";
  intrinsic_resistance(G1 G1) {
     related_output : "ZN";
     value : 9.0;
  }
  intrinsic_resistance(G1) {
     related_output : "ZN1";
     value : 62.2;
  }
  intrinsic_capacitance(G2 G2) {
     value : 31.47;
  }
}
```

In this case, the pg_current within switching_group has two pg pins, V2 and G1, which is wrong. The pg_current within leakage_current has two pg pins, G1 and G2, which is wrong. The intrinsic_resistance has two pg names, G1 and G1, which is wrong. The intrinsic_capacitance has two pg names, G2 and G2, which is wrong. The first gate_leakage has two pin names A3 and A2, which is wrong, and the second gate_leakage has no name there, which is wrong, too. You might want to change all of them to one PG or pin name to avoid the error.

Feedback

The following is an example message:

```
Error Line 272, 'pg_current' only allows single pg pin name. (LBDB-790)
Error Line 222, 'gate_leakage' only allows single pin name. (LBDB-790)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-791

(error) pg_pin group is required for ccs power cell.

Description

If the cell is a ccs power cell, which contains dynamic_current, leakage_current or intrinsic_parasitic, then pg_pin group is required.

The following example shows an instance where this message occurs:

```
cell (AND3) {
  ...
  power_cell_type : stdcell;
  dynamic_current() {
    when : "A1";
    related_inputs : "A2 A3";
    related_outputs : "ZN ZN1";
    typical_capacitances(0.3 0.4);
    switching_group() {
    ...
    }
    ...
  } ...
}
```

In this case, cell, AND3, is a ccs power cell. The pg_pin must be specified within cell to fix the error as shown below :

```
cell (AND3) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
```

```
    voltage_name : GND2;
    pg_type : backup_ground;
  }

  power_cell_type : stdcell;
  dynamic_current() {  ...
```

The following is an example message:

```
Error Line 272, pg_pin group is required for ccs power cell. (LBDB-791)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-792

(error) leakage current in simplified format must be >= 0.

Description

If there is no pg_current within leakage_current group, we defined that as simplified format. Please refer to users guide for details.

If leakage_current is in simplifed format, then the value of leakage current must be zero or positive floating number.

The same rule is applied to va_leakage_current.

The following example shows an instance where this message occurs:

```
cell (OR2) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  leakage_current() {
     when : "A1 & !A2 & ZN";
     value : 3.1;
  }
  leakage_current() {
     when : "A1 & !A2 & !ZN";
     value : 0.0;
  }
  leakage_current() {
     /* default state */
     value : -8.1;
  }
```

Feedback

```
  ...
}
```

In this case, leakage current -8.1 is not allowed. The value must be >= 0 in simplified format.

The following is an example message:

```
Error Line 272, leakage current in simplified format must be >= 0.
 (LBDB-792)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-793

(error) Name specified in '%s' is not a valid %s pin.

Description

You got this message because an invalid PG or signal pin is used.

The pin name specified in intrinsic_capacitance, intrinsic_resistance, or pg_current group must be referred to a valid PG pin defined in cell, and a pg name is required for these groups.

The pin name specified in gate_leakage group must be referred to a valid signal pin defined in cell, and a pin name is required for gate_leakage.

The following example shows an instance where this message occurs:

```
cell (AND3) {
  ...
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
     pg_type : backup_ground;
  }
 ...
 dynamic_current() {
```

Feedback

```
  when : "A1";
  related_inputs : "A2 A3";
  related_outputs : "ZN ZN1";
  typical_capacitances(0.3 0.4);
  switching_group() {

    input_switching_condition(fall);
    output_switching_condition(rise fall);

    pg_current(V5) {     /* error */
      vector(test_2) {
      ...
    }
    pg_current() {       /* error */
    ...
  ...
}
 ...
 leakage_current() {
   when : "A1 & !A2 | ZN";
   pg_current(V5) {      /* error */
     value : 4.5;
   }
   pg_current(V2) {
     value : 4.5;
   }
   pg_current(G2) {
     value : -3.5;
   }
   pg_current() {       /* error */
     value : 4.5;
   }
}
...
intrinsic_parasitic() {
  when : "A1 & A2 & ZN";
  intrinsic_resistance() {    /* error */
     related_output : "ZN";
     value : 9.0;
  }
  intrinsic_resistance(V5) {   /* error */
     related_output : "ZN1";
     value : 62.2;
  }
  intrinsic_capacitance(G2) {
     value : 31.47;
  }
  intrinsic_capacitance() {    /* error */
     value : 31.47;
  }
  intrinsic_capacitance(V5) {  /* error */
     value : 31.47;
  }
```

```
    ...
  }
}
```

Please check the lines marked as 'error'. For these lines, they are either refers to an empty pg name, or refers to a invalid pg pin name, V5. Both are wrong. To fix the problems, please change V5 to a valid pg pin like V1, and also give a valid pg name for the empty ones.

The following is an example message:

```
Error Line 272, Name specified in 'pg_current' is not a valid PG pin.
 (LBDB-793)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-794

(warning) The value of pg_current should be '%s'.

Description

This is rule for leakage_current groups. If the PG pin is a power or internal ground pin, then the value of leakage current should be either zero or positive floating number. If the PG pin is a ground or internal power pin, then the value of leakage current should be either zero or negative floating number.

The following example shows an instance where this message occurs:

```
cell (AND3_1) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(V3) {
     voltage_name : VDD3;
     pg_type : internal_ground;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
     pg_type : backup_ground;
```

Feedback

```
   }
   pg_pin(G3) {
      voltage_name : GND3;
      pg_type : internal_power;
   }
   leakage_current() {
      when : "A1 & !A2 & ZN";
      pg_current(V1) {
        value : -4.5;
      }
      pg_current(V2) {
        value : -4.5;
      }
      pg_current(G2) {
        value : 4.5;
      }
      pg_current(V3) {
        value : -4.5;
      }
      pg_current(G1) {
        value : 4.5;
      }
      pg_current(G3) {
        value : 4.5;
      }
   }
   ...
}
```

In this case, V1, V2 and V3 should be positive or zero, and G1, G2 and G3 should be negative or zero based on the pg_type.

The following is an example message:

```
Warning Line 272, The value of pg_current should be '>=0'. (LBDB-794)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-795

(error) Only one PG pin can be omitted in %s group.

Description

All the PG pins except one shall be specified in leakage_current. This rule is also applied to va_leakage_current group.

Feedback

The following example shows an instance where this message occurs:

```
cell (AND3) {

  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(G2) {
     voltage_name : GND2;
     pg_type : backup_ground;
  }
  leakage_current() {
     when : "A1 & A2 & !ZN";
     pg_current(V1) {
       value : 4.5;
     }
     pg_current(V2) {
       value : 4.5;
     }
  }
  ...
}
```

There are 4 pg pins in the cell AND3, and based on rule only one pg pin can be omitted in leakage_current group. Meaning you have to specify at least three pg pins for this case. However, there are only two pg pins (V1 and V2) specified in leakage_current. To fix the problem, please specify at least one of ground pins for leakage_current as shown below.

```
leakage_current() {
     when : "!A1 & A2 & ZN";
     pg_current(V1) {
       value : 4.5;
     }
     pg_current(V2) {
       value : 4.5;
     }
     pg_current(G2) {
       value : -4.5;
     }
  }
```

Feedback

The following is an example message:

```
Error Line 272, Only one PG pin can be omitted in leakage_current group.
 (LBDB-795)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-796

(warning) The leakage current of all PG pins and gate\n \tleakage current of all input/inout pins must be summed up to zero.

Description

This rule applies to leakage_current and va_leakage_current groups if leakage current of all PG pins are specified.

If no gate_leakage are specified, the leakage current of all PG pins should add up to zero. If gate_leakage of all input/inout pins are specified, the leakage current of all PG pins and gate leakage current of all input/inout pins should add up to zero.

Total leakage current must add up to zero. A small error of +/- 1e-10 A (0.1 nA) is allowed. Larger errors must still be within a tolerance of 1.0e-6 * (total of absolute values of leakage current). The tolerance is calculated as follows:

```
| total of leakage current |
       ------------------------------  <= 1.0e-06
        total of | leakage current |
```

The following example shows an instance where this message occurs: In the example below, the total of leakage current is -0.000028. Based on the rule above, it will be like | -0.000028 | / 27.000028 = 1.03 * 1.0e-6 The result is greater than 1.0e-6. To fix the problem, we can change the G3 current to -4.500020.

```
cell (AND3_1) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
  }
  pg_pin(V3) {
     voltage_name : VDD3;
     pg_type : internal_ground;
  }
  pg_pin(G1) {
     voltage_name : GND1;
```

Feedback

```
      pg_type : primary_ground;
   }
   pg_pin(G2) {
      voltage_name : GND2;
      pg_type : backup_ground;
   }
   pg_pin(G3) {
      voltage_name : GND3;
      pg_type : internal_power;
   }
   leakage_current() {
      when : "A1 & A2 & ZN";
      pg_current(V1) {
        value : 4.5;
      }
      pg_current(V2) {
        value : 4.5;
      }
      pg_current(G2) {
        value : -4.5;
      }
      pg_current(V3) {
        value : 4.5;
      }
      pg_current(G1) {
        value : -4.5;
      }
      pg_current(G3) {
        value : -4.500028;
      }
 }
```

The following is an example message:

```
Warning: Line 246, The leakage current of all PG pins and gate leakage
         current of all input/inout pins must be summed up to zero.
 (LBDB-796)
```

What Next

Check the library source file and make the necessary correction.

LBDB-797

(warning) The leakage_current is in wrong format.

Description

Please also refer to LBDB-798.

The leakage_cuurent only allow either regular or simplified format. The regular format shall contain pg_current group, and the simplified format shall contain value attribute.

Feedback

The following example shows an instance where this message occurs:

```
leakage_current() {
     when : "A1 & !A2 & !ZN";
   }
```

In this case, leakage_current is neither in regular nor in simplified format. To avoid the warning, please change it to either of following formats:

```
simplified format :
   leakage_current() {
     when : "A1 & !A2 & !ZN";
     value : 0.0;
   }

  regular format :
   leakage_current() {
     when : "A1 & !A2 & !ZN";
     pg_current(V1) {
       value : 0.0;
     }
   }
```

The following is an example message:

```
Warning Line 272, The leakage_current is in wrong format. (LBDB-797)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-798

(error) The leakage current groups have mix format.

Description

Please also refer to LBDB-797.

The leakage_cuurent only allow either regular or simplified format. The regular format shall contain pg_current group, and the simplified format shall contain value attribute. And, two formats can not be mixed.

The following example shows an instance where this message occurs:

```
cell (test) {
  ...
  leakage_current() {
     pg_current(V1) {
       value : 4.5;
     }
     pg_current(G1) {
```

```
        value : -4.5;
      }
      pg_current(G2) {
        value : -14.5;
      }
      pg_current(V2) {
        value : 14.5;
      }
  }
  leakage_current() {
     when : "!A1 & !A2 & ZN";
     value : 0.0;
  }
  ...
}
```

In this case, first leakage_current is in regular format and second leakage_current is in simplified format, which is wrong. Two formats can not be mixed under the same cell.

The following is an example message:

```
Error Line 272, The leakage current groups have mix format. (LBDB-798)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-799

(error) The multiple PG pins can not be simplified format\n \tin %s.

Description

The simplified format in leakage_current means no pg_current group specified under this leakage_current. If a cell have more than one power or ground pin, then we can not use simplified format for leakage_current.

The rule is also applied to va_leakage_current.

The following example shows an instance where this message occurs:

```
cell (test) {
  pg_pin(V1) {
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(G1) {
     voltage_name : GND1;
     pg_type : primary_ground;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
```

Feedback

```
      pg_type : backup_ground;
  }
  leakage_current() {
      when : "A1 & !A2 | ZN";
      value : 3.1;
  }
 ...
}
```

In this case, the cell 'test' has more than one power pin, and leakage_current is in simplified format, which is wrong. To fix the problem, change the simplified format to regular format as shown below.

```
leakage_current() {
     when : "A1 & !A2 | ZN";
     pg_current(V1) {
       value : 1.1;
     }
     pg_current(G1) {
       value : -3.1;
     }
     pg_current(V2) {
       value : 2.0;
     }
  }
```

The following is an example message:

```
Error Line 272, The multiple PG pins can not be simplified format
        in leakage_current group. (LBDB-799)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-800

(error) In group '%s', the number of differnt\n \t'%s' values in the vectors is %d, which should \n \tbe at least %d.

Description

This error message occurs because Library Compiler requires the vectors should contain at least 2 different slew values and 2 different load values.

The following example shows an output_current_rise group with vectors containing only 1 slew value, which is 1.

```
output_current_template(CCT) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
```

Feedback

```
 variable_3 : time;
}
. . .
output_current_rise() {
  vector(CCT) {
     reference_time : 0.11;
     index_1 ("0.1");
     index_2 ("1");
     index_3 ("1, 2, 3");
     values ("1, 2, 3");
  }
   vector(CCT) {
     reference_time : 0.11;
     index_1 ("0.2");
     index_2 ("1");
     index_3 ("1, 2, 3");
     values ("1, 2, 3");
  }
}
```

```
Error: Line 198, In group 'output_current_rise', the number of differnt
        'total_output_net_capacitance' values in the vectors is 1, which
 should
       be at least %d. (LBDB-800)
```

What Next

Check the library source file and add a vector for each input_net_transition and total_output_net_capacitance pair.

LBDB-801

(error) %s and %s attributes must be specified in pair.

Description

The max_input_switching_count and min_input_switching_count attributes must be defined in pair within a switching_group. Meaning that if max_input_switching_count is defined, then min_input_switching_count must be defined under the same switching_group and vice versa.

The following example shows an instance where this message occurs:

```
power_cell_type : macro;
  dynamic_current() {
    ...
    switching_group() {
      min_input_switching_count : 1;
      ...
    }
  ...}
```

In this case, min_input_switching_count is defined, but there is no max_input_switching_count, which is wrong. To fix the problem, you can either remove min_input_switching_count from the switching_group or specify max_input_switching_count within switching_group.

The following is an example message:

```
Error Line 272, min_input_switching_count and max_input_switching_count
 attributes must be specified in pair. (LBDB-801)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-802

(error) %s can not be defined within a %s\n \tgroup where %s is defined.

Description

You can only specify either max_input_switching_count and min_input_switching_count or input_switching_condition within a switching_group group. Meaning max_input_switching_count/ min_input_switching_count and input_switching_condition shall not present under the same switching_group group.

ALSO SEE LBDB-801

The following example shows an instance where this message occurs:

```
switching_group() {
      min_input_switching_count : 1;
      max_input_switching_count : 9;
      input_switching_condition(rise);
      ...
   }
```

In this case, min_input_switching_count and max_input_switching_count are defined, and also input_switching_condition is defined under the same switching_group where min_input_switching_count and max_input_switching_count are defined. This is wrong. To fix the problem, please remove either input_switching_condition or min_input_switching_count and max_input_switching_count.

The following is an example message:

```
Error Line 272, input_switching_condition can not be defined within a
 switching_group
        group where min_input_switching_count or
 max_input_switching_count is defined. (LBDB-802)
```

Feedback

What Next

Check the library source file, and make the necessary correction.

LBDB-803

(error) %s and %s are required for all %s\n \tgroups within this %s group.

Description

If min_input_switching_count and max_input_switching_count are specified in one of switching_group groups within a dynamic_current group, then they must be defined in the rest of switching_group groups.

This message indicates that min_input_switching_count and max_input_switching_count are not defined in all switching_group groups within a dynamic_current.

The following example shows an instance where this message occurs:

```
cell(lbdb803) {
    ...
  dynamic_current() {
     ...
   switching_group() {
      pg_current(V1) {
        vector(test_3) {
          reference_time : 193.2;
          index_1("1.1");
          index_2("18.2 18.3 19.0");
          values("13.78 192.4 1100.1");
         }
        vector(test_3) {
          reference_time : 193.2;
          index_1("1.8");
          index_2("18.2 19.4 19.8");
          values("11.78 112.4 1110.1");
         }
        vector(test_3) {
          reference_time : 193.2;
          index_1("2.1");
          index_2("18.2 19.4 19.8");
          values("12.78 122.4 1120.1");
         }
         ...
       }
    }
   switching_group() {
      min_input_switching_count : 1;
      max_input_switching_count : 9;
      pg_current(V2) {
        vector(test_3) {
```

```
          ...
          }
        vector(test_3) {
          ...
          }
          ...
       }
     }
  }
  ...
```

In this case, min_input_switching_count and max_input_switching_count are defined in second switching_group, but not in first switching_group. This is wrong. min_input_switching_count and max_input_switching_count are required for all switching_group groups if they are defined in one of switching_group under the same dynamic_current. To fix the problem, please define min_input_switching_count and max_input_switching_count in first switching_group.

The following is an example message:

```
Errorr Line 272, min_input_switching_count and max_input_switching_count
 are required for all switching_group
        groups within this dynamic_current group. (LBDB-803)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-804

(error) The switching count shall cover all bits in related_inputs.

Description

The max_input_switching_count and min_input_switching_count attributes defined in a dynamic_current shall cover all bits specified in related_inputs.

The following example shows an instance where this message occurs:

```
type(bus6) {
  base_type : array ;
  data_type : bit ;
  bit_width : 6 ;
  bit_from : 5 ;
  bit_to : 0 ;
  downto : true ;
}
cell (libdb804) {
  bus(sel) {
    bus_type : bus6 ;
    direction : input ;
```

```
    ...
  }
  bundle(C) {
    members(Cx, Cy, Cz);
    direction : input;
    ...
  }
 pin(A1) {
  direction : input;
 ...
   }
 pin(A2) {
  direction : input;
  ...
   }
 pin(A3) {
  direction : input;
   ...
   }
  ...
  power_cell_type : macro;
  dynamic_current() {
    when : "A1";
    related_inputs : "Cx A3 Cy sel[0:3] A2";
    switching_group() {
      min_input_switching_count : 1;
      max_input_switching_count : 3;
      ...
    }
    switching_group() {
      min_input_switching_count : 5;
      max_input_switching_count : 8;
      ...
    }
  }
  ...
```

In this case, total number of bits in related_inputs is 8, so the switching count we specified in min_input_switching_count and max_input_switching_count shall cover number from 1 up to 8. The first switching group covers number from 1 to 3 and second switching group covers number from 5 to 8. The number 4 is not covered by any switching count within the dynamic_current. This is wrong. To fix the problem, change the third switching_group as follows :

```
switching_group() {
      min_input_switching_count : 4;
      max_input_switching_count : 4;
      ...
    }
```

Feedback

The following is an example message:

```
Error Line 272, The switching count shall cover all bits in
 related_inputs. (LBDB-804)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-805

(error) The value of %s is invalid.

Description

The message indicates that you are breaking one of following rules :

1> The value of min_input_switching_count must be greater than 0. 2> The value of max_input_switching_count must be greater than or equal to min_input_switching_count. 3> The value of max_input_switching_count must be less than or equal to total number of bits in related_inputs

The following example shows an instance where this message occurs:

```
type(bus6) {
  base_type : array ;
  data_type : bit ;
  bit_width : 6 ;
  bit_from : 5 ;
  bit_to : 0 ;
  downto : true ;
}
cell (libdb804) {
  bus(sel) {
    bus_type : bus6 ;
    direction : input ;
    ...
  }
  bundle(C) {
    members(Cx, Cy, Cz);
    direction : input;
    ...
  }
 pin(A1) {
  direction : input;
 ...
   }
 pin(A2) {
  direction : input;
  ...
   }
 pin(A3) {
```

```
direction : input;
 ...
 }
...
power_cell_type : macro;
dynamic_current() {
  when : "A1";
  related_inputs : "Cx A3 Cy sel[0:3] A2";
  switching_group() {
    min_input_switching_count : 0;
    max_input_switching_count : 9;
    ...
  }
  switching_group() {
    min_input_switching_count : 8;
    max_input_switching_count : 6;
    ...
  }
}
...
```

In this case, total number of bits in related_inputs is 8, so the switching count we specified in min_input_switching_count and max_input_switching_count shall cover only from 1 up to 8. 0 in min_input_switching_count is not a valid number, and 9 in max_input_switching_count is not a valid number, either. In the second switching_group, min_input_switching_count is greater than max_input_switching_count, which is wrong.

The following is an example message:

```
Error Line 272, The value of min_input_switching_count is invalid.
 (LBDB-805)
Error Line 272, The value of max_input_switching_count is invalid.
 (LBDB-805)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-806

(error) table_lookup is required model in ccs.

Description

The table_lookup is required delay_model for following ccs syntax forms :

ccs timing (driver and receiver), compact ccs timing, ccs noise, and ccs power

The message indicates that either there is no delay_model in your library or the delay_model you defined is not "table_lookup".

Feedback

The following example shows an instance where this message occurs:

```
library(libdb806) {
  ...
  cell(test_1) {
    pin(Z) {
      direction : output;
      timing() {
        compact_ccs_rise(template) {
          ....
        }
        compact_ccs_fall(template) {
          ....
        }
      }
    }
    ...
  }
  ...
}
```

In this case, ccs compact is defined but there is no delay_model specified, which is wrong. This is the fix to avoid the error message.

```
library(libdb806) {
  delay_model : table_lookup;
  ...
  cell(test_1) {
    ...
}
```

The following is an example message:

```
Error Line 272, table_lookup is required model in ccs. (LBDB-806)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-807

(error) The power_down_function is not allowed in test_cell.

Description

The power_down_function attribute can not be specified under test_cell group.

The following example shows an instance where this message occurs:

```
cell(libdb807) {
  ...
    test_cell() {
```

```
      pin(QN) {
        direction : output;
        power_down_function : "!VDD + VSS";
        function : "IQN";
        signal_type : test_scan_out_inverted;
      }
    }
  ...
}
```

In this case, power_down_function attribute is defined under a test_cell, which is wrong. You can avoid the message by comment out power_down_function attribute.

The following is an example message:

```
Error Line 272, The power_down_function is not allowed in test_cell.
 (LBDB-807)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-808

(error) The %s can't be specified if %s is not defined.

Description

The nominal tables must be specified if variation-aware tables are there. Meaning the following variation-aware tables can be specified only if the corresponding nominal tables are defined.

va tables : va_compact_ccs_rise , va_compact_ccs_fall va_receiver_capacitance1_rise , va_receiver_capacitance2_rise va_receiver_capacitance1_fall , va_receiver_capacitance2_fall va_rise_constraint, va_fall_constraint and va_leakage_current

corresponding nominal tables : compact_ccs_rise , compact_ccs_fall receiver_capacitance1_rise , receiver_capacitance2_rise receiver_capacitance1_fall , receiver_capacitance2_fall rise_constraint, fall_constraint and leakage_current

For the leakage_current, we need to consider when statement. Meaning that va_leakage_current can be defined only if leakage_current with the same state condition as what va_leakage_current has and it is defined within the same cell as where va_leakage_current is deinfed.

The same rule is applied to gate_leakage. The gate_leakage in va_leakage_current can't be specified if gate_leakage with same pin name is not defined in leakage_current, and both va_leakage_current and leakage_current are under the same state condition.

Feedback

The following example shows an instance where this message occurs:

```
pin(QN) {
   ...
   pin_based_variation() {
      va_parameters(var1, var2);
      nominal_va_values(10.0, 20.0);
      va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
        va_values(10.0, 21.0);
        values ( \
          "1.100, 1.100, 1.100");
      }
      ...
    }
  }
```

In this case, there is no receiver_capacitance specified within QN pin, so it is wrong to define va_receiver_capacitance1_rise table.

The following is the example message:

```
Error: Line 341, The va receiver cap can't be specified if nominal
 receiver cap is not defined. (LBDB-808)
```

The following example shows another instance where this message occurs:

```
leakage_current() {
     when : "B1";
     ...
   }
   leakage_current() {
     when : "C1";
     ...
   }
   leakage_current() {
     when : "D1";
     ...
   }
   leakage_current() { /* default */
     ...
   }
   cell_based_variation() {
      va_parameters(var1, var2);
      nominal_va_values(10.0, 20.0);
      va_leakage_current() {
        when : "A1";
        va_values(10.0, 21.0);
        ...
      }
      ...
    }
  }
```

Feedback

In this case, there is no "when statement" A1 in leakage_current, but "when : A1" is defined in va_leakage_current, which is wrong.

The following is an example message:

```
Error: Line 246, The va_leakage_current can't be specified if
 leakage_current with the same state condition is not defined.
 (LBDB-808)
```

The following example shows another instance where this message occurs:

```
leakage_current() {
     when : "A2";
     pg_current(V1) {
       value : 4.5;
     }
     pg_current(G1) {
       value : -4.5;
     }
     gate_leakage(A2) {
       input_high_value : 7.1;
     }
   }
   cell_based_variation() {
      va_parameters(var1);
      nominal_va_values(10.0);
      va_leakage_current() {
        when : "A2";
        va_values(11.0);
        pg_current(V1) {
          value : 4.5;
        }
        pg_current(G1) {
          value : -4.5;
        }
        gate_leakage(A1) {
         input_high_value : 9.3;
         input_low_value : -8.7;
        }
      }
      ...
    }
  }
```

The gate_leakage "A1" is defined under va_leakage_current, but it is not defined under leakage_current, where va_leakage_current and leakage_current have same state condition (when : "A2"). This violate the rule.

The following is the example message:

```
Error: Line 161, The gate_leakage in va_leakage_current can't be
 specified if gate_leakage in leakage_current is not defined.  (LBDB-808)
```

Feedback

What Next

Check the library source file, and make the necessary correction.

LBDB-809

(error) The left_id and right_id must be either defined in\n \tpairs or non-defined.

Description

The left_id and right_id are optoinal attributes for variation-aware compact table. If they are defined, then they must be defined in pairs.

The following example shows an instance where this message occurs:

```
library(libdb809) {
 ...
 compact_lut_template(va_test){
  variable_1 : input_net_transition ;
  variable_2 : total_output_net_capacitance ;
  variable_3 : curve_parameters;
  index_1 ( "5.236700e-02, 6.042500e-02, 8.710600e-02" ) ;
  index_2 ( "1.000000e-03, 1.511000e-03" ) ;
  index_3 ("init_current, peak_current, peak_voltage, peak_time,
 left_id");
  base_curves_group : "tt";
 }
 ...
   timing () {
     ...
      timing_based_variation() {
        va_parameters(var1, var2);
        nominal_va_values(10.0, 20.0);
        va_compact_ccs_rise(va_test) {
         va_values(10.0, 21.0);
         values ( \
            "0.01, 3.45, 3.20, 1.3, 1", "1.01, 2.45, 4.20, 2.3, 1",
 "2.01, 3.35, 5.20, 3.3, 1","3.01, 4.45, 6.20, 4.3, 1","4.01, 5.45, 7.20,
 5.3, 1", "6.01, 7.45, 8.20, 6.3, 1");
       }
     }
   ...
}
```

In this case, va_compact_ccs_rise is referring to a template, va_test, which has only left_id without right_id. This is wrong. To avoid the error message, you shall either remove left_id from the template or define right_id in the template.

The following is an example message:

```
Error: Line 813, The left_id and right_id must be either defined in
        pairs or non-defined. (LBDB-809)
```

Feedback

What Next

Check the library source file, and make the necessary correction.

LBDB-810

(error) The %s can't be empty.

Description

There must be at least one variable specified in va_parameters attribute.

The following example shows an instance where this message occurs:

```
pin_based_variation() {
        va_parameters();
        ...
    }
```

In this case, there is no value inside va_parameters, which is wrong. You can specified a list of variables in va_parameters(), and the list can't be empty.

The following is an example message:

```
Error: Line 1029, The va_parameters can't be empty. (LBDB-810)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-811

(error) The %s must be defined before %s is defined.

Description

The va_parameters can be defined within library(), timing_based_variation(), pin_based_variation() or cell_based_variation() group.

The va_parameters is referred by nominal_va_values and va_values, and must be defined before nominal_va_values and va_values are defined.

The following example shows an instance where this message occurs:

```
library(libdb811) {
  ...
    pin_based_variation() {
        nominal_va_values(10.0, 20.0);
        ...
        va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
         va_values(10.0, 21.0);
```

Feedback

```
          values ( \
             "1.100, 1.100, 1.100");
          }
      }
    ...
    va_parameters(var1, var2);
}
```

In this case, there is no va_parameters attribute defined inside either library() or pin_based_variation() before nominal_va_values and va_values. To fix the problem, please move va_parameters(var1, var2) to the line above pin_based_variation().

```
library(libdb811) {
  va_parameters(var1, var2);
  ...
    pin_based_variation() {
        nominal_va_values(10.0, 20.0);
        ...
        va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
         va_values(10.0, 21.0);
         values ( \
            "1.100, 1.100, 1.100");
        }
    }
  ...
}
```

Or, you can move the va_parameters(var1, var2) to the line above nominal_va_values(10.0, 20.0).

```
library(libdb811) {
  ...
    pin_based_variation() {
        va_parameters(var1, var2);
        nominal_va_values(10.0, 20.0);
        ...
        va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
         va_values(10.0, 21.0);
         values ( \
            "1.100, 1.100, 1.100");
        }
    }
  ...
}
```

The following is an example message:

```
Error: Line 626, The va_parameters must be defined before
 nominal_va_values is defined. (LBDB-811)
Error: Line 638, The va_parameters must be defined before va_values is
 defined. (LBDB-811)
```

Feedback

What Next

Check the library source file, and make the necessary correction.

LBDB-812

(error) The size of %s and %s must be identical.

Description

When the above-mentioned attributes are specified, they must be of the same size.

This rule applies to:

1. receiver_capacitance_fall_threshold_pct and receiver_capacitance_rise_threshold_pct.
2. va_parameters, nominal_va_values, and va_values.

The following example shows an instance where this message occurs:

```
library(libdb821) {
  ..
  receiver_capacitance_rise_threshold_pct("0 50 60 70 80 90 100 ");
  receiver_capacitance_fall_threshold_pct("100 50 40 30 20 10 ");
  ...
}
```

The two attribtues are of different sizes (7 versus 6).

Examples

The following is an example message:

```
Error: Line 18, The size of receiver_capacitance_fall_threshold_pct and
 receiver_capacitance_rise_threshold_pct must be identical. (LBDB-812)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-813

(error) The values in %s must be unique.

Description

This error message occurs when the specified variables in va_parameters are not unique or when the variable name in ff/latch/ff_bank/latch_bank is not unique.

Feedback

The following example shows an instance where this message occurs: The following example is incorrect, because there are 2 var2 entries in va_parameters:

```
va_parameters(var1, var2, var2, var4); i
```

This causes the following error message:

```
Error: Line 363, The values in va_parameters must be unique.
(LBDB-813)
```

In this example, the second and the third ff have the same variable name of IQ1, which is incorrect. All variable names in an ff group within a cell must be unique.

```
cell (LBDB-813) {
   ...
   ff ("IQ","IQN") {
          ...      }
   ff ("IQ1","IQN1") {
          ...      }
   ff ("IQ1","IQN2") {
          ...      }
   ...
}
```

This results in the following error message:

```
Error: Line 363, The values in ff/latch/ff_bank/latch_bank must
be unique.  (LBDB-813)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-814

(error) The values in %s must be the same as defined values.

Description

The following predefined parameters can be specified in *va_parameters*:

- The parameters defined in default_operating_conditions, such as process, temperature, and voltage
- The voltage names defined in voltage_map

If these predefined parameters are specified in *va_parameters*, then the values defined in *nominal_va_values* must match the values of the predefined parameters.

Feedback

If both *default_operating_conditions* and *voltage_map* are defined, and *voltage* is defined in *va_parameters*, then Library Compiler considers *voltage* as a user-defined parameter, an exception to the rule.

What Next

Check the library source file, and make sure the values are correct.

In the following example, the predefined parameter *voltage* is specified in *va_parameters*, and the corresponding value in *nominal_va_values* is defined as 15.1. This value is incorrect because it will be the same value of 9.0 as defined in *default_operating_conditions*, WCCOM. For the *process* predefined parameter, 35.0 in *nominal_va_values* is incorrect, because it is not the same value of 1.5 as defined in *default_operating_conditions*.

```
library(libdb814) {
    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 45 ;
        voltage : 9.0 ;
        tree_type : "worst_case_tree" ;
    }
    default_operating_conditions : WCCOM;
    ...
      timing_based_variation() {
        va_parameters(voltage, var2, process, temperature);
        nominal_va_values(15.1, 25.0, 35.0, 45.0);
        ...
      }
    ...
}
```

In the example below, both *default_operating_conditions* and *voltage_map* are defined. The *voltage* is user-defined parameter, (not a predefined parameter), which means you can specify any voltage value in *nominal_va_values*. However, VDD is a predefined parameter in *voltage_map*. If you specified it in *va_parameters*, then the corresponding value of 10.0 in *nominal_va_values* will be the same as the value of 9.0 defined in *voltage_map*. The values are not the same, so the error message is generated.

```
library(libdb814) {
    ...
    voltage_map( VDD, 9.0);
    voltage_map(VDDH, 4.91);
    voltage_map(VDDL, 4.80);
    voltage_map(VSS, 0.0);

    operating_conditions(WCCOM) {
        process : 1.5 ;
        temperature : 45 ;
        voltage : 9.0 ;
        tree_type : "worst_case_tree" ;
```

Feedback

```
    }
    default_operating_conditions : WCCOM;
    ...
      timing_based_variation() {
        va_parameters(voltage, var2, VDD, temperature);
        nominal_va_values(15.1, 25.0, 10.0, 45.0);
        ...
      }
    ...
}
```

LBDB-815

(error) The number of %s in %s must be exactly twice the number of the values in va_parameters.

Description

This error message occurs when the number of variation tables does not equal twice the number of the values in *va_parameters*.

The following are the possible variation tables that you can specify under *pin_based_variation*:

```
va_receiver_capacitance1_rise
va_receiver_capacitance2_rise
va_receiver_capacitance1_fall
va_receiver_capacitance2_fall
```

in -25i

The following are the possible variation tables that you can specify under *timing_based_variation*:

```
va_receiver_capacitance1_rise
va_receiver_capacitance2_rise
va_receiver_capacitance1_fall
va_receiver_capacitance2_fall
va_rise_constraint
va_fall_constraint
va_compact_ccs_rise
va_compact_ccs_fall
```

The total number of these tables must be exactly twice number of values in *va_parameters*.

The following example shows an instance where this message occurs: In the following example, there are 5 *va_receiver_capacitance1_rise groups* under *timing_based_variation*. Since the size of va_parameters is 2, var1 and var2, the total number of *va_receiver_capacitance1_rise* groups will be 4 instead of 5.

Feedback

```
timing_based_variation() {
  va_parameters(var1, var2);
  nominal_va_values(15.0, 25.0);
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(16.0, 25.0);
    values ( \
      "1.100, 1.100", "1.100, 1.100", "1.100, 1.100");
  }
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(14.0, 25.0);
    values ( \
      "1.200, 1.200", "1.200, 1.200", "1.200, 1.200");
  }
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(15.0, 26.0);
    values ( \
      "1.300, 1.300", "1.300, 1.300", "1.300, 1.300");
  }
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(15.0, 24.0);
    values ( \
      "1.400, 1.400", "1.400, 1.400", "1.400, 1.400");
  }
  va_receiver_capacitance1_rise ( va_TB2INVXC_rise_1 ) {
    va_values(15.0, 23.0);
    values ( \
      "1.400, 1.400", "1.400, 1.400", "1.400, 1.400");
  }
 ...
```

What Next

Check the library source file, make the necessary corrections, and run the command again.

LBDB-816

(error) %s in this group and %s defined in %s\n \tshall have identical values on all but one.

Description

The values you specified in va_values and nominal_va_values must be identical except for one value.

The following example shows an instance where this message occurs:

```
pin_based_variation() {
  va_parameters(var1, var2, var3, var4);
  nominal_va_values(15.0, 25.0, 35.0, 45.0);
  va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
    va_values(15.0, 25.0, 35.0, 45.0);
    values ( \
```

```
      "1.100, 1.100, 1.100");
  }

  va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
    va_values(14.0, 25.0, 35.0, 45.0);
    values ( \
      "1.200, 1.200, 1.200");
  }

  va_receiver_capacitance1_rise ( pinTB2INVXC_rise_1 ) {
    va_values(15.0, 26.0, 36.0, 45.0);
    values ( \
      "1.300, 1.300, 1.300");
  }
   ...
```

In the first va_receiver_capacitance1_rise, all values in nominal_va_values and va_values are the same, which is wrong. There must be one value difference.

In the second va_receiver_capacitance1_rise, var1 has different value between va_values and nominal_va_values, which is okay.

In the third va_receiver_capacitance1_rise, var2 and var3 have different values between va_values and nominal_va_values, which is wrong. Only one value is allowed to be different.

The following is an example message:

```
Error: Line 381, va_values in this group and nominal_va_values defined in
 pin_based_variation
        shall have identical values on all but one.      (LBDB-816)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-817

(error) For %s groups in %s, one characterization point\n \tis required and up to two points are allowed for each parameter.

Description

At least one characterization point is required for each parameter, and only up to two points are allowed. The value of characterization point must be different from the nominal value. If there are two points, then one must be greater than nominal value, and the other must be less than nominal value.

This rule also applies for all va_leakage_current groups under the same state condition.

Feedback

The following example shows an instance where this message occurs:

```
timing_based_variation() {
  va_parameters(var1, var2);
  nominal_va_values(15.0, 25.0);
  va_compact_ccs_rise(va_lut) {
     va_values(16.0, 25.0);
     values ( ... );
  }
  va_compact_ccs_rise(va_lut) {
     va_values(19.0, 25.0);
     values ( ... );
  }
  va_compact_ccs_rise(va_lut) {
     va_values(15.0, 26.0);
     values ( ... );
  }
  va_compact_ccs_rise(va_lut) {
     va_values(15.0, 24.0);
     values ( ... );
  }
  ...
}
```

For the parameter var1, there are two variations (19.0 and 16.0), and both of them are greater than nominal value 15.0, which is wrong.

The following example shows another instance where this message occurs:

```
timing_based_variation() {
        va_parameters(var1, var2);
        nominal_va_values(15.0, 25.0);
            va_rise_constraint(va_sup_hld) {
                va_values(16.0, 25.0);
                index_1(" 0.006, 0.04, 0.1, 0.2, 1");
                index_2(" 0.006, 0.04, 0.1, 0.2, 1");
                values( ...);
                }
            va_rise_constraint(va_sup_hld) {
                va_values(14.0, 25.0);
                index_1(" 0.006, 0.04, 0.1, 0.2, 1");
                index_2(" 0.006, 0.04, 0.1, 0.2, 1");
                values( ...);
                }
            va_rise_constraint(va_sup_hld) {
                va_values(16.0, 25.0);
                index_1(" 0.006, 0.04, 0.1, 0.2, 1");
                index_2(" 0.006, 0.04, 0.1, 0.2, 1");
                values( ...);
                }
           va_rise_constraint(va_sup_hld) {
                va_values(15.0, 24.0);
                index_1(" 0.006, 0.04, 0.1, 0.2, 1");
```

Feedback

```
                index_2(" 0.006, 0.04, 0.1, 0.2, 1");
                values( ...);
                }
        ...
```

For parameter var1, there are three variation values (16.0, 14.0 and 16.0 again). This is wrong because only up to 2 points are allowed. For parameter var2, there is only one variation value (24.0), which is okay.

The following example shows another instance where this message occurs:

```
cell_based_variation() {
        va_parameters(var1, var2);
        nominal_va_values(15.0, 25.0);
            va_leakage_current() {
                when : "A1";
                va_values(17.0, 25.0);
                 ...
                }
            va_leakage_current() {
                when : "A1";
                va_values(13.0, 25.0);
                 ...
                }
            va_leakage_current() {
                when : "!A1";
                va_values(17.0, 25.0);
                 ...
                }
            va_leakage_current() {
                when : "!A1";
                va_values(15.0, 29.0);
                 ...
                }
            va_leakage_current() {  /* default state */
                va_values(16.0, 25.0);
                 ...
                }
            va_leakage_current() {  /* default state */
                va_values(15.0, 26.0);
                 ...
                }
       } /* end of cell_based_variation */
         ...
```

Under the when statement "A1", there is no characterization point for var2, which is wrong, and var1 have two points (17.0 and 13.0), which are okay. For the cases with state condition "!A1" and without any state condition (default state), both are okay.

The following is an example message:

```
Error: Line 552, For va_rise_constraint groups in timing_based_variation,
 one characterization point
```

Feedback

```
        is required and up to two points are allowed for each parameter.
 (LBDB-817)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-818

(error) At least, one of the variation-aware groups is absent.

Description

This message indicates that at least you are missing one of the variation-aware tables. Here is the rule : if both of nominal tables are defined, then either no variation-aware table is required or all variation-aware tablea are required. Meaning that if all nominal tables are defined, then you can't not just define partial of correspoding variation-aware tables.

The following example shows an instance where this message occurs:

```
timing() {
       ...
         fall_constraint(sup_hld) {
            index_1(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
     ");
            index_2(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
     ");
            values( ...
         }
         rise_constraint(sup_hld) {
            index_1(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
     ");
            index_2(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
     ");
            values( ...
         }
         timing_based_variation() {
         ...
            va_rise_constraint(va_sup_hld) {
              ...
              values( ...
         ...}
      ...}
 ,,,}
```

In this case, both nominal tables (fall_constraint and rise_constraint) are defined and only one of variation-aware tables (va_rise_constraint) is defined, which is wrong. To fix the problem, add va_fall_constraint:

```
timing() {
       ...
```

Feedback

```
      fall_constraint(sup_hld) {
         index_1(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
   ");
         index_2(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
   ");
         values( ...
      }
      rise_constraint(sup_hld) {
         index_1(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
   ");
         index_2(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
   ");
         values( ...
      }
      timing_based_variation() {
      ...
         va_rise_constraint(va_sup_hld) {
           ...
           values( ...
      ...}
         va_fall_constraint(va_sup_hld) {
           ...
           values( ...
      ...}

   ...}
...}
```

or remove va_rise_constraint from the timing arc :

```
timing() {
     ...
      fall_constraint(sup_hld) {
         index_1(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
   ");
         index_2(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
   ");
         values( ...
      }
      rise_constraint(sup_hld) {
         index_1(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
   ");
         index_2(" 0.006    ,  0.04     ,  0.1      ,  0.2      ,  1
   ");
         values( ...
      }
      timing_based_variation() {
      ...
   ...}
...}
```

Feedback

The following is an example message:

```
Error: Line 552 At least, one of the variation-aware groups is absent.
 (LBDB-818)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-819

(warning) The %s %s is not present, so\n \taccuracy can be deteriorated.

Description

You will get the warning due to the following reason : - If CCS timing driver model is defined, then CCS timing receiver model is expected to be there, too.

The following example shows an instance where this message occurs:

```
...
    pin(I) {
      direction : input ;
      capacitance : 0.0014397 ;
      rise_capacitance : 0.0013000 ;
      fall_capacitance : 0.0012000 ;
    }
    pin(Z) {
      direction : output ;
      max_capacitance : 0.17890 ;
      function : "I" ;

      timing() {
        related_pin : "I" ;
        timing_sense : positive_unate ;
        cell_rise(delay_template_7x7) {
          ...
        }
        rise_transition(delay_template_7x7) {
          ...
        }
        cell_fall(delay_template_7x7) {
                  ...
        }
        fall_transition(delay_template_7x7) {
                   ...
        }
        output_current_fall() {
           ...
        }
        output_current_rise() {
           ...
```

```
        }
        ...
      }
    ...
```

In this case, ccs receiver data for pin 'I' is expected because ccs driver model is defined.

The following is an example message:

```
Warning: Line 3186, The CCS receiver data is not present, so
        accuracy can be deteriorated. (LBDB-819)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-819e

(error) The %s %s is not present, so\n \taccuracy can be deteriorated.

Description

If CCS timing driver model is defined, then CCS timing receiver model is expected to be there, too. If both pin-based and arc-based receiver model is missing for the pin in a CCS library, you will get this error.

The following example shows an instance where this message occurs:

```
...
    pin(I) {
      direction : input ;
      capacitance : 0.0014397 ;
      rise_capacitance : 0.0013000 ;
      fall_capacitance : 0.0012000 ;
    }
    pin(Z) {
      direction : output ;
      max_capacitance : 0.17890 ;
      function : "I" ;

      timing() {
        related_pin : "I" ;
        timing_sense : positive_unate ;
        cell_rise(delay_template_7x7) {
          ...
        }
        rise_transition(delay_template_7x7) {
          ...
        }
        cell_fall(delay_template_7x7) {
                  ...
        }
```

```
        fall_transition(delay_template_7x7) {
                  ...
        }
        output_current_fall() {
           ...
        }
        output_current_rise() {
           ...
        }
        ...
      }
    ...
```

In this case, ccs receiver data for pin 'I' is expected because ccs driver model is defined.

The following is an example message:

```
Warning: Line 3186, The CCS receiver data is not present, so
        accuracy can be deteriorated. (LBDB-819e)
```

What Next

Check the library source file, and add the missing receiver model.

LBDB-820

(error) The %s is preferred pg type.

Description

If the cell is an always_on cell, then for all signal pins, the backup_power is preferred pg_type that related_power_pin shall refer to, and backup_ground is preferred pg_type that related_ground_pin shall refer to.

The following example shows an instance where this message occurs:

```
cell(test) {
   always_on : TRUE;
   pg_pin(PWR) {
   voltage_name : VDD;
   pg_type : primary_power;
   }
   pg_pin(GND) {
   voltage_name : VSS;
   pg_type : primary_ground;
   }
   pg_pin(GND1) {
   voltage_name : VSS1;
   pg_type : backup_ground;
   }
   pg_pin(VDDI) {
   voltage_name : VDDH;
```

Feedback

```
    pg_type : backup_power;
    }
    ...
    pin(A1) {
         always_on : TRUE;
         direction : input;
         related_power_pin : PWR;
         related_ground_pin : GND1;
       ...
    }
    pin(A2) {
         direction : input;
         related_power_pin : VDDI;
         related_ground_pin : GND;
      ...
    }
    ...
}
```

For the always_on pin, A1 , the related_power_pin is pointing to PWR, which is not backup_power. For the non always_on pin, A2, the related_ground_pin is pointing to GND, which is not backup_ground either. Both of them shall connect to backup PG.

The following is an example message:

```
Error: Line 335, The backup_power is preferred pg type. (LBDB-820)
Error: Line 385, The backup_ground is preferred pg type. (LBDB-820)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-821

(error) The always_on pin is required for always_on cells.

Description

An always_on cell requires at least one or more always_on pin under it.

The following example shows an instance where this message occurs:

```
cell(test) {
    always_on : TRUE;
    ...
    pin(sp) {
         direction : input;
         related_power_pin : PWR;
         related_ground_pin : GND;
       ...
    }
    pin(a) {
```

```
        ...
    }
    ...
}
```

Since 'test' cell is an always_on cell, the always_on attribute is required to be specified at least in one of pins under 'test' cell.

The following is an example message:

```
Error: Line 1548, The always_on pin is required for always_on cells.
 (LBDB-821)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-822

(error) A pin can only has either non-programmable or\n \tprogrammable driver types.

Description

Under a pin, there can only be either non-programmable driver type or programmable driver types, but not both.

The following example shows an instance where this message occurs:

```
pin(ZN) {
  direction : inout;
  pull_up_function : "!A1 * !A2 * !A3";
  pull_down_function : "A1 * A2 * !A3";
  bus_hold_function : "A1 * !A2 * !A3";
  driver_type : pull_up;
  ...
 }
```

In pin ZN, there are three programmable driver types, pull_up_function, bus_hold_function, and pull_down_function. Also, the non-programmable driver type, "driver_type : pull_up", is defined under the same pin, which is wrong. Please remove either programmable driver types or non-programmable driver type from the pin.

The following is an example message:

```
Error: Line 104, A pin can only has either non-programmable or
        programmable driver types. (LBDB-822)
```

What Next

Check the library source file, and make the necessary correction.

Feedback

LBDB-823

(information) The %s %s is not present, so\n \taccuracy can be deteriorated.

Description

You will get the message due to one of following reasons : - ccs model is expected to be defined to improve the data accuracy.

The following example shows an instance where this message occurs:

```
...
      timing() {
        related_pin : "I" ;
        timing_sense : positive_unate ;
        cell_rise(delay_template_7x7) {
          ...
        }
        rise_transition(delay_template_7x7) {
          ...
        }
        cell_fall(delay_template_7x7) {
                  ...
        }
        fall_transition(delay_template_7x7) {
                   ...
        }
        ...
      }
```

In this case, there is no ccs timing model but NLDM, and we expected ccs timing models for better accuracy.

The following is an example message:

```
Information: Line 582, The CCS data output_current_rise is not present,
 so
        accuracy can be deteriorated. (LBDB-823)
Information: Line 582, The CCS data output_current_fall is not present,
 so
        accuracy can be deteriorated. (LBDB-823)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-824

(error) This static '%s' group cannot be specified in a '%s' group at line %u.

Feedback

Description

This message indicates that a static ccsn_*_stage or input/output_ccb group has been specified in a timing arc or input/internal pin. This is not allowed.

A static CCS/CCB noise model captures the behaviors of a static channel connected block. A static channel connected block does not have any input terminal or the voltage level at the input terminal does not affect the output current of the block. It cannot be used for propagating crosstalk delay or noise waveforms through the cell under study. Consequently, the only use for a static noise model is for a tie-off pin that is permanently 0 or 1. Please refer to "CCS Noise Library Characterization Guide" for detailed information.

The following is an example message:

```
Error: Line 27, The 'timing' group cannot specify a static
 'ccsn_first_stage' group. (LBDB-824)
```

What Next

Replace the aforementioned data with a non-static ccsn_*_stage or *_ccb group.

LBDB-826

(error) The %s entry cannot be found for %s(%s) of cell(%s).

Description

This message indicates that you do not specify the relative entry in the map file required by add_pg_pin_to_db command.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error: The pg_to_voltage_map entry cannot be found for pg_pin(VDD) of
 cell(sample). (LBDB-826)
```

LBDB-826w

(warning) The %s entry cannot be found for %s(%s) of cell(%s).

Description

This warning message occurs when there is no related entry for *pg_pin*, *rail_connection*, or other attributes specified in the map file required by the *add_pg_pin_to_db* command.

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: The pg_to_voltage_map entry cannot be found for pg_pin(VDD) of
 cell(sample). (LBDB-826w)
```

What Next

This is only a warning message. No action is required.

However, you can eliminate this warning message by adding the required entry to the map file.

LBDB-827

(error) The input library '%s' has not been read in.

Description

This message indicates that the input library has not been read in.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error: The input library 'a.db' has not been read in. (LBDB-827)
```

LBDB-828

(error) The input library '%s' is pg_pin-based library.

Description

This message indicates that the input library is pg_pin-based.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error: The input library 'a.db' is pg_pin-based library. (LBDB-828)
```

What Next

The input library is already pg_pin based, and no need to be converted by the utility. However, if you want to add or update the library with pg or power management attributes, you should specify a tcl file with update_lib_model and associated commands.

Feedback

LBDB-828w

(warning) The input library '%s' is pg_pin-based library.

Description

This message indicates that the input library is pg_pin-based.

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: The input library 'a.db' is pg_pin-based library. (LBDB-828w)
```

What Next

The input library is already pg_pin based, and only incremental update will be performed.

LBDB-829

(error) The input library '%s' does not have default operating_conditions.

Description

This message indicates that the input library does not have default operating_conditions.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error:  The input library 'A.db' does not have default
 operating_conditions. (LBDB-829)
```

LBDB-830

(error) The input library '%s' does not have 'voltage' attribute in the default operating_conditions '%s'.

Description

This message indicates that the input library does not have default operating_conditions.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error:  The input library 'A.db' does not have 'voltage' attribute  in
 trhe default operating_conditions 'nom_pvt'. (LBDB-830)
```

Feedback

LBDB-831

(error) The converted voltage_map table is empty.

Description

This message indicates that converted voltage_map table is empty.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error:  The converted voltage_map table is empty. (LBDB-831)
```

LBDB-832

(error) The number of pg_pin's generated for cell(%s) is %d, which is less than 2.

Description

This message indicates that the number of generated pg_pin's for the cell is less than the required minimum value (2).

The following example shows an instance where this message occurs:

The following is an example message:

```
Error:  The number of pg_pin's generated for cell(A) is 1, which is less
 than 2. (LBDB-832)
```

LBDB-833

(error) The related_pg_pin for %s %s power_level(%s) of cell(%s) cannot be found.

Description

This message indicates that the related_pg_pin entry cannot be found for internal_power/ leakage_power group.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error:  The related_pg_pin for cell-level internal_power power_level(VDD)
 of cell(A). (LBDB-833)
```

LBDB-834

(error) The related_pg_pin for %s %s of cell(%s) cannot be found.

Feedback

Description

This message indicates that the related_pg_pin entry cannot be found for internal_power/ leakage_power group.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error:  The related_pg_pin for cell-level internal_power of cell(A).
 (LBDB-834)
```

LBDB-835

(error) For cell(%s), the %s(%s) which is the %s of pin(%s) cannot be found.

Description

This message indicates that you do not specify the power/ground pg_pin of a cell in the map file required by add_pg_pin_to_db command.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error: For cell(sample), the pg_pin(VDD) which is the related_power_pin
 of pin(A) cannot be found. (LBDB-835)
```

LBDB-836

(warning) Unable to convert to %s from pin(%s) of cell(%s).

Description

This message indicates that add_pg_pin_to_db or update_lib_model command cannot 1) convert to pg_pin from the signal pin. In the following cases, it cannot be converted to pg_pin: a) pin(VDD) with timing, internal_power, ccsn_first_stage/ccsn_last_stage or receiver_capacitance group, where VDD is a PG pin in FRAM view. b) pin(VDD) referenced in function/statetable expressions in the cell. c) pin(VDD) referenced in the when or related_pin of the other pin's internal_power groups or when in other pin's ccsn_first_stage, ccsn_last_stage or receiver_capacitance groups or leakage_power, dynamic_current, leakage_current or intrinsic_parasitic groups in the cell. 2) generate related_power_pin/related_ground_pin for the specfied signal pin.

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: Unable to convert to pg_pin from pin(VDD) of cell(r1hd).
 (LBDB-836)
```

What Next

You can correct the pin group as described above. For example, if pin(VDD) has ccsn_first_stage group and you deem it is a pg_pin, you should remove the group under the pin to make the conversion. However, if it is an analog pin, you should not remove such a group and no conversion to pg_pin will be performed.

LBDB-837

(error) The %s for pin(%s) of cell(%s) cannot be found.

Description

This message indicates that the related_power_pin/related_ground_pin cannot be found for the specified pin.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error:  The related_power_pin for pin(A) of cell(sample) cannot be found.
 (LBDB-837)
```

LBDB-838

(error) Failed to find the file name for %s option.

Description

In add_pg_pin_to_db command, some options have dependency and requirement. (1) An output db file name must be specified in -output option and must be different from the input db file. (2) If -mw_library_name is not specified, -pg_map_file must be specified, and vice versa. (3) If the Milkyway library does not cover all cells in db, -pg_map_file must be specified. (4) the map file name must be valid and exists in disk.

The following example shows an instance where this message occurs:

```
add_pg_pin_to_db input.db -output pg_pin.db
```

In this case, neither -pg_map_file nor -mw_library_name is specified. You will get the second error message in the following example.

The following is an example message:

```
Error: Failed to find the file name for -output option. (LBDB-838)
Error: Failed to find the file name for either -pg_map_file or
 -mw_library_name. (LBDB-838)
Error: Failed to find the file name for -pg_map_file option. (LBDB-838)
```

Feedback

What Next

Check the options to this command, and specify all the necessary ones.

LBDB-839

(warning) Partial Milkyway library for the input library file.

Description

In add_pg_pin_to_db command, when you specify -mw_library_name and the Milkyway library does not cover all cells in the input db, this warning will occur. This includes missing cells, as well as missing and mismatched pins. This is shown after check_library command is invoked under the hood, and you will also see Logic vs. physical library check summary: Number of cells missing in logic library: <number of missing cells>

The following example shows an instance where this message occurs:

```
add_pg_pin_to_db input.db -mw_library_name mwlib -pg_map_file pg.map
 -output pg_pin.db

In this case, Milkyway library mwlib does not cover all cells in
 input.db.
You will get the second error message in the following example.
```

The following is an example message:

```
Logic vs. physical library check summary:
Number of cells missing in logic library:       23
Logic library is INCONSISTENT with physical library.
Warning: Partial Milkyway library for the input library file. (LBDB-839)
```

What Next

First you need to check if the Milkyway library you specified is the correct one. Otherwise, you should specify mapping in the map file for those cells that do not exist or exist but have missing or mismatched pins in the Milkyway library. Otherwise, later checking in the flow will find such cells are not specified in the map file and pg_pin based db will not be generated. If you want to get a list of the missing cells and/or missing and mismatched pins, run check_library command for logic vs. physical library cross checking with default options. You do not need to use set_check_library_options command to set options. You only need to specify logic and Milkyway library names in check_library command.

LBDB-840

(warning) No %s found in map file.

Feedback

Description

In the map file, if any of the following occurs: (1) No BEGIN <section_name> or END <section_name> (2) incorrect <section_name> (3) incorrect key words in title line this message will be printed out. Valid section names include: PG_PIN_MAP PG_TO_VOLTAGE_MAP VOLTAGE_MAP POWER_DOWN_FUNCTION_MAP

Key words in title line include: (1) PG_TO_VOLTAGE_MAP section cell, pg_pin, voltage_name, pg_type and direction where key word direction is optional. (2) PG_PIN_MAP section cell, pin, rail_connection and pg_pin (3) VOLTAGE_MAP section voltage_name and voltage_value (4) POWER_DOWN_FUNCTION_MAP cell, pin and power_down_function

The key words in each title line should be in the above order and delimited by Tab or space(s). Invalid record will be ignored. If BEGIN or END section line or title line is missing, the whole section will be ignored. In the map file, the following lines are legal but will be ignored: (1) a comment line starting with # is a comment line and (2) a blank line

The following example shows an instance where this message occurs:

```
BEGIN PG_TO_VOLTAGE_MAP
cell            pg_pin          voltage_name    pg_type
ADDFHX1         VDD             VDD             power
ADDFHX1         VSS             VSS             primary_ground
END PG_TO_VOLTAGE_MAP
```

The following is an example message:

```
Warning: Line 14, No END section found in map file. (LBDB-840)
Warning: Line 20, No BEGIN section found in map file. (LBDB-840)
Warning: Line 44, No title line found in map file. (LBDB-840)
```

What Next

You should correct the syntax errors in the map file.

LBDB-841

(error) Failed to read input library '%s'.

Description

This message occurs when one or more of the following exist: 1) the input library file does not exist 2) the file cannot open for read 3) the library is not a valid technology library 4) the library file cannot compile. 5) .lib file loaded by read_db

The following example shows an instance where this message occurs:

The following is an example message:

```
Error: Failed to read input library 'rail.db'. (LBDB-841)
```

What Next

Check for the input library file name and location to make sure it exists with read permission. If it does, check if the input library is a valid technology library. If the library cannot compile, please check the Error messages during compilation, and correct them.

LBDB-842

(warning) Number of rail_connections %d for cell '%s' is not equivalent to number of power pins %d in %s.

Description

In cell group in db, rail_connection is used to specify power rails, not ground or internal pins. Therefore, if a rail_connection is for ground, such as VSS in the following example, the rail_connection is not valid.

The following example shows an instance where this message occurs:

```
cell (test) {
        rail_connection(VDD, VDD);
        rail_connection(VDD_AUX, VDD1);
        rail_connection(VSS, VSS);
        ...
    }

    In Milkyway library, cell test has VDD and VSS, but no VDD1.
```

The following is an example message:

```
Warning: Number of rail_connections 3 for cell 'test' is not equivalent
 to number of power pins 1 in Milkyway. (LBDB-842)
```

What Next

If you have more rail_connections in db than power pins in Milkyway or map file, check if the extra rail is proper or not. If not, you should remove it from db. Otherwise, there is mismatch between db and Milkyway (or map file if the cell is from map file) and the command will stop conversion for a new pg_pin db.

LBDB-843

(error) %s cell '%s' does not have %s pg_pins.

Feedback

Description

Each cell with NLDM, CCS-T and CCS-N has at least 2 pg_pins (1 power and 1 ground) while a load or pull_up (tieoff high) or pull_down (tieoff low) cell has at least one pg_pin as documented in LC manual. Further, a pull_up cell should have a power pg_pin while a pull_down cell should have a ground pg_pin.

The following example shows an instance where this message occurs:

```
BEGIN PG_TO_VOLTAGE_MAP
cell            pg_pin          voltage_name    pg_type
tieoff_pullup   VDD             VDD             primary_power
tieoff_pulldown VSS             VSS             primary_power
END PG_TO_VOLTAGE_MAP
where tieoff_pulldown cell does not have a ground pg_pin.
```

The following is an example message:

```
Error: Tieoff cell 'tieoff_pulldown' does not have ground pg_pins.
 (LBDB-843)
Error: cell 'ADDFHX4' pin 'A' does not have related_power pg_pins.
 (LBDB-843)
```

What Next

Check and specify the correct pg_pin in the map file: 1) for a cell with NLDM, CCS-T and CCS-N, check if there are at least 1 power and 1 ground pg_pin's, and 1 power and 1 ground pg_pin's for each signal pin. 2) for a load cell, check if there are at least 1 pg_pin 3) for a pull_up cell, check if there is 1 power pg_pin 4) for a pull_down cell, check if there is 1 ground pg_pin

---

LBDB-843w

(warning) %s cell '%s' does not have %s pg_pins.

Description

Each cell with NLDM, CCS-T and CCS-N has at least 2 pg_pins (1 power and 1 ground) while a load or pull_up (tieoff high) or pull_down (tieoff low) cell has at least one pg_pin as documented in LC manual. Further, a pull_up cell should have a power pg_pin while a pull_down cell should have a ground pg_pin.

The following example shows an instance where this message occurs:

```
BEGIN PG_TO_VOLTAGE_MAP
cell            pg_pin          voltage_name    pg_type
tieoff_pullup   VDD             VDD             primary_power
tieoff_pulldown VSS             VSS             primary_power
END PG_TO_VOLTAGE_MAP
where tieoff_pulldown cell does not have a ground pg_pin.
```

The following is an example message:

```
Warning: Tieoff cell 'tieoff_pulldown' does not have ground pg_pins.
 (LBDB-843w)
```

What Next

Check and specify the correct pg_pin in the map file: 1) for a cell with NLDM, CCS-T and CCS-N, check if there are at least 1 power and 1 ground pg_pin's, and 1 power and 1 ground pg_pin's for each signal pin. 2) for a load cell, check if there are at least 1 pg_pin 3) for a pull_up cell, check if there is 1 power pg_pin 4) for a pull_down cell, check if there is 1 ground pg_pin

---

LBDB-844

(warning) %s '%s' does not exist in input db. Remove it from map.

Description

When a cell and/or pin specified in the map file does not exist in the input db, it will be ignored and removed from the map. The cell may come from the map file or Milkyway. If it comes from Milkyway, no line number is printed out.

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: Line 24, Cell 'test' does not exist in input db. Remove it from
 map. (LBDB-844)
```

What Next

Check if the cell and/or pin is what you want. If so, you need to check the input db for the missing cell. Otherwise, ignore it or remove it from the map file.

LBDB-845

(error) %s '%s' is missing in %s.

Description

This error message occurs when a .db cell and/or pin is missing in the map file or its Milkyway library.

The following is an example message:

```
Error: Cell 'test' is missing in map file. (LBDB-845)
Error:  'Map data or FRAM' is missing in input. (LBDB-845)
```

Feedback

What Next

Add the mapping in the map file or specify the correct Milkyway library for the missing cells to generate a complete pg_pin based .db file. You can use the * (asterisk) wildcard character for all cells that are not explicitly specified in the map file. For dirty flow and on-the-fly PG library updates, input either Milkyway library or map data for non-rail_based .dbs. In the case of incremental updates to a PG library, specify a map file or a Tcl file for maps.

LBDB-845w

(warning) %s '%s' is missing in %s.

Description

If a power management attribute is missing in the cell, this message will occur. If a db cell and/or pin is missing in the map file or its Milkyway library, this message will be printed out. You need to add its mapping in the map file to generate a complete pg_pin based db file.

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: Cell 'LS16FROM16TO20' 'level_shifter_type' is missing in
 library'. (LBDB-845w)
```

What Next

You need to add the missing attribute for power management cells; otherwise, the cells will not be used for UPF. You need to add the mapping in the map file or specify the correct Milkyway library for the missing cells to generate a complete pg_pin based db file. You can use wild card "*" for all the cells that are not explicitly specified in the map file.

LBDB-846

(warning) Cell '%s' has %d %s pins in Milkyway library.

Description

If a cell has multiple power or ground pins in Milkyway and db, you should specify related_power_pin and related_ground_pin for its signal pins.

The following example shows an instance where this message occurs:

```
BEGIN PG_PIN_MAP
cell    pin rail_connection pg_pin
test    LSI VDD             VDD
test    LSO VDD_AUX         VDD_AUX
```

```
test    LSI -               VSS
test    LSO -               VSS
END PG_PIN_MAP
where cell test has 2 power pins: VDD and VDD_AUX.
```

The following is an example message:

```
Warning: Cell 'test' has 2 power pins in Milkyway library. (LBDB-846)
```

What Next

Check PG_PIN_MAP section in the map file to see if related_power_pin and related_ground_pin's are specified for these cells that have multiple P/G pins. This is only a warning message. In the flow that follows this message, there are other checkings that will catch error if you did not specify related_power_pin and related_ground_pin for these cells.

LBDB-847

(error) Too many values (%d) specified in the table.

Description

This message indicates that there are too many values specified in the table. (number = index1_size * index2_size [* index3_size] [*index4_size]). The number exceed the limit (32767) that Library Compiler current handles.

The following is an example message:

```
Error: Line 307, Too many values (45000) specified in the table.
 (LBDB-847)
```

What Next

Split the table, to make each table's size less than the limit.

LBDB-848

(error) There is no '%s' %s defined for '%s' %s.

Description

This message indicates the library does not define the voltage_map for the voltage_name specified in a pg_pin, or input_signal_level/output_signal_level defined in a pin, or the active state of pg pin/pg setting in pg_setting_value group.

The following example shows an instance where this message occurs:

```
voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);
```

Feedback

```
      voltage_map(VSS, 0.0);

        ...
      cell(sample) {
        pg_pin(VDD) {
                voltage_name : VDD2;
                ...
        }
        ...
      }
      ...
```

In this case, there is no voltage_map defined for voltage_name VDD2. To fix the problem, add the voltage_map attribute for VDD2 at the library level:

```
voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);
      voltage_map(VDD2, 1.2);
      voltage_map(VSS, 0);

        ...
      cell(sample) {
        pg_pin(VDD) {
                voltage_name : VDD2;
                ...
        }
        ...
      }
      ...
```

The following is an example message:

```
Error: Line 23, There is no 'VDD2' voltage_map defined for 'VDD2'
 voltage_name. (LBDB-848)
```

What Next

Add the missing voltage_map.

LBDB-848w

(warning) There is no '%s' %s defined for '%s' %s.

Description

This message indicates the library does not define the voltage_map for the voltage_name specified in a pg_pin, or input_signal_level/output_signal_level defined in a pin, or the active state of pg pin/pg setting in pg_setting_value group.

Feedback

The following example shows an instance where this message occurs:

```
voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);
      voltage_map(VSS, 0.0);

        ...
      cell(sample) {
        pg_pin(VDD) {
                voltage_name : VDD2;
                ...
        }
        ...
      }
      ...
```

In this case, there is no voltage_map defined for voltage_name VDD2. To fix the problem, add the voltage_map attribute for VDD2 at the library level:

```
voltage_map(VDD, 1.08);
      voltage_map(VDD1, 1.1);
      voltage_map(VDD2, 1.2);
      voltage_map(VSS, 0);

        ...
      cell(sample) {
        pg_pin(VDD) {
                voltage_name : VDD2;
                ...
        }
        ...
      }
      ...
```

The following is an example message:

```
Warning: Line 23, There is no 'VDD2' voltage_map defined for 'VDD2'
 voltage_name. (LBDB-848w)
```

What Next

Add the missing voltage_map.

LBDB-849

(warning) The '%s' group is overwritten by the '%s' group on line %d.

Description

The same group has been defined multiple times and only the last one will be recoded in the library db.

Feedback

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: The 'dc_current' group is overwritten by the 'dc_current' group
 on line 120. (LBDB-849)
```

What Next

Check the dc_current groups for wrong information and fix.

LBDB-850

(warning) Missing %s value under section %s in map file.

Description

If data entered in map file is incomplete, this message will be printed out. In PG_TO_VOLTAGE_MAP section, there are four fields: cell, pg_pin, pg_type and voltage_name. If one or more fields are left blank, you will see missing data in this section. The same is true for other sections. In VOLTAGE_MAP, for multi-rail library you should specify voltage_map entry with voltage_value = 0. Invalid record will be ignored. In POWER_DOWN_FUNCTION_MAP, if power_down_function values are missing for some cell/pins, the default values !VDD1+!VDD2+...+VSS1+VSS2 will be used where VDDi and VSSi are pg_pins of the cell.

The following example shows an instance where this message occurs:

```
BEGIN PG_TO_VOLTAGE_MAP
cell            pg_pin          voltage_name    pg_type
ADDFHX1         VDD             VDD
ADDFHX1         VSS             VSS             primary_ground
END PG_TO_VOLTAGE_MAP
```

The following is an example message:

```
Warning: Line 14, Missing pg_type value under section PG_TO_VOLTAGE_MAP
 in map file. (LBDB-850)
Warning: Line 20, Missing voltage value under section VOLTAGE_MAP in map
 file. (LBDB-850)
```

What Next

You should enter values for each field in the map file. Do not leave blank in any field except optional direction field in PG_TO_VOLTAGE_MAP section.

LBDB-851

(error) %s section %s in map file.

Feedback

Description

If the whole map section is missing (neither in map file nor derivable) or no pg_pins are available, this message will be printed out. For single-rail library, only PG_TO_VOLTAGE_MAP is required if no Milkyway library. If there is complete Milkyway library to cover all the cells in the input db, no map file is required. In this case, VOLTAGE_MAP will be derived from the input db that includes one voltage_map for nominal voltage and the other one for ground (voltage value = 0). For multi-rail library, PG_PIN_MAP, PG_TO_VOLTAGE_MAP, VOLTAGE_MAP and POWER_DOWN_FUNCTION_MAP sections are all required. If there are rail_connection's, PG_PIN_MAP is required in any case. Please note that invalid entries in the map section are ignored and removed. So even though these entries exist in the map section, the final map table may not include such entries. If pg_pins defined in FRAM have the same name pins in db as signal pins and these pins are unable to be converted to pg_pins due to complexity of these pins such as having timing, noise or power groups, most likely analog pins, they will stay as signal pins in db and no pg_pins of the same names are added.

The following example shows an instance where this message occurs:

```
BEGIN PG_TO_VOLTAGE_MAP
cell    pg_pin  voltage_name    pg_type
*       VDD     VDD             primary_power
*       VSS     VSS             primary_ground
*       VSS1    VSS1            backup_ground
END PG_TO_VOLTAGE_MAP
BEGIN POWER_DOWN_FUNCTION_MAP
cell    pin     power_down_function
test    test    VSS
*       *       !VDD+VSS+VSS1
END POWER_DOWN_FUNCTION_MAP
```

The following is an example message:

```
Error: Missing section PG_PIN_MAP in map file. (LBDB-851)
Error: Missing section VOLTAGE_MAP in map file. (LBDB-851)
```

What Next

Enter the missing section. For multi-rail library, specify all the four map sections with complete data. You can use "*" in cell and/or pin fields for all the others that are not listed in the map section. For single-rail library, specify at least PG_TO_VOLTAGE_MAP section with complete pg_pin, voltage_name and pg_type for each cell. Otherwise, check if those complex pins are analog pins or pg_pins. If pg_pins, remove the defined groups or attributes that make the pins complex so that they can be converted to pg_pins.

Feedback

LBDB-852

(error) %s found in %s is missing in %s.

Description

This message occurs during cross checking of map sections. (1) PG_PIN_MAP and PG_TO_VOLTAGE_MAP It is two-way checking. It is to check consistency of pg_pin associated with a cell between the two map sections. If a pg_pin for a cell exists in one map section but either the pg_pin or cell is missing in the other section, you will see this message. (2) PG_PIN_MAP and POWER_DOWN_FUNCTION_MAP It is to check signal pin consistency between the two sections. If a pin for a cell exists in POWER_DOWN_FUNCTION_MAP but is missing in PG_PIN_MAP, you will see this message. This checking is for multi-rail library. (3) PG_TO_VOLTAGE_MAP and VOLTAGE_MAP It is to check voltage_name consistency between the two sections. If the voltage_name for the nominal voltage is specified in VOLTAGE_MAP but is missing in PG_TO_VOLTAGE_MAP, you will see a message saying so. Please also refer to LBDB-854. In VOLTAGE_MAP, you can have more entries than necessary.

The following example shows an instance where this message occurs:

```
BEGIN PG_PIN_MAP
cell    pin rail_connection pg_pin
ADDFHX1 A       -   VSS
ADDFHX1 A       -   VDD
ADDFHX1 A       -   VDD1
END PG_PIN_MAP
BEGIN PG_TO_VOLTAGE_MAP
cell    pg_pin  voltage_name    pg_type
ADDFHX1 VDD     VDD primary_power
ADDFHX1 VSS     VSS primary_ground
END PG_TO_VOLTAGE_MAP
```

The following is an example message:

```
Error: Line 14, Cell 'test' pg_pin 'VDD1' found in PG_PIN_MAP is missing
 in PG_TO_VOLTAGE_MAP. (LBDB-852)
```

What Next

Check if the missing data (cell, pg_pin or pin) is what is required in the map section or extra data in the section where it exists. In the following example, if it is a multi-rail library and pg_pin VDD1 is what you should need in the library, you should list its entry in PG_TO_VOLTAGE_MAP, in the form of ADDFHX1 VDD1 VDD1 backup_power Otherwise, if it is a single-rail library, you should remove the entry for VDD1 from PG_PIN_MAP.

Feedback

LBDB-853

(warning) Voltage value %g for voltage_name '%s' is replaced by %g from input library.

Description

In add_pg_pin_to_db, it takes the data in the input db as higher priority. Therefore, if you defined a voltage_map in the map file while there is a different voltage value in the db for this voltage_name, the user defined value will be replaced by the value from the db, e.g. power_rail. The voltage value from the input db is taken in the following order: 1. If the library db has defined default_operating_conditions, then the specified voltage value in operating_condition will be used as the nominal voltage. 2. Otherwise, nom_voltage value defined at the library level will be used as the nominal voltage.

The following example shows an instance where this message occurs:

```
BEGIN VOLTAGE_MAP
voltage_name    voltage_value
VDD             1.1
VSS             0.0
END VOLTAGE_MAP
in default_operating_conditions,
   power_rail (VDD, 1.2)
```

The following is an example message:

```
Warning: Voltage value 1.1 for voltage_name 'VDD' is replaced by 1.2 from
 input library. (LBDB-853)
```

LBDB-854

(warning) voltage_name '%s' for nominal voltage not referenced in %s.

Description

This warning message occurs when you specify a voltage_map with the nominal voltage (or in the case of a single-rail or 1P1G library, a default voltage_map for the nominal voltage is automatically derived from the input db), but this voltage name is not referenced in the PG_TO_VOLTAGE_MAP table for add_pg_pin_to_db/lib or pg_pin group in .lib.

The following example shows an instance where this message occurs: The following is an example:

```
BEGIN PG_TO_VOLTAGE_MAP
cell    pg_pin  voltage_name   pg_type
test    VDD1    VDD1           primary_power
test    VSS     VSS            primary_ground
END PG_TO_VOLTAGE_MAP

BEGIN VOLTAGE_MAP
```

```
voltage_name    voltage_value
VDD             1.2
VDD1            1.08
VSS             0.0
END VOLTAGE_MAP
where 1.2 is nominal voltage.
```

The following is an example message:

```
Warning: voltage_map 'VCC' for nominal voltage not referenced in
 PG_TO_VOLTAGE_MAP. (LBDB-854)
Warning: voltage_name 'VCC' for nominal voltage not referenced in pg_pin
 group.  (LBDB-854)
```

What Next

Check if this nominal voltage and voltage name are correct. If so, add its mapping entry from pg_pin to voltage_map with the nominal voltage in PG_TO_VOLTAGE_MAP or reference the voltage_name in a pg_pin group in .lib. If you have not specified the correct voltage name for the nominal voltage in voltage_map, correct the voltage name. If you have not specified the voltage_map in the map file for the nominal voltage and it is derived by the utility, specify the voltage map for the nominal voltage using the correct voltage name from PG_TO_VOLTAGE_MAP.

LBDB-855

(warning) Invalid %s found under section %s in map file.

Description

In the map file, if any of the following is incorrect, (1) pg_type (2) pg_pin direction (3) voltage value (4) wild card or - in wrong field (5) incorrect section name or keywords in title line (6) pin direction in POWER_DON_FUNCTION_MAP (7) duplicate data specified on the same cell/pin (8) incorrect rail_connection this message will occur.

Valid pg_type values include: primary_power primary_ground backup_power backup_ground internal_power internal_ground Valid pg_pin direction values include input output inout internal nwell pwell deepnwell deeppwell

Valid voltage values are non-negative floating point numbers. Valid pin directions in POWER_DOWN_FUNCTION_MAP are output or inout. Valid power_down_functions are double quoted strings or unquoted strings if no space within the strings and the strings must contain only the power and ground pin names. rail_connection value should be derived from input .lib/db for the cell. If no rail_connection, please enter -.

Wild cards "*" and "-" can only be entered in some specific fields: (1) PG_PIN_MAP section "*" can be entered in cell and pin fields, and "-" can be entered in pin and rail_connection fields. (2) POWER_DOWN_FUNCTION_MAP section "*" can be entered in cell and pin fields. (3) PG_TO_VOLTAGE_MAP section "*" can be entered in cell

field only, and "-" can be entered in optional direction field. (4) VOLTAGE_MAP section No "*" or "-" can be entered in any field in this section. Caret "^" cannot be entered in the first entry of each map section. In checking title lines, the key words and their order should be exactly the same as mentioned in the spec. If an invalid value is entered or the value is entered in the wrong field in the map file, the whole record will be ignored for all fields except optional field in which only optional value is ignored. For example, if the pg_pin direction value is invalid, only the invalid value in this field is ignored. However, if the value is invalid in other fields, the whole line of record wil be ignored. (5) POWER_MANAGEMENT_ATTRIBUTE_MAP section If you specify duplicate entries on the same cell/pin/attribute, the last one will be ignored. For example, if you specify retention_2 sv retention_pin (save, "1") retention_2 sv retention_pin (restore, "0") you will receive this message and the second entry will be ignored. If you want to specify pin SAVE as both save and restore, specify it in this way, retention_2 sv retention_pin (save_restore, "0")

The following example shows an instance where this message occurs:

```
BEGIN PG_TO_VOLTAGE_MAP
cell            pg_pin          voltage_name    pg_type
ADDFHX1         VDD             VDD             power
ADDFHX1         VSS             VSS             primary_ground
GEND PG_TO_VOLTAGE_MAP
```

The following is an example message:

```
Warning: Line 14, Invalid pg_type found under section PG_TO_VOLTAGE_MAP
 in map file. (LBDB-855)
Warning: Line 20, Invalid wild card found under section PG_PIN_MAP in map
 file. (LBDB-855)
```

What Next

You should correct the invalid values in the map file. For example, in pg_type field, if you enter power, you will receive this message. The correct pg_type should be primary_power.

LBDB-856

(error) For pin(%s) of cell(%s), the %s entry for %s of pin(%s) cannot be found.

Description

This message indicates that you do not specify the relative_power_pin/related_ground_pin of the signal pin in the PG_PIN_MAP section of the map file used by add_pg_pin_to_db command.

Feedback

The following example shows an instance where this message occurs:

The following is an example message:

```
Error: For pin(A) of cell(sample), the pg_pin_map entry for
 related_power_pin of pin(A) cannot be found. (LBDB-856)
```

LBDB-857

(error) Missing %s under section %s.

Description

You will receive this Error if the following occurs: (1) VOLTAGE_MAP for multi-rail library if you do not specify voltage_map entry with voltage_value = 0 (2) POWER_MANAGEMENT_ATTRIBUTE_MAP if you do not specify a complete set of power management attributes in the map file, or the input .lib has partial power management attributes but you do not specify the ones that are missing in the library

The following example shows an instance where this message occurs:

```
BEGIN VOLTAGE_MAP
voltage_name    voltage_value
VDDlow      1.6
VDDhigh     2.0
VSS             0.1
END VOLTAGE_MAP
```

The following is an example message:

```
Error: Missing voltage value 0 under section VOLTAGE_MAP. (LBDB-857)
Error: Missing power_pin_class for cell 'retention' pin 'sv' under
 section POWER_MANAGEMENT_ATTRIBUTE_MAP. (LBDB-857)
```

What Next

You should enter values for each field in the map file. Do not leave blank in any field except optional direction field in PG_TO_VOLTAGE_MAP section. In VOLTAGE_MAP, for multi-rail library you should specify voltage_map entry with voltage_value = 0. In POWER_MANAGEMENT_ATTRIBUTE_MAP, specify the missing power attributes. In converting power_gating_pin, it uses power_pin_class and map_to_logic attributes in DB, and change power_pin_class = 6, 7, 8 to pin class "save", "restore" and "save_restore", respectively, and take the value of map_to_logic as <disable_value>. If the input .lib does not have power_pin_class = 6, 7 or 8, you should specify retention_pin_class as in the example RET_1 sv retention_pin (save, "0")

LBDB-858

(error) The timing arc %s->%s with when condition "%s" doesn't have ccs noise model.

Feedback

Description

For every timing arc, there must be one of the followings: (1) arc-based ccs noise models with the same "when" condition as the "when" of the timing arc, (2) pin-based ccs noise models with the same "when" condition as the "when" of the timing arc, or (3) pin-based ccs noise models with default (i.e., no "when") "when" condition.

For example,

```
pin(CO) {
  timing() {
    when : "!B&A";
    ...
    ccsn_first_stage() {
      /* no when condition */
      ...
    } /* qualified model 1 */
  }

  ccsn_last_stage() {
    when : "!B&A";
    ...
  } /* qualified model 2 */

  ccsn_last_stage() {
    /* no when condition */
    ...
  } /* qualified model 3 */

  ...
}
```

when condition "default" means that this timing arc has no "when" attribute.

The following is an example message:

```
Error: The timing arc CI->CO with when condition "!B&A" doesn't have ccs
 noise model. (LBDB-858)
```

What Next

Add ccs noise model with the qualified "when" condition.

LBDB-859

(error) There is no cross point in this %s group with input_net_transition %s.

Description

For expanded ccs power, if *pg_current* is represented as a sparse cross table, if there is no *input_net_transition*, then there must be one and only one cross point in one of the

vectors. if *input_net_transition* is specified, then one and only one cross point is required for each *input_net_transition*.

For compact ccs power, if *pg_current* is represented as a sparse cross table, then the typical capacitance of the pin specified in "index_output" must be one of the values in index with variable "total_output_net_capacitance".

The following example shows an instance where this message occurs:

```
dynamic_current() {
    ...
    related_outputs : "Q QN QN1 QN2";
    typical_capacitances(10.0, 12.0, 14.0, 16.0);
    switching_group() {
      ...
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "QN1";
          index_1 ("0.01");
          index_2 ("14.0"); /* cross point */
          ...
        }
        vector(CCS_power_1) {
          index_output : "QN2";
          index_1 ("0.02");
          index_2 ("11.0"); /* non cross point */
          ...
        }
      }
      ...
    }
  }
```

In this case, pg_current has only two vectors. There is no cross point with input_net_transition 0.02. So error message LBDB-859 will be issued.

The following is an example message:

```
Error: There is no cross point in this pg_current group with
 input_net_transition 0.02. (LBDB-859)
```

What Next

Add cross point for each input_net_transition.

LBDB-860

(warning) This cross point vector is inconsistent with a previous one with the same input_net_transition on Line %d.

Feedback

Description

If two cross point *vector* groups have the same *index* value of *input_net_transition*, then waveform of the I-t curve and *reference_time* must be the same for both vectors.

Two I-t curve waveforms are "equal" means,

Step1. Use the 1st waveform as a reference. For each time point in the reference waveform, get the current from the 2nd waveform. (may involve linear interpolation).

Step2. Take the sum of absolute difference on currents for each time point at the reference waveform. Assume total num of points in the reference waveform is N.

Step3. Calculate relative waveform difference as Sum_of_difference_on_current / (peak_from_reference * N), which should <= 2%.

Step4. Calculate relative peak difference as ABS (peak_from_2nd - peak_from_reference) / peak_from_reference, which should <= 2%.

The following example shows an instance where this message occurs:

```
dynamic_current() {
    ...
    related_outputs : "Q QN";
    typical_capacitances(10.0, 12.0);
    switching_group() {
      ...
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "Q";
          reference_time : 0.01;
          index_1 ("0.02"); /* input_net_transition */
          index_2 ("10.0"); /* total_output_net_capacitance */
          index_3 ("0.000, 0.0873, 0.135, 0.764"); /* time */
          values ("0.002, 0.009, 0.134, 0.546");
        }
        vector(CCS_power_1) {
          index_output : "QN";
          reference_time : 0.04;
          index_1 ("0.02"); /* input_net_transition */
          index_2 ("12.0"); /* total_output_net_capacitance */
          index_3 ("0.000, 0.0873, 0.135, 0.764"); /* time */
          values ("0.002, 0.009, 0.134, 0.546");
        }
      }
      ...
    }
  }
```

In this case, pg_current is a sparse cross table, two vectors are represented as cross points, and both have the same input_net_transition 0.02. In such a case, I-t curve

Feedback

waveform and reference_time (0.01 and 0.04, not identical. Issue a warning.) must be the same.

The following is an example message:

```
Warning: This cross point vector is inconsistent with a previous one with
 the same input_net_transition on line 57191. (LBDB-860)
```

What Next

Correct one of the cross points to make them consistent.

LBDB-861

(error) This vector is repeated with a previous one under the same pg_current group.

Description

Under the same *pg_current* group, no two vectors can have the same *index_output* and values of all *index* attributes except for the last *index* (time). Otherwise, this vector will be regarded as repeated.

The following example shows an instance where this message occurs:

```
pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "QN1";
          reference_time : 0.01;
          index_1 ("0.01"); /* input_net_transition */
          index_2 ("14.0"); /* total_output_net_capacitance */
          index_3 ("0.001, 0.003, 0.006"); /* time */
          ...
        }
        vector(CCS_power_1) {
          index_output : "QN1";
          reference_time : 0.01;
          index_1 ("0.01"); /* input_net_transition */
          index_2 ("14.0"); /* total_output_net_capacitance */
          index_3 ("0.004, 0.007, 0.009"); /* time */
          ...
        }
      }
```

In this case, index_output (QN1), input_net_transition (0.01), and total_output_net_capacitance(14.0) are all the same between two vectors. So error message LBDB-861 will be issued.

The following is an example message:

```
Error: This vector is repeated with a previous one under the same
 pg_current group. (LBDB-861)
```

Feedback

What Next

Correct one of the vectors to make them different.

LBDB-862

(error) The dense table under the pg_current group is incomplete with input_net_transition %s.

Description

If a <template> with two *total_output_net_capacitance* variables is applied to all vectors under a *pg_current* group, then all possible combination of capacitances between two output pins must be specified if all of them have the same *input_net_transition*.

The following example shows an instance where this message occurs:

```
pg_current(VDD) {
        vector(CCS_power_dense) {
          reference_time : 0.01;
          index_1 ("0.01"); /* input_net_transition */
          index_2 ("1.0"); /* total_output_net_capacitance */
          index_3 ("2.0"); /* total_output_net_capacitance */
          index_4 ("0.000, 0.0873, 0.135, 0.764"); /* time */
          values ("0.002, 0.009, 0.134, 0.546");
        }
        vector(CCS_power_dense) {
          reference_time : 0.01;
          index_1 ("0.01"); /* input_net_transition */
          index_2 ("1.5"); /* total_output_net_capacitance */
          index_3 ("2.5"); /* total_output_net_capacitance */
          index_4 ("0.100, 0.0873, 0.135, 0.764"); /* time */
          values ("0.113, 0.110, 0.243, 0.657");
        }
        vector(CCS_power_dense) {
          reference_time : 0.01;
          index_1 ("0.01"); /* input_net_transition */
          index_2 ("1.5"); /* total_output_net_capacitance */
          index_3 ("2.0"); /* total_output_net_capacitance */
          index_4 ("0.000, 0.0873, 0.135, 0.764"); /* time */
          values ("0.224, 0.221, 0.358, 0.769");
        }
      }
```

In this case, all possible combinations of (c1, c2) with input_net_transition 0.01 are (1.0, 2.0), (1.5, 2.5), (1.0, 2.5) and (1.5, 2.0). But (1.0, 2.5) is missing. So error message LBDB-862 will be issued.

Feedback

The following is an example message:

```
Error: The dense table under the pg_current group is incomplete with
 input_net_transition 0.01. (LBDB-862)
```

What Next

Add vectors to make the dense table complete.

LBDB-863

(error) Size or values of total_output_net_capacitance are not identical for output pin %s.

Description

The size and values of *total_output_net_capacitance* for the same output pin or *index_output* (cross type) shall be identical for all vectors which have different *input_net_transition* index values.

In other words, every fixed (without tolerance) input_net_transition needs the same set of total_output_net_capacitance.

In the message, "output pin" means index_output (cross type) or all pins in "related_outputs" (dense type and diagonal type).

The following example shows an instance where this message occurs:

```
dynamic_current() {
    ...
    related_outputs : "Q QN";
    typical_capacitances(10.0, 12.0);
    switching_group() {
      ...
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "Q";
          reference_time : 0.01;
          index_1 ("0.01"); /* input_net_transition */
          index_2 ("5.0"); /* total_output_net_capacitance */
          ...
        }
        vector(CCS_power_1) {
          index_output : "Q";
          reference_time : 0.01;
          index_1 ("0.01"); /* input_net_transition */
          index_2 ("10.0"); /* total_output_net_capacitance */
          ...
        }
        vector(CCS_power_1) {
          index_output : "Q";
          reference_time : 0.01;
          index_1 ("0.01"); /* input_net_transition */
```

Feedback

```
    index_2 ("15.0"); /* total_output_net_capacitance */
    ...
  }
  vector(CCS_power_1) {
    index_output : "QN";
    reference_time : 0.01;
    index_1 ("0.01"); /* input_net_transition */
    index_2 ("6.0"); /* total_output_net_capacitance */
    ...
  }
  vector(CCS_power_1) {
    index_output : "QN";
    reference_time : 0.01;
    index_1 ("0.01"); /* input_net_transition */
    index_2 ("12.0"); /* total_output_net_capacitance */
    ...
  }
  vector(CCS_power_1) {
    index_output : "QN";
    reference_time : 0.01;
    index_1 ("0.01"); /* input_net_transition */
    index_2 ("18.0"); /* total_output_net_capacitance */
    ...
  }
  vector(CCS_power_1) {
    index_output : "Q";
    reference_time : 0.01;
    index_1 ("0.02"); /* input_net_transition */
    index_2 ("5.0"); /* total_output_net_capacitance */
    ...
  }
  vector(CCS_power_1) {
    index_output : "Q";
    reference_time : 0.01;
    index_1 ("0.02"); /* input_net_transition */
    index_2 ("11.0"); /* total_output_net_capacitance */
    ...
  }
  vector(CCS_power_1) {
    index_output : "Q";
    reference_time : 0.01;
    index_1 ("0.02"); /* input_net_transition */
    index_2 ("15.0"); /* total_output_net_capacitance */
    ...
  }
  vector(CCS_power_1) {
    index_output : "QN";
    reference_time : 0.01;
    index_1 ("0.02"); /* input_net_transition */
    index_2 ("6.0"); /* total_output_net_capacitance */
    ...
  }
  vector(CCS_power_1) {
```

Feedback

```
          index_output : "QN";
          reference_time : 0.01;
          index_1 ("0.02"); /* input_net_transition */
          index_2 ("12.0"); /* total_output_net_capacitance */
          ...
        }
        vector(CCS_power_1) {
          index_output : "QN";
          reference_time : 0.01;
          index_1 ("0.02"); /* input_net_transition */
          index_2 ("18.0"); /* total_output_net_capacitance */
          ...
        }
        vector(CCS_power_1) {
          index_output : "QN";
          reference_time : 0.01;
          index_1 ("0.02"); /* input_net_transition */
          index_2 ("24.0"); /* total_output_net_capacitance */
          ...
        }
      }
      ...
    }
  }
```

When input_net_transition is 0.01 and output pin is Q, total_output_net_capacitance size=3, values = (5.0, 10.0, 15.0). /*group1*/ When input_net_transition is 0.01 and output pin is QN, total_output_net_capacitance size=3, values = (6.0, 12.0, 18.0). /*group2*/ When input_net_transition is 0.02 and output pin is Q, total_output_net_capacitance size=3, values = (5.0, 11.0, 15.0). /*group3*/ When input_net_transition is 0.02 and output pin is QN, total_output_net_capacitance size=4, values = (6.0, 12.0, 18.0, 24.0). /*group4*/ group1 and group3 have different values. group2 and group4 have different sizes. So error message LBDB-863 will be issued.

The following is an example message:

```
Error: Size or values of total_output_net_capacitance are not identical
 for output pin Q. (LBDB-863)
Error: Size or values of total_output_net_capacitance are not identical
 for output pin QN. (LBDB-863)
```

What Next

Change the size or values of total_output_net_capacitance with a input_net_transition value to make the size and values consistent.

LBDB-864

(error) The design '%s' has separate intrinsic_parasitic groups.

Feedback

Description

This error occurs when there are two intrinsic_parasitic groups in the same cell, where the only difference is that one group has only intrinsic_resistance, and the other group has only intrinsic_capacitance.

However, it is allowed that only intrinsic_resistance or intrinsic_capacitance is defined for the intrinsic_parasitic group.

The following example shows an instance where this message occurs:

```
cell (AND3) {
  ...
  intrinsic_parasitic() {
    /* default state */
    intrinsic_resistance(G1) {
       related_output : "ZN";
       value : 9.0;
    }
  }

  intrinsic_parasitic() {
    /* default state */
    intrinsic_capacitance(G2) {
       value : 8.2;
    }
  }
}
```

In this case, cell 'AND3' has both an intrinsic_parasitic group with only intrinsic_resistance and an intrinsic_parasitic group with only intrinsic_capacitance. So error message LBDB-864 will be issued.

The following is an example message:

```
Error: The design 'AND3' has separate intrinsic_parasitic groups.
 (LBDB-864)
```

What Next

Combine the separate intrinsic_parasitic groups into one group.

LBDB-868

(warning) The estimated time when output signal reaches\n \tVDD level is out of range [%g, %g].

Feedback

Description

The time when output signal reaches VDD level is estimated as T = reference time + NLDM delay Reference time means the time when input signal reaches VDD level. T has to be within the range of the current waveform (min and max of time in current waveform).

The way to evaluate NLDM delay is to lookup the cell_rise/cell_fall table in the corresponding timing arc with the given input_net_transition and total_output_net_capacitance in the vector.

If the given input_net_transition and total_output_net_capacitance can not be found in the cell_rise/cell_fall table, use the nearest index to get the delay value.

The following example shows an instance where this message occurs:

```
lu_table_template (table_dodelaycell_rise_0k0aa01m1) {
  variable_1 : total_output_net_capacitance
  variable_2 : input_net_transition
  index_1 (" 0.006404, 0.055194, 0.147118 ");
  index_2 (" 0.060000, 0.400000, 0.800000 ");
}
pg_current_template(t1) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
  variable_3 : time;
  index_1("0.6 0.9");
  index_2("0.6 0.9");
  index_3("0.3 4.7");
}

cell (AND3) {
  dynamic_current() {
    ...
    related_inputs : "A2 A3";
    related_outputs : "ZN ZN1";
    typical_capacitances(0.3 0.4);
    switching_group() {
      ...
      pg_current(V2) {
        vector(t1) {
          reference_time : 15.6;
          index_output : "ZN1";
          index_1("0.5");
          index_2("0.043");
          index_3("18.2 18.3 19.0");
          values("13.78 192.4 1100.1");
        }
      }
    }
  }

  pin(ZN1) {
```

```
    ...
    timing() {
      related_pin : "A1 A2"
      cell_rise( scalar ) {
        values("0.28"); }
      cell_fall( scalar ) {
        values("0.0"); }
      ...
    }
    timing() {
      related_pin : "A3"
      cell_rise ("table_dodelaycell_rise_0k0aa01m1") {
      values (\
        "0.1729, 0.2200, 0.2397 ",\
        "0.3494, 0.4012, 0.4273 ",\
        "0.6499, 0.7018, 0.7281 "\
      );
    }
    cell_fall( scalar ) {
      values("0.0"); }
    }
  }
}
```

In this case, the information on the given current waveform is, (1) the time range is [18.2, 19.0]; (2) reference time is 15.6; (3) input pins are "A2 A3", output pin is ZN1; (4) input_net_transition is 0.5; (5) total_output_net_capacitance is 0.043.

In the section of pin(ZN1), (1) the first timing arc is specified with input pin "A1 A2", overlaped with "A2 A3" in the current waveform. So the delay is needed. delay1 = MAX(0.28, 0.0) = 0.28.

(2) the second timing arc is specified with input pin "A3", overlaped with "A2 A3" in the current waveform. So the delay is needed.

Look up cell_rise table with (input_net_transition=0.5, total_output_net_capacitance=0.043). The nearest index is values[1][1] = 0.4012. delay2 = MAX(0.4012, 0.0) = 0.4012.

max_delay = MAX(delay1, delay2) = 0.4012.

reference_time + max_delay = 15.6+0.4012 = 16.0012. It isn't within the range [18.2, 19.0]. So warning message LBDB-868 will be issued.

The following is an example message:

```
Warning: The estimated time when output signal reaches VDD level is out
 of range [18.2, 19.0]. (LBDB-868)
```

What Next

Extend current waveform, or change reference time and delay.

Feedback

LBDB-869

(information) Failure rate of the library cells will be overwritten.

Description

Failure rate is a Design-For-Yield concept, it is a integer number, value from 0 ~ 1e9, means the number of failures per billion.

In Liberty syntax, there are two models can describe the cell yield, under the same cell level group, functional_yield_metric().

```
cell (my_cell) {
  ...
  functional_yield_metric() {
    /* 1st method */
    average_number_of_faults(<template>) {
      values("float...float");
    }
    /* 2nd method */
    critical_area_table(<template>) {
      defect_type:enum(short, open, short_and_open);
      related_layer:<layer_name>;
      index_1("float...float"); /*particle diameter array*/
      values("float...float"); /*critical area values */
    }
  }
  ...
}
```

Using the 1st method can defined the average failure rate and derive a cell failure rate directly by Library Compiler.

The 2nd method, besides the critical area table in .lib, user need particle distribution function file, using command calculate_caa_based_yield2db to calculate out the failure rate.

This message is reported when the command calculate_caa_based_yield2db is called to calculate the CAA based yield (failure rate), while the failure rate attribute is already exist in the library(db file), regardless the failure rate is calculated by 1st or 2nd method before.

The following is an example message:

```
Information: Failure rate of the library cells will be overwritten.
 (LBDB-869)
```

What Next

This is just an information to update the status, you can just ignore it.

Feedback

LBDB-870

(information) Redundant cross point vector with input_net_transition %s is removed.

Description

If there are more than one cross point vectors with the same input_net_transition under a pg_current group, read_lib will only keep the first one. Others will be removed.

The following example shows an instance where this message occurs:

```
dynamic_current() {
    ...
    related_outputs : "Q QN QN1 QN2";
    typical_capacitances(10.0, 12.0, 14.0, 16.0);
    switching_group() {
      ...
      pg_current(VDD) {
        vector(CCS_power_1) {
          index_output : "QN1";
          index_1 ("0.01");
          index_2 ("14.0"); /* cross point */
          ...
        }
        vector(CCS_power_1) {
          index_output : "QN2";
          index_1 ("0.01");
          index_2 ("16.0"); /* cross point */
          ...
        }
      }
      ...
    }
  }
```

In this case, there are two cross points with input_net_transition 0.01. So the second one will be removed.

The following is an example message:

```
Info: Redundant cross point vectors with input_net_transition 0.01 are
 removed. (LBDB-870)
```

What Next

It's just an information. Change in .lib is not required. However, in order to remove this message, keep only one cross point vector with the specified input_net_transition.

Feedback

LBDB-871

(error) The difference between the first point \n \t current value(%f) and the peak current value (%f) is less than 0.001%%.

Description

This error is issued when init current value is numerically identical to the peak current in CCS Timing or Compact CCS Timing data. The tolerance is set to 0.001%, that is: if fabs((I(first_point) - I(peak_point))/I(peak_point)) < 0.001%,

This could potentially cause larger errors in the calculation if data is truncated during reading, when these two values are too close.

The following example shows an instance where this message occurs:

```
output_current_rise() {
        vector(ccs) {
        reference_time : 1.493117e+00;
        index_1(2.986235e+00);
        index_2(2.500000e+01);
        index_3("8.216709e+00, 8.391117e+00, 1.775112e+01, 3.249112e+01,
 4.366012e+01, 6.033512e+01, 7.932612e+01, 9.818012e+01, 1.184101e+02,
 1.420501e+02, 1.728901e+02, 1.851275e+02");
        values( "4.299772e-01, 4.299781e-01, 4.117592e-01, 3.890655e-01,
 3.539464e-01, 2.690953e-01, 1.685153e-01, 9.581405e-02, 4.934546e-02,
 2.188565e-02, 7.340714e-03, 5.989923e-03");
        }
      }
```

The following is an example message:

```
Error: Line 3383, The first point current value(0.429977) is almost
        the same as peak point current value(0.429978). (LBDB-871)
```

What Next

Check the library source file and correct the data, most likely, you may need to re-characterize the library cells for CCS timing data.

LBDB-872

(warning) Curve parameters in %s are not exact for compact CCS power.

Feedback

Description

This warning message occurs when the curve parameters are not exact for compact CCS power. If a compact_lut_template is for compact CCS power, the value of the curve_parameters index (the last index) must be the following:

```
init_time, init_current, bc_id1, point_time1, point_current1, bc_id2,
[point_time2, point_current2, bc_id3, ...], end_time, end_current
```

This is a pattern instead of a specified series because the compact CCS power table varies in size.

The following example shows an instance where this message occurs: The following example results in this warning message:

```
compact_lut_template(t1) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
    index_1 : ("...");
    index_2 : ("...");
    index_3 : ("init_time, init_current, bc_id1");
  }
```

The values in index_3 are not exact for compact CCS power.

What Next

This is only a warning message. No action is required.

However, to avoid this warning message you can change the values in the curve_parameters index and run the command again.

See Also

- LBDB-873
- LBDB-876
- LBDB-877

LBDB-873

(error) Invalid size of data for I-t curve #%d in "values".

Description

In compact ccs power, an I-t curve is always described with the pattern init_time, init_current, bc_id1, point_time1, point_current1, bc_id2, [point_time2, point_current2, bc_id3, ...], end_time, end_current

Feedback

So the size of data within a pair of quotation (e.g., data for an I-t curve) should be able to reprented as 8+3i (i>=0).

"I-t curve #?" means the order of this curve in "values". For example, "I-t curve #2" means the 2nd curve in "values".

The following example shows an instance where this message occurs:

```
compact_ccs_power(t1) {
    ...
    values("0.0, 1, 0.32, 1.08, 2, 0.87, -0.33, 3, 1.03, 0.0, 4, 1.50,
 0.67", /* size = 13 */\
           "0.0, 0.0, 1, 0.28, 0.93, 2, 0.45, 0.28", /* size = 8 */\
           "0.0, 0.0, 1, 0.36, 1.05, 2, 0.52, -0.49, 3, 0.88, 0.22",/*
 size = 11 */\
           "0.0, 0.0, 1, 0.33, 1.31, 2, 0.61, -0.83, 3, 0.96, 0.66" /*
 size = 11 */);
  }
```

In this example, size of the first line in "values" is 13, which is invalid. Sizes of other lines are valid.

The following is an example message:

```
Error: Line 388, Invalid size of data for I-t curve #1 in "values".
 (LBDB-873)
```

What Next

Change size and data in "values".

LBDB-874

(error) Time values in I-t curve #%d in "values" should be monotonically increasing.

Description

In compact ccs power, an I-t curve is always described with the pattern init_time, init_current, bc_id1, point_time1, point_current1, bc_id2, [point_time2, point_current2, bc_id3, ...], end_time, end_current

Time values with corresponding parameter "init_time", "point_time*" and "end_time" in an I-t curve should be monotonically increasing.

"I-t curve #?" means the order of this curve in "values". For example, "I-t curve #2" means the 2nd curve in "values".

The following example shows an instance where this message occurs:

```
compact_ccs_power(t1) {
    ...
```

```
    values("0.0, 0.0, 1, 1.32, 1.08, 2, 0.87, -0.33, 3, 1.03, 0.0, 4,
 1.50, 0.67", ...
  }
```

In this example, time-related data are {0.0, 1.32, 0.87, 1.03, 1.50}, which are not monotonically increasing.

The following is an example message:

```
Error: Line 388, Time values for I-t curve #1 in "values" should be
 monotonically increasing. (LBDB-874)
```

What Next

Change values of time-related data in "values".

LBDB-875

(warning) %s value %f in I-t curve #%d is too small and may be reset 0.

Description

In a I-t curve, all time values with corresponding parameter "init_time", "point_time*" and "end_time" can't be too diverse. Otherwise, small values will be reset 0. Similarly, all current values with corresponding parameter "init_current", "point_current*" and "end_current" can'be too diverse, either. "I-t curve #?" means the order of this curve in "values". For example, "I-t curve #2" means the 2nd curve in "values".

The following example shows an instance where this message occurs:

```
compact_ccs_power(t1) {
    ...
    values("0.0, 0.0, 1, 1.32, 1.08, 2, 0.87, -0.33, 3, 1.03, 0.0, 4,
 1e+100, 0.67", ...
  }
```

In this example, "end_time" is 1e+100, which will make other non-zero time values 1.32, 0.87 and 1.03 reset 0.

The following is an example message:

```
Warning: Line 388, Time value 1.32 in I-t curve 1 is too small and may be
 reset 0. (LBDB-875)
```

What Next

Change time or current values.

Feedback

LBDB-876

(error) Variables are specified behind indexes in compact_lut_template.

Description

compact_lut_template requires variables are specified before indexes. Other templates don't have this requirement.

The following example shows an instance where this message occurs:

```
compact_lut_template (t1) {
    index_1 ("0, 1");
    index_2 ("0, 1");
    index_3 ("init_time, init_current, bc_id1, point_time1,
 point_current1,
              bc_id2, [point_time2, point_current2, bc_id3, ...],
              end_time, end_current");
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : curve_parameters;
  }
```

The following is an example message:

```
Error: Line 388, Variables are specified behind indexes in
 compact_lut_template. (LBDB-876)
```

What Next

Put all variables in front of indexes.

LBDB-877

(error) Variables in compact_lut_template are invalid.

Description

Variables in compact_lut_template must satisfy, (1) The last variable is "curve_parameters"; (2) The variables before the last one are "input_net_transition" and "total_output_net_capacitance".

If this template is applied in compact ccs timing or va compact ccs timing, (3) There should be exactly one "input_net_transition" and one "total_output_net_capacitance".

If this template is applied in compact ccs power, (3) There should be at most one "input_net_transition" and at most two "total_output_net_capacitance".

Feedback

The following example shows an instance where this message occurs:

```
compact_lut_template(t1) {
    variable_1 : input_net_transition;
    variable_2 : curve_parameters;
    variable_3 : total_output_net_capacitance;
  }
```

To fix the problem, exchange the values between variable_2 and variable_3.

The following is an example message:

```
Error: Line 388, Variables in compact_lut_template are invalid.
 (LBDB-877)
```

What Next

Make necessary change in variable and index.

LBDB-878

(error) One point current value(%f) is almost\n \tthe same as the adjacent point current value(%f).

Description

This error is issued when current value in one point is numerically identical to that in the adjacent point in Compact CCS Power data. The tolerance is set to 0.001%, that is: if fabs((I(first_point) - I(second_point))/I(second_point)) < 0.001%,

This could potentially cause larger errors in the calculation if data is truncated during reading, when these two values are too close.

The following example shows an instance where this message occurs:

```
compact_ccs_power(t1) {
    ...
    values("0.0, 0.0, 1, 0.28, 0.93, 2, 0.45, 0.929999", ...
  }
```

The following is an example message:

```
Error: Line 388, One point current value(0.93) is almost the same as the
 adjacent point current value(0.929999). (LBDB-878)
```

What Next

Check the library source file and correct the data, most likely, you may need to re-characterize the library cells for CCS power data.

Feedback

LBDB-879

(error) Pin '%s' can't be a pll %s pin.

Description

This message is issued because pin direction doesn't match the required direction of pll reference/feedback/output pin. If a pin is set "is_pll_reference_pin" or "is_pll_feedback_pin" true, it should be an input pin. If a pin is set "is_pll_output_pin" true, it should be an output pin.

The following example shows an instance where this message occurs:

```
cell (AND2) {
  is_pll_cell : true;
  pin (A1) {
    direction : input;
    is_pll_output_pin : true;
  }
  ...
}
```

The following is an example message:

```
Error: Pin 'A1' can't be a pll output pin. (LBDB-879)
```

What Next

Specify the attribute "is_pll_reference_pin", "is_pll_feedback_pin" or "is_pll_output_pin" under another pin with consistent direction.

LBDB-880

(error) More than one exclusive pll pin attributes are specified in pin '%s'.

Description

In a cell, pll reference pin, pll feedback pin and pll output pin must be different pins. Therefore in a pin group, at most one of the three attributes "is_pll_reference_pin", "is_pll_feedback_pin" and "is_pll_output_pin" can be set true.

The following example shows an instance where this message occurs:

```
cell (AND2) {
  is_pll_cell : true;
  pin (ZN1) {
    direction : input;
    is_pll_reference_pin : true;
    is_pll_feedback_pin : true;
  }
```

```
  ...
}
```

The following is an example message:

```
Error: More than one exclusive pll pin attributes are specified in pin
 'ZN1'. (LBDB-880)
```

What Next

Move all pll pin specifications except one to other pins.

LBDB-881

(error) Pll cell '%s' has wrong pll %s pin defined.

Description

If a cell is specified as a pll cell, then the cell group should contain one and only one pll reference pin, one and only one pll feedback pin, and one or more pll output pins.

The following example shows an instance where this message occurs:

```
cell (AND2) {
  is_pll_cell : true;
  pin (ZN1) {
    direction : input;
    is_pll_reference_pin : true;
  }
}
```

The following is an example message:

```
Error: Pll cell 'AND2' has wrong pll feedback pin defined. (LBDB-881)
Error: Pll cell 'AND2' has wrong pll output pin defined. (LBDB-881)
```

What Next

Correct pins under the pll cell.

LBDB-882

(warning) Pll pin tags in non-pll cell '%s' will be ignored.

Description

If a cell is not set "is_pll_cell" true, then pin level attributes "is_pll_reference_pin", "is_pll_feedback_pin" and "is_pll_output_pin" will be ignored.

Feedback

The following example shows an instance where this message occurs:

```
cell (AND2) {
  pin (ZN1) {
    direction : input;
    is_pll_reference_pin : true;
  }
}
```

The following is an example message:

```
Warning: Pll pin tags in non-pll cell 'AND2' will be ignored. (LBDB-882)
```

What Next

Remove pll pin tags from the non-pll cell.

LBDB-883

(error) More than one physical only cell types are specified in design '%s'.

Description

In a pin group, at most one of the three attributes "is_decap_cell", "is_filler_cell" and "is_tap_cell" can be set true.

The following example shows an instance where this message occurs:

```
cell (S1CAP1) {
  is_filler_cell : true;
  is_decap_cell : true;
  ...
}
```

The following is an example message:

```
Error: More than one physical only cell types are specified in design
 'S1CAP1'. (LBDB-883)
```

What Next

Remove all physical only cell type specifications except one.

LBDB-884

(error) Physical only cell '%s' can't contain I/O pins.

Description

If one of the three attributes "is_decap_cell", "is_filler_cell" and "is_tap_cell" is set true, this cell is a physical only cell. It should contain pg-pin only and has no signal pins in it.

Feedback

The following example shows an instance where this message occurs:

```
cell (S1CAP1) {
  is_decap_cell : true;
  pin(A1) {
    ...
  }
  ...
}
```

The following is an example message:

```
Error: Physical only cell 'S1CAP1' can't contain I/O pins. (LBDB-884)
```

What Next

Remove I/O pins in this cell.

LBDB-885

(error) There is no bias pin named '%s' related to this\n \tsignal pin's related power or ground pin.

Description

This error message is reported when the association of power/ground pin and bias pin in signal is incorrect.

A signal pin's related bias pin must one of the related bias pins of this signal pin's related power/ground pin.

The following is an example message:

```
Error: Line 546, There is no bias pin named vpw related to this signal
 pin's
related power/ground pin.(LBDB-885)
```

What Next

Check if this related bias pin is related to this signal pin's power pin or ground pin.

LBDB-885w

(warning) There is no bias pin named '%s' related to this\n \tsignal pin's related power or ground pin.

Description

This warning message is reported when the association of power/ground pin and bias pin in signal is incorrect.

Feedback

A signal pin's related bias pin must one of the related bias pins of this signal pin's related power/ground pin.

The following is an example message:

```
Waring: Line 546, There is no bias pin named vpw related to this signal
 pin's
related power/ground pin.(LBDB-885w)
```

What Next

Check if this related bias pin is related to this signal pin's power pin or ground pin.

LBDB-886

(error) Bias pg_pin '%s' can not be properly associated to\n \tthe pg_pin.

Description

This error message is reported when bias pin %s can not be properly associated to a pg_pin.

Power type pg_ppin should be associated with a nwell type bias pg pin; ground type pg_pin should be associated with a pwell type bias pg pin.

The following example shows an instance where this message occurs:

```
pg_pin(PWR) {
    voltage_name : VDD;
    pg_type : primary_power;
    related_bias_pin : "vpw"
  }
  pg_pin(vpw) {
    voltage_name : VDDL;
    pg_type : pwell;
    bias_connection : routing_pin;
  }
```

The following is an example message:

```
Error: Line 546, Bias pg_pin vpw can not be properly associated to the
pg_pin.(LBDB-886)
```

What Next

Check the pg_type of the pg_pin to be assoicated and the pg_type of the bias pg_pin.

LBDB-887

(warning) Only one (P or N)well bias pin exists.

Feedback

Description

This message is indicates that only one bias pin with pg_type P or N well is exists. Generally, pwell and nwell bias pins should be exsit as a pair.

The following is an example message:

```
Warning: Line 546, Only one (P or N)well bias pin vpw exists.(LBDB-887)
```

What Next

Delete the odd bias pin or add a new bias pin to be couple with the odd one.

LBDB-888

(error) physical_connection is associated with an invalid pg_type.

Description

This error message occurs when the physical_connection is associated with an invalid pg_type. The pg_type of a bias PG pin must be one of the predefined bias types: pwell, nwell, deeppwell, or deepnwell.

The following is an example message:

```
Error: Line 546,  physical_connection is associated with an invalid
 pg_type.
(LBDB-888)
```

What Next

Make sure the pg_type of the bias PG pin is one of the valid types listed above.

LBDB-889

(error) The pg_type of bias pg pin '%s' to be related is invalid.

Description

This error message is reported when a bias pg pin is related to a pg_pin or a signal pin, its type_type is not one of the predefined bias types: pwell|nwell|deeppwell|deepnwell.

The following is an example message:

```
Error: Line 546, The pg_type of bias pg pin vpw to be related
is invalid.(LBDB-889)
```

What Next

Check the pg_type of the bias pg pin.

Feedback

LBDB-890

(warning) Isolation cell '%s' contains more than two input pins.

Description

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: Line 202, Isolation cell 'acell' contains more than two input
 pins. (LBDB-890)
```

What Next

Delete unwanted input pins to keep the input pin number is no less than 2.

LBDB-891

(error) Retention cell '%s' has no retention pin.

Description

This error message occurs because a retention cell (identified by the *retention_cell* or *power_gating_cell* attribute), must have at least one control pin (identified by the retention_pin or power_gating_pin function).

The following example shows the correct control pin in the retention cell:

```
cell(retention_dff) {
  ...
  retention_cell : "my_retention_dff" ;
  clock_gating_integrated_cell : "generic";

  pin(SAVE) {
    ...
    direction : input;
  retention_pin (save, "0") ;
  }

  pin(RESTORE) {
    ...
    direction : input;
  retention_pin (restore, "0") ;
  }
}
```

The following is an example message:

```
Error: Retention cell 'retention_dff' has no retention pin. (LBDB-891)
```

Feedback

What Next

Add retention pins to the given cell and run the command again.

LBDB-892

(error) Pin name '%s' is duplicated with pg pin name.

Description

Names of Signal pins should be different with pg pin names and vice-versa.

The following is an example message:

```
Error: Pin name 'VSS' is duplicated with pg pin name.(LBDB-892)
```

What Next

Change the duplicated signal pin name or pg pin name.

LBDB-894

(warning) No scaling is done in '%s' because nominal process can not be found.

Description

This message is issued because scaling feature is turned on and there is no nominal process defined in the library.

Nominal process is selected in this order of precedence:

(1) if "default_operating_conditions" is specified, nominal process is taken from attribute "process" in the default "operating_conditions" group; (2) nominal process is taken from library-level attribute "nom_process".

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: No scaling is done because nominal process can not be found.
 (LBDB-894)
```

What Next

Define nominal process in library to continue scaling.

LBDB-895

(warning) "values" in "%s" group won't be scaled because "%s" is not found.

Feedback

Description

This message is issued because scaling feature is turned on and there is no corresponding k-factor defined for the specified attribute.

Here is the mapping table of supported k-factors and db attributes.

Nominal process is selected in this order of precedence:

k-factor name db_attribute_name k_process_cell_rise timing -> cell_rise -> values k_process_cell_fall timing -> cell_fall -> values k_process_rise_propagation timing -> rise_propagation -> values k_process_fall_propagation timing -> fall_propagation -> values k_process_rise_transition timing -> rise_transition -> values k_process_fall_transition timing -> fall_transition -> values k_process_setup_rise timing -> rise_constraint ->values (when "timing_type" is "setup_rising" or "setup_falling") k_process_setup_fall timing -> fall_constraint ->values (when "timing_type" is "setup_rising" or "setup_falling") k_process_hold_rise timing -> rise_constraint ->values (when "timing_type" is "hold_rising" or "hold_falling") k_process_hold_fall timing -> fall_constraint ->values (when "timing_type" is "hold_rising" or "hold_falling") k_process_recovery_rise timing -> rise_constraint ->values (when "timing_type" is "recovery_rising" or "recovery_falling") k_process_recovery_fall timing -> fall_constraint ->values (when "timing_type" is "recovery_rising" or "recovery_falling") k_process_removal_rise timing -> rise_constraint ->values (when "timing_type" is "removal_rising" or "removal_falling") k_process_removal_fall timing -> fall_constraint ->values (when "timing_type" is "removal_rising" or "removal_falling")

The following example shows an instance where this message occurs:

The following is an example message:

```
Warning: "values" in "cell_rise" group won't be scaled because
 "k_process_cell_rise" is not found. (LBDB-895)
```

What Next

Add corresponding k-factor.

LBDB-896

(error) Invalid %s found under section %s in map file.

Description

This error message occurs if any the following are incorrect in the map file:

- `voltage_name`
- `voltage value`
- `power management attributes`

Feedback

A valid voltage_name must be a valid string that starts with either an uppercase character A-Z or a lowercase character a-z.

The voltage_name in the PG_TO_VOLTAGE_MAP section must be the name used in VOLTAGE_MAP. The name could be a rail name, and can be the same as the pg_pin name. You cannot use an invalid value such as "-" or "*" in the voltage_name field in PG_TO_VOLTAGE_MAP or VOLTAGE_MAP section.

Valid voltage values are non-negative floating point numbers, for example, 0.9, that are valid voltage values in the input library.

For valid power management attributes see the *Library Compiler Modeling Timing, Signal Integrity, and Power in Technology Libraries User Guide*. The following are some examples of power management attributes:

- valid switch_cell_type is coarse_grain and fine_grain
- valid level_shifter_type is HL, LH and HL_LH
- always_on pins are related to backup power
- a switch cell has VVDD+VDD or VVSS+VSS and VVDD has pg_function where VVDD is virtual VDD;
- a valid retention_cell must be a sequential cell with retention_cell and retention_pin attributes

The following example shows an instance where this message occurs: The following example shows a "-" in the voltage name field, resulting in the error message:

```
BEGIN PG_TO_VOLTAGE_MAP
cell            pg_pin          voltage_name    pg_type
ADDFHX1         VDD             -               power
ADDFHX1         VSS             VSS             primary_ground
END PG_TO_VOLTAGE_MAP
```

What Next

Correct the invalid values or voltage_name in the map file. For example, if there is a "-" in the voltage_name field, this message occurs. You must input a valid voltage_name; for example, VDD.

LBDB-897

(error) The input library '%s' has pg_pin's defined as signal pins.

Feedback

Description

When pg_pin's are as signal pins in the library, this message occurs. add_pg_pin_to_db abd add_pg_pin_to_lib have limitation. In the above case, the utility will stop generation of map template and pg_pin based .lib/db.

The following example shows an instance where this message occurs:

The following is an example message:

```
Error: The input library 'test.lib' has pg_pin's defined as signal pins.
 (LBDB-897)
```

What Next

Check the contents of the library to see if there are pg_pin's or rail names or in/output_signal_level as signal pins. If so, remove these pin groups in your .lib and try to rerun the utility add_pg_pin_to_lib.

LBDB-898

(warning) both 'stage_type : pull_up' and 'stage_type : pull_down' '%s' groups are specified with an identical or overlapping when condition.

Description

This warning message occurs when both "stage_type : pull-up" and "stage_type : pull_down" ccs_first_stage/ccs_last_stage groups are specified with an identical or overlapping when condition.

If a first (last) CCB can physically make both rising and falling output transition under the same side-pin condition, then the stage_type of the CCB should be marked as both. The CCSN data should not be split into two stage_type pull_up/pull_down. Otherwise, the characterized result will not be correct.

The following example shows incorrect usage of the *stage_type* attribute, resulting in the warning message:

```
cell(bad) {
    ...
        Pin (A) {
        ...
        ccsn_first_stage() {
        stage_type : PULL_UP;
        when : "B";
                }

        ccsn_first_stage() {
        stage_type : PULL_DOWN;
        when : "B";
```

Feedback

```
                    }
            }

    }
```

In this example, pin 'A' has both "stage_type : pull-up" and "stage_type : pull_down" ccs_first_stage groups specified with an identical or overlapping when condition.

What Next

Check the library source file and correct the incorrect *stage_type* attribute.

LBDB-899

(warning) there is no CCS Noise information.

Description

This warning message occurs when checking cells for CCS Noise information. The tool determined that there are some cells that have CCS Noise data, but no CCS Noise information is defined for the specified cell.

What Next

This is only a warning message. No action is required.

If CCS Noise information is not needed for the cell, you can ignore this message. Otherwise, you can add CCS Noise data for the cell and run the command again.

LBDB-900

(error) The %f value of the power distribution table is not between 0 and 1.

Description

This error message occurs when the values of the power distribution tables are not between 0 and 1.

What Next

Modify the values of the power distribution tables to meet the requirements. Make sure the values are between 0 and 1.

See Also

- LBDB-901
- LBDB-902
- LBDB-903

Feedback

LBDB-901

(error) Missing power distribution tables in %s.

Description

This error message occurs when a cell contains one leakage power group with power distribution tables, but not all leakage power groups have power distribution tables, or when a pin contains one internal power group with power distribution tables, but not all internal power groups have power distribution tables.

What Next

Make sure that all leakage power groups have power distribution tables in a cell, or that all internal power groups have power distribution tables in a pin. Add the missing distribution tables in the .lib file before reading it in.

LBDB-902

(error) The sum of the values in all the distribution tables\n \tattached to %s table is not equal to 1.

Description

This error message occurs when the sum of all values in the distribution tables are not equal to 1. Each value in the distribution table must be between 0 and 1, and the sum of them should be 1.

What Next

Check all the values in all distribution tables attached to the specified leakage power or internal power to make sure that each value is between 0 and 1, and the sum of them is 1. Update the values as needed to meet the requirements.

LBDB-903

(error) In an internal power group, the number of values for power and power\n \tdistribution tables are not the same.

Feedback

Description

This error message occurs when the number of values in the paired power and power distribution tables are not the same in the internal power group. For example, there are 5 values in the rise power table, but there are 6 values in the paired rise power distribution table.

What Next

Check the internal power group for the number of values between the power group and paired power distribution table, rise power group and paired rise power distribution table, or fall power group and paired fall power distribution table. Make sure the number is the same.

LBDB-904

(error) The %s distribution tables are not paired with the %s tables in\n \tthe internal power group.

Description

This error message occurs when power, rise, or fall power distribution tables are not paired with the related power group. For example, when the rise power distribution table is found in the internal power group but no rise power table is found, the tool issues this error message.

What Next

Check the power distribution tables in the internal power group. When the power, rise power, or fall power distribution tables are found, there must be paired power, rise power, fall power groups. If this is not the case, remove the unpaired power distribution tables or add paired power, rise power, fall power groups before reading in the .lib file.

LBDB-905

(error) Indices for the distribution tables are not matched with the\n \tpaired rise power, fall power, or power groups.

Description

This error message occurs when the indices for the distribution tables are not matched with the paired rise power, fall power, or power groups.

What Next

In the internal power group, check the power template and indices for distribution tables and its paired rise power, fall power, or power groups. If the power template is used, they should be the same for distribution tables and its paired rise power, fall_power, or power

Feedback

groups. Index_1 and index_2 for distribution tables and its paired rise power, fall power, or power groups should also be the same. If necessary, update the power template and indices to meet the requirements.

LBDB-906

(error) Missing related_ground_pin in the power distribution table.

Description

This error message occurs when no related_ground_pin is specified in the power distribution table.

What Next

Check the power distribution table to determine if the related_ground_pin attribute is specified. If necessary, add the missing attribute before reading in the .lib file.

LBDB-907

(error) Invalid ground_pin %s with incorrect pg_type.

Description

This error message occurs when the ground_pin is not a valid PG pin defined for the cell with pg_type of primary_ground, backup_ground, or internal_ground.

What Next

Check the pg_type of the related_ground_pin in the power distribution table to see if it is primary_ground, backup_ground, or internal_ground. If the related_ground_pin is not specified as one of the 3 types, it is not a valid ground pin in the power distribution table. Re-specify a valid ground pin for power distribution.

LBDB-908

(error) The logic (%s) represented by %s 'when' attribute on line %u is incompatible with or is a subset of the logic (%s) represented by %s '%s' attribute on line %u.

Description

This error message indicates that the "when" attribute in the noise data group is a subset of the "when" attribute in the current timing group or incompatible with the function attribute of the pin. Note that a noise group is a ccsn_first_stage or ccsn_last_stage for the old format, or an input_ccb or output_ccb referenced in active_input_ccb, active_output_ccb, or propagating_ccb for the new format.

Feedback

The "when" condition in the noise group can only be equal or superset of the "when" condition in the current timing group. Otherwise, the characterized result is not correct.

The following example results in this error. The "when" condition "A" in the ccsn_first_stage is a subset of the "when" condition "A+B" of the timing group. When (A=0 & B=1), the timing group is active, but the ccsn_first_stage group is disabled. This behavior contradicts the fact the ccsn_first_stage is supposed to propagate noise.

```
cell(bad) {
      pin (Out) {
         function : "(A+B) C";
         timing () {
     related_pin : C;
            when : "A+B";
            ccsn_first_stage() {
               when : "A";
               ...
            }
            ...
         }
         ...
      }
      ...
   }
```

The following is the example message:

Error: Cell 'bad', pin 'A', the logic represented by the 'when' attribute (A) in 'ccsn_first_stage' group is a subset of the logic represented by the 'when' attribute (A+B) in the timing group.

Note: OUTPUT PINS NOT PERMITTED You may not use an output pin in the "when" attribute. You need to replace the pin with the expression stored in its "function" attribute.

What Next

Check the library source file, and correct the incorrect "when" attribute.

LBDB-909

(warning) The cell should have at least 1 primary_ground pg_pin and at least 1 primary_power pg_pin. It's being marked as dont_use, dont_touch.

Description

This warning message occurs because in the new libraries based on pg_pin, all of the cells must have at least 1 primary_ground pg_pin and at least 1 primary_power pg_pin.

Feedback

What Next

This is only a warning message. No action is required if users do not want to modify the cell pg pin modeling.

However, if users want to avoid this warning message, add the missing primary_ground pg_pin or primary_power pg_pin and run the command again.

LBDB-910

(warning) The cell skips partial PG requirement checking. It's being marked as dont_use, dont_touch.

Description

This warning message advises you that cells in the specified category skip PG pin requirement checking. The cells could have partial PG pins, meaning the cells are without a primary_power pg_pin or a primary_ground pg_pin. Currently, there is only one type ETM cell in the category.

What Next

This is only a warning message. No action is required.

However, to avoid this warning message, add the missing primary_ground pg_pin or primary_power pg_pin and run the command again.

LBDB-911

(error) The attribute '%s' violates the variation-aware consistence rule.

Description

This warning message advises you that the variation data in the library violates the consistence rule. If any variation attribute contains N/2N data entries, all variation attributes in the same library must also contain N/2N entries at the same N/2N process points (va_values). The number of data entries must be either N or 2N for any variation attribute. This checking rule includes the following models:

- `VA Timing Constraint Model`
- `VA Compact CCS Timing Driver Model`
- `VA CCS Timing Receiver Model (arc-based and pin-based)`

Feedback

What Next

Add the missing variation attribute or correct the process point (va_values). This message appears only once on the first violation entry. Check the other entries in the variation group for violations.

LBDB-912

(error) The variation needs to be consistent across corresponding arcs.

Description

This error message occurs when a variation inconsistency is found among the timing arcs. If the timing_based_variation group exists in a timing arc, all its corresponding timing arcs must also contain the timing_based_variation group. Otherwise, none of the arcs can contain the timing_based_variation group.

What Next

Add the missing timing_based_variation in the corresponding timing arcs and run the command again.

LBDB-913

(warning) is missing '%s' pg_pin, so it will become a black-box cell for multivoltage functional optimization flow. It is being marked dont_touch, dont_use.

Description

This warning message occurs when a cell has 2 or more power or ground pins, but there is no backup power or backup ground pin.

The following conditions apply to retention and isolation cells:

- If cell has 2 or more power pins, there must be a backup power pin.
- If cell has 2 or more ground pins, there must be a backup ground pin.

If the conditions, are not met, the tool issues this warning message. The cell is black box for the multivoltage flow and is being marked as a dont_touch, dont_use (d,u). The black box cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, add or correct the backup_ground pg_pin or backup_power pg_pin and run the command again.

Feedback

LBDB-913e

(error) is missing '%s' pg_pin, so it will become a black box cell for multivoltage functional optimization flow. This cell should be marked as dont_touch, dont_use.

Description

This error message occurs when a cell has 2 or more power or ground pins, but there is no backup power or backup ground pin.

The following conditions apply to retention and isolation cells:

- If the cell has 2 or more power pins, there must be a backup power pin.
- If the cell has 2 or more ground pins, there must be a backup ground pin.

If the above conditions are not met, the tool issues this error message. The cell is black box for the multivoltage flow and should be marked as dont_touch, dont_use (d,u). The black box cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

What Next

If the result is not what you intended, add or correct the backup_ground pg_pin or backup_power pg_pin and run the command again. Alternatively, you can mark this cell as dont_touch, dont_use.

LBDB-914

(warning) is missing related_power_pin to a '%s' pg_pin, so it will become a black box cell for multivoltage functional optimization flow. It is being marked as dont_touch, dont_use.

Description

This warning message occurs when a cell has no related_power_pin, or when the related_power_pin relates to an incorrect pg_pin.

For retention cells, if save or save_restore pins exist, they should be related to the backup power or ground, depending on whether backup power or ground is available. All other signal pins should be related to the primary power or ground. For isolation cells, if a backup power pin exists, the output pin must be related to backup power through a related_power_pin.

The cell is black box for the multivoltage flow and is marked as dont_touch, dont_use (d,u). it cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

Feedback

The following example shows an instance where this message occurs:

```
cell(Isolation_Cell2){
  area : 1.0;
is_isolation_cell : true;
dont_touch : true;
dont_use : true;

pg_pin(VDDB) {
  voltage_name : VDDB;
  pg_type : backup_power;
}

pg_pin(VDD) {
  voltage_name : VDD;
  pg_type : primary_power;
}

pg_pin(VSS) {
  voltage_name : VSS;
  pg_type : primary_ground;
}

  leakage_power() {
    when : "!A";
    value : 1.5;
    related_pg_pin : VDD;
  }
  leakage_power() {
    value : 0.5;
    related_pg_pin : VDD;
  }

pin(A) {
  direction : input;
  related_power_pin : VDD;
  related_ground_pin : VSS;
  isolation_cell_data_pin : true;
  capacitance : 1.0;
  internal_power() {
    rise_power (scalar) { values ("0.0");}
    fall_power (scalar) { values ("0.0");}
  }
}

pin(EN) {
  direction : input;
  related_power_pin : VDD;
  related_ground_pin : VSS;
  isolation_cell_enable_pin : true;
  capacitance : 1.0;
  internal_power() {
    rise_power (scalar) { values ("0.0");}
```

Feedback

```
    fall_power (scalar) { values ("0.0");}
  }
}
pin(Y) {
  direction : output;
  /*VDD is a primary power pin. For isolation output pin,
    it should related to backup power, issue LBDB-914 warning message */
  related_power_pin : VDD;
  related_ground_pin : VSS;
  function : "A * EN";
  power_down_function : "!VDD + VSS";
  timing() {
    related_pin : "A EN";
        cell_rise(scalar) { values ("0.1");}
        rise_transition (scalar) { values ("0.1");}
        cell_fall(scalar) { values ("0.1");}
        fall_transition (scalar) { values ("0.1");}
  }
  internal_power() {
    related_pin : A;
    related_pg_pin : VDD;
        rise_power (scalar) { values ("0.0");}
        fall_power (scalar) { values ("0.0");}
  }

    }/* end pin group*/
  }
```

The following is an example message:

```
Warning: Line 192, Cell 'Isolation_Cell2', pin 'Y', Cell
 'Isolation_Cell2', pin 'Y', is missing related_power_pin to a
 'backup_power' pg_pin, so it will become a black box cell for
 multivoltage functional optimization flow. It is being marked as
 dont_touch, dont_use.  (LBDB-914)
```

What Next

Check the library source file to add or correct related_power_pin attributes.

LBDB-914e

(error) is missing related_power_pin to a '%s' pg_pin, so it will become a black box cell for multivoltage functional optimization flow. This cell should be marked as dont_touch, dont_use.

Description

This error message occurs when a cell has no related_power_pin, or when the related_power_pin relates to an incorrect pg_pin.

For retention cells, if save or save_restore pins exist, they should be related to the backup power or ground, depending on whether backup power or ground is available. All other signal pins should be related to the primary power or ground. For isolation cells, if a backup power pin exists, the output pin must be related to backup power through a related_power_pin.

The cell is black box for the multivoltage flow and should be marked as dont_touch, dont_use (d,u). The cell cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

What Next

If the result is not what you intended, add or correct the related_power_pin and run the command again. Alternatively, you can mark this cell as dont_touch, dont_use.

LBDB-915

(warning) is missing related_ground_pin to a '%s' pg_pin, so it will become a black box cell for multivoltage functional optimization flow. It is being marked as dont_touch, dont_use.

Description

This warning message occurs when a cell has no related_ground_pin, or when the related_ground_pin is related to an incorrect pg_pin.

For retention cells, if save and restore pins exist, they should be related to the backup power or ground, depending on whether backup power or ground is available. All other signal pins should be related to the primary power or ground.

The cell is black box for the multivoltage flow and is marked as dont_touch, dont_use (d,u). It cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

The following example shows an instance where this message occurs:

```
cell(retention_dff) {
  area : 1.0;
  retention_cell : "my_retention_dff" ;

  pg_pin(VDDB) {
    voltage_name : VDDB;
    pg_type : backup_power;
  }
  pg_pin(VDD) {
    voltage_name : VDD;
    pg_type : primary_power;
  }
  pg_pin(VSS) {
    voltage_name : VSS;
    pg_type : primary_ground;
```

Feedback

```
}
pg_pin(VSS1) {
  voltage_name : VSS1;
  pg_type : backup_ground;
}

pin(D) {
  direction : input;
  capacitance : 1;
  nextstate_type : data ;
  related_power_pin : VDD;
  related_ground_pin : VSS;
    internal_power() {
      rise_power(scalar) { values ("1.0");}
      fall_power(scalar) { values ("1.0");}
    }
}

pin(CP) {
  direction : input;
  capacitance : 1;
  related_power_pin : VDD;
  related_ground_pin : VSS;
    internal_power() {
      rise_power(scalar) { values ("1.0");}
      fall_power(scalar) { values ("1.0");}
    }
   }

pin(SAVE) {
  direction : input;
  capacitance : 1.0;
  nextstate_type : data ;
  related_power_pin : VDD;
  /* backup power exists, SAVE/SAVE_RESTORE retention pin must use
backup power,
   issues LBDB-915 warning message*/
  related_ground_pin : VSS;
  retention_pin (save, "0") ;
    internal_power() {
      rise_power(scalar) { values ("1.0");}
      fall_power(scalar) { values ("1.0");}
    }
}

pin(RESTORE) {
  direction : input;
  capacitance : 1.0;
  nextstate_type : data ;
  related_power_pin : VDDB;
  /*RESTORE retention pin can use primary or backup ground as RGP, VDD
is a primary power,
   issues LBDB-915 warning message */
```

Feedback

```
    related_ground_pin : VDD;
    retention_pin (restore, "0") ;
      internal_power() {
        rise_power(scalar) { values ("1.0");}
        fall_power(scalar) { values ("1.0");}
      }
  }

  ff("IQ", "IQN") {
    next_state : "D & (!SAVE & !RESTORE)" ;
    clocked_on : "CP" ;
  }

  pin(Q) {
    direction : output;
    function : "IQ";
    power_down_function : "!VDD + !VDDB + VSS";
    max_capacitance : 5.0 ;
    related_power_pin : VDD;
    related_ground_pin : VSS;
      timing() {
        related_pin : CP;
        timing_type : rising_edge;
        cell_rise(scalar) { values ("0.1");}
        rise_transition (scalar) { values ("0.1");}
        cell_fall(scalar) { values ("0.1");}
        fall_transition (scalar) { values ("0.1");}
      }
      internal_power() {
        related_pin : "D SAVE RESTORE CP";
        rise_power(scalar) { values ("1.0");}
        fall_power(scalar) { values ("1.0");}
      }
  }
  cell_leakage_power : 0.5 ;
  leakage_power() {
    when  : "!SAVE & !RESTORE" ;
    value : 0.7 ;
  }
  leakage_power() {
    when  : "SAVE" ;
    value : 0.1 ;
  }
 }
```

The following is an example message:

```
Warning: Line 103, Cell 'retention_dff', pin 'SAVE', is missing
 related_ground_pin to a 'backup_ground' pg_pin, so it will become a
 black box cell for multivoltage functional optimization flow. It is
 being marked as dont_touch, dont_use. (LBDB-915)
Warning: Line 116, Cell 'retention_dff', pin 'RESTORE', is missing
 related_ground_pin to a 'primary_ground' pg_pin, so it will become a
```

```
black box cell for multivoltage functional optimization flow. It is
being marked as dont_touch, dont_use. (LBDB-915)
```

What Next

Check the library source file to add or correct related_ground_pin attributes.

LBDB-915e

(error) is missing related_ground_pin to a '%s' pg_pin, so it will become a black box cell for multivoltage functional optimization flow. This cell should be marked as dont_touch, dont_use.

Description

This error message occurs when a cell has no related_ground_pin, or when the related_ground_pin is related to an incorrect pg_pin.

For retention cells, if save and restore pins exist, they should be related to the backup power or ground, depending on whether backup power or ground is available. All other signal pins should be related to the primary power or ground.

The cell is black box for the multivoltage flow and should be marked as dont_touch, dont_use (d,u). It cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

What Next

If the result is not what you intended, add or correct the related_ground_pin and run the command again. Alternatively, mark this cell as dont_touch, dont_use.

LBDB-916

(warning) pin '%s' and pin '%s' have different related_power_pin settings, so it will become a black box cell for multivoltage functional optimization flow. It is being marked as dont_touch/dont_use.

Description

This warning message occurs when the 2 specified pins do not relate to the same related_power_pin.

For a level-shifter cell, the related power pin of enable pin should be either same as the related power pin of output pin or data pin, or a backup power pin which is not of std_cell_main_rail.

Feedback

The cell is black box for the multivoltage flow and is marked as dont_touch, dont_use (d,u). It cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

The following example shows an instance where this message occurs:

```
cell (LVLHLEHX2){
  cell_footprint : lvlhleh

  pg_pin(VDDI) {
 voltage_name : "VDDH";
 pg_type : primary_power;
  }
  pg_pin(VDDO) {
 voltage_name : "VDDL";
 pg_type : primary_power;
  }
  pg_pin(VSS) {
 voltage_name : "VSS";
 pg_type : primary_ground;
  }

  is_level_shifter : true ;

  area : 5.883500;
  pin(A) {
    direction : input;
    input_signal_level : VDDH;
    related_power_pin : VDDI;
    related_power_pin : VDDO; /* warning : LBDB-16 */
    related_ground_pin : VSS;
    capacitance : 0.001462;
    ...
  }
  pin(EN) {
    direction : input;
    input_signal_level : VDDH;
    related_power_pin : VDDI;
    related_ground_pin : VSS;
    level_shifter_enable_pin : true ;
    capacitance : 0.001699;
    internal_power();
    ...
  }
  pin(Y) {
    direction : output;
    output_signal_level : VDDL;
    related_power_pin : VDDO;
    related_ground_pin : VSS;
    capacitance : 0.0;
    function : "(A EN)";
    ...
  }
```

Feedback

```
}
```

The following is an example message:

```
Warning: Line 308, Cell 'LVLHLEHX2', pin 'Y' and pin 'EN' have different
 related_power_pin settings, so it will become a black box cell for
 multivoltage functional optimization flow. It is being marked as
 dont_touch/dont_use. (LBDB-916)
```

What Next

Check the library source file to correct related_power_pin attributes.

LBDB-916e

(error) pin '%s' and pin '%s' have different related_power_pin settings, so it will become a black box cell for multivoltage functional optimization flow. This cell should be marked as dont_touch, dont_use.

Description

This error message occurs when the 2 specified pins do not relate to the same related_power_pin.

For a level-shifter cell, the enable pin and the output pin must be related to the same power pin.

The cell is black box for the multivoltage flow and should be marked as dont_touch, dont_use (d,u). It cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

What Next

If the result is not what you intended, make sure the specified pins have the same related_power_pin and run the command again. Alternatively, you can mark this cell as dont_touch, dont_use.

LBDB-917

(warning) no pg_pin or signal pin in this pad cell.

Description

This message indicates this pad cell hasn't a signal pin or pg_pin.

The following example shows an instance where this message occurs:

```
cell(AN2) {
      pad_cell : true;
```

```
    ...
}
```

In this case, the IO cell has no signal pin or pg_pin. To fix the problem, add one signal pin or pg_pin with attribute "is_pad : true".

Warning: Line 12, Cell 'AN2', no pg_pin or signal pin in this pad cell. (LBDB-917)

What Next

Add one signal pin or pg_pin with attribute "is_pad : true".

LBDB-918

(error) The cell '%s' has a retention pin, but it is not a retention cell.

Description

This error message occurs because retention pin and retention cell attributes are considered in pairs. A retention cell is defined with the *retention_cell* or *power_gating_cell* attribute. The cell must have at least one retention control pin, which is defined with the *retention_pin* or *power_gating_pin* attribute.

This means that if one of the pins within a cell is a retention control pin, then the cell might be a retention cell. The retention pin and cell attributes are considered in pairs.

The following example shows an instance where this message occurs: In the following example, there is a *retention_pin* attribute, but there is no *retention_cell* attribute. Remove the comment from the *retention_cell* attribute to correct the problem.

```
cell(retention_dff) {
  ...
  /* retention_cell : "my_retention_dff"; */
  clock_gating_integrated_cell : "generic";

  pin(SAVE) {
    ...
    direction : input;
    retention_pin (save, "0");
  }

  pin(RESTORE) {
    ...
    direction : input;
    retention_pin (restore, "0");
  }
}
```

Feedback

The following is an example message: The above example results in the following error message:

```
Error : The cell 'retention_dff' has a retention pin, but it is not a
retention cell. (LBDB-918)
```

What Next

Resolve the issue by either removing the *retention_pin* attribute or adding a *retention_cell* attribute.

See Also

- LBDB-891

LBDB-919

(warning) Retention cell '%s' is a zero pin design.

Description

This warning message occurs because a retention cell (identified by the *retention_cell* or *power_gating_cell* attribute), might not have a retention pin.

The following example shows an instance where this message occurs: The following design does not have a retention pin, so it is a zero pin retention cell:

```
cell(retention_dff) {
  ...
  retention_cell : "my_retention_dff" ;

  pin(SAVE) {
    ...
    direction : input;
  }

  pin(RESTORE) {
    ...
    direction : input;
  }
}
```

The following is an example message:

```
Warning: Retention cell 'retention_dff' is a zero pin design (LBDB-919)
```

What Next

Check that the design is a real zero pin retention cell.

Feedback

See Also

- LBDB-891
- LBDB-918

LBDB-920

(warning) The is_inverting attribute of ccsn_first_stage and ccsn_last_stage are not matched with the arc's timing_sense type.

Description

This warning message occurs when the timing arc's CCS noise data does not match with the timing_sense of this arc. The tool expects the following matching between arc-based noise data and timing_sense:

- When both *ccsn_first_stage* and *ccsn_last_stage* have is_inverting = TRUE, the expected timing_sense is pos_unate.
- When both *ccsn_first_stage* and *ccsn_last_stage* have is_inverting = FALSE, the expected timing_sense is pos_unate.
- When either *ccsn_first_stage* or *ccsn_last_stage* has is_inverting = TRUE, and the other has is_inverting = FALSE, the expected timing_sense is neg_unate.

  The following example shows an instance where this message occurs: The incorrect input below causes this warning message:

```
pin(CO) {
  timing() {
    timing_sense : neg_unate ;
    ccsn_first_stage() {
      is_inverting = true;
      ...
    } /* qualified model 1 */
    ccsn_first_stage() {
      is_inverting = true;
      ...
    } /* qualified model 1 */
  }
  ...
}
```

In this example, the CO pin has a two stage arc, and both the first and last stages are inverting, so a positive arc is expected. To fix the problem, change timing_sense to positive.

The following is an example message: The following is an example of the warning message:

```
Warning: The is_inverting attribute of ccsn_first_stage and
ccsn_last_stage are not matched with the arc's timing_sense type.
```

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, correct the noise modeling. If the noise modeling comes from the noise characterization tool, check with the noise characterization tool to determine why this type of data was generated.

LBDB-921

(warning) %s is missing in timing arc in pin %s.

Description

This warning message occurs when a timing arc has *receiver_capacitance_rise* or *receiver_capacitance_fall*, but not both.

The following is an example message: The following is an example of the warning message:

```
Warning: Line 206, receiver_capacitance_fall is missing in timing arc
in pin A.(LBDB-921)
```

What Next

This is only a warning message. No action is required.

LBDB-922

(warning) In '%s' group, ccsn_first_stage at line %u and\n \tccsn_last_stage at line %u have different values for related_ccb_node.

Description

related_ccb_node of the ccsn_first_stage and ccsn_last_stage in the same timing group should be identical.

The following example shows an instance where this message occurs:

```
library(test) {
  cell (flop) {
    ...
    pin (CP) {
      ...
```

Feedback

```
    }
    pin (Q) {
      ...
      timing () {
        ...
        related_pin :CP;
        ccsn_first_stage() {
          related_ccb_node : "net3:3";
          ...
        }
        ccsn_last_stage() {
          related_ccb_node : "net7:5";
          ...
        }
      }
    }
    ...
  }
}
```

The following is an example message:

```
Warning: Line 32, In 'timing' group, ccsn_first_stage at line 35 and
        ccsn_last_stage at line 39 have different values for
 related_ccb_node. (LBDB-922)
```

What Next

Use same values for the related_ccb_node of the ccsn_first_stage and ccsn_last_stage in the same timing group.

LBDB-923

(error) %s but not %s is needed in this timing arc %s.

Description

This error message occurs when a mismatched *receiver_capacitance_rise* exists in a timing arc. For example, when timing_type = combinational_rise and timing_sense = positive_unate, then *receiver_capacitance_rise* is needed. The error occurs when the timing arc has only *receiver_capacitance_fall*.

The following is an example message: The following is an example of the error message:

```
Error: Line 206, receiver_capacitance_rise but not
receiver_capacitance_fall is needed in timing arc.(LBDB-921)
```

Feedback

What Next

Correct the timing modeling. If the timing modeling comes from the timing characterization tool, check with the timing characterization tool to determine why this type of data was generated.

LBDB-924

(warning) There are more than %d %s in %s. \n

Description

This message indicates that the object number is not as expected.

Only one pg_pin can be specified in pg_function Boolean expression of a non-macro switch cell, otherwise the cell will be marked dont use.

The following example shows an instance where this message occurs:

```
cell(lbdb136) {
      area : 9;
      pg_pin(VDD) {
        pg_type : primary_power;
        voltage_name :VDD;
      }
      pg_pin(VSS) {
        pg_type : primary_ground;
        voltage_name :VSS;
      }
      pg_pin(VVDD) {
        pg_type : internal_power;
        voltage_name :VVDD;
        switch_function : "sleep";
        pg_function : "!VDD+VSS";
      }
    }
```

In this case, the pg_function is composed by two pg_pin, which suppose to be 1.

The following is an example message:

```
Warning: Line 1848, There are more than 1 pg_pin in pg_function.
 (LBDB-924)
```

What Next

Refer to the "Library Compiler User Guide" to determine the object number. Make the correction.

Feedback

LBDB-925

(warning) The %s of %s%s%s should be %s. \n

Description

This message indicates that the value or attribute is not as expected.

For non-macro switch cell, the pg_pin specified in pg_function of a power pg_pin must be primary/backup power, the pg_pin specified in pg_function of a ground pg_pin must be primary/backup ground.

For macro switch cell, the pg_pin specified in pg_function of a power pg_pin must be primary/internal/backup power, the pg_pin specified in pg_function of a ground pg_pin must be primary/internal/backup ground.

The following example shows an instance where this message occurs:

```
cell(lbdb136) {
      area : 9;
      pg_pin(VDD) {
        pg_type : primary_power;
        voltage_name :VDD;
      }
      pg_pin(VSS) {
        pg_type : primary_ground;
        voltage_name :VSS;
      }
      pg_pin(VVDD) {
        pg_type : internal_power;
        voltage_name :VVDD;
        switch_function : "sleep";
        pg_function : "!VDD+VSS";
      }
    }
```

In this non-macro case, the pg_function is specified on pg_pin VVDD, whose pg_type is internal_power. So the pg_function should be composed by pg_pin whose pg_type is primary_power or backup_power.

The following is an example message:

```
Warning: Line 848, The pg_type of pin VDD in pg_function should be
 primary_power or backup_power. (LBDB-925)
```

What Next

Refer to the "Library Compiler User Guide" to determine the value or attribute. Make the correction.

Feedback

LBDB-926

(warning) The %s '%s' is missing the attribute '%s'.

Description

You receive this message when the required attribute is missing.

The following example shows an instance where this message occurs:

```
cell(lbdb926) {
      area : 9;
      pg_pin(VDD) {
        pg_type : primary_power;
        voltage_name :VDD;
      }
      pg_pin(VSS) {
        pg_type : primary_ground;
        voltage_name :VSS;
      }
      pg_pin(VVDD) {
        pg_type : internal_power;
        voltage_name :VVDD;
      }
    }
```

In this case, there is no pg_function when pg_type is internal_power

The following is an example message:

```
Warning: Line 848, The pg_pin 'VVDD' is missing the attribute
 'pg_function'. (LBDB-926)
```

This is another example:

```
cell(lbdb926) {
      area : 9;
      pg_pin(VDD) {
        pg_type : primary_power;
        voltage_name :VDD;
      }
      pg_pin(VSS) {
        pg_type : primary_ground;
        voltage_name :VSS;
      }
      pg_pin(VVDD) {
        pg_type : internal_power;
        voltage_name :VVDD;
        switch_function : "sleep";
      }
    }
```

Feedback

In this case, there is only switch_function in pg_pin VDD, which should coexist with pg_function.

The following is an example message:

```
Warning: Line 848, The pg_pin 'VVDD' is missing the attribute
 'pg_function'. (LBDB-926)
```

What Next

Specifiy the missing attribute.

LBDB-927

(warning) It is invalid to specify the '%s' %s \n \ton the '%s' %s%s.

Description

This message indicates that you specified an invalid attribute/group on a cell/pin.

The following example shows an instance where this message occurs:

```
cell (p) {
    clocked_cell : rising_edge;
    pin(clk) {
        clock : true;
    }

    pin(out) {
        function : "clk";
    }
  }
```

To solve this issue, we need to add "combinational" timing arcs between "clk" pin and "out" pin.

The following is an example message:

```
Warning: Line 67, It is invalid to specify the 'clocked_cell' attribute
        on the 'p' cell. (LBDB-927)
```

What Next

Check the library source file, and correct the problem. For example, in order to specify the "clocked_cell" attribute, the cell needs to satisfy the following 2 conditions: - has only 1 clock pin whose "clock" attribute is set to "true". - has at least 1 timing arc between the clock pin and an output pin.

Feedback

LBDB-928

(warning) The pin '%s' specified in the '%s' is neither\n \tan %s pin nor an inout pin.

Description

This message indicates that direction of the pin you specified in a *related_inputs*, *related_outputs*, *related_output*, *index_output* or *gate_leakage* is wrong.

The following example shows an instance where this message occurs:

```
cell(lbdb730) {
  area : 2;
  pin(A) {
    direction : input;
    capacitance : 1;
  }
  pin(B) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "A B";
    timing() {
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      slope_rise : 0.0;
      slope_fall : 0.0;
      related_pin : "A B";
    }
  }
  leakage_current() {
     when : "A & !B & Z";
     pg_current(V1) {
      ...
     }
     ...
     gate_leakage(Z) {  /* must be input or inout pin */
       input_high_value : 2.1;
       input_low_value : -1.7;
     }
  }
  dynamic_current() {
    when : "A";
    related_inputs : "Z";
    related_outputs : "B"
    typical_capacitances(0.3);
    switching_group() {
      input_switching_condition(fall);
```

Feedback

```
        output_switching_condition(rise);
        pg_current(<pg_name>) {
          vector(<lu_template_name>) {
            reference_time : 93.2;
            index_output : "A";
            index_1("5.1");
            index_2("0.3");
            index_3("8.2 9.4 9.8");
            values("1.78 12.4 110.1");
          }
        }
       ...
      }
    }
    intrinsic_parasitic() {
      /* default state */
      intrinsic_resistance(<pg_name>) {
         related_output : "B";
         value : 9.0;
      }
      intrinsic_capacitance(<pg_name>) {
         value : 8.2;
      }

    }
    ...
}
```

In this case, all related_output, related_outputs, related_inputs, index_output and gate_leakage have a wrong pin name. To fix the problems, change the name from 'Z' to either 'A' or 'B' in the related_inputs, change the name from 'B' to 'Z' in the related_outputs, change the name from 'A' to 'Z' in the index_output, change the name from 'B' to 'Z' in the related_output and change the name from 'Z' to either 'A' or 'B' in the gate_leakage.

The following is an example message:

```
Warning: Line 272, The pin 'Z' specified in the 'related_inputs' is
 neither
        an input pin nor an inout pin. (LBDB-928)
Warning: Line 471, The pin 'B' specified in the 'related_outputs' is
 neither
        an output pin nor an inout pin. (LBDB-928)
Warning: Line 526, The pin 'A' specified in the 'index_output' is neither
        an output pin nor an inout pin. (LBDB-928)
Warning: Line 890, The pin 'B' specified in the 'related_output' is
 neither
        an output pin nor an inout pin. (LBDB-928)
Warning: Line 749, The pin 'Z' specified in the 'gate_leakage' is neither
        an input pin nor an inout pin. (LBDB-928)
```

Feedback

What Next

Check the library source file, and make the necessary correction.

LBDB-929

(error) The %s cell is invalid for missing %s%s. It's being marked as dont_use.\n

Description

This message indicates that there are some attribute/group missing for the cell.

The following example shows an instance where this message occurs:

```
cell(lbdb136) {
      switch_cell_type : coarse_grain;
      area : 9;
      pg_pin(VDD) {
        pg_type : primary_power;
        voltage_name :VDD;
      }
      pg_pin(VSS) {
        pg_type : primary_ground;
        voltage_name :VSS;
      }
      pg_pin(VVDD) {
        pg_type : internal_power;
        voltage_name :VVDD;
        pg_function : "VDD";
      }
    }
```

In this case, the switch cell has no internal_power|ground pg_pin with both "switch_function" and "pg_function".

The following is an example message:

```
Error: Line 820, The switch cell is invalid for missing
 internal_power|ground
pg_pin with both switch_function and pg_function. It's being marked as
 dont_use. (LBDB-929)
```

What Next

Refer to the "Library Compiler User Guide" to sepcify the attribute/group. Make the correction.

LBDB-930

(warning) The %s cell is invalid for missing %s%s. \n

Feedback

Description

This message indicates that there are some attribute/group missing for the cell.

The following example shows an instance where this message occurs:

```
cell(lbdb136) {
      switch_cell_type : coarse_grain;
      area : 9;
      pg_pin(VDD) {
        pg_type : primary_power;
        voltage_name :VDD;
      }
      pg_pin(VSS) {
        pg_type : primary_ground;
        voltage_name :VSS;
      }
      pg_pin(VVDD) {
        pg_type : internal_power;
        voltage_name :VVDD;
        pg_function : "VDD";
      }
    }
```

In this case, the switch cell has no internal_power|ground pg_pin with both "switch_function" and "pg_function".

The following is an example message:

```
Warning: Line 820, The switch cell is invalid for missing
 internal_power|ground
pg_pin with both switch_function and pg_function. (LBDB-930)
```

What Next

Refer to the "Library Compiler User Guide" to sepcify the attribute/group in source lib file. Make the correction and regenerate a new db file.

LBDB-931

(error) The %s number is less than %d in %s.

Description

This message indicates that the object number is not as expected.

The following example shows an instance where this message occurs:

```
cell(lbdb136) {
      area : 9;
      is_level_shifter : TRUE;
      pin_opposite("A", "BB");
```

Feedback

```
      contention_condition : "A";
      pin(A) {
        direction : input;
        level_shifter_data_pin : TRUE;
      }
      pin(BB) {
        direction : input;
        level_shifter_data_pin : TRUE;
      }
      pin(Y) {
        direction : output;
        function : "A+BB"
      }
    }
```

In this case, the contention_condition is composed by one pin, which suppose to be at least 2.

The following is an example message:

```
Error: Line 1848, The pin number is less than 2 in contention_condition
 for a differential level shifter. (LBDB-931)
```

What Next

Refer to the "Library Compiler User Guide" to determine the object number. Make the correction.

LBDB-932

(warning) The %s%s%s%s is missing%s.

Description

This message indicates that there is object/group missing.

The following example shows an instance where this message occurs:

```
cell(lbdb136) {
      area : 9;
      is_level_shifter : TRUE;
      pin_opposite("A", "BB");
      contention_condition : "!(A^BB)";
      pin(A) {
        direction : input;
        level_shifter_data_pin : TRUE;
      }
      pin(BB) {
        direction : input;
        level_shifter_data_pin : TRUE;
      }
      pin(Y) {
```

```
        direction : output;
        function : "A+BB"
      }
    }
```

In this case, there should be the timing constraints group between A and BB.

The following is an example message:

```
Warning: Line 1848, The nonsequential timing constraints group between
 pin A and pin BB is missing for a differential level shifter. (LBDB-932)
```

What Next

Refer to the "Library Compiler User Guide" to determine if the object/group is required. Make the correction.

LBDB-933

(error) The value of '%s' is %g, and is not in the range of %s which is between %g and %g.

Description

This message indicates that the attribute value you have specified is not in the required range. For example: For input_signal_level, Library Compiler will check if it is in pin level "input_voltage_range". If there is no pin level "input_voltage_range", check the range of cell level "input_voltage_range"; . For output_signal_level, Library Compiler will check if it is in pin level "output_voltage_range". If there is no pin level "output_voltage_range", check the range of cell level "output_voltage_range"; .

The following example shows an instance where this message occurs:

```
cell (ls) {
    input_voltage_range(0.5, 1.2);
    pin(A) {
      input_signal_level : 1.3;
    }

    pin(Y) {
      function : "A";
    }
  }
```

To correct the error, change the input_signal_level to 1.2, which is in the range of (0.5 ~ 1.2)

Feedback

The following is an example message:

```
Error: Line 77, Cell 'ls', pin 'Y', The value of 'input_signal_level' is
 1.3, and is not in the range of input_voltage_range which is between 0.5
 and 1.2. (LBDB-933)
```

What Next

Check the library source file, and ensure the attribute value is consistent with corresponding range.

LBDB-934

(warning) Overwrite '%s' defined in 'operating_condition' by '%s' value %f.

Description

In existing .db files, nom PVT can be copied over to all PVT (process, voltage and temperature) defined in default_operating_conditions.

The warning message indicates that whatever PVT defined in default_operating_conditions have been overwritten by values of nom PVT.

The following example shows an instance where this message occurs:

```
library(libdb934) {
 ...
  nom_process : 1.3
  nom_temperature : 20.0;
  nom_voltage : 4.0;

  operating_conditions ( TYPICAL ) {
    process : 1.0 ;
    temperature : 22.0 ;
    voltage : 3.0 ;
    tree_type : balanced_tree ;
  }
  default_operating_conditions :  TYPICAL;
   ...
  voltage_map(VDD1, 4.0); /* new pg pin syntax */
  voltage_map(VDD2, 4.5);
   ...
  cell (and2) {
   ...
  pg_pin(V1) { /* new pg pin syntax */
     voltage_name : VDD1;
     pg_type : primary_power;
  }
  pg_pin(V2) {
     voltage_name : VDD2;
     pg_type : backup_power;
```

```
  }
  ...
```

In this case, process defined in default operating_conditions group will be overwritten by "nom_process" value 1.3. Temperature defined in default operating_conditions group will be overwritten by "nom_temperature" value 20.0. Voltage defined in default operating_conditions group will be overwritten by "nom_voltage" value 4.0.

The following are example messages:

```
Warning: Line 100, Overwrite 'process' defined in 'operating_conditions'
 by default 'nom_process' value 1.3. (LBDB-934)
Warning: Line 100, Overwrite 'voltage' defined in 'operating_conditions'
 by default 'nom_voltage' value 20.0. (LBDB-934)
Warning: Line 100, Overwrite 'temperature' defined in
 'operating_conditions' by default 'nom_temperature' value 4.0.
 (LBDB-934)
```

LBDB-935

(error) Attribute %s is not allowed in this ccs noise stage.

Description

input_signal_level and output_signal_level are used to provide additional information on the operation of a CCS noise stage, but not to override voltages that can be determined from the pin, or related pin.

The following usage is disallowed:

```
input_signal_level in a pin-based ccsn_first_stage group
output_signal_level in a pin-based ccsn_last_stage group
input_signal_level or output_signal_level in an arc-based
 ccsn_first_stage
or ccsn_last_stage group

The following example shows an instance where this message occurs:
library(lbdb935) {
  ...
  voltage_map(COREVDD1,1.080000);
  voltage_map(COREGND1,0.000000);
  voltage_map(COREVDD2,0.900000);
  voltage_map(COREVDD3,0.990000);
  ...
  cell (INV_PIN_BASED) {
    ...
    pg_pin(VDD) {
      voltage_name : VDD1;
      ...
    }
    pg_pin(VDDL) {
```

```
      voltage_name : VDD2;
      ...
    }
    pg_pin(VSS) {
      voltage_name : GND1;
      ...
    }
    pin (I) {
      direction : input;
      related_power_pin : VDDL;
      ccsn_first_stage {
        input_signal_level : COREVDD1;
        ...
      }
      ...
    }
    pin (Z) {
      direction : output;
      related_power_pin : VDD2;
      ccsn_last_stage {
        output_signal_level : COREVDD1;
        ...
      }
      ...
    }

  ...
```

The input signal level of the ccsn_first_stage group is determined by related_power_pin of pin I. The output signal level of the ccsn_last_stage group is determined by the related_pin of pin Z.

The following are example messages:

```
Error: Line 4303, Cell 'INV_PIN_BASED', pin 'I', Attribute
 input_signal_level not allowed in this ccs noise stage (LBDB-935)

Error: Line 4455, Cell 'INV_PIN_BASED', pin 'Z', Attribute
 output_signal_level not allowed in this ccs noise stage (LBDB-935)
```

LBDB-936

(error) %s is an invalid signal value.

Description

The signal level referenced by input_signal_level or output_signal_level of a CCS or CCB noise stage must already be defined in a pg_pin. Also the signal level must has a positive and non-zero voltage.

Feedback

The following example shows an instance where this message occurs:

```
library(lbdb936) {
  ...
  voltage_map(COREVDD1,1.080000);
  voltage_map(COREGND1,0.000000);
  voltage_map(COREVDD2,0.900000);
  voltage_map(COREVDD3,0.990000);
  ...
  cell (INV_BAD_SIGNAL_LEVEL) {
    ...
    pg_pin (VDD) {
      voltage_name : COREVDD1;
      ...
    }
    pg_pin (VDDL) {
      voltage_name : COREVDD2;
      ...
    }
    pg_pin (VSS) {
      voltage_name : COREGND1;
      ...
    }
    pin (I) {
      direction : input;
      related_ground_pin : VSS;
      related_power_pin : VDDL;
      ...
      ccsn_first_stage () {
        ...
        output_signal_level : COREVDD3;
...
    }
    ...
  }
  ...
```

The output_signal_level COREVDD3 is not declared in any pg_pins of cell INV_BAD_SIGNAL_LEVEL

The following is an example message:

```
Error: Line 187, Cell 'INV_BAD_SIGNAL_LEVEL', pin 'I', COREVDD3 is an
 invalid signal level. (LBDB-936)
```

What Next

Correct the problem.

LBDB-937

(error) Arc-based level-shifting CCS noise stages have inconsistent voltages.

Feedback

Description

This error message concerns arc-based, two-stage noise models (ccsn_first_stage/ ccsn_last_stage pair inside a timing group) that are level shifting. The voltage value given in the output_signal_level attribute of the first stage does not agree with that from the input_signal_level attribute of the last stage.

The following example shows an instance where this message occurs:

```
library(lbdb937) {
  ...
  voltage_map(VDD1,1.080000);
  voltage_map(GND1,0.000000);
  voltage_map(VDD2,0.900000);
  ...
  cell (INV_ARC_LS) {
    ...
    pg_pin (VDD) {
      voltage_name : VDD1;
      ...
    }
    pg_pin (VDDL) {
      voltage_name : VDD2;
      ...
    }
    pg_pin (VSS) {
      voltage_name : GND1;
      ...
    }
    pin (I) {
      direction : input";
      related_power_pin : VDDL;
      ...
   }
   pin (Z) {
     direction : output;
     related_power_pin : VDD;
     timing () {
       related_pin : I;
       ccsn_first_stage {
         output_signal_level: VDD2;
       }
       ccsn_last_stage {
         input_signal_level: VDD1;
       }
     ...
     }
  ...
```

The first stage has an output level of 0.9V, but the last stage has an input level of 1.08V. Correct the problem.

Feedback

The following is an example message:

```
Error: Line 1255, Cell 'INV_ARC_LS', pin 'Z', arc-based level-shifting
 CCS noise stages have inconsistent voltages" (LBDB-937)
```

LBDB-938

(error) The related_pins in this timing group have incompatible input signal levels.

Description

A timing group may be shared by multiple input pins by putting the names of the input pins in the related_pin attribute. For CCS noise model sharing to be valid, the inputs must have the same signal levels.

The following example shows an instance where this message occurs:

```
library(lbdb938) {
  ...
  voltage_map(VDD1,1.080000);
  voltage_map(GND1,0.000000);
  voltage_map(VDD2,0.900000);
  ...
  cell (BAD_RELATED_PINS) {
    ...
    pg_pin (VDD) {
      voltage_name : VDD1;
      ...
    }
    pg_pin (VDDL) {
      voltage_name : VDD2;
      ...
    }
    pg_pin (VSS) {
      voltage_name : GND1;
      ...
    }
    pin (E) {
      direction : "input";
      level_shifter_enable_pin : true;
      related_ground_pin : "VSS";
      related_power_pin : "VDD";
      ...
    }
    pin (I) {
      direction : "input";
      level_shifter_data_pin : true;
      related_ground_pin : "VSS";
      related_power_pin : "VDDL";
      ...
    }
    pin (Z) {
```

Feedback

```
      direction : output;
      related_power_pin : VDDL;
      timing () {
        function : "I' E'";
        related_pin : "I E";  /* two pins */
        ccsn_first_stage () { /* this is a shared arc-based noise model
 */
        ...
      }
     ...
    }
  ...
```

The ccsn_first_stage is shared by input pins E and I. However, pins E and I have different signal levels, which is illegal.

The following is an example message:

```
Error: Line 198, Cell 'BAD_RELATED_PINS', pin 'Z', The related_pins in
 this timing group have incompatible input signal levels" (LBDB-938)
```

LBDB-939

(warning) This CCS noise stage group is missing %s attribute

Description

A level shifter cell is likely to have a CCS noise stage group that is level shifting. This particular group is assumed to be single voltage. If it is actually a low-to-high level shifting stage, you will also most likely encounter errors LBDB-706 and LBDB-953 as well. See section EXAMPLE MESSAGE at the end.

The following example shows a liberty modeling snippet where this message occurs:

```
voltage_map("VDD1",1.080000);
  voltage_map("VSS", 0.000000);
  voltage_map("VDD2",0.900000);

  cell (low_to_high_LS) {
    is_level_shifter : true;
    level_shifter_type : "LH";
    input_voltage_range(0.900000,1.320000);
    output_voltage_range(0.900000,1.320000);
    ...
    pg_pin (VDD1) {
      pg_type : "primary_power";
      voltage_name : "VDD1";
      std_cell_main_rail : true;
    }
    pg_pin (VDD2) {
      pg_type : "primary_power";
      voltage_name : "VDD2";
```

```
    }
    pg_pin (VSS) {
      pg_type : "primary_ground";
      voltage_name : "VSS";
    }
    pin (I) {
      direction : "input";
      level_shifter_data_pin : true;
      related_ground_pin : "VSS";
      related_power_pin : "VDD2";
      ccsn_first_stage () {
        /* output_signal_level : "VDD1"; */
        ...
      }
      ...
    }
    pin (Z) {
      direction : "output";
      function : "I'";
      related_ground_pin : "VSS";
      related_power_pin : "VDD1";
      ...
      ccsn_last_stage () {
        /* input_signal_level : "VDD2"; */
        ...
      }
      ...
  }
```

The ccsn_first_stage group is missing the output_signal_level attribute. The ccsn_last_stage group is missing the input_signal_level attribute

The following is an example message:

```
Warning: Line 180, Cell 'low_to_high_LS', pin 'I', This CCS noise stage
 group is missing output_signal_level (LBDB-939)
Error: Line 180, Cell 'low_to_high_LS', pin 'I', output_voltage_fall
 analysis failed during CCS Noise compilation (LBDB-706)
Warning: Line 332, Cell 'low_to_high_LS', pin 'Z', This CCS noise stage
 group is missing input_signal_level (LBDB-939)
```

What Next

Add the missing input_signal_level or output_signal_level with a correct voltage name.

LBDB-940

(error) The level shifter cell contains invalid related power/ground pin configuration for input pin '%s' and output pin '%s'.

Feedback

Description

The tool issues this error message if the related power and ground pin configuration for the specified input and ouput pins is modeled incorrectly for a level-shifter cell.

Liberty supports the following types of power and ground pin configurations for the input and output pins of a level shifter:

- Power level shifters

  The related power pins are different and the related ground pins are the same.

- Ground level shifters

  The related ground pins are the same and the related power pins are different.

- Power and ground level shifters

  Both the related power pins and the related ground pins are different.

This error occurs when both the related power pins and the related ground pins are the same for the input and output of a level-shifter cell.

The following example shows an instance where this message occurs: The following example shows a level shifter with incorrect modeling and the resulting error message in the PG syntax:

```
library (test) {
  ...
  voltage_map( VSS, 0.0);
  voltage_map( VDDH, 0.9);
  voltage_map( VDDL, 0.7);
  ...
  cell(LS) {
  ...
    pg_pin(GND) {
      voltage_name : VSS;
      pg_type : primary_ground;
    }
    pg_pin(VDD2) {
      voltage_name : VDDH;
      pg_type : primary_power;
    }
    pg_pin(VDD1) {
      voltage_name : VDDL;
      pg_type : primary_power;
    }

    is_level_shifter : true;
    ...
    pin(in) {
      ...
      related_power_pin : VDD1;
```

Feedback

```
      related_ground_pin : GND;
    }
    pin(out) {
      ...
      related_power_pin: VDD1;
      related_ground_pin : GND;
    }
  }
  ...
}

Error: Line 191, Cell 'LS', The level shifter cell contains invalid
related power/ground pin configuration for input pin 'in' and output
pin 'out'. (LBDB-940)
```

What Next

Modify the modeling information of the level shifter to meet the requirements.

To correct the modeling of the previous example, make the *related_power_pin* value of the input pin different from the *related_power_pin* value of the output pin as follows:

```
cell(LS) {
  is_level_shifter : true;
  ...
  pin(in) {
    ...
    related_power_pin: VDD1;
    related_ground_pin : GND;
  }
  pin(out) {
    ...
    related_power_pin: VDD2;
    related_ground_pin : GND;
  }
}
```

LBDB-941

(error) Attribute "scan_start_pin" can only be specified under an output/inout bus/bundle.

Description

This message indicates that the direction of the bus/bundle with attribute "scan_start_pin" is not output/inout.

The following example shows an instance where this message occurs:

```
cell (mb_cell) {

    bundle(Q) {
      members(Q0, Q1)
```

Feedback

```
     direction       : internal;
      scan_start_pin : Q0;
      ...
    }

    ...

  }
```

The following is an example message:

```
Error: Line 253, Cell 'SDFF2_SO', pin 'Q', Attribute "scan_start_pin" can
 only be specified under an output/inout bus/bundle. (LBDB-941)
```

What Next

Check the library source file, and make sure the attribute "scan_start_pin" is specified under the correct bus/bundle.

LBDB-942

(error) Can't find single-bit scan input/output pin in the multi-bit scan cell.

Description

This message indicates that the multi-bit scan cell with attribute "scan_start_pin" must have both single-bit scan input pin and scan output pin defined. The single-bit scan input/output pin should be specified with signal_type "test_scan_in"/"test_scan_out" in test_cell.

The following example shows an instance where this message occurs:

```
cell (mb_cell) {

    pin(SI) {
        direction          : input;
        ...
    }
    pin(SO) {
        direction          : output;
        ...
    }

    bundle(Q) {
        members(Q0, Q1)
        direction       : output;
        scan_start_pin : Q0;
        ...
    }

    test_cell() {
        pin(SI) {
            direction          : input;
```

```
            signal_type         : "test_scan_in";
            ...
        }
        pin(SO) {
            direction           : output;
            /* signal_type      : "test_scan_out"; */
            ...
        }
    }
    ...

}
```

The following is an example message:

```
Error: Line 149, Cell 'SDFF2_SO', Can't find single-bit scan input/output
 pin in the multi-bit scan cell. (LBDB-942)
```

What Next

Check the library source file, and make sure the correct signal_type attribute is specified in test_cell.

LBDB-943

(error) Can't find attribute "single_bit_degenerate" in the multi-bit scan cell.

Description

This message indicates that the attribute "single_bit_degenerate" is missing for the multi-bit scan cell with attribute "scan_start_pin" on bus/bundle. To mapping a complex multi-bit scan cell with serial scan chain and dedicate scan output, a single-bit degenerate cell is needed for mapping the multi-bit cell to N-slice single-bit cell.

The following example shows an instance where this message occurs:

```
cell (mb_cell) {

    /* single_bit_degenerate : sb_cell; */

    bundle(Q) {
      members(Q0, Q1)
     direction       : output;
      scan_start_pin : Q0;
      ...
    }

    ...

  }
```

Feedback

The following is an example message:

```
Error: Line 149, Cell 'SDFF2_SO', Can't find attribute
 "single_bit_degenerate" in the multi-bit scan cell. (LBDB-943)
```

What Next

Check the library source file, and make sure the attribute "single_bit_degenerate" is specified under the cell

---

LBDB-944

(error) The value of "scan_start_pin" can only be the first or last bit pin of the bus/bundle.

Description

This message indicates that the value of attribute "scan_start_pin" can only be the first/last bit pin of the bus/bundle.

The following example shows an instance where this message occurs:

```
cell (mb_cell) {

    bundle(Q) {
      members(Q0, Q1, Q2, Q3)
     direction       : output;
      scan_chain_path : Q2;
      ...
    }

    ...

  }
```

The following is an example message:

```
Error: Line 199, Cell 'mb_4_scanin_gated_scanout1', pin 'Q', The value
 of "scan_start_pin" can only be the first or last bit of the parent
 bus/bundle. (LBDB-944)
```

What Next

Check the library source file, and make sure the value of attribute "scan_start_pin" is the first/last bit pin of the bus/bundle.

LBDB-945

(warning) Since the function of the cell is understood the "single_bit_degenerate" attribute will be ignored.

Feedback

Description

This message indicates that the "single_bit_degenerate" attribute is not needed for this multi-bit cell function specification, and will be ignored in function extraction. User should remove it from the Liberty file.

The function of this multi-bit scan cell can be recognized, and the corresponding single-bit cell can be degenerated from the multi-bit cell itself.

This attribute is only required when the multi-bit cell function is too complex, that corresponding single-bit cell can't be denegerated from the multi-bit cell.

What Next

Check the library source file, and remove attribute "single_bit_degenerate".

LBDB-946

(error) The voltage value %f of the insulated PG pin voltage_map '%s' is not the same as the value %f of voltage of the tied to power/ground PG pin voltage_map '%s'.

Description

This message indicates the insulated well PG pin voltage_map attribute specify the different voltage value from that of the voltage of the tied to power/ground PG pin. They should be equal.

The following example shows an instance where this message occurs:

```
library(insulatedPgpin) {
  ...
   voltage_map (vdd, 1.0);
   voltage_map (gnd, 0.0);
   voltage_map (vddo, 1.0);
   voltage_map (gndo, 0.0);
   voltage_map (vdds, 0.0);
   voltage_map (gnds, 1.0);
   voltage_map (vdds', 1.0);
   voltage_map (gnds', 1.0);
cell (insulated_well) {
   area : 0.3264;
   pg_pin(gndo){
    pg_type : backup_ground;
    voltage_name : gndo;
    related_bias_pin : gnds';
   }

   pg_pin(vddo){
    pg_type : backup_power;
    voltage_name : vddo;
    related_bias_pin : vdds';
```

```
    }
    pg_pin(gnds') {
     pg_type : pwell;
     voltage_name : gnds';
     is_insulated : TRUE;
     tied_to : gndo;
     direction : internal;
     }
     pg_pin(vdds') {
     pg_type : nwell;
     voltage_name : vdds';
     is_insulated : TRUE;
     tied_to : vddo;
     direction : internal;
     }
     pg_pin(gnds) {
     pg_type : pwell;
     voltage_name : gnds;
     direction : internal;
     physical_connection : device_layer;
     }
     pg_pin(vdds) {
     pg_type : nwell;
     voltage_name : vdds;
     direction : internal;
     physical_connection : device_layer;
     }
     }
} /* end library */
```

The following is an example message:

```
Error: Line 58, Cell 'insulated_well', pin 'gnds'', The voltage value
 1.000000 of the insulated PG pin voltage_map 'gnds'' is not the same
 as the value 0.000000 of voltage of the tied to power/ground PG pin
 voltage_map 'gndo'. (LBDB-946)
```

What Next

Correct the voltage value of the insulated well PG pin's voltage_map.

LBDB-947

(warning) is an insulated well but not PG pin is tied to. The cell is being marked dont_touch/dont_use.

Description

This warning message occurs when the insulated substrate well PG pin do not tie off to other PG pin.

For a insulated substrate well PG pin, it must be tied off to a power/ground PG pin.

Feedback

The cell is black box for the multivoltage flow and is marked as dont_touch, dont_use (d,u). It cannot be recognized during functional optimization by the tools (Power Compiler and IC Compiler).

The following example shows an instance where this message occurs:

```
library(insulatedPgpin) {
 ...

   voltage_map (vdd, 1.0);
   voltage_map (gnd, 0.0);
   voltage_map (vddo, 1.0);
   voltage_map (gndo, 0.0);
   voltage_map (vdds, 0.0);
   voltage_map (gnds, 1.0);
   voltage_map (vdds', 1.0);
   voltage_map (gnds', 0.0);
cell (insulated_well) {
   area : 0.3264;

    pg_pin(vdds') {
    pg_type : nwell;
    voltage_name : vdds';
    is_insulated : TRUE;
    direction : internal;
/*    physical_connection : device_layer;*/
    }
    }
} /* end library */
```

The following is an example message:

```
Warning: Line 65, Cell 'insulated_well', pin 'vdds'' is an insulated well
 but not PG pin is tied to. The cell is being marked dont_touch/dont_use.
 (LBDB-947)
```

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure the specified PG pins have the tied power/ground PG pin and run the command again.

LBDB-948

(error) Insulated substrate well PG pin is associated with an invalid pg_type.

Feedback

Description

This error message occurs when the insulated substrate well PG pin is associated with an invalid pg_type. The pg_type of a bias PG pin must be one of the predefined bias types: pwell, nwell, deeppwell, or deepnwell.

The following example shows an instance where this message occurs:

```
library(insulatedPgpin) {

   voltage_map (vdd, 1.0);
   voltage_map (gnd, 0.0);
   voltage_map (vddo, 1.0);
   voltage_map (gndo, 0.0);
   voltage_map (vdds, 0.0);
   voltage_map (gnds, 1.0);
   voltage_map (vdds', 1.0);
   voltage_map (gnds', 0.0);
cell (insulated_well) {
   area : 0.3264;


   pg_pin(gnds') {
    pg_type : internal_power;
    voltage_name : gnds';
    is_insulated : TRUE;
    tied_to : gndo;
    direction : internal;
    /*physical_connection : device_layer;*/
    }
  ...
  }
} /* end library */
```

The following is an example message:

```
Error: Line 54, Cell 'insulated_well', pin 'gnds'', Insulated substrate
 well PG pin is associated with an invalid pg_type. (LBDB-948)
```

What Next

Make sure the pg_type of the bias PG pin is one of the valid types listed above.

LBDB-949

(error) Exactly 5 measurement points are required for this vector group inside %s.

Description

When AWP mode is enabled on CCS noise modeling, each vector group inside a output_voltage_rise or output_voltage_fall group must have exactly 5 time-voltage point

Feedback

in waveform measurement. Note that time and voltage values are stored in "index_3" and "values" respectively.

The following example shows an instance where this message occurs:

```
ccsn_first_stage () {
    is_needed : "true";
    stage_type : "both";
    is_inverting : "true";
    miller_cap_fall : "0.00266914";
    miller_cap_rise : "0.00252059";
    output_voltage_rise() {
      vector("ccsn_ov") {
        index_1("0.01");
 index_2("0.0407");
        index_3("0.0137562, 0.0212768, 0.0403229, 0.0554306");
        values("0.081, 0.243, 0.567, 0.729");
      }
      ...
    }
    ...
  }
```

The following is an example message:

```
Error: Line 19484, Cell "test_ccsn", pin "z", Exactly 5 measurement
 points are required for this vector group in output_voltage_rise
```

What Next

Correct the problem in the characterization setup.

LBDB-950

(error) The 5 voltage points in this vector group is not consistent with those of the first group.

Description

When AWP mode is enabled on CCS Noise modeling, all measurements within an output_voltage_rise or output_voltage_fall group must have the same voltage values. Note that voltage values are store in attribute "values" of a "vector" group.

The following example shows an instance where this message occurs:

```
voltage_map("vddfx", 0.8100);
  ...
  cell (test) {
    ...
    pin (z) {
      direction : output;
      related_power_pin : vddfx;
```

Feedback

```
      ...
      ccsn_last_stage () {
        is_needed : "true";
        stage_type : "both";
        is_inverting : "true";
        miller_cap_fall : "0.00266914";
        miller_cap_rise : "0.00252059";
        output_voltage_rise() {
          vector("ccsn_ov") {
            index_1("0.01");
          index_2("0.0407");
            index_3("0.0137562, 0.0212768, 0.0299644, 0.0403229,
0.0554306");
            values("0.081, 0.243, 0.405, 0.567, 0.729");
          }
  vector("ccsn_ov") {
            index_1("0.01");
            index_2("0.0263933");
            index_3("0.0150596, 0.0229561, 0.0316666, 0.0417733,
0.0562343");
            values("0.091, 0.253, 0.410, 0.562, 0.719");
          }
        ...
      }
    ...
```

The *"values"* attributes have different numbers.

The following is an example message:

```
Error: Line 19484, Cell "test_ccsn", pin "z", the 5 voltage points given
 in the "values" attribute should be of specific values.
```

What Next

Correct the problem in the characterization setup.

LBDB-951

(warning) The 5 voltage points should be of specific values in %s group.

Description

When AWP mode is enabled on CCS noise modeling, the five voltage points (stored in attribute "values") in each vector group of output_voltage_rise group should be 10%, 30%, 50%, 70%, 90% of Vdd, and for output_voltage_fall group, 90%, 70%, 50%, 30%, 10% of vdd.

The following example shows an instance where this message occurs:

```
voltage_map("vddfx", 0.8100);
  ...
```

Feedback

```
 cell (test) {
   ...
   pin (z) {
     direction : output;
     related_power_pin : vddfx;
     ...
     ccsn_last_stage () {
       is_needed : "true";
       stage_type : "both";
       is_inverting : "true";
       miller_cap_fall : "0.00266914";
       miller_cap_rise : "0.00252059";
       output_voltage_rise() {
         vector("ccsn_ov") {
           index_1("0.01");
         index_2("0.0407");
           index_3("0.0137562, 0.0212768, 0.0299644, 0.0403229,
0.0554306");
           values("0.089, 0.243, 0.405, 0.567, 0.729");
         }
         ...
       }
output_voltage_fall() {
  vector("ccsn_ov") {
           index_1("0.01");
           index_2("0.0263933");
           index_3("0.0150596, 0.0229561, 0.0316666, 0.0417733,
0.0562343");
           values("0.729, 0.567, 0.405, 0.243, 0.089");
         }
       ...
     }
   ...
```

The following is an example message:

```
Error: Line 19484, Cell "test_ccsn", pin "z", the 5 voltage points given
 in the "values" attribute should be of specific values.
```

What Next

Correct the problem in the characterization setup.

LBDB-952

(warning) Incomplete when condition coverage for CCS receiver capacitance model%s.

Description

This warning message occurs when pin-based/arc-based receiver capacitance has incomplete "when" condition coverage. To be more specific, for input/inout pin has

pin-based receiver capacitance, or the timing arc from this pin has arc-based receiver capacitance: 1. If default receiver capacitance exists on pin (without when), skip checking. 2. If receiver capacitance exists on default timing arc, skip checking. 3. Combine all pin-based when condition and arc-based when condition for each input->output arc respectively, it should be a complete set. 4. warning will be issued for in-complete states. Note: if there is no arc-based receiver capacitance, the message will be issued on input pin. Or else, the message will be issued on output pin.

The following example shows an instance where this message occurs:

```
...
    pin(I) {
      direction : input ;
      receiver_capacitance () {
        when : "A*!B";
        ...
      }
      receiver_capacitance () {
        when : "!A*B";
        ...
      }
      /*
      receiver_capacitance () {
        when : "!A*!B";
        ...
      }
      */
    }
    pin(Z) {
      direction : output ;
      function : "A*B*I" ;
      timing() {
        related_pin : "I" ;
        when : "A*B";
        receiver_capacitance_*() {...}
        ...
      }
    }
    ...

In the example above, input pin"I" does not have a receiver capacitance
 model
for the when condition "!A*!B".

The following is an example message:
The following is an example of the warning message:

Warning: Line 206, cell 'test', pin 'Z', Incomplete when condition
 coverage for CCS receiver capacitance model of related_pin 'I'.
 (LBDB-952)
```

Feedback

What Next

Complete the receiver model. Either introduce a receiver capacitance model with the missing "when" condition, or add a default model (without the "when" attribute). If the timing modeling comes from the timing characterization tool, check with the timing characterization tool to determine why this type of data was generated.

LBDB-953

(warning) CCS/CCB noise output DC swing (%g, %g) is not within %.1f%% of rail voltages (%g, %g)

Description

For a normal CMOS circuit, the DC output swing is rail to rail. This CCS/CCB noise tage has abnormal output swing according to its dc_current table.

If either the output low has a significant offset to ground, or the output high has a significant droop with respect to Vdd, or both, the output is deemed to have inadequate swing. The problem may be caused by cell characterization issues using improper supply voltage, or it may be due to serious DC leakage in the design. An LBDB-706 error may also be reported.

If the output high is larger than Vdd, the problem is caused by improper voltage used in cell characterization.

Note that if the stage_type attribute is "pull_up" or "pull_down", the output starting voltage is not analyzed, and assumed to be 0 or Vdd respectively.

The following is an example message:

```
Error: Line 1934, Cell "test", pin "a", DC output swing (0.023, 0.849) is
not within 5.0% of rail voltages (0.0, 0.9);
```

What Next

SolvNet article 2069871 has explanation about LBDB-706. Apply the same demonstration of example 4 using the dc_current group where one of the LBDB-706/LBDB-953 occurs to understand why the CCS/CCB noise output DC swing is not within 5% of rail voltages.

LBDB-954

(error) an invalid zero or negative capacitance value of '%s' is found.

Description

This message indicates zero or negative value is found of the capacitance attributes.

Feedback

This checker is triggered when lc_enable_10nm_mode set true, and capacitance attributes are specified under connected input pin, otherwise it's skipped and another warning message LBDB-163 reported.

Consider of single precision for values stored in .db, the checker uses a tolerance of 1e-6, if value < 1e-6, LC treats it less than or equal to 0.

LC checks these capacitance values:

Pin level attributes: capacitance, rise_capacitance, fall_capacitance:

There is a special case: when there is no pin capacitance attribute defined in .lib, and library level input/inout/outpu default capacitances equal to zero, e.g. library (my_library) { default_input_pin_cap : 0 ; default_output_pin_cap : 0 ; default_inout_pin_cap : 0 ; .... cell (my_cell) { ... pin (ABC) { direction : input; /* no capacitance attribute defined */ ... } /* end pin 'ABC' */ } /* end cell */ } In this case, input pin 'ABC' capacitance will inherit from library level attribute "default_input_pin_cap" which happens to be zero with a LBDB-172 warning, e.g. Warning: Line 100, Cell 'my_cell', pin 'ABC', The 'capacitance' attribute is not specified. Using 0.00. (LBDB-172)

Then LBDB-954 error will be reported for pin 'ABC' capacitance. Users can define pin capacitance attribute to override the value in library "default_input_pin_cap".

The following example shows an instance where this message occurs:

```
pin (I) {
…
direction : input;
capacitance : 0.0; /*wrong*/
rise_capacitance: 0.0000001; /*<1e-6, wrong*/
fall_capacitance: 0.001; /*correct*/
}
```

The following is an example message:

```
Error: Line 385, Cell 'HP_SHDFFNX1', pin 'I', an invalid zero or negative
 capacitance value of 'capacitance' is found. (LBDB-954)
Error: Line 386, Cell 'HP_SHDFFNX1', pin 'I', an invalid zero or negative
 capacitance value of 'rise_capacitance' is found. (LBDB-954)
```

What Next

Change the value of the attributes to positive, make sure value >= 1e-6.

LBDB-954w

(warning) an invalid zero or negative capacitance value of '%s' is found.

Feedback

Description

This message indicates zero or negative value is found in the capacitance model.

Consider of single precision for values stored in .db, the checker uses a tolerance of 1e-6, if value < 1e-6, LC treats it less than or equal to 0 .

LC checks these capacitance values:

1. the first value of N-cap model under pin or timing level.
2. receiver_capacitance1_rise|fall value under pin or timing level.
3. miller_cap_rise/miller_cap_fall under first/last_ccsn_stage or input/output_ccb group, this checker is controlled by lc_enable_10nm_mode.

The following example shows an instance where this message occurs:

```
pin(I)  {
   ...
receiver_capacitance() {
 receiver_capacitance1_fall(LTT1) {
 index_1 ("0.05,0.075,0.100,0.225,0.400");
 values (\
 "0.0,1.960000e-03,1.992000e-03,2.031000e-03,2.185000e-03"\
 );
}
pin(Z)  {
    direction : output;
    function : "I";
    timing() {
      related_pin : "I";
 ...
 receiver_capacitance1_fall (LTT2) {
 index_1 ("0.05,0.075,0.100,0.225,0.400");
 index_2 ("0.010,0.025,0.040,0.075");
 values (\
 "1.947000e-03,1.959000e-03,1.988000e-03,2.016000e-03",\
 "1.960000e-07,1.969000e-03,1.994000e-03,2.020000e-03",\
 "1.992000e-03,1.997000e-03,2.012000e-03,2.030000e-03",\
 "2.031000e-03,2.032000e-03,2.035000e-03,2.043000e-03",\
 "2.185000e-03,2.184000e-03,2.179000e-03,2.171000e-03"\
 );
 }
```

The following is an example message:

```
Warning: Line 374, Cell 'BUFFD0', pin 'I', an invalid zero or negative
 capacitance value of 'receiver_capacitance1_fall' is found. (LBDB-954w)
Warning: Line 415, Cell 'BUFFD0', pin 'Z', an invalid zero or negative
 capacitance value of 'receiver_capacitance1_fall' is found. (LBDB-954w)
```

Feedback

What Next

Change the value of the attributes to positive, make sure value >= 1e-6.

LBDB-955

(warning) an illegal value of '%s' %f is found, it cannot be %s than \ '%s' value '%s %f'.

Description

```
This message indicates that the values of all capacitance
 models/attributes is not correct.

the capacitance values should meet the following 4 rules:

C1 = receiver_capacitance1_[rise|fall] values
C2 = receiver_capacitance2_[rise|fall] values
Cmiller_rise = miller_cap_rise value
Cmiller_fall = miller_cap_fall value

pin_capacitance = rise_capacitance or fall_capacitance or if missing, use
 pin capacitance

1. C1 < (2 * pin_capacitance);
2. C2 <= (5 * pin_capacitance)
3. Cmiller_rise/fall >= 10% * pin_capacitance;
4. Cmiller_rise/fall < pin_capacitance;
```

The following example shows an instance where this message occurs:

```
pin(I)  {
    direction : input;
    capacitance : 0.002;
    receiver_capacitance() {
 receiver_capacitance1_rise(LTT1) {
 index_1 ("0.05,0.075,0.100,0.225,0.400");
 values (\
 "0.002,0.005,1.992000e-03,2.031000e-03,2.185000e-03"\
 );
}
```

The following is an example message:

```
Warning: Line 364, Cell 'BUFFD0', pin 'I', an illegal value of 'values'
 0.005000 is found, it cannot be more than '2 * capacitan' value '2 *
 0.002000'. (LBDB-955)
```

What Next

Change the value of the attributes to meet the screener rules.

Feedback

LBDB-956

(warning) 'miller_cap_rise' cannot more than 5 times value of 'miller_cap_fall'.

Description

This message indicates that the difference of miller_cap_rise and miller_cap_fall is wrong.Cmiller_rise/Cmiller_fall must be less than 5.

The following example shows an instance where this message occurs:

```
pin(I) {
      direction : input;
      max_transition : 2100.0;
      capacitance : 0.002000;
      fanout_load : 1;

      /* test pin-level */
        ccsn_first_stage ( ) {
          is_needed     : true;
          is_inverting    : true;
          stage_type      : both;
          miller_cap_rise : 0.0021;
          miller_cap_fall : 0.0002;
    ...
  }
```

The following is an example message: Warning: Line 106, Cell 'inv0d0', pin 'I', 'miller_cap_rise' cannot more than 5 times value of 'miller_cap_fall'. (LBDB-956)

What Next

Change the value of the attributes to non-zero, make sure Cmiller_rise/Cmiller_fall < 5.

LBDB-957

(warning) No driver waveform defined in the %s.

Description

In cell characterization, the shape of the Waveform driving the characterized circuit can have a significant impact on the final results.

This message is reported when there is no "normalized_driver_waveform" group defined in the library. Or there is normalized_driver_waveform group in library, but a library cell does not have driver waveform defined By any of following cell level or pin level attributes: driver_waveform, driver_waveform_rise and driver_waveform_fall.

The checkers is for 10nm library.

Feedback

The following is an example message:

```
Missing normalized_driver_waveform in library:
Warning: Line 6, No driver waveform defined in the library. (LBDB-957)

Missing driver_waveform, driver_waveform_rise, driver_waver_fall in cell:
Warning: Line 594, Cell 'TCAINVXC', No driver waveform defined in the
 cell. (LBDB-957)
```

What Next

Define normalized_driver_waveform group in library or define driver_waveform, driver_waveform_rise, driver_waver_fall in cell or pin level.

LBDB-958

(warning) dc_current values not correct for tied output

Description

For an output pin that is tied to low or high, the dc_current table of its ccsn_last_stage must be of a special form. In a strict sense, this ccsn stage does not have an input (because the function is 0 or 1). To conform the current data to the input/output format, we repeat the same values for all input voltages, as shown below:

```
dc_current {
   ...
   values( \\
      "0.0672194, 0.0647206, 0.0628569, 0.0621341 ..." \\
      "0.0672194, 0.0647206, 0.0628569, 0.0621341 ..." \\
      "0.0672194, 0.0647206, 0.0628569, 0.0621341 ..." \\
      ...)
   ...
}
```

The following is an example message:

```
Warning: Line 214, Cell 'hptiehi', pin 'Z', dc_current values not correct
 for tied output. (LBDB-958)
```

What Next

Review the "values" attribute of the affected "dc_current" group, root cause the differences in row values, and re-characterize with correct settings.

LBDB-959

(warning) suspicious dc_current value (%g) detected at row %d, entry %d

Feedback

Description

The "values" attribute in dc_current group contains complex, two-dimensional numerical data. A potentially bad value has been identified at the shown location. An example is given below:

```
dc_current {
   ...
   values( \\
      "0.270561, 0.111316, ... 0.0110591, -1.465e-05, ...",\\ (1st row)
      ...
      "0.348481, 0.137316, ... -0.0899564, 1.45095e+31, ...", \\ (25th
 row)
      ...)
   ...
}
```

The 23rd entry of the 25th row is abnormally large (1.45095e+31). A subsequent LBDB-706 error is possible.

The following is an example message: Warning: Line 120, Cell 'inv', pin 'Z', suspicious dc_current value (1.45095e+31) detected at row 25, entry 23 (LBDB-959)

What Next

Review the "values" attribute of the affected "dc_current" group. Re-generate the library with corrected data.

LBDB-960

(error) "%s" is not a valid characterization model for %s%s.

Description

This error is issued when <char_model> is not one of the valid enumerated values for all attributes, a specific attribute, or a specific value of a atribute.

The following is an example message:

```
Error: Line 10, "invalid_char_model" is not a valid characterization
 model for all attributes. (LBDB-960)
```

What Next

Check the library source file, correct the <char_model> definition.

LBDB-961

(warning) Attribute driver_waveform, driver_waveform_rise, driver_waveform_fall defined outside of char_config group.

Feedback

Description

This error is issued when char_config is defined but there is driver_waveform, driver_waveform_rise, driver_waveform_fall defined outside of char_config group.

If char_config is defined, all driver_waveform attributes should be defined inside char_config group.

The following is an example message:

```
Warning: Line 10, Attribute driver_waveform, driver_waveform_rise,
 driver_waveform_fall defined outside of char_config group. (LBDB-961)
```

What Next

Check the library source file, remove driver_waveform attributes which defined outside char_config group.

LBDB-962

(error) "%s" is not a valid selection method.

Description

For these two attributes:

default_value_selection_method(<char_model>, <method>);
merge_selection(<char_model>, <method>);

This error is issued when <method> is not one of these enumerated values: any min max average min_mid_table max_mid_table follow_delay

The following is an example message:

```
Error: Line 10, "invalid_method" is not a valid selection method.
 (LBDB-962)
```

What Next

Check the library source file, correct the <method> definition.

LBDB-963

(warning) Missing driver_waveform_name in normalized_driver_waveform group.

Description

When char_config() group is defined, the default driver_waveform should be defined by using "all" as <char_model> in driver_waveform definition. In this case, all normalized_driver_waveform group should have a driver_waveform_name.

Feedback

The following is an example message:

```
Warning: Line 10, Missing driver_waveform_name in
 normalized_driver_waveform group. (LBDB-963)
```

What Next

Check the library source file, either add driver_waveform_name to all normalized_driver_waveform group, or delete the normalized_driver_waveform which do not have driver_waveform_name.

LBDB-964

(warning) default char_config attribute %s is not defined for the library.

Description

For characterization configuration, each attribute may have a default value in the library level. If it is intended not to use a default value for the whole library, this warning can be ignored.

The following is an example message:

```
Error: Line 10, default char_config attribute dirver_waveform for nldm
 model is not defined for the library. (LBDB-964)
```

What Next

Check the library source file, define the default attribute for the library.

LBDB-965

(warning) default char_config attribute %s is not defined for the library when "%s" is defined.

Description

This is for when a default char_config attribute is required defined for the library but is not defined. Sometimes a default attribute is required to be defined if char_config group is used. Sometimes a default attribute is required to be defined if another default attribute is defined.

The following is an example message:

```
Warning: Line 10, default "ccs_timing_segment_voltage_tolerance_rel"
 attribute is not defined for the library when char_config is defined.
 (LBDB-965)
```

Feedback

What Next

Check the library source file, define the default attribute for the library.

LBDB-966

(information) The '%s' pg_pin is not '%s' of any signal \n \t pin on the cell.

Description

This information is issued when a pg_pin group satisfies the following conditions: - the pg_pin must be a 'primary_power' or 'primary_ground' pg_pin. - the pg_pin must be a 'std_cell_main_rail' pg_pin. - if the pg_pin is 'primary_power', the pg_pin is not the related power pin of any signal pin. - if the pg_pin is 'primary_ground', the pg_pin is not the related ground pin of any signal pin. The 'voltage_name' is optional for this pg_pin.

The following example shows an instance where this message occurs:

```
cell(ls) {
    is_level_shifter : true;

    pg_pin(VDD) {
        voltage_name : VDDL;
        pg_type : primary_power;
        std_cell_main_rail : true;
    }
    ...
  }
```

The following is an example message:

```
Information: Line 84, The 'VDD' pg_pin is not a 'related_power_pin'
 pg_pin of any signal pin on the cell. (LBDB-966)
```

What Next

If any screener rule fails on 'voltage_name', delete the 'voltage_name' under the pg_pin.

LBDB-967

(error) The delay trip point "%s" is not in the range between slew lower trip point "%s" and slew upper trip point "%s".

Description

This message indicates that the attribute value you have specified is not in the required range. For the 4 delay trip point attributes below, their value should be in the range of slew lower and upper trip point. input_threshold_pct_rise input_threshold_pct_fall output_threshold_pct_rise output_threshold_pct_fall

Feedback

Below are the attributes for slew upper/lower trip point. slew_lower_threshold_pct_rise slew_upper_threshold_pct_rise slew_lower_threshold_pct_fall slew_upper_threshold_pct_fall

For example: slew_lower_threshold_pct_rise < input_threshold_pct_rise < slew_upper_threshold_pct_rise slew_lower_threshold_pct_fall < input_threshold_pct_fall < slew_upper_threshold_pct_fall slew_lower_threshold_pct_rise < output_threshold_pct_rise < slew_upper_threshold_pct_rise slew_lower_threshold_pct_fall < output_threshold_pct_fall < slew_upper_threshold_pct_fall

The following example shows an instance where this message occurs:

```
library (test) {
    slew_lower_threshold_pct_rise : 30.0;
    slew_upper_threshold_pct_rise : 70.0;
    slew_lower_threshold_pct_fall : 30.0;
    slew_upper_threshold_pct_fall : 70.0;
    input_threshold_pct_rise : 50.0;
    input_threshold_pct_fall : 50.0;
    output_threshold_pct_rise : 50.0;
    output_threshold_pct_fall : 80.0;

  }
```

To correct the error, change the output_threshold_pct_fall to 50.0, which is in the range of (30.0 ~ 70.0)

The following is an example message:

```
Error: Line 30, The delay trip point "output_threshold_pct_fall" is not
 in the range between
  slew lower trip point "slew_lower_threshold_pct_fall" and slew upper
 trip point
  "slew_upper_threshold_pct_fall". (LBDB-967)
```

What Next

Check the library source file, and ensure the attribute value is consistent with corresponding range.

LBDB-968

(Error) This %s group does not have a driver waveform associated with input %s.

Description

This library uses input_ccb and output_ccb for noise/timing applications, instead of ccsn_first_stage and ccsn_last_stage. An associated change is that all output_voltage_rise &_voltage_fall data (in input_ccb & output_ccb) are obtained with a driver waveform that is consistent with timing characterization.

Feedback

The driver waveform must be specified at the pin or cell level using driver_waveform, driver_waveform_rise, or driver_waveform_fall attribute. If these attributes are missing, a default normalized_driver_waveform group (without the "driver_waveform_name" attribute) needs to be present at the library level.

This message indicates the above search fails to find a waveform.

Examples

Line 786, Cell 'inv0d0', pin 'ZN', This output_ccb group does not have a driver waveform associated with input fall. (LBDB-968)

What Next

Check the library source file, add an appropriate cell-level driver_waveform attribute or a default normalized_driver_waveform group at the library level.

LBDB-969

(error) The '%s' group should not be used in a non-retention cell.

Description

This error message occurs because user specifies following groups in a non-retention cell. retention_condition clock_condition clear_condition preset_condition Retention cell must have cell level attribute "retention_cell", otherwise it is a non-retention cell. These groups can only work in a retention cell.

The following example shows an instance where this message occurs: In the following example, there is a *retention_condition* group, but there is no *retention_cell* attribute. Remove the comment from the *retention_cell* attribute to correct the problem.

```
cell(retention_dff) {
  ...
  /* retention_cell : "my_retention_dff"; */

  retention_condition() {
    required_condition : "!sleep";
    power_down_function : "!vcc+vss" ;
  }

}
```

The following is an example message: The above example results in the following error message:

```
Error: Line 192, Cell 'retention_latch_with_async_preset_clear', The
 'retention_condition'
  group should not be used in a non-retention cell. (LBDB-969)
```

Feedback

What Next

Resolve the issue by either removing these groups or adding a *retention_cell* attribute.

LBDB-970

(error) Invalid parent group '%s' of the user defined %s '%s'.

Description

This message indicates that the group where the user defined attribute belongs to is not valid.

The following example shows an instance where this message occurs:

```
library(test) {
  define(user_defined_attribute, user_defined_group, string);
  define_group(another_user_defined_group, user_defined_group);
  ...
}
```

The following is an example message:

```
Error: Line 2, Invalid parent group 'user_defined_group' of the user
 defined attribute 'user_defined_attribute'.  (LBDB-970)
Error: Line 3, Invalid parent group 'user_defined_group' of the user
 defined group 'another_user_defined_group'.  (LBDB-970)
```

What Next

Check the parent group, define it before this line or fix the group name it is a typo.

LBDB-971

(error) User defined group '%s' cannot use the same name as its parent group.

Description

This message indicates that the user defined group is using same name as its parent group in define_group function.

The following example shows an instance where this message occurs:

```
library(test) {
  define_group(user_defined_group, library);
  define_group(user_defined_group, user_defined_group);
  ...
}
```

The following is an example message:

```
Error: Line 2, User defined group 'user_defined_attribute' cannot use the
 same name as its parent group.  (LBDB-971)
```

What Next

Check the define_group, using different name between the user defined group and its parent group.

LBDB-972

(error) The scan pin '%s' should not be used in the non-scan mode function.

Description

The test_cell is describing the non-scan mode of the scan cell, scan pin should not be used in the test_cell function. Only non-scan pin is allowed. Currently, scan input pin and scan enable pin is not allowed to be used in the ff group under test_cell.

The following example shows an instance where this message occurs:

```
cell(test) {
  ...
    test_cell() {
      ...
      pin(SD) {
        direction : input ;
        signal_type : test_scan_in ;
      }
      pin(SE) {
        direction : input ;
        signal_type : test_scan_enable ;
      }
      ...
      ff(IQ, IQN) {
        clocked_on : "CK" ;
        next_state : "((RT&((SE&SD)|(!SE&D))&SL)|(IQ&!RT&SL))" ;
      }
      ...
    }
  ...
}
```

In this case, the scan input pin "SD" and scan enable pin "SE" are used in the ff group "next_state" attribute inside test_cell. This is not allowed, user should correct the next_state attribute, remove the scan pin inside.

Feedback

The following is an example message:

```
Error: Line 2759, Cell 'scan_cell', test_cell, The scan pin 'SE' should
 not be used in the non-scan mode function. (LBDB-972)
Error: Line 2759, Cell 'scan_cell', test_cell, The scan pin 'SD' should
 not be used in the non-scan mode function. (LBDB-972)
```

What Next

Check the test_cell function and scan pin, remove the scan pin in function description.

LBDB-973

(error) Attribute '%s' should be '%s',\n \t\twhich is conflict with user sepcified info.

Description

For multibit scan cell with dedicated scan output pin, user should specify attribute "scan_start_pin" to indicate the scan chain direction, and attribute "scan_pin_inverted" to indicate if the scan signal shifting between sequential elements is inverted. In the mean time, LC will also auto-derive these two attributes. For each MB scan cell with auto-derived scan_start_pin/scan_pin_inverted, if user also specifies these attributes explicitly, a consistency check will be performed. This message reports the conflict if the user-given values are different from the derived values.

The following example shows an instance where this message occurs:

```
cell(test) {

  ...
  statetable (" D  CP  SE  SI " ,         "IQ IQN" )
    { table : " -  ~R     -    -  : - - :  N  N ,   \
                H/L  R     L   -  : - - : H/L H/L,  \
                 -   R   H  H/L  : - - : H/L L/H";
    }

  bundle(Q){
    scan_start_pin : Q1; /* This is wrong, should be Q0 */
    scan_pin_inverted : true;

    pin(Q0) {
      internal_node : "IQ" ;
      input_map : " D0  CP  SE  SI";
      ...
    }
    pin(Q1) {
      internal_node : "IQ" ;
      input_map : " D1  CP  SE  Q0";}
      ...
    }
    ...
```

```
  }
  pin(SO) {
    state_function : "SE * Q1" ;
    ...
  }
  ...
}
```

The attribute "scan_start_pin" should be "Q0"

The following is an example message:

```
Error: Line 437, Cell 'test', pin 'Q', Attribute 'scan_start_pin' should
 be 'Q0',
        which is conflict with user sepcified info.  (LBDB-973)
```

What Next

Check library file, correct attribute "scan_start_pin" and "scan_pin_inverted"

LBDB-974

(warning) The logic represented by the '%s' attribute (%s)\n \tis not equal or a subset of the logic represented by the '%s' attribute (%s)

Description

This error message indicates that the 'char_when', 'char_when_rise' or 'char_when_fall' attribute should be equal or a subset of the "when" attribute.

The following example shows an instance where this message occurs: The following example results in this warning. The "char_when" condition "A" in the receiver_capacitance is a superset of the "when" condition "A*B".

```
cell(bad) {
      Pin (A) {
         receiver_capacitance () {
            when : "A*B";
            char_when : "A";
            ...
         }
         ...
      }
      ...
   }
```

The following is an example message:

```
Warning: Line 84, The logic represented by the 'char_when' attribute (A)
        is not equal or a subset of the logic represented by the 'when'
 attribute (A*B). (LBDB-974)
```

Feedback

What Next

Check the library source file, and correct the incorrect attribute.

LBDB-975

(information) The "scan_start_pin" attribute is not needed for multi-bit function extraction and is ignored.

Description

This message indicates that the multi-bit scan cell can derive the mulbit-bit mapping info from cell function, attribute "scan_star_pin" is useless and should be removed from the cell. Attribute 'scan_start_pin' is only needed in multi-bit scan cell with single-bit scan output pin.

The following example shows an instance where this message occurs:

```
cell (test) {
  ...
  statetable (" D  CP SE SI ",         "QN   QT") {
     table : "  - ~R   -  -  : -  - :  N    N, \
                H/L R   L  -  : -  - : L/H  L/H, \
                  -  R   H H/L : -  - : L/H  H/L";
  }
  bundle(QN) {
    members (QN1, QN2);
    direction : output;
    scan_start_pin : QN1;
    ...
    pin(QN1) {
      internal_node : "QN";
      input_map : "D1 CP SE SI";
      max_capacitance : 0.0724592;
    }
    pin(QN2) {
      internal_node : "QT";
      input_map : "D2 CP SE QN1";
      max_capacitance : 0.0724218;
    }
  }

  /* no single-bit scan output pin */

  ...
}
```

The following is an example message:

```
Information: Line 303, Cell 'test', The "scan_start_pin" attribute is not
 needed for multi-bit function extraction and is ignored. (LBDB-975)
```

Feedback

What Next

Check the library source file, and remove attribute "scan_start_pin".

LBDB-976

(Warning) The multi-bit retention cell should be modeled with\n \treference_input attribute for multi-bit pin mapping.

Description

The mutli-bit retention scan cell must be modeled with 1-pair of sequential groups and reference_input, then the 1-pair of sequential can be used for the slice modeling for function processing. Warning if it is wrongly modeled with N-pairs sequential groups.

The multi-bit cell function cannotbe recognized by Design Compiler during banking/de-banking flow.

The following example shows an instance where this message occurs:

```
cell(test) {
  ...
    latch(iq1_1,iqn1_1) {
      enable : "(CK * RET)'" ;
      data_in : "D[0] * !SE + SI * SE" ;
      power_down_function : "!VDD+VSS" ;
    }
    latch(iq1_2,iqn1_2) {
      enable : "(CK * RET)" ;
      data_in : "iq1_1" ;
      power_down_function : "!VDDB+VSS" ;
    }
    latch(iq2_1,iqn2_1) {
      enable : "(CK * RET)'" ;
      data_in : "D[1] * !SE + iq1_2 * SE" ;
      power_down_function : "!VDD+VSS" ;
    }
    latch(iq2_2,iqn2_2) {
      enable : "(CK * RET)" ;
      data_in : "iq2_1" ;
      power_down_function : "!VDDB+VSS" ;
    }
    bundle(Q) {
   members(Q[0], Q[1]);
   direction : output ;
   pin(Q[0]) {
    function : iq1_2;
        ...
   }
   pin(Q[1]) {
    function : iq2_2;
```

```
        ...
    }
  }
  ...
}
```

In this case, the cell is using 2 pairs of latch groups (4 latches), which can't be analyaze in function processing. User should correct the cell modeling with 1-pair of latch groups and reference_input as below.

```
cell(test) {
  ...
    latch("pa pb", iq1, iqn1) {
      enable : "(CK * RET)'" ;
      data_in : "pa * !SE + pb * SE" ;
    power_down_function : "!VDD+VSS" ;
    }
    latch("pc", iq2, iqn2) {
      enable : "(CK * RET)" ;
      data_in : "pc" ;
    power_down_function : "!VDDB+VSS" ;
    }
   bundle(Q) {
   members(Q[0], Q[1]);
   direction : output ;
   pin(Q[0]) {
    function : iq2;
        reference_input : "QT[0]";
   }
   pin(Q[1]) {
    function : iq2;
        reference_input : "QT[1]";
   }
  }
    bundle(QT) {
   members(QT[0], QT[1]);
      direction : internal;
      pin(QT[0]) {
        reference_input : "D[0] SI";
        function : iq1;
      }
      pin(QT[1]) {
        reference_input : "D[1] Q[0]";
        function : iq1;
      }
    }
  ...
}
```

Feedback

The following is an example message:

```
Warning: Line 32, Cell 'MB2_scan_retention_1control_master_slave_design',
 The multi-bit retention cell should be modeled with
 reference_input attribute for multi-bit pin mapping. (LBDB-976)
```

What Next

Check the cell function, correct the cell modeling with reference_input.

LBDB-977

(warning) In attribute '%s', CCB groups '%s' and '%s' have different values for related_ccb_node.

Description

related_ccb_node of the CCB noise stages specified in propagating_ccb should be identical.

The following example shows an instance where this message occurs:

```
library(test) {
  cell (flop) {
    ...
    pin (CP) {
      ...
      input_ccb("CCB_CP2") {
        related_ccb_node : "net3:3";
      }
      ...
    }
    pin (Q) {
      ...
      output_ccb("CCB_Q1") {
        related_ccb_node : "net7:5";
      }
      timing () {
        related_pin : CP;
        active_input_ccb ("CCB_CP1");
        propagating_ccb("CCB_CP2", "CCB_Q1");
      }
      ...
    }
    ...
  }
}
```

The following is an example message:

```
Warning: Line 32, In attribute 'propagating_ccb', CCB groups 'CCB_CP2'
 and
 'CCB_Q1' have different values for related_ccb_node.
```

What Next

Use same values for the related_ccb_node of the CCB noise stages specified in propagating_ccb.

LBDB-978

(error) Old CCSN stage noise model cannot co-exist with new CCB noise model.

Description

If the presence of input_ccb or output_ccb is detected, the library is assumed to use the new CCB format. Any ccsn_first_stage or ccsn_last_stage will trigger an error.

The following is an instance where this error occurs:

```
library (test) {
  ...
  cell (flop) {
    pin (D) {
      input_ccb("CCB_D1") {
        is_needed : true;
        related_ccb_node : "net1:5";
      }
      ccsn_first_stage() {
        is_needed : true;
        related_ccb_node : "net1:5";
      }
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 9, Cell 'flop', pin 'D', Old CCSN stage noise model cannot
 co-exist
with new CCB noise model. (LBDB-978)
```

What Next

Use either old CCSN stage noise model or new CCB noise model.

Feedback

LBDB-979

(warning) attribute '%s'. '%s' stage at\ line %u has a value (%g) in '%s/vector/%s' (line %u) that does\ not match any values of '%s' in '%s' at line %u.

Description

In the referenced ccs noise data modeling, output_voltage_rise and output_voltage_fall are characterized in ways to be closer to timing behavior. Their "input slew" (vector/index_1) and "output load" (vector/index_2) values form a 2D grid, similar to various timing lookup tables.

To best match timing behavior, the ccb's referenced by the 'propagating_ccb' attribute need to meet the following guideline on input slew and output load values:

The starting/ending values must match those of NLDM delay data (cell_rise/cell_fall). See LBDB-980

Intermediate values may be sparse, but they have to match some entries in the delay data.. This message, LBDB-979, addresses the mimsatch.

Note that there is a different requirement one the output load of input_ccb in an input_ccb/output_ccb two-stage configuration. See LBDB-588.

The following example shows an instance where this message occurs:

```
library(test) {
  ...
  normalized_driver_waveform(ndw1) {
    driver_waveform_name : "driver_waveform_default_fall" ;
    index_1("0.003209, 0.0133113, 0.033516, 0.0726625, 0.152218,
 0.31133");
    ...
  }
  ...
  cell (flop) {
    ...
    pin(A) {
      ...
      driver_waveform_fall : driver_waveform_default_fall ;
      ...
      input_ccb(ccb1) {
        ...
        output_voltage_fall() {
          vector(vec1) {
            index_1("0.013209");
            ...
          }
          ...
        }
        ...
```

Feedback

```
        }
      ...
      }
      pin (Y) {
        ...
        timing() {
          related_pin : "A" ;
          ...
          propagating_ccb(ccb1, ccb2);
        }
        ...
      }
      ...
    }
}
```

Examples

Warning: Line 10287, Cell 'xyz', pin 'nx2', attribute 'propagating_ccb'. 'input_ccb' stage at line 2321 has a value (0.005) in 'output_voltage_rise/vector/index_1' (line 2380) that does not match any values of 'index_1' in 'cell_fall' at line 9728. (LBDB-979)

What Next

Correct the characterization procedure.

LBDB-980

(warning) attribute '%s'. '%s' stage at line %u has a %s value (%g) in '%s/vector/%s' (line %u) that does not match the %s value of '%s' in '%s' at line %u.

Description

In the referenced ccs noise data modeling, output_voltage_rise and output_voltage_fall are characterized in ways to be closer to timing behavior. Their "input slew" (vector/index_1) and "output load" (vector/index_2) values form a 2D grid, similar to various timing lookup tables.

To best match timing behavior, the ccb's referenced by the 'propagating_ccb' attribute need to meet the following guideline on input slew and output load values:

The starting/ending values must match those of NLDM delay data (cell_rise/cell_fall). This message, LBDB-980, addresses the mismatch.

Intermediate values may be sparse, but they have to match some entries in the delay data. See LBDB-979.

Note that there is a different requirement one the output load of input_ccb in an input_ccb/output_ccb two-stage configuration. See LBDB-588.

Feedback

The following example shows an instance where this message occurs:

```
library(test) {
  ...
  normalized_driver_waveform(ndw1) {
    driver_waveform_name : "driver_waveform_default_fall" ;
    index_1("0.003209, 0.0133113, 0.033516, 0.0726625, 0.152218");
    ...
  }
  ..
  cell (flop) {
    ...
    pin(A) {
      ...
      driver_waveform_fall : driver_waveform_default_fall ;
      ...
      input_ccb(ccb1) {
        ...
        output_voltage_fall() {
          vector(vec1) {
            index_1("0.002209");
            ...
          }
          ...
        }
        ...
    }
    ...
    pin (Y) {
      ...
      timing() {
        related_pin : "A" ;
        ...
        propagating_ccb(ccb1, ccb2);
      }
      ...
    }
    ...
  }
}
```

Examples

Warning: Line 7492, Cell 'xyz', pin 'nx2', attribute 'propagating_ccb'. 'input_ccb' stage at line 488 has a min value (0.005) in 'output_voltage_rise/vector/index_1' (line 561) that does not match the first value of 'index_1' in 'cell_fall' at line 6933. (LBDB-980)

What Next

Correct the characterization procedure.

Feedback

LBDB-981

(warning) For the referenced ccs noise data modeling, each delay timing arc needs to have valid CCB model.

Description

```
For the referenced ccs noise data modeling, each delay timing arc needs
 to have:
1.  at least one active input_ccb which is being referenced by
 active_input_ccb
or propagating_ccb
2.  one or two active output_ccb which is being referenced by
 active_output_ccb
or propagating_ccb, in case of two output_ccb, one is of
 stage_type:pull_up, the
other is of stage_type:pull_down
If any of above is not satisfied, the warning is issued.
```

The following example shows an instance where this message occurs:

```
library(test981) {
  ...
  cell(BUF) {
    pin(Z) {
      timing() {
      }
      output_ccb(BUFX) {
      ...
      }
    }
  }
}
```

The following is an example message:

```
Warning: Line 223, Cell 'BUF', pin 'Z', For the referenced ccs noise data
modeling, each delay timing arc needs to have valid CCB model. (LBDB-981)
```

What Next

Resolve the issue by providing appropriate CCB combinations for each timing.

LBDB-982

(warning) is a '%s' class retention pin but is missing all recommended attributes.

Description

This message occurs in either of following situations: 1. Missing following 'save' related retention attributes in a save class retention pin. save_action save_condition

Feedback

1. Missing following 'restore' related retention attributes in a restore class retention pin. restore_action restore_condition restore_edge_type
2. Missing following 'save' or 'restore' related retention attributes in a save_restore class retention pin. save_action save_condition restore_action restore_condition restore_edge_type

The following example shows an instance where this message occurs: In the following example, this pin is a *save* class retention pin, but retention attributes *save_action* and *save_condition* are missing. To correct the problem, add both *save_action* and *save_condition* in this retention pin.

```
cell(retention_dff) {
  ...
  retention_cell : "my_retention_dff";

  pin(SAVE) {
    retention_pin (save, 1);
    /* save_action : L; */
    /* save_condition : CK; */
  }

}
```

The following is an example message: The above example results in the following error message:

```
Warning: Line 192, Cell 'retention_dff', Pin 'SAVE', is a 'save' class
 retention pin but is missing all recommended attributes.(LBDB-982)
```

What Next

Resolve the issue by add the missing retention attributes in the retention pin.

LBDB-983

(warning) Found inconsistency between attribute '%s' and retention pin disable value.

Description

Retention pin disable value and save_action/restore_action must be consistent as below: 1. For a save class retention pin When save_action is "L" or "R", disable value should be "1" When save_action is "H" or "F", disable value should be "0" 2. For a restore class retention pin When restore_action is "L", disable value should be "1" When restore_action is "H", disable value should be "0" When restore_action is "R", and restore_edge_type is "leading", disable value should be "0" When restore_action is "F", and restore_edge_type is "leading", disable value should be "1" When restore_action is "R", and restore_edge_type is "trailing" or missing, disable value should be "1" When

Feedback

restore_action is "F", and restore_edge_type is "trailing" or missing, disable value should be "0"

The following example shows an instance where this message occurs: In the following example, this pin is a *save* class retention pin, and *save_action* is 'L', but the disable value is not '1'. To correct the problem, change disable value to '1'.

```
cell(retention_dff) {
  ...
  retention_cell : "my_retention_dff";

  pin(SAVE) {
    retention_pin (save, 0);
    save_action : L;
    save_condition : CK;
  }

}
```

The following is an example message: The above example results in the following error message:

```
Warning: Line 192, Cell 'retention_dff', Pin 'SAVE', Found inconsistency
 between attribute 'save_action' and retention pin disable
 value.(LBDB-983)
```

What Next

Resolve the issue by correct the save_action/restore_action attribute or retention pin disable value.

LBDB-984

(warning) Missing attribute required_condition under retention_condition group of the zero-pin retention cell, this cell will be black-box for multi-voltage functional flow. It is marked as dont_touch and dont_use.

Description

```
For zero-pin retention cell, user must specify group retention_condition
and sub-attribute required_condition, otherwise the cell will be marked
as black-box.
This attribute is important to client tools in power opimization flow.
```

The following example shows an instance where this message occurs:

```
library(test) {
 ...
  cell (zpr) {
    ...
    latch(IQ1,IQN1) {
```

Feedback

```
      enable : "!clk" ;
      data_in : "d" ;
      power_down_function : "!vcc+vss" ;
    }
    latch(IQ2,IQN2) {
      enable : "clk" ;
      data_in : "IQ1" ;
      power_down_function : "!vcc_in+vss" ;
    }

    retention_condition() {
      /* required_condition : "!clk"; */
      power_down_function : "!vcc+vss" ;
    }

    ...
  }
}
```

The following is an example message:

```
Warning: Line 3, Cell 'zpr', Missing attribute required_condition under
 retention_condition group
of the zero-pin retention cell, this cell will be black-box for
 multi-voltage
functional flow. It is marked as dont_touch and dont_use. (LBDB-984)
```

What Next

```
Add the missing retention_condition and sub-attribute required_condition
```

LBDB-985

(error) The pin '%s' specified in required_condition attribute should be an input signal pin powered by backup power or backup ground.

Description

```
For zero-pin retention cell, the pins specified in required_condition
 attribute
must be input signal pins powered by backup_power or backup_ground.

For other types of retention cell (like 1-pin or 2-pin), the pins
 specified in
required_condition attribute must be retention pins, or input signal pins
 powered by
backup_power or backup_ground.
```

The following example shows an instance where this message occurs:

```
library(test) {
 ...
```

Feedback

```
  cell (zpr) {
    ...
    pin(clk) {
      direction : input ;
      related_ground_pin : VSS ;
      related_power_pin : VDD_BAK ;
      ...
    }

    pin(d) {
      direction : input ;
      related_ground_pin : VSS ;
      related_power_pin : VDD ;
      ...
    }

    latch(IQ1,IQN1) {
      enable : "!clk" ;
      data_in : "d" ;
      power_down_function : "!VDD+VSS" ;
    }
    latch(IQ2,IQN2) {
      enable : "clk" ;
      data_in : "IQ1" ;
      power_down_function : "!VDD_BAK+VSS" ;
    }

    retention_condition() {
      required_condition : "!clk + d"; /* d is incorrect */
      power_down_function : "!VDD+VSS" ;
    }

    ...
  }
}
```

The following is an example message:

```
Error: Line 3, Cell 'zpr', The pin 'd' specified in required_condition
 attribute should be
 an input signal pin powered by backup power or backup ground. (LBDB-985)
```

What Next

```
Add correct pins specified in required_condition under
 retention_condition group of the cell.
```

LBDB-986

(warning) The '%s' pin '%s' specified in required_condition attribute is not using the '%s' value.

Feedback

Description

```
For zero-pin retention cell, the clock pin logic in required_condition
 must be
the disable value.
For zero-pin retention cell, the async preset/clear pin logic in
 required_condition
must be the inactive value.

For 2-pin retention cell, the "save" signal logic in required_condition
 must using
the disable value.
For 1-pin retention cell, the "save_restore" signal logic in
 required_condition must using
the enable value.
```

The following example shows an instance where this message occurs:

```
library(test) {
 ...
  cell (zpr) {
    ...
    pin(clk) {
      direction : input ;
      related_ground_pin : vss ;
      related_power_pin : vcc_in ;
      ...
    }

    latch(IQ1,IQN1) {
      enable : "!clk" ;
      data_in : "d" ;
      power_down_function : "!vcc+vss" ;
    }
    latch(IQ2,IQN2) {
      enable : "clk" ;
      data_in : "IQ1" ;
      power_down_function : "!vcc_in+vss" ;
    }

    retention_condition() {
      required_condition : "clk"; /* "clk" is incorrect, should be "clk"
 */
      power_down_function : "!vcc+vss" ;
    }

    ...
  }
}
```

Feedback

The following is an example message:

```
Warning: Line 3, Cell 'zpr', The 'clock' pin 'clk' specified in
 required_condition attribute is not using the 'disable' value.
 (LBDB-986)
```

What Next

```
Add correct the pin logic specfied in required_condition of
 retention_condition.
```

LBDB-987

(warning) Can't find '%s' in zero-pin retention cell.

Description

```
Zero-pin retention cell with master-slave latches must have an alive
 latch
to save data in the retention mode.

The alive latch is the latch contains backup power or backup ground
in its power_down_function.

For zero-pin retention cell modeled with ff grorup, the ff group also
 needs
power_down_function attribute with backup power or backup ground.
```

The following example shows an instance where this message occurs:

```
library(test) {
 ...
  cell (zpr) {
    ...
    pin(clk) {
      direction : input ;
      related_ground_pin : vss ;
      related_power_pin : vcc_in ;
      ...
    }

    latch(IQ1,IQN1) {
      enable : "!clk" ;
      data_in : "d" ;
      power_down_function : "!vcc+vss" ;
    }
    latch(IQ2,IQN2) {
      enable : "clk" ;
      data_in : "IQ1" ;
      power_down_function : "!vcc+vss" ;  /* should be "!vcc_in + vss" */
    }
```

```
    retention_condition() {
      required_condition : "!clk";
      power_down_function : "!vcc+vss" ;
    }

    ...
  }
}
```

The following is an example message:

```
Warning: Line 3, Cell 'zpr', Can't find 'alive latch' in zero-pin
 retention cell.
```

What Next

```
Add or correct the power_down_function in the ff/latch group.
```

LBDB-988

(error) Can't specify "retention_pin" attribute in zero-pin retention cell.

Description

```
Zero-pin retention cell is a retention cell with no retention pin.
User cannot specify "retention_pin" attribute on clock pin.
```

The following example shows an instance where this message occurs:

```
library(test) {
 ...
  cell (zpr) {
    ...
    pin(clk) {
      direction : input ;
      related_ground_pin : vss ;
      related_power_pin : vcc_in ;
      retention_pin(save_restore, 1); /* wrong attribute, should be
 removed */
      ...
    }

    latch(IQ1,IQN1) {
      enable : "!clk" ;
      data_in : "d" ;
      power_down_function : "!vcc+vss" ;
    }
    latch(IQ2,IQN2) {
      enable : "clk" ;
      data_in : "IQ1" ;
      power_down_function : "!vcc_in+vss" ;
    }
```

```
    retention_condition() {
      required_condition : "!clk";
      power_down_function : "!vcc+vss" ;
    }

    ...
  }
}
```

The following is an example message:

```
Error: Line 3, Cell 'zpr', Can't specify "retention_pin" attribute in
 zero-pin retention cell.
```

What Next

```
Remove the "retention_pin" attribute in this cell.
```

LBDB-989

(error) the cell has bad antenna diode type.

Description

This message means that value of attribute "antenna_diode_type" doesn't meet the following requirement.

(1) The cell is not an antenna cell. Antenna cell signal pin should be direction input or inout.

(2) If diode_cell_type is "power-ground", the signal pin must specify "antenna_diode_related_power_pins" and "antenna_diode_related_ground_pins".

If diode_cell_type is "power", the signal pin must specify "antenna_diode_related_power_pins".

If diode_cell_type is "ground", the signal pin must specify "antenna_diode_related_ground_pins".

The following is an example message:

```
Error: Line 1023, Cell 'ANTENNA', pin 'a', the cell has bad diode cell
 type. (LBDB-989)
```

What Next

Correct either the signal pin or "antenna_diode_type" attribute.

Feedback

LBDB-989w

(warning) the antenna cell has more than one signal pin. It is marked as dont_touch and dont_use.

Description

Antenna cell should have only one signal pin. This message means that this antenna cell has more than one signal pin, it is marked as dont_touch and dont_use, it can not be auto inferred by galaxy design tools (e.g. ICC1/ICC2 router).

The following is an example message:

```
Warning: Line 1023, Cell 'ANTENNA', the antenna cell has more than one
 signal pin. It is marked as dont_touch and dont_use. (LBDB-989w)
```

What Next

Correct either the signal pin or "antenna_diode_type" attribute.

LBDB-990

(error) the pin has bad antenna diode type.

Description

This message means that pin-level attribute "antenna_diode_type" doesn't meet the following requirement.

If antenna_diode_type is "power-ground", the signal pin must specify "antenna_diode_related_power_pins" and "antenna_diode_related_ground_pins".
If antenna_diode_type is "power", the signal pin must specify "antenna_diode_related_power_pins". If antenna_diode_type is "ground", the signal pin must specify "antenna_diode_related_ground_pins".

The following is an example message:

```
Error: Line 1023, Cell 'HM_MACRO', PIN 'Z', the pin has bad antenna diode
 type. (LBDB-990)
```

What Next

Correct attribute "antenna_diode_type".

LBDB-991

(error) attribute antenna_diode_type is defined in both cell and pin.

Feedback

Description

This message means the cell specifies attribute "antenna_diode_type", and one or more of its signal pins also specifies attribute "antenna_diode_type".

Cell-level attribute "antenna_diode_type" is used in a dedicated antenna diode cell, which basically has only one signal pin for static diffusion.

If a cell has a build-in diode port for static diffusion protection, this port should specify pin-level attribute "antenna_diode_type".

So cell-level attribute "antenna_diode_type" and pin-level attribute "antenna_diode_type" can't coexist in one cell.

The following is an example message:

```
Error: Line 1023, Cell 'ANTENNA', attribute "antenna_diode_type" is
 defined in both cell and pin. (LBDB-991)
```

What Next

Keep at most one "antenna_diode_type" attribute in this cell.

LBDB-992

(error) The '%s' related retention attributes can't be specified in a %s retention pin.

Description

This error message occurs in either of following situations: 1. user specifies following 'save/restore' related retention attributes in a non-retention pin. save_action save_condition restore_action restore_condition restore_edge_type 2. user specifies following 'save' related retention attributes in a restore class retention pin. save_action save_condition 3. user specifies following 'restore' related retention attributes in a save class retention pin. restore_action restore_condition restore_edge_type

Retention pin must have pin level attribute "retention_pin", and the retention pin class spcified in it must be consistent with retention attributes.

In the following example, this pin has *save_action* and *save_condition* attributes, but the retention pin class in *retention_pin* attribute is *restore* To correct the problem, either change the 'restore' to 'save' in the retention_pin attribute, or use 'restore' retention attribute instead of 'save' in this pin.

```
cell(retention_dff) {
  ...
  retention_cell : "my_retention_dff";

  pin(SAVE) {
    retention_pin (restore, 1);
```

Feedback

```
    save_action : L;
    save_condition : CK;
  }

}
```

The above example results in the following error message:

```
Error: Line 192, Cell 'retention_dff', Pin 'SAVE', The 'save' related
 retention attributes
  can't be specified in a restore class retention pin. (LBDB-992)
```

What Next

Resolve the issue by add/correct the *retention_pin* attribute, or use correct save/restore retetion attributes.

LBDB-993

(error) The pin '%s' specified in required_condition attribute should be a retention pin, or an input signal pin powered by backup power or backup ground.

Description

```
For zero-pin retention cell, the pins specified in required_condition
 attribute
must be input signal pins powered by backup_power or backup_ground.

For other types of retention cell (like 1-pin or 2-pin), the pins
 specified in
required_condition attribute must be retention pins, or input signal pins
 powered by
backup_power or backup_ground.
```

The following example shows an instance where this message occurs:

```
library(test) {
 ...
  cell (nonzpr) {
    ...
    pin(save) {
      direction : input ;
      retention_pin(save, "1");
      related_ground_pin : VSS ;
      related_power_pin : VDD_BAK ;
      ...
    }

    pin(d) {
      direction : input ;
      related_ground_pin : VSS ;
      related_power_pin : VDD ;
```

Feedback

```
      ...
    }

    latch(IQ1,IQN1) {
      enable : "!clk" ;
      data_in : "d" ;
      power_down_function : "!VDD+VSS" ;
    }
    latch(IQ2,IQN2) {
      enable : "clk" ;
      data_in : "IQ1" ;
      power_down_function : "!VDD_BAK+VSS" ;
    }

    retention_condition() {
      required_condition : "!save + d"; /* d is incorrect */
      power_down_function : "!VDD+VSS" ;
    }

    ...
  }
}
```

The following is an example message:

```
Error: Line 3, Cell 'nonzpr', The pin 'd' specified in required_condition
 attribute should be
a retention pin, or an input signal pin powered by backup power or backup
 ground. (LBDB-993)
```

What Next

```
Add correct pins specified in required_condition under
 retention_condition group of the cell.
```

LBDB-994

(error) In attribute '%s', The ccsn noise stage referenced is insufficient for this timing.

Description

The ccsn noise stage referenced(thereafter, "ccb") in active_output_ccb must be pull-up/down compatible with the timing. The valid ccb(s) with proper stage_type could be any one of the following:

1. when output of the timing could be rise and fall. (e.g. timing_type:"combinational")

1. one ccb with stage_type:both

2. two ccb's, one with stage_type:pull_up, the other with stage_type:pull_down

    a. when output of the timing always rise. (e.g. timing_type:"combinational_rise")

Feedback

3. one ccb with stage_type:both
4. one ccb with stage_type:pull_up
    a. when output of the timing always fall. (e.g. timing_type:"combinational_fall")
5. one ccb with stage_type:both
6. one ccb with stage_type:pull_down

The following example shows an instance where this message occurs:

```
library(test) {
    cell(INV) {
      pin(X) {
        direction : "output" ;
        ...
        output_ccb(o_rise) {
          stage_type : pull_up ;
          ...
        }
        timing() {
          timing_type : "combinational" ;
          ...
          active_output_ccb(o_rise);
        }
      }
    }
  }
```

The following is an example message:

```
Error: Line 3401, Cell 'INV', pin 'X', In attribute 'active_output_ccb',
 The
ccsn noise stage referenced is insufficient for this timing. (LBDB-994)
```

What Next

Provide the valid ccb(s) accordingly.

LBDB-995

(error) it's not allowed to specify both intrinsic_capacitance and total_capacitance in macro cell intrinsic_parasitic group.

Description

If cell is macro cell, user can specify only intrinsic_capacitance or total_capacitance, but not both.

Feedback

The following example shows an instance where this message occurs:

```
cell (my_macro_cell) {
  ...
  power_cell_type : macro;
  intrinsic_parasitic() {
    when : "A1";
    total_capacitance(V2) {
       value : 9.0;
    }
    intrinsic_capacitance(G1) {
       value : 62.2;
    }
  }
}
```

In this case, cell 'my_macro_cell' is a macro cell, both total_capacitance and intrinsic_capacitance are specified in intrinsic_parasitic. So error message LBDB-995 will be issued.

The following is an example message:

```
Error: Line 115, Cell 'my_macro_cell', it's not allowed to specify
 both intrinsic_capacitance and total_capacitance in macro cell
 intrinsic_parasitic group. (LBDB-995)
```

What Next

Remove intrinsic_capacitance or total_capacitance group.

LBDB-996

(error) The timing arc's fpga_arc_condition attribute contains \n \tinvalid format '%s.%s'.

Description

This message indicates that you specified invalid <pin_name>.<pin_status> or <fpga_cond_name>.<fpga_cond_value_name> in the fpga_arc_condition attribute of the timing arc.

The following example shows an instance where this message occurs:

```
cell(test) {

  ...
  pin(A) {
        ...
  }
  pin(B) {
        ...
        timing() {
                ...
```

```
                fpga_arc_condition: "wrong_pin.CONNECTED";
                ...
        }
        ...
  }
  ...
}
```

We can correct it by replace "wrong_pin" with "A".

The following is an example message:

```
Error: Line 206, The timing arc's fpga_arc_condition attribute contains
        invalid format 'wrong_pin.CONNECTED'. (LBDB-996)
```

What Next

Modify <A>.<B> to make it as a valid <pin_name>.<pin_status> or <fpga_cond_name>.<fpga_cond_value_name>.

LBDB-997

(warning) The fpga_condition(%s) group is defined\n \tmultiple times.

Description

This message indicates that you specified the same fpga_condition group multiple times. Only the last one is retained.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;

  fpga_condition(cond1) {
    ...
  }
  fpga_condition(cond1) {
    ...
  }
  ...
}
```

The following is an example message:

```
Warning: Line 206, The fpga_conditino(cond1) group is defined
        multiple times. (LBDB-997)
```

What Next

Change the group name, or delete the duplicated group.

Feedback

LBDB-998

(error) The fpga condition '%s' has no values defined.

Description

A fpga_condition group must have at least one fpga condition value defined.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  fpga_condition(cond1) {
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The fpga condition 'cond1' has no values defined.
 (LBDB-998)
```

What Next

Define the fpga condition values.

LBDB-999

(warning) The fpga_condition_value(%s) group is defined\n \tmultiple times.

Description

This message indicates that you specified the same fpga_condition_value group multiple times. Only the last one is retained.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;

  fpga_condition(cond1) {
    fpga_condition_value(normal) {
      fpga_arc_condition : "operation_mode=normal";
    }
    fpga_condition_value(normal) {
      fpga_arc_condition : "operation_mode=arithmetic";
    }
  }
}
```

The following is an example message:

```
Warning: Line 206, The fpga_condition_value(normal) group is defined
        multiple times. (LBDB-999)
```

What Next

Change the group name, or delete the duplicated group.

LBDB-1000

(error) The fpga_arc_condition attribute is not specified\n \tfor the fpga_condition_value.

Description

This message indicates that you have not specified fpga_arc_condition attribute within fpga_condition_value.

The following example shows an instance where this message occurs:

```
cell(CGNP) {
  area : 1;
  fpga_condition(cond1) {
    fpga_condition_value(normal) {
      fpga_arc_condition : "operation_mode=normal";
    }
  }
  ...
}
```

The following is an example message:

```
Error: Line 206, The fpga_arc_condition attribute is not specified for
 the
        fpga_condition_value. (LBDB-1000)
```

What Next

Add the missing fpga_arc_condition attribute.

LBDB-1001

(error) Found one or more cells defined before '%s' group.

Description

This message indicates the named group in phys_library is not defined before all cell groups.

Feedback

The following example shows an instance where this message occurs:

```
phy_library(test) {
        ...
        macro (cell1) {
         ...
        }
        resource ( std_cell ) {
          ...
        }
    }
```

The following is an example message:

```
Error: Line 59, Found one or more cells defined before 'resource' group.
 (LBDB-1001)
```

What Next

Move this group inside the physical library so that it is defined in front of all cell groups.

LBDB-1002

(error) The resource name is not supported.

Description

Library Compiler accepts resource with the following names: - std_cell - array

This message indicates the resource group is using a name other than mentioned above.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        resource ( wrong_name ) {               /* ERROR */
          ...
        }
    }
```

The following is an example message:

```
Error: Line 5, The resource name is not supported. (LBDB-1002)
```

What Next

Change the resource group name to either "std_cell" or "array".

LBDB-1003

(error) The resource group does not contain any layer definition.

Feedback

Description

Library Compiler requires that one or more layer definition be defined in the resource group. A layer definition can be one of the following functions / groups: - device_layer - contact_layer - overlap_layer - routing_layer

This message indicates there is none of the above defined in the resource group.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        resource ( std_cell ) {          /* ERROR */
        }
        ...
    }
```

The following is an example message:

```
Error: Line 3, The resource group does not contain any layer definition.
 (LBDB-1003)
```

What Next

Add layer information into resource group.

LBDB-1004

(error) The resource group does not contain any site / tile definition.

Description

Library Compiler requires that one or more site / tile groups be defined in the resource group.

This message indicates there is neither any site nor any tile groups defined in the resource group.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        resource ( std_cell ) {          /* ERROR */
        }
        ...
    }
```

The following is an example message:

```
Error: Line 3, The resource group does not contain any site / tile
 definition. (LBDB-1004)
```

Feedback

What Next

Add site information into resource group.

LBDB-1005

(warning) Found a duplicate %s attribute. Using the first value.

Description

This message indicates an attribute has been defined twice. The second definition is ignored.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
        }
        macro(and2a) {
          ...
        }
        macro(and2a1) {
          ...
          eq_cell : and2a;
          eq_cell : and2;
          ...
        }
    }
```

The following is an example message:

```
Warning: Line 34, Found a duplicate eq_cell attribute. Using the first
 value. (LBDB-1005)
```

What Next

Remove the duplicate definition of the attribute.

LBDB-1006

(error) Cannot accept the '%s' pin as the logically equivalent pin.

Description

This message indicates the eq_pin attribute value is an unacceptable pin name. An unacceptable eq_pin is defined as either - a name equivalent to the current pin name; or - a pin that is not already defined.

Feedback

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          pin(a) {
            eq_pin : a1;        /* error */
            ...
          }
          pin(a1) {
          }
        }
    }
```

The following is an example message:

```
Error: Line 34, Cannot accept the 'a1' pin as the logically equivalent
 pin. (LBDB-1006)
```

What Next

Check the pin name and change it. Also make sure the pin specified in the eq_pin attribute is pre-defined.

LBDB-1007

(error) The %s name '%s' is an undefined layer name.

Description

This message indicates the obs / geometry group name is not a legal layer name.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          pin(a) {
            ...
            obs(new_layer) {    /* error */
              ...
            }
          }
        }
    }
```

The following is an example message:

```
Error: Line 34, The obs name 'new_layer' is an undefined layer name.
 (LBDB-1007)
```

Feedback

What Next

Use a pre-defined layer name as the name for the obs / geometry group.

LBDB-1008

(error) The %s function has inconsistent number of arguments.

Description

This message indicates the path / polygon / rectangle function has wrong number of arguments. In Library Compiler, - a path function requires odd number of arguments no less than 3; - a polygon function requires even number of arguments no less than 8; - a rectangle function requires 4 arguments.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          pin(a) {
            ...
            obs(new_layer) {
              rectangle(0.1, 0.3);  /* error */
            }
          }
        }
    }
```

The following is an example message:

```
Error: Line 34, The rectangle function has inconsistent number of
 arguments. (LBDB-1008)
```

What Next

Make sure the right argument is used for each function.

LBDB-1009

(error) Non-positive number found in the size function.

Description

This message indicates either the width or the height of the size function is a non-positive number.

Feedback

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          size (-1.5, 2.0);       /* error */
        }
    }
```

The following is an example message:

```
Error: Line 34, Non-positive number found in the size function.
 (LBDB-1009)
```

What Next

Make sure both width or height of the size function are positive numbers.

LBDB-1010

(error) The site '%s' is not defined in the resource group.

Description

This message indicates name of the site attribute is not a pre-defined site.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          site : new_site;       /* error */
        }
    }
```

The following is an example message:

```
Error: Line 34, The site 'new_site' is not defined in the resource group.
 (LBDB-1010)
```

What Next

Make sure the site attribute uses a pre-defined site.

LBDB-1011

(error) Cannot accept the '%s' macro as the equivalent cell.

Feedback

Description

This message indicates the eq_cell attribute value is an unacceptable macro name. An unacceptable macro name is defined as either - a name equivalent to the current macro name; or - a macro that is not already defined.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2a1) {
          ...
          eq_cell : and2;               /* error */
          ...
        }
        macro(and2) {
          ...
        }
    }
```

The following is an example message:

```
Error: Line 34, Cannot accept the 'and2' macro as the electrically
 equivalent cell. (LBDB-1011)
```

What Next

Check the macro name and change it. Also make sure the macro specified in the eq_cell attribute is pre-defined.

LBDB-1012

(error) The layer name, '%s', in the '%s' group is not unique.

Description

Each via group can specify up to 3 geometry groups with the 'layer1', 'contact' and 'layer2' groups. The name of each group gives the name of the layer on which all geometry shapes are defined. The 3 geometry groups must be defined on different layers. This error message indicates that 2 or more geometry groups are specified on the same layer.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        resource(std_cell) {
          ...
          via (test) {
            ...
            layer1(met1) {
                ...
```

```
            }
            contact(con1) {
                ...
            }
            layer2(met1) {      /* error */
                ...
            }
          ...
          }
        }
    }
```

The following is an example message:

```
Error: Line 34, The layer name, 'met1', in the 'layer2' group is not
 unique. (LBDB-1012)
```

What Next

Check the layer names on the 'layer1', 'contact' and 'layer2' groups and make sure they call for different layer names.

LBDB-1013

(error) The %s function has inconsistent number of arguments.

Description

This message indicates the via / via_iterate function has wrong number of arguments. In Library Compiler, - a via function requires 3 arguments: a name followed by x / y coordinates; - a via_iterate function requires 7 arguments: 2 integers (for x-iteration and y-iteration), 2 real numbers (for x-spacing and y-spacing), a name and another 2 real numbers for the first x / y coordinates.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          pin(a) {
            ...
            obs(new_layer) {
              via(0.1, 0.3);  /* error */
            }
          }
        }
    }
```

Feedback

The following is an example message:

```
Error: Line 34, The via function has inconsistent number of arguments.
 (LBDB-1013)
```

What Next

Make sure the right argument is used for each function.

LBDB-1014

(error) The via group does not have a 'contact' group.

Description

Each via group is required to have a 'contact' group defined for the geometry in the contact layer. This error message indicates that the 'contact' group is missing from the current via group.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        resource(std_cell) {
          ...
          via (test) {  /* error */
            layer1(met1) {
                ...
            }
            layer2(met2) {
                ...
            }
          ...
          }
        }
    }
```

The following is an example message:

```
Error: Line 34, The via group does not have a 'contact' group.
 (LBDB-1014)
```

What Next

Make sure the 'contact' group is defined in current 'via' group.

LBDB-1015

(error) One or more rectangles are required in this group.

Feedback

Description

The 'layer1', 'contact' and 'layer2' sub-groups inside a 'via' group define the geometry shapes for the via. This error message indicates that the current sub-group has no rectangle specified.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        resource(std_cell) {
          ...
          via (test) {
            layer1(con1) { }    /* error */
            ...
          }
        }
    }
```

The following is an example message:

```
Error: Line 34, One or more rectangles are required in this group.
 (LBDB-1015)
```

What Next

Make sure there are at least 1 rectangle defined in the current sub-group. Otherwise, remove the sub-group altogether.

LBDB-1016

(error) The routing_grid function has inconsistent number of arguments.

Description

This message indicates the routing_grid function has wrong number of arguments. In Library Compiler, - a routing_grid function requires 6 arguments: x-starting-coordinate, number-of-columns, x-space, y-start-coordinate, number-of-rows, y-space.

The following example shows an instance where this message occurs:

```
phys_library(test) {
      ...
      array(ABC) {
        routing_grid(100, 200);
        ...
      }
      ...
    }
```

Feedback

The following is an example message:

```
Error: Line 34, The routing_grid function has inconsistent number of
 arguments. (LBDB-1016)
```

What Next

Make sure the right arguments are used for each function.

LBDB-1017

(error) The floorplan group contains mismatching site_array group.

Description

This message indicates that either: - the default floorplan (with no given name) is missing site_array with "regular" placement_rule; or - the non-default floorplan contains site_array with "regular" placement_rule.

The default floorplan should contain one or more "regular" site_array groups. The non-default floorplan should not contain any "regular" site_array group.

The following example shows an instance where this message occurs:

```
phys_library(test) {
      ...
      array(ABC) {
        floorplan() {
          site_array(new) {
            placement_rule : can_place;
            ...
          }
        }
        ...
      }
      ...
    }
```

The following is an example message:

```
Error: Line 34,  The floorplan group contains mismatching site_array
 group.  (LBDB-1017)
```

What Next

Check all site_array groups under the current floorplan and make sure the above rules are followed.

Feedback

LBDB-1018

(warning) The floorplan group does not contain can_place/cannot_occupy\n \t site_array groups.

Description

This message indicates that the current floorplan group only contain site_array groups with "regular" placement_rule.

The following example shows an instance where this message occurs:

```
phys_library(test) {
      ...
      array(ABC) {
        floorplan() {
          site_array(new) {
            placement_rule : regular;
            ...
          }
        }
        ...
      }
      ...
    }
```

The following is an example message:

```
Warning: Line 34,  The floorplan group does not contain
 can_place/cannot_occupy
                 site_array groups.  (LBDB-1018)
```

What Next

Make sure this is the correct physical library technology data.

LBDB-1019

(error) The array group does not contain base floorplan.

Description

This message indicates that the current array group contain no base floorplan data. An array group must have a base floorplan group - i.e. a floorplan group defined with no given name.

The following example shows an instance where this message occurs:

```
phys_library(test) {
      ...
      array(ABC) {
```

Feedback

```
        floorplan(NEW) {
            ...
          }
      }
        ...
      }
      ...
    }
```

The following is an example message:

```
Error: Line 34,  The floorplan group does not contain base floorplan.
 (LBDB-1018)
```

What Next

Add base floorplan data into this array group.

LBDB-1020

(error) The '%s' function has inconsistent number of arguments.

Description

This message indicates the iterate function in the current site_array has wrong number of arguments. In Library Compiler, - a iterate function requires 4 numerical arguments.

The following example shows an instance where this message occurs:

```
phys_library(test) {
      ...
      array(ABC) {
        site_array(test) {
          iterate (100, 200);
          ..
        }
        ...
      }
      ...
    }
```

The following is an example message:

```
Error: Line 34, The iterate function has inconsistent number of
 arguments. (LBDB-1020)
```

What Next

Make sure the right arguments are used for each function.

Feedback

LBDB-1021

(error) The resource group does not contain any via definition.

Description

Library Compiler requires that one or more via groups be defined in the resource group.

This message indicates there is no via groups defined in the resource group.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        resource ( std_cell ) {          /* ERROR */
        }
        ...
    }
```

The following is an example message:

```
Error: Line 3, The via group does not contain any site definition.
 (LBDB-1021)
```

What Next

Add via information into resource group.

LBDB-1022

(error) The resource group must be defined before the\n \ttopological_design_rules group.

Description

Library Compiler requires all physical library plib file to specify the resource group before specifying the topological_design_rules group.

This message indicates there is no resource group defined before the topological_design_rules group.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        topological_design_rules ( ) {          /* ERROR */
        }
        ...
    }
```

The following is an example message:

```
Error: Line 2, The resource group must be defined before the
               topological_design_rules group.  (LBDB-1022)
```

Feedback

What Next

Add or move the resource group to the front of the topological_design_rules group.

LBDB-1023

(warning) No '%s' group defined in the topological_rules group.

Description

There is no specified group information in the current library.

The following example shows an instance where this message occurs:

```
phys_library(test) {
      resource(std_cell) {
        ...
      }
      topological_rules() {
      }
      ...
    }
```

The following is an example message:

```
Warning: Line 34,  No via_rule group defined in the topological_rules
 group. (LBDB-1023)
```

What Next

Make sure the library is correct.

LBDB-1024

(error) The %s function has inconsistent number of arguments.

Description

This message indicates the min_generate_via_size function has wrong number of arguments. In Library Compiler, it requires 2 floating numbers in the min_generated_via_size function.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        min_generated_via_size (0.1, 0.2, 0.1);
        ...
    }
```

Feedback

The following is an example message:

```
Error: Line 2, The min_generated_via_size function has inconsistent
 number of arguments. (LBDB-1024)
```

What Next

Make sure the right argument is used for the function.

LBDB-1025

(error) The '%s' function cannot be supplied a \n \tnonpositive value.

Description

This message indicates that the specified function cannot have a nonpositive value.

The following example shows an instance where this message occurs:

```
min_generate_via_size(-1, 0.3);
```

The following is an example message:

```
Error: Line 18, The 'min_generate_via_size' function cannot be supplied a
       nonpositive value. (LBDB-1025)
```

What Next

Change all value of the function to positive in the physical library file.

LBDB-1026

(error) The '%s' function has inconsistent arguments.

Description

This message indicates the same_net_min_spacing function has wrong arguments. In Library Compiler, it requires 2 layer names followed by a floating numbers and a boolean value (TRUE or FALSE) in the same_net_min_spacing function.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        same_net_min_spacing (metal1, metal2, 0.1);
        ...
    }
```

The following is an example message:

```
Error: Line 2, The 'same_net_min_spacing" function has inconsistent
 arguments. (LBDB-1026)
```

Feedback

What Next

Make sure the right argument is used for the function.

LBDB-1027

(error) The '%s' function has inconsistent arguments.

Description

This message indicates the contact_spacing function has wrong arguments. In Library Compiler, it requires 2 floating numbers in the contact_spacing function.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        contact_spacing (0.1, 0.2);
        ...
    }
```

The following is an example message:

```
Error: Line 158, The 'contact_spacing" function has inconsistent
 arguments. (LBDB-1027)
```

What Next

Make sure the right argument is used for the function.

LBDB-1028

(error) The '%s' layer name is of invalid layer type. A %s name is expected.

Description

This message indicates that you specified an layer name with wrong type for the current attribute or function. The name should be a routing_layer or contact_layer name as indicated in the error message.

The following example shows an instance where this message occurs:

```
contact_min_spacing(metal1, contact1, 0.1);
```

The following is an example message:

```
Error: Line 104, The 'metal1' layer name is of invalid layer type.  A
 contact_layer name is expected.  (LBDB-1028)
```

Feedback

What Next

Check your library to see if you have an error in either previous layer definition or the current attribute / function.

LBDB-1029

(error) There is no rectangle defined in the contact_formula group.

Description

There is no rectangle defined in the current contact_formula group. Library Compiler requires at least 1 rectangle being specified in each contact_formula group.

The following example shows an instance where this message occurs:

```
via_rule_generate(GEN1) {
      contact_formula(con1) {   /* error */
        routing_direction : horizontal;
        resistance : 0.2;
      }
    }
```

The following is an example message:

```
Warning: Line 34,  There is no rectangle defined in the  contact_formula
 group. (LBDB-1029)
```

What Next

Define the rectangle shape for the contact_formula group.

LBDB-1030

(error) The '%s' attribute value is larger than the '%s' attribute value.

Description

This message indicates that the 'min_wire_width' value is larger than 'max_wire_width' value. Library Compiler requires that the 'min_wire_width' is no larger than 'max_wire_width' value.

The following example shows an instance where this message occurs:

```
routing_layer_rule(met1) {
      min_wire_width : 2.0;
      max_wire_width : 1.0;
      ...
    }
```

Feedback

The following is an example message:

```
Error: Line 18, The 'min_wire_width' attribute value is larger than the
 'max_wire_width' attribute value.  (LBDB-1030)
```

What Next

Change all related values follow the requirement.

LBDB-1031

(error) The wire_rule group is empty.

Description

This message indicates the wire_rule group does not have any layer_rule / via group or same_net_min_spacing function defined. Library Compiler requires that the wire_rule group not be empty.

The following example shows an instance where this message occurs:

```
wire_rule(rule1) {
    }
```

The following is an example message:

```
Error: Line 34, The wire_rule group is empty. (LBDB-1031)
```

What Next

Make sure the the wire_rule group is not empty.

LBDB-1032

(error) Cannot accept the '%s' pin as the must_join pin.

Description

This message indicates the must_join pin attribute value is an unacceptable pin name. An unacceptable must_join is defined as either - a name equivalent to the current pin name; or - a pin that is not already defined.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          pin(a) {
            must_join : a1;     /* error */
            ...
```

Feedback

```
            }
            pin(a1) {
            }
        }
    }
```

The following is an example message:

```
Error: Line 34, Cannot accept the 'a1' pin as the must_join pin.
 (LBDB-1032)
```

What Next

Check the pin name and change it. Also make sure the pin specified in the must_join attribute is pre-defined.

LBDB-1033

(error) The '%s' function has inconsistent arguments.

Description

This message indicates the ranged_spacing function has wrong arguments. In Library Compiler, it requires 3 floating numbers in the ranged_spacing function.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ranged_spacing (0.1, 0.2);
        ...
    }
```

The following is an example message:

```
Error: Line 2, The 'ranged_spacing" function has inconsistent arguments.
 (LBDB-1033)
```

What Next

Make sure the right argument is used for the function.

LBDB-1034

(warning) The '%s' %s group already exists and\n \tcannot be overwritten. The first definition will be used.

Description

This message indicates that you multiply defined a site group. Library Compiler does not allow the overwriting of existing site groups.

Feedback

The following example shows an instance where this message occurs:

```
site(IOsite) {
         ...
        }
        site(IOsite) {
         ...
        }
```

The following is an example message:

```
Error: Line 31, The 'IOsite' site group already exists and
       cannot be overwritten. The first definition will be used.
 (LBDB-1034)
```

What Next

Delete the second specification of the site group.

LBDB-1035

(error) The '%s' array must have '%d' entries.

Description

You receive this message because the specified array has a different size from the one expected.

Where *N* is the number of routing layers, the following criteria are set:

```
plate_cap array must have ((N * (N-1)) / 2) entries
overlap_wire_ratio must have (N * (N-1)) entries
adjacent_wire_ratio must have N entries
wire_ratio_x must have N entries
wire_ratio_y must have N entries
```

The following example shows an instance where this message occurs:

```
plate_cap( "0.05, 0.06, 0.03" );
```

The following is an example message: Error: Line 127, The 'plate_cap' array must have '6' entries. (LBDB-1035)

What Next

Correct the values in the specified array.

LBDB-1036

(error) The sum of values in the '%s' array attribute does not meet the requirement.

Feedback

Description

You receive this message because the sum of ratios does not match the specified criteria. The following criteria are set:

overlap_wire_ratio: the sum of value[i(N-1)] to value[i(N-1)+(N-2)] must not exceed 100.0 (100 percent); where *N* is the number of routing layers and *i* is the routing layer id in the range of i=0..N-1.

adjacent_wire_ratio: n/a (not applicable);

wire_ratio_x: the sum of all values must equal 100.0 (100 percent);

wire_ratio_y: the sum of all values must equal 100.0 (100 percent).

The following example shows an instance where this message occurs:

```
wire_ratio_x( "40.1, 20.0, 20.5" );
```

The following is an example message: Error: Line 127, The sum of values in the 'wire_ratio_x' array attribute does not meet requirement. (LBDB-1036)

What Next

Correct the values in the specified array.

LBDB-1037

(error) Cannot accept the '%s' as the default_routing_wire_model value.

Description

You receive this message because the default_routing_wire_model attribute value is an unacceptable routing_wire_model name, that is, one that is a routing_wire_model that has not already been defined.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        resource(...) {
          ...
          default_routing_wire_model : model_1;          /* error */
          ...
          routing_wire_model(model_1) {
          ...
          }
        }
    }
```

Feedback

The following is an example message: Error: Line 34, Cannot accept the 'model_1' as the default_routing_wire_model value. (LBDB-1037)

What Next

Change the routing_wire_model name. Ensure that the routing_wire_model specified in the default_routing_wire_model attribute is predefined.

LBDB-1038

(error) The plate_cap attribute is not predefined.

Description

You receive this message because the *plate_cap* attribute is not predefined. It has not been defined before the routing_wire_model() group is defined.

The following example shows an instance where this message occurs:

```
phys_library(test) {
    ...
    resource(...) {
      ...
      routing_wire_model(model_1) { /* error: LBDB-1038 */
      ...
      }
      plate_cap ("0.05, 0.04, 0.06");
    }
}
```

The following is an example message: Error: Line 34, The plate_cap attribute is not predefined. (LBDB-1038)

What Next

Ensure that *plate_cap* is defined before the routing_wire_model() group is defined.

LBDB-1039

(error) The '%s' attribute has an out-of-range '%f' ratio.

Description

You receive this message because a percentage ratio in an array attribute is larger than 100.0 (100%) or less than 0 (0%); it has not been accepted.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
```

Feedback

```
        resource(...) {
          ...
          routing_wire_model(model_1) {
            ...
            wire_ratio_x ("21.3, 305.4, 19.4"); /* error */
            ...
          }
        }
    }
```

The following is an example message: Error: Line 34, The 'wire_ratio_x' attribute has an out-of-range '305.4' ratio. (LBDB-1039)

What Next

Ensure that all values are between 0.0 (0%) and 100.0 (100%).

LBDB-1040

(error) The %s function has an inconsistent number of arguments.

Description

You receive this message because the *obs_clip_box* or *keepout_clip_box* function has the wrong number of arguments. In Library Compiler, the specified command requires four floating numbers in the *obs_clip_box* or *keepout_clip_box* function.

The following example shows an instance where this message occurs:

```
keepout_clip_box (0.1, 0.2, 0.1);
        ...
```

The following is an example message: Error: Line 25 The keepout_clip_box function has an inconsistent number of arguments. (LBDB-1040)

What Next

Ensure that the right argument is used for the specified function.

LBDB-1041

(error) The %s function has inconsistent arguments.

Description

You receive this message because the *gds2_layer_map* function has the wrong number or type of arguments. In Library Compiler, the specified function requires an integer, a string, and an integer in the *gds2_layer_map* function.

Feedback

The following example shows an instance where this message occurs:

```
gds2_layer_map (0.1, METAL1, 1);
```

The following is an example message: Error: Line 30, The gds2_layer_map function has inconsistent arguments. (LBDB-1041)

What Next

Ensure that the right argument is used for the function.

LBDB-1042

(warning) The dist_conversion_factor value '%d' is not allowed. Using default value '%d'.

Description

You receive this message because you specified a dist_conversion_factor value that either is not a multiple of 100 or may be a nonpositive number.

The following example shows an instance where this message occurs:

```
dist_conversion_factor : 123;
```

The following is an example message: Warning: Line 85, The dist_conversion_factor value '123' is not allowed. Using default value '1000'. (LBDB-1042)

What Next

Examine the library source file, and correct the dist_conversion_factor value.

LBDB-1043

(error) The gds2_conversion_factor value '%d' is not allowed.

Description

You receive this message because you specified a *gds2_conversion_factor* value that is not a multiple of 100s or may be a nonpositive number.

The following example shows an instance where this message occurs:
gds2_conversion_factor : -100;

The following is an example message: Warning: Line 85, The gds2_conversion_factor value '-100' is not allowed. (LBDB-1043)

What Next

Examine the library source file, and correct the *gds2_conversion_factor* value.

Feedback

LBDB-1044

(error) The process resource group must be defined after the \n \tresource group and the topological design rules group.

Description

This message indicates that there is no resource group and/or topological design rules group defined before the process resource group. Library Compiler requires all physical library plib files to specify the resource group and the topological_design_rules group before specifying the process_resource group.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        process_resource (...) {                /* ERROR */
        }
        ...
    }
```

The following is an example message:

```
Error: Line 2, The process_resource group must be defined after the
               resource group and the topological_design_rules group.
 (LBDB-1044)
```

What Next

Add or move the resource group and the topological design rules group to the front of the process resource group.

LBDB-1045

(error) The %s name '%s' is an undefined %s name.

Description

This error message means that the specified process routing layer, process via, or process wire rule name was not predefined.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        resource(...) {
          routing_layer (met1) {
          }
        }
        process_resource(...) {
          process_routing_layer(METAL1) { /* ERROR: METAL 1 is not
 defined.  Use met1 instead */
          }
```

Feedback

```
        ...
        macro(and2) {
          ...
          pin(a) {
            ...
            obs(new_layer) {    /* error */
              ...
            }
          }
        }
    }
```

The following is an example message:

```
Error: Line 34, The process_routing_layer name 'METAL1' is an undefined
 routing_layer name. (LBDB-1045)
```

What Next

Use the *read_lib* command and specify a predefined routing layer, via, or process wire rule.

LBDB-1046

(warning) The boundary_layer attribute is not defined in\n \t gds2_extraction_rules.

Description

This warning message tells you that you used the *read_lib* command and specified the *boundary_layer* attribute, but the *boundary_layer* attribute is not defined in gds2_extraction_rules. In Library Compiler, the *boundary_layer* attribute specifies a layer ID for GDSII extraction to look for the designated macro boundary for the macro size in the PLIB file. When this attribute is missing, the macro size in the PLIB file is determined by the bounding box of all geometries.

The following is an example message: Warning: The boundary_layer attribute is not defined in gds2_extraction_rules. (LBDB-1046)

What Next

Make sure you did not intend to specify the boundary layer. If you did intend to specify the boundary layer, define the *boundary_layer* attribute and reexecute the command.

See Also

- read_lib

Feedback

LBDB-1047

(error) The '%s' function has inconsistent arguments.

Description

This message indicates the lateral_oxide function has wrong arguments. In Library Compiler, it requires 2 floating numbers in the lateral_oxide function.

The following example shows an instance where this message occurs:

```
lateral_oxide (0.1, 0.2, 0.3);
```

The following is an example message:

```
Error: Line 2, The 'lateral_oxide" function has inconsistent arguments.
 (LBDB-1047)
```

What Next

Make sure the right argument is used for the function.

LBDB-1048

(error) The '%s' permittivity value is less than 1.00.

Description

The permittivity value must be at least 1.00. It also includes the second value in lateral_oxide() complex attribute.

The following example shows an instance where this message occurs:

```
lateral_oxide ( 3.9, 0.99 );
```

The following is an example message:

```
Error: Line 46, The 'lateral_oxide' permittivity value is less than 1.00.
  (LBDB-1048)
```

What Next

Check your library and use correct permittivity value.

LBDB-1049

(error) The '%s' thickness value is less than zero.

Feedback

Description

The thickness value must be positive. It also applies to the first value in lateral_oxide() complex attribute.

The following example shows an instance where this message occurs:

```
lateral_oxide ( -3.9, 3.99 );
```

The following is an example message:

```
Error: Line 46, The 'lateral_oxide' thickness value is less than zero.
 (LBDB-1049)
```

What Next

Check your library and use correct thickness value.

LBDB-1050

(error) There is no rectangle defined in the via_contact_layer group.

Description

There is no rectangle defined in the current via_contact_layer group. Library Compiler requires at least 1 rectangle being specified in each via_contact_layer group.

The following example shows an instance where this message occurs:

```
default_via_generate(GEN1) {
      via_contact_layer(con1) {          /* error */
        resistance : 0.2;
      }
    }
```

The following is an example message:

```
Warning: Line 34,  There is no rectangle defined in the
 via_contact_layer group. (LBDB-1050)
```

What Next

Define the rectangle shape for the via_contact_layer group.

LBDB-1051

(error) The %s attribute is obsolete.

Feedback

Description

This message indicates the named attribute is obsolete and need to be changed accordingly.

The following example shows an instance where this message occurs:

```
lateral_oxide_thickness : 0.5 ;
```

The following is an example message:

```
Error: Line 34, The lateral_oxide_thickness attribute is obsolete.
 (LBDB-1051)
```

What Next

Refer to the Library Compiler User Guide for the newest attribute names.

LBDB-1052

(error) The 'layer_antenna_factor' function has inconsistent arguments.

Description

This message indicates the layer_antenna_factor function has wrong arguments. In Library Compiler, it requires one layer name followed by a floating number in the layer_antenna_factor function.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        layer_antenna_factor (metal1, metal2, 0.1);
        ...
    }
```

The following is an example message:

```
Error: Line 25, The 'layer_antenna_factor' function has inconsistent
 arguments. (LBDB-1052)
```

What Next

Make sure the right argument is used for the function.

LBDB-1053

(error) The '%s' group contains conflicting layer specification styles,\n \t'%s' and '%s'.

Feedback

Description

This message indicates the gds2 layer id definition styles are found. For example, you should either use obs_layer_map or obs_layer_id to specify geometry layer id and/or data type, but never use both functions in the same plib/pplib file.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        gds2_extraction_rules() {
          obs_layer_map ( "14, 16, 18, 20", "07, 08, 09, 10");
          obs_layer_id (22, 0, 11, 0);
        ...
    }
```

The following is an example message:

```
Error: Line 25, The 'gds2_extraction_rules' group contains conflicting
 layer specification styles,
        'obs_layer_map' and 'obs_layer_id'. (LBDB-1053)
```

What Next

Make sure only one style is used in layer id definition.

LBDB-1054

(warning) The port '%s' does not have the attribute '%s' specified. The value (%f, %f) will be assigned to the attribute.

Description

You receive this error message when the *rise_capacitance* and *fall_capacitance* attributes are specified for a port, but the *rise_capacitance_range* and *fall_capacitance_range* attribute are not. (*rise_capacitance*, *rise_capacitance*) will be assigned to attribute *rise_capacitance_range\ and (fall_capacitance, fall_capacitance) will be assigned to attribute fall_capacitance_range respectively.*

What Next

If you accept the value assigned to the attribute referenced in the error message, no action is required on your part. If not, assign a value to the attribute.

LBDB-1055

(error) The '%s' function has inconsistent arguments.

Feedback

Description

This message indicates the contact_min_spacing function, min_overhang function or diff_net_min_spacing function has wrong arguments. In Library Compiler, it requires 2 layer names followed by a floating numbers in the contact_min_spacing function, min_overhang function or diff_net_min_spacing function.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        topological_design_rules() {
          contact_min_spacing (contact1, 0.5);
          min_overhang (metal1, contact1, 0.3);
          diff_net_min_spacing (metal1, contact1, 0.6);
          ...
        }
        ...
    }
```

The following is an example message:

```
Error: Line 245, The 'contact_min_spacing" function has inconsistent
 arguments. (LBDB-1027)
```

What Next

Make sure the right argument is used for the function.

LBDB-1056

(warning) The '%s' value '%d' is not allowed. Using default value '%d'.

Description

You receive this message because you specified a conversion factor value that either is not a multiple of 100 or may be a nonpositive number. A conversion factor can be - capacitance_conversion_factor, or - resistance_conversion_factor, or - current_conversion_factor, or - inductance_conversion_factor.

The following example shows an instance where this message occurs:

```
capacitance_conversion_factor : 123;
```

The following is an example message: Warning: Line 85, The 'capacitance_conversion_factor' value '123' is not allowed. Using default value '1000'. (LBDB-1056)

What Next

Examine the library source file, and correct the conversion factor value.

Feedback

LBDB-1057

(error) Found milkyway_layer_map group defined before '%s' group.

Description

This message indicates the named group in phys_library is not defined before milkyway_layer_map group.

The following example shows an instance where this message occurs:

```
phy_library(test) {
        ...
        milkyway_layer_group () {
         ...
        }
        resource ( std_cell ) {
          ...
        }
    }
```

The following is an example message:

```
Error: Line 59, Found milkyway_layer_group defined before 'resource'
 group. (LBDB-1001)
```

What Next

Move this group inside the physical library so that it is defined in front of milkyway_layer_map group.

LBDB-1058

(error) The '%s' color name is invalid.

Description

This message indicates that you specified an invalid color name for the current attribute or function. The color name should match a color name previously defined in the color groups.

The following example shows an instance where this message occurs:

```
color : foo ;
```

The following is an example message:

```
Error: Line 104, The 'foo' color name is invalid.  (LBDB-1058)
```

Feedback

What Next

Check your library to see if you have an error in either previous color definition or the current attribute / function.

LBDB-1059

(error) The '%s' '%s' name is invalid.

Description

This message indicates that you specified an invalid line_style/stipple name for the current attribute or function. The color name should match a line_style/stipple name previously defined in the line_style/stipple groups.

The following example shows an instance where this message occurs:

```
stipple : foo ;
```

The following is an example message:

```
Error: Line 104, The 'foo' 'stipple' name is invalid.  (LBDB-1059)
```

What Next

Check your library to see if you have an error in either previous line_style/stipple definition or the current attribute / function.

LBDB-1060

(error) The tile '%s' is not defined in the resource group.

Description

This message indicates name of the tile attribute is not a pre-defined tile.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          in_tile : new_tile;   /* error */
        }
    }
```

The following is an example message:

```
Error: Line 34, The tile 'new_tile' is not defined in the resource group.
 (LBDB-1060)
```

Feedback

What Next

Make sure the tile attribute uses a pre-defined tile.

LBDB-1061

(error) The %s shape has zero or negative area.

Description

This message indicates the path / polygon / rectangle function has zero or negative size. That is not a real geometrical shape.

The following example shows an instance where this message occurs:

```
phys_library(test) {
        ...
        macro(and2) {
          ...
          pin(a) {
            ...
            obs(new_layer) {
              rectangle(0.1, 0.3, 0.1, 0.3);  /* error */
            }
          }
        }
    }
```

The following is an example message:

```
Error: Line 34, The rectangle shape has zero area. (LBDB-1061)
```

What Next

Make sure it is a real geometry.

LBDB-1062

(error) The '%s' via name is invalid.

Description

This message indicates that you specified an invalid name for the current attribute or function. The via name should match a name previously defined in the resource group.

The following example shows an instance where this message occurs:

```
reference_cut_table( my_template ) {
        values ( "via12, via12a, via12b");
   }
```

Feedback

The following is an example message:

```
Error: Line 104, The 'via12a' via name is invalid.  (LBDB-1062)
```

What Next

Check your library to see if you have an error in either previous layer definition or the current attribute / function.

LBDB-1063

(warning) The argument value %d of the '%s' function\n \tis out of range. It is expected to be between 0 and 1.

Description

This message indicates that the out-of-range value has been set to the specified function.

```
pattern( 0, 1, 0, 1 );                /* correct */
```

The following example shows an instance where this message occurs:

```
pattern( 0, 20, 0, 1 );               /* incorrect */
```

The following is an example message:

```
Warning: Line 17, The argument value 20 of the 'pattern' function
        is out of range.  It is expected to be 0 or 1.  (LBDB-1063)
```

What Next

Change the physical library to correct the arguments.

LBDB-1064

(error) Invalid attribute '%s' value '%d' is detected. The value must be\n \tunique among all '%s' objects.

Description

This message indicates a non-unique id is found. - All via are required to have a unique via_id value. - All mask layers (device_layer, poly_layer, routing_layer, cont_layer) must have a unique mw_map id specified in its corresponding stream_layer group.

The following example shows an instance where this message occurs:

```
via (via12) {
    via_id : 12 ;
    ...
  }
  via (via23) {
```

```
    via_id : 12 ;
    ...
  }
```

The following is an example message:

```
Error: Line 56, Invalid attriute 'via_id' value '12' is detected.  The
 value must be
        unique among all 'via' objects. (LBDB-1064)
```

What Next

Make sure the specified id value is unique among all named objects.

LBDB-1065

(warning) No '%s' attribute has been specified for the\n \t%s '%s'. It is set to default value '%d'.

Description

This message indicates that the library, perhaps an older PLIB file, does not contain the newly required object id's and default values are assigned to it. - All via are required to have a unique via_id value, from 1 to 255. - All mask layers (device_layer, poly_layer, routing_layer, cont_layer) must have a unique mw_map id specified in its corresponding stream_layer group. Datatype in mw_map is always default to 0.

The following example shows an instance where this message occurs:

```
via (via12) {
    ...
  }
```

The following is an example message:

```
Warning: Line 56, No 'via_id' attribute has been specified for the
        via 'via12'.  It is set to default value '12'.  (LBDB-1065)
```

What Next

Enhance PLIB file to - specify a unique via_id for each via specification; - specify a corresponding stream_layer (with mw_map attribute) for each mask layer. These stream_layer should have unique mw_map layer id among them.

LBDB-1066

(warning) Cannot locate corresponding layer id and layer datatype\n \tfor display_layer '%s'. It is set to layer id %d and layer datatype %d.

Feedback

Description

This message indicates that the library, perhaps an older PLIB file, does not contain the newly required matching stream_layer object and mw_map(id, datatype) attribute values for all display_layer object. A unique mw_map(id, datatype) is automatically assigned to it.

The following example shows an instance where this message occurs:

```
display_layer (m1_pg) {
    ...
  }
```

The following is an example message:

```
Warning: Line 56,  Cannot locate corresponding layer id and layer
 datatype
for display_layer 'm1_pg'. It is set to layer id 23 and layer datatype
 '3'. (LBDB-1066)
```

What Next

Enhance PLIB file to - specify a corresponding stream_layer (with mw_map attribute) for each display layer. These stream_layer should have unique mw_map(id, datatype) value pair.

LBDB-1067

(error) The '%s' attribute value(s) is out of range.\n

Description

This message indicates that the gds_map or mw_map attribute has out-of-range values.

The acceptable value ranges are:

id <= 255 datatype <= 255 where mw_map (id , datatype); gds_map (id, datatype);

The following example shows an instance where this message occurs:

```
mw_map ( 23, 256 );
```

In this case, the datatype value 256 is out of range.

The following is an example message:

```
Error: Line 912, The 'mw_map' attribute' attribute value is out of range.
 (LBDB-1067)
```

What Next

Change the attribute value to satisfy the value range.

Feedback

LBDB-1068

(warning) Floating-point value %s in '%s' attribute is too precise and\n \twill be truncated to %s.

Description

This warning message occurs when the specified floating-point number cannot be completely stored in the database and must be rounded off.

When storing floating-point numbers in the database, the number is scaled by multiplying the floating-point number by dist_conversion_factor. Digits to the right of the decimal point are dropped. When nonzero digits are dropped, this message appears.

The following example shows an instance where this message occurs:

```
min_width : 0.1155 ;
```

The following is an example message:

```
Warning: Floating-point value 0.11550 in 'min_width' attribute is too
 precise and
         will be truncated to 0.115. (LBDB-1068)
```

What Next

This is a warning message only. No action is required.

However, if the result is not what you intended, you can increase the dist_conversion_factor or reduce the number of digits in the floating-point number, and then run the command again.

LBDB-1069

(error) The %s object '%s' has a width %d and height %d\n \tthat is inconsistent with the pattern size %d.

Description

This error message occurs when the pattern length of the specified section does not match the size specified by the pattern width and height. The number of elements in the pattern list must equal the product of the pattern width and height.

The following example shows an instance where this message occurs:

```
stipple ( S1 ) {
        width : 3 ;
        height : 2 ;
        pattern ( 1, 1, 0, 0 );
     }
```

Feedback

The following is an example message:

```
Error: Line 67, Stipple object 'S1'  has a width 3 and height 2
        that is inconsistent with the pattern size 4. (LBDB-1069)
```

What Next

Change the width and height attribute values or add or remove Boolean values to the pattern list. After making your changes, run the command again.

LBDB-1070

(warning) Layer '%s' has a pitch %.4f that is less than the minimum spacing\n \tand width sum %.4f.

Description

This warning message occurs when the specified Layer section contains an invalid pitch, minimum spacing or minimum width. The pitch must be greater than or equal to the sum of the layer's minimum spacing and minimum width.

The following example shows an instance where this message occurs:

```
layer ( M1 ) {
        min_width : 0.10 ;
        spacing : 0.12 ;
        pitch : 0.15 ;
     }
```

The following is an example message:

```
Warning: Line 24, Layer 'M1' has a pitch 0.1500 that is less than the
 minimum spacing
and width sum 0.2200.  (LBDB-1069)
```

What Next

This is a warning message only. No action is required.

However, if the result is not what you intended, change the pitch, minimum spacing, or minimum width to meet the requirement that the pitch be greater than or equal to the sum of the layer's minimum spacing and minimum width.

LBDB-1071

(warning) Routing_layer '%s' has invalid spacing_table value %.4f.

Feedback

Description

This warning message occurs when the specified routing_layer contains an invalid spacing_table value. The spacing_table values must be equal to or greater than the routing_layer spacing value.

The following example shows an instance where this message occurs:

```
layer ( M1 ) {
        spacing : 0.12 ;
        spacing_table (1d_table) {
          values (" 0.1 , 0.15, 0.24" );
        }
     }
```

The following is an example message:

```
Warning: Line 235, Routing_layer 'M1' has invalid spacing_table value
 0.100. (LBDB-1071)
```

What Next

This is only a warning message. No action is required.

However, it is best practice to change the spacing_table value of the specified routing_layer so the values are equal to or greater than the layer spacing value. After making your changes, run the command again.

LBDB-1072

(error) Routing_layer '%s' has invalid spacing_table value %.4f.

Description

This warning message occurs when the specified routing_layer contains an invalid spacing_table value. The spacing_table values must be equal to or greater than the routing_layer spacing value. And values[0] = spacing.

The following example shows an instance where this message occurs:

```
layer ( M1 ) {
        spacing : 0.12 ;
        spacing_table (1d_table) {
          values (" 0.1 , 0.15, 0.24" );
        }
     }
```

The following is an example message:

```
Error: Line 235, Routing_layer 'M1' has invalid spacing_table value
 0.100. (LBDB-1072)
```

Feedback

What Next

Change the spacing_table value so the value in the list are equal to or greater than the layer spacing value. After making your changes, run the command again.

LBDB-1073

(warning) Layer '%s' has a pitch %.4f that does not match the recommended\n \twire-to-via pitch %.4f.

Description

This warning message occurs when the pitch of the specified layer does not match the recommended pitch. The wire-to-via pitch is the recommended pitch and provides the best wire track resources for routing.

The wire-to-wire pitch is more aggressive, the via-to-via is more conservative and neither are recommended. The metal layer pitch must match the wire-to-via pitch in the routing direction.

The horizontal wire-to-via pitch is calculated as follows:

```
(min spacing) + (min width)/2 + (via metal width)/2

The vertical wire-to-via pitch is calculated as follows:

    (min spacing) + (min width)/2 + (via metal height)/2
```

The via metal width and height are based on the larger of the lower and upper default contact codes.

The following example shows an instance where this message occurs:

```
layer ( metal3 ) {
        spacing : 1.9;
        min_width : 1.8;
        pitch : 4.5;
        ...
     }

     via (via23) {
        ...
        via_layer(metal3) {
          rectangle ( -1.1, -1.1, 1.1, 1.1 );
        }
     }
     via (via34) {
        ...
        via_layer(metal3) {
          rectangle  ( -1.1, -1.1, 1.1, 1.1 );
```

```
        }
     }
```

The following is an example message:

```
Warning : Line 36, Layer 'metal3' has a pitch 4.500 that does not match
 the recommended
        wire-to-via pitch 3.900. (LBDB-1073)
```

What Next

This is only a warning message. No action is required.

You can leave the pitch of the specified layer at the current setting, or you can change the pitch of the layer to the recommended pitch.

LBDB-1074

(warning) Layer '%s' has a pitch %.4f that is not aligned with\n \tbottom layer pitch %.4f.

Description

This warning message occurs when the pitch of the specified layer is not double or triple the pitch of the lower metal layer with the same routing direction. Doubling or tripling the pitch value, maximizes routing resources and minimizes overlap with other metal layers.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
        pitch : 1.9;
        ...
     }
        ...
     layer ( metal3 ) {
        pitch : 3.9;
        ...
     }
```

The following is an example message:

```
Warning : Line 36, Layer 'metal3' has a pitch 3.900 that is not aligned
 with
        bottom layer pitch 1.900. (LBDB-1074)
```

What Next

This is only a warning message. No action is required.

You can either leave the pitch of the specified layer unchanged, or change the pitch to the doubled or tripled pitch and run the command again.

Feedback

LBDB-1075

(error) The attribute '%s' has %d entries, which exceeds the maximal\n \tallowed 8 entries.

Description

This error message occurs when the specified index array in routing_layer/cont_layer group that is too large. The index array size must be beween 1 and 8 inclusive.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
        spacing_table ( 1d_stable ) {
          index_1 (0.0, 1.3, 2.4, 4.5, 6.6, 7.1, 9.3, 12.2, 25.0, 33.9);
        }
        ...
     }
```

The following is an example message:

```
Warning : Line 36, The attribute 'index_1' has 10 entries, which exceeds
 the maximal
        allowed 8 entries. (LBDB-1075)
```

What Next

Change the index array so that it does not exceed 8 entries. Then run the command again.

LBDB-1076

(warning) The attribute '%s' has invalid threshold values %.4f.

Description

This warning message occurs when the specified table index contains an invalid threshold values. The threshold list must meet the following requirements:

- The first value must be between 0 and the default_routing_width inclusively.
- The second value must be greater than the layer min_width.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
        min_width : 1.5 ;
        spacing_table ( 1d_stable ) {
          index_1 (0.0, 1.3, 2.4, 4.5, 6.6, 7.1, 9.3, 12.2, 25.0, 33.9);
          ...
        }
        ...
     }
```

Feedback

The following is an example message:

```
Warning : Line 36, The attribute 'index_1' has invalid index value 1.3.
 (LBDB-1076)
```

What Next

This is only a warning message. No action is required.

However, it is best practice to change the index values to meet the above requirements. After making your changes, run the command again.

LBDB-1077

(error) The attribute '%s' has invalid threshold values %.4f.

Description

This warning message occurs when the specified table index contains an invalid threshold values. The threshold list must meet the following requirements:

- The first value must be between 0 and the min_width inclusively.
- The second value must be greater than the layer min_width.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
        min_width : 1.5 ;
        spacing_table ( 1d_stable ) {
          index_1 (0.0, 1.3, 2.4, 4.5, 6.6, 7.1, 9.3, 12.2, 25.0, 33.9);
          ...
        }
        ...
     }
```

The following is an example message:

```
Error : Line 36, The attribute 'index_1' has invalid index value 1.3.
 (LBDB-1077)
```

What Next

Change the index values to meet the above requirements. After making your changes, run the command again.

LBDB-1078

(error) Layer '%s' has a default_routing_width value %.4f that is less than its\n \tmin_width value %.4f.

Feedback

Description

This error message occurs when the default width or minimum width of the specified Layer section is invalid. The default width (default_routing_width) of each layer must be greater than or equal to its minimum width (min_width).

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
        min_width : 1.5 ;
        default_routing_width : 1.3;
          ...
        }
        ...
     }
```

The following is an example message:

```
Error : Line 36, Layer 'metal1' has a default_routing_width value 1.3000
 that is less than its
        min_width value 1.5000. (LBDB-1078)
```

What Next

Change the default_routing_width or min_width of the specified Layer section so that the default_routing_width is greater than or equal to the min_width. After making your changes, run the command again.

LBDB-1079

(warning) The attribute '%s' has rounded threshold value %.4f.

Description

This warning message occurs when the threshold value from the index array contains rounded values. It is best practice to avoid ending threshold values with a 0 digit in the most precise position. This practice minimizes the confusion between tools that interpret the thresholds as exclusive, rather than inclusive, lower bounds.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
        spacing_table ( 1d_spacing ) {
          index_1 ( "0.0, 1.500, 3.015" );
          ...
        }
        ...
     }
```

Feedback

The following is an example message:

```
Warning : Line 36, The attribute 'index_1' has rounded threshold value
 1.5000. (LBDB-1079)
```

What Next

This is only a warning message. No action is required.

However, you can either increase the rounded threshold value by one grid resolution value and run the command again, or you can leave the threshold value at the current setting.

LBDB-1080

(warning) Attribute '%s' has insignificant differences between\n \tthreshold values %.4f and %.4f.

Description

This warning message occurs when the index threshold contains insignificant differences between the threshold values. It is best practice to have thresholds differ by more than half of the min_width and more than ten percent of the greater threshold. If they do not differ by these amounts, then the table values can contain redundant data, be unnecessarily large, and increase router run-time dramatically.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
        min_width : 1.5;
        spacing_table ( 1d_spacing ) {
          index_1 ( "0.0, 1.905, 1.915" );
          ...
        }
        ...
     }
```

The following is an example message:

```
Warning : Line 36, The attribute 'index_1' has insignificant differences
 between
        threshold values 1.9050 and 1.9150. (LBDB-1080)
```

What Next

This is only a warning message. No action is required.

However, you can check the table values for redundant data. If you find redundant data, then reduce the index dimension and the number of threshold values. After making your changes, rerun the command.

Feedback

LBDB-1081

(warning) Routing layer '%s' does not contain positive min_enclosed_area value.

Description

The value of the *minEnclosedArea* attribute for default metal layers should be greater than 0. Other values can affect the quality of the application results and can cause excessive design rule constraint violations during physical verification.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
          ...
     }
```

The following is an example message:

```
Warning : Line 36, Routing layer 'metal1' does not contain positive
 min_enclosed_area value. (LBDB-1081)
```

What Next

This is only a warning message. No action is required.

However, it is best practice to check the min_enclosed_area or min_enclosed_area_table attribute value of the specified layer, and then change the value to a value greater than 0, if necessary. After making your changes, run the command again.

LBDB-1082

(error) The u_shaped_wire_spacing attribute value %.4f in routing layer '%s'\n \tis less than spacing value %.4f.

Description

This message indicates that the u_shaped_wire_spacing value is less than the spacing value, which is not allowed. It is required that u_shaped_wire_spacing attribute value be no less than the spacing attribute value of the same routing layer.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
          spacing : 1.4;
          u_shaped_wire_spacing : 1.0;
          ...
     }
```

Feedback

The following is an example message:

```
Error : Line 45, The u_shaped_wire_spacing attribute value 1.0000 in
 routing layer 'metal1'
        is less than the spacing attribute value 1.400. (LBDB-1082)
```

What Next

Change u_shaped_wire_spacing value so that it is equal or more than the spacing value. Then run the command again.

LBDB-1083

(error) The same_net_min_spacing attribute value %.4f in routing layer '%s'\n \tis more than spacing value %.4f.

Description

This message indicates that the same_net_min_spacing value is more than the spacing value, which is not allowed. It is required that same_net_min_spacing be no more than the spacing attribute value of the same routing layer.

The following example shows an instance where this message occurs:

```
layer ( metal1 ) {
          spacing : 1.4;
          same_net_min_spacing : 1.7;
          ...
     }
```

The following is an example message:

```
Error : Line 45, The same_net_min_spacing attribute value 1.7000 in
 routing layer 'metal1'
        is more than the spacing attribute value 1.400. (LBDB-1083)
```

What Next

Change same_net_min_spacing value so that it is equal or less than the spacing value. Then run the command again.

LBDB-1084

(warning) Tile '%s' has size %.4f that is not a multiple of\n \t%s routing layer pitch %.4f.

Description

This warning message occurs when: - in horizontal floorplan, tile width is not consistent with first vertical routing layer pitch; or - in vertical floorplan, tile height is not consistent with first horizontal routing layer pitch.

Feedback

It is recommended that the tile dimension lines up with pitch to maximize utilization.

The following example shows an instance where this message occurs:

```
layer ( metal2 ) {
          routing_direction : vertical ;
          pitch : 1.4;
          ...
     }
        ...
     tile (unit) {
          size ( 1.6, 5.5 );
          ..
     }
```

The following is an example message:

```
Warning : Line 45, Tile 'unit' has size 1.6000 that is not a multiple of
        metal2 routing layer pitch 1.4000. (LBDB-1084)
```

What Next

This is a warning message only. No action is required.

However, it is best practice to either change the size value in question to the suggested pitch, or change the specified routing layer pitch to match tile dimension. After making your changes, run the command again.

LBDB-1085

(error) Cannot find via defined for contact layer '%s'.

Description

This error message occurs when there is no via defined with a specific contact layer between 2 metal layers.

At least one via must be defined between 2 metal layers in a library.

The following is an example message:

```
Error : Cannot find via defined for contact layer 'via12'. (LBDB-1085)
```

What Next

Define at least one via for the contact layer. Run the command again.

LBDB-1086

(warning) The %s attribute value in via '%s' specifies\n \tnon-positive metal enclosure.

Feedback

Description

This warning message occurs when the specified via section contains non-positive metal enclosure dimensions or non-positive enclosure metal rectangle. If the non-positive metal enclosure values are set intentionally, this warning can be ignored. Otherwise, the values may cause the router to create enclosures that violate design rule constraints, such as completely enclosed spaces or donuts.

The following example shows an instance where this message occurs:

```
via ( via12 ) {
        via_layer( metal1 ) {
          enclosure ( 0, 0 );
        }
     }
```

The following is an example message:

```
Warning : Line 45, The enclosure attribute value in via 'via12' specifies
        non-positive metal enclosure. (LBDB-1086)
```

What Next

This is a warning message only. No action is required.

However, if the zero metal enclosure values are not intentional, you can change either the rectangle coordinates or change enclosure value in via group to avoid potential design rule violations.

LBDB-1088

(warning) There are more than 255 layers in this library.

Description

This warning message occurs when more than 255 layers are found in the current library. It does not include display layers. Currently Milkyway database can accommodate up to 255 layers. Upper layers exceeding the limit will be ignore in the database.

The following is an example message:

```
Warning : There are more than 255 layers in this library. (LBDB-1088)
```

What Next

This is a warning message only. No action is required.

However, it is best practice to make sure that the total number of layers do not exceed the limit. After making your changes, run the command again.

Feedback

LBDB-1089

(warning) '%s' and '%s' layers in %s attribute are not\n \tadjacent layers.

Description

This warning message occurs when the 2 layers specified in: - same_net_min_spacing - diff_net_min_spacing - contact_min_spacing - corner_min_spacing - min_overhang - min_enclosure - end_of_line_enclosure complex attributes are not adjacent layers.

It is recommended that the 2 layers must be adjacent routing or contact layers.

The following example shows an instance where this message occurs:

```
diff_net_min_spacing ( met1, met4, 1.4 );
```

The following is an example message:

```
Warning : Line 45, 'met1' and 'met3' layers in diff_net_min_spacing
 attribute are not
        adjacent layers. (LBDB-1089)
```

What Next

This is a warning message only. No action is required.

However, it is best practice to follow the above guideline. After making your changes, run the command again.

LBDB-1090

(warning) Cannot find matching stream_layer for layer '%s'.

Description

This warning message occurs when the layer is specified in resource layer section, but no stream_layer with identical name can be found in milkyway_layer_map group.

It is recommended that a stream_layer is defined for each layer found in resource group.

The following is an example message:

```
Warning : Cannot find matching stream_layer for layer 'metal1'.
 (LBDB-1090)
```

What Next

This is a warning message only. No action is required.

However, it is best practice to add stream_layer definition for the specified layer. After making your changes, run the command again.

Feedback

LBDB-1091

(warning) Reset density value from %4.1f to %4.1f.

Description

Density value defined in density_property in PLIB file should be between 0.0 and 100.0. Else, it will be reset to 0.0 or 100.0.

The following is an example message:

```
Warning: Line 12, Reset density value from 101.6 to 100.0. (LBDB-1091)
```

What Next

Revise density value if the reset value is not expected.

LBDB-1092

(warning) Layer '%s' attribute '%s' has a value of %g.

Description

This warning message occurs when the value of the specified layer attribute may not be optimal.

The values can affect the quality of the application results and can cause excessive design rule constraint violations during physical verification.

For a set of rule, completeness of rule parameters should be maintained:

For enclosed via min edge length rule, if enclosed_via_min_edge_length is specified, min_edge_length should be specified, and enclosed_via_min_edge_length > min_edge_length > 0

For U-shape rule, if you specify u_shaped_min_length or u_shaped_wire_spacing, you should also specify u_shaped_min_depth and min_spacing. And u_shaped_wire_spacing > min_spacing.

For multiple min area rule, "min_area" attribute is needed if "min_polygon_area_rule() -> polygon_min_area" is specified and min_polygon_area_rule()->polygon_min_area > min_area. If both "min_polygon_area_rule() -> polygon_min_area" and "min_polygon_area_rule() -> max_edge_length" are specified, "min_length" should be specified. And min_polygon_area_rule() -> max_edge_length >= min_length

For non-preferred direction routing rule, if you specify non_preferred_dir_width, it will satisfy non_preferred_dir_width > default_routing_width. If you specify both non_preferred_dir_width and non_preferred_dir_max_length, it will satisfy non_preferred_dir_max_length > non_preferred_dir_width-default_routing_width.

Feedback

For min_spacing rule in routing_layer, if you specify min_spacing(x_min_spacing, y_min_spacing), it will satisfy x_min_spacing >= spacing and y_min_spacing >= spacing.

For jog wire corner to corner spacing rule, if you specify aligned_jog_width and unaligned_jog_diag_width, it will satisfy aligned_jog_width >= min_width and unaligned_jog_diag_width >= min_width.

For [x|y]_min_spacing_table, [x|y]_max_spacing_table, the first value, i.e., value[0], will satisfy value[0] >= spacing.

For [x|y]_max_spacing_check_range_table, the first value, i.e., value[0], will satisfy value[0] >= spacing*2 + min_width.

The following is an example message:

```
WARNING : Layer 'M1' attribute 'polygon_min_area' has a value of 0.03.
 (LBDB-1092)
```

What Next

This is only a warning message. No action is required.

However, it is best practice to check the attribute value of the specified layer, and then change the value to a value greater than 0, if necessary. After making your changes, run the command again.

LBDB-1093

(warning) Layer '%s' attribute '%s' is missing.

Description

This warning message occurs when the specified section is missing an important attribute. If the attribute is not specified in PLIB file, the default value is 0 for number attributes, or an empty string for string attributes.

For multiple min area rule, "min_area" attribute is needed if "min_polygon_area_rule() -> polygon_min_area" is specified and min_polygon_area_rule()->polygon_min_area > min_area. If both "min_polygon_area_rule() -> polygon_min_area" and "min_polygon_area_rule() -> max_edge_length" are specified, "min_length" should be specified.

For U-shape rule, if you specify u_shaped_min_length or u_shaped_wire_spacing, you should also specify u_shaped_min_depth and min_spacing.

For enclosed via min edge length rule, if enclosed_via_min_edge_length is specified, min_edge_length should be specified, and enclosed_via_min_edge_length > min_edge_length > 0 If both enclosed_via_min_edge_length and min_edge_length are specified, enclosed_via_adjacent_edge_length should be specified.

Feedback

For 2-line end rule, if end_to_end_min_spacing is specified, end_of_line_metal_max_width should be specified.

For end of line rule, if end_of_line_side_keepout_length is specified, end_of_line_metal_max_width should be specified.

For line end depth rule, if end_of_line_min_length is specified, end_of_line_metal_max_width should be specified.

The following is an example message:

```
WARNING : Layer 'M1' attribute 'min_area' is missing. (LBDB-1093)
```

What Next

This is only a warning message. No action is required.

However, if you do not want to use the default value for the attribute, add the attribute with the desired value to the specified section in PLIB file and rerun the command.

LBDB-1094

(error) The table '%s' can supports 'scalar' template only.

Description

This error message is reported for some table groups, that currently only a scalar value is supported for them by the tool. But found they are using a non-scalar template name.

Following two groups are under the restriction for now:

```
pgate_antenna_ratio(template_name) {
}
ngate_antenna_ratio(template_name) {
}
```

The following is an example message:

```
Error: Line 531, The table 'pgate_antenna_ratio' can supports 'scalar'
 template only. (LBDB-1094)
```

What Next

Modify the plib file accordingly, change the template name to 'scalar' and specify only one value for the table.

Example:

```
antenna_rule("M1_ANTENNA_RULE")
    ...
    pgate_antenna_ratio("antenna_tempalte1") {
        index_1 ("0.0 1.0 2.0 3.0")
```

Feedback

```
        values ("200 200 400 600");
    }
}
```

Modify the group to:

```
antenna_rule("M1_ANTENNA_RULE")
    ...
    pgate_antenna_ratio("scalar") {
        values ("200");
    }
}
```

LBDB-1095

(error) The '%s' should coexist with '%s' in '%s' group.

Description

This error message is reported when there is restriction that two tables/functions/attributes should coexist the group, but only one found.

Example:

In antenna_rule group, the pgate_antenna_ratio table should coexist with ngate_antenna_ratio. If any of the other is not specified when one is present, the error is reported.

```
antenna_rule (M1_mode1_d4) {
    antenna_ratio ("antenna_tempalte") {
        index_1("0, 0.05 0.06 0.6");
        values("100 100 300 500");
    }
    pgate_antenna_ratio("scalar") {
        values("100");
    }
    layer_antenna_factor("M1", 1.0);
}
```

The following is an example message:

```
Error: Line 546, The 'pgate_antenna_ratio' should coexist with
 'ngate_antenna_ratio' in 'antenna_rule' group. (LBDB-1095)
```

What Next

Modify the plib file accordingly, specify both tables/attributes/functions in the group. or remove the existing one.

Feedback

LBDB-1096

(error) There is unsupported antenna data in the group.

Description

This error message is reported when there is unsupported antenna data found in the antenna_rule group. Mainly, the error is issued for following situations:

1. Usage of pgate_antenna_ratio and ngate_antenna_ratio
   pgate_antenna_ratio and ngate_antenna_ratio can't be supported when: antenna_accumulation_calculation_method : accumulative_ratio; with routing_layer_calculation_method : top_area|side_wall_area;

Note that when reading a plib file to Milkyway library, antenna_accumulation_calculation_method is default to accumulative_ratio and routing_layer_calculation_method is default to top_area;

So, if you want to define pgate_antenna_ratio and ngate_antenna_ratio in the antenna_rule group, you can't leave these two attributes undefined, otherwise, this error will be issued too.

1. Usage of antenna area rule The antenna_rule group is defined as antenna area rule, when antenna_ratio_calculation_method == total_routing_area. And there is restrcitions to antenna_accumulation_calculation_method and geometry_calculation_method, according to current tool support. Following combinations are supported now, this error will be issued for other combinations. mode 1: calculate metal area ignore all lower layer segments. antenna_accumulation_cm = single_layer, geometry_cm = connected_only; mode 2: calculate metal area includes lower layer segments to input pins. antenna_accumulation_cm = accumulative_area, geometry_cm = connected_only; mode 3: calculate metal area includes all lower layer segments. antenna_accumulation_cm = accumulative_area, geometry_cm = all_geometries;

Besides above three calculation methods, the antenna_ratio should using scalar template and have only one value defined as max allowable antenna area, attribute max_diode_insertion_distance is used to define max allowable distance from inserted diode to gate.

other attributes and groups defined in antenna area rule are totally ignored during read_plib and not stored into database.

The following is an example message:

```
Error: Line 546, There is unsupported antenna data in the
 group.(LBDB-1096)
```

Feedback

What Next

Modify the plib file accordingly to rule above.

LBDB-1097

(error) Layer '%s' attribute '%s' and '%s' are different.

Description

x_min_spacing_table, y_min_spacing_table, x_max_spacing_table, y_max_spacing_table, x_max_spacing_check_range_table, y_max_spacing_check_range_table currently require the content in index_1 and index_2 are the same.

If both exist, the dimension and content in index_1[] in fat_wire_via_keepout_enclosure_table and in fat_wire_via_keepout_edge_table should be the same.

If both exist, the dimension and content in index_1[] in fat_wire_via_keepout_enclosure_table and in fat_wire_via_spacing_threshold_table should be the same.

The following is an example message:

```
Error : Layer 'M1' attribute 'x_min_spacing/index_1' and
 'x_min_spacing/index_2' are different. (LBDB-1097)
```

What Next

Unify the different elements.

LBDB-1098

(error) Layer '%s' has wrong '%s'.

Description

Values in x_legal_width and y_legal_width should satisfy, (1) the width values are in ascending order; (2) the first value >= min_width; (3) the last value <= max_width if max_width is specified; (4) default_routing_width is among the values.

The following is an example message:

```
Error : Layer 'M1' has wrong 'x_legal_width'. (LBDB-1098)
```

What Next

Re-specify x_legal_width or y_legal_width.

Feedback

LBDB-1099

(error) Layer '%s' '%s' and '%s' can't co-exist.

Description

fat_wire_via_keepout_edge_table and fat_wire_via_spacing_threshold_table can't co-exist in a cont_layer.

The following is an example message:

```
Error : Layer 'M1' 'fat_wire_via_keepout_edge_table' and
 'fat_wire_via_spacing_threshold_table' can't co-exist. (LBDB-1099)
```

What Next

Remove at least one of the two given attributes/functions/groups.

LBDB-1100

(information) Dummy cell '%s' defined in the library.

Description

This info message is reported when there is dummy cell defined in an incremental plib file (that is, the library attribute is_incremental_library : true;)

A dummy cell is identified by following features: 1. The cell name has wildcard '*' used, and the '*' is the last character in the cell name, for example, cell name is "*", or "AND*". 2. There is no cell geometries (macro obs, pin port) defined in the cell.

A dummy cell is expected only in an incremental plib file, and it's used to update cell/pin attributes for FRAM view cells when read plib data to Milkyway database.

What Next

Users do not need to do anything.

LBDB-1101

(error) There is geometry data defined in dummy cell '%s'.

Description

This warning message is reported when there is geometry data defined in the dummy cell.

A dummy cell is identified by following features: 1. The cell name has wildcard '*' used, and the '*' is the last character in the cell name, for example, "*" or "AND*". 2. There is no cell geometries (macro obs, pin port) defined in the cell.

A dummy cell is expected only in an incremental plib file, and it's used to update cell/pin attributes for a set of FRAM view cells (pattern matched cells) when read plib data to Milkyway database.

The following is an example message:

```
Error: Line 546, There is geometry data defined in dummy cell
 '*'.(LBDB-1101)
```

What Next

Remove all geometry data from the cell (macro obs, pin port) if users want to use dummy cell to update cell/pin attributes for a set of cells. Otherwise, rename the cell name to avoid it match with dummy cell naming rule.

LBDB-1111

(error) Incorrect number of arguments specified in '%s' attribute.

Description

This message indicates the number of arguments for an attribute does NOT meet one of the requirements: minimum/maximum number, even/odd number, multiples of certain number, etc.

The following example shows an instance where this message occurs:

```
library(test) {
        ...
        cell(testcell) {
          example(1, 2);            /* line 20 */
        }
    }
```

The requirement is the number of argument of 'example' attribute should be odd and bigger than 2.

The following is an example message:

```
Error: Line 20, Cell 'cell1', Incorrect number of arguments specified in
 'example' attribute. (LBDB-1111)
```

What Next

Make sure the correct argument is used for the attribute.

LBDB-1112

(error) Different number of arguments found in '%s' attributes declared under this %s group.

Feedback

Description

This message indicates this multiply declared attribute under the same parent group have different number of Arguments. The numbers of arguments should be identical among them.

The following example shows an instance where this message occurs:

```
library(test) {
        ...
        cell(testcell) {            /* line 19 */
          example(1, 2, 3);
          example(1, 2, 3, 4, 5);
        }
    }
```

The following is an example message:

```
Error: Line 19, Cell 'cell1', Different number of arguments found in
 'example' attributes declared under this 'cell' group. (LBDB-1112)
```

What Next

Make sure the correct argument is used for the attributes.

LBDB-1150

(error) Invalid value in end_of_line_via_wire_rule.

Description

Name the five values in end_of_line_via_wire_rule as layer1, layer2, end_of_line_via_wire_min_width, end_of_line_via_wire_min_spacing, end_of_line_via_ortho_wire_max_threshold, respectively.

Suppose layer1 is routing_layer, and layer2 is cont_layer. default_via is the default via on layer2. Taking min_width and min_spacing specification from layer1, and compute cut_width by the geometry of default_via.

If there is another design rule for this layer pair

min_enclosure (string, string, float); /* layer1, layer2, min_enclosure */

Take min_enclosure from this specification. Otherwise let min_enclosure=0.

Values should satisfy, (1) end_of_line_via_wire_min_width > min_width (2) end_of_line_via_wire_min_width >= cut_width + 2* min_enclosure (3) end_of_line_via_wire_min_spacing >= min_spacing + min_enclosure (4) end_of_line_via_ortho_wire_max_threshold >= minWidth

Feedback

The following is an example message:

```
Error : Invalid value in end_of_line_via_wire_rule. (LBDB-1150)
```

What Next

Change the value to satisfy all the 4 restrictions.

LBDB-1151

(error) "%s" has invalid value %f.

Description

same_segment_center_min_spacing, same_net_center_min_spacing, diff_segment_center_min_spacing, diff_net_center_min_spacing in cont_layer() group or in topological_design_rules() group should satifsy, [same|diff]_[segment|net]_center_min_spacing >= min_cut_spacing + cut_width

The value of min_cut_spacing and cut_width is explained as follows.

As for [same|diff]_[segment|net]_center_min_spacing in cont_layer() group, let "default_via" to be the default via of this cont_layer. Then min_cut_spacing is taken from contact_spacing specification. Cut_width is taken from the geometry of default_via.

As for [same|diff]_[segment|net]_center_min_spacing in topological_design_rules() group, we only check if both layer1 and layer2 are cont_layers. Let "default_via_1" to be the default via on layer1, "default_via_2" to be the default via on layer2. min_cut_spacing is taken from the function in topological_design_rule():

contact_min_spacing (layer1, layer2, min_cut_spacing)

Cut_width_1 and cut_width_2 are taken from the geometry of default_via_1 and default_via_2, respectively. Let cut_width = (cut_width_1+cut_width_2)/2.

The following is an example message:

```
Error : "diff_segment_center_min_spacing" has invalid value 0.12.
 (LBDB-1151)
```

What Next

Change the value to satisfy the restriction.

LBDB-1152

(error) The '%s' attribute has an invalid sequence of\n \tdata '%g , %g'. The values must be in decreasing order.

Feedback

Description

This message indicates that the set of data is not specified in decreasing order. Content in "values" in min_metal_spacing_table must be in descending order.

The following is an example message:

```
Error: Line 22, The 'values' attribute has an invalid sequence of
        data '1.200000 , 2.300000'. The values must be in decreasing
 order. (LBDB-1152)
```

What Next

Check your library and correct the order of the values.

LBDB-1153

(error) '%s' has 0 or more than %d arguments.

Description

[x|y]_legal_width requires that the argument number is greater than 0 and less than or equal to 16.

The following is an example message:

```
Error: Line 22, 'x_legal_width' has 0 or more than 16 arguments.
 (LBDB-1153)
```

What Next

Add or reduce arguments into the specified function.

LBDB-1154

(error) There is no noise information in the library.

Description

This information occurs when checking library for noise information, but there is no noise information in the library at all.

What Next

If noise information is not needed, cancel the noise checking; If noise information is needed, add I-V characteristics, noise immunity data and noise propagation data.

Feedback

LBDB-1155

(error) Invalid %s found under section %s in map file.

Description

In the map file, if any of the following is incorrect, (1) voltage_name (2) voltage value (3) power management attributes this message will occur.

Valid voltage_name should be a valid string that starts with a character a-z or A-Z. The voltage_name in PG_TO_VOLTAGE_MAP section should be one in VOLTAGE_MAP. It could be a rail name, and could be the same as pg_pin name. But never input an invalid value such as "-" or "*" in voltage_name field in PG_TO_VOLTAGE_MAP or VOLTAGE_MAP section. Valid voltage values are non-negative floating point numbers, for example, 0.9, that are valid voltage values in the input library. For valid power management attributes, please refer to related documents or user guide. The following are only a few examples: valid switch_cell_type is coarse_grain and fine_grain; valid level_shifter_type is HL, LH and HL_LH; always_on pins are related to backup power; a switch cell has VVDD+VDD or VVSS+VSS, and. VVDD has pg_function where VVDD is virtual VDD.

The following example shows an instance where this message occurs:

```
BEGIN PG_TO_VOLTAGE_MAP
cell            pg_pin          voltage_name    pg_type
ADDFHX1         VDD             -       power
ADDFHX1         VSS             VSS             primary_ground
GEND PG_TO_VOLTAGE_MAP
```

The following is an example message:

```
Error: Line 14, Invalid voltage_name found under section
 PG_TO_VOLTAGE_MAP in map file. (LBDB-1155)
```

What Next

You should correct the invalid values and/or voltage_name in the map file. For example, in voltage_name field, if you enter "-", you will receive this message. You must input a valid voltage_name, e.g. VDD.

LBDB-1156

(warning) private variable '%s' is enabled. Do not use the compiled DB in design flow.

Description

This message indicates that a pribate variable is enabled when compiling the DB. The compiled DB file may cause design flow fail.

Feedback

What Next

Disable the private variable and recompile the DB file.

LBDB-1157

(warning) The direction of pg_pin '%s' can only be input or inout when pg_type is '%s'!

Description

You receive this message when pg_type is primary_power or primary_ground but the pg_pin direction is output.

The following example shows an instance where this message occurs:

```
cell(lbdb1157) {
      area : 9;
      pg_pin(VDD) {
        direction : output ;
        pg_type : primary_power;
        voltage_name :VDD;
      }
      pg_pin(VSS) {
        pg_type : primary_ground;
        voltage_name :VSS;
      }
    }
```

In this case, direction of pg_pin VDD is output but its pg_type is primary_power.

The following is an example message:

```
Warning: Line 848, The direction of pg_pin 'VDD' can only be input or
 inout when pg_type is 'primary_power'! (LBDB-1157)
```

What Next

Correct the direction or pg_type

LBDB-1158

(error) Multiple '%s' groups found when same group with type 'both' is defined at line %d!

Description

You receive this message when more than one specified group are specified and the 'type' attribute in one of the group is 'both'.

Feedback

The following example shows an instance where this message occurs:

```
cell(lbdb1158) {
    tap_cell_properties() {
        type : both;
        coverage_distance (23, 10) ;
        min_row_edge_distance : 12;
        coverage_pattern_left : left_full ;
        coverage_pattern_right : right_full;
    }
    tap_cell_properties() {
        type : nwell ;
        coverage_distance (10, 23) ;
        min_row_edge_distance : 16;
        coverage_pattern_left : left_full ;
        coverage_pattern_right : right_full;
  }
}
```

In this case, two tap_cell_properties are specified

The following is an example message:

```
Error : Line 1000, Multiple 'tap_cell_properties' groups found when same
 group with type 'both' is defined at line 1001! (LBDB-1158)
```

What Next

Remove one of the group.

LBDB-1159

(error) The value of '%s' cannot be less than %d!

Description

You receive this message when the value in the attribute is less than minimum allowed number.

The following example shows an instance where this message occurs:

```
cell(lbdb1158) {
    tap_cell_properties() {
        type : both;
        coverage_distance (-1, 10) ;
        min_row_edge_distance : 12;
        coverage_pattern_left : left_full ;
        coverage_pattern_right : right_full;
    }
}
```

In this case, value in coverage_distance is less than 0

Feedback

the following is an example message:

```
Error : Line 1000,  The value of 'coverage_distance' cannot be less than
 0!
```

What Next

Remove one of the group.

LBDB-1161

(error) The attribute '%s' is required for %s.

Description

This message indicates that the required attribute on the specified pin is missing.

For single rail no enable isolation cell, it is a requirement that the output pin has attribute 'alive_during_partial_power_down'.

The following example shows an instance where this message occurs:

```
cell(Isolation_Cell) {
  is_isolation_cell : true;
  pg_pin(DVDDB) {
    voltage_name : DVDDB;
    pg_type : primary_power;
  }
  pg_pin(VSS) {
    voltage_name : VSS;
    pg_type : primary_ground;
  }
  pin(D) {
    direction : input;
    related_power_pin : DVDDB;
    related_ground_pin : VSS;
    isolation_cell_data_pin : true;
  }
  pin(Z) {
    direction : output;
    related_power_pin : DVDDB;
    related_ground_pin : VSS;
    function : "D";
    clamp_0_function : "!DVDDB";
    power_down_function : "VSS";
      timing() {
        related_pin : "D";
        …
      } /* end timing group */
  }/* end pin group*/
}/*end cell group*/
```

Feedback

In this case, the alive_during_partial_power_down is missing in pin Z.

The following is an example message:

```
Error: Line 326, Cell 'Isolation_Cell', pin 'Z', The attribute
 'alive_during_partial_power_down' is required for single rail no enable
 isolation cell. (LBDB-137)
```

What Next

Add required attribute to the output pin.

LBDB-1162

(error) The %s pin '%s' in %s cannot be used in %s!

Description

This message indicates that the pin name should not be in the function.

If pg_function is MUX21, the signal pin used in switch_function should be a different signal pin from pg_function.

The following example shows an instance where this message occurs:

```
cell(LBDB-1162) {
switch_cell_type : coarse_grain;
   pg_pin (VDD) {
        direction : output;
        pg_function : "VDDB * A + !A * VDDA";
        pg_type : internal_power;
        switch_function : "!(A|B)";
        voltage_name : "VDD";
   }

}/*end cell group*/
```

In this case, A cannot be used in switch_function as A is used in pg_function

The following is an example message:

```
Error: Line 326, The signal pin 'A' in switch_function cannot be used in
 pg_function! (LBDB-1162)
```

What Next

remove the signal pin from switch_function.

LBDB-1162w

(warning) The %s pin '%s' in %s cannot be used in %s!

Feedback

Description

This message indicates that the pin name should not be in the function.

If pg_function is MUX21, the signal pin used in switch_function should be a different signal pin from pg_function.

The following example shows an instance where this message occurs:

```
cell(LBDB-1162w) {
switch_cell_type : coarse_grain;
   pg_pin (VDD) {
        direction : output;
        pg_function : "VDDB * A + !A * VDDA";
        pg_type : internal_power;
        switch_function : "!(A|B)";
        voltage_name : "VDD";
   }

}/*end cell group*/
```

In this case, A cannot be used in switch_function as A is used in pg_function

The following is an example message:

```
Warning: Line 326, The signal pin 'A' in switch_function cannot be used
 in pg_function! (LBDB-1162w)
```

What Next

remove the signal pin from switch_function.

LBDB-1163

(error) Invalid pg_function '%s' found for switch cell!

Description

This message indicates that pg_function format is incorrect.

For switch cell, pg_function can only be a single pg_pin, or two pg_pins and one or more signal pins in a MUX21 format (signal pins are the select pins).

The following example shows an instance where this message occurs:

```
cell(LBDB-1162) {
switch_cell_type : coarse_grain;
   pg_pin (VDD) {
        direction : output;
        pg_function : "VDDB * VDDA";
        pg_type : internal_power;
        switch_function : "!(A|B)";
```

```
        voltage_name : "VDD";
   }

}/*end cell group*/
```

In this case, there are two pg pins in pg_function and it is not in MUX21 format

The following is an example message:

```
Error: Line 326, Invalid pg_function 'VDDB * VDDA' found for switch cell!
 (LBDB-1163)
```

What Next

only write one pg pin in pg_function or write the function in MUX21 format.

LBDB-1163w

(warning) Invalid pg_function '%s' found for switch cell!

Description

This message indicates that pg_function format is incorrect.

For switch cell, pg_function can only be a single pg_pin, or two pg_pins and one or more signal pins in a MUX21 format (signal pins are the select pins).

The following example shows an instance where this message occurs:

```
cell(LBDB-1163w) {
switch_cell_type : coarse_grain;
   pg_pin (VDD) {
        direction : output;
        pg_function : "VDDB * VDDA";
        pg_type : internal_power;
        switch_function : "!(A|B)";
        voltage_name : "VDD";
   }

}/*end cell group*/
```

In this case, there are two pg pins in pg_function and it is not in MUX21 format

The following is an example message:

```
Warning: Line 326, Invalid pg_function 'VDDB * VDDA' found for switch
 cell! (LBDB-1163w)
```

What Next

only write one pg pin in pg_function or write the function in MUX21 format.

Feedback

LBDB-1164

(error) Multiple %s '%s' groups are defined at line %d!

Description

You receive this message when more than one specified group are specified.

The following example shows an instance where this message occurs:

```
cell(lbdb1164) {
     site(site_def_1) {
         width: 2;
         height: 3;
         type: pad;
         symmetry (x);
         is_default: true;
     }
     site(site_def_2) {
         width: 2;
         height: 3;
         type: pad;
         symmetry (y);
         is_default: true;
     }

}
```

In this case, two site are specified and they are both default.

The following is an example message:

```
Error : Line 1000, Multiple default 'site' groups are defined at line
 1001! (LBDB-1164)
```

What Next

Remove one of the group.

LBDB-1165

(error) The size of %s [%d] should be an integral multiple of the size of %s [%d]!

Description

When the above-mentioned attributes are specified, the size should be an integral multiple of some attribute.

The following example shows an instance where this message occurs:

```
library(libdb1165) {
  ..
```

Feedback

```
site (unitTile) {
  track_pattern (M1) {
      type : uniform;
      direction: horizontal;
      mask_pattern (“mask_one”, “mask_two”, “mask_one”, “mask_two”);
      spacing : 0.2;
      offsets (“0.3”);
      widths(“0.1”);
      reserved_width_flags(“true”);
      grid_low_offsets(“0.1, 0.2, 0.3, 0.4”);
      grid_high_offsets(“0.1, 0.2, 0.3, 0.4”);
      grid_low_steps(“0.3”, “0.2, 0.4”, “0.2, 0.4”, “0.3, 0.4” );
      grid_high_steps(“0.3, 0.4”, “0.2, 0.4”, “0.2, 0.4”, “0.3, 0.4” );
  }
  ...
}
```

grid_low_steps has size 7 but mask_pattern has size 4. 7 is not integral multiple of 4.

Examples

The following is an example message:

```
Error: Line 18,  The size of grid_low_steps [7] should be an integral
 multiple of the size of mask_pattern [4]! (LBDB-1165)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-1166

(error) The size of '%s' in group '%s' should be %s!

Description

When the above-mentioned attributes are specified, the size should be required size. For track_pattern, 1) if the type is uniform, 1.a) the size of 'offsets', and 'reserved_width_flags' if specified should be 1. 1.b) the size of 'widths' can be either 1 or same as size of 'mask_pattern'. 2) if the type is non-uniform, the size of 'mask_pattern', 'widths' and 'reserved_width_flags' if specified should be same as size of 'offsets'. 3) the size of 'grid_low_offsets' and 'grid_high_offsets' if specified should be same as size of 'mask_pattern'.

The size of resize under derived_layer should be either 2 or 3 or 5. first parameter is layer name and other parameters are float numbers. following are correct resize format. 1) resize(poly, 0.005); If one float value is provided, the left, bottom, right and top are each expanded by the distance 0.005. 2) resize(poly, 0.005, 0.00); If two float values are provided, the left and right edges are each expanded by the first distance 0.005 and the top and bottom edges are each expanded by the second distance 0.00 3) resize(poly,

Feedback

0.005, 0.10, 0.002, 0.0); If four values are provided, the left, bottom, right, and top edges are expanded the respective distances.

The following example shows an instance where this message occurs:

```
library(libdb1166) {
  ..
  site (unitTile) {
    track_pattern (M1) {
        type : uniform;
        direction: horizontal;
        mask_pattern (“mask_one”, “mask_two”, “mask_one”, “mask_two”);
        spacing : 0.2;
        offsets (“0.3 0.2”);
        widths(“0.1”);
        reserved_width_flags(“true”);
        grid_low_offsets(“0.1, 0.2, 0.3, 0.4”);
        grid_high_offsets(“0.1, 0.2, 0.3, 0.4”);
        grid_low_steps(“0.3 0.1”, “0.2, 0.4”, “0.2, 0.4”, “0.3, 0.4” );
        grid_high_steps(“0.3, 0.4”, “0.2, 0.4”, “0.2, 0.4”, “0.3, 0.4” );
    }
    ...
  }
```

offsets has size 2 but its size should be 1. of 4.

Examples

The following is an example message:

```
Error: Line 18,  The size of 'offsets' in group 'track_pattern' should be
 1! (LBDB-1166)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-1167

(error) Invalid single site '%s' defined in attribute '%s'!

Description

The single site specified in attribute 'overlapping_site_mapping' should be exist in attribute 'site_list' in same 'row_pattern' group.

The following example shows an instance where this message occurs:

```
library(libdb1167) {
  ..
  row_pattern() {
     site_list ("unitH182, unitH210, unitH210");
```

Feedback

```
    overlapping_site_alignment("unitH392", "unitH192, unitH210", R0);
    overlapping_site_alignment("unitH392MX", "unitH182, unitH210", MX);
    first_row_orientation: R0;
    last_site_row_index: 0;
  };
 ...
}
```

unitH192 defined in overlapping_site_mapping doesn't exist in 'site_list' of 4.

Examples

The following is an example message:

```
Error: Line 18,  Invalid single site 'unitH192' defined in attribute
 'overlapping_site_alignment'! (LBDB-1167)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-1169

(warning) The values in '%s' are not decreasing %g, %g,\n \twhen %s = %g, %s = %g, %g.

Description

This information appears when the values in the specified table do not decrease monotonically with the increasing output voltage from voltage value of VSS through VDD.

The following example shows an instance where this message occurs:

```
dc_current(template) {
    index_1("-0.675, -0.3375, -0.135, -0.0675, 0, 0.03375, 0.0675,
 0.10125, 0.135, 0.16875, 0.2025, 0.23625, 0.27, 0.30375, 0.3375,
 0.37125, 0.405, 0.43875, 0.4725, 0.50625, 0.54, 0.57375, 0.6075,
 0.64125, 0.675, 0.7425, 0.81, 1.0125, 1.35"); /* input_voltage */
    index_2("-0.675, -0.3375, -0.135, -0.0675, 0, 0.03375, 0.0675,
 0.10125, 0.135, 0.16875, 0.2025, 0.23625, 0.27, 0.30375, 0.3375,
 0.37125, 0.405, 0.43875, 0.4725, 0.50625, 0.54, 0.57375, 0.6075,
 0.64125, 0.675, 0.7425, 0.81, 1.0125, 1.35"); /* output_voltage */
    values("...0.0166949, 0.016715,...")
  }
```

The following is an example message:

```
Warning: Line 762, Cell 'A', pin 'clk', The values in 'dc_current' are
 not decreasing 0.0166949, 0.016715,
        when input_voltage = 0.0675, output_voltage = 0.16875, 0.2025.
 (LBDB-1169)
```

Feedback

What Next

Make sure that the values decrease monotonically with the increasing output voltage from voltage value of VSS through VDD.

LBDB-1170

(error) The '%s' attribute is not specified.

Description

This message indicates that an attribute is missing. start_site_id should be specified for all cells in a cell group. For the cells in a cell group, you can either specify start_site_id for them all, or not specify it at all.

The following example shows an instance where this message occurs:

```
library ( prf ) {
    ...
    cell (A) {
      cell_group: A;
      start_site_id (1, 2);
    }
    cell (A1) {
      cell_group: A;
    }
  }
```

The following is an example message:

```
Error: Line 52, Cell 'A1', The 'start_site_id' attribute is not
 specified. (LBDB-1170)
```

What Next

Add the missing attribute.

LBDB-1171

(error) The '%s' attribute is specified without '%s' attribute specified.

Description

This message indicates that an attribute is specified without another attribute specified in a cell group.

The following example shows an instance where this message occurs:

```
library ( prf ) {
    ...
    cell (A) {
```

```
      delta_tap_distance (-0.18,0.27,0.09,0.09,0.09,0.09,-0.18,0.27);
    }
  }
```

The following is an example message:

```
Error: Line 52, Cell 'A', The 'delta_tap_distance' attribute is specified
 without 'tap_boundary_wall_cell_properties' attribute specified.
 (LBDB-1171)
```

What Next

Add the missing attribute.

LBDB-1172

(error) The '%s' attribute is specified without '%s' attribute specified in the referred '%s (%s)' group at line %u.

Description

This message indicates that an attribute is specified without another attribute specified. One case is that both 'delta_tap_distance' and 'tap_boundary_wall_cell_properties : <prop_name>' attributes are specified in a cell group, however in the referred 'tap_boundary_wall_cell_properties(<prop_name>)' group in the library, the 'tap_distance' attribute is not specified.

The following example shows an instance where this message occurs:

```
library ( prf ) {
    tap_boundary_wall_cell_properties( AAA ) {
    /* tap_distance (TTT, TTT, 0, 0, 0, 0, TTT, TTT); */
    }
    ...
    cell (A) {
      tap_boundary_wall_cell_properties: AAA;
      delta_tap_distance (-0.18,0.27,0.09,0.09,0.09,0.09,-0.18,0.27);
    }
  }
```

The following is an example message:

```
Error: Line 68, Cell 'A', The 'delta_tap_distance' attribute is
 specified without 'tap_distance' attribute specified in the referred
 'tap_boundary_wall_cell_properties ( AAA )' group at line 23.
 (LBDB-1172)
```

What Next

Add the missing attribute.

Feedback

LBDB-1173

(error) Number of elements in %s (%u) is not same as that in %s (%u) at line %u.

Description

This message indicates that the size of 'delta_tap_distance' is not same as the size of 'tap_distance' in the referred 'tap_boundary_wall_cell_properties()' group.

The following example shows an instance where this message occurs:

```
library ( prf ) {
    tap_boundary_wall_cell_properties( AAA ) {
      tap_distance (TTT, TTT, 0, 0, 0, 0, TTT, TTT);
    }
    ...
    cell (A) {
      tap_boundary_wall_cell_properties: AAA;
      delta_tap_distance (-0.18,0.27,0.09,0.09);
    }
  }
```

The following is an example message:

```
Error: Line 52, Cell 'A', Number of elements in delta_tap_distance (4) is
 not same as that in tap_distance (8) at line 24. (LBDB-1173)
```

What Next

Add the missing attribute.

LBDB-1174

(error) Number of elements in %s (%u) is neither 8 nor 4.

Description

This message indicates that the size of 'tap_distance' is neither 8 nor 4.

The following example shows an instance where this message occurs:

```
library ( prf ) {
    tap_boundary_wall_cell_properties( AAA ) {
      tap_distance (0, 0);
    }
    ...
  }
```

The following is an example message:

```
Error: Line 52, Number of elements in tap_distance (2) is neither 8 nor
 4. (LBDB-1174)
```

Feedback

What Next

Provide the correct number of elements for the attribute.

LBDB-1175

(warning) The vector has duplicate indices for input_net_transition and total_output_net_capacitance pair with other vector.

Description

This error message occurs because under the output_voltage_rise|fall, some vector's total_output_net_capacitance and input_net_transition are duplicate with other vector.

The following example shows an output_current_rise group without a dense vector and resulting error message.

```
output_voltage_template(ccsnov) {
  variable_1 : input_net_transition;
  variable_2 : total_output_net_capacitance;
  variable_3 : time;
 }
 . . .
 output_voltage_rise() {
   vector(ccsnov) {
      index_1 ("0.1");
      index_2 ("1");
      index_3 ("1, 2, 3");
      values ("1, 2, 3");
   }
    vector(ccsnov) {
      reference_time : 0.11;
      index_1 ("0.1");
      index_2 ("1");
      index_3 ("3, 4, 6");
      values ("1, 2, 3");
   }
 }

Error: Line 198, The vector has duplicate indices for
 input_net_transition and total_output_net_capacitance with other vector.
 (LBDB-1175)
```

What Next

Check the library source file and correct the vector for input_net_transition and total_output_net_capacitance pair.

Feedback

LBDB-1176

(error) The '%s' in '%s' is invalid.

Description

This message indicates that one of the value in 'tap_distance' is invalid. Each value in 'tap_distance' can be a name of pre-defined 'tap_rule' group, or direct number.

The following example shows an instance where this message occurs:

```
library ( prf ) {
    tap_rule( TTT ) {
      default_tap_distance : 15;
      tap_distance_layer_rule (LUP_075U, 10);
      tap_distance_layer_rule (LUP_045U, 3);
    }
    tap_boundary_wall_cell_properties( AAA ) {
      tap_distance (TTT, TTT, 0, 0, 0, 0, TTT, XXX);
    }
    ...
  }
```

The following is an example message:

```
Error: Line 23, The 'XXX' in 'tap_distance' is invalid. (LBDB-1176)
```

What Next

Provide a name of pre-defined 'tap_rule' group or direct number for each value in 'tap_distance'.

LBDB-1177

(error) The '%s' in '%s' refers to a '%s' group which is defined at line %u after this line.

Description

This message indicates that one of the value in 'tap_distance' refers to a 'tap_rule' group after this line.

The following example shows an instance where this message occurs:

```
library ( prf ) {
    tap_boundary_wall_cell_properties( AAA ) {
      tap_distance (TTT, TTT, 0, 0, 0, 0, TTT, TTT);
    }
    tap_rule( TTT ) {
      default_tap_distance : 15;
      tap_distance_layer_rule (LUP_075U, 10);
      tap_distance_layer_rule (LUP_045U, 3);
```

Feedback

```
    }
    ...
  }
```

The following is an example message:

```
Error: Line 23, The 'TTT' in 'tap_distance' refers to a 'tap_rule' group
 which is defined at line 25 after this line. (LBDB-1177)
```

What Next

Define tap_rule group before using it.

LBDB-1178

(warning) The '%s' under '%s' group must have at least one '%s' which is defined in '%s' group.

Description

This message indicates that 'default_pg_setting' should be specified in one pg_setting under mode_value group for each mode_definition group.

The following example shows an instance where this message occurs:

```
cell(test) {
   pg_setting_definition(PD) {
      default_pg_setting : PV1;
      pg_setting_value(PV1) {
        ...
      }
      pg_setting_value(PV2) {
        ...
      }

   }
   mode_definition(rw) {
      mode_value(read) {
         pg_setting(PD, PV2);
      }
   }
}
```

The following is an example message:

```
Warning: Line 35, The 'pg_setting' under 'mode_value' group must have at
least one 'default_pg_setting' which is defined in
'pg_setting_definition' group. (LBDB-1178)
```

What Next

Add the group if it is missing, or fix the attribute value if it has a typo.

Feedback

LBDB-1179

(error) The '%s' attribute for %s '%s' is specified without '%s' attribute for the same %s.

Description

This message indicates that an attribute is specified without another attribute specified. One case is that there is no corresponding "extra_site_list" for the same name site-array when relative_shift" for the named site-array is specified

The following example shows an instance where this message occurs:

```
library ( prf ) {
    row_pattern (demo) {
       site_list (core);
       extra_site_list (“halo”, R0);
       relative_shift (“halo1”, “-0.025, 0”);
       ……
    }
  }
```

The following is an example message:

```
Error: Line 68,The 'relative_shift' attribute for site-array 'halo1' is
 specified without 'extra_site_list' attribute for the same site-array.
```

What Next

Add the missing attribute.

LBDB-1180

(error) An invalid zero or negative value (%f) of '%s' is found.

Description

This message indicates zero or negative value is found for the attribute.

library (my_library) { lifetime_profile_definition (lifetime_profile_1) { stress_time : 10; stress_voltage : 1.1; stress_temperature : 125; signal_probability : 0.5; activity_factor : 0.5; stress_mode: HCI; /*stress_clock_period cannot be 0 and should be larger than 0*/ stress_clock_period: 0; stress_slew_index: 2; stress_load_index: 0; }

}

The following is an example message:

```
Error: Line 136, An invalid zero or negative value (0.000000) of
 'stress_clock_period' is found. (LBDB-1180)
```

Feedback

What Next

Change the value of the attributes to positive, make sure value >= 1e-6.

LBDB-1181

(warning) There is no %s specified on %s pin, may affect STA accuracy.

Description

This warning message occurs when a internal pin has no related_power_pin/ related_ground_pin attribute.

The following example shows an instance where this message occurs:

```
cell(test_LBDB-1181){
  area : 1.0;

pg_pin(VDDB) {
  voltage_name : VDDB;
  pg_type : backup_power;
}

pg_pin(VDD) {
  voltage_name : VDD;
  pg_type : primary_power;
}

pg_pin(VSS) {
  voltage_name : VSS;
  pg_type : primary_ground;
}


pin(A) {
  direction : internal;
}
}
```

The following is an example message:

```
Warning: Line 192, Cell 'test_LBDB-1181', pin 'A', There is no
 related_power_pin specified on internal pin, may affect STA accuracy.
 (LBDB-1181)
Warning: Line 193, Cell 'test_LBDB-1181', pin 'A', There is no
 related_ground_pin specified on internal pin, may affect STA accuracy.
 (LBDB-1181)
```

What Next

Check the library source file to add or correct related_power_pin/related_ground_pin attributes.

Feedback

LBDB-1210

(error) Incomplete when condition coverage ("%s") for the '%s' group%s.

Description

This message occurs when internal_power, leakage_power or timing group has incomplete "when" condition coverage

The following example shows an instance where this message occurs:

```
...
    pin(Z) {
      direction : output ;
      timing() {
        related_pin : "I" ;
        when : "A*B";
        ...
      }
      timing() {
        related_pin : "I" ;
        when : "A*!B";
        ...
      }
      timing() {
        related_pin : "I" ;
        when : "!A*B";
        ...
      }
      /*
      timing() {
        related_pin : "I" ;
        when : "!A*!B";
        ...
      }
      */
      ...
    }
    ...

In the example above, the arc from 'I' to 'Z' does not have a timing
 model
for the when condition "!A*!B".

The following is an example of the message:

Error: Line 206, cell 'test', pin 'Z', Incomplete when condition
 coverage("A + B") for the 'timing' group of related_pin 'I'. (LBDB-1210)
```

Feedback

What Next

Complete the model. Either introduce a new group with the missing "when" condition, or add a default “when” condition.

LBDB-1211

(error) The value for 'parameter_value_delta' index size must be one.

Description

Currently only support one dimension for 'parameter_value_delta'.

The following example shows an instance where this message occurs:

```
lu_table_template (lle_delta_template_3x3x1) {
    variable_1 : input_net_transition;
    variable_2 : total_output_net_capacitance;
    variable_3 : parameter_value_delta;
    index_1 ("0, 0.0625, 1");
    index_2 ("0, 0.0625, 1");
    index_3 ("0,1");
  }
  ...
  lle_delta_cell_rise (lle_delta_template_3x3x2) {
    related_params : “vth”;
    related_devices : “tr2”;
    index_1 ("0.0018, 0.0743, 1.15149");
    index_2 ("9.35e-05, 0.0025, 0.039");
    index_3 ("0.050,0.06");
    values ("0.000100", "0.000200", "0.000300", \
            "0.001000", "0.002000", "0.003000", \
            "0.010000", "0.020000", "0.030000");
  }
```

The following is an example message:

```
Error: Line 144, The value for 'parameter_value_delta' index size must be
 one. (LBDB-1211)
```

What Next

Check the library source file to see if you defined the 'parameter_value_delta' not one dimension for the specified group.

LBDB-1212

(warning) The timing arc from '%s' to '%s' is missing possible condition: "%s".

Feedback

Description

This message indicate some possible conditions are missing for this timing arc, and there is no default arc.

The following example shows an instance where this message occurs:

```
pin(Z) {
    direction : output;
    function : "(S' * A+S * B)";
    timing () {
      related_pin : "A";
      when :     "B * !S";
      sdf_cond : "B * !S";
      cell_rise(scalar)       { values ( "0.1");}
      rise_transition(scalar) { values ( "0.1");}
      cell_fall(scalar)       { values ( "0.1");}
      fall_transition(scalar) { values ( "0.1");}
    }
```

In this case, the condition "B' S'" is missing for this timing arc from 'A' to 'Z'. To fix the problem, add the following timing group:

```
timing () {
      related_pin : "A";
      when :     "!B * !S";
      sdf_cond : "!B * !S";
      cell_rise(scalar)       { values ( "0.1");}
      rise_transition(scalar) { values ( "0.1");}
      cell_fall(scalar)       { values ( "0.1");}
      fall_transition(scalar) { values ( "0.1");}
    }

The following is an example message:
Warning: Line 190, Cell 'MUX21', pin 'Z', The timing arc from 'A' to 'Z'
 is missing possible condition: "B' S'". (LBDB-1212)
```

What Next

Add the timing arcs with missing conditions between the two pins.

LBDB-1213

(error) The value '%s' for 'related_devices' of lle delay must be listed in 'lle_devices' definition.

Description

The following example shows an instance where this message occurs:

```
cell ( cell_a ) {
      lle_devices: "tr2 tr1";
```

Feedback

```
      lle_params: "vth vth1";
  ...
  }
  lle_delta_cell_rise (lle_delta_template_3x3x2) {
    related_params : “vth”;
    related_devices : “tr3”;
    index_1 ("0.0018, 0.0743, 1.15149");
    index_2 ("9.35e-05, 0.0025, 0.039");
    index_3 ("0.050,0.06");
    values ("0.000100", "0.000200", "0.000300", \
            "0.001000", "0.002000", "0.003000", \
            "0.010000", "0.020000", "0.030000");
  }
```

The following is an example message:

```
Error: Line 144, The value 'tr3' for 'related_devices' of lle delay must
 be listed in 'lle_devices' defined. (LBDB-1213)
```

What Next

Check the value for 'related_devices' to see if your definition is in 'lle_devices' allowable values.

LBDB-1214

(error) The value '%s' for 'related_params' of lle delay must be listed in 'lle_params' definition.

Description

The following example shows an instance where this message occurs:

```
cell ( cell_a ) {
      lle_devices: "tr2 tr1";
      lle_params: "vth vth1";
  ...
  }
  lle_delta_cell_rise (lle_delta_template_3x3x2) {
    related_params : "vth0";
    related_devices : "tr2";
    index_1 ("0.0018, 0.0743, 1.15149");
    index_2 ("9.35e-05, 0.0025, 0.039");
    index_3 ("0.050,0.06");
    values ("0.000100", "0.000200", "0.000300", \
            "0.001000", "0.002000", "0.003000", \
            "0.010000", "0.020000", "0.030000");
  }
```

Feedback

The following is an example message:

```
Error: Line 144, The value 'vth0' for 'related_params' of lle delay must
 be listed in 'lle_params' defined. (LBDB-1214)
```

What Next

Check the value for 'related_params' to see if your definition is in 'lle_params' allowable values.

LBDB-1215

(error) The '%s' group is missing the table definition for %s %s,%s %s.

Description

The following example shows an instance where this message occurs:

```
cell ( cell_a ) {
      lle_devices: "tr2 tr1";
      lle_params: "vth";
  ...
  }
  lle_delta_cell_rise (lle_delta_template_3x3x2) {
    related_params : "vth";
    related_devices : "tr1";
    index_1 ("0.0018, 0.0743, 1.15149");
    index_2 ("9.35e-05, 0.0025, 0.039");
    index_3 ("0.050,0.06");
    values ("0.000100", "0.000200", "0.000300", \
            "0.001000", "0.002000", "0.003000", \
            "0.010000", "0.020000", "0.030000");
  }
```

The following is an example message:

```
Error: Line 27, Cell 'cell_a', pin 'z', The 'lle_delta_cell_rise' group
 is missing the table definition for related_devices tr2,related_params
 vth. (LBDB-1215)
```

What Next

Check lle_delta group to see if you are missing the table definition for all lle_devices and lle_params specified in cell.

LBDB-1216

(warning) is missing internal_power with when condition: "%s" from '%s' to '%s'.

Feedback

Description

This message indicate some possible conditions are missing for this timing arc, and there is no default arc.

The following example shows an instance where this message occurs:

```
pin(Z) {
    direction : output;
    function : "(S' * A+S * B)";
    internal_power () {
      related_pin : "A";
      when :     "B * !S";
    }
```

In this case, the internal_power condition "B' S'" is missing for this arc from 'A' to 'Z'. To fix the problem, add the following internal_power group:

```
internal_power () {
      related_pin : "A";
      when :     "!B * !S";
    }

The following is an example message:
Warning: Line 190, Cell 'MUX21', pin 'Z', is missing internal_power with
 when condition: "B' S'" from 'A' to 'Z'. (LBDB-1216)
```

What Next

Add the internal_power group with missing conditions between the two pins.

LBDB-1217

(warning) is missing internal_power with when condition: "%s".

Description

This message indicate some possible conditions are missing for this input, and there is no default arc.

The following example shows an instance where this message occurs:

```
pin(Z) {
    direction : output;
    function : "a&b&c";
    ...
    }
    pin(a){
    direction : input;
    internal_power(){
      when :   "!b&c";
    }
```

Feedback

```
    internal_power(){
      when :   "!b&!c";
    }
   }
```

In this case, the internal_power condition "b&!c" is missing for this input pin 'a'. To fix the problem, add the following internal_power group:

```
internal_power () {
      when :     "b&!c";
    }

The following is an example message:
Warning: Line 190, Cell 'MUX21', pin 'a', is missing internal_power with
 when condition: "b&!c".(LBDB-1217)
```

What Next

Add the internal_power group with missing conditions for input pin's dynamic power.

LBDB-1218

(warning) The internal_power group with when condition "%s" from '%s' to '%s' is invalid.

Description

A arc from an input pin to an output pin for internal_power is dormant if the signal change on the input pin can never cause the change on the output without simultaneous changes on any other input pins.

The following example shows an instance where this message occurs:

```
cell(a_cell) {
    pin(Z) {
    direction : output;
    function : "A * B";
    internal_power () {
       related_pin : "A";
       when :     "!B";
       rise_power(scalar)       { values ( "0.1");}
       fall_power(scalar) { values ( "0.1");}
    }
   }
  }
```

In this example, if only pin 'A' is changed, pin 'Z' will not have the signal transitions between '0' and '1'. The combinational arc between 'A' and 'Z' is invalid.

The following is an example message:

```
Warning: Line 50000, The internal_power group with when condition "!B"
 from 'A' to 'Z' is invalid. (LBDB-1218)
```

Feedback

What Next

This is caused by the input sharing between 'function', 'three_state', and 'x_function'. The signal transition is not physically possible and generally the arc should not be specified.

LBDB-1219

(warning) The internal_power group with when condition "%s" is invalid.

Description

A arc from an input pin for internal_power(dynamic power) is dormant if the signal change on the input pin can never cause the change on the output without simultaneous changes on any other input pins.

The following example shows an instance where this message occurs:

```
cell(a_cell) {
    pin(Z) {
    direction : output;
    function : "a&b&c";
    ...
    }
    pin(a){
    direction : input;
    internal_power(){
      when :   "b&c";
    }
  }
```

In this example, if input pin 'a' is changed, pin 'Z' will not have the signal transitions between '0' and '1'. So the input pin 'a' for internal_power(dynamic_power) is dormant.

The following is an example message:

```
Warning: Line 50000, The internal_power group with when condition "b&c"
 is invalid. (LBDB-1219)
```

What Next

This is caused by the input sharing between 'function', 'three_state', and 'x_function'. The signal transition is not physically possible and generally the arc should not be specified.

LBDB-1220

(warning) is missing leakage power possible condition: "%s".

Feedback

Description

This message indicate some possible conditions are missing for this cell, and there is no default arc.

The following example shows an instance where this message occurs:

```
cell(std) {
    leakage_power () {
      when :     "B";
    }
```

In this case, the leakage power condition "B'" is missing for this cell 'std'. To fix the problem, add the following leakage_power group:

```
leakage_power () {
      when :     "!B ";
    }

The following is an example message:
Warning: Line 190, Cell 'std', is missing leakage power possible
 condition: "B'". (LBDB-1220)
```

What Next

Add the leakage_power group with missing conditions for the cell.

LBDB-1221

(error) non input signal pin is not allowed to be specified in bump cell.

Description

This message indicate bump cell have not only input signal pins.

The following example shows an instance where this message occurs:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : output ;
      bump_type: front_side;
    }
  }
```

In this case, the pin "pad" direction is not input signal pin. To fix the problem, change direction to input:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : input ;
```

```
      bump_type: front_side;
    }
  }
```

```
The following is an example message:
Error: Line 190, Cell 'simple_front_side_bump', pin 'PAD', non input
 signal pin is not allowed to be specified in bump cell. (LBDB-1221)
```

What Next

Change pin to input signal pin for the bump cell.

LBDB-1222

(error) is missing bump_type on signal pin of bump cell.

Description

This message indicate signal pins in bump cell has not bump_type attribute.

The following example shows an instance where this message occurs:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : input ;
    }
  }
```

In this case, the pin "pad" has no bump_type attribute. To fix the problem, add the following bump_type attribute:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : input ;
      bump_type: front_side;
    }
  }
```

```
The following is an example message:
Error: Line 190, Cell 'simple_front_side_bump', pin 'PAD', is missing
 bump_type on signal pin of bump cell. (LBDB-1222)
```

What Next

Add bump_type attribute for the bump cell signal pin.

LBDB-1223

(error) the "is_pad" attribute is not allowed to be specified in signal pin of bump cell.

Feedback

Description

This message indicate bump cell contains is_pad pin attributes.

The following example shows an instance where this message occurs:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : input ;
      bump_type: front_side;
      is_pad   : true;
    }
  }
```

In this case, contains is_pad attributes. To fix the problem, remove the following is_pad attribute:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : input ;
      bump_type: front_side;
    }
  }

The following is an example message:
Error: Line 190, Cell 'simple_front_side_bump', pin 'PAD', the "is_pad"
 attribute is not allowed to be specified in signal pin of bump cell.
 (LBDB-1223)
```

What Next

Remove pin's is_pad attribute for the bump cell.

LBDB-1224

(error) pg_pin is not allowed to be specified in bump cell.

Description

This message indicate bump cell contains pg_pin.

The following example shows an instance where this message occurs:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : input ;
      bump_type: front_side;
    }
    pg_pin(VDD){
```

```
    ..
    }
  }
```

In this case, contains pg_pin. To fix the problem, remove the following pg_pin attribute:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : input ;
      bump_type: front_side;
    }
  }

The following is an example message:
Error: Line 190, Cell 'simple_front_side_bump', pg_pin is not allowed to
 be specified in bump cell. (LBDB-1224)
```

What Next

Remove pg_pin for the bump cell.

LBDB-1225

(error) the "%s" attribute is not allowed to be specified in bump cell.

Description

This message indicate bump cell contains pad_cell or auxiliary_pad_cell attributes.

The following example shows an instance where this message occurs:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    auxiliary_pad_cell : true;
    pin (PAD) {
      direction : input ;
      bump_type: front_side;
    }
  }
```

In this case, the pin "pad" contains auxiliary_pad_cell. To fix the problem, remove the following auxiliary_pad_cell attribute:

```
cell (simple_front_side_bump) {
    bump_cell: true;
    pin (PAD) {
      direction : input ;
      bump_type: front_side;
    }
  }
```

Feedback

```
The following is an example message:
Error: Line 190, Cell 'simple_front_side_bump', the "auxiliary_pad_cell"
 attribute is not allowed to be specified in bump cell. (LBDB-1225)
```

What Next

Remove auxiliary_pad_cell/pad_cell for the bump cell.

LBDB-1230

(error) The value '%s' for 'related_devices' of lle leakage power must be listed in 'lle_devices' definition.

Description

The following example shows an instance where this message occurs:

```
cell ( cell_a ) {
      lle_devices: "tr1 tr2";
      lle_params: "vth vth1";
   ...
   leakage_power() {
        when : "(!A) | (A)" ;
        value : 0.00644538 ;
  lle_delta_leakage_power( lle_template_sample ) {
   related_params : "vth" ;
   related_devices : "tr3" ;
   index_1("-0.1,0.1") ;
   values("4.20784,4.20785");
  }
     }
   }
```

The following is an example message:

```
Error: Line 144, The value 'tr3' for 'related_devices' of lle leakage
 power must be listed in 'lle_devices' defined. (LBDB-1230)
```

What Next

Check the value for 'related_devices' to see if your definition is in 'lle_devices' allowable values.

LBDB-1231

(error) The value '%s' for 'related_params' of lle leakage power must be listed in 'lle_params' definition.

Feedback

Description

The following example shows an instance where this message occurs:

```
cell ( cell_a ) {
      lle_devices: "tr1 tr2";
      lle_params: "vth vth1";
   ...
   leakage_power() {
        when : "(!A) | (A)" ;
        value : 0.00644538 ;
  lle_delta_leakage_power( lle_template_sample ) {
   related_params : "vth2" ;
   related_devices : "tr2" ;
   index_1("-0.1,0.1") ;
   values("4.20784,4.20785");
   }
     }
   }
```

The following is an example message:

```
Error: Line 144, The value 'vth2' for 'related_params' of lle leakage
 power must be listed in 'lle_params' defined. (LBDB-1231)
```

What Next

Check the value for 'related_params' to see if your definition is in 'lle_params' allowable values.

LBDB-1232

(error) The '%s' group is missing the table definition for %s %s,%s %s.

Description

The following example shows an instance where this message occurs:

```
cell ( cell_a ) {
      lle_devices: "tr2 tr1";
      lle_params: "vth";
   ...
   leakage_power() {
        when : "(!A) | (A)" ;
        value : 0.00644538 ;
  lle_delta_leakage_power( lle_template_sample ) {
   related_params : "vth" ;
   related_devices : "tr2" ;
   index_1("-0.1,0.1") ;
   values("4.20784,4.20785");
   }
```

```
      }
    }
```

The following is an example message:

```
Error: Line 27, Cell 'cell_a', leakage_power, The
 'lle_delta_leakage_power' group is missing the table definition for
 related_devices tr1,related_params vth. (LBDB-1232)
```

What Next

Check lle_delta group to see if you are missing the table definition for all lle_devices and lle_params specified in cell.

LBDB-1233

(warning) The same timing arc with different sdf_cond has already been specified%s.

Description

This message indicates the same timing arc with different sdf_cond is specified multiple times.

What Next

Check the library source file if there is a duplicate, gave the warning

EXMAPLES

The following example shows two timing arc definition are same with different sdf_cond.

```
pin(Q) {
            timing(){
               timing_type: rising_edge;
               related_pin: "B";
               sdf_cond : "sdf1";
               when: "A";
             }

            timing(){
               timing_type: rising_edge;
               related_pin: "B";
               sdf_cond : "sdf2";
               when: "A";
             }
        }
```

Examples

```
Warning: Line 456, Cell 'sass', pin 'CLKA', The same timing arc with
 different sdf_cond has already been specified at line 123.(LBDB-1233)
```

Feedback

LBDB-1234

(error) Invalid attribute '%s' value '%s' is detected. The value %s.

Description

This message indicates that you specified an invalid value.

```
lib ( liberty_lde )    {
      lde_boundary_type_names ("w1", "w2");
   ... ...
      cell ( cell_a ) {
     lde_boundary_count : 0 ;
     lde_boundary_types ( "w1" ) ;
        pin(A) {
    timing () {
   lde_delta ( ) {
   ...
   }
    }
  }
      }
      ... ...
  }
```

The following is an example message:

```
Error: Line 12, Invalid attribute 'lde_boundary_count' value '0' is
 detected. The value must be positive integer. (LBDB-1234)
```

What Next

Check the library source file, and correct the attribute value in the library.

LBDB-1235

(error) Invalid attribute '%s' is detected. The size must be same with lde_boundary_count : %d.

Description

This message indicates that you specified an invalid attribute size.

```
lib ( liberty_lde )    {
   lde_boundary_type_names ("w1", "w2");
      cell ( cell_a ) {
     lde_boundary_count : 2 ;
     lde_boundary_types ( "w1" ) ;
        pin(A) {
    timing () {
   lde_delta ( ) {
```

Feedback

```
   ...
   }
    }
  }
      }
      ... ...
    }
```

The following is an example message:

```
Error: Line 22, Cell 'cell_a', Invalid attribute 'lde_boundary_types' is
 detected. The size must be same with lde_boundary_count : 2. (LBDB-1235)
```

What Next

Check the library source file, and correct the attribute size in the library.

LBDB-1236

(error) The '%s' group is missing the table definition for lde_boundary_id:%d, lde_boundary_type:%s.

Description

The following example shows an instance where this message occurs:

```
lib ( liberty_lde )    {
   lde_boundary_type_names ("w1", "w2");
      cell ( cell_a ) {
     lde_boundary_count : 1 ;
     lde_boundary_types ( "w1" ) ;
        pin(z) {
    timing () {
   lde_delta ( ) {
    lde_boundary_id : 1 ;
    lde_boundary_type : "w2" ;
   ...
   }
    }
  }
      }
      ... ...
    }
```

The following is an example message:

```
Error: Line 29, Cell 'cell_a', pin 'z', The 'lde_delta' group is missing
 the table definition for lle_boundary_id:1, lle_boundary_type:w1.
 (LBDB-1236)
```

Feedback

What Next

Check lde_delta group to see if you are missing the table definition for all lde_boundary_count and lde_boundary_type_names specified in cell.

LBDB-1237

(error) The '%s' that required by liberty lde delta model is missing in %s '%s'.

Description

Defined lde_delta groups in .lib, but the dependent attribute is missing in the library or cell.

The following example shows an instance where this message occurs:

```
lib ( liberty_lde )    {
   /*lde_boundary_type_names miss*/
      cell ( cell_a ) {
     lde_boundary_count : 1 ;
     lde_boundary_types ( "w1" ) ;
        pin(A) {
    timing () {
   lde_delta ( ) {
     lde_boundary_id : 1 ;
     lde_boundary_type : "w1" ;
   ...
   }
    }
  }
      }
      ... ...
    }
```

The following is an example message:

```
Error: Line 3, The 'lde_boundary_type_names' that required by liberty lde
 delta model is missing in library 'liberty_lde'. (LBDB-1237)
```

What Next

Check the library source file to see if you missed the required content for the specified group.

LBDB-1237w

(warning) The '%s' is defined in %s '%s', but no lde_delta use it.

Feedback

Description

Defined lde_boundary_type_names attribute in liberty_lde library, but there is no lde_delta group in all timing arcs.

The following example shows an instance where this message occurs:

```
lib ( liberty_lde )    {
   lde_boundary_type_names ( "w1",  "w2" )
      cell ( cell_a ) {
     lde_boundary_count : 1 ;
     lde_boundary_types ( "w1" ) ;
        pin(A) {
    timing () {
   /* No lde_delta in timing arc*/
   ...
   }
    }
  }
      }
      ... ...
    }
```

The following is an example message:

```
Warning: Line 3, The 'lde_boundary_type_names' is defined in library
 'libertyLdeMulti', but no lde delta use it. (LBDB-1237w)
```

What Next

Check the library source file to see if you need the content that not used for the specified group.

LBDB-1238

(error) The number of '%s' in group '%s' should be %s.

Description

When the above-mentioned attributes are specified, the number of the elements should be required size. For track_pattern, the number of <list_of_offsets> in row_grid_low_steps and row_grid_high_steps should be same as the size of grid_low_offsets.

The following example shows an instance where this message occurs:

```
library(libdb1166) {
  ..
  row_pattern (unit10_unit12) {
    track_pattern (M1) {
        type : uniform;
        direction: horizontal;
        mask_pattern (“mask_one”, “mask_two”, “mask_one”, “mask_two”);
```

Feedback

```
        spacing : 0.2;
        offsets (“0.3 0.2”);
        widths(“0.1”);
        reserved_width_flags(“true”);
        grid_low_offsets(“0.1, 0.2, 0.3, 0.4”);
        grid_high_offsets(“0.1, 0.2, 0.3, 0.4”);
        row_grid_low_steps("unit10", “0.3 0.1”, “0.2, 0.4”, “0.2, 0.4”);
        row_grid_high_steps("unit12", “0.3, 0.4”, “0.2, 0.4”, “0.2, 0.4”,
 “0.3, 0.4” );
    }
    ...
  }
```

row_grid_low_steps has number of <list_of_offsets> as 3 but its size should be 4. of 4.

Examples

The following is an example message:

```
Error: Line 18,  The number of '<list_of_offsets> in row_grid_low_steps'
 in group 'track_pattern' should be 4. (LBDB-1238)
```

What Next

Check the library source file, and make the necessary correction.

LBDB-1239

(warning) The '%s' is not supported for this %s group.

Description

This warning indicates that the specified attribute(e.g. receiver_capacitance_rise_delta, receiver_capacitance_fall_delta, leakage_derate) or group(e.g. receiver_capacitance_rise, receiver_capacitance_fall) is not supported by down-steam tools like FC/PT and will be ignored for now.

The following example shows an instance where this message occurs:

```
leakage_power() {
      value : "0.0369201" ;
      related_pg_pin : "VDD" ;

      sensitivity() {
        device_param : "delta_xyz_n1" ;
        perturbation_value : "-0.02" ;
        leakage_derate : "-4.87648e-03" ;
      }
    }
    ...
```

Feedback

The following is an example message:

```
Warning: Line 327, The 'leakage_derate' is not supported for this
 sensitivity group. (LBDB-1239)
```

What Next

Check the library source file to see if you need the content that not supported for now.

LBDB-1240

(error) The switch pin is not found in switch_function of any pin in the cell.

Description

This error indicates that the specified switch pin is not in switch_function of any pin in the current cell.

The following is an example message:

```
Error: Line 326, Cell 'FD1', pin 'sp2', The switch pin is not found in
 switch_function of any pin in the cell. (LBDB-1240)
```

What Next

Check the library source file to see if you need to add the pin to switch_function of a pin or set flag of switch_pin as false or remove switch_pin attribute from the pin.

LDB

LDB-1

(error) Cannot delete views from the non-view-based library .db '%s'.

Description

This error message occurs because views can only be deleted in a view-based library .db file.

What Next

Convert the original .db file into a view-based .db file, and read in the file again.

LDB-2

(error) Cannot delete view '%s'.

Feedback

Description

This error message occurs when the specified view cannot be deleted because it's not a valid view name.

What Next

Check the view name and correct as needed.

LDB-3

(error) Failed to load the skeleton view to get all cell names.

Description

This error message occurs because when reading a view for unspecified cells, the tool reads the skeleton view node to get all cell names. If the skeleton view node cannot be read, this step fails and nothing is loaded.

What Next

Make sure the skeleton view node can be read successfully by ldbatt.

LDB-4

(error) Failed to load view node '%s'.

Description

This error message occurs when there is incorrect data in the input view-based .db file.

The pattern of the view node name is as follows:

```
<path_name>/<view_based_db_file_name>/<lib_name>/<view_name>
```

What Next

Make sure the content in the specified view node is correct (by ldbatt).

LDB-5

(warning) Cannot read cell '%s'.

Description

This error message occurs when the cell name doesn't exist in the library.

What Next

Correct cell name.

Feedback

LEFR

LEFR-001

(error) Cannot find lef file '%s'.

Description

The lef file specified to the set_eco_options command cannot be read.

What Next

Check the existence of the lef file to the set_eco_options in the search_path using the *which* command.

LEFR-002

(error) read lef '%s' failed.

Description

read lef file failed.

What Next

Check the logfile file provided to the set_eco_options for lef file syntax and content related errors.

LEFR-018

(warning) Site '%s' already exists having width %d and height %d, which conflicts with the LEF site width %d and height %d.

Description

The indicated site already exists in the library, and its dimensions do not match the LEF site definition. The LEF site definition cannot overwrite the existing site in the library. The existing library site is not modified.

What Next

Check whether you have read the correct LEF file. Check whether the LEF or existing library site definition is correct.

Feedback

LEFR-021

(error) Layer '%s' does not exist in the library technology information provided at lineNumber %d.

Description

The indicated layer was not defined in the technology file which was provided to the set_eco_options.

What Next

Manually add the missing layer into the technology file, and read in the physical information again.

LEFR-050

(warning) Invalid SITE row '%s' detected with width %d, height %d at lineNumber %d.

Description

The indicated SITE row definition has invalid width or height. This SITE row will be skipped.

What Next

Check the SITE row definition in the LEF file provided to the set_eco_options for correctness.

LEFR-051

(error) Invalid MANUFACTURINGGRID value '%f' at lineNumber %d.

Description

The Manufacturing grid is used for geometry allignment to snap the shapes and cells into the manufacturing grid. The Manufacturing grid value must be a positive number specified in microns.

What Next

Check the MANUFACTURINGGRID value in the LEF file provided to the set_eco_options for correctness.

LEFR-052

(warning) Redefinition of MANUFACTURINGGRID value, previously set to '%s', now set to '%s' found at lineNumber %d.

Feedback

Description

Multiple definitions of the manufacturing grid statement have been detected with different values. Will ignore the duplicate definition and use the previously set MANUFACTURINGGRID value.

What Next

Check the MANUFACTURINGGRID value in the LEF files provided to the set_eco_options for correctness. Multiple definitions suggest the LEF files could belong to different technology nodes.

LEFR-053

(warning) Identified polygon shaped LEF obstruction on a layer not of TYPE OVERLAP at lineNumber %d. This obstruction will be ignored. If this LEF obstruction is intended to create notches in the LEF macro, the notches will not be created and a rectilinear shaped macro will be created instead.

Description

If this polygon shaped LEF obstruction is a routing obstruction, this warning can be ignored. If this polygon shaped LEF obstruction is a placement obstruction it must be defined on a layer of TYPE OVERLAP. LEF layer definitions are usually provided in the technology LEF file. Ensure the technology LEF file is provided to the set_eco_options.

What Next

Check the order of LEF files provided to the set_eco_options for correctness. When multiple LEF files are provided the -tech_lef_files option of set_eco_options should be used to provide the technology lef file. Incase the -tech_lef_files option is not used the first LEF file provided to the -physical_constraint_file will be treated as the technology LEF file. It is not mandatory for Layer definitions to exist in the technology LEF file. However they must be provided in a LEF file prior to usage of the LEF obstruction.

LEFR-054

(warning) No Technology Library Exchange Format (LEF) files provided to set_eco_options.

Description

The set_eco_options command provided the -physical_tech_lib_path option to provide the path to the Technology Library Exchange Format (LEF) files. PrimeTime reads the Technology Library Exchange Format (LEF) files prior to reading in the cell LEF files. The Technology LEF files contain physical constraints that apply to all cell LEF files. Some of the important physical constraints specified in the technology LEF files include

Feedback

layer definitions, via definitions, viarule definitions and overlapped layer constructs used to specify polygon shapes for LEF macros. When multiple LEF files are available it is recommended that this option be exercised to provide the right Technology LEF files. When multiple LEF files are available and the Technology LEF files are not provided, the order in which the LEF files are provided becomes critical. If the order of the LEF files is such that the Technology files are not provided prior to the cell LEF files, physically aware ECO commands will not have the right physical constraint definitions. This can lead to poor QOR and/or incorrect physical ECO results.

What Next

Ensure the Technology LEF files are provided to the set_eco_options.

LEFW

LEFW-001

(error) The specified design '%s' has neither frame view nor design view.

Description

Neither design not frame views created for design.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

LEFW-002

(error) Cannot find layer of layer number %d.

Description

Missing layer definition.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

LEFW-003

(error) Fail to write %s '%s' of %s '%s'.

Feedback

Description

Invalid LEF syntax detected.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

LEFW-004

(Information) Block '%s' has %s view with multiple labels, will write out empty label only.

Description

Multiple labels detected for block.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

LEFW-005

(warning) Block '%s' has no %s view with empty label, will ignore it.

Description

Ndm block has no views created.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

LEFW-006

(warning) The frame view with non-empty label '%s' will be written out for block '%s'.

Description

Frame view has non empty labels.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

Feedback

LEFW-007

(error) Use %s %s as the WRONGDIRECTION width for layer '%s'.

Description

Wrong direction width specified for layer in ndm lef.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

LEFW-008

(warning) Terminals with eeq_class %d of block '%s' will be outputted in different PORT sections.

Description

Usually, terminals with same eeq_class will be outputted in one PORT section so that when read back the LEF, proper eeq_class can be derived. However, for the terminals of the reported block and eeq_class, they have different classes. So they will be outputted in different PORT section as every PORT section can have only one class. That means the eeq_class information of these terminals will be lost.

What Next

Please correct the eeq_class or class attribute for the reported terminals and try again.

LGL

LGL-001

(error) Placement attributes of instance %s do not match any sites.

Description

Leaglization could not find any sites in the floorplan with the same site definition, voltage area and exclusive move bound as this cell instance.

What Next

Find the site definition the reference cell. Check that the design contains site rows with this site definition. Next, check that the voltage area of the cell includes valid sites. If the voltage area is embedded inside another voltage area, make sure the stacking order allows it to be seen, *i.e.*, it is not completely covered by other voltage areas. Finally, if

Feedback

the cell belongs to an exclusive move bound, make sure it also includes valid sites in the proper voltage area.

LGL-002

(warning) Spare cell instance %s is not placed.

Description

This cell is a spare cell but is marked as unassigned. Legalization will ignore this cell.

What Next

Spare cells should be placed by the *create_placement* or other commands which call *create_placement* internally. If this was done, and the cells are still unplaced, then contact the developers.

LGL-003

(warning) Standard cell instance %s is not placed.

Description

This cell is marked as unassigned. Legalization requires that all non-spare standard cells have a valid placement, otherwise this cell will be ignored during legalization.

What Next

Make sure that *create_placement* was run previously, either as a stand-alone command or from within another command, and succeeded.

LGL-004

(error) Cell instance %s is not placed.

Description

This cell has not been placed in the floorplan.

What Next

Make sure the cell is placed in the floorplan.

LGL-005

(warning) Cell instance %s has no reference cell and cannot be legalized.

The named cell has no reference cell. It will be assumed to be a blockage.

Feedback

What Next

This problem is usually caused when a design is opened and the reference library is missing. Make sure your input is data correct.

LGL-006

(warning) Reference %s has no design and cannot be legalized.

Description

The named reference cell has no design associated with it. Cell instances with this reference will be assumed to be blockage.

LGL-007

(error) Site row %s overlaps %s with the same site definition.

Description

Site rows are not allowed to overlap.

What Next

Check your floorplan to find overlapping rows. Modify your DEF file to eliminate the overlap.

LGL-008

(error) Could not initialize physical design checker.

Description

The legality subsystem could not start the physical design checker.

What Next

Look for PDC-NNN messages for more information.

LGL-009

(error) Site rows with site definition %s are misaligned.

Description

All the site rows with the same site definition must be aligned such that there is no vertical offset between sites.

Feedback

What Next

Change the floorplan so that the rows align properly. Ensure that the distance between x-origins of the different rows is zero modulo the site width.

LGL-010

(Error) Incompatible site rows overlap.

Description

Site rows with different site definitions cannot overlap unless the site definitions are compatible. A site definition is compatible with another site definition if its dimensions are an integral multiple of the dimensions of the other site definition. Rows with compatible site definitions can overlap if their sites are aligned.

What Next

Change the floorplan so that the incompatible rows do not overlap. If the rows should be compatible, make sure they are aligned properly.

LGL-011

(error) Design has no site rows.

Description

There are no site rows defined for the design. Site rows are required for placement.

LGL-012

(error) Cell %s is not in a proper voltage area.

Description

This message is indicating that this cell instance is not inside its corresponding voltage area.

What Next

Move this cell instance into the correct voltage area boundary manually or through command legalize_placement.

LGL-013

(error) This design is not MV ready, please check the UPF setting for your design.

Feedback

Description

This message is indicating that some UPF problem has been detected, and the run cannot proceed.

What Next

Check the UPF setting and correct the problem.

LGL-014

(error) Cell %s is not in a proper movebound.

Description

This message is indicating that this cell instance is not inside its corresponding movebound.

What Next

Move this cell instance into the correct movebound boundary manually or through command legalize_placement.

LGL-015

(error) cell instance %s is illegal for all sites.

Description

This message is indicating that the legalization has detected that the above cell instance is illegal for all sites, in other words, this cell instance cannot be placed legally within this design.

As below are some frequently encountered situations which may cause this issue:

(1) This cell belongs to multiple exclusive bounds, voltage areas at the same time, but these exclusive bounds and/or voltage areas do not have "common area".

(2) This cell may be specified with one site master, but there is no such type of site rows within this design.

(3) This cell may contain some complex pin shape, which may be illegal for all pnet checking.

What Next

Customer may need to double check the design constraint setup, make sure that each cell instance can have some "legal locations" to be placed into.

Feedback

LGL-016

(error) Cell %s violates one or more pnets.

Description

This message is indicating that this cell instance is violating one or more pnet straps in the design.

What Next

Run command legalize_placement.

LGL-017

(error) Cell %s and cell %s are violating one or more standard cell spacing rules.

Description

This message is indicating that this cell instance and one other neighbor cell are violating one or more standard cell spacing rules.

What Next

Run command legalize_placement.

LGL-018

(error) Cell %s and cell %s are violating CTS cell spacing rules.

Description

This message is indicating that this cell instance and one other neighbor cell are violating CTS cell spacing rules.

What Next

Re-run the CTS commands.

LGL-019

(error) Cell %s is unplaced and will not get processed by checker or legalizer

Description

This message is indicating that this cell instance is unplaced.

Feedback

What Next

Assign one initial location for this cell instance.

LGL-020

(error) Cell %s is overlapping with cell %s .

Description

This message is indicating that this cell instance and one other neighbor cell are overlapping each other.

What Next

Run command legalize_placement.

LGL-021

(error) macro cell %s is overlapping with macro cell %s .

Description

This message is indicating that this macro cell and one other neighbor cell are overlapping each other.

What Next

Move the macro cell to remove the overlapping.

LGL-022

(error) cell %s is overlapping with blockage %s .

Description

This message is indicating that this cell instance is overlapping with a blockage.

What Next

Run command legalize_placement.

LGL-023

(error) Cell %s is not in a proper row.

Description

This message is indicating that this cell instance is not inside a proper row.

Feedback

What Next

Run command legalize_placement.

LGL-024

(error) Cell %s has an illegal orientation.

Description

This message is indicating that this cell instance has an illegal orientation.

What Next

Run command legalize_placement.

LGL-025

(warning) Site master "%s" has both X-Symmetry and Y-Symmetry. Usually, this may not be correct, and may cause the legalization to fail.

Description

This message is indicating that the legalization has detected that the above site master has both X-Symmetry and Y-Symmetry at the same time. For a normal design, usually, the site master may have only one "site symmetry", either "X-Symmetry" or "Y-Symmetry". A site master having both "X-Symmetry" and "Y-Symmetry" at the same time may cause the legalization to fail.

What Next

Please double-check the design and library setting and make sure the setting is correct.

LGL-026

(information) Using "Y-Symmetry" for site master "%s" in legalization because this is a horizontal design.

Description

This message is indicating that the legalization has detected that the above site master has both X-Symmetry and Y-Symmetry at the same time. Usually, for a normal horizontal design, the site master may have "site symmetry" of "Y-Symmetry" only.

What Next

Please double-check the design and library setting and make sure the setting is correct.

Feedback

LGL-027

(information) Using "X-Symmetry" for site master "%s" in the legalization because this is a vertical design.

Description

This message is indicating that the legalization has detected that the above site master has both X-Symmetry and Y-Symmetry at the same time. Usually, for a normal vertical design, the site master may have "site symmetry" of "X-Symmetry" only. A site master having both "X-Symmetry" and "Y-Symmetry" at the same time may cause the legalization to fail.

What Next

Please double-check the design and library setting and make sure the setting is correct.

LGL-028

(error) This design has both horizontal site rows and vertical site rows, which cannot be supported.

Description

This message is indicating that the legalization has detected that this design has both horizontal site rows and vertical site rows at the same time.

This type of designs cannot be supported by the legalization at this time. One design can have either horizontal site rows or vertical site rows at one time.

What Next

Please double-check the site row specification.

LGL-029

(error) The legalization cannot place the block because it is over capacity (density is %5.1f%%).\n \tPlease enlarge the size of the legalization working area and/or reduce the number of the contained cells.

Description

This message is indicating that the legalization has detected that the standard cells area is over utilized (more than 100%) in this area, so the legalization cannot produce a legal placement for your block.

Feedback

What Next

Increase the legalization working area (for example, adding more site rows, reducing placement blockage areas, etc), or reduce the number of movable standard cells within this area.

LGL-030

(warning) Cell instance %s (lib_cell: %s) does not have initial location.\n \tAssign it to the low left corner of the core area.

Description

This message is indicating that the legalization has detected that the input cell instance does not have initial location. It is recommended that all cell instances should contine initial locations before running legalization.

What Next

Check the design flow, make sure all cell instances have initial locations before running legalization.

LGL-031

(warning) Site master "%s" has neither X-Symmetry nor Y-Symmetry. The "legal orientations" for the standard cells will be limited.

Description

This message is indicating that the legalization has detected that the above site master has neither X-Symmetry nor Y-Symmetry. For a normal design, usually, the site master may have either "X-Symmetry" or "Y-Symmetry".

If a site master does not have either of "X-Symmetry" and "Y-Symmetry", the standard cells will have limited legal orientations because the standard cells will not be allowed to flip within the site rows.

What Next

Please double-check the design and library setting and make sure the setting is correct.

LGL-032

(information) The Variant-aware Legalization started.

Description

This message is indicating that the Variant-aware Legalization is running.

Feedback

What Next

Check the Variant-aware Legalization result.

LGL-033

(information) The Variant-aware Legalization succeeded.

Description

This message is indicating that the Variant-aware Legalization finished successfully.

What Next

Check the Variant-aware Legalization result.

LGL-034

(error) A legal placement could not be found.

Description

This message is indicating that the legalization cannot find a legal placement for this block. You probably have to enlarge the core area and re-try.

What Next

Check the design setting, and make sure all of the constraints are correct. If no problem has been found, then you may need to enlarge the core area.

LGL-035

(error) Cell %s has a Gemini violation.

Description

This message is indicating that this cell instance is violating one Gemini constraint in the design.

What Next

Run command legalize_placement.

LGL-036

(warning) Cell %s is out of the core area.

Feedback

Description

This message is indicating that this cell instance is out of the core area.

What Next

Move this cell into the core area manually or run command legalize_placement.

LGL-037

(information) Fixed cell %s has been swapped because it has a "gemini_swap_only" attribute.

Description

This message is indicating that this cell instance has been swapped to meet the Gemini constraint in the design. Usually, the legalization should not touch a "fixed cell". However, if a fixed cell contains "gemini_swap_only" attribute, then it is expected that this cell can be "swapped".

What Next

Run command legalize_placement.

LGL-038

(information) %s been swapped because attribute "gemini_swap_only" has been set.

Description

This message is indicating that some fixed cell instances have been swapped to meet the Gemini constraint in the design.

What Next

Run command check_legality.

LGL-039

(error) Cell %s violates CPODE L2 rule

Description

This message is indicating that this cell instance is violating CPODE L2 rule.

What Next

Run command legalize_placement.

Feedback

LGL-040

(error) Color violation detected between cell %s and cell %s .

Description

This message is indicating that color violation is found between two abutted cells.

What Next

Run command legalize_placement.

LGL-041

(error) Cell %s violates OD L5 rule

Description

This message is indicating that this cell instance is violating OD L5 rule.

What Next

Run command legalize_placement.

LGL-042

(Warning) Advanced rule query engine not initialized. No advanced rule checking performed.

Description

This message is indicating that there was an error in initialization of the advanced rule query engine and thus no advanced rule checking will be performed by optimization. This may result in illegal placement.

What Next

Review the design and floorplan preparation.

LGL-043

(error) Cell %s pin color alignment check.

Description

This message is indicating that this cell instance is violating pin color alignment in its current location.

Feedback

What Next

Run command legalize_placement.

LGL-044

(error) Design has vertical site rows.

SH DESCRIPTION There are vertical site rows defined for the design. Vertical site rows are not currently supported.

LGL-045

(error) Site rows with site definition '%s' are not covered by base site rows (%s).

Description

If site rows with different compatible site definitions overlap, then there must be a base site definition whose rows cover all other site rows. When there are multiple site definitions with overlapping rows, the base site definition is determined to be the one with the smallest dimensions whose rows occupy the largest area. All other site definitions must be have dimensions that are multiples of the base.

What Next

Modify the floorplan so that there is a base site definition whose rows completely cover the rows of compatible site definitions.

LGL-046

(Warning) Library cell

Description

The warning message tells user that there are inconsistent setup between design and library. The site def used in current design has different width or height compared to same site def name used in library. User should have consistent setup between design and library, otherwise it may cause legalization error. If any placeable cell instance is from this library cell, it will result in LGL-047 error and legalization will stop.

What Next

Please make sure site def width and height are same between design and libraries.

LGL-047

(Error) Placeable cell %s has inconsistent site def defined in design and library.

Feedback

Description

This error tells user that the site def definition used in current design is not consistent with library. For example, site def defined in current design has width 1240, height 2480. However, the site def used in library cell has width 500, height 1000. When this cell is not fixed, which is placeable, but their definitions are inconsistent between design and library, legalize_placement cannot place it because it cannot place a cell with width 500 and height 1000 into current design's row with width 1240, height 2480.

What Next

Please refer previous warning message LGL-046 to see which library cell and the detail information

---

LGL-048

(Warning) Library cells %s and %s have different supply architectures.

Description

Based on their site definitions and the corresopnding site rows, the two library cells are intended to be placeable together in the same row. In the normal R0 orientation, however, one cell appears to have its ground pin at the bottom while the other has its power pin at the bottom creating a conflict.

What Next

The most common cause of this error is incompatible libraries which use the same site definition being loaded together. Either they need to use different site definitions, or they cannot both be present at the same time.

LGL-049

(Warning) Cannot determine %s supply pin for library cell %s.

Description

When examining the geometries of the power and ground pins, it could not be determined which is at the top or bottom of the cell.

What Next

In most cases this warning can be ignored. This information is only used when the LEF/DEF information is insufficient to determine the legal rows for multi-row cells. It may indicate a problem in library preparation, or this cell may have a special purpose for which the pin geometries are unusual but correct.

Feedback

LGL-050

(Warning) Library cell %s is missing supply pins. Its power structure cannot be determined.

Description

When examining the geometries of the power and ground pins, one or both waas missing. Subsequent analysis will assume that the ground rail lies along the bottom of the cell when in the normal (R0) orientation.

What Next

This information is only used when the LEF/DEF information is insufficient to determine the legal rows for multi-row cells. It may indicate a problem in library preparation.

LGL-051

(warning) Could not find legal location for cell instance %s(%s).

Description

This message is indicates that a legal location could not be found for this cell during legalization. There are many possible causes for this. Below is a partial list.

(1) The legalizer may be trying to place the cell in a region that is over-constrained.

(2) This cell belongs to multiple exclusive bounds, voltage areas at the same time, but these exclusive bounds and/or voltage areas do not have "common area".

(3) This cell may be specified with one site definition, but there is no such type of site rows within this design.

(4) This cell may contain some complex pin shape, which may be illegal for all sites.

What Next

Check the design setup with respect to bounds or voltage areas. If the pass-rate of the reference of this cell is very low or zero (see command 'analyze_lib_cell_placement'), then check the design rule setup (disable individual rules and rerun legalization).

LGL-052

(warning) Unable to swap lib cell from %s to %s (variant index %d) on cell %s due to color alignment check.

Description

This warning message indicated that there is one lib cell cannot be swapped to other lib cell to fix color alignment violation, and the corresponding lib cell and its variant index

number failed due to color alignment check. User will only see this warning message when all variants defined in the variant cell group cannot fix current color alignment violation by swapping. User must go back to check all variants defined in the cell group and investigate why all variants cannot fix the violation.

When variant swapping failed, legalizer will start a normal legalization by moving cells to fix the rest violations. If users don't want to have additional legalization run, they can use *set_app_option -name place.legalize.enable_full_variant_check -value true* to make legalizer performs real check on all queries to make cells defined in invalid cell group will be moved automatically. However, by using that app option, it may have runtime impact depends on the query and variant status.

What Next

report_cell_groups set_app_option -name place.legalize.enable_full_variant_check -value true

---

LGL-053

(warning) Unable to swap lib cell from %s to %s (variant index %d) on cell %s due to pnet check.

Description

This warning message indicated that there is one lib cell cannot be swapped to other lib cell to fix color alignment violation. To fix color alignment by swapping lib cells, legalizer will check both color alignment and pnet, not only color alignment. If user receives this message, but there is no LGL-052 message at all, that means this lib cell has color matched, but it will cause pnet violation so legalizer will not be able to swap this lib cell. If user receives both LGL-052 and LGL-053 messages, that means this variant lib cell is not valid to swap by color alignment check and pnet check.

User will only see this warning message when all variants defined in the variant cell group cannot fix current color alignment violation by swapping. User must go back to check all variants defined in the cell group and investigate why all variants cannot fix the violation.

When variant swapping failed, legalizer will start a normal legalization by moving cells to fix the rest violations. If users don't want to have additional legalization run, they can use *set_app_option -name place.legalize.enable_full_variant_check -value true* to make legalizer performs real check on all queries to make cells defined in invalid cell group will be moved automatically. However, by using that app option, it may have runtime impact depends on the query and variant status.

What Next

report_cell_groups set_app_option -name place.legalize.enable_full_variant_check -value true

Feedback

LGL-054

(information) %s moved %d cells (%.1f%%) with an average displacement of %.3lf and a maximum of %.3lf.

Description

This message indicates how many cells where moved and how much they where moved during a certain phase of the legalizer. The average displacement is the average over all cells that moved.

LGL-055

(error) There %s %d cell%s which cannot be legalized.

Description

This message summarizes the amount of cells for which no legal location could be found. Message LGL-051 indicates which cells are affected.

What Next

Please check whether the design is over-utilized or constraints are not correctly applied.

LGL-056

(warning) Could not find layer '%s' in the design technology library. Ignoring shapes on this layer for pin '%s/%s'.

The given library cell pin has shapes on a layer which is not present in the design's technology library.

What Next

Make sure that all library cells are bound to the same tech library (reference) as the current design.

LGL-057a

(warning) Unbound instance '%s' is ignored by the legalizer.

Description

The instance shown is unbound, that is, it is not mapped to any library cell, or it is not mapped to a library cell with a physical view. As such, it cannot be legalized, so the legalizer is ignoring it. A summary of how many instances are unbound is covered by LGL-057. By default, 10 of these will be displayed when the legalizer is initialized.

Feedback

What Next

Make sure that all cells in the design are bound to a reference library cell.

See Also

- LGL-057

LGL-057

(warning) %d cell%s not bound to any reference.

The given number of cells are unbound, i.e. they are not mapped to any library cell.

What Next

Make sure that all cells in the design are bound to a reference library cell.

LGL-058

(error) The number of references must be greater than 0 for the command.

The command requires the number of references to be greater than 0.

What Next

Ensure that the number of reference value is greater than 0.

LGL-059

(Error) Site '%s' has a height (%s) which is not a multiple of the base site '%s' height (%s).

Description

All sites need to have a height which is a integer multiple of the base site height. All other site configurations are not accepted by the legalizer. An exception are half height sites used in inbound flows. This rule also applies to non-overlapping site rows.

What Next

Please correct the site row definitions.

LGL-060

(warning) Could not find legal location for cell instance %s(%s).

Feedback

Description

This message is indicates that a legal location could not be found for this cell. There are many possible causes for this. Below is a partial list.

(1) The current command may be trying to place the cell in a region that is over-constrained.

(2) This cell belongs to multiple exclusive bounds, voltage areas at the same time, but these exclusive bounds and/or voltage areas do not have "common area".

(3) This cell may be specified with one site definition, but there is no such type of site rows within this design.

(4) This cell may contain some complex pin shape, which may be illegal for all sites.

What Next

If the cause is reason (1) above, the command will usually adapt and this message is informational only. Otherwise, there may be a problem with the design. If 'legalize_placement' also fails, then further investigation is required. If legalization succeeds, then the message may be ignored.

LGL-061

(warning) Cell '%s' has an orientation '%s' with 90 degree rotation. Most rule checks are disabled for this cell.

Description

The given cell is 90 degree rotated. The cell is not legalizable.

What Next

You need to change the orientation of the cell to R0, MX, MY, or R180.

LGL-062

(warning) No site rows found for site '%s'.

Description

The given site definition has no site rows defined. The given site definition will be ignored and all cells referring to that site won't get legalized.

What Next

You need to define site rows for the given site definition.

Feedback

LGL-063

(error) There is no site row or array found in the design.

Description

No site definitions with rows were found in the design. The design cannot be legalized.

What Next

You need to define site definitions with site rows for all sites referred to by the cells in the design.

LGL-064

(error) Unable to find site rows to legalize cell '%s'.

Description

No site rows were found to legalize the given cell.

What Next

You need to define site definitions with site rows for all sites referred to by the cells in the design.

LGL-065

(error) Unable to legalize cell '%s' because cell width '%s' is not multiple of site (%s) width '%s'.

Description

The width of the given cell is not a multiple of the width of the associated site defintion.

What Next

You need to assign a suitable site definition to the lib cell of the given cell.

LGL-067

(error) Cell %s with reference %s is is misaligned.

Description

This message is indicating that this cell instance is not aligned to a site row.

Feedback

What Next

Make sure that all cells are properly placed and aligned to site rows before running the command that generated the error message.

LGL-068

(Error) TPO width error encountered near %s.

Description

You received this error message because tool encounters unexpected condition during TPO width checking around indicated cell. If you encounter this error running filler insertion, the possible cause is design is not legality clean before.

What Next

1. If running filler insertion, please ensure check_legality is clean before filler insertion.
   2. Please use below option to specify cells whose TPO layer not exntend to left or right edge of cell: set_app_options -name place.legalize.cpode_exception_cells -value "BOUNDARY TAP"

LGL-069

(warning) Library cell %s has missing vertical abutment indexes

Description

This library cell provides only partial vertical abutment indexes. Missing indexes will be ignored.

What Next

Make sure library cell contains vertical abutment indexes on both top and bottom edges

---

LGL-070

(warning) Library cell %s has missing vertical abutment indexes; duplicate missing indexes from other side.

Description

This library cell provides only partial vertical abutment indexes. Missing indexes will be duplicated from the top/bottom side with indexes.

What Next

Make sure library cell contains vertical abutment indexes on both top and bottom edges

Feedback

LGL-071

(warning) %s%s%s It cannot be used to reduce displacement during variant aware legalization.

Description

The reported library cells are part of a common cell group (variant definition), but these library cells are not compatible, i.e. one cannot replace the other. The legalizer won't use these library cells as variants for each other.

What Next

Make sure that the library preparation and cell group definiton only references library cells that can be used for sizing a cell. Use the 'report_cell_groups' command to get an overview of the defined sets of variants.

LGL-072

(warning) %s '%s' has cells attached but does not overlap the core area.

Description

This message is printed for move bounds and voltage areas. The given bound or voltage area doesn't overlap the core area and hence the cells attached to it cannot be legalized.

What Next

Make sure that either the bound or voltage area doesn't have any cells attached or it overlaps the core area (standard cell placement area).

LGL-073

(error) The advanced checker/legalizer has detected non-abutting or non-aligned site row %s at coordinate {%s}.

Description

A site row configuration has been found which is not supported by default.

What Next

Try using the app option place.legalize.legalize_non_uniform_va_exbound

LGL-074

(warning) No filler cells present in the reference library of the design.

There are no cells in the design marked as filler cells. Neither does any cell present in the reference library has filler design type, nor has the user provided list of filler cells. This may lead to gaps between the standard cells after placement, and therefore DRC violations or discontinuity in PG rails connections.

What Next

Make sure that there are appropriately defined filler cells in the reference library to avoid any design violations.

LGL-075

(warning) Spacing rules are being applied to lib/CTS cell %s.

Spacing rules on a lib/CTS cell will result in rules being directed to each and every cell having the same lib cell. If applied to a larger number of library or CTS cells might cause a longer runtime in AL.

What Next

Reduce number of lib cells having spacing rules while running advanced legalizer.

LGL-076

(information) Via ladder spacing app_option or command being used which is not required during AL.

App_options and command related to via_ladder_spacing are for classic legalizer and there is no need to use them while running AL. Advanced legalizer supports these setting in a more advanced manner.

LGL-077

(warning) Smallest size of filler cells present in the library is %.2f, which is larger than the smallest site width.

1X size filler cell unavailable in the library to fill gaps. The lack of fillers sized = 1 typically cause extra constraints to legalization as the legalizer can't leave a gap 1X wide.

What Next

Check the filler cell definitions in the reference libraries.

LGL-078

(error) Site symmetry is set incorrectly : Y symmentry = %d, X symmentry = %d.

Feedback

Default site symmentry is "Y" after ICC2 floorplan creation. Since, symmetry determines legal orientations during legalization, incorrect symmetry will result in failure during filler cells insertion in Advanced Legalizer.

What Next

Set the site symmetry correctly before running AL.

LGL-079

(warning) Vertical keepout will be considered as place.legalize.advanced_ignore_vertical_keepout_margin is false. This may cause runtime and displacement issues during legalization.

Description

Vertical keepouts cause significant displacement degradations during legalization. It may lead to over constraining. So the legalizer aborts if many cells have vertical keepout margins.

What Next

Turn on the app option place.legalize.advanced_ignore_vertical_keepout_margin

---

LGL-080

(warning) The bound %s of type %s has a high utilization of %.3g which could lead to high runtime.

Description

The VA or bounds with this high density could lead to longer runtime.

What Next

Stop the run.

LGL-081

(warning) The command set_legalizer_preroute_keepout is not supported by the advanced legalizer.

Description

The preroute keepout command is not supported by the advanced legalizer and nplDRC.

What Next

Do not run this command.

Feedback

LGL-082

(warning) Stream place is not required in Advanced Legalizer

Description

Stream place is no longer needed in Advanced legalizer. Stream place replaces single large displacement with a stream of small displacements but Advanced Legalizer is taking care of this already.

LGL-083

(error) The cell %s is unplaced and outside the core area.

Description

When the cell is present outside the core area and is unplaced, it may lead to longer runtime.

LGL-084

(warning) For color rules defined in tech file, the design has layer with colored routing tracks = %s, and/or colored stdcells' pins = %s.

Color rules for standard cells' pins in the frame and routing tracks on a layer at design level should not be mismatched, i.e., either both or neither must be colored.

LGL-085

(Error) Filler prediction failed due to off-site-row cells.

Description

You received this error message because tool encounters unexpected condition during OD Edge Rule checking due to off-site-row cells. If you encounter this error during check_legality, the possible cause is design is not legalized before.

What Next

If running check_legality, please ensure legalize_placement is run before.

LGL-086

(warning) Cell %s is unplaceable after %d trials.

Feedback

Description

This message is printed if a cell cannot be legalized after specified number of tries during legalization.

What Next

Check the library-cell and the floorplan to see why the cell difficult to legalize. For unlimited number of trials to legalize, set app-option place.legalize.limit_legality_checks to false.

LGL-087

(warning) %lu cells with invalid orientation present in the design.

Description

If a cell has bad orientation, it will not be legalized.

What Next

Check the library-cell and the floorplan to see why the cell has invalid orientation. If such cells are present in the design, run create_placement before legalizer.

LGL-088

(warning) Ignoring cell '%s' from IR-drop optimization%s.

Description

The legalizer cannot move the specified cell due to the given reason. IR-drop optimization will be limited around this cell.

What Next

This message might, for example, show up after clock tree synthesis where most of the sequential cells are marked as fixed. In this case, this user can ignore the warning but should be aware that the IR-drop optimization has limited room to move cells.

LGL-089

(warning) cellmap ignored instance with missing physical info: %s

Description

cellmap is asked by the client to operate on the instance (e.g. add/remove) that doesn't have needed physical info. For instance, the instance may lack a reference (i.e. it is set as NULL) or the reference doesn't have proper definition of sites assigned.

Feedback

What Next

If the instance reported should not have been ignored then the user is to verify that proper physical data present either in the reference library or the given block.

LGL-090

(warning) Via ladder constraint %s of lib cell %s does not match its pin structure, so the via ladder check on the cell instances derived from this lib cell with the given via ladder constraint is bypassed.

Description

You received this warning message because there exists a lib cell, denoted by $lc, in your design having a short pin such that advanced legalizer is not able to grow a via ladder on it based on the given via ladder constraint, because advanced legalizer does NOT support automatically pin extension. Advanced legalizer will automatically bypass the via ladder checks on those cell instances of the lib cell $lc, and still perform via ladder checks on other normal cells if the app option place.legalize.enable_via_ladder_checks was enabled.

What Next

You can take one of the following actions to fix this warning. 1. Modify the mismatched via ladder constraints such that advanced legalizer can grow via ladders on pins without pin extension. For example, decrease the number of cut rows/cuts per row. 2. Modify the cell layout by manually extending the short pins

---

LGL-091

(warning) Found duplicate spacing rule %s(%d) - %s(%d) %u - %u in library '%s'.

Description

The tool picks up spacing rules first from the design library, and then from the reference libraries. This message indicates that duplicate definitions of spacing rules were found. The occurance of this situation has no impact and QoR.

LGL-092

(warning) Ignoring already existing max. horizontal width label '%s' of library '%s'.

Description

The tool picks up maximum horizontal with labels first from the design library, and then from the reference libraries. This message indicates that duplicate definitions of labels were found (see PRF flow).

Feedback

LGL-093

(warning) Ignoring vertical abuttment rules from reference library '%s'.

Description

The tool picks up vertical abuttment rules first from the design library, and then from the reference libraries. This message indicates that abuttment rule definitions were found in the design library as well as in the given reference libary. The ones from the reference library are ignored.

LGL-094

(warning) Routing layer '%s' has a non uniform routing pitch.%s

Description

Certain runtime improvement settings and optimizations require that lower routing layers have a constant track pitch.

LGL-095

(warning) Lib-cell '%s' has %s '%s' which is not a multiple of the VT site %s '%s'. VT information will be ignored.

Description

The given library cell has a width or height which is not an integer multiple of the considered VT site map. The library cell will hence be ignored for any VT implant checks.

LGL-096

(information) Lib-cell '%s' is vertical stacked length exception lib-cell.

Description

The given library cell is ignored for the vertical stacked length design rule check.

LGL-097

(warning) The safety register '%s' is marked as fixed but requires spacing for tap cell insertion.

Feedback

Description

A safety register rule hass been defined for the given cell which requires tap cells next to it. Since the cell is fixed, the legalizer cannot move the cell to enforce enough space net to the cell.

LGL-098

(warning) The design contains library cells, example %s, having very low legalization pass rates.

The design has cells with zero or low pass rates. This will cause a longer runtime during legalization because a cell with low pass rate would mean that as compared to the number of sites tested, it is placeable at a very small number of sites in any orientation.

What Next

Run analyze_lib_cell_placement to identify problem cells.

LGL-099

(warning) On-by-default app options : place.legalize.enable_cell_spreading is set as false = %s ; and place.legalize.enable_cell_ordering is set as false = %s in the design.

Description

On-by-default app options for enable_cell_spreading and enable_cell_ordering, both are required to be always true in advanced legalizer.

What Next

Turn on these app options before running AL.

LGL-100

(warning) Metal1/Metal2 PG rails in the design at coordinates {%s} have shape type = %s.

M1/M2 PG rails should have only one of the following shape types : lib_cell_pin_connect or follow_pin or stripe. If the rails has shape other than these, say "user_route", the legalizer considers it route specific to a specific pin and not the primary PG grid. Any other PG shapes other than the three mentioned above cause long runtime/hang while running advanced legalizer.

What Next

Check the design and set the PG rails properly.

Feedback

LGL-101

(warning) The cell '%s' has incorrect site definition %s.

Lib-cells used in this design either do not have a site association, or have a site def for which there are no site rows nor site arrays in the design. These cells cannot be placed anywhere.

LGL-102

(warning) For overlapping site rows, the dimensions of their site definitions, namely %s and %s, are not an integral multiple of the dimensions of base site def.

If overlapping site rows are present in the design, the height or width of their respective site defs should be integral multiple of the base/unit site def which is determined as the site def with the smallest dimensions.

LGL-103

(warning) Site rows with site definition %s are misaligned.

Description

All the site rows with the same site definition must be aligned such that there is no vertical offset between sites.

What Next

Change the floorplan so that the rows align properly. Ensure that the distance between x-origins of the different rows is zero modulo the site width.

LGL-104

(warning) Library cell %s doesn't have sufficient allowable orientations.

Description

Allowable orientations on lib cells and possible legal orientations on the site rows have no legal orientation in common. The cell won't find a legal placable orientation, hence causing longer runtime.

What Next

Set place.legalize.enable_allowable_orient false.

Feedback

LGL-105

(warning) Cell map created for block %s is invalid.

Description

Current design has one or more invalid cell maps, which might cause the command to assert. Cell map data is not being generated properly. This might occur due to variety of reasons realted to bad/dirty design inputs (such as, missing physical information).

What Next

Check design before running.

LGL-106

(Warning) For color rules defined in tech file, the design has layer %s with colored routing tracks = %s, but colored stdcells' pins = %s.

Color rules for standard cells' pins in the frame and routing tracks on a layer at design level should not be mismatched, i.e., either both or neither must be colored.

What Next

Check the color contraints of the afrementioned layer in this design or revise your app option settings.

See Also

- LGL-084

LGL-107

(warning) Overlapping site rows having site defs %s and %s not completely used in the design floorplan.

Overlapping site rows must cover the entire site array.

LGL-108

(warning) Spare cells present in the design at {%s} are pre-clumped.

Clumping of spare cells together might cause high local density in the design, hence causing longer runtime.

Feedback

LGL-109

(warning) Direction for routing layer %s is not specified.

Routing layer must have a direction (horizontal or vertical) defined.

LGL-110

(warning) Zero spacing blockage %s is present on PG net %s.

Large zero-spacing blockages not excluded from PG net will hang the legalizer engine.

What Next

Please set net type (eg., clock, reset, scan, signal, tie_high, tie_low) for zero spacong blockages.

LGL-111

(warning) %s

Description

This message is to communicate to the user that for the specified cell (or reference cell) cellmap runs into lengthy search operation to find legal location.

What Next

The user needs to be aware that layout internals of the particular cell (or reference cell) may interacts with existing routing that limits available locations where the cell (or reference cell) can be legally placed. Also the user needs to be aware that lacking appropriate filler cells in the library may manifest itself in a similar way. In each case the cell (or reference cell) needs to be looked at from this perspective. Refining settings for cellmap checks may be needed.

See Also

- LGL-113

LGL-112

(warning) %s

Description

This message is to communicate to the user that for the specified cell (or reference cell) cellmap runs into lengthy search operation to find legal location (iterating rows).

Feedback

What Next

The user needs to be aware that layout internals of the particular cell (or reference cell) may interacts with existing routing that limits available locations where the cell (or reference cell) can be legally placed. Also the user needs to be aware that lacking appropriate filler cells in the library may manifest itself in a similar way. In each case the cell (or reference cell) needs to be looked at from this perspective. Refining settings for cellmap checks may be needed.

See Also

- LGL-113

LGL-113

(warning) %s

Description

This message serves to print out Legality Checks Profile that captures effort and statistics for the specified cell (or reference cell) when cellmap does search to find legal location.

What Next

The user needs to be aware that layout internals of the particular cell (or reference cell) may interact with existing routing that limits available locations where the cell (or reference cell) can be legally placed. Also the user needs to be aware that lacking appropriate filler cells in the library may manifest itself in a similar way. In each case the cell (or reference cell) needs to be looked at from this perspective. Refining settings for cellmap checks may be needed.

See Also

- LGL-111
- LGL-112

LGL-114

(information) %s

Description

This message serves to print out Legality Checks Profile for each executed FLL (find legal location) query by cellmap along with additional debug information like number of checks, elapsed CPU and Wall time.

Feedback

What Next

The user can grep these messages from the log file and analyze specific queries in terms of how long each query took to run and how many checks were made in the process along with Legality Checks Profile statistics.

See Also

- LGL-113

LGL-115

(warning) App option place.legalize.enable_pin_color_alignment_check is set to false.

Description

enable_pin_color_alignment_check must be set to true while running AL, which enables legalizer to automatically align cell pin/shapes to track on the given metal layer.

What Next

Turn on the app option before running AL.

LGL-116

(warning) Track offset on layer %s is set incorrectly. One example library cell with shape to track mis-alignment: '%s'.

Description

Lib cells' pins are not center aligned with routing tracks on layer %s.

What Next

Set the following app options before running AL. 1) place.legalize.enable_pin_color_alignment_check to true to enable legalizer to automatically align cell pin/shapes to track on the given metal layer. 2) If above is already true, set place.legalize.disable_advanced_legalizer_rules -value {pg_drc} to bypass the issue from mis-aligned tracks if want to go with dirty design.

LGL-117

(Information) Setting orientation for the cell %s to R0.

Description

This message indicates that this cell has Invalid orientation which might cause problem during legalization.

Feedback

What Next

Check the library-cell and the floorplan to see why the cell has invalid orientation. If such cells are present in the design, run create_placement before legalizer.

LGL-118

(information) Enabling the app option place.legalize.enforce_1x_min_filler

Description

This message indicates that the design does not contain filler cells. As a result, it might cause long runtime or hang at the legalization or check_legality in TPO, VT, OD rules.

What Next

Please doube check the design and the libraries for filler cells.

LGL-119

(information) The bound %s of type %s has utilization > 100%. Hence leaving all the cells inside it unlegalized.

Description

This message indicates that this bound has very high utilization. Any bound with utilization this high cannot be legalized. It will take a lot of runtime and at the end leave cells unlegalized.

What Next

Increase the size of this bound or decrease the number of cells present in it.

LGL-120

(information) Trying to legalize the cell %s in this gap by disabling allowable orient.

Description

This message indicates that for this gap, this lib cell might not have sufficient allowable orientations. As a result of which, legalizer could not find a legal orientation for this gap.

What Next

Please double-check the design and library and make sure the there are asufficient allowable orientations for a given lib cell.

Feedback

LGL-121

(information) Bound has utilization > 120%. Recomputing total density by removing the placeable and total area of the bound.

Description

This messages indicates that the floorplan has utilization greater than 100%. There are bounds having density greater than 120% which might be causing high overall density. Therefore leaving those bounds unlegalized and removing their area from the total floorplan area.

What Next

Increase the total area of the bound or decrease its utilization.

LGL-122

(information) Enabling the app option %s locally.

Description

This messages indicates that the app option place.legalize.enable_cell_spreading and place.legalize.enable_cell_ordering should not be turned off during advanced legalizer.

What Next

Turn on the app options before running legalize_placement for advanced legalizer.

LGL-123

(error) Advanced Legalizer detects incorrect data input; legalization aborts

Description

This messages indicates that advanced legalizer fails to initialize engine because of incorrect data input.

What Next

Check the input data and run check_legalizer_sanity to get warnings related to incorrect data.

LGL-124

(error) Basic rule engine initialization fails

Feedback

Description

This message indicates that advanced legalizer failed to initialize basic rule engine because of incorrect data.

What Next

Check for incorrect data before running advanced legalizer.

LGL-125

(warning) Voltage area '%s' has an empty effective area but cells assigned.

Description

The given voltage area has no effective physical area but at least one cell is assigned to it. All cells assigned to such a voltage area cannot be legalized.

What Next

Correct the voltage area setup. Also check the stacking order which impacts the effective area of the voltage areas.

LGL-126

(error) The legalization cannot place the block because it has no placeable area.\n \tPlease remove some blockages from the design to be able to place cells.

Description

This message is indicating that the legalization has detected that there is no placeable area in this floor plan, so the legalization cannot produce a legal placement for your block.

What Next

Remove some bloackages from the block.

LGL-127

(information) Lib-cell '%s' is a user-defined filler cell.

Description

The given library cell is considered a filler cell due to app-option place.legalize.filler_lib_cells.

Feedback

LGL-128

(information) Via Ladder constraint %s failed to find solution due to PG shapes on layer %s.

Description

Tool could not find legal location for this via ladder constraint. The root cause is the PG layer report in the message.

What Next

Review the PG structure and via ladder constraint. Fix at least one of them to solve the problem.

LGL-129

(warning) Via Ladder check on libCell %s is ignored after failure threshold.

Description

Via ladder failure on libCell meet the threshold, so tool will ignore the libCell.

What Next

Review the PG structure and via ladder constraint.

LGL-130

(information) Legalizer threading is enabled with %s effort

Description

This is an informational message emitted during legalizer initialization reminding you that you requested the legalizer use threading.

See Also

- LGL-131

LGL-131

(information) Legalizer used up to %d thread%s

Description

This is an informational message emitted when the legalizer completes telling you the peak number of threads used for legalization.

Feedback

See Also

- LGL-130

LGL-132

(error) Initialization of the command failed.

Description

This message indicates that command failed because site def grids could not get initialised as part of Basic Rule Engine initialisation.

What Next

Check for incorrect site definitions.

LGL-133

(warning) This design has spacing rules applied on lib cells, causing over constraints. Spacing rule constraints have been relaxed.

Description

This message indicates that the design has spacing rules applied to lib cells. As a result, they are over constrained to be legalized. The spacing rule max constraints have been optimized according to thier utilizations.

What Next

Relax the applied spacing rules.

LGL-134

(warning) The library cell "%s" has implant layers missing in frame.

Description

This message indicates that the design has lib cells with no implant layer which can cause hang or long runtime.

What Next

Rectify the design by assigning the implant layers to the lib cell. Turn on the app option place.legalize.use_virtual_implant_layer.

Feedback

LGL-135

(warning) Using virtual implant layer for lib cell "%s" not having implant layer. Enabling the app option place.legalize.use_virtual_implant_layer locally.

Description

This message indicates that there were some lib cells that had no implant layer assigned to them. To avoid hang a virtual implant layer has been assigned to them.

What Next

Provide implant layer information for all such lib cells.

LGL-136

(warning) Design has high local density %s which may cause higher runtime.

Description

This message indicates that the design has high local density.

What Next

You may need to check your placement constraints.

LGL-137

(warning) Pre clumping of spare cells resulted in an increased density of %s.

Description

This message indicates that the design has high spare cell density.

What Next

You may need to check your placement constraints.

LGL-138

(warning) Missing fillers for %s layer.

No fillers found for the given layer. It can cause legalizer to hang.

What Next

Check the filler cells constraints on the cell lib.

Feedback

LGL-139

(warning) Duplicate color variant %s has been detected. This library cell will be ignored by the legalizer.

Multiple identical color variants make variant legalization useless because any variant swap attempted by Advanced Legalizer would still give the same result.

LGL-140

(warning) Lib-cell '%s' has %s '%s' which is not a multiple of the OD site %s '%s'. OD information will be ignored.

Description

The given library cell has a width or height which is not an integer multiple of the considered OD site map. The library cell will hence be ignored for any OD implant checks.

LGL-141

(warning) Via ladder constraint %s of lib cell %s is blocked by cell's internal objects, so the via ladder check on the cell instances derived from this lib cell with the given via ladder constraint is bypassed.

Description

You received this warning message because there exists a lib cell, denoted by $lc, other objects inside the lib cell generate DRC violation against the via ladder constraint and block via ladder insertion. Advanced legalizer will automatically bypass the via ladder checks on those cell instances of the lib cell $lc, and still perform via ladder checks on other normal cells if the app option place.legalize.enable_via_ladder_checks is enabled.

What Next

You can take one of the following actions to fix this warning. 1. Modify the mismatched via ladder constraints such that advanced legalizer can grow via ladders on pins without causing DRC violation against other objects inside cell. For example, decrease the number of cut rows/cuts per row. 2. Modify the cell layout by manually removing objects block via ladder construction.

LGL-142

(error) Cell '%s' has a height (%s) which is not a multiple of the associated site definition '%s' height (%s). Cell is skipped.

Feedback

Description

The height of the given cell is not a multiple of the height of the associated site defintion.

What Next

You need to regenerate the corresponding lib cell properly.

LGL-143

(error) No special cell has been specified.

Description

This message is indicating that there are no cells defined while setting special cell legalization constraints. Special cell legalization won't take place.

What Next

Correctly specify cells constraint.

LGL-144

(error) Both X max displacement and Y max displacement can't be zero simultaneously.

Description

No correct direction set for moving cells while setting special cell legalization constraints. Special cell legalization won't take place.

What Next

Correctly specify at least one of, X or Y direction displacement for special cell movement.

LGL-145

(Warning) Cell '%s' of ref '%s' does not have a site association compatible with floorplan. Cell cannot be snapped to row.

Description

Site information in the listed lib_cell is either missing or is not compatible with the site_def(s) of the site rows in the current design. Instance cannot be snapped to row for placement.

What Next

Check lib_cell properties.

Feedback

LGL-146

(Warning) Cell '%s' has an invalid orientation '%s'. The cell will be ignored.

Description

The given cell has an orientation which is either not defined or has a 90 degree rotation. Allowed orientations are R0, MX, R180, and MY.

What Next

Use the 'orientation' attribute to define a valid orientation on the cell.

LGL-147

(error) Options for report_special_cell_legalization : -cell = %s, -all = %s, -summary = %s.

Description

Not all options can be specified simultaneously for reporting special cell constraints. Specify only one. If none is provided, summary is printed.

What Next

Correctly specify report special cells constraint.

LGL-148

(error) None of the options for remove_special_cell_legalization have been set.

Description

Both the options (-cell and -all) can't be simultaneously set to false for removing special cell constraints. Specify at least one.

What Next

Correctly specify remove special cells constraint.

LGL-149

(warning) Site master "%s" has no Y-Symmetry. The "legal orientations" for the standard cells will be limited.

Feedback

Description

This message is indicating that the legalization has detected that the above site master has no Y-Symmetry. For a normal design, usually, the site master should have "Y-Symmetry".

If a site master does not have "Y-Symmetry", the standard cells will have limited legal orientations because the standard cells will not be allowed to flip within the site rows.

What Next

Please double-check the design and library setting and make sure the setting is correct.

LGL-150

(information) %s

Description

This message prints information about found lib cells and filler cells in the reference libraries.

LGL-151

(warning) Filler cell '%s' has no VT implant layer shapes.

Description

The given filler cell has no shapes on any implant layer. So this lib cell cannot be used for virtual filler insertion.

What Next

Make sure that the frame view has VT implant layer shapes.

LGL-155

(warning) Filler lib cell %s is set to dont_use and will be ignored during legalization.

Description

Fillers with dont_use attribute set to true will be ignored during legalization/check legality.

What Next

To use this filler lib cell, mark dont_use attribute to false.

Feedback

LGL-156

(warning) Design %s has no EM via ladders defined. Disabling via ladder related checks.

Description

No EM via ladder definitions have been found. Disabling the via ladder related rule checks for this design.

What Next

Enable Electromigration via ladder rule for the design.

LGL-157

(warning) Layer %s has no proper routing tracks.

Description

Tech layer should have routing tracks. No pins can be routed in this layer.

What Next

Repair this layer by adding routing tracks to it.

LGL-158

(warning) Layer '%s' not found.

Description

The layer whose debug parameters were passed by user is not available for this design.

What Next

Correct the layer name specification.

LGL-159

(warning) The available area of Voltage Area shapes%s '%s' is smaller than the cell area for cell '%s'. These shapes are ignored for legalization.

Description

This Voltage Area or Move Bound shape has area less than any cell that belong to this region. Hence this shape is ignored for any legalization.

Feedback

What Next

Increase the area of this shape.

LGL-160

(warning) Cannot enable fast_pg rule due to missing vertical M1 (mask metal2) layer.

Description

Since this design does not have vertical M1 layer, fast_pg rule cannot be enabled here.

What Next

Disable fast pg rule check

LGL-161

(warning) Cross row VT check is not supported for inbound (N12) designs.

Description

The Advanced Legalizer does not support cross row VT checks for inbound designs. Cross row VT checks are not performed.

What Next

Disable cross row VT checks

LGL-162

(warning) Reference %s pin %s does not have port_type attribute set.

Description

The pin does not have port type set. Hence it cannot be used in Advanced Legalizer.

What Next

Set the port type for this pin in the library cell.

LGL-163

(warning) Failed to find legal location for %s (%s) after %d trials.

Description

This cell has exceeded the maximum failed trials for any one cell to find legal location in Advanced Legalizer.

Feedback

What Next

Increase the max trials for legalizer by using the app option place.legalize.max_legality_failures.

LGL-164

(warning) After %d legalization trials, instance %s (%s) has the following legality failures:

Description

This message is printed for a cell after a given interval of legalization trials (default interval : 40000). This signifies that the cell has high failure rate.

What Next

There is a detailed tally of the number of failures for each rule after this message. Debug to find out reason for rule failures.

LGL-165

(information) Printing the legality failure profile for this legalization.

Description

This legality failure profile is printed when the app option place.legalize.profile_legality_failures is set to true. It prints the fail count for each rule in this legalize_placement run.

What Next

Check why these rules are failing and accordingly make changes in the design.

LGL-166

(warning) Unable to set layer shape mask fixed for cell '%s'.

Description

Failed to set layer shape mask fixed for the block instance in NDM.

LGL-167

(warning) Unable to set blockage mask fixed for cell '%s'.

Description

Failed to set blockage mask fixed for the block instance in NDM.

Feedback

LGL-168

(warning) Unable to save %s file %s.

Description

File could not be saved as number of report files already saved in this directory exceed 10000.

What Next

Cleanup the directory as the report exceeds limit.

LGL-169

(warning) %s than 2 spacing rule labels are found from %s, from line %d %s, %s.

Description

For any given spacing rule, only 2 labels are required. If there are more than 2 labels, only 2 are useful and if there are less than 2 labels, that spacing rule cannot be applied. Hence, the rule is ignored.

What Next

Redefine the spacing rules providing only 2 labels for each rule.

LGL-170

(warning) No rule engine found. Pin Access Optimization is not executed.

Description

Basic engine is not initialized for this design. Cannot execute Pin Access Optimization without basic engine.

What Next

Rerun the design with place.legalize.enable_early_data_support to check the reason for basic engine failure and rectify the design accordingly.

LGL-171

(warning) No base site definition found. Pin Access Optimization is not executed.

Feedback

Description

Basic site def is not set for this design. Pin Access Optimization cannot be executed without basic site def.

What Next

Rerun the design with place.legalize.enable_early_data_support to check the reason for no basic site def.

LGL-172

(warning) No grid found with non-zero width. Pin Access Optimization is not executed.

Description

This design does not have a grid with non-zero width. Pin Access Optimization cannot be executed without a non-zero width grid

---

LGL-173

(warning) Pin access %s encountered some internal issue. Reverting changes done by it.

Description

Failed to commit or uncommit a cell or move during pin access optimization. Restoring the cell placement to original state.

LGL-174

(information) Pin access %s used up to %d thread%s.

Description

This is an informational message emitted when the pin access optimization completes telling you the peak number of threads used for it.

LGL-175

(warning) No characterization data in memory. Will use default (method 0) for legalization library characterization.

Description

No characterization data found for legalization library characterization.

Feedback

LGL-176

(warning) There is no legality library to link to the existing legalizer.

Description

Legality library unavailable for the current legalizer.

What Next

Create a legality library for this legalizer.

LGL-177

(warning) Existing legality information is compiled from different %s.

Description

The current legality library compiled does not match the design or rule setting.

What Next

Recompile the legality library for this design and rule setting.

LGL-178

(warning) Resetting existing compiled legality information.

Description

The existing legality information is for different design or rule setting. Hence resetting it.

LGL-179

(warning) There %s %d NDM instance%s out of sync with ALMap's final state (existence %d; reference %d; origin %d; orient %d).

Description

There are instances that are not in sync with the final state after restoring states. There could be multiple reasons for sync failure like 1. Origin mismatch 2. Orient mismatch 3. Library cell mismatch 4. Cell deleted in Advanced Legalizer but not in NDM

LGL-180

(warning) Library cell %s fails compilation/processing. Skipping.

Feedback

Description

The library cell has failed processing or legality compilation because of any of the following reasons. 1. Library cell name not unique. A library cell with same name already exists with same name. 2. Library cell is not standard. 3. Legality file is unreadable.

LGL-181

(warning) Design %s has Short Pins. Advanced Legalizer automatically adjusts DRC rule sets.

Description

This design has short pins. Advanced Legalizer will automatically adjust DRC rules to support them.

LGL-182

(warning) Overwriting CTS spacing constraints (old x=%g y=%g) (new x=%g y=%g) for cell '%s (%s)'.

Description

Updating the CTS spacing contraints for this cell.

LGL-183

(warning) Site '%s' of cell '%s' has no grid width or grid height.

Description

This cell's site map is not initialized properly. Hence the cell cannot be placed anywhere.

What Next

Check the instance data carefully and run the design again.

LGL-184

(warning) Cannot place cell %s into %s %s.

Description

Cannot find site row in Move Bound or Voltage Area matching the site definition for this cell.

Feedback

LGL-185

(warning) Layer %s %s is not a 2 dimentional table. TF information will be ignored.

Description

This table is not a 2 dimentional table. Hence removing the information as it cannot be used.

What Next

Create a 2 dimentional table.

LGL-186

(warning) Cannot place cell %s because the design does not contain site rows with site definition %s.

Description

This cell cannot be placed as there are no site rows available for this site definition.

LGL-187

(warning) Layer has non-constant pitch at the track location %f.

Description

This layer has non constant pitch at the mentioned track location. But the pitches are integral multiple of each other. Choosing the smaller one.

LGL-188

(warning) Cannot find library cell %s in the 2D rule query system.

Description

The 2D query system does not have a library cell. Will not be able to process the VT type for this design.

LGL-189

(warning) Unable to process non-standard pin shapes of %s (%s).

Feedback

Description

Advanced Legalizer can only process pin shapes of type NDM_OBJ_TYPE_POLYGON and NDM_OBJ_TYPE_RECT. Any other pin shapes cannot be processed.

What Next

Only use pins with shapes NDM_OBJ_TYPE_POLYGON and NDM_OBJ_TYPE_RECT for this design.

LGL-190

(warning) Empty repelling bound for %s '%s' is ignored.

Description

Cannot build safety bounds as the repelling bound for heirarchy/group does not have any shapes.

LGL-191

(warning) Library cell %s of site definition %s contains no element site definition.

Description

Cannot build lib cell info for VT or OD rules for this library cell as it does not have an element site definition.

LGL-192

(warning) Library cell %s's %s %d is not an integral multiple of site %s %d.

Description

This library cell's width/height is not an integral multiple of the site width/height. Cannot build library cell information for VT and OD rules for this library cell.

LGL-193

(warning) Library cell %s of height %d is not an integral multiple of its element site definition %s of height %d.

Description

Cannot build library cell information for VT or OD rules as it's height is not an integral multiple of the element site definition's height.

Feedback

LGL-194

(warning) Cannot find%s pin %s from cell %s.

Description

Cannot process power grid blockage rules as the pin for this cell is missing.

LGL-195

(warning) Unable to legalize cell %s.

Description

The cell could not be legalized.

LGL-196

(warning) Library cell %s has no corresponding site definition.

Description

This library cell has no site definition. Hence it cannot be processed or used.

What Next

Define a site definition for this library cell and rerun the design.

LGL-197

(warning) Multiple site id alignment app options are set. Please check the flow used in below message and review app options setup.

Description

There is a problem with the app option set up as multiple site id allignment app options should be set. Site id should have a unique value set.

What Next

Set only one app option for site id allignment.

LGL-198

(warning) Invalid Site Id Alignment Flow. Please check the app options setup.

Feedback

Description

Site Id align should not have 1 set to it. This is invalid site id alignment flow.

LGL-199

(warning) The max number of variants within all cell groups is %d, but the site row cycle is set to %d at This may be design setup issue and may cause legalization failure. Please review cell groups and check design setup.

Description

The current design has a setup failure and can cause legalization failure. The max number of variants within all cell groups is not eqaul to site row cycle.

LGL-200

(warning) Variant Id/N-Variants Id alignment is enabled, but "place.legalize.enable_variant_aware" is disabled.

Description

The app option place.legalize.enable_variant_aware should be set if variant id allignment is enabled.

LGL-201

(warning) Illegal region filter option.

Description

The pin access region filter to be optimized is illegal.

LGL-202

(warning) Invalid %s in golden DRC marker file. Ignoring the file.

Description

Invalid syntax/bbox in the DRC marker file. This file cannot be used for processing the DRC regions. Hence ignoring this file.

LGL-203

(warning) Have tried %d filler combinations for the gap...

Feedback

Description

This message is printed after every 1000 legalizer trials of the filler combinations for the gap.

LGL-204

(warning) Site row not found at {%g %g}.

Description

No site row is present at the given coordinate. Hence cannot place the cell here.

LGL-205

(warning) Unable to fill gap at {%g %g}.

Description

Could not fill these gaps because of the following reasons: 1. Number of trials exceed the threshold trials. 2. Could not find an instance to fill the gap 3. Could not build a new instance with similar cell design as the gap

---

LGL-206

(warning) The app option %s is not set.

Description

The value of this app option returned is the default value.

What Next

Set the app option if required.

LGL-207

(warning) Via0 alignment rule will be ignored.

Description

The via0 allignment rule is ignored because of the following reasons: 1. The app option is not set. 2. Could not find the name of the via0 allignment grid specified by user.

What Next

Set the app option if not set already, and if the app option is set, pass the grid which exists in this design.

Feedback

LGL-208

(warning) Max %s inbound allignment rules/length checks will be ignored.

Description

The specified rules or checks have been ignored because of the app option not set.

LGL-209

(warning) There are no inbound cells in the design. CPOR7 rules will be ignored.

Description

CPOR7 rules cannot be checked without Inbound cells. This design does not have inbound cells.

LGL-210

(warning) %s tech layer was not found.

Description

Metal tech layer not found for this design. Fast PG engine and other PG related parameters will not be initialised and used in this flow.

LGL-211

(warning) Cell %s %sOrientation %d cannot be recognized in Cell Library DRC Soft Rule.

Description

In cell library DRC soft rule, the cell's orientation could not be recognized.

LGL-212

(warning) %s rule info has already been constructed, skipped...

Description

This engine's rule info has already been constructed. Skipping the initialization again.

LGL-213

(warning) Cannot find cell edge alignment grid named %s; cell edge alignment rule will be ignored.

Feedback

Description

Cell edge alignmnet rules are being ignored. Cell edge alignment grid names not found.

LGL-214

(warning) Issue found in calculating ML prediction accuracy. Skipping it.

Description

Could not calculate ML prediction accuracy.

LGL-215

(warning) Skipping ML prediction accuracy as zero floor area.

Description

Cannot calculate ML prediction accuracy as the floor area is zero.

LGL-216

(warning) Evaluation of command returned error code %d, command was %s.

Description

The command returned error with the given code.

LGL-217

(warning) Skipping route-aware pin-access check due to large displacement for inst: %s.

Description

The instance shows a large displacement. Hence skipping route aware pin access check for it.

LGL-218

(warning) Unknown 2D filler rule %s, will be ignored.

Description

This filler rule is not known to Advanced Legalizer, hence will be skipped.

Feedback

LGL-219

(warning) M0PO max length check will be skipped as %s.

Description

The M0PO max length check is skipped because of one of the following reasons: 1. There is no layer with mask name metal0 in the design. 2. M0 layer has no max length info in the tech file.

LGL-220

(error) 3D grid (%u, %u, %u) cannot connect to %s-layer grid due to %s %f".

Description

3D grid could not connect to upper/lower layer because of X/Y rule failure.

LGL-221

(error) 3D grid (%u, %u, %u) cannot connect to %s-layer grid due to wrong index (%d, %d, %u).

Description

Because of wrong index passed, the #D grid cannot connect to upper/lower layer.

LGL-222

(error) Layer %s not found %s.

Description

Could not find any layer in Advanced Legalizer to match the layer name given.

What Next

Please check the layer name passed.

LGL-223

(error) Library cell %s not found %s.

Description

Could not find a library cell with same name as this in the Advanced Legalizer.

Feedback

LGL-224

(error) Unable to obtain base site definition information.

Description

The base site definition information is missing. Legalizer will not function properly if base site definition is not set.

LGL-225

(error) Unable to extract horizontal legal pattern for the library cell %s.

Description

Cannot build legal pattern for this Advanced Legalizer as the tool could not extract the horizontal legal pattern for this given library cell.

LGL-226

(error) Base site def %s %s %g is not a multiple of grid %s %g.

Description

It might be an invalid legalizer design as base site def should always be an integral multiple of the grid width/height.

What Next

Rerun the design with place.legalize.enable_early_data_handling set to true to check if this design is valid or not. Can also use chck_legalizer_sanity command instead of legalize_placement.

LGL-227

(error) Cell %s has an invalid orientation %s.

Description

Cell does not have an orientation set or the orientation set is invalid for Advanced Legalizer. Cannot set keepout for this cell.

What Next

Set a valid orientation for this cell.

Feedback

LGL-228

(error) Cell Map initialization failed.

Description

Cell map could not be initialized properly because of basic engine failure.

LGL-229

(error) compile_legality failed.

Description

This command failed as either the pg_drc rules are not set or legal map initialization failed.

LGL-230

(error) Found a non-regular via color %d.

Description

The via color found is non regular.

LGL-231

(error) Found zero pitch %d.

Description

The layer has zero pitch.

LGL-232

(error) Unable to snap cell %s to row.

Description

The cell could not be snapped to row. Cannot continue legalization.

LGL-234

(error) Pin access %s detected incorrect data input. Aborting.

Feedback

Description

Pin access optimization or cell spreader were aborted because the engines could not be initialized properly. Some incorrect data has been passed in the design.

What Next

Check for reason of engine initialization failure and find out the incorrect data which led to failure.

LGL-235

(error) Could not find hybrid weight for cell '%s'.

Description

Could not get the hybrid weightage for this cell. Hence cannot perform hybrid spreading for the cell.

LGL-236

(error) Lib-cell '%s' is unplaceable. %d success after %d trials; passing rate %g.

Description

This lib-cell is unplaceable. After performing a lot of trials, the success rate or pass rate is very low. Cells of this lib-cell will remain unlegalized during this legalization run.

What Next

Run check_legality for cells of this lib-cell to get the rules which are failing for this cell.

LGL-237

(error) Tcl ""%s"" execution failed.

Description

Could not execute the tcl.

LGL-238

(error) Cell from cell map is NULL or invalid.

Description

Cell passed from cell map is either NULL or invalid. Could not obtain cell's block instance and hence invalid.

Feedback

LGL-239

(error) The via ladder %s has a locked/fixed shape %s. Ignore removing this via ladder.

Description

This via ladder will not be removed as it has locked or fixed shape.

LGL-240

(error) NYPD legalizer is not initialized.

Description

Advanced Legalizer(NYPD legalizer) has not been initialized yet. Rerun the flow after initializing NYPD legalizer object.

What Next

First initialize the NYPD legalizer before calling this functionality.

LGL-241

(error) Unable to uncommit cell %s.

Description

Could not uncommit cell for the current location. There could be different reasons for not being able to uncommit it depending on different rule engines. eg. another cell might be placed at the location where we trying to uncommit this cell.

LGL-242

(error) Found an MX_site cell %s not placed on an MX site %s.

Description

The cell cannot be placed at this site as the cell has MX orientation which does not match the site orientation. The cell will be legalized at another location which matches the orientation.

LGL-243

(error) App option place.legalize.enable_machine_learning is not turned on.

Feedback

Description

The app option place.legalize.enable_machine_learning needs to be set for the Advanced Legalizer to continue lib cell legality query.

What Next

Enable the app option place.legalize.enable_machine_learning and rerun the command.

LGL-244

(error) Got unknown option

Description

Passed an option that does not match the requirements/criterion of spacing rule/label definition.

What Next

Re define the spacing rule/label with proper options.

LGL-245

(error) Range %s

Description

While specifing the spacing rule, the range between labels should always be a non negative integer. Except for adjacent rows, that too only for horizontal spacing.

What Next

Re define the spacing rule, making sure the spacing range is a non negative integer.

LGL-246

(error) Range %s

Description

The given spacing range should be in range of the maximum spacing that can be used for Advanced Legalizer. If the range is specified in micron rather than site width, then it should be within maximum spacing * site width.

What Next

Redefine the spacing label considering the maximum constraints.

Feedback

LGL-247

(error) Range %s

Description

The spacing rule range specified in microns must always be a non-negative real number.

What Next

Redefine the spacing rule with proper range in micron.

LGL-248

(error) Got unknown command

Description

Unknown data passed to the spacing rule command. Could be: 1. Read string not required for the option. 2. Unknown option passed along with the command. 3. Unknown command called. 4. Unknown side passed.

What Next

Rerun teh script with appropriate data/commands.

LGL-249

(error) Cannot specify

Description

Out of vertical and horizontal, only one direction of spacing label can be specified in one command.

What Next

Redefine the spacing labels, such that there is different spacing label for horizontal and vertical spacing label.

LGL-250

(error) Neither -side nor -vertical_side is specified from line %d

Description

Cannot make the spacing labels and spacing rules till the sides are not specified.

Feedback

What Next

Redefine the spacing label with sides defined.

LGL-251

(error) The %s label

Description

Cannot define the spacing rules if the label is not defined.

What Next

Redefine the spacing labels.

LGL-252

(error) Label

Description

Labels have different polarity, i.e both labels should either be horizontal or should be vertical. Mismatch is not allowed.

What Next

Redefine the rule with labels having same polarity.

LGL-253

(error) -adjacent_row cannot be specified with -halo together, from line %d

Description

The two options -adjacent_row and -halo cannot be specified by the user together.

LGL-254

(error) Cannot open vertical spacing rule configuration file name

Description

Cannot load spacing rule information as the vertical spacing rule configuration files could not be opened.

Feedback

LGL-255

(error) LegalMap val %d at index %d,%d is not a valid cellId.

Description

The cell id value in legal map at the given index is not valid. Cannot check for overlap at this location.

LGL-256

(error) Range is not specified for line %d

Description

Cannot define a spacing rule without the range. Hence this spacing rule will be ignored.

What Next

Redefine the spacing rule with maximum and minimum spacing range.

LGL-257

(error) Unable to read boundary leakage side file.

Description

Boundary leakage details will not be available as the boundary leakage side file could not be read.

LGL-258

(error) Unable to commit ignoreCell %s %s %s.

Description

Unable to commit cell because of: 1. Region failure. 2. Rule failure.

LGL-259

(error) File '%s' is not of expected type.

Description

File type does not match the expected type.

Feedback

LGL-260

(error) Empty _rtLayers.

Description

Cannot build the via coloring map and tracks as the rt layers vector is empty.

LGL-261

(error) Unknown violation type. Violation rule = %s.

Description

This violation rule does not have any such violation type.

LGL-262

(error) 2D checker/legalizer does not support a site row (%s) whose width is not an even multiple of the grid width (%s).

Description

Any site row which has site width odd multiple of the grid width cannot be used in Advanced Legalizer. Cannot build basic engine with such site rows. Hence an invalid design.

What Next

Make sure the site row's width is an even multiple of the grid width.

LGL-263

(error) Unable to restore %s (ref %s) to original legal state %d (last state %d; engine %s) Cell siteMap %s Lib siteDef %s Cell origin %d %d orient %s libCell %s.

Description

Cannot restore the cell to the original legal state from the last state.

LGL-264

(error) Unable to read equiv lib cell file %s.

Description

The equivalent lib cell cannot be read.

Feedback

LGL-265

(error) Library cell %s's height is a not multiple of the site height.

Description

Cannot place a cell whose height is not an integral multiple of the base site height. There is no site row in this Advanced Legalizer where it can be placed.

What Next

Change the library cell's height to integra multiple of the base site height.

LGL-266

(error) Unable to run DRC prediction.

Description

Cannot run drc predictions

LGL-267

(error) Invalid DRC prediction model.

Description

The drc prediction model is not valid. Cannot continue drc predictions.

LGL-268

(error) No DRC error file.

Description

Could not find any DRC file.

LGL-269

(error) Illegal row height specified.

Description

Row height specified here is illegal. Cannot generate 2D multi height gaps.

Feedback

LGL-270

(error) Failed to generate new mask vec.

Description

Could not generate new mask vector.

LGL-271

(error) The app option place.legalize.max_horizontal_pin_density must be a set with pair of non-zero positive integers {%d %d}.

Description

The app option should get both the values for pin density, positive integral values. Cannot initialize horizontal pin density.

What Next

Re define the app option with proper values.

LGL-272

(error) Duplicated maximum cell group constraints in PRF & json_glc_lib_cell; following PRF constraints & skipping the other!!

Description

These constraints are already present in the PRF. Hence skipping it.

LGL-273

(error) No %s height filler library cells are specified to fill %s height gaps.

Description

Cannot insert filler full/half gaps as no full/half height filler library cells specified.

LGL-274

(error) Unable to legalize %s due to max displacement constraint (%gum > %gum).

Description

The cell is surpassing the maximum displacement constraints. Hence it cannot be legalized.

Feedback

LGL-275

(error) Unable to read cell library drc side file.

Description

Could not find data in the file passed for cell library dc side.

LGL-276

(error) Failed to insert BBox{ {%d, %d} {%d, %d} }, keyX = %d, keyY = %d, lay = %lu.

Description

Could not insert bbox.

LGL-277

(error) Failed to insert Obj(%s), keyX = %d, keyY = %d, lay = %lu.

Description

Failed to insert object.

LGL-278

(error) Failed to insert Mask(%d) of BBox{ {%d, %d} {%d, %d} }, keyX = %d, keyY = %d, lay = %lu.

Description

Failed to insert mask.

LGL-279

(error) The list of OD.S.17 forbidden spacing range {min, max} is empty. Ignore OD.S.17 checking.

Description

OD.S.17 spacing forbidden range is not found.

LGL-280

(error) Dynamic OD length constriants' techfields should be 0 or 5!!

Feedback

Description

The value of dynamic OD length constraints should either by 0 or 5. Any other value is invalid.

LGL-281

(error) Cannot find dummy cell for filler lib cell %s.

Description

No dummy cell has been created for this filler library cell.

LGL-282

(error) No basic site map is found.

Description

Basic site map not found for this Advanced Legalizer. Cannot continue with the design.

LGL-283

(error) The list of OD proximity values is empty. Ignore clock min jog check.

Description

Clock min jog check will be ignored as the OD proximity value list is empty.

LGL-284

(error) Error in processing place.legalize.VT_groups app options. Layer %s is not a valid layer for VT group.

Description

The app option cannot be processed as the value passed by the user is not valid for the VT group.

LGL-285

(error) VT group %s is not defined . %s.

Description

Cannot continue this check as the VT group is not defined.

Feedback

LGL-286

(error) Layer %s is not a valid implant layer.

Description

The specified layer is not an implant layer.

LGL-287

(error) PG blockage spec {%s} is not a valid specification (e.g. VR:name|LIBCELL:name layerName blockRate).

Description

The PG blockage specification is not valid. It should be of the format as shown.

LGL-288

(error) Unable to read via ladder analysis file vialadderAnalysisFile.

LGL-289

(error) Via ladder rule %s has unmatched pin region W x H = %d x %d!

Description

The pin region does not match the specification of the via ladder rule.

LGL-290

(error) Cannot restore %s to its original library cell %s.

Description

Could not commit the instance with swapped library cell.

LGL-291

(error) The PT-ECO link has already been initiated; must terminate it first.

Description

The PT ECO has already been initialized. To re initialize it, the already existing PT ECO has to be terminated.

Feedback

What Next

Terminate the already existing PT ECO.

LGL-292

(error) Trial placement must be {instance_name reference_name} list pair.

Description

The trial placement passed by the user should be a pair of two objects: instance name and reference name. Cannot execute trial placement for the passed list.

What Next

Pass the list according to the specified format.

LGL-293

(error) Unable to find 2D checker cell named %s.

Description

The PT ECO link cannot find any instance with same name in advanced legalizer.

LGL-294

(error) Unable to %s trial placement %s file %s.

Description

PT ECO link could not read/write the input/output file as the file name is not correct.

LGL-295

(error) Instance at (%f, %f) is not covered by valid routing tracks.

Description

No valid routing tracks are present at the given location. Hence the instance cannot be covered by the tracks.

LGL-296

(error) Instance %s is not covered by valid %s routing tracks.

Feedback

Description

No valid routing tracks are present at the location where this instance is placed. Hence it cannot be covered by the tracks.

LGL-297

(error) Wrong via %s.

Description

The via does not match the requirement.

LGL-298

(error) No bot pattern.

Description

No bot pattern.

LGL-299

(error) The PT-ECO link has not been initiated; %s.

Description

Cannot perform the operation as teh PT ECO link has not been initialized yet.

LGL-300

(error) Invalid sameColorCutCenterMinSpacing.

Description

Invalid spacing constraint.

LGL-301

(error) Cannot find sameColorCutCenterMinSpacigTbl in V1.

Description

The spacing table is not found for this Advanced Legalizer.

Feedback

LGL-302

(error) Invalid AON cells spec %s.

Description

The AON cell spec passed by user from the app option "place.legalize.AON_cell_placement_spec" has invalid data. There should be 3 tokens for every entry in the list.

LGL-303

(error) Unable to find %s %s from AON placement spec.

Description

The attribute passed in the AON placement spec is not present in the Advanced Legalizer.

What Next

Check the design for this attribute.

LGL-304

(error) Invalid AON cell pin keepout spec %s.

Description

The AON cell pin keepout spec passed by user from the app option "place.legalize.AON_pg_keepout_spec" has invalid data. There should be 3 tokens for every entry in the list

LGL-305

(error) Unable to find %s %s from AON cell pin keepout spec.

Description

The attribute passed in the AON placement spec is not present in the Advanced Legalizer.

What Next

Check the design for this attribute.

LGL-306

(error) Metal/via tech layer was not found.

Feedback

Description

No metal or tech layer found. The LA rules engine cannot be initialized.

LGL-307

(error) Movable region size should be -1 or positive values, but its current value: %d.

Description

The movable region size should either be -1 or some positive value. It is currently set to 0, which is not a valid movable region size.

LGL-308

(error) For the id (%d), cross cell subnet is out of range.

Description

The value of cross cell subnet is out of range for this id.

LGL-309

(error) Cannot find library cell info for cell %s.

Description

The LA info map does not contain any library cell info for the given cell.

LGL-310

(error) Tech layer has no minimum width information.

Description

This tech layer does not have a minimum width information. Using default value for this tech layer.

LGL-311

(error) Layer's minimum widths from the tech file are not correct.

Description

The tech file does not have valid minimum width for the layers.

Feedback

LGL-312

(error) Boundary values are not set in getSpecificBox function.

Description

The boundary values should be set for specific box. Asserting.

LGL-313

(error) 3D layer %u has ZERO grid size: %lu x %lu, rt_pin_access is not enabled!

Description

Rt pin access is not enabled as the 3D layer has zero grid size.

LGL-314

(error) Pin layer has no upper grid connection at (%u, %u).

Description

The pin layer should have an upper grid connection at the given coordinates.

LGL-315

(error) 3D grid connection failed (broken num: %d).

Description

The connection for 3D grid failed.

LGL-316

(error) Unable to compile the library cell %s.

Description

The legality compiler could not compile the given library cell because: 1. It could not read the legality file. 2. Could not find site map for this library cell.

LGL-317

(error) Unable to write legality compile file %s.

Feedback

Description

Could not write legality compile file because either the pg_drc data was missing or the file name was incorrect.

LGL-318

(error) There is no legality compilation information.

Description

The legality compilation information is missing.

LGL-319

(error) Unable to read legality library file %s.

Description

The legality compiler cannot read library file because either the file name is wrong.

LGL-320

(error) PG data changed since library %s. Need to regenerate library compiler file.

Description

The data saved previously has changed. The library compiler file needs to regenerated.

LGL-321

(error) Fail to open PURE %s file: %s.

Description

Could not open the file.

LGL-322

(error) Syntax is wrong in %s layers in PURE!!!

Description

Wrong syntax for the specified layer.

Feedback

LGL-323

(error) Order of %s %d is incorrect.

Description

Order of the id is not valid for the shape/pattern.

LGL-324

(error) Too many features > 100.

Description

Features should not exceed 100.

LGL-325

(error) Layer name: %s has no mapping layer number.

Description

The layer number passed from the file has no layer number. Cannot process this layer.

LGL-326

(error) No %s in pattern, patID = %d.

Description

No layer/box in the specified pattern.

LGL-327

(error) NO layers in PURE!!!

Description

No layers found from the user passed file.

LGL-328

(error) Orientation %s is not supported in PURE!

Description

This orientation is not supported in the flip graph. Only MX, MY and R180 are allowed.

Feedback

LGL-329

(error) Cannot initialize graph with no layers!!!!

Description

There are no layers present, hence cannot initialize the pattern graph.

LGL-330

(error) Illegal pattern index %d to add violation box!!!!

Description

Cannot add violation box this pattern index.

LGL-331

(error) No box id in pattern graph!!!

Description

The pattern graph has no box.

LGL-332

(error) This pattern is not implemented yet...

Description

The specified pattern is not specified yet. Cannot continue.

LGL-333

(error) The layer %d is not defined yet.

Description

The specified layer has not been defined yet.

LGL-334

(error) ShapeBBox is not covered by patBBox. Please modify patBBox %s to cover %s.

Description

The pattern bbox should cover the shape bbox. Modify the pattern bbox to cover it.

Feedback

LGL-335

(error) There is no site def defined for the block.

Description

This block does not have any site def defined. Advanced Legalizer cannot function for such block.

LGL-336

(information) Adjusting %s to a multi-height library cell.

Description

The height of this library cell is more than equal the base site height. So marking this library cell as multi height.

LGL-337

(warning) No cells selected for IR-drop optimization.

Description

There are no cells for IR drop optimization.

LGL-338

(error) Cannot get value for max group length from library '%s'.

Description

The library has no value for max group length.

LGL-339

(warning) CPODE Layer %s has no corresponding tech layer.

Description

There is no tech layer for the CPODE layer obtained from the tech file.

LGL-340

(warning) The max length of rule max_cpode_length is not specified by app option max_vertical_stacked_length.

Feedback

Description

Cannot initialize CPODE rules as the app option place.legalize.max_vertical_stacked_length does not specify the max length of max_cpode_length.

LGL-341

(warning) The max length of rule max_cpode_length is not positive from tech file, so cpode check will be ignored.

Description

The value of max cpode length specified from tech file is not positive. Cpode rule check will be ignored.

LGL-342

(warning) Max parallel run spacing %g is less than the site width %g.

Description

Max parallel run spacing should not be less than the site width.

LGL-343

(warning) AL should get a hybrid filler at {%g %g}, but got another cell instead (cell = %s, lib = %s, orient = %s, bbox = {{%g %g} {%g %g}}), indicating this cell might not be on site.

Description

At the given location, there should be a hybrid filler but there is another instance placed here. This should be resolved before filler insertion.

LGL-344

(warning) User rule %s will be overidden.

Description

This user rule has been overidden.

LGL-345

(warning) Repeated layers during graph construction!

Feedback

Description

The layer has already been included in the pattern graph.

LGL-346

(warning) Anchor Point is invalid; it should be located at a shape's corner.

Description

The anchor point should always be present at the corner of the shape. This point is invalid.

LGL-347

(warning) Misaligned gap found; offending cell is %s ref %s origin {%g %g}, gapX1IndexU %d gapX2IndexU %d gapYIndexU %d gapX1IndexL %d gapX2IndexL %d gapYIndexL %d.

Description

The found gap is misaligned.

LGL-348

(warning) Could not find nypdLibCell for VL excluded libCell %s.

Description

No nypdLibCell found in Advanced Legalizer with same name as the given VL excluded library cell.

LGL-349

(warning) %d out of %d fixed cells need TPT recoloring!

Description

Out of the total fixed cells, these many cells need TPT recoloring.

LGL-350

(warning) There are %d fixed cells w/ TPT coloring violations.

Description

These many fixed cells show TPT colouring violations.

Feedback

LGL-351

(warning) More than 2 values in the list of OD.S.17 forbidden spacing range {min, max} are found. Only the first 2 values will be used.

Description

Only two values should be passes along the OD.S.17 spacing range. The user has passed more than two values so only first two will be used.

LGL-352

(warning) There are hybrid fillers in the filler library but the app option "%s" %s. Otherwise, hybrid fillers would be treated as normal fillers, resulting in jog violations.

Description

Hybrid filler are present in the filler library, but because of this app option, these hybrid fillers would be treated as normal fillers.

LGL-353

(warning) There is no special filler in the filler library but the app option "place.legalize.enable_1cpp_filler_rule_check" is enabled. Thus, the boundary transition rule check is "automatically" disabled, so that only filler1 and filler1 abutment rule is considered.

Description

Only the above specified rules are enabled as there are no special fillers, and this app option is enabled.

LGL-354

(warning) No instance in the design or No POD in library cells!!

Description

No POD in the library cells.

LGL-355

(warning) More than 2 proximity values in the list are found. Only the first 2 values will be used.

Feedback

Description

Only two values should be present in the list. Only first two proximity values will be used.

LGL-356

(warning) Select %d as major POD!

Description

Select major POD value as the one specified.

LGL-357

(warning) Improper setting of minWidth uJog = %d (%g um) > lJog = %d (%g um). Should set to equal.

Description

Improper setting of minWidth Jog. Will be set to eqaul.

LGL-358

(warning) Improper setting of min 1-fin diffusion length = %d (%g um) > lJog = %d (%g um). Should set to equal.

Description

The setting for min 1 fin diffusion length is not correct. Should be set to equal.

LGL-359

(warning) No OD related tech field was set. AL will automatically omit OD checking.

Description

Advanced Legalizer will skip OD rules checking as the OD related fields are not set.

LGL-360

(warning) No LUP shape of name =

Description

There is no LUP shape on the layout with the name as this.

Feedback

LGL-361

(warning) Additional power management user lib type name

Description

This lib type has already been registered in the Advanced Legalizer. Hence this will be skipped.

LGL-362

(warning) Additional power management lib type name

Description

This librry type is not present in the Advanced Legalizer. Hence the lib cell list will be ignored.

LGL-363

(warning) A tap uncover violation at {{%g %g} {%g %g}} is suppressed due to %s.

Description

The violation has been suppressed becuase of the following reasons: 1. The app option place.legalize.suppress_bndry_cover_violation. 2. Drop edge with given bbox.

LGL-364

(warning) The user tap rule table

Description

The table is empty or invalid. Hence the user tap rule will be ignored.

LGL-365

(warning) The user tap rule table one but an odd number of numbers, so the last number will be ignored.

Description

The number of values in the tap rule table should have even number ov values. If the number of values passed by user is odd,we will ignore the last value.

Feedback

LGL-366

(warning) Additional power management lib-cell name

Description

The library cell passed by the user through app option is not found in the cell library for this Advamced Legalizer.

LGL-367

(warning) Tap cover distance in site %d is too much, should be less than %d.

Description

The tap cover distance is very high.

LGL-368

(warning) No rule is specified. Please set rules via "set_tap_boundary_wall_cell_rules" before checking.

Description

There are no rules specified for checking the chip finishing. The rule set_tap_boundary_wall_cell_rules should be set before checking for rules.

LGL-369

(warning) Tap distance is not a positive number. Please check the rule setting by "set_tap_boundary_wall_cell_rules".

Description

Tap distance should always be a positive number.

LGL-370

(warning) The tap coverage distance is not defined in either rule container or app option (place.legalize.tap_cover_distance <micron>). The tap coverage checking might fail.

Description

The tap coverge might fail as the tap coverage is not defined.

Feedback

LGL-371

(warning) Failed to uncommit cell '%s'.

Description

Advanced Legalizer could not uncommit this cell.

LGL-372

(warning) Characterization data for library cell '%s' not found.

Description

No information found for this library cell in Advanced Legalizer.

LGL-373

(warning) Unable to find characterized lib-pin shape %s. Cell: %s pin: %s.

Description

Could not find characterization data for library pin shape.

LGL-374

(warning) Illegal access point at %s for shape %s.

Description

There is no access point for this shape at the given coordinates.

LGL-375

(warning) No site definition found. Unable to extract local connectivity.

Description

Could not extract local connectivity as there is no site definition for this pin access optimizer.

LGL-376

(warning) Duplicate cell found in move set. Aborting move.

Feedback

Description

Cannot normalize cells as a duplicate cell os found in the move set.

LGL-377

(warning) Debug options are defined.

Description

Debug options are defined by debug app option.

LGL-378

(warning) Failed to read value '%s' for option '%s'.

Description

Could not read values for the given option.

LGL-379

(warning) Couldn't find option '%s'.

Description

The given debug option in the app option value is not defined.

LGL-380

(error) User Rule JSON BBox has no complete L B T R values.

Description

Update the JSON bbox for complete information.

LGL-381

(error) Syntax is not correct for User Rule JSON: (name, value)=(%s, %s).

Description

No data passed for either name or value of the user rule JSON.

Feedback

LGL-382

(error) User Rule mode %s is not defined.

Description

Mode for this user rule is not defined.

LGL-383

(error) User Rule feature %s is not defined.

Description

Feature for this user rule is not defined.

LGL-384

(error) User Rule JSON BBox has no layers.

Description

No layers defined for the user rule JSON BBox.

LGL-385

(error) Unknown syntax!!!

Description

Cannot extract user rule information from JSON as the syntax is not correct.

LGL-386

(error) Syntax wrong for inputFileName: %s.

Description

Cannot read the data from file as the file name is not correct.

LGL-387

(error) ShapeOrient only support 1 orient.

Description

Syntax error in the shape orient. Only 1 orient is supported.

Feedback

LGL-388

(error) Syntax not correct at the line %s.

Description

The syntax at this line does not match the required syntax, hence closing the file without reading data.

LGL-389

(warning) Want to get a non-initialized flipped graph.

Description

The user wants to get non initialized flipped graph.

LGL-390

(warning) Gui is not running.

Description

Could not highlight the bbox as the gui is not running. Run the gui before executing this command.

LGL-391

(warning) No cells to be legalized/checked in %s.

Description

This VA or MB does not have any movable cell to legalize or check.

LGL-392

(warning) Removing the cell %s as it belongs to high local density area.

Description

The design has high local density which may lead to high runtime. So removing the cells in the high local density area to ensure reduced runtime. The area occupied by these cells will be replaced by a blockage and the design remains unlegalized.

What Next

Decrease local density for the mentioned location and rerun AL.

Feedback

LGL-393

(warning) Library cell %s has a VT layer %s (%d) that does not exist in Tech File.

Description

The layer number for this library cell does not match in the tech file.

LGL-394

(warning) Invalid value of vertical abutment. Insert spaces between values for valid input.

Description

The value of vertical abutment input by user is invalid. The vaue exceeds the maximum possible value. Insert space between abutment values to ensure correct input.

LGL-396

(information) Removing unfixed physical only cell %s.

Description

Removing the unfixed physical only cells as the app option place.legalize.exclude_unfixed_physical_only_cells is enabled.

LGL-397

(Warning) No site rows found in floorplan.

Description

This message is indicating that there was an error when analyzing site row configuration in current block.

What Next

Review the design and floorplan preparation.

LGL-398

(Error) Site row header %s has missing site definition.

Description

The specified site row header has missing site definition. Such designs with missing site definition are not valid for legalize_placement and check_legalizer_sanity.

What Next

Define a site definition for the site row header.

LGL-399

(Warning) Option design.sort_em_via_ladders is enabled. The priority of EM via ladder constraints on cell pin is modified.

Description

This warning message is to remind user the priority of EM via ladder constraints on cell pin is modified. Tool would try to preserve more routing resource for EM via ladder insertion during legalize_placement. It is expected to see larger cell displacement or longer runtime.

What Next

If you observe any unexpected cell displacement or runtime increase, please turn off app_option design.sort_em_via_ladders so that the tool would honor the original EM via ladder constraint priority.

LGL-400

(Warning) App option place.legalize.enable_early_data_support is set to true. Early data handling is enabled for Advanced Legalizer.

Description

The app option when set to true, detects and handles dirty input. It may lead to bailing out of legalizer at an early stage leading to unlegalized instances and could also involve making changes in the design to prevent any crash, hang or long runtime condition that may occur because of the dirty data input.

What Next

Check for early data warning and error messages in the log if any and make changes in the input accordingly.

LGL-401

(Error) No mask shift layer definition in Cell %s NDM %s.

There is a conflict in the setting of color-shifting flow between the app option value and the library cell attribute. Color-shifting flow would not be performed. Please reexamine your app option setting regarding color-shifting flow and the attribute of the library cell.

Feedback

What Next

Revise the aforementioned app option settings or reassign the attributes for the library cells.

LGL-402

(error) Found MX_site cell %s not placed on MX site %s origin {%g %g} orient %s.

Description

This message is indicating that MX_site cell not placed correctly on MX site.

What Next

Run command legalize_placement.

LGL-403

(Warning) All non-default voltage areas are ignored due to app option 'place.legalize.ignore_voltage_areas'.

Description

This message is indicating that the app option 'place.legalize.ignore_voltage_areas' has been turned on and all non-default voltage areas are ignored during legalization and check_legality. Even if cells are not assigned to a specific voltage area, they can be placed within a non-default voltage area.

LGL-404

(Warning) auto_stagger is enabled in router for via ladder, but it is not enabled in legalizer.

Description

route.auto_via_ladder.auto_stagger is enabled, but place.legalize.via_ladder_auto_stagger is not enabled.

What Next

The suggestion is to set the two options consistently.

LGL-405

(Warning)

Feedback

Description

place.legalize.user_route_via_pillar_map is an obsolete app option that is no longer needed. This app option will be removed in the next release. Please remove this setting before the next release.

What Next

The suggestion is to remove the usage of app option place.legalize.user_route_via_pillar_map

---

LGL-406

(Warning) Single height rectilinear lib-cell '%s' found. This lib-cell is considered as a rectangular cell.

Description

This message is indicating that there is a setup issue regarding the site definition of a rectilinear cell. Rectilinear cells need to be multi-height with respect to its sitedef.

What Next

Review the sitedef setup.

LGL-407

(Warning) Not a recommended usage for color-shifting: app option place.legalize.%s and cell %s attribute %s. Use app option definition.

There is a conflict in the setting of color-shifting flow between the app option value and the library cell attribute. Color-shifting flow would adopt the app option setting regardless of the attributes from the library cell. Please reexamine your app option setting regarding color-shifting flow and the attribute of the library cell.

What Next

Revise the aforementioned app option settings or reassign the attributes for the library cells.

LGL-408

(Error) Inconsistent between app option %s and cell %s NDM %s.

There is a conflict in the setting of color-shifting flow between the app option value and the library cell attribute. Color-shifting flow would not be performed. Please reexamine your app option setting regarding color-shifting flow and the attribute of the library cell.

Feedback

What Next

Revise the aforementioned app option settings or reassign the attributes for the library cells.

LGL-409

(Warning) No mask shift layer definition in Cell %s NDM %s, use app option definition.

There is a conflict in the setting of color-shifting flow between the app option value and the library cell attribute. Color-shifting flow would not be performed. Please reexamine your app option setting regarding color-shifting flow and the attribute of the library cell.

What Next

Revise the aforementioned app option settings or reassign the attributes for the library cells.

LGL-410

(warning) For cpode_spacing in AL, could not open the side file %s.

Description

Users need to define side file for cpode_spacing.

What Next

Please set the app_option place.legalize.cpode_spacing_side_file. You can set it to the directory name or use this format<dir>/*.txt.

LGL-411

(warning) For cpode_spacing in AL, there's missing information for cpode soft placement constraints. Need to specify target cells, attacking types and two kinds of keepout distance \n

Description

Users need to set all four app_options related to cpode_spacing.

What Next

Please check if all app_options are set correctly:
place.legalize.cpode_soft_placement_constraint_attacking_types
place.legalize.cpode_soft_placement_constraint_target_cells
place.legalize.cpode_soft_placement_constraint_target_cell_keepout_distance
place.legalize.cpode_soft_placement_constraint_attacking_cell_keepout_distance

Feedback

LGL-412

(warning) For cpode_spacing in AL, the list number of target cells, attacking types and keepout distance do not match.

Description

Users need to define same types of target cells, attacking types and corresponding keepout distance.

What Next

Please check if the type number in app_options are same:
place.legalize.cpode_soft_placement_constraint_attacking_types
place.legalize.cpode_soft_placement_constraint_target_cells
place.legalize.cpode_soft_placement_constraint_target_cell_keepout_distance
place.legalize.cpode_soft_placement_constraint_attacking_cell_keepout_distance

LGL-413

(warning) For cpode_spacing in AL, unable to find user defined group name %s in target cells and attacking types.

Description

The group name in cpode_spacing app_options do not match.

What Next

Please check if group name in app_options are set correctly:
place.legalize.cpode_soft_placement_constraint_attacking_types
place.legalize.cpode_soft_placement_constraint_target_cells
place.legalize.cpode_soft_placement_constraint_target_cell_keepout_distance
place.legalize.cpode_soft_placement_constraint_attacking_cell_keepout_distance

LGL-414

(information) Found redundancy group '%s'.

Description

Prints the names of the safety register redundancy groups that are considered by legalization.

LGL-415

(information) Found safety_error_code_group '%s'.

Feedback

Description

Prints the names of the safety error-code groups that are considered by legalization.

LGL-416

(information) Found failsafe_fsm_group '%s'.

Description

Prints the names of the safety fail-safe groups that are considered by legalization.

LGL-417

(information) Vertical abutment prohibit pattern %d-%d accepted.

Description

Prints the pattern pairs of prohibited vertical abutments of std cells. The legalizer will consider these patterns as a hard placement rule and avoids vertical abutment of std cells with these given patterns.

LGL-418

(information) Reducing rule set for cell '%s'.

Description

In early data mode when the strategy is set to limit_legalize for the zero-pass-rate legalization check, the legalizer will reduce the rule set to overlap-free and cell-on-site. This message indicates which cells are affected by this rule set reduction.

LGL-419

(information) Pass-rate based cell priority: %s.

Description

This is a debug message for lib-cell pass-rate based cell priority definition.

LGL-420

(Error) CTS is trying to legalize %u unplaced cell%s.

This error message indicates a flow problem during CTS. CTS should never try to legalize cells without a placed location.

Feedback

LGL-421

(warning) App option '%s' is enabled.

Description

This messages indicates that the given app option is enabled which might have a negative impact on the legalization result.

What Next

Check whether this setting is required.

LGL-422

(information) Short variant '%s' is wider than the M1 PG pitch. This lib-cell is allowed to be placed under M1 PG shapes.

When the app options place.legalize.avoid_wide_variants and place.legalize.limit_wide_variants are turned on, wide variants (in X direction) are only allowed to be placed under M1 PG shapes. The shorter varaints are not allowed to be placed under PG shapes. However, if the M1 PG pitch is smaller than the width of the shorter variant(s), then an exception applies and the shorter variants are allowed to straddle the PG shapes.

What Next

None

LGL-430

(Warning) Couldn't find secondary PG %s at location (%g, %g) in %d sites, for AON cell %s. Will ignore aon_under_pg on the cell in legalization to avoid large displacement.

Description

It's a sanity check for AON cells to avoid missing PG around it. Will ignore aon_under_pg rule on the cell in legalization.

LGL-431

(Error) Missing PG for more than %d AON cells. Please check if there is a region without AON PG stripe.

Feedback

Description

It's a sanity check for AON cells to avoid missing PG around it. If the number of cells who found missing PG around it exceeds the value of place.legalize.limit_aon_cells_missing_2nd_pg, this error is repored.

LGL-460

(Warning) Lib cell %s does not have any primary PG pin.

Description

This message indicates that this lib cell does not have PG pins with necessary attribute "pg_type == primary". It could lead to false track capacity violation on multi-height cells.

What Next

Please double-check the design and library and make sure all lib cells have necessary primary PG pins.

LGL-461

(Error) Legalizer encounter internal memory error... %s : %s.

Description

This message indicates that during legalization, some internal memory error related to the indicated object(s)/condition(s).

What Next

Follow message suggestion to remedy the issue if any. Run check_database before saving/continuing design and report this to Synopsys.

LGL-462

(Error) Legalizer exceed max allowed internal memory errors.

Description

This message indicates that during legalization,more than the number of allowed internal memory errors happened and therefore command exits

What Next

Look for earlier error messages to remedy the issue if possible. Run check_database before saving/continuing design and report this to Synopsys.

Feedback

LGL-463

(Warning) site '%s' polarity undetermined.

Description

You received this message because the named site polarity has not been determined.

What Next

Please file a bug report.

LGL-464

(warning) There are %n non-default %sLegalizer/Chip-Finishing app-options in use.

The design has non-default legalizer/chip-finishing app_options, which may lead to unexpected behavior.

What Next

Cross-check non-default place.legalize.* and chipfinishing.* app_options, and please check with CAE on hidden non-default settings being used.

LGL-465

(warning) The specified region is too big; it is more than %.2f percent of core area.

The region provided by cellmap client is too big, which can lead to long-runtime issue.

What Next

Ask the client to review the usage of the region-based APIs from the stack trace below the message.

LGL-466

(information) cellmap bailed out after %n trials.

We have a trial limit from cellmap runtime improvement for non-region-based cellmap query/commit.

What Next

Please use a region-based cellmap API if a far-away legal location is acceptable.

Feedback

LGL-467

(warning) CLO_ERR: LocalOTF for this thread does not exist!!!

The client did not setup CLO or ALMap to use in lock-free mode during multi-threading

What Next

Open a bug so that this can be addressed

LGL-468

(Warning) via %s doesn't have lower metal layer.

This message indicate that via doesn't have connected lower metal layer.

What Next

Please check via has associated upper and lower metal layer.

LGL-470

(information) Adding AON placement spec: %s

An AON placement specification is added as a legalization constraint

What Next

None

LGL-471

(Error) Cell %s has ndm-cm mismatch. %s

Description

This message indicates that there is inconsistency between NDM and CM in terms of the cell and describes its details.

What Next

None

LGL-472

(Error) Cell %s has no ref block, but it was loaded into cellmap

Feedback

Description

The cell was loaded into cellmap, but it has no reference block.

What Next

None

LGL-473

(info) %s

Description

The message prints summary of NDM and cellmap consistency check

What Next

None

LGL-474

(warning) In vertical abutment rule specification, the portion of pattern exceeding the width of cell %s must be an even number. Pattern %s is ignored.

Description

While specifying the vertical abutment rule, if the pattern length is larger than the cell site width, the portion exceeding the cell width must be an even number.

What Next

Re define the vertical abutment rule.

LGL-475

(Warning) AL-Cellmap cannot commit app_fixed cell %s (lib %s) at %s %s, which could lead to cell overlaps after the flow.

AL-Cellmap expects no overlaps between app_fixed cells in the incoming database; otherwise, cell overlaps after AL-Cellmap are expected. To fix the error, please ensure all app_fixed cells are legal before running the flow.

What Next

To detect all violating app_fixed cells, please enable the app_option "place.legalize.enable_check_legality_before_and_after_cellmap". Clean up all violations and rerun the flow to see the cell overlapping issue is resolved.

Feedback

LGL-476

(Warning) A large %d-row-height cell %s (Lib %s) is detected in CLO, which may cause long runtime to find a legal location.

When CLO legalizes a big cell, typically it leads to long runtime.

What Next

If there is a freezing issue, please add dont_use on the big Lib cell(s).

LGL-477

(Warning) app option place.legalize.v0vt_layer_abutment_edge_distance will be deprecated in the future release. Please use place.legalize.v0_layer_abutment_edge_distance, place.legalize.v1_layer_abutment_edge_distance, and place.legalize.vt_layer_abutment_edge_distance instead

Description

place.legalize.user_route_via_pillar_map is an obsolete app option that is no longer needed. This app option will be removed in the next release. Please remove this setting before the next release.

What Next

Please replace it with suggested app option instead

LGL-478

(warning) lib-pin %s at (%s) has %s access points, but the Via ladder constraint %s needs %s access points, this Via ladder constraint is infeasible at current location.

Description

You received this warning message since this lib pin $lp at current location is not able to grow a via ladder on it based on the given via ladder constraint, because advanced legalizer does NOT support automatically pin extension.

What Next

You can take one of the following actions to fix this warning. 1. Modify the mismatched via ladder constraints such that advanced legalizer can grow via ladders on pins without pin extension. For example, decrease the number of cut rows/cuts per row. 2. Modify the cell layout by manually extending the short pins. 3. If you want to bypass this via ladder constraint, please enable place.legalize.enable_via_ladder_early_data_support. Tool will

Feedback

automatically bypass the via ladder checks on those cell instances of the lib cell $lc, and still perform via ladder checks on other normal cells (see LGL-090).

LGL-479

(warning) Instance %s has infeasible bound constraint. Ignoring repelling group bound/ safety core group %s for this instance.

Description

This message indicate instance has move bound or voltage area constraint but there is no intersection area or intersection area is smaller then instance with repelling group bound or safety core group. This instance will ignore repelling group bound/safety core group and will honor move bound/voltage area.

What Next

Change instance's move bound/voltage area or change repelling group bound/safety core group constraint which can be intersect and intersect area is bigger then instance's size.

LGL-480

(Warning) Detected lib cells with no implant layer shapes. Please check the lib cells to see if need to use virtual implant. If user want to use virtual implant, please enable related app options. (place.legalize.use_virtual_implant_layer and set up place.legalize.virtual_implant_layer_min_width)

Description

This Lib cell doesn't have implant. Please check the lib cell to see if need to use virtual implant.

What Next

Check the libcell to see if need to use virtual implant.

LGL-481

(Warning) Detected lib cells: %s (layer %s) with colorless pins/shapes.

Description

This Lib cell has colorless pins/shapes but it also has colored pins/shapes. Please use place.legalize.enable_check_uncolored_shapes_in_libcell to check this.

What Next

Check the mask attribute of the colorless pins/shapes.

Feedback

LGL-482

(Warning) User enabled place.legalize.enable_gui_drc_error_status_support. It will be on by default in future release.

Description

place.legalize.enable_gui_drc_error_status_support enables DRC violation marked as error in GUI error browser.

What Next

App option "place.legalize.enable_gui_drc_error_status_support" will be on by default

LIB

LIB-001

(error) Current library is not defined.

Description

The current library is not defined. Some commands require that the current library is set.

What Next

You must open or create a library and set current library with the current_lib command

LIB-002

(error) Empty reference library path.

Description

A reference library path was blank or an empty string.

What Next

Check that the given reference library path has a value that can be found on the search_path.

LIB-003

(error) Reference library name %s in library path %s has the same name as path %s.

Feedback

Description

The library name is the last part of each reference library path. Each reference library path in a reference library list must have a unique library name.

What Next

Check the list of reference library paths for libraries that end in the same name. Each library name must be unique. Libraries ending in the same name must be renamed. Once the library with the duplicate name has been renamed, the library may be added to the reference library path list.

LIB-004

(error) Cannot find reference library path %s.

Description

The reference library given in the -before or -remove argument cannot be found in this library's reference library path list.

What Next

Check the ref_libs in the library with the get_attribute command or the report_ref_libs command. Use either the library name (the last part of the path), the reference library path, or the full path name to that library for the set_ref_libs command's -before or -remove argument.

LIB-005

(error) Library name cannot contain ":", "|", or white spaces.

Description

The ':' and '|' character is used to delimit library and design names. It cannot be used for library name.

LIB-006

(error) Library '%s' already exists

Description

This error message occurs because a library of the specified name already exists.

Feedback

What Next

Use another name for the new library or remove the library from the file system and rerun the command.

LIB-007

(error) Cannot load technology file '%s'.

Description

The specified technology file cannot be loaded.

When using read_tech_file xxx.tf -merge 1) If the merge tech option is opened but current tech is none, we can not load technology file. 2) If merged tech file (xxx.tf) is invalid, we can not load tech file.

What Next

Make sure the path points to a valid technology file.

LIB-008

(Error) %s failed. Library '%s' is modified.

Description

The specified operation failed because the library contains modified and un-saved data.

What Next

Try again with the -force option.

LIB-009

(error) Library directory '%s' already exists

Description

A library directory with the specified name already exists.

What Next

Use another name for the new library or remove the library from the file system and rerun the command.

Feedback

LIB-010

(error) Library name is blank or empty.

Description

A library name was blank or an empty string.

What Next

Check that the given library name is valid simple path.

LIB-011

(error) Library '%s' is not found.

Description

The specified library is not found on the current search_path.

What Next

Check that the given library name has a valid value that can be found on the search_path.

LIB-012

(error) %s failed. Library '%s' is in read mode.

Description

The specified operation failed because the library is open in read mode.

What Next

open the library again in edit mode and try again.

LIB-013

(error) %s failed because the library cell library '%s' cannot be modified.

Description

The specified operation failed because the library is a library cell library. Library cell libraries are read-only in icc2_shell. They can be modified only in the library manager shell, lm_shell.

What Next

Use the library manager shell to make changes to this library.

Feedback

LIB-014

(Information) Re-setting technology section of library '%s' with '%s'.

Description

The technology section of the specified library is being replaced.

LIB-015

(Information) Adding design '%s' to library '%s'.

Description

The specified design.view is being added the the library.

LIB-016

(Information) Removing design '%s' from library '%s'.

Description

The specified design.view is being removed the the library.

LIB-017

(Information) Incrementing open_count of library '%s' to %d.

Description

The library is already in memory. Each open_lib command on a library will increase a library's open_count by one.

LIB-018

(Information) Decrementing open_count of library '%s' to %d.

Description

The library is still in memory. Each close_lib command will decrease a library's open_count by one. The library is removed from memory when its open_count drops to zero.

LIB-019

(Error) rebuild_lib cannot be used on single-file format library.

Feedback

Description

rebuild_lib can only be used on directory-format library to rebuild a library's design catalog based on the directory contents.

What Next

Make sure the library is in directory format and try again.

LIB-020

(Error) Technology replacement failed. Technology is incompatible.

Description

The technology data must be compatible with the existing technology data in the library.

What Next

Make sure the replacement technology data is compatible.

LIB-021

(Error) Cannot copy library to self.

Description

The source and destination library are the same. Copying a library to itself is not allowed.

What Next

Try a different destination library name.

LIB-022

(Error) Cannot move library to self.

Description

The source and destination library are the same. Moving a library to itself is not allowed.

What Next

Try a different destination library name.

LIB-023

(Warning) Library '%s' is being opened in read mode because it is a library cell library.

Feedback

Description

Library cell libraries are read-only in icc2_shell. They can be modified only in the library manager shell, lm_shell.

What Next

Use the library manager shell to make changes to this library.

LIB-024

(Error) %s failed. Library '%s' is modified.

Description

The specified operation failed because the library contains modified and un-saved data.

What Next

Try again with the -force option.

LIB-025

(Error) technology library '%s' is invalid.

Description

A technology library must be a valid library and it must have a technology section.

What Next

Try again with a library with a valid technology section and that is accessible through the current search_path setting.

LIB-026

(error) Reference library path '%s' is the same as the library.

Description

The reference library path cannot point to the library itself.

What Next

Make sure the reference library path is not the same as the library path and try again.

LIB-027

(error) Reference library path '%s' is not a valid library

Feedback

Description

The reference library path does not point to a valid library given the current search_path setting.

In case that physical source files were provided to automatically create reference libraries, a technology file must also be specified. If no technology file specified, then the tool will treat all files provided as full NDM reference libraries, thus report this message.

What Next

Check that the given reference library path has a value that can be found on the search_path. If auto reference libraries creation is desired, then please also provide a technology file.

LIB-028

(Error) rebuild_lib cannot be used on library that hasn't been saved to disk.

Description

rebuild_lib can only be used on directory-format library to rebuild a library's design catalog based on the on-disk directory contents.

What Next

If you haven't saved the library to disk, you don't need rebuild_lib.

LIB-029

(Error) Library already has a technology section.

Description

read_tech_file cannot be used to replace the technology section of a library. It will fail if a library already has or associates with a technology section.

What Next

Make sure the library does not already contain a technology section.

LIB-030

(Error) Library '%s' has no technology information.

Description

The library does not have a technology section. copy or move a designs into this library will fail.

Feedback

What Next

Check that the library contains a technology section. Use read_tech_file to create a technology section.

LIB-031

(Error) Library '%s' and '%s' contain incompatible technology information.

Description

The specified libraries contain incompatible technology sections. copy or move designs between these two libraries will fail.

What Next

Check that the two libraries contains compatible technology sections.

LIB-032

(information) Overwriting library '%s'.

Description

The library is being overwritten. It will be removed from the ref_lib list of all currently opened libraries that reference it, and be replaced with a new library.

What Next

Showing the library name to help understand when a library is being overwritten.

LIB-033

(Information) Promoting open_mode of library '%s' from read to edit.

Description

The library is already open in read mode. Subsequent open_lib -edit will promote the library open_mode from read to edit.

LIB-034

(error) Cannot write out technology file '%s'.

Description

The specified library cannot write out technology file.

Feedback

What Next

Make sure the specified library was valid.

LIB-035

(warning) Library '%s' is not being saved because it is in read mode.

Description

The specified library is not saved during save_lib -all because it is open in read mode.

What Next

open this library in edit mode and try again.

```
prompt> open_lib <lib_name> -edit
```

LIB-036

(error) Library '%s' is referenced by another library '%s'.

Description

A library cannot be closed or removed if it is on another library's reference library list. The higher-level library that references it must be closed first.

What Next

Remove the library that references this library first, and then remove this library. Or force the library to be purged from memory with the *-purge* option.

```
prompt> close_lib -force ...
```

LIB-037

(information) Replacing %s file '%s' with '%s'

Description

This informational message shows the full path name and type of a file being read into the application, replacing an existing one.

What Next

Use the full path name to help understand any problems encountered while reading the file.

Feedback

LIB-038

(error) Cannot open %s library '%s' as reference library.

Description

Physical libraries can be generated from Library Manager frame flow or Library Compiler create_physical_lib. In order to use such libraries as reference libraries with physical data only, the libraries must be prepared using Library Manager “create_workspace -flow physical_only” or Library Compiler “create/compile_fusion_lib -frame” commands. Direct usage will no longer be supported starting in T-2022.03-SP3 release.

LIB-039

(error) Cannot open logical library '%s' in '%s' flow.

Description

You can save a library from the library manager shell (lm_shell) prior to checking the workspace using *save_lib*. If the source of the library was a DB or .lib file, this is considered a logical source library. These libraries can be reloaded into the library manager at a later time, but they cannot into a workspace in any of these flows: *edit*, *physical_only* or *organize_by_pvt*.

LIB-041

(error) Cannot open %s library '%s' outside of a workspace.

Description

Only complete NDM files can be opened outside of a workspace, and they will be read-only. Other NDM file types (such as frame files) cannot be opened outside of the workspace.

What Next

If you are trying to change a frame NDM, create a workspace with the frame flow, and load the ndm file using *read_ndm*.

LIB-042

(warning) Library '%s' cannot be added to the aggregate library.

Feedback

Description

Design libraries or aggregate libraries cannot be added to an aggregate library. Only libraries which were written by the library manager, lm_shell, using *commit_workspace*, using a flow other than the *aggregate* flow, can be added to an aggregate.

LIB-043

(information) Library '%s' has been added to the aggregate library.

Description

This is an informational message that you will see in the library manager shell, using the aggregate flow, indicating that a lib-cell library has been added to the aggregate library, usually after using *open_lib*.

LIB-044

(information) Library '%s' has been removed from the aggregate library.

Description

This is an informational message that you will see in the library manager shell, using the aggregate flow, indicating that a lib-cell library has been removed from the aggregate library, usually after using *close_lib*.

LIB-045

(error) Can not save %s library '%s'.

Description

This message is reported when you try to save a workspace library or uncommitted logic library in Library Manager.

What Next

Can not save workspace library or uncommitted logic library.

LIB-046

(error) Library '%s' cannot be used for the the edit flow

Feedback

Description

When creating a workspace in the library manager shell (lm_shell) with the edit flow, only a library previously committed by lm_shell can be specified. Design libraries, aggregate libraries, or libraries saved from the lm_shell with *save_lib* cannot be used in this context.

LIB-047

(warning) library '%s' is already in the aggregate library.

Description

This lib-cell library was already in the aggregate library. It cannot be added to the aggregate library multiple times.

LIB-048

(Information) Technology file was not replaced. '%s' is identical to the current technology file.

Description

This informational message tells that technology file was not replaced. The replacement technology file contains identical content as the current technology file.

LIB-049

(error) Block '%s' is open. Technology file cannot be replaced while blocks are opened in the library.

Description

It is an error to replace the technology section in a library in which there are open blocks. As technology file replacement could clobber in-memory design data. All blocks must be closed during technology file replacement.

What Next

close all opened block and try again

LIB-050

(error) Library '%s' is also bound to this tech section. Technology file cannot be replaced if the tech section is bound to more than one library.

Feedback

Description

It is an error to replace the technology section in a library if the technology section are referenced by other libraries in memory, as technology file replacement could clobber in-memory library data. All other libraries that reference this technology section must be closed during technology file replacement.

What Next

close the other libraries and try again.

LIB-051

(error) Version '%s' is not supported. Use report_versions to list available versions.

Description

The specified version is not supported. save_lib can only save to specific release versions. Please use report_versions to list the versions available.

What Next

Try again with a valid release version.

LIB-052

(error) Cannot close a member library of an aggregate library.

Description

This message indicates that you tried to close a member library of an aggregate library but the closing of a member library was not allowed. When an aggregate library is opened, all member libraries of the aggregate library are also opened automatically and will be closed when the aggregate library is closed. If a member library is specifically closed using the close_lib or remove_lib command, the member library will be removed from the containing aggregate library. However, the removal of a member library from an aggregate library can only be done in the aggregate flow in the library manager shell.

LIB-053

(error) Specified length precision '%d' does not match that of already opened libraries '%d'.

Description

This message indicates that you specified the length precision for the new library in create_lib command using "-scale_factor" option. However, libraries with a different length precision are already open. This is not allowed. All libraries open at the same time must

have the same length precision. Similarly, the length precision of any reference libraries used for create_lib, must be identical to the length precision for the new library.

What Next

Here are a few options, 1) Provide the correct length precision or remove the option, in which case length precision will be inherited from previously opened libraries. 2) If the libraries already open are not needed, please close them and rerun the command.

LIB-054

(error) Specified length precision '%d' is not valid.

Description

The specified length precision is not a valid value.

What Next

The valid values for length precision are 100, 200, 1000, 2000, 4000, 10000 and 20000

LIB-055

(error) Length precision '%u' in the input file is not compatible with the length precision '%u' used in the current library.

Description

The input file (DEF, LEF or GDS) cannot be read in as it will result in data being lost when converting length numbers from the file to the internal data in the library.

What Next

Please choose a different input file which has a length precision that can be used to translate the numbers without loss of data.

LIB-056

(error) Length precision '%d' specified for output file is not compatible with the length precision '%d' used in the current library.

Description

The file (DEF, LEF or GDS) cannot be written out with the specified length precision, as it will result in data being lost when converting length numbers from internal data in the library for output.

Feedback

What Next

Please specify a compatible length precision, which can preserve all data.

LIB-057

(error) The length precision of the library being opened '%s' does not match that of already opened libraries '%d'.

Description

This message indicates that the library being opened has a scale factor different from libraries previously opened. This can happen for a library being opened explicitly, using *open_lib*, or implicitly if it is being set as a reference library for a main library using either *create_lib* or *set_ref_libs* commands. This is not allowed. All libraries opened at the same time must have the same length precision. All reference libraries must have the same length precision as the main library.

What Next

Here are a few options, 1) If the library is used as a reference library, remove it from the list of specified reference libraries. 2) Choose reference libraries with the correct scale factor. 3) Close previously opened libraries if they are no longer needed.

LIB-058

(warning) Length precision '%d' specified for output file can result in loss of data because it is less than the precision used in the library '%d'.

Description

The file (DEF, LEF or GDS) should not be written out with the specified length precision, as it will result in data being lost when converting length numbers from internal data in the library for output.

What Next

Please specify a compatible length precision, which can preserve all data.

LIB-059

(Error) technology library '%s' does not match any library on the reference library list.

Feedback

Description

The technology library must be specified either as a simple path that matches the tail portion of an reference library entry or as a relative or absolute path that exactly match an entry on the reference library list.

What Next

Add a matching entry of the technology library on the reference library list.

Examples

create_lib -use_technology_lib technology_lib.nlib -ref_libs { technology_lib.nlib }

create_lib -use_technology_lib ../nlibs/technology_lib.nlib -ref_libs { ../nlibs/technology_lib.nlib }

create_lib -use_technology_lib technology_lib.nlib -ref_libs { ../nlibs/technology_lib.nlib }

LIB-060

(error) Version '%s' is not supported. Supported version range must be within %s and %s.

Description

The specified version is either not in the supported format, or outside the supported range. Schema version must be specified in <major>.<minor> format and between the last compatible schema version and the current schema version.

What Next

Try again with a valid schema version format within the allowable range.

LIB-061

(information) Version '%s' is truncated to '%s'.

Description

The input version cannot be found, to truncate the input version string to the character '-' from the last one to the first. The truncation will stop when the rest string is legal or without '-' in the rest.

What Next

To input legal version. User can get legal versions by report_version.

Feedback

LIB-062

(error) The length precision of the library being opened '%s' does not allow its data to be scaled correctly.

Description

This message indicates that the library being opened has a scale factor that cannot be correctly scaled for the *design.session_scale_factor*. This can happen for a library being opened explicitly, using *open_lib*, or implicitly if it is being set as a reference library for a main library using either *create_lib* or *set_ref_libs* commands. This is not allowed. The *design.session_scale_factor* must be a multiple of the length precision of the library being opened.

What Next

Here are a few options, 1) Set *design.session_scale_factor* to a different value which is a multiple of length precision of all libraries needed. Please note if *design.session_scale_factor* is changed, all open libraries must be closed and reopened. 2) If the library is used as a reference library, remove it from the list of specified reference libraries. 3) Choose reference libraries with the correct scale factor. 4) Close previously opened libraries if they are no longer needed.

LIB-063

(info) The library must be saved, closed and reopened for any change in value of half_node_scale_factor attribute to take effect.

Description

The library must be saved, closed and reopened for any change in value of *half_node_scale_factor* attribute to take effect. Further, the attibute *half_node_scale_factor* can only be set when no designs from the library are open.

What Next

Please close all designs from this library before changing *half_node_scale_factor*. After changing the attribute, save, close and reopen the library to continue.

LIB-064

(error) Specified scale factor '%d' is not compatible with the session scale factor '%d'.

Description

This message indicates that the specified the scale factor is not compatible with the session scale factor. Scale factor is also known as length precision. The session scale

factor is specified using the app option *design.session_scale_factor*. The session scale factor must be a mutliple of the scale factor for the library.

What Next

Please specify a scale factor so that the session scale factor is a multiple of that.

LIB-065

(error) Required argument '%s' was not found.

Description

This message indicates that the *-scale_factor* argument must be specified due to the app options being used. If either of *design.allow_multiple_scale_factors* or *design.is_3dic_mode* app options are set to true and *design.session_scale_factor* is also set, the *-scale_factor* must be specified when running *create_lib*.

What Next

Please specify the -scale_factor argument

LIB-066

(error) Specified scale factor '%d' does not match the session scale factor '%d'.

Description

For converting libraries from one scale factor to another, the session scale factor is the library scale factor. A different scale factor is not allowed. The session scale factor is specified using the app option *design.session_scale_factor*.

What Next

Please specify a scale factor so that it is same as the session scale factor or remove the argument from the command.

LIB-067

(warning) Length precision '%d' specified in the input file can result in loss of data because it is more than the precision used in the library '%d'.

Description

The file (DEF) being read in has distance data in length precision higher than the design library. It can potentially result in data being lost when converting length numbers to internal data in the library during read.

Feedback

What Next

Please use a library with appropriate scale factor to avoid data loss.

LIB-068

(error) Cannot open library '%s' because it has potential risk of precision loss.

Description

Physical library created with potential risk of precision loss is not allowed to be opened and used. The physical lib could be created with smaller scale factor than its tech file's length precision.

What Next

Regenerate the physical library and make sure its scale factor is equal or larger than its tech file's length precision.

LIB-068w

(Warning) The library '%s' opened has potential risk of precision loss.

Description

Physical library created with potential risk of precision loss is not allowed to be opened and used, unless lib.setting.allow_ref_lib_with_lossy_scale_factor has been turned on. The physical lib could be created with smaller scale factor than its tech file's length precision.

What Next

Regenerate the physical library and make sure its scale factor is equal or larger than its tech file's length precision.

LIB-069

(Warning) The physical library '%s' is being created with potential risk of precision loss.

Description

The physical lib is being created with smaller scale factor than its tech file's length precision, which could lead to precision loss.

What Next

Regenerate the physical library and make sure its scale factor is equal or larger than its tech file's length precision.

Feedback

LIB-070

(error) No such PVT configuration rule '%s'

Description

The rule you specified to *set_pvt_configuration -rule* does not exist. When this error occurs, for convenience, the application will show the current configuration.

What Next

Check for spelling errors and re-enter the command to change the current rule and apply changes to it.

LIB-071

(information) %s PVT configuration rule '%s'

Description

This is an informational message indicating that the *set_pvt_configuration* command either created a new rule or deleted an existing rule because you removed all constraints from it.

LIB-072

(error) No panes in lib '%s' matched your PVT configuration

Description

You created a PVT configuration using *set_pvt_configuration*. Now, when opening a reference library with *open_lib*, the information from the configuration is used to determine which logical panes of data are active. Your configuration has deactivated all of the panes from this library, effectively rendering the library useless to timing, power, and optimization. The library fails to open.

What Next

It's possible that you loaded a library that simply does not have any desirable PVTs. If this message is unexpected, consult the configuration (using *set_pvt_configuration* with no arguments) and determine why all of the panes were filtered out. Then adjust the configuration rules accordingly to enable the desired PVTs.

LIB-073

(warning) PVT configuration changes are not applied to open libs

Feedback

Description

You made a change to the PVT configuration using *set_pvt_configuration* and there were one or more reference libraries already open. The PVT configuration is only applied at the time the reference library is opened with *open_lib*. Incremental changes to libraries already opened is not possible.

What Next

If you wanted to change the available PVTs for the libraries that are already open, you need to first close these libraries, then reopen them after the configuration has been updated.

LIB-074

(error) Cannot create PVT configuration rule named '%s': %s

Description

The name you specified to *set_pvt_configuration -name* is invalid. The message will say why. Typically, the name you supplied is already in use as a rule name, or it is empty or all whitespace.

What Next

Check for spelling errors and re-enter the command to create the rule.

LIB-075

(warning) Library '%s' has no reference Libraries.

Description

The Libaries has no reference Libraries.

What Next

The reference library list can be set using set_ref_lib command.

LIB-080

(warning) Cannot find .frame/LEF/Milkyway input, the auto reference library creation will be disabled.

Description

When link_library is specified, those db files should either 1) be covered by full NDM reference libraries, or 2) there should have .frame/LEF/Milkyway physical library view

specified, so that auto reference library can be created. This message indicates that no physical library view can be found, so that the auto reference library creation will be disabled.

What Next

To create reference library automatically, please provide physical library views corresponding to the link_library.

LIB-081

(warning) No db files from link_library to create reference libraries, will create a physical-only reference library.

Description

For automatic reference library creation, the logical data comes from the db files specified in link_library setting. If full NDM reference libraries also specified, then those db files already in the full NDM reference libraries will be excluded from auto reference library creation.

This message indicates that either no db files specified in link_library, or all db files specified in link_library are already contained in full NDM reference libraries. In that case, no db files will be used for auto reference library creation, thus a physical-only reference library will be created.

What Next

If creating physical-only reference library is not desired, please provide necessary db files in link_library setting.

LIB-082

(error) Failed to create reference library %s, please check log file %s for detailed error.

Description

This message indicates that the reported reference library was not created successfully from auto reference library creation.

What Next

Please refer to the error message printed prviously, or indicated log file for detailed error information.

Feedback

LIB-083

(warning) There are %d %s not used for creating cell libraries: %s.

Description

This message reports a list of files that provided but not used for cell libraray creation. This could be caused by not reading the files successfully. For db files, it could be caused by no corresponding physical data.

What Next

Please check messages printed previously, or the log files under the log directory to know the detailed information.

LIB-084

(information) Auto created reference libraries are up-to-date, no need to rebuild.

Description

This message indicates that all automatically created reference libraries are up-to-date. There is no need to rebuild them.

What Next

This is an informational message, no action required.

LIB-085

(information) Need to rebuild auto created reference library: %s.

Description

This message indicates that automatically created reference libraries need to be rebuilt. The reason was given along with the message itself.

What Next

This is an informational message, no action required.

LIB-086

(information) Rebuild of auto created reference libraries succeeded.

Feedback

Description

This message indicates that rebuild of the automatically created reference libraries succeeded.

What Next

This is an informational message, no action required.

LIB-087

(warning) Skip the rebuild of the auto created reference libraries: %s.

Description

This message indicates that the auto created reference libraries need to be rebuild. However, some pre-conditions cannot be met so the rebuild was skipped. Most likely, the source files for rebuild the auto created reference libraries cannot be found.

What Next

To rebuild the auto created reference libraries, please make sure that all source files for building them can be found using search_path.

LIB-088

(error) Failed to rebuild the auto created reference libraries.

Description

This message indicates that the rebuild of the auto created reference libraries failed.

What Next

Please refer to the previously reported error messages for detailed information.

LIB-089

(error) %s '%s' is not valid: %s.

Description

This message indicates that the specified file is not valid. The reason is reported with the message itself.

LIB-090

(error) %s '%s' must be specified: %s.

Feedback

Description

This message indicates that required option must be specified. The reason was reported alone with the message itself.

LIB-091

(error) Failed to convert Milkyway libraries to frame view.

Description

This message indicates that convert Milkyway libraries to frame view failed.

What Next

Please refer to previously reported error messages for detailed information.

LIB-092

(error) Failed to create %d (total %d) reference libraries, please check log file '%s' for detailed error.

Description

This message indicates that auto reference libraries creation failed. There are some reference libraries not created successfully.

What Next

Check the reported log file for detailed errors.

LIB-093

(information) Successfully built %d reference libraries: %s.

Description

This message indicates that auto reference library creation was succeeded.

What Next

This is an informational message. No action required.

LIB-094

(information) Successfully converted %d Milkyway libraries: %s.

Feedback

Description

This message indicates that the Milkyway library to frame conversion was succeeded.

What Next

This is an informational message. No action required.

LIB-095

(error) Failed to create frame library %s, please check log file '%s' for detailed error.

Description

This message indicates that the reported frame library was not created successfully from corresponding Milkyway library.

What Next

Please refer to the error message printed prviously for detailed error information.

LIB-096

(error) Cannot launch %s to %s.

Description

This message indicates that launching a specific executable for a specific job failed.

What Next

If the executable is IC Compiler shell, please make sure it is a valid executable.

LIB-097

(information) db files specified in link_library already covered by full NDM reference libraries, the auto reference library creation will be disabled.

Description

When link_library is specified, those db files should either 1) be covered by full NDM reference libraries, or 2) there should have .frame/LEF/Milkyway physical library view specified, so that auto reference library can be created. This message indicates that db files already covered by full NDM reference libraries, so that the auto reference library creation will be disabled. The full NDM reference libraries specified will be used directly.

What Next

This is an informational message, no action is required.

Feedback

LIB-098

(information) Use existing reference libraries.

Description

There should be an attempt to rebuild the auto reference libraries and the attemp was failed. This message indicates that existing reference libraries will be used.

LIB-099

(warning) Override the previous label mapping, now db '%s' attaches to %s label '%s'.

Description

This message occurred when users attached the same db name with 2 or more different labels by setting app option lib.configuration.process_label_mapping. For example: When users set the process label mapping with the below command: set_app_options -name lib.configuration.process_label_mapping -value {{label1 {tcbn90ghplt_ccs.db}} {label2 {tcbn90ghplt_ccs.db}}}

The LIB-099 warning message will be displayed as below: Warning: Override the previous label mapping, now db 'tcbn90ghplt_ccs.db' attaches to process label 'label1'.(LIB-099)

What Next

Please correct the issue of the app option(lib.configuration.process_label_mapping) setting, and then set the app option with the corrected setting.

LIB-100

(warning) link_library does not cover all db files of the library '%s'.

Description

This message is reported when lib.configuration.force_update_timing_views app option is set to true. It indicates that the db files specified in the link_library app var does not cover all db files of a source library. So, one or more db files in the source library will missing in the generated cell library.

What Next

Please verify that the missing of db files is expected.

LIB-101

(error) Prebuilt library '%s' cannot be in the output directory '%s'.

Feedback

Description

This message is issued when the *lib.configuration.force_update_timing_views* application option is set to *true* and the reported prebuilt library is in the output directory specified with *lib.configuration.local_output_dir* application option.

What Next

Put the prebuilt library into another directory, or specify a different output directory with the *lib.configuration.local_output_dir* application option.

LIB-102

(error) Physical source file '%s' cannot be associated with two assembly scripts: '%s' and '%s'.

Description

This message indicates that the value specified for *lib.configuration.assembly_scripts* application option is not valid. The reported physical source file is associated with more than one assembly script. This is not allowed as the tool will not able to determine which assembly script should be used to assembly the data.

What Next

Revise the app option value to make sure every physical source file only be associated with one assembly script.

LIB-103

(error) Application option '%s' has an invalid value.

Description

This message indicates that the specified application option has an invalid value.

What Next

Provided a correct value for the application option.

LIB-104

(error) Cannot determine assembly script: physical source file '%s' associated with assembly script '%s', physical source file '%s' associated with assembly script '%s'.

Feedback

Description

This message indicates that two physical source files of one lib have different assembly scripts. In this case, tool cannot determine which assembly script to use.

What Next

Revise the lib.configuration.assembly_scripts application option to have correct mapping between assembly scripts and physical source files.

LIB-105

(error) Failed to group source data, please check log file %s for detailed error.

Description

This message indicates that the tool failed to group the source data, .db files from link_library and physical files from -ref_libs option, into groups that for reference libraries creation.

What Next

Please refer to the indicated log file for detailed error information.

LIB-106

(warning) %s will not be persistent because '%s' is a library cell library, so the setting will be lost when the session ends.

Description

The specified operation will apply in this session only because the library is a library cell library. Library cell libraries are read-only in icc2_shell. They can be modified only in the library manager shell, lm_shell. To have the setting persist without using the library manager shell, you can make the setting in a script that is called at each new session.

What Next

Use the library manager shell to make permanent changes to this library. To have the setting persist without using the library manager shell, you can make the setting in a script that is called at each new session.

LIB-107

(warning) Found duplicated db file '%s' in the link_library. The duplicated one will be ignored.

Feedback

Description

The reported db file is duplicated specified in the link_library. Only the first one will be used. All duplicates will be ignored.

What Next

Remove the duplicated db files in the link_library.

LIB-108

(information) Can reuse library %s, skip %s.

Description

This message indicates that specified library is up-to-date. The specified action can be skipped.

What Next

This is an informational message, no action required.

LIB-109

(information) Cannot reuse library %s: %s.

Description

This message indicates that specified library cannot be reused for current operation. The reason is given in the message.

What Next

This is an informational message, no action required.

LIB-110

(error) No opened physical library to save.

Description

There is no opened physical library in memory, so no library for this command to save.

What Next

Check if you need to create or open a library before save it to disk.

Feedback

LIB-111

(Error) Technology data in %s and currrent physical library's technology data is not compatible

Description

Technology data in the library which is reading and current physical library's technology data must be compatible, otherwise *read_ndm* will fail.

What Next

Try another library with compatible technology data.

LIB-112

(warning) Current physical library's technology data replaced by the technology data from '%s'

Description

read_ndm will replace the current physical library's technology data with technology data from the library which is reading. The replacement occurs when the two technology data are compatible.

LIB-113

(error) Cannot open or create multiple libraries, library '%s' has already been opened.

Description

Only one physical library is allowed to be opened or created at the same time. You can only create or open another physical library after closing current library.

What Next

Close the current the library, and then create or open the new library.

LIB-114

(error) Cannot open a none library cell library '%s'.

Description

Only library cell library is allowed to be opened with this command. You will see this error if you are trying to open a none library cell library with this command, such as design library.

Feedback

What Next

Open a library cell library instead.

LIB-115

(warning) Set app option '%s' has no effect when app option '%s' is %s.

Description

Set first app option has no effect when the second app option has specified value.

What Next

Make sure the second app option has a proper value, then set the first app option again.

LIB-116

(warning) Ignore the application option '%s': %s.

Description

The reported application option will be ignored for the given reason.

What Next

Refer to the man page of the corresponding application option and make sure it has a proper value.

LIB-117

(warning) Library configuration will not be performed: %s.

Description

This warning message indicates that the library configuration will not be performed. The possible reason is that technology file is not specified.

This message will only be reported when link_library application variable is specified.

What Next

Make sure technology file is specified if need to invoke library configuration.

LIB-118

(error) Reference library path '%s' will introduce cyclic reference libraries on the library.

Feedback

Description

The reference library path should not introduce cyclic reference libraries as it will lead to opening a library infinite times. Cyclic reference libraries structure: library 'MID' is reference library to library 'TOP' and again library 'TOP' is reference library ot library 'MID'.

What Next

Make sure the reference library path doesn't create any cyclic reference libraries. To make sure no cyclic reference libraries are formed, add the reference libraries bottom-up (BOT->MID->TOP) approach.

LIB-119

(error) Invalid value '%s' specified for application option '%s': %s.

Description

This message indicates that the specified application option has an invalid value.

What Next

Provided a correct value for the application option.

LIB-120

(error) Invalid value '%s' specified for command option '%s': %s.

Description

This message indicates that the specified command option has an invalid value.

What Next

Provided a correct value for the command option.

LIB-121

(error) Current working directory is not writable.

Description

The command being executed need a writable current working directory.

What Next

Change current working directory to a writable directory and try again.

Feedback

LIB-122

(information) There are missing or invalid reference libraries. Will try to rebuild.

Description

This message indicates that some or all reference libraries of the library to be opened is missing or invalid. It will try to rebuild reference libraries.

What Next

This is an informational message, no action required.

LIB-123

(warning) Local output directory '%s' containing cell libraries that are used by following processes: %s. Cannot remove it now. Please remove it manually when those processes exit.

Description

This warning message will reported when *lib.configuration.remove_local_output_dir* application option is true, but it cannot remove the local output directory because there are other processes are using the cell libraries in it.

What Next

Check the processes reported in the message. When they all exit, remove the local output directory manually.

LIB-124

(warning) Cannot use '%s' as local output directory. Library configuration skipped.

Description

This warning message indicates that the value of *lib.configuration.local_output_dir* application option is not valid, and the library configuration will be skipped. Usually, this means the directory is a volatile cache of another process.

What Next

Set *lib.configuration.local_output_dir* to another proper directory and try again.

LIB-125

(error) Attribute '%s' cannot be imported: You defined it as %s; db defines it as '%s'.

Feedback

Description

You receive this error message because while reading an attribute from db, there was a mismatch between the type (integer, string, etc.) that db defines for the attribute and the type that PrimeTime defines for the attribute. Usually, this is a user-defined attribute, defined with the *-import* option on *define_user_attribute*, and the types do not match.

What Next

Rerun PrimeTime and define the attribute correctly. You might need to use other Synopsys applications to determine the actual type of the attribute.

LIB-126

(information) Cannot use '%s' as local output directory. Library configuration skipped.

Description

This message indicates that the tool cannot use the specified directory as the local output directory, and the library configuration will be skipped. Usually, this means the directory is already a volatile cache of another process.

What Next

This is an informational message and no action required.

LIB-127

(Information) Find %s '%s' from %s.

Description

This message indicates where a specific executable was found.

LIB-128

(error) Cannot find %s '%s' from %s: %s.

Description

This message indicates that a specific executable cannot be found from the reported location.

What Next

Check whether the related environment variable is correct.

Feedback

LIB-129

(error) Library configuration skipped, since "%s" are different between master and current session.

Description

This message indicates that current session changed link_library or physical libraries while the shared volatile cache directory is using by the other ICC2 sessions.

What Next

Run the library configuration flow again while there is no other session using the volatile cache directory.

LIB-130

(information) Library configuration is pending, the master session is running library configuration with the same configuration as the current session.

Description

This message indicates that the current session has the same link_library and physical libraries' setting as the master session which is running library configuration to build the reference libs in the shared volatile cache directory.

What Next

This is an informational message and no action required.

LIB-131

(warning) Library '%s' is not in the reference library list of current_lib '%s'.

Description

The desired library must be a reference library of current_lib.

What Next

Either use current_lib switch to the design library which has desired library as reference library, or add the desired library to the current lib's reference library list.

LIB-132

(warning) None of panes in lib '%s' matched the specification.

Feedback

Description

The *get/set_lib_timing*, *get/set_lib_pin_capacitance*, *get/set_lib_max_cap_table*, *get/set_lib_max_trans_table* commands issue this error message when they cannot find a pane in the desired library that matched the voltage, temperature, process number, and process label data.

What Next

Either use *report_lib* to find out the exactly values of voltage, temperature, process number, and process label data, or simply delete the option -voltage/-number/-label/-temperature if you don't know the exactly values.

LIB-133

(warning) The objects do not have specified constraint table.

Description

The *get/set_lib_timing* commands issue this error message when they cannot find the desired constraint table.

What Next

Check the object with input options again. Use *get_lib_timing -table setup_hold */** to see if the desired table are there.

LIB-134

(error) The option -shift_value must be followed by a non-zero value.

Description

The *set_lib_timing* command issues this error message when giving zero to -shift_value.

What Next

Gives a non-zero value to -shift_value and run the command again.

LIB-135

(warning) The command only supports setting scalar, 1-D, and 2-D table.

Description

The *set_lib_timing* command issues this warning message when the object is the table that dimension greater than two. The table value will keep the same.

Feedback

What Next

Use *set_lib_timing* on the table which has dimension smaller or equal to two.

LIB-136

(error) The objects do not exist in reference libraries.

Description

The *get/set_lib_pin_capacitance*, *get/set_lib_max_cap_table*, *get/set_lib_max_trans_table* commands issue this error message when they cannot find the desired object in reference libraries.

What Next

Make sure the desired objects are in the reference libraries.

LIB-137

(warning) There is no %s table on this lib pin.

Description

The *get/set_lib_max_cap_table*, *get/set_lib_max_trans_table* commands issue this warning message when there is no max_cap/max_trans table on the specified library pin.

What Next

Make sure the specified library pin contains max_cap/max_trans table.

LIB-138

(warning) The desired table on the specified library pin is not a 1-d frequency based %s table.

Description

The *get/set_lib_max_cap_table*, *get/set_lib_max_trans_table* commands issue this warning message when the desired table on the specified library pin is not a 1-d frequency based max_cap/max_trans table. The *get/set_lib_max_cap_table*, *get/set_lib_max_trans_table* commands are only supporting get/set 1-d frequency based max_cap/max_trans table.

What Next

Make sure the desired table on the specified library pin is a 1-d frequency based max_cap/max_trans table.

Feedback

LIB-139

(error) When -index_1 option is specified, the -value option must be a single value.

Description

The *set_lib_max_cap_table* command issues this error message when specified -index_1 option but the argument for -value is not a single value. Using -index_1 only when you want to modify a value in max_cap table at certain index (frequency). You must to specify a single value for -value.

What Next

Give a single value for -value and run the command again.

LIB-140

(warning) Invalid -index_1 value '%f', only accepts existing table index

Description

The *set_lib_max_cap_table*, *set_lib_max_trans_table* commands issue this warning message when specified -index_1 option but none of that index_1 value is in the table index.

What Next

Use *get_lib_max_cap_table*, *get_lib_max_trans_table* to see all the index_1 values in the table.

LIB-141

(error) -value list size is '%lu', which is different to table width '%d'

Description

The *set_lib_max_cap_table*, *set_lib_max_trans_table* commands issue this error message when the given list of -value size is not equal to table width.

What Next

Use *get_lib_max_cap_table*, *get_lib_max_trans_table* to check the table size.

LIB-142

(information) There is no lib data change in the scope of current_lib: '%s'

Feedback

Description

The *report_lib_changes* command issues this informational message when there is no lib data change related to the reference libraries of current library.

What Next

This is an informational message and no action required.

LIB-143

(information) All lib data changes in the scope of current_lib are reverted back to original values.

Description

The *revert_lib_changes* command issues this informational message when it reverted all modified data within the scopt of current_lib back to original values successfully.

What Next

This is an informational message and no action required.

LIB-144

(information) Previous set lib data command attachment is now deleted

Description

This informational message means there was an attachment recording the operations of *set_lib_timing*, *set_lib_pin_capacitance*, *set_lib_max_cap_table* and/or *set_lib_max_trans_table*; and now the attachment has been deleted because you reverted all lib changes and saved it.

What Next

This is an informational message and no action required.

LIB-145

(information) Set lib data command(s) found, are saved into attachment.

Description

This informational message means there were operations of *set_lib_timing*, *set_lib_pin_capacitance*, *set_lib_max_cap_table* and/or *set_lib_max_trans_table* in the session. The operations were recorded and saved in an attachment. These operations will be reapply when you use *open_lib* to open the library again.

Feedback

What Next

This is an informational message and no action required.

LIB-146

(information) Reapplying previous lib data changes recorded in '%s'

Description

This informational message means there were operations of *set_lib_timing*, *set_lib_pin_capacitance*, *set_lib_max_cap_table* and/or *set_lib_max_trans_table* saved inside the design library, and these operations are re-applying.

What Next

This is an informational message and no action required.

LIB-147

(warning) The attachment recorded lib data change(s) failed to compile, so the previous lib data changes are not reapplied.

Description

This warning message is issued when there is an attachment recorded operations of *set_lib_pin_capacitance*, *set_lib_max_cap_table*, *set_lib_timing* and/or *set_lib_max_trans_table*, but the attachment can not be compiled successfully during *open_lib*, so that the previous lib data changes are not able to reapply. The reason could be 1. Too old Library Compiler version (require at least 19.12 version). 2. Attachment format is invalid.

What Next

Make sure your $SYNOPSYS_LC_ROOT is pointing to latest version Library Compiler. Make sure the attachment (lib.setLibDataCmd) format is valid Liberty format.

LIB-148

(warning) Library data change is applied, but not recorded.

Description

The commands *set_lib_pin_capacitance*, *set_lib_max_cap_table*, *set_lib_timing*, *set_lib_max_trans_table* issue this warning message when the settings are applied without recorded. *set_lib_pin_capacitance*, *set_lib_max_cap_table*, *set_lib_timing*, *set_lib_max_trans_table* operations will only be recorded in a design library.

Feedback

What Next

Use *current_lib* to see if current library is a design library.

LIB-149

(error) The input of option -index_1 is invalid. Please make sure the values in the list are monotonically increasing.

Description

The commands *set_lib_max_cap_table*, *set_lib_max_trans_table* issue this error message when option -index_1 is specified with a invalid list of values.

What Next

Make sure the values in the list are monotonically increasing.

LIB-150

(error) The length of the input of option -index_1 and -value should be the same.

Description

The commands *set_lib_max_cap_table* and *set_lib_max_trans_table* issue this error message when give the option -index_1 and the option -value two different length input lists.

What Next

Make sure the the input lists of the option -index_1 and -value have same length.

LIB-151

(information) Successfully configured DB+Frame reference library: %s.

Description

This message indicates that DB+Frame reference library-configuration succeeded.

What Next

This is an informational message. No action required.

LIB-152

(error) Cache-free library name must be a simple name, it cannot be absolute or relative path.

Feedback

Description

The '~' and '/' character are used in absolute and relative path. It cannot be used in name of cache-free library.

What Next

Specify a simple name for the cache-free library.

LIB-153

(warning) We do not recommend a mixture of library specific rules and non-library specific rules.

Description

A -library rule is added and there are non-library rules, or if a non -library rule is added and there are -library rules. For example: set_pvt_configuration -library "libA libB*" -temperatures 125 -voltages 1.05 set_pvt_configuration -add -temperatures -25 Such setting may lead all panes in a library being eliminated. For example: lib 1 name : rose pane0: voltage 1.1 pane1: voltage 1.8 pane2: voltage 2.0 lib 2 name : rose2 pane0: voltage 1.2 Pane1: voltage 2.0 lib 3 name : daisey pane0: voltage 1.3 pane1: voltage 1.5

For the below mix setting(not recommend), all the panes of rose2 should be filtered. set_pvt_configuration -lib rose -voltage 1.1 set_pvt_configuration -add -voltage 1.3 The setting is equal to the below setting: set_pvt_configuration -lib rose -voltage 1.1 set_pvt_configuration -add -lib * -voltage 1.3

What Next

Specify all rules with -library or without -library option For example: set_pvt_configuration -library "libA libB*" -temperatures 125 -voltages 1.05 set_pvt_configuration -add -library "moreLib" -temperatures -25 or set_pvt_configuration -temperatures 125 -voltages 1.05 set_pvt_configuration -add -temperatures -25

LIB-154

(warning) The library option must be a file name (it cannot be a path): change the path "%s" to "%s".

Description

The file name specified with the -library option must be file name only, i.e. it cannot contain any path. For example: For the following reference library: tcbn90ghplvtwc_ccs, 2 panes: Pane 0: process = "" (1), voltages: 0.9; temperatures: 125 Pane 1: process = "" (1), voltages: 1.1; temperatures: -40 Here is a correct setting with library option to set pvt for pane0: set_pvt_configuration -library tcbn90ghplvtwc_ccs -voltages 0.9

But if users set the library option as below(bad setting): set_pvt_configuration -library ./ref/tcbn90ghplvt_ccs.ndm -voltages 0.9 The tool will issue LIB-154 and try to fix the issue by changing the path name to file name. For example: Warning: The library option must be a file name (it cannot be a path): change the path "./ref/tcbn90ghplvt_ccs.ndm" to "tcbn90ghplvt_ccs". (LIB-154) Current PVT Configuration: rule_1: Process Labels : <All included> Process Numbers: <All included> Voltages : 0.9 Temperatures : <All included> Libraries : "tcbn90ghplvt_ccs"

What Next

Specify a file name instead of path name for the library option.

LIB-155

(error) Cannot merge reference library name '%s' from ref_lib list of library '%s' to ref_lib list of library '%s' because it may be overshadowed by reference library name '%s'.

Description

This message indicates that merging the ref_lib from the ref_lib list of a sub-library to it's parent during uncommit_block could cause an issue, because a ref_lib of the parent would be used for a lib-cell instead of the sub-library. present in the sub-library would change positions relative to a ref_lib present in both libraries.

For example: lib1 has ref_libs {A C}, and sub_lib2 has ref_libs {B C}, and both B and C have the a lib-cell with the same name but different versions. Merging the ref_libs from sub_lib2 into lib1 would cause the ref_libs to be {A C B}, which may cause issues with ref_lib C overshadowing the element of ref_lib B

What Next

Try to manually merge the ref_libs in such a way that avoids one ref_lib overshadowing another for your project.

LIB-156

(Error) parasitic tech library '%s' does not match any library on the reference library list.

Description

The parasitic tech library must be specified either as a simple path that matches the tail portion of an reference library entry or as a relative or absolute path that exactly match an entry on the reference library list.

What Next

Add a matching entry of the parasitic tech library on the reference library list.

Feedback

Examples

create_lib -use_parasitic_tech_lib parasitic_tech_lib.nlib -ref_libs { parasitic_tech_lib.nlib }

create_lib -use_technology_lib ../nlibs/parasitic_tech_lib.nlib -ref_libs { ../nlibs/parasitic_tech_lib.nlib }

LIB-157

(Error) parasitic tech library '%s' is invalid.

Description

A parasitic tech library must be a valid library and it must have a parasitic tech section.

What Next

Try again with a library with a valid parasitic tech section and that is accessible through the current search_path setting.

LIB-158

(error) %s library has dedicated parasitic tech library %s.

Description

Library with dedicated parasitic tech library can not create local parasitic. First remove dedicated parasitic tech library from reference library list.

What Next

Check "set_ref_libs" command to remove dedicated parasitic tech library from reference list

---

LIB-159

(error) Library '%s' is referenced by another library as parasitic tech lib.

Description

A parasitic techs can not be replaced if library is, another library's parasitic tech lib.

What Next

Remove library from another library's reference list or close another library.

Feedback

LIB-160

(error) Cannot write library '%s' which has timing data.

Description

The write_physical_lib command can only write physical library. The given library has timing data so cannot be written.

What Next

Use Library Manager to write library with timing data.

LIB-161

(warning) Open library in read only mode, only physical library can be opened in edit mode.

Description

This message indicates that the given library is not a physical only library, and the -read option was not specified to open it. Library Compiler does not support modify a library with logical information. So the library was opened in read only mode. You can query information from it. But please do not use write_physical_lib with it.

What Next

This is a warning message. No action needed.

LIB-162

(error) Mask constraints check on library '%s' failed.

Description

This message indicates that mask constraints check on reported library failed. There is either uncolored shapes on multi-pattern layers, or colored shapes on uni-pattern layers. As the *lib.setting.check_mask_constraints* is set to *strict*, the current command will error out.

If the reported library is a library cell library, then the check is performed on it directly. If the reported library is a design library, then the check is performed on all the reference libraries of it.

What Next

Either rebuild the reported library, or set *lib.setting.check_mask_constraints* to *loose* or *none*.

Feedback

LIB-163

(error) Mixture use of library configuration and fusion library not supported.

Description

This message indicates that there is fusion library specified for library configuration. This is not allowed.

What Next

Either use library configuration for all reference libraries, or create fusion libraries for all reference libraries. The mixture use of them are not supported.

LIB-164

(error) This library contains advanced technology not supported by this product. Please contact your Synopsys representative for more information.

Description

This library contains advanced technology not supported by this product.

What Next

Please contact your Synopsys representative for more information.

LIB-165

(error) Pane id %d is invalid for cell library '%s'.

Description

The pane id specified for the *-paneId* option is invalid. It is greater than the maximum pane id of the given cell library.

What Next

If the pane id was specified at the shell directly, please specify a valid pane id and try again. The maximum pane id can be got from the output of the *report_lib* command.

If *-paneId* option was not used for setting the lib data, then this error message must be reported during open a design library. It means the cell library had been changed since last time the lib data was set with the design library. There are fewer panes in the new cell library. And most likely, the change of the cell library, as the reference library of the design library, didn't through the *set_ref_libs* command. Please re-run the lib data setting with the design library to fix the error. After saving the design library again, it should have no this kind of error messages when open the design library next time.

Feedback

LIB-166

(error) Cannot find the default technology file.

Description

This message indicates that the default technology file cannot be found. The default technology file "default.tf" should be installed at <install_directory>/auxx/lc.

What Next

Check why the "default.tf" is missing from <install_directory>/auxx/lc.

LIBCHK

LIBCHK-001

(warning) Missing option %s when %s is specified.

Description

This message occurs when an option is specified but its associated option is missing. -optimization {power} requires -criteria {lvth_groups=lvt_name_list} to be associated with it. Since -all and -logic include -optimization {power}, when you specify -all or -logic, you also need to specify -criteria. -tolerance {type relative_tolerance absolute_tolerance} should be specified together. If only the type is specified without tolerance value, this message also occurs. If the associated option is not specified, the check as specified by the primary option will be ignored

What Next

Please specified the missing option.

Examples

```
Warning: Missing option -criteria {lvth_groups=lvt_name_list} when -all
 is specified. (LIBCHK-001)
```

LIBCHK-002

(warning) Specified variable or option '%s' ignored.

Description

This message occurs when an option or its value or variable is specified incorrectly in syntax or location, and will be ignored. To report line numbers, please specify set lc_check_lib_keep_line_number true before read_lib. When -compare and other options

Feedback

such as -validate are specified either in one command or separate, and there is only one library exists, this message also occurs.

What Next

If you set lc_check_lib_keep_line_number true, but still do not see line numbers reported, please make sure this variable is set before read_lib command and the library, if specified in -logic_library_name, is exactly the same as the File name with Path name when you see after issuing read_lib and list_lib or do not explicitly specify the library in -logic_library_name option in which case, the runtime library will be checked. If the group/attribute name specified in -group_attribute option is not found in the library, it will be ignored. To compare libraries, more than one libraries should be specified.

Examples

```
Warning: Specified variable or option 'lc_check_lib_keep_line_number'
 ignored. (LIBCHK-002)
```

LIBCHK-003

(warning) No check done for logic library checking. Please specify valid options and libraries.

Description

This message occurs when any of the following occurs: 1) No logic library specified or available at runtime for logic related checks including default checks. 2) Less than 2 libraries specified or available at runtime for -compare option. 3) Invalid cell names specified in -cells option. 4) Invalid voltage_name in create_scaling_lib_group -exclude_voltage_names option. 5) -logic_vs_physical specified but -logic_library_name not specified or no logic library available at runtime.

What Next

Please specify the missing libraries or option based on above scenario.

Examples

```
Warning: No check done for logic library checking. Please specify valid
 options and libraries. (LIBCHK-003)
```

LIBCHK-100

(warning) %s data found. Please refer to %s.

Feedback

Description

This message occurs when there are more serious issues that are found in the checking result listed in the table that follows. It redirects you to the message ID on next line that will give you detailed information.

What Next

Please refer to the man page of the recommended message ID for details.

Examples

```
Warning: Mismatched data found. Please refer to LIBCHK-110. (LIBCHK-100)
```

LIBCHK-101

(error) %s data found. Please refer to %s.

Description

This message occurs when there are more serious issues are found in the checking result listed in the table that follows. It redirects you to the message ID on next line that will give you detailed information.

What Next

Please refer to the man page of the recommended message ID for details.

Examples

```
Error: Mismatches data found. Please refer to LIBCHK-212. (LIBCHK-101)
```

LIBCHK-110

(information) List of cells with missing views

Description

This message is for reporting cells with missing views in physical library. All the physical cells with CEL/FRAM view missing will be reported in this table. In this report table, there are three columns: Cell name, CEL and FRAM. In the table, the CEL and FRAM columns list the cell name:version number. An X marks the view that is missing.

What Next

If FRAM view is missing, it is more critical that missing CEL view. You should use extract BPV command extract_blockage_pin_via to generate FRAM view.

Feedback

Examples

```
List of cells with missing views
-------------------------------------------------------------------------
--------
Cell name                       CEL                     FRAM
-------------------------------------------------------------------------
--------
dffs_1                          dffs_1:2                X
tiehi_1                         tiehi_1:2               X
-------------------------------------------------------------------------
--------
```

Examples

```
Information: List of cells with missing views (LIBCHK-110)
```

LIBCHK-111

(warning) List of cells with mismatched views

Description

This message is for reporting cells with mismatched veiwewss in physical library. All the physical cells with CEL/FRAM view mismatched will be reported in this table. In this report table, there are five columns: Cell name, CEL Version, CEL Modified time, FRAM Version and FRAM Modified time. the CEL version and FRAM version columns list the version numbers, and the CEL and FRAM modified time columns list the time when the view was last modified. If a cell has an earlier FRAM view than its CEL view, it is marked as mismatched. The time checked is the internal view creation or modification time in the Milkyway database, not the UNIX time. No mismatch check is performed on the cell content.

What Next

If a cell has an earlier FRAM view than its CEL view, please chec is its FRAM view is not updated. You may need to regenerate FRAM view by extracting BPV. If you read FRAM views from the LEF and then stream in CEL views, the views are shown as mismatched. You can ignore this report in this case.

Examples

```
List of cells with mismatched views
-------------------------------------------------------------------------
--------
                              CEL          CEL           FRAM          FRAM
Cell name                  Version   Modified time     Version   Modified
 time
-------------------------------------------------------------------------
--------
```

```
FILL8                          2    Oct 24 19:17:9 2000    1    Oct 24
 19:14:33 2000
FILL4                          2    Oct 24 19:17:9 2000    1    Oct 24
 19:14:33 2000
ANTENNA                        2    Oct 24 19:17:23 2000   1    Oct 24
 19:14:43 2000
--------------------------------------------------------------------------
--------
```

Examples

```
Warning: List of cells with mismatched views (LIBCHK-111)
```

LIBCHK-112

(information) List of cells with same names

Description

This message is for reporting cells with same names among the specified main or design library and all physical reference libraries linked to the specified library. All the physical cells with same name will be reported in this table. In this report table, there are two columns: Cell name and Library list in precedence order. If there are cells with the same name in multiple reference libraries, the tool uses the first cell in the reference control file and ignores the remaining cells. This option does not check naming among the logic libraries.

What Next

This is information only. If there are cells with the same name in multiple reference libraries, the tool uses the first cell in the reference control file and ignores the remaining cells. This option does not check naming among the logic libraries.

Examples

```
List of cells with same names
-------------------------------------------------------------
   Cell Name                 Library list in precedence order
-------------------------------------------------------------
   XOR3                      mainlib ref ref1 ref3 ref5
   DFF                       ref ref1 ref3
-------------------------------------------------------------
```

Examples

```
Information: List of cells with same names (LIBCHK-112)
```

LIBCHK-113

(information) List of signal EM data

Feedback

Description

This message is for reporting signal EM data for routing layers in physical library. All EM data will be reported in this table. In this report table, there are three columns: Layer name, Current model and Model type. If no signal EM data at all in the library, it will not print the table but print a message: The library is missing signal EM data.

What Next

If the signal EM data is not complete, for example, it exists only in some layers but not all layers, you should check and reload the missing data.

Examples

```
List of signal EM data (LIBCHK-113)
-------------------------------------------------------------
     Layer name      Current model       Model type
-------------------------------------------------------------
     METAL1              peak                table
     METAL1              rms                 table
     METAL1              average             table
-------------------------------------------------------------
```

Examples

```
Information: List of signal EM data (LIBCHK-113)
```

LIBCHK-114

(warning) The library is missing signal EM data.

Description

This message occurs when there is no signal EM data for routing layers at all in the physical library.

What Next

For flows for and EM analysis with different temperature corners, signal EM data is required. You should check and reload the data into the physical library.

Examples

```
Warning: The library is missing signal EM data. (LIBCHK-114)
```

LIBCHK-115

(information) List of antenna rules

Feedback

Description

This message is for reporting antenna rules in the layers in the specified main library. In this report table, there are six columns: Layer name, Mode, Diode mode, Default metel ratio, Default cut ratio and Max ratio.

What Next

This is information only.

Examples

```
List of antenna rules
-------------------------------------------------------------------------
                                      Default     Default
  Layer Name    Mode   Diode mode   metal ratio  cut ratio   Max ratio
-------------------------------------------------------------------------
  M1             1         3           500.00      20.00      500.00
  M2             1         3           500.00      20.00      500.00
-------------------------------------------------------------------------
```

Examples

```
Information: List of antenna rules (LIBCHK-115)
```

LIBCHK-116

(warning) The library is missing antenna rules.

Description

This message occurs when no antenna rules exist in the physical library.

What Next

Please check and load the antenna rule file after FRAM view is created.

Examples

```
Warning: The library is missing antenna rules. (LIBCHK-116)
```

LIBCHK-117

(warning) List of cells missing antenna property

Description

This message is for reporting missing antenna property for cells in physical library. All the cells that are missing antenna property will be reported in this table. In this table, it lists cell names and pin names missing the antenna property and the missing property type. If an input pin is missing the gate size, it is counted as missing the property. If an output pin is

Feedback

missing diode pro tection, it is counted as missing the property. If a macro is missing the hierarchical antenna property, then it is counted as missing the property. It is considered good practice to specify hierarchical antenna properties for macros.

What Next

For antenna fix, please check and load the antenna properties (CLF) after FRAM view is created.

Examples

```
List of cells missing antenna property
------------------------------------------------------------------------
--------
   Cell name             Cell type  Missing property     Pin name(s)
------------------------------------------------------------------------
--------
   TLATNTSCAX1           StdCell    DiodeProt            ECK
   TLATNTSCAX4           StdCell    DiodeProt            ECK
   XOR2X4                StdCell    DiodeProt            Y
   XOR2XL                StdCell    DiodeProt            Y
------------------------------------------------------------------------
--------
```

Examples

```
Warning: List of cells missing antenna property (LIBCHK-117)
```

LIBCHK-118

(information) List of cells with rectilinear boundaries

Description

This message is for reporting cells with rectilinear boundaries in physical library. All cells with rectilinear boundaries will be reported in this table. In this report table, there are four columns: Cell name, Cell type, Number of points and Coordinate.

What Next

This is information only. No further action is required.

Examples

```
List of cells with rectilinear boundaries
------------------------------------------------------------------------
  Cell Name    Cell type  Number of points                    Coordinate
------------------------------------------------------------------------
  datapath     Macro            17     ( 78.750,   0.000) ( 78.750,
 490.760)
                                       ( 44.435, 490.760) ( 44.435,
 915.035)
```

```
                                        ( 27.440, 915.035)
 ( 27.440,1143.605)
                                        (  0.000,1143.605) (
  0.000,1313.200)
                                        (677.295,1313.200)
 (677.295,1143.605)
                                        (649.855,1143.605) (649.855,
 915.035)
                                        (632.860, 915.035) (632.860,
 490.760)
                                        (598.545, 490.760) (598.545,
 0.000)
                                        (  0.017,   0.000)
-------------------------------------------------------------------------
```

Examples

```
Information: List of cells with rectilinear boundaries (LIBCHK-118)
```

LIBCHK-119

(information) List of physical only cells

Description

This message is for reporting physical-only cells in the physical library. In Milkyway, physical-only cells are defined as FillerCell: Filler cell IOPadCell: Pad filler (IO Pad) cell CornerCell: Corner (pad) cell ChipCell: Chip cell FlipChipPadCell:Flip chip pad (bump) cell CoverCell: Cover cell TapCell: Tap cell PGPinOnlyCell: PG-pin-only cell (containing only PG ports) In this report table, there are three columns: Cell name, Cell type and Physical library.

What Next

Please verify that the cell types of the physical only cells are marked correctly in the physical library.

Examples

```
List of physical only cells
-------------------------------------------------------------------------
Cell name                  Cell type            Physical library
-------------------------------------------------------------------------
FILL8                      FillerCell           tsmc18_cg_LM
FILL64                     FillerCell           tsmc18_cg_LM
-------------------------------------------------------------------------
```

Examples

```
Information: List of physical only cells (LIBCHK-119)
```

Feedback

LIBCHK-120

(information) List of main and reference libraries

Description

This message is for reporting each libraries (main and reference physical libraries) and their full path locations, along with unit tile name and size. In this report table, there are four columns: Library name, Path, Unit tile and Tile size.

What Next

This is information only. No further action is required. Note: if tile patterns listed in List of tile patterns are not consistent with tiles in List of main and reference libraries, it is recommended that users redo library prep to use same tile. Please refer to example 2.

Examples

```
Example 1:
Information:         List of main and reference libraries (LIBCHK-120)
------------------------------------------------------------------------
---------
Library name       Path                                        Unit tile
 Tile size
------------------------------------------------------------------------
---------
tsmc18_cg_LM       /remote/reg_designs/LIB_CENTER/180nm/san unit
 0.660x5.040
------------------------------------------------------------------------
---------

Example 2:
Information:         List of main and reference libraries(LIBCHK-120)
------------------------------------------------------------------------
---------
Library name       Path                                        Unit tile
 Tile size
------------------------------------------------------------------------
---------
cb18os120_unit010  /remote/dept5532b/styao/design              unit010
 0.560x5.600
------------------------------------------------------------------------
---------

                List of tile patterns
------------------------------------------------------------------------
--------
 Tile pattern     Unit tile     Location     Orientation          Tile
 size
 1                   unit         (0,0)    R0|R0_MX
 0.560x0.560
```

Feedback

```
 2                    unit          (-0.28,0)R0|R0_MX
 0.560x0.560
-------------------------------------------------------------------------
--------
```

Examples

```
Information: List of main and reference libraries (LIBCHK-120)
```

LIBCHK-121

(information) List of placement properties

Description

This message is for reporting placement properties for cells in physical library. In this report table, there are seven columns: Cell name, PR boundary, Cell Height, Symmetry, Orientation, Tile pattern and Remarks. PR boundary is represented by its lower left and upper right coordinates. Cell height is relative to the unit tile height, such as 1xH for single height. Cell symmetry includes: rxy - RXYsymmetry xy - XYsymmetry y - Ysymmetry x - Xsymmetry r - Rsymmetry a - Asymmetry Cell orientation includes: R0_MX R0_MY R180 R90_MY R90 R270 R90_MX Number in Tile pattern denotes the serial number in the associated List of tile patterns table. Remarks notes that the PR boundary mismatches the tile pattern. For macros, this table reports cell boundary and height. The unit tile size is reported in the format of width x height.

What Next

For standard cells, if mismatches are found between PR boundary and the tile pattern (Mismatch in Remarks column), please use the cmSetMultiHeightProperty command to set tile patterns for multi-height cells.

Examples

```
List of tile patterns
-------------------------------------------------------------------------
--------
 Tile pattern     Unit tile     Location     Orientation          Tile
 size
 1                    unit          (0,0)      R0|R0_MX
 0.660x5.040
-------------------------------------------------------------------------
--------

         List of placement properties
 -----------------------------------------------------------------------
--------------------
 Cell name      PR boundary       Height  Symmetry  Orientation
 Tile pattern  Remarks
```

Feedback

```
 ------------------------------------------------------------------------
--------------------
 TLATNTSCAX1     (0,0)(9.24,5.04)      1xH  xy         R0|R0_MX           1
 NOR2X1          (0,0)(1.98,5.04)      1xH  xy         R90_MY             1
                        Mismatch
------------------------------------------------------------------------
--------------------
```

Examples

```
Information: List of placement properties (LIBCHK-121)
```

LIBCHK-122

(information) List of routing properties

Description

This message is for reporting routing properties for routing layers in physical library. All routing properties for layers will be reported in this table. In this report table, there are six columns: Layer, Preferred direction, Track direction, Offset, Pitch and Remarks. Remarks column denotes if the routing property on this layer has issues. If no issues are found, you will see OK in this Remarks; otherwise, it will note what issue is found, for example, if the offset is 0.46*pitch, which is neither 0 nor half pitch, offset=0.46pitch will be noted.

What Next

If remarks other than OK are noted, such as offset=0.46pitch, please check the issue and correct it. In the case of offset!=0.5*pitch, please reset the offset to be either 0 or half pitch. If blanks are left in Preferred direction, that denotes the preferred routing direction has not been set. Please define the preferred routing direction. If less than three routing layers are listed in this table, it is an error. Please check technology file and if some routing layers are missing, define them in the technology file and reload it.

Examples

```
List of routing properties
------------------------------------------------------------------------
              Preferred      Track
   Layer      direction    direction   Offset    Pitch   Remarks
------------------------------------------------------------------------
   METAL1         H            H       0.280     0.560   OK
   METAL2         V            V       0.330     0.660   OK
   METAL3                      H       0.280     0.560   OK
   METAL4                      V       0.330     0.660   OK
   METAL5                      H       0.280     0.610   offset=0.46pitch
   METAL6                      V       0.380     0.950   offset=0.40pitch
------------------------------------------------------------------------
```

Feedback

Examples

```
Information:  List of routing properties (LIBCHK-122)
```

LIBCHK-123

(information) List of cell and pin properties

Description

This message is for reporting cell and pin properties for cells in physical library. In this report table, there are six columns: Cell name, Cell type, Pin name, Pin direction, Pin type and Multi PG. If a cell has either multiple power pins or multiple ground pins, multiPG will be noted in the last column. At the end of the table, it also reports the number of cells with multiple P/G pins.

What Next

If there is not any power or ground pins for a cell, it is an error. Please check the cell and may need to rerun extract BPV.

Examples

```
List of cell and pin properties
------------------------------------------------------------------------
------------
   Cell name            Cell type     Pin name      Pin direction  Pin
 type  Multi PG
------------------------------------------------------------------------
------------
   XOR2XL               StdCell       Y             Output         signal
                                      VSS                          ground
                                      B             Input          signal
                                      A             Input          signal
                                      VDD                          power
   NAND4BBX1            StdCell       BN            Input          signal
                                      Y             Output         signal
                                      VSS                          ground
                                      C             Input          signal
                                      AN            Input          signal
                                      D             Input          signal
                                      VDD                          power
------------------------------------------------------------------------
------------
```

Examples

```
Information:  List of cell and pin properties (LIBCHK-123)
```

Feedback

LIBCHK-124

(warning) List of pins without optimal routeability

Description

This message is for reporting pins without optimal routeability in physical library. All pins without optimal routeability will be reported in this table. Optimal routeability means pin's on-track accessibility of defined wire tracks. It also reports the total number of pins without optimal on-track routability and lists pin names, directions, layers, and tracks for each cell of this issue. In the track column, an H denotes that the pin is not accessible on a horizontal track, a V denotes the pin is not accessible on a vertical track, and H&V denotes that the pin is not accessible on both horizontal and vertical tracks.

What Next

If a pin is reported as not accessible on track, the pin might be routed by off-track wire during detailed routing. If too many pins do not have any on-track routability, adjust the offset values of the wire track (0 or half pitch preferred) and run the the create_lib_track command to reduce the number of pins without optimal accessibility. If routability checking is not successful, the cause may be no unit tile.

Examples

```
List of pins without optimal routeability
-------------------------------------------------------------
   Cell Name          Pin Name  Layer     Direction   Track
-------------------------------------------------------------
   TLATNSRX2          D         METAL1    Input       H&V
   SDFFSRHQX2         SE        METAL1    Input       H&V
   NOR4BBXL           C         METAL1    Input       H&V
   DFFRHQX1           D         METAL1    Input       H&V
   AND4X2             C         METAL1    Input       H&V
-------------------------------------------------------------
```

Examples

```
Warning: List of pins without optimal routeability (LIBCHK-124)
```

LIBCHK-125

(warning) List of cells with DRC violation

Description

This message is for reporting cells with DRC violation in physical libraries. All cells with DRC violation will be reported in this table. It checks design rules such as wire minWidth, minEdgeLength, minEnclosedArea, minSpacing, cutWidth, cutSpacing, and minEnclosure.

Feedback

In this report table, there are three columns: Cell Name, Cell type and Error cell. Error cell contains detailed information for DRC violation of the FRAM view cell.

What Next

Check the error cells for details of DRC violations. If a cell has DRC violation, it may not be used in the design without correction.

Examples

```
List of cells with DRC violation
-----------------------------------------------------------
     Cell name                    Cell type      Error cell
-----------------------------------------------------------
     ONEPIN                       Standard       ONEPIN.err
-----------------------------------------------------------
```

Examples

```
Warning: List of cells with DRC violation (LIBCHK-125)
```

LIBCHK-126

(warning) List of cells with metal density error

Description

This message is for reporting cells with metal density error in physical library. All cells with metal density error will be reported in this table. It checks macro metal density data for the cells, i.e. it checks if a cell has at least one of the following errors: (1) Metal density data in CEL view and FRAM view are inconsistent (2) Metal density windows do not cover the entire area on the layer In this report table, there are three columns: Cell Name, Inconsistency and the layer on which the density windows do not cover the entire area. Y denotes Yes or Inconsistency exists and N denotes No consistency.

What Next

If the density windows do not cover the entire area, you may need to add metal fill or smooth metal wire density. If metal density data in CEL view and FRAM view are inconsistent, please check FRAM vs. CEL view.

Examples

```
List of cells with metal density error
-------------------------------------------------------------------
   Cell name          Inconsistency       Not cover entire area
-------------------------------------------------------------------
   ADDFX1MTR          Y                   M4
   OA21X1MTR          N                   M1
                                          M2
-------------------------------------------------------------------
```

Feedback

Examples

```
Warning: List of cells with metal density error (LIBCHK-126)
```

LIBCHK-130

(information) Physical library checks FAILED.

Description

This message is a concluding statement after physical checks are done. When any issue is found, for example, no physical libary to check, or no cells need to check, this message will occur. Otherwise, it reports Physical library checks PASSED.

Examples

```
Information: Physical library checks FAILED. (LIBCHK-130)
```

What Next

You are advised to go back to the check report to see inconsistent results and resolve them as directed by the associated LIBCHK and FRAM man pages.

If you see the below message IDs in the check report, go to the related messages for details in

```
LIBCHK-112
LIBCHK-114
LIBCHK-116
LIBCHK-125
FRAM-010
FRAM-014
FRAM-015
FRAM-018
FRAM-019
FRAM-020
FRAM-022
FRAM-027
FRAM-028
FRAM-029
FRAM-030
FRAM-031
FRAM-033
FRAM-034
FRAM-039
FRAM-055
FRAM-056
FRAM-058
FRAM-062
FRAM-064
FRAM-070
FRAM-075
```

Feedback

```
FRAM-078
FRAM-079
FRAM-080
FRAM-081
```

Any of the related LIBCHK FRAM messages will lead to the conclusion of some issues found during the checking.

See Also

- LIBCHK-112
- LIBCHK-114
- LIBCHK-116
- LIBCHK-125

LIBCHK-140

(warning) List of inconsistent ICC2 and %s attributes in %s class

Description

This table lists ICC2 and MW/LEF/GDS attributes with inconsistent values in lib_cell/ mw_cel class. In this table, there are five columns: Library, Cell name, Attribute name, ICC2 value and MW/LEF/GDS value.

Examples

```
Warning: List of inconsistent ICC2 and MW attributes in lib_cell class
 (LIBCHK-140)
-------------------------------------------------------------------------
----------------------
Library                   Cell name           Attribute name      ICC2
 value      MW value
-------------------------------------------------------------------------
----------------------
testlib                   AND2X1_LVT          allowable_orientation
                                                                    {R0
 R180 MX MY} {N FN FS}
testlib                   AND2X1_LVT          area
 2.03315   2.04111
-------------------------------------------------------------------------
----------------------
```

LIBCHK-141

(warning) List of inconsistent ICC2 and %s attributes in %s class

Feedback

Description

This table lists ICC2 and MW/LEF/GDS attributes with inconsistent values in port/lib_pin class. In this table, there are five columns: Cell name, Object name, Attribute name, ICC2 value and MW/LEF/GDS value.

Examples

```
Warning: List of inconsistent ICC2 and MW attributes in port class
 (LIBCHK-141)
------------------------------------------------------------------------
----------------------
Cell name                    Object name         Attribute name     ICC2
 value      MW value
------------------------------------------------------------------------
----------------------
XOR3X2_LVT                   A1                  direction          input
  inout
XOR3X2_LVT                   A1                  is_diode           false
  true
------------------------------------------------------------------------
----------------------
```

LIBCHK-142

(warning) List of inconsistent ICC2 and %s attributes in %s class

Description

This table lists ICC2 and MW attributes with inconsistent values in terminal class. In this table, there are five columns: Cell name, Object name, Attribute name, ICC2 value and MW value. users can find the MW value from import_icc_fram_lib.

Examples

```
Warning: List of inconsistent ICC2 and MW attributes in terminal class
 (LIBCHK-142)
------------------------------------------------------------------------
----------------------
Cell name                    Object name         Attribute name     ICC2
 value      MW value
------------------------------------------------------------------------
----------------------
XOR3X2_LVT                   A1                  access_direction    all
XOR3X2_LVT                   A2                  is_fixed
 false   true
------------------------------------------------------------------------
----------------------
```

Feedback

LIBCHK-143

(warning) List of inconsistent ICC2 and %s attributes in %s class

Description

This table lists ICC2 and MW attributes with inconsistent values in shape class. In this table, there are five columns: Cell name, Object name, Attribute name, ICC2 value and MW value. Users can find the MW value from import_icc_fram_lib.

Examples

```
Warning: List of inconsistent ICC2 and MW attributes in shape class
 (LIBCHK-142)
-------------------------------------------------------------------------
--------------------------
Cell name                    Object name         Attribute name      ICC2
 value     MW value
-------------------------------------------------------------------------
--------------------------
HSBULT08_AOI21_MMY2_4        RECT_159_4          owner               B
           B_1
HSBULT08_AOI21_MMY2_4        RECT_159_5          owner               B_1
           B_2
HSBULT08_AOI21_MMY2_4        RECT_2030_6 / RECT_2030_0
                                                 mask_constraint
 mask_two       no_mask
HSBULT08_AOI21_MMY2_4        RECT_2030_7 / RECT_2030_1
                                                 mask_constraint
 mask_two       no_mask
-------------------------------------------------------------------------
----------------------
```

LIBCHK-144

(warning) List of inconsistent ICC2 and %s attributes in %s class

Description

This table lists ICC2 and MW attributes with inconsistent values in routing_blockage class. In this table, there are five columns: Cell name, Object name, Attribute name, ICC2 value and MW value. Users can find the MW value from import_icc_fram_lib.

Examples

```
Warning: List of inconsistent ICC2 and MW attributes in routing_blockage
 class (LIBCHK-142)
-------------------------------------------------------------------------
--------------------------
Cell name                    Object name         Attribute name      ICC2
 value     MW value
```

Feedback

```
-------------------------------------------------------------------------
--------------------------
HSBULT08_AOI21_MMY2_4        RB_1               mask_constraint
 mask_one       no_mask
HSBULT08_AOI21_MMY2_4        RB_7 / RB_2        mask_constraint
 mask_two       no_mask
HSBULT08_AOI21_MMY2_4        RB_8 / RB_3        mask_constraint
 mask_two       no_mask
-------------------------------------------------------------------------
----------------------
```

LIBCHK-210

(information) List of cells missing in logic library

Description

This message is for reporting missing cells in logic library during logic vs. physical library checking. All the physical cells except physical only cells that are missing in logic library will be reported in this table. In this report table, there are three columns: Cell name, Cell type and Physical library. Cell type includes Core, Pad, InputPad, OutputPad, PowerPad, SpacerPad, and Unknown.

What Next

If some cells are found missing in specified logic library (.db), please check if you have not specified all the db files since logic cells may exist in different db files while the physical cells exist in one Milkyway library.

Examples

```
List of cells missing in logic library
-------------------------------------------------------------------------
Cell name                  Cell type             Physical library
-------------------------------------------------------------------------
AND2                       Core                  phys_lib
NOR1                       Core                  phys_lib
-------------------------------------------------------------------------
```

Examples

```
Information: List of cells missing in logic library (LIBCHK-210)
```

LIBCHK-211

(warning) List of cells missing in physical library

Feedback

Description

This message is for reporting missing cells in physical library during logic vs. physical library checking. All the logic cells that are missing in physical library will be reported in this table. In this report table, there are three columns: Cell name, Cell type and Logic library. The cell type includes pad_cell, non pad_cell and unknown. If no missing cells, no table will be printed out, but Number of cells missing in logic library: 0 (out of total) will be printed out.

What Next

If some cells are found missing in specified physical library (Milkyway library), please check if you have complete Milkyway library specified since physical cells may exist in different Milkyway library directories. If the cells are used in the design, the physical cells have to exist in the physical library that you are using. If the cells are not expected to be part of the physical library, then the incoming netlist must not have any of the missing cells. For example, by setting the dont_use attribute during synthesis.

Examples

```
Number of cells missing in physical library:   2 (out of 498)
   List of cells missing in physical library
-------------------------------------------------------------------------
Cell name                  Cell type            Logic library
-------------------------------------------------------------------------
gaard21                    non pad_cell         memory.lib
gaard22                    non pad_cell         memory.lib
-------------------------------------------------------------------------
```

Examples

```
Warning: List of cells missing in physical library (LIBCHK-211)
```

LIBCHK-212

(warning) List of pins missing in %s library

Description

This message is for reporting missing pins in logic (or physical) cells during logic vs. physical library checking. All the physical(or logic) pins that are missing in logic (or physical) cells will be reported in this table. In this report table, there are four columns: Physical(Logic) library, Cell name, Pin name and Pin direction It also checks pg_pin's in logic library vs. PG pins in physical library if there are pg_pin's in the logic library, and reports them in the same table.

What Next

If some signal pins are found missing in logic cells, it is a real issue and therefore an Error message LIBCHK-101 will occur to direct you to correct the cells that are missing these

Feedback

pins in the logic library. If pg_pins are missing in the logic library, it indicates that the logic library is not pg_pin based, and for UPF flow you need to use add_pg_pin_to_db utility to convert it into pg_pin based db.

Examples

```
List of pins missing in logic library
------------------------------------------------------------------------
----
Physical library        Cell name       Pin name        Pin direction
------------------------------------------------------------------------
----
NLC13IOplLib_3v         pnl_go          A                       Output
------------------------------------------------------------------------
----
```

Examples

```
Warning: List of pins missing in logic library (LIBCHK-212)
```

LIBCHK-212e

(error) List of signal and PG pins missing in %s library

Description

This message reports missing signal pins and pg_pins in logical (or physical) cells in logic vs. physical library checking. All the logical (or physical) pins that are missing in physical (or logical) cells will be reported in this table. It also reports same name physical MUSTJOIN pins if defined in DB as such pins are not logical signal pins, which indicates the pins should be either removed from logic library or added in physical library as logical signal pins. In this report table, there are four columns: Physical(or Logic) library, Cell name, Pin name and direction It also checks pg_pin's in logic library and PG pins in physical library, and reports them in the same table.

What Next

If some signal pins are found missing in logic cells, it is a real issue and you need to correct the inconsistency. If pg_pins are missing in the logic library, it indicates that the logic library is not pg_pin based. UPF flow requires pg_pin based library.

In fusion library, when you see

missing logical pins reported in LIBCHK-212e

without LIBCHK-212e table, please run one of the following to get detailed report in the table format. 1) check_fusion_lib 2) set_app_options -name fusion_lib.check_fusion_lib_verbose -value true before create_fusion_lib 3) report_check_library_records autofix0.db3 -libchk_codes LIBCHK-212e where autofix0.db3 is located in fusion lib dir or current dir.

Feedback

Examples

```
Error: List of signal and PG pins missing in logic library (LIBCHK-212e)
-------------------------------------------------------------------------
----
Physical library        Cell name       Pin name        direction
-------------------------------------------------------------------------
----
NLC13IOplLib_3v         pnl_go          A               in
av16_lib                a16_fillprog_a2 A.1             in
-------------------------------------------------------------------------
----

Number of cells missing pins in logic library:   2
```

Examples

```
Warning: List of signal and PG pins missing in logic library
 (LIBCHK-212e)
```

LIBCHK-213

(error) List of pins mismatched in logic and physical libraries

Description

This message is for reporting pins mismatched in either direction or pin type between the logic and physical cells during logic vs. physical library checking. All the mismatched pins will be reported in this table. In this report table, at the header of this table, the logic and physical library full path file names are listed followed by the table contents with four columns: Cell name, Pin name, Pin direction and Pin type. In Pin direction and Pin type columns, it lists values for both logic and physical libraries.

What Next

If some pins are found mismatched in either pin direction or pin type between logic and physical cells, it is a real issue and you need to correct the cells with this issue in either the logic or physical library or both.

Examples

```
List of pins mismatched in logic and physical libraries
Logic library:    NLC13IOplLib_3v_fast132Vm40C
Physical library: /remote/fae99/smoot/TO_XIREN/NLC13IOplLib_3v
-------------------------------------------------------------------------
----
                                        Pin direction       Pin type
Cell name                   Pin name    Logic   Physical    Logic
 Physical
-------------------------------------------------------------------------
----
```

Feedback

```
pnl_go                          VSSO        output  Output      signal
 ground
                                GND         input   Input       signal
 ground
                                VDDP        input   Input       signal
 power
-------------------------------------------------------------------------
----
```

Examples

```
Error: List of pins mismatched in logic and physical libraries
 (LIBCHK-213)
```

LIBCHK-213w

(warning) List of pins mismatched in logic and physical libraries

Description

This message is for reporting pins mismatched in either direction or pin type between the logic and physical cells during logic vs. physical library checking. All the mismatched pins will be reported in this table. In this report table, at the header of this table, the logic and physical library full path file names are listed followed by the table contents with four columns: Cell name, Pin name, Pin direction and Pin type. In Pin direction and Pin type columns, it lists values for both logic and physical libraries.

What Next

If some pins are found mismatched in pin type between logic and physical cells, i.e. pg_pins in physical library modelled as signal pins in logical library, add_pg_pin_to_db/lib utility may correct it. Otherwise, if some pins are found mismatched in either pin direction or pin type between logic and physical cells, it is a real issue and you need to correct the cells with this issue in either the logic or physical library or both.

Examples

```
List of pins mismatched in logic and physical libraries
Logic library:    NLC13IOplLib_3v_fast132Vm40C
Physical library: /remote/fae99/smoot/TO_XIREN/NLC13IOplLib_3v
-------------------------------------------------------------------------
----
                                        Pin direction       Pin type
Cell name                   Pin name    Logic   Physical    Logic
 Physical
-------------------------------------------------------------------------
----
pnl_go                          VSSO        output  Output      signal
 ground
                                GND         input   Input       signal
 ground
```

```
                              VDDP        input   Input       signal
 power
-------------------------------------------------------------------------
----
```

Examples

```
Warning: List of pins mismatched in logic and physical libraries
 (LIBCHK-213w)
```

LIBCHK-214

(information) List of bus naming styles

Description

This message is for reporting bus delimiters in logic and physical libraries. There are three columns in this report table: Library name, Library type and Bus naming style where Library type is either physical library or logic library. If there is no bus delimiter in the library, the field is blank in the report. To report bus naming styles, please set -bus_delimiter to set_check_library_options command. it is often true that logic libraries do not specify the bus delimiter.

What Next

This is information only. No further action is needed.

Examples

```
List of bus naming styles
-------------------------------------------------------------------
Library name                 Library type        Bus naming style
-------------------------------------------------------------------
tsmc18_xx                                        Physical library
 _<%d>
memory.lib                   Logic library
-------------------------------------------------------------------
```

Examples

```
Information: List of bus naming styles (LIBCHK-214)
```

LIBCHK-215

(warning) List of cells with cell_footprint attribute

Description

This message is to check that the cell PR boundary or Cell boundary for Macro in the physical library is consistent among a class of cells with the same cell_footprint attribute

Feedback

specified in the logic library. This option reports cell names and their PR boundaries grouped by cell_footprint string.

What Next

If the cells are used in the design, please check their PR boundaries or cell boundaries for inconsistency. For example, if the PR boundaries of the cells with the same cell_footprint are different, you can not use them during optimization by swapping these cells.

Examples

```
List of cells with cell_footprint attribute
-------------------------------------------------------------------
Footprint  Logic library name  Cell name           PR boundary
-------------------------------------------------------------------
add42      slow                CMPR42X1            (0,0)(22.44,5.04)
           slow                CMPR42X2            (0,0)(26.4,5.04)
addf       slow                ADDFX1              (0,0)(13.86,5.04)
-------------------------------------------------------------------
```

Examples

```
Warning: List of cells with cell_footprint attribute (LIBCHK-215)
```

LIBCHK-216

(warning) List of cells with inconsistent area

Description

This message is to check the area attribute of cells in the logic library versus the actual area by cell PR boundary in the physical library. For comparison, the ratio of a stdCell PRBoundary in the rectangle (or Macro CellBoundary in the polygon) in the FRAM view to the cell area in the .db is used. If the ratio is the same for all the cells in the library, the cell areas are considered to be consistent. Otherwise, if the ratio for a cell deviates from the normal or average ratio for this library by a margin of 5%, it is counted as an inconsistent area. and will be included in the table. The average area ratio is calculated by first filtering out cells with the max and min area ratios and then dividing the total area ratios by the number of cells. There is no area check for pad cells. A pad cell is a special cell at the chip boundary with the pad_cell attribute in a logic cell. Pad cells are not checked because they are not used as internal gates and always have an area of 0. To check cell area, please set -cell_area to set_check_library_options command.

What Next

If the cell areas are inconsistent between logic and physical libraries, it will affect timing and placement accurary. The bigger the area deviation, the worse the accuracy and correlation. If the area value is 0 or no area attribute in logic cells, it is more serious and an

Feedback

Error LIBCHK-101 will occur. In this case, you need to correct logic library by adding valid area values to the cells.

Examples

```
Average cell area ratio physical/logic in the library:  0.9978
Number of cells with inconsistent area: 9

     List of cells with inconsistent area
-------------------------------------------------------------------
                                                  Area ratio
Logic library name           Cell name            Phys/logic
-------------------------------------------------------------------
slow                         AFCSHCONX4           0.7966
slow                         AFCSHCONX2           0.8431
slow                         AFHCONX2             0.9167
slow                         AFHCINX4             0
-------------------------------------------------------------------
```

Examples

```
Warning: List of cells with inconsistent area (LIBCHK-216)
```

LIBCHK-217

(warning) List of cells mismatched in logic and physical libraries

Description

This message is for reporting cells mismatched in antenna diode type between the logic and physical cells during logic vs. physical library checking. All the mismatched pins will be reported in this table. In this report table, at the header of this table, the logic and physical library names are listed followed by the table contents with two columns: Cell name, Antenna Diode type. In Antenna Diode type column, it lists values for both logic and physical libraries.

The mapping table between .db and FRAM view is as follows.

Type name in Logic Type name in Physical power_and_ground AntennaDiodeTypePowerAndGround power AntennaDiodeTypePower ground AntennaDiodeTypeGround

What Next

If some cells are found mismatched in antenna diode type between logic and physical cells, command "update_mw_port_by_db -antenna_diode_type" may correct it.

Examples

```
List of cells mismatched in logic and physical libraries
Logic library:    saed90nm_max
```

Feedback

```
Physical library: ./design
-------------------------------------------------------------------------
----
                          Antenna Diode Type
Cell name              Logic               Physical
-------------------------------------------------------------------------
----
cell1                  power_and_ground    AntennaDiodeTypePower
cell2                  ground              missing
-------------------------------------------------------------------------
----
```

Examples

```
Warning: List of cells mismatched in logic and physical libraries
 (LIBCHK-217)
```

LIBCHK-220

(information) Logic library is INCONSISTENT with physical library

Description

This message is a concluding statement after cross checking is done. When any inconsistency, for example, missing cells and mismatched pins, is found during cross checking, this message will occur.

What Next

This is for your information. You need to go back to the check report to see inconsistent results and resolve them as directed by related man pages (LIBCHK).

Examples

```
Information: Logic library is INCONSISTENT with physical library
 (LIBCHK-220)
```

LIBCHK-300

(warning) List of inconsistent library group data

Description

This message is for reporting inconsistent data in logic libraries during logic vs. logic library checking. In the associated report table, it reports inconsistent values of the attributes at the library level. The attributes include. a) library version b) library type (pg_pin based or non-pg_pin based) c) units of timing, power,capacitance, etc. d) trip points e) base curve_x

Feedback

What Next

If some inconsistencies are reported at the library level, please check the libraries and correct them. Some attributes should be consistent cross the libraries. If the libraries are used for timing scaing, trip points should be consistent, and if they are used for UPF or MV flow, the libraries should be pg_pin based.

Examples

```
List of inconsistent library group data
-------------------------------------------------------------------------
-----
Library name              SR60_W_SVT_UHD.db      SR60_S_SVT_UHD.db
-------------------------------------------------------------------------
-----
Voltage unit              1V                     1mV
base_curves/curve_x       "0.2, 0.5, 0.8"        "0.2, 0.5, 0.9"
-------------------------------------------------------------------------
-----
```

Examples

```
Warning: List of inconsistent library group data (LIBCHK-300)
```

LIBCHK-301

(warning) List of incompliant operating conditions

Description

This message is for reporting incompliant operating conditions in the logic libraries. In this report table, nom_voltage, nom_temperature, nom_process and default_operating_conditions of each library are reported. If default_operating_condition is not specified, Library Compiler will add a default name nom_pvt by creating one from nominal PVTs.

What Next

For library scaling, the operating conditions in the same scaling library group should be different in nominal voltage, temperature and/or process. For MCMM and MV/UPF, the nominal voltages should be different under different operating conditions. For -compare, the operating_consitions should be identical. For all others, this is information only. No further action is required. For voltage scaling, it is recommended that the voltages should be no more than 20% apart for good accuracy

Examples

```
List of incompliant operating conditions
-------------------------------------------------------------------------
-----
```

Feedback

```
Library name        SR60_W_SVT_UHD.db           SR60_S_SVT_UHD.db
-------------------------------------------------------------------------
-----
nom P/V/T           3.0/1.0/105.0               1.0/1.4/105.0
default_opcon       "W_105_0.99"                "S_105_1.21"
-------------------------------------------------------------------------
-----
```

Examples

```
Warning: List of incompliant operating conditions (LIBCHK-301)
```

LIBCHK-302

(information) Voltages for library scaling are more than 20%% apart.

Description

This message is for voltage scaling, the voltages should be no more than 20% apart for good accuracy.

What Next

This is information only. However, for better accuracy, it is recommended that the voltages should be no more than 20% apart for voltage scaling.

Examples

```
Information: Voltages for library scaling are more than 20% apart.
 (LIBCHK-302)
```

LIBCHK-303

(warning) Missing libraries in scaling groups

Description

This table reports missing corner libraries in the scaling library group. It indicates the missing libraries by operating conditions (temperature and voltages on rails)

What Next

User needs to add the missing libraries into the group to make a full use of all the libraries in the group for better scaling accuracy.

Examples

```
Warning: Missing libraries in scaling groups  (LIBCHK-303)
-------------------------------------------------
Group name          Temp         VDD1   VDD2
-------------------------------------------------
```

Feedback

```
grp1                -40.0         1.10  1.21
-------------------------------------------------
```

LIBCHK-304

(information) Valid scaling library groups

Description

This table reports valid scaling library groups that meet the library formations. In the case of a complete library list are not specified, it will list the subset of the libraries meeting the formation. In the table, it also reports temperature (T) and voltage (V) ranges and adjacent voltage difference percentage in the group for scaling, or individual T & V values for exact match.

What Next

User can pick any library group from the list in the case of multiple groups are found, but it is recommended to pick the one with maximum number of libraries and maximum scaling dimensions.

Examples

```
Information: Valid scaling library groups (LIBCHK-304)
------------------------------------------------------------------------
----------------
Group name Library list      T range  V range  Max delta V
------------------------------------------------------------------------
----------------
grp1     v1t1.db v2t1.db v1t2.db v2t2.db  -40 to 125 0.9 to 1.2 33.3%
grp2       lib21 lib12 lib13     -40, 125 0.9, 1.2
------------------------------------------------------------------------
----------------
```

LIBCHK-305

(error) Library group '%s' not ready for %s.

Description

The library group is not ready for scaling because of at least one of the following reasons: 1) Library data consistency checks by check_library not passed 2) Originally defined scaling library group is missing some corners or some corner libraries are removed to generate reduced subsets that meet the formation. 3) When a library is specified in multiple library groups by create_scaling_lib_group command, or a user defined lib group has multiple groups in terms of cells. The libraries at this issue can be seen in Library grouping table LIBCHK-308.

The library group is not ready for voltage interpolation if no enough libraries form on one dimension, i.e. one variable rail (e.g. VDD) to interpolate on with other dimensions (e.g. VDD2) fixed. For quadratic interpolation, it needs at least 3 libraries with different voltage values on on rail while others are fixed.

What Next

Also refer to comments in the output script by write_scaling_lib_group, and fix library data consistency and/or add the missing corner libraries if not for -exact_match_only.

For PVT interpolation, please specify enough libraries with >=3 voltage values on a rail/voltage_name while other dimensions are fixed. To exclude rails not used for scaling/pvt_interpolation or dependent rails (most likely a bias pin), please use create_scaling_lib_group -exclude_voltage_names {VBP}, for example.

Examples

```
Error:Library group 'grp1' not ready for scaling.
```

LIBCHK-306

(warning) link_library %s '%s'.

Description

This message occurs when 1) link_library has extra libraries 2) link_library is missing a library from groups In PrimeTime, it is required that 1) one-and-only-one library in SLG to be in link_library 2) one library cannot be in more than one DSLGs. In ICC/DC, it is recommended but not required.

What Next

Remove the extra libraries from link_library or add a missing library from the group.

Examples

```
Warning: link_library has extra library: 'p1v1.db' (LIBCHK-306)
```

LIBCHK-307

(information) List of miscellaneous inconsistent library data

Description

This message is reporting different values in the same group/attributes that are not reported in any other tables when comparing 2 dbs. In this report table, Path name consists of hierarchical group/object names. If the attribute is at the library level, it is the library_name. This is mainly for internal use.

Feedback

What Next

If difference is reported for the attribute, please open the db files to view the values to see if it is expected.

Examples

```
List of miscellaneous inconsistent library data
-------------------------------------------------------------------------
-----------------
Path name                      Object              Attribute
 Value(lib#1)   Value(lib#2)
-------------------------------------------------------------------------
-----------------
mycell/Q3/                     bag_contents(CP)    active        2
      1
-------------------------------------------------------------------------
-----------------
```

Examples

```
Information: List of miscellaneous inconsistent library data (LIBCHK-307)
```

LIBCHK-308

(information) Library grouping table

Description

This message is for reporting list of libraries with group name and group number they belong to. When a library is specified in multiple library groups by create_scaling_lib_group command, or a user defined lib group has multiple groups in terms of cells, the group number will include sub-group number, e.g. 2.1.

What Next

For library scaling, the operating conditions in the same scaling library group should be different in nominal voltage, temperature and/or process. For MCMM and MV/UPF, the nominal voltages should be different under different operating conditions. For -compare, the operating_consitions should be identical. For all others, this is information only. No further action is required. For voltage scaling, it is recommended that the voltages should be no more than 20% apart for good accuracy

Examples

```
When user defines
set search_path "dbs"
create_scaling_lib_group -exact -name SVT
"SVT_ts28nmhsdst_ss0p81v0c.db \
 SVT_ts28nmhsdst_ss0p81v125c.db  \
 SVT_ts28nmhsdst_tt0p9v25c.db  \
```

Feedback

```
 SVT_ts28nmhsdst_tt0p9v85c.db"
create_scaling_lib_group -exact -name LVT
"SVT_ts28nmhsdst_ss0p81v0c.db \
 LVT_ts28nmhldst_ff0p99vn40c.db \
 LVT_ts28nmhldst_tt0p9v85c.db"

check_library report will be

Error: set_lib_group or create_scaling_lib_group -name "LVT" has multiple
 lib groups (LIBCHK-305)

Information: Library grouping table (LIBCHK-308)
-------------------------------------------------------------------------
-------
Group name Number Library name           Library file name
-------------------------------------------------------------------------
-------
SVT         1    ts28nmhsdst_ss0p81v0c    dbs/SVT_
 ts28nmhsdst_ss0p81v0c.db
SVT         1    ts28nmhsdst_ss0p81v125c
 dbs/SVT_ts28nmhsdst_ss0p81v125c.db
SVT         1    ts28nmhsdst_tt0p9v25c
 dbs/SVT_ts28nmhsdst_tt0p9v25c.db
SVT         1    ts28nmhsdst_tt0p9v85c
 dbs/STD_SVT_ts28nmhsdst_tt0p9v85c.db
LVT         2.1  ts28nmhsdst_ss0p81v0c
 dbs/SVT_ts28nmhsdst_ss0p81v0c.db
LVT         2.2  ts28nmhldst_ff0p99vn40c
 dbs/LVT_ts28nmhldst_ff0p99vn40c.db
LVT         2.2  ts28nmhldst_tt0p9v85c
 dbs/LVT_ts28nmhldst_tt0p9v85c.db
-------------------------------------------------------------------------
-------
```

LIBCHK-310

(information) List of cells missing in logic libraries

Description

This message is for reporting cells missing in one or more logic libraries during logic vs. logic library checking. All the logic cells that are missing will be reported in this table.

What Next

If cells are found missing in one or more of the libraries, please check why these are existing in onle library but missing in the other. If such cells are used in design, these cells have to be in all the libraries.

Feedback

Examples

```
List of cells missing in logic libraries
-------------------------------------------------------------------------
-----
Cell name           SR60_W_SVT_UHD.db           SR60_S_SVT_UHD.db
-------------------------------------------------------------------------
-----
nsdffnqs_f4_svt     missing                     existing
-------------------------------------------------------------------------
-----
```

Examples

```
Warning: List of cells missing in logic libraries (LIBCHK-310)
```

LIBCHK-311

(warning) List of cells with mismatched or missing attributes in logic libraries

Description

This message is for reporting mismatched cell data in logic libraries during logic vs. logic library checking. Mismatched cells are those that have inconsistent attribute values at the cell level. For characterization values (e.g. cell_leakage_power), there are calculated absolute and relative errors along with respective values in each library. They are listed in the columns on the right-hand side.

What Next

Mismatched cells will cause issues if used in design. The same name cells existing in different libraries should have the same values for attributes such as function, dont_use and dont_touch, and same attributes should exist in all the libraries.

Examples

```
Warning: List of cells with mismatched or missing attributes in logic
 libraries (LIBCHK-311)
-------------------------------------------------------------------------
---------
                                        Attribute value
 Error
Cell name           Attribute           lib#1       lib#2       Absolute
 Relative
-------------------------------------------------------------------------
---------
tieofflx_svt        function            "A * B"     "A * B + c"
std_cell_inv        pin_order           "A_Y"       "VDD_A_Y"
usb30io_io8kv_ns    cell_leakage_power  56.356129   18.580099   -37.77603
 -67.03%
```

Feedback

```
usb30io_io8kv_ew    cell_leakage_power  56.356129   18.580099   -37.77603
 -67.03%
--------------------------------------------------------------------------
---------
```

Examples

```
Warning: List of cells with mismatched or missing attributes in logic
 libraries (LIBCHK-311)
```

LIBCHK-312

(information) List of cell classification

Description

This message is for reporting cell classification of logic libraries. In this report table, numbers of total cells, inverters, buffers, level shifters, isolation cells, retention cells, switch cells, and always on cells in each library For library scaling, number of single and multi-rail cells in pg_pin based libraries is also reported. are reported.

What Next

For UPF flow, special cells such as level shifters should exist in the library. in general, the library should have inverters. For library scaling, single and multi-rail cells should be in separate libraries. For all other cases, this is information only. No further action is required.

Examples

```
List of cell classification
--------------------------------------------------------------------------
-----
Library name        SR60_W_SVT_UHD.db         SR60_S_SVT_UHD.db
--------------------------------------------------------------------------
-----
Total number               3                         3
Inverter                   2                         1
Buffer                     0                         0
Level shifter              0                         0
Differential level shifter 0                         0
Isolation cell             0                         0
Clock Isolation cell       1                         1
Retention cell             0                         0
Switch cell                0                         0
Always on cell             0                         0
--------------------------------------------------------------------------
-----
```

Examples

```
Information: List of cell classification (LIBCHK-312)
```

Feedback

LIBCHK-313

(warning) List of function groups missing high threshold_voltage_group cells

Description

This message will occur when high threshold_voltage_group for the same function group. In this report table, the following columns are listed: function, Library name and Example cell name.

What Next

If some cells are found missing high threshold_voltage_group in logic cells, please check if the specified target_library is correct or missing some libraries in target_library.

Examples

```
Number of function groups missing high threshold_voltage_group:   14 (out
 of 148)

      List of function groups missing high threshold_voltage_group cells
------------------------------------------------------------------------
----------------
function                              Library name
 Example cell name
------------------------------------------------------------------------
----------------
A1 A2                                 tcbn45lpbwplvtwc
 AN2D0BWPLVT
(A1 A2) A3                            tcbn45lpbwplvtwc
 AN3D0BWPLVT
((A1 A2)+B)+C                         tcbn45lpbwplvtwc
 AO211D0BWPLVT
(A1 A2)+B                             tcbn45lpbwplvtwc
 AO21D0BWPLVT
((A1 A2)+(B1 B2))+C                   tcbn45lpbwplvtwc
 AO221D0BWPLVT
------------------------------------------------------------------------
----------------
```

Examples

```
Warning: List of function groups missing high threshold_voltage_group
 cells (LIBCHK-313)
```

LIBCHK-314

(information) List of mapping multi bit to single bit cells

Feedback

Description

This message occurs when checking multi bit mapping to single bit cells. It shows the mapping between multi bit cells and single bit cells. In this report table, the following columns are listed for each multibit function as a mapping between multi bit cells and single bit cells with library index: Multi bit cell(lib#) and Single bit cell(lib#). Blackbox multibit(MB) cells with single_bit_degenerate attribute will be reported in a separate table of the same LIBCHK type.

What Next

If mapping single bit cells are found missing as reported in LIBCHK-314w, please check if the specified target_library or lc_single_bit_degenerate_cell_library is correct or missing some libraries in the library list.

Examples

```
List of mapping multi bit to single bit cells (LIBCHK-314)
------------------------------------------------------------------------
-------
Multi bit cell(lib#)                    Single bit cell(lib#)
------------------------------------------------------------------------
-------
mb_4_scanin_gated_scanout1(lib#2)       sb_gated_scanout1(lib#2)
------------------------------------------------------------------------
-------
```

Examples

```
Information: List of mapping multi bit to single bit cells (LIBCHK-314)
```

LIBCHK-314w

(warning) List of missing/mapping multi bit to single bit cells

Description

This message will occur when checking multi bit mapping to single bit cells. When single bit cells are not found in the libraries, it will be reported as missing single bit cells. In this report table, the following columns are listed for each multibit function as a mapping between multi bit cells and single bit cells with library index: Multi bit cell(lib#) and Single bit cell(lib#). Blackbox multibit (MB) cells with single_bit_degenerate attribute will be reported in a separate table of the same LIBCHK type.

What Next

If mapping single bit cells are found missing, please check if the specified target_library or lc_single_bit_degenerate_cell_library is correct or missing some libraries in the library list.

Feedback

Examples

```
List of missing/mapping multi bit to single bit cells (LIBCHK-314w)
-------------------------------------------------------------------------
-------
Multi bit cell(lib#)                    Single bit cell(lib#)
-------------------------------------------------------------------------
-------
STL_FSDPQOMB_D_1(lib#1)                 missing
mb_4_scanin_gated_scanout1(lib#2)       sb_gated_scanout1(lib#2)
-------------------------------------------------------------------------
-------

Number of multibit cells missing single bit cells: 1 (out of 2)
```

Examples

```
Warning: List of missing/mapping multi bit to single bit cells
 (LIBCHK-314w)
```

LIBCHK-315

(warning) List of data models and check policy in cells

Description

This message occurs when there are inconsistent early data models and/or policies in the cells. Similar to report_early_data_check_records that is reporting for single DB the early library data on the lib cells, check_library will report these data recorded in each DBs excluding error codes in the LIBCHK-315 table.

What Next

Early data models tolerated or repaired in the library compilation should be used for early stage in the design, and should not be used for sign-off.

Examples

```
Warning: List of data models and check policy in cells (LIBCHK-315)
-----------------------------------------------------------------
                                          Policy
Cell name   Data model        lib#1       lib#2
-----------------------------------------------------------------
BUF1      nldm           tolerate repair
ISO1      power_aware    repair  error
ISO1      ccsn           tolerate repair
-----------------------------------------------------------------
```

Examples

```
Warning: List of data models and check policy in cells (LIBCHK-315)
```

Feedback

LIBCHK-320

(warning) List of pins missing in logic libraries

Description

This message is for reporting missing signal pins in logic cells during logic vs. logic library checking. All the logic pins that are missing in a cell but existing in other cells will be reported in this table. In this report table, the following columns are listed: Cell name, Pin name and each logic library names.

What Next

If some signal pins are found missing in logic cells, it is a real issue and therefore an Error message LIBCHK-101 will occur to direct you to correct the cells that are missing these pins in the logic library.

Examples

```
List of pins missing in logic libraries
------------------------------------------------------------------------
-----
Cell name       Pin name SR60_W_SVT_UHD.db         SR60_S_SVT_UHD.db
------------------------------------------------------------------------
-----
tieofflx_svt    AA    missing                  existing
tieofflx_svt    ZZ    missing                  existing
------------------------------------------------------------------------
-----
```

Examples

```
Warning: List of pins missing in logic libraries (LIBCHK-320)
```

LIBCHK-321

(warning) List of pins with mismatched or missing attributes in logic libraries

Description

This information message occurs when the tool finds mismatched pins in the logic cells during logic versus logic library checking. Mismatched pins are those that have inconsistent pin attributes such as pin direction, function, related_power_pin, and so forth. For characterization values (e.g. capacitancer), there are calculated absolute and relative errors along with respective values in each library. They are listed in the columns on the right-hand side. Pin level user defined attributes also are reported in this table if mismatched or missing.

The report table has the following columns:

```
Cell name
Pin name
Attribute/Group name
Attribute value of each of the logic libraries
Absolute and Relative errors
```

What Next

This is only an information message. No action is required.

However, mismatched pins will cause issues if the cells are used in the design. The same name pins should exist in the same name cells in different libraries with consistent values for attributes such as function, direction, related_power_pin, and related_ground_pin, and the same attributes should exist for the same pins in the same name cells. Characterization values such as capacitance can be different. For mcmm, mismatched pin_number's will cause MV-087 Error.

Examples

The following is an example of a mismatched pins list:

```
Warning: List of pins with mismatched or missing attributes in logic
 libraries (LIBCHK-321)
------------------------------------------------------------------------
---------------
                      Subgroup/              Attribute value
 Error
Cell name Pin name    Attribute           lib#1       lib#2
 Absolute  Relative
------------------------------------------------------------------------
---------------
tieoff    lo          pin_number          0           1
std_inv   Y           related_ground_pin  missing     VSS
MX02D1    I1          fall_capacitance_upper
                                          0.003505    0.003509
 0.0000040 0.11%
MX02D1    S           fall_capacitance_upper
                                          0.005593    0.005586
 -0.000007 -0.13%
MX02D1    I0          fall_capacitance_lower
                                          0.003723    0.003727
 0.0000040 0.11%
MX02D1    I1          fall_capacitance_lower
                                          0.003505    0.003509
 0.0000040 0.11%
MX02D1    I0          fall_capacitance    0.003723    0.003727
 0.0000040 0.11%
MX02D1    I1          fall_capacitance    0.003505    0.003509
 0.0000040 0.11%
```

Feedback

```
MX02D1    S           fall_capacitance    0.005593    0.005586
 -0.000007 -0.13%
MX02D1    I1          capacitance         0.003596    0.003598
 0.0000020 0.06%
CKGTPLS   CK          ecsm_capacitance    missing     existing
-------------------------------------------------------------------------
---------------
```

LIBCHK-322

(warning) List of pg_pins with mismatched or missing attributes in logic libraries

Description

This information message occurs when the tool finds pg_ pins with mismatched or missing attributes in the logic cells during logic versus logic library checking. Mismatched pg_pins are those that have inconsistent pg_pin attributes.

The report table has the following columns:

```
Cell name
pg_pin name
Attribute/Group name
Attribute value of each of the logic libraries
```

What Next

Mismatched pg_pins will cause issues if the cells are used in the design. The same name pg_pins should exist in the same name cells in different libraries with consistent values for attributes such as direction, pg_function and switch_function. The same attributes should exist for the same pg_pins in the same name cells.

Examples

The following is an example of mismatched pg_pins list:

```
List of pg_pins with mismatched or missing attributes in logic libraries
-------------------------------------------------------------------------
-----
                           Attribute                Attribute value
Cell name       pg_pin name  /Group               non_pg_lib      pg_lib
-------------------------------------------------------------------------
-----
LVLLHCD         VDD         std_cell_main_rail     missing         true
FOOTER          VSS         pg_function            missing         "TVSS"
-------------------------------------------------------------------------
-----
```

Feedback

LIBCHK-323

(warning) List of pg_pins missing in logic libraries

Description

This message is for reporting missing pg_pins in logic cells during logic vs. logic library checking. All the logic pg_pins that are missing in logic cells will be reported in this table. In this report table, the following columns are listed: Cell name, pg_pin and each logic library names.

What Next

If pg_pins are missing in the logic library, it indicates that the logic library is not pg_pin based, and you need to use add_pg_pin_to_db utility to convert it into pg_pin based db.

Examples

```
List of pg_pins missing in logic libraries
-------------------------------------------------------------------------
-----
Cell name       pg_pin          SR60_W_SVT_UHD.db
 SR60_S_SVT_UHD.db
-------------------------------------------------------------------------
-----
tieofflx_svt    __VSS    missing                  existing
tieofflx_svt    __VDD    missing                  existing
-------------------------------------------------------------------------
-----
```

Examples

```
Warning: List of pg_pins missing in logic libraries (LIBCHK-323)
```

LIBCHK-330

(warning) List of timing arcs missing in libraries

Description

This message is for reporting timing arcs missing in the logic libraries.

What Next

For timing scaling, timing arc information should exist with consistent timing data in each library. For other cases, this is information only. No further action is required.

Feedback

Examples

```
List of timing arcs missing in libraries
-------------------------------------------------------------------------
-----
Cell name     Arc             SR60_W_SVT_UHD.db         SR60_S_SVT_UHD.db
-------------------------------------------------------------------------
-----
tbufl_f7_svt  gz_y            existing                  missing
-------------------------------------------------------------------------
-----
```

Examples

```
Warning: List of timing arcs missing in libraries (LIBCHK-330)
```

LIBCHK-331

(warning) List of timing arcs mismatched in logic libraries

Description

This message is for reporting mismatched arcs in logic libraries during logic vs. logic library checking. It also includes inconsistent output load indices. This report table has the following columns: Cell name, Arc name, Attribute/Group name and attrbute values of each logic libraries.

What Next

For timing scaling and timing/delay calculations, consistent timing data should exist in the libraries for each timing arc.

Examples

```
List of timing arcs mismatched in logic libraries
-------------------------------------------------------------------------
-----
Cell name           Arc      Attribute             Attribute value
                              /Group         SR60_W_SVT_UHD.db
 SR60_S_SVT_UHD.db
-------------------------------------------------------------------------
-----
tbufl_f7_svt        gz_y     timing_sense    positive_unate     non_unate
-------------------------------------------------------------------------
-----
```

Examples

```
Warning: List of timing arcs mismatched in logic libraries (LIBCHK-331)
```

Feedback

LIBCHK-332

(warning) Library '%s' is missing CCS %s models.

Description

This warning message occurs during logic versus logic library checking, when no driver or receiver model exists in the library.

What Next

This is only a warning message. No action is required.

However, receiver models and driver models (compressed or original format) must exist in the libraries for timing scaling. For all other cases, this is information only.

LIBCHK-340

(warning) List of inconsistent CCS noise models

Description

This message is for reporting inconsistent CCS noise models in logic libraries. It reports: a) inconsistent input_voltage and output_voltage indices for CCS noise models. They should be in the same percentage of nominal voltages. b) inconsistent conditional (when) pin models (when order). c) inconsistent CCS noise models for all pins and arcs. This report table includes the following columns: Cell name, Pin name, Group name, Attrbute name and attribute value of each library.

What Next

For CCS noise scaling, consistent noise models are required. For other cases, it is for information only.

Examples

```
List of inconsistent CCS noise models
-------------------------------------------------------------------------
-----
                                        Attribute           Attribute value
Cell name Pin name  Group name          /variable    SR60_W_SVT_UHD
 SR60_S_SVT_UHD
-------------------------------------------------------------------------
-----
inv0d0    ZN        ccsn_first_stage    input_net_transition
                                                  "175.0"
 "980.0"
inv0d0    ZN        ccsn_last_stage     total_output_net_capacitance
                                                  "0.0"             "0.0"
```

Feedback

```
-------------------------------------------------------------------------
-----
```

Examples

```
Warning: List of inconsistent CCS noise models (LIBCHK-340)
```

LIBCHK-341

(warning) List of inconsistent power models.

Description

This warning message occurs when there are inconsistent power models in the logic library. For characterization values (e.g. internal_power), there are calculated absolute and relative errors as well as error type along with respective values in each library. They are listed in the columns on the right-hand side.

It reports the following inconsistencies:

- `Inconsistent dynamic_current groups for each cell`
- `Inconsistent intrinsic_parasitic tables for each cell`
- `Inconsistent leakage_current groups for each cell`
- `Inconsistent power_cell_type attribute for each cell`
- `Inconsistent internal_power tables for each pin or cell`
- `Inconsistent leakage_power tables for each cell`

The report table includes the following columns:

```
Cell name
Group name
Attribute name
Attribute value of all logic libraries
Absolute and Relative errors and type
```

What Next

This is only a warning message. No action is required.

However, consistent power models are required for power scaling. For other cases, the report is for information only.

Feedback

Examples

The following is an example of a list of inconsistent power models:

```
List of inconsistent power models
------------------------------------------------------------------------
-----
                                                          Attribute value
Cell name  Group            Attribute       SR60_W_SVT_UHD
 SR60_S_SVT_UHD
------------------------------------------------------------------------
-----
ap001_svt  leakage_power    value           0.000000         2.686740
an02d1     dynamic_current  related_inputs  "A1"             "A0"
------------------------------------------------------------------------
-----

List of inconsistent power models. (LIBCHK-341)
index_1:    input_transition_time
------------------------------------------------------------------------
-------------------------------------------------

       Attribute value               Error
Cell name Group           when                Group/Attribute
 (index_1,index_2) lib#1     lib#2     Absolute  Relative Type
------------------------------------------------------------------------
-------------------------------------------------
ap001_svt leakage_power   A+B                 value
       0.000000  2.686740
usb30io_io8kv_ns
          wpu_n/internal_power
                          hold_h_n&sig_in&ds[0]'&ds[1]'
                                              rise_power/values
                                                              0.0208537
       0.003811  0.0010794 -0.002731 -71.68%  NLPM_IP
                                                              0.0417187
       0.0041157 0.0012722 -0.002843 -69.09%  NLPM_IP
                                                              0.0834375
       0.004725  0.0016579 -0.003067 -64.91%  NLPM_IP
                                                              0.166875
       0.0049465 0.0016862 -0.003260 -65.91%  NLPM_IP
                                                              0.33375
       0.0053895 0.0017428 -0.003646 -67.66%  NLPM_IP
                                                              0.6675
       0.0062755 0.001856  -0.004419 -70.42%  NLPM_IP
                                                              1.335
       0.0080475 0.0020824 -0.005965 -74.12%  NLPM_IP
------------------------------------------------------------------------
-------------------------------------------------
```

Feedback

LIBCHK-342

(warning) List of inconsistent data between CCS noise and NLDM models

Description

This is validation between NLDM delay/slews and those derived from CCSN with NLDM as reference. This message occurs when there are inconsistent delay and slew data between CCS noise and NLDM models in the logic library. The default relative and absolute tolerance values for delay are 2% and 5ps, respectively, and for slew, 3% and 7.5ps. In the table, N/A, if any, refers to that CCSN model does not exist on that timing arc.

What Next

This is a warning message about CCSN accuracy. It may render library cells with the reported accuracy issue unusable.

Examples

The following is an example of a list of inconsistent power models:

```
List of inconsistent data between CCS noise and NLDM models (LIBCHK-342)
-------------------------------------------------------------------------
-------------------------------------------------

 tsmc_cln40g_sclmp_pt_fast_125c_0p99v      Error
Cell name     pin/related_pin  timing_type    when   Group
 index_1,index_2   (NLDM)       (CCSN)      Absolute    Relative
-------------------------------------------------------------------------
-------------------------------------------------
XOR3X05LMP_BZA_P21
              Z/C              combinational  !A&B   cell_rise
 "0.002,0.0005"    0.0127228   0.00456662  -0.008156   -64.11%
XOR3X05LMP_BZA_P21
              Z/C              combinational  !A&B   rise_transition

 "0.002,0.0005"    0.022014    0.00171184  -0.020302   -92.22%
XOR3X05LMP_BZA_P21
              Z/C              combinational  !A&B   fall_transition

 "0.002,0.0106444" 0.1157      0.066054    -0.049646   -42.91%
-------------------------------------------------------------------------
-------------------------------------------------
```

LIBCHK-343

(warning) List of sensitive CCSN models

Feedback

Description

The CCSN models of some cells are very sensitive in delay and slew to their input driving waveform. Small distortion of the input driving waveform tail can lead to a significantly different output waveform. A library cell is considered sensitive if the difference of delay or slew of output responses of the library cell to an input waveform versus a tail-distorted version of the input waveform is larger than the given tolerances. The default relative and absolute tolerance values for delay are 2% and 5ps, respectively, and for slew, 3% and 7.5ps. In the table, N/A, if any, refers to that CCSN model does not exist.

What Next

This is a warning message about CCSN sensitivity. To drive sensitive cells, it is recommended that a driver cell with better full swing (>95% VDD) be used. And library developer may choose more proper CCB cut to minimize the issue. Otherwise, it may render library cells with the reported accuracy issue unusable.

Examples

The following is an example of the report:

```
List of sensitive CCSN models (LIBCHK-343)
-------------------------------------------------------------------------
-------------------------------------------------

 tsmc_cln40g_sclmp_pt_fast_125c_0p99v      Error
Cell name     pin/related_pin  timing_type    when   Group
 index_1,index_2   (Normal)   (Clamped)      Absolute    Relative
-------------------------------------------------------------------------
-------------------------------------------------
XOR3X05LMP_BZA_P21
              Z/C              combinational  !A&B   cell_rise
 "0.002,0.0005"    0.0127228   0.00456662  -0.008156   -64.11%
XOR3X05LMP_BZA_P21
              Z/C              combinational  !A&B   rise_transition

 "0.002,0.0005"    0.022014    0.00171184  -0.020302   -92.22%
XOR3X05LMP_BZA_P21
              Z/C              combinational  !A&B   fall_transition

 "0.002,0.0106444" 0.1157      0.066054    -0.049646   -42.91%
-------------------------------------------------------------------------
-------------------------------------------------
```

LIBCHK-344

(warning) Table of attribute value range analysis

Feedback

Description

This table lists scalar attributes and their values that are out of range as defined in set_check_library_option. In the table, the following fields are listed: Cell name, pin/subgroup, timing_type, when, Attribute, value and line_num where the second field can be pin or a subgroup name under the cell such as leakage_power. When an entry has no value in a field, it is blank. If the library is loaded from source .lib and the tcl var lc_check_lib_keep_line_number is set true, line_num field will show the line numbers where the attribute group starts.

This table also reports dc_resistance_high/low derived from dc_current tables in CCSN V1 and V2: 1) for 1-stage CCSN, check ccsn_first_stage/input_ccb 2) for multi- or 2-stage CCSN, check ccsn_last_stage/output_ccb only

What Next

Please check the attributes that have values out of range and correct them as needed. User should check the values and find out if characterization or setting have done correctly.

Examples

The following is an example table:

```
Warning: Table of attribute value range analysis (LIBCHK-344)
-------------------------------------------------------------------------
--------------------------
Cell name           pin/subgroup    timing_type   when      Attribute
       value     line_num
-------------------------------------------------------------------------
--------------------------
STN_AN6_1           leakage_power                 A1 * A2  value
      0.00502   1048
STN_AN6_1           A4
 rise_capacitance    0.000598  1739
STN_AN6_1           A5                                     capacitance
       0.000625  1882
STN_FDNQ_1          Q
 ccsn_last_stage/miller_cap_rise

       0.000246  16064
-------------------------------------------------------------------------
--------------------------
```

LIBCHK-345

(warning) Table of %s value ratios.

Feedback

Description

This table lists the dynamic_current groups, which has output switching, that:
1. The ratio of peak pg_current(power) to peak pg_current(ground) are out of range as defined in set_check_library_options -analyze {pg_current} \ -criteria {min_power_to_ground_current_ratio=...} .

1. The ratio of time constant of CCSP to time constant of NLDM/CCST are out of range as defined in set_check_library_options -analyze {ccsp_time_constant} \ -criteria { max_nldm_to_ccsp_time_const_ratio=... \ max_ccst_to_ccsp_time_const_ratio=...}

The report table includes the following columns:

```
Common columns:
  Cell name
  Group name
  When condition
  Attribute name
  index_1/index_2
  line_num1(optional)
  line_num2(optional)

For peak current check:
  Peak pg_current for Power
  Peak pg_current for Ground
  Ratio of Power/Ground
  Ratio of Ground/Power

For time constant check:
  Time of CCSP
  Time of NLDM/CCST
  Ratio of time constant
  Type : NLDM or CCST
```

If the library is loaded from source .lib and the tcl var lc_check_lib_keep_line_number is set true, line_num field will show the line numbers where the group starts.

What Next

User should check the reported group and verify if the value is correct.

Examples

The following is an example of a table of PG Current value ratios:

```
Warning: Table of PG Current value ratios (LIBCHK-345)
-------------------------------------------------------------------------
-------------------------------------------------------------
Cell name Group                    when        Group/Attribute line_num1
 line_num2 (index_1,index_2) Power    Ground    (P/G)      (G/P)
-------------------------------------------------------------------------
-------------------------------------------------------------
```

```
XOR4XD8BWP12T
          related_outputs:Z/related_inputs:A4/input:rise|output:fall
                                  A1&A2&A3   pg_current/peak_value
                                                          10978
 11061     0.0017,0.00205     0.786786  0.980786  0.8022     1.247

          0.0017,0.06806     0.614211  2.34515   0.2619     3.818
```

The following is an example of a table of CCSP Time constant ratios:

```
Warning: Table of CCSP Time constant value ratios. (LIBCHK-345)
------------------------------------------------------------------------
-------------------------------------------------------------------
Cell name Group                    when        Group/Attribute line_num1
 line_num2 (index_1,index_2)  CCSP     NLDM/CCST  Ratio    Type
------------------------------------------------------------------------
-------------------------------------------------------------------
XOR4XD8BWP12T
          related_outputs:Z/related_inputs:A4/input:rise|output:rise
                          !A1&!A2&!A3         pg_current/time 10463
 40914     0.2109,0.00205     0.714328  0.0254     28.12     CCST

          0.2109,0.06806     0.714328  0.058      12.32     CCST
```

LIBCHK-346

(warning) List of inconsistent data between CCS noise and CCS timing models

Description

This is validation between the times at the trip points derived from CCST and those derived from CCSN with CCST as reference. This message occurs when there are inconsistent data between CCS noise and CCS timing models in the logic library. The default relative and absolute tolerance values for all trip points are 5% and 0.005ns, respectively.

What Next

This is a warning message about CCSN vesus CCST accuracy. It may render library cells with the reported accuracy issue unusable.

Examples

The following is an example of a list of inconsistent CCS noise and CCS timing models:

```
List of inconsistent data between CCS noise and CCS timing models
 (LIBCHK-346)
------------------------------------------------------------------------
-----------------------------------------------

        ss_0p5225v_m25c                Error
```

```
Cell name     pin/related_pin  timing_type    when   point
 index_1,index_2   (CCST)      (CCSN)      Absolute    Relative
-------------------------------------------------------------------------
-------------------------------------------------
INV_X8M_A9TL  Y/A              combinational         rise_0.15
 0.003209,0.448719 0.108767    0.107171    -0.001595   -1.47%
INV_X8M_A9TL  Y/A              combinational         rise_0.15
 0.003209,0.904573 0.214978    0.211207    -0.003771   -1.75%
INV_X8M_A9TL  Y/A              combinational         rise_0.15
 0.0133113,0.448719

        0.113749    0.112348    -0.001400   -1.23%
-------------------------------------------------------------------------
-------------------------------------------------
```

LIBCHK-347

(warning) List of inconsistent receiver_capacitance C1/C2

Description

This is validation between C1/C2 converted from C1/Cn and original receiver_capacitance1/2_rise/fall. When the difference exceeds the default or specified capacitance tolerance, the values will be reported.

What Next

This is a warning message about n-receiver_capacitance accuracy.

Examples

The following is an example of the report.

```
#BEGIN_XCHECK_C1C2

Warning: List of inconsistent receiver_capacitance C1/C2 (LIBCHK-347)
-------------------------------------------------------------------------
-------------------------------

 values                Error
Cell name     pin/related_pin  timing_type   when    Attribute (C1/C2)
 (Cn converted) Absolute  Relative
-------------------------------------------------------------------------
-------------------------------
DBLVT16       X/A1             combinational A2      fall_c2   0.00310165
  0.00413994  0.0010382 33.48%
MUX2_12       X/S              combinational D0&!D1  rise_c2   0.00471183
  0.00585422  0.0011423 24.25%
MUX2_8        X/S              combinational D0&!D1  rise_c2   0.00332178
  0.00448415  0.0011623 34.99%
-------------------------------------------------------------------------
-------------------------------
```

Feedback

```
#END_XCHECK_C1C2
```

LIBCHK-350

(warning) List of inconsistent data between different timing models

Description

This message is for validating library data between CCS and NLDM models. It reports: a) inconsistent output load indices between CCS and NLDM models, and inconsistent load indices for CCS drive/receiver b) inconsistent NLDM delay and slew indices and values with a default or user specified tolerance. c) inconsistent delays between NLDM and CCS timing with a user specified tolerance for both compact CCS and expanded CCS d) inconsistent data between two CCS driver model current waveforms including compact CCS with expanded CCS data with a tolerance e) inconsistent between CCS power data and NLPM data (not in 2008.09 releases) In this report table, including following columns: Cell name, Croup name, Attrbute name and attribute value of all liogic libraries.

What Next

If the difference is significantly larger between the models, please rerun the simulation to correct the libraries.

Examples

```
Warning: List of inconsistent data between different models (LIBCHK-350)
Cell name:  dtmuxi3_d10m
index_1:    total_output_net_capacitance
index_2:    input_net_transition
-------------------------------------------------------------------------
---------------------------------

 gold_timing_index_lib     Error
pin/related_pin timing_type   when  Group/Attribute (index_1,index_2)
 (NLDM)     (CCS)     Absolute Relative
-------------------------------------------------------------------------
---------------------------------
y/s2            combinational       cell_rise/values
                                                        (1.83,0.5)
 18.016    18.2206   0.20456  1.1%
                                                        (1.83,4)
 19.5332   19.8679   0.33468  1.7%
                                                        (1.83,12)
 23.9233   28.2093   4.286    18%
-------------------------------------------------------------------------
---------------------------------
```

Examples

```
Warning: List of inconsistent data between different models (LIBCHK-350)
```

Feedback

LIBCHK-351

(information) List of inconsistent constructs and values

Description

This message is for reporting inconsistent liberty syntax constructs and/or values of the two logic libraries

What Next

This is information only. No further action is required.

Examples

```
Information: List of inconsistent constructs and values (LIBCHK-351)
```

LIBCHK-352

(information) Table of variation-aware model analysis

Description

This table lists variation aware analysis results for driver, receiver and constraint models. For a set of va_values, there are normally three values: nominal, -Sigma and +Sigma. From the three values for each pair of indices, a linear model is used to find: a) monotonicity (trend) including - delays increase as slew and load increase. - delays increase/decrease as va_parameters increase. b) significance of each va_parameters

As trial and error procedure, the following statistics will be used in the study on the VA models. iThe linear model is used to roughly measure how significant each va_parameters affects on delay. 1) If slope ~= 0, va_parameter is insignificant (not sensitive) 2) If slope > 0, monotonously increasing 3) If slope < 0, monotonously decreasing 4) Alternating slopes may indicate issues 5) Trend: If Dnom > both D+/-sigma, or If Dnom < both D+/-sigma, not monotonous, where D is Delay. 6) coefficient of correlation to measure how closely the va_parameters are related to delays. Std error is used to measure how much va_parameter and delay points deviate from the linear model.

This report table includes the following columns: pin/related_pin, timing_type, when, Group, va_values, (index_1,2), nomimal, -Sigma, +Sigma, Slope, Std error and Trend In Trend column, / is monotonously increasing, \ is monotonously decreasing, ^ is non-monotonous up, V is non-monotonous down and - is flat.

What Next

If the difference is significantly larger between the models, please rerun the simulation to correct the libraries.

Feedback

Examples

```
Information: Table of variation-aware model analysis (LIBCHK-352)
Cell name:         Sdffcqs
va_parameters:     (var1, var2)
nominal_va_values: (10,20)
index_1:                   input_net_transition
index_2:                   output_net_capacitance
-------------------------------------------------------------------------
-------------------------------------

              values
pin/related_pin timing_type  when  Group   va_values  (index_1,2) nomimal
 -Sigma +Sigma  Slope Std error Trend
-------------------------------------------------------------------------
-------------------------------------
sq/clk          rising_edge  scan  compact_ccs_rise
                                                        var1+/-0.4
 (1.11,0.92) 23.02   22.42  23.82   0.3   0.86%     /
                                                      (3.7,
 0.92) 32.04   31.04  33.06   0.3   0.56%     /
-------------------------------------------------------------------------
-------------------------------------
```

Examples

```
Information: Table of variation-aware model analysis (LIBCHK-352)
```

LIBCHK-353

(information) Report of the statistical analysis results of characterization models.

Description

This information message reports the statistical analysis results of characterizations between CCS and NLDM models or between the same types of models in two libraries, using the golden NLDM or first library as the base. In counting the grid points, for example, if a 7x7 NLDM table grids mismatch 7X7 CCS, it should be counted as 49, not 98. And delay/slew values passed do not include failed grid points.

The columns in the table include the following:

- Group type: Delay, Slew, Constraint, Receiver capacitance
- Mean of differences: Absolute, Relative
- Standard deviation: Absolute, Relative
- Max outlier: the maximum value of the deviations

Feedback

- Number of grid points: Passed, Failed

What Next

If the mean is far from 0, the two models or libraries have significant differences. If the standard deviation is significantly large, the differences of these two are dispersed. In any case, small numbers of mean and deviation, close to 0, should be expected if the characterizations are generated under the same operating conditions.

Examples

The following is an example report of the statistical analysis results of characterization models:

```
Information: List of statistical analysis (LIBCHK-353)
------------------------------------------------------------------------
----------
               Mean of differences    Std deviation
 Number of grids
Group type      Absolute Relative   Absolute Relative   Max outlier  Pass
    Fail
------------------------------------------------------------------------
----------
Delay           0.0001   0.00%      0.0016   0.00%      0.0309       892
    4
Slew            -0.0003  -0.00%     0.0044   0.01%      -0.0773      856
    40
Constraint      65.6896  -69.56%    463.0871 3034.77%   3905.8228    878
    42
Receiver cap    0.0000   0.00%      0.0000   0.00%      0.0000       1072
    0
------------------------------------------------------------------------
----------
```

LIBCHK-354

(information) Table of characterization timing table trend analysis.

Description

This information message presents a table of single characterization timing table trend analysis results for delay, slew, driver, receiver and constraint models. The trends include the following:

```
/       monotonously increasing
\\\       monotonously decreasing
^       non-monotonous up
V       non-monotonous down
-       flat
```

```
M       Multiple peaks
W       Multiple troughs
N       2 peaks with 2nd not turning low
```

What Next

This is an information message only. No action is required.

However, if the trend indicates that the values do not increase as slew/load indices, please check that the characterizations have been done correctly.

Examples

The following is an example table:

```
Table of characterization timing table trend analysis (LIBCHK-354)
index_1:    related_pin_transition
index_2:    output_net_capacitance
------------------------------------------------------------------------
---------------------------
Cell name   pin/related_pin timing_type    when    Group
 index_1,index_2   values         Trend
------------------------------------------------------------------------
---------------------------
sdffcqs     q/clk           min_pulse_width        fall_constraint
                                                              1.11,*
        "66.528,..."   V
sdffcqs     q/clrz          clear                  cell_fall   1.11,*
        "50.8109,..."  /
------------------------------------------------------------------------
---------------------------
```

LIBCHK-355

(warning) Table of characterization table bound analysis.

Description

This warning message presents a table of single characterization table value bound analysis results for delay, slew, driver, receiver, constraint and power tables. The bound include upper bound (max value) and lower bound (min value).

The violation (table values out of bound) will be triggered and reported when 1) table-value > upper bound or 2) table-value < lower bound

If no violate found for upper criteria or lower criteria, '-' will be reported, otherwise the peak value (largest violation for upper criteria or smallest violation for lower criteria, or the larger of the absolute values if both violated) will be reported in the table.

The index field indicate the grid point that peak violation located, and the '*' in index field indicate which index direction is scaned during the analysis.

Feedback

What Next

This warning message will show the value tables that have value out of the upper bound or lower bound. User should check the value and find out if characterization have done correctly.

Examples

The following is an example table:

```
Table of characterization table bound analysis (LIBCHK-355)
-------------------------------------------------------------------------------
---------------------------------------
Cell name          pin/related_pin  timing_type         when   Group
 index_1, index_2    Min value  Max value
-------------------------------------------------------------------------------
---------------------------------------
T11ZNRBN1C1F4ZSE   IO/IN            3_state_enable_fall
 CFO&!CHDRV&!IE&NRST
                                                              cell_fall

 "1.5, 10.9009*"     -          3.81301

 "2.5, 10.9009*"     -          3.85745
-------------------------------------------------------------------------------
-----------------------------------------
```

LIBCHK-356

(warning) Table of characterization table slope analysis.

Description

This warning message presents a table of single characterization table value slope analysis results for delay, slew, driver, receiver, constraint and power tables. The slope include the max slope and min slope, and defined as:

```
Slope=((V2-V1)/(S2-S1))*(Srange/Vrange)
V2, V1: the values of two adjacent points in the table;
S2, S1: the index values of two adjacent points in the table;
Vrange = V_largest - V_smallest
Srange = S_largest - S_smallest
```

When checking the slope, violation will be triggered and reported when: 1) curve-slope > max slope or 2) curve-slope < min slope

If no violate found for upper criteria or lower criteria, '-' will be reported, otherwise the peak value (largest violation for upper criteria or smallest violation for lower criteria, or the larger of the absolute values if both violated) will be reported in the table.

The index field indicate the grid point that peak violation located, and the '*' in index field indicate which index direction is scaned during the analysis.

What Next

This warning message will show the value tables that have data slope out of the max slope or min slope. User should check the value and find out if characterization have done correctly.

Examples

The following is an example table:

```
Table of characterization table slope analysis. (LIBCHK-356)
------------------------------------------------------------------------
---------------------------------------
Cell name          pin/related_pin  timing_type         when   Group
 index_1, index_2    Min slope  Max slope
------------------------------------------------------------------------
---------------------------------------
T11ZNRBN1C1F4ZSE   OUT/IE           combinational              cell_rise

 "0.05, 2.72*"       -          5.44444
------------------------------------------------------------------------
---------------------------------------
```

LIBCHK-357

(information) Table of characterization table index analysis.

Description

This information message presents a table of single characterization table index analysis results for delay, slew, driver, receiver and constraint models. It lists all the index tables that meet index[i+1]/index[i] > x-factor specified.

What Next

This is an information message only. However, if the index analysis indicates that the index values increase extremely, the accuracy may suffer.

Examples

The following is an example table:

```
Table of characterization table index analysis (LIBCHK-357)
index_1:    related_pin_transition
index_2:    output_net_capacitance
------------------------------------------------------------------------
------------------------------
Cell name     pin/related_pin  timing_type    when   Group/attribute
 value                    Max ratio
```

Feedback

```
-------------------------------------------------------------------------
------------------------------
T11ZNRBN1C1F4ZSE
              OUT/IE           combinational  CFO&!CHDRV&!IN&IO&NRST)
                                                    cell_rise/index_2
 "0.03,2.72,...           90.6667
-------------------------------------------------------------------------
------------------------------
```

LIBCHK-358

(warning) Table of interpolation accuracy analysis

Description

This interpolation accuracy analysis is performed by fitting the rows and columns of a 2-D NLDM timing model (delay/slew/constraint) with (bi)cubic and linear models, and comparing the values at mid index points with one index fixed. For example, in a 7x7 table, there would be 6 checks along each row and 6 checks along each column at mid index points. If the difference between the two models exceeds the specified tolerances, the mid grid (index values) and the interpolated values will be reported.

What Next

If the interpolation difference is too large, the library needs to be enhanced by either increasing table size or using better spacing between the indexes.

Examples

The following is an example table:

```
Warning: Table of interpolation accuracy analysis (LIBCHK-358)
index_1:  related_net_transition
index_2:  total_output_net_capacitance
-------------------------------------------------------------------------
-------------------------------------

 Interpolation                 Error
Cell name  pin/related_pin  timing_type  when   Group
 index_1,index_2 (Bicubic) (Linear)  Absolute Relative
-------------------------------------------------------------------------
-------------------------------------
sdffcqs_f2 q/clk           rising_edge  !scan  cell_rise  1.11,3.71
  0.06724   0.07724   0.0100   14.87%
-------------------------------------------------------------------------
-------------------------------------
```

LIBCHK-359

(warning) Table of partial voltage ranges on timing arcs

Feedback

Description

This message presents a table of partial voltage ranges/swings on timing arcs. It lists all the timing arcs with partial voltage ranges that exceed the voltage threshold/tolerance specified.

What Next

The voltage range or swing check goes together with sensitivity check. If a driver cell whose output voltage never reaches full voltage swing and this cell drives a sensitive cell, there will be an issue. However, if the receiver cell is not sensitive, it should not be an issue.

Examples

The following is an example table:

```
Warning: Table of partial voltage ranges on timing arcs (LIBCHK-359)
-------------------------------------------------------------------------------
------------------
Cell name   pin/related_pin timing_type    when   VDD   Voltage range
 Relative error Type
-------------------------------------------------------------------------------
------------------
XOR3X05LMP  z/a             combinational  !a     0.99  0.980
 -1.01%         CCSN
sdffcqs_f2  q/clk           rising_edge    !a     1.20  1.122
 -6.50%         CCST
-------------------------------------------------------------------------------
------------------
```

LIBCHK-360

(information) Logic library inconsistencies found for MCMM.

Description

This information message occurs when any inconsistency in MCMM is found during cross checking the libraries. MCMM requires the following:

```
a)      Same pin (pg_pin) names, directions, types, functions and
 voltage_name
b)      Same in/output_signal_level for rail-based library and same
 related_power_pin/related_ground_pin for pg_pin-based library
c)      Same derived pin_number attribute values
d)      Different PVT values for different characterizations between
 two libraries for different operation conditions, i.e. libraries with
 same-name cells have different nominal PVT values.
e)      Same cell attributes: dont_use, dont_touch and black box
f)      Same power_down_function for output/inout pins
```

Feedback

```
g)      Power data (leakage_power etc.) exist for all opconds with
 non-zero value
h)      Same threshold_voltage_group attribute values for same cells
 across corner libraries
```

What Next

You are advised to go back to the check report to see inconsistent results and resolve them as directed by the associated LIBCHK man pages.

If you see "inconsistencies found" in the summary report, go to the related tables for details in

```
LIBCHK-300
LIBCHK-301
LIBCHK-310
LIBCHK-311
LIBCHK-312
LIBCHK-320
LIBCHK-321
LIBCHK-322
LIBCHK-323
LIBCHK-330
LIBCHK-331
LIBCHK-340
```

Any of the related LIBCHK messages will lead to the conclusion of inconsistencies found.

See Also

- LIBCHK-300
- LIBCHK-301
- LIBCHK-310
- LIBCHK-311
- LIBCHK-312
- LIBCHK-320
- LIBCHK-321
- LIBCHK-322
- LIBCHK-323
- LIBCHK-330
- LIBCHK-331
- LIBCHK-340

Feedback

LIBCHK-361

(information) Logic library inconsistencies found for UPF.

Description

This message occurs after the checking of the libraries is completed. When any inconsistency in the UPF flow is found during the checking, this message appears. UPF requires the following:

```
a)      Same pin (pg_pin) names, directions, types, functions and
 voltage_name
b)      Same in/output_signal_level for rail-based library and same
 related_power_pin/related_ground_pin for pg_pin-based library
c)      Same derived pin_number attribute values
d)      Different PVT values for different characterizations
e)      NLDM or CCS model under different voltage conditions exists
f)      Level shifter, isolation, retention and switch cells exist with
 consistent and complete attributes
g)      voltage_map and pg_pin groups exist in multi P/G pg_pin based
 library with consistent attributes
h)      Same power_down_function for output/inout pins
i)      Power data (leakage_power etc.) exist for all opconds with
 non-zero value
j)      power_down_function must be specified on all output/inout pins
k)      always_on inverter and always_on buffer cells must be specified
l)      input/output_voltage_range specified on the same pin must have
 identical values among all PVT libraries
m)      PG/PM checking for on-the-fly UPF library update
n)      Same threshold_voltage_group attribute values for same cells
 across corner libraries
```

What Next

You are advised to go back to the above check report to see inconsistent results and resolve them as directed by the associated LIBCHK man pages.

If you see "inconsistencies found" in the summary report, go back to the related tables for details in

```
LIBCHK-300
LIBCHK-301
LIBCHK-302
LIBCHK-310
LIBCHK-311
LIBCHK-312
LIBCHK-320
LIBCHK-321
LIBCHK-322
LIBCHK-323
LIBCHK-330
LIBCHK-331
```

Feedback

```
LIBCHK-332
LIBCHK-340
```

Any of the related LIBCHK messages will lead to the conclusion of inconsistencies found.

See Also

- LIBCHK-300
- LIBCHK-301
- LIBCHK-310
- LIBCHK-311
- LIBCHK-312
- LIBCHK-320
- LIBCHK-321
- LIBCHK-322
- LIBCHK-323
- LIBCHK-330
- LIBCHK-331
- LIBCHK-332
- LIBCHK-340

LIBCHK-362

(information) Logic library inconsistencies found for %s scaling.

Description

This information message occurs after the cross checking of the libraries is completed. When the tool finds any inconsistencies, such as CCS timing scaling, CCS noise scaling, or power scaling during cross checking, this message appears.

What Next

This is an information only message. No action is required.

However, you are advised to go back to the above check report to see the inconsistent results and resolve them as directed by the associated LIBCHK man pages.

When you see "inconsistencies found for CCS timing scaling" in the summary report, go back to the related tables for details in

Feedback

```
LIBCHK-300
LIBCHK-301
LIBCHK-302
LIBCHK-310
LIBCHK-311
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-332
LIBCHK-340
LIBCHK-350
```

Any of the related LIBCHK man pages will lead to this conclusion.

When you see "inconsistencies found for CCS noise scaling" in the summary report, go back to the related tables in

```
LIBCHK-300
LIBCHK-301
LIBCHK-302
LIBCHK-310
LIBCHK-311
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-340
```

Any of the related man pages (LIBCHK) will lead to this conclusion.

When you see "inconsistencies found for power scaling" in the summary report, go back to the related tables in

```
LIBCHK-300
LIBCHK-301
LIBCHK-302
LIBCHK-310
LIBCHK-311
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-341
```

Any of the related LIBCHK man pages will lead to this conclusion.

See Also

- LIBCHK-300
- LIBCHK-301

Feedback

- LIBCHK-302
- LIBCHK-310
- LIBCHK-311
- LIBCHK-320
- LIBCHK-321
- LIBCHK-330
- LIBCHK-331
- LIBCHK-332
- LIBCHK-340
- LIBCHK-350

LIBCHK-363

(information) Logic library inconsistencies found for %s comparison.

Description

This information message occurs after cross checking between the two libraries is completed. When any the tool finds inconsistencies in the Liberty syntax construct comparison or value comparison during cross checking, this message will appears. In construct comparison, the missing or existing data is reported. In value comparison, the characterization values are reported.

What Next

This is an information only message. No action is required.

However, you are advised to go back to the above check report to see inconsistent results and resolve them as directed by the associated LIBCHK man pages.

When you see "inconsistencies found" for the construct or value comparison in the summary report, go back to the related tables for details in

```
LIBCHK-300
LIBCHK-301
LIBCHK-310
LIBCHK-311
LIBCHK-312
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
```

Feedback

```
LIBCHK-340
LIBCHK-341
```

Any of the related LIBCHK man pages will lead to this conclusion.

See Also

- LIBCHK-300
- LIBCHK-301
- LIBCHK-310
- LIBCHK-311
- LIBCHK-312
- LIBCHK-320
- LIBCHK-321
- LIBCHK-330
- LIBCHK-331
- LIBCHK-340
- LIBCHK-341

LIBCHK-364

(information) Logic library inconsistencies found for %s validation.

Description

This information message occurs after validation checking between the two libraries or between two models (NLDM versus CCST/CCSN) is completed. When the tool finds any inconsistency in validation during validation checking, this message appears. If grid points are mismatched, the tool will not validate the delay, slew, and constraint values. In this case, you can ignore this message.

What Next

Please review the check report to see the inconsistent results and resolve them as directed by the related LIBCHK man pages.

When you see "inconsistencies found" in the summary report, review the related tables for details in the following messages:

```
LIBCHK-300
LIBCHK-301
```

Feedback

```
LIBCHK-310
LIBCHK-311
LIBCHK-320
LIBCHK-321
LIBCHK-330
LIBCHK-331
LIBCHK-350
```

Any of the related LIBCHK man pages will lead to this conclusion.

See Also

- LIBCHK-300
- LIBCHK-301
- LIBCHK-310
- LIBCHK-311
- LIBCHK-320
- LIBCHK-321
- LIBCHK-330
- LIBCHK-331
- LIBCHK-350

LIBCHK-365

(information) Statistics of all characterization data per library

Description

This information table reports the overall statistical analysis results of library checking with one library (group) in one row. This only includes characterization model types listed in LIBCHK-353: delay, slew, constraint, receiver_cap, ccs driver, voltage range, ccsn (dc_current), internal_power, and leakage_power. The columns in the table include the following:

- `Library name`
- `Abs/Rel mean error: Absolute/Relative mean error`
- `Abs std dev: Absolute/Relative standard deviation`
- `Cell pass rate: ratio of number of characterization model check passed cells to number of total cells checked`

Feedback

What Next

If the mean error is far from 0, the models are not so accurate. If the standard deviation is significantly large, the models are dispersed, i.e. the deviation is significant. In any case, small numbers of mean error and deviation, close to 0, should be expected for high accuracy.

Examples

The following is an example:

```
Information: Statistics of all characterization data per library
 (LIBCHK-365)
------------------------------------------------------------------------
-------------
Library name    Abs mean error Rel mean error  Abs std dev Rel std dev
 Cell pass rate
------------------------------------------------------------------------
-------------
library_typ     0.000344       1.04%           0.00176     16.86%
 79.00%
test_typ        0.000688       2.08%           0.00352     33.72%
 56.12%
------------------------------------------------------------------------
-------------
```

LIBCHK-366

(error) Logic library inconsistencies found for single mode macros.

Description

This message occurs after the checking of the single mode libraries is completed. When any incorrect data or inconsistency in the single mode libraries such as ETMs is found during the checking, this message appears. Single mode cells including ETM require the following:

```
a)      Each single model cell, e.g. ETM, has to have timing_model_type
 (for ETM, the value must be extracted) and is_macro_cell defined
b)      The single mode libraries for different modes have to have the
 same PVT
c)      Consistencies in specific library/cell/pin level attributes
 across single mode libraries at same PVTs
For details, please refer to related LC document or App Note.
The checks in check_library for ETM is consistent with merge_models
 command in PrimeTime.
Please note that for other single model cells than ETM,
 timing_model_type : extracted is not required.
```

Feedback

What Next

You are advised to go back to the above check report to see inconsistent results and resolve them as directed by the associated LIBCHK man pages.

```
LIBCHK-300
LIBCHK-301
LIBCHK-310
LIBCHK-311
LIBCHK-320
LIBCHK-321
LIBCHK-322
LIBCHK-330
LIBCHK-331
```

Any of the related LIBCHK messages will lead to the conclusion of inconsistencies found.

LIBCHK-367

(error) Logic library inconsistencies found for cell electromigration.

Description

This message occurs after checking of cell electromigration/em_max_toggle_rate across corner libraries. When structural inconsistency in the EM groups is found during the checking, this message appears.

What Next

You are advised to go back to the above check e.g. report LIBCHK-321 to see inconsistencies across the libraries and resolve them as directed by the associated LIBCHK man pages. If the electromigration table is not characterized for the expected PVT corners, in PrimePower, user can use set_em_scaling_factor command to set a scaling factor on the cell max toggle rate; however, this may still compromise the accuracy.

Examples

```
Warning: List of pins with mismatched or missing attributes in logic
 libraries (LIBCHK-321)
------------------------------------------------------------------------
------------------
                      Subgroup/              Attribute value
 Error
Cell name Pin name    Attribute           lib#1       lib#2
 Absolute  Relative
------------------------------------------------------------------------
------------------
ad3       y           em_max_toggle_rate/current_type:2
                                          existing    missing
ad3       y           em_max_toggle_rate/current_type:2/current_type
                                          peak        missing
```

Feedback

```
ad3       y           electromigration/related_pins:a
                                          existing    missing
-------------------------------------------------------------------------
------------------
```

LIBG

LIBG-1

(error) The Synopsys database is corrupted. The library is not created.

Description

A file is read in but no library is found in the file. It is most likely that the file is empty.

What Next

Check you library file to make sure it is a valid library.

Examples

```
Error: The Synopsys database is corrupted. The library is not created.
 (LIBG-1)
```

LIBG-2

(error) An invalid '%s' function string in the '%s' cell.

Description

This error message occurs when the string given is not valid for representing a Boolean logic defined in Synopsys format.

What Next

See the Library Compiler documentation to find out the valid format of the string.

Constant Boolean expressions do not allow multiple constants with operators; for example, the following expressions are not allowed:

```
function/when : "10" ;

function/when : "1 ^ 0" ;
```

Specify constant Boolean expressions as follows:

```
function/when : "0" ;

function/when : "1" ;
```

Feedback

Examples

This example causes an error message because the closing parenthesis is missing in the function string:

```
cell(libg2) {
  area : 1 ;
  pin (I0) {
        direction : input ;
        capacitance : 0 ;
  }
  pin ("Y") {
        direction : output ;
        function : "(I0" ;
        timing() {
                related_pin     : "I0" ;
                intrinsic_rise  : 1.0 ;
                rise_resistance : 0.0 ;
                intrinsic_fall  : 1.0 ;
                fall_resistance : 0.0 ;
        }
  }
```

Examples

The resulting error message lists the cause of the error:

```
Error: Line 400, An invalid '(IO' function string in the 'libg2' cell.
 (LIBG-2)
```

LIBG-3

(error) A bad '%s' pin name in the '%s' cell.

Description

This error gets detected during a *read_lib* and an *update_lib* commands. The pin name does not either exist or a previous error in any of the attributes of the pin group is detected. In this case the pin group is not recognized and the pin name is labeled as bad.

What Next

Check your library for a wrong pin name in any related attribute or for an incorrect pin group.

Examples

```
cell (libg3) {
  area : 4
  pin(A) {
    direction : input
    capacitance : 1
```

Feedback

```
    fanout_load : 1.0
  }
  pin(EN) {
    direction : input
    capacitance : 1
    fanout_load : 1.0
  }
  pin (Z) {
    direction : output
    function : "A"
    three_state : "E";       /* <-- This is wrong */
    max_fanout : 10
 }
```

Examples

```
Error: Line 426, A bad 'E' pin name in the 'libg3' cell. (LIBG-3)
```

LIBG-4

(error) In the '%s' cell, the '%s' noninput pin \n \tcannot be used in the function.

Description

The string associated with a *function* and *three_state* attributes should include only be of *input* or *inout* directions.

What Next

Check your library for a wrong direction of the pin in the function attribute. Another possibility is to check the use of the wrong pin name.

Examples

```
cell (libg4) {
  area : 4
  pin(A) {
    direction : input
    capacitance : 1
    fanout_load : 1.0
  }
  pin(EN) {
    direction : input
    capacitance : 1
    fanout_load : 1.0
  }
  pin (Z1) {
    direction : output
    function : "A"
    max_fanout : 10
 }
  pin (Z) {
```

Feedback

```
    direction : output
    function : "Z1"           /* <-- This is wrong */
    three_state : "Z1";       /* <-- This is wrong */
    max_fanout : 10
 }
```

Examples

```
Error: Line 431, In the 'libg4' cell, the 'Z1' noninput pin
        cannot be used in the function. (LIBG-4)
```

LIBG-5

(error) Cannot find the '%s' pin in the '%s' cell.

Description

This error is issued when a pin name attached to a *related_pin* or a *related_bus_pins* attribute does not exist in the cell.

What Next

Check your library for a wrong pin name.

Examples

```
cell(libg5) {
  area : 1 ;
  pin (I0) {
        direction : input ;
        capacitance : 0 ;
  }
  pin ("Y") {
        direction : output ;
        function : "I0" ;
        timing() {
                related_pin     : "IO" ; /* typo zero replaced by letter
 O */
                intrinsic_rise  : 1.0 ;
                rise_resistance : 0.0 ;
                intrinsic_fall  : 1.0 ;
                fall_resistance : 0.0 ;
        }
  }
```

Examples

```
Error: Line 403, Cannot find the 'IO' pin in the 'libg5' cell. (LIBG-5)
```

Feedback

LIBG-6

(error) Missing a related_pin for the '%s' pin timing group\n \tin the '%s' cell.

Description

This error is issued when the *related_pin* or the *related_bus_pins* attribute is missing in a timing group.

What Next

Check your library for a typo in the attribute or add it if it is missing.

Examples

```
cell(libg6) {
  area : 1 ;
  pin (I0) {
        direction : input ;
        capacitance : 0 ;
  }
  pin ("Y") {
        direction : output ;
        function : "I0" ;
        timing() {
           frelated_pin : "I0" ; /* typo f inserted before attribute */
           intrinsic_rise       : 1.0 ;
           rise_resistance : 0.0 ;
           intrinsic_fall  : 1.0 ;
           fall_resistance : 0.0 ;
        }
  }
```

Examples

```
Error: Line 399, Missing a related_pin for the 'Y' pin timing group
        in the 'libg6' cell. (LIBG-6)
```

LIBG-8

(error) In the '%s' cell, the '%s' input drives more than one function.

Description

This error is issued when attribute three_state on a port has common input ports with attribute inside ff, ff_bank, latch, latch_bank, or seq group.

What Next

Either delete one of the attributes or associate a unique string to each of them.

Feedback

Examples

```
cell(libg8) {
         area : 6.50;
         pin(D TE) {
           direction : input;
           capacitance : 3.0;
         }
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        ff("IQ","IQN") {
                next_state : "D";
                clocked_on : "CLK";
                preset     : "TE";
                }
        pin(Q) {
                direction : output;
                function : "IQ";
                three_state : "D";   /* wrong, D is shared with
 next_state. */
        }
        pin(QN) {
                direction : output;
                function : "IQN";
        }
      }
```

Examples

```
Error: Line 411, In the 'libg8' cell, the 'D' input drives more than one
 function. (LIBG-8)
```

LIBG-10

(warning) Failed to recognize the functionality of cell '%s'.

Description

The warning message is to notify users that Library Compiler fails to synthesize a netlist structure representing functionality of this cell. In order to other cells to recognize the cell, user can specifiy the "user_function_class" attribute either in the .lib file or in Design Compiler.

Note, although the function id of the cell is unknown, it may not be black-box. That is why we are saying that it may not be recognized by Design Compiler.

This message can be used to identify a cell for which pin-class conflict exists. Pin-class is defined as the set of pins which can be swapped without changing the functionality of the gate and is used for DC mapping. In the following simple example, we have PO =

Feedback

~(PAD * PI) and Y=PAD, and it will cause pin-class conflict because: After parsing the 1st function, we have pin_class(PAD) = pin(PI) because PAD and PI can be exchangable without changing the functionality of the pin PO. However it will break the functionality of the 2nd function cause Y=PAD and Y=PI are totally different.

When pin-class conflict happens, the function id of the cell is set to unknown.

What Next

Check your library.

Examples

```
cell(libg28) {
          area : 1;
          ...
          pin(PAD) {
            direction : input;
            ...
          }
          pin(PI) {
            direction : input;
            ...
          }

          pin(PO) {
            direction : output;
            capacitance : 0;
            ...
            function: "!(PAD * PI)"
          }
          pin(Y) {
            direction : output;
            capacitance : 0;
            ...
            function: "PAD"
          }
        }
```

Examples

```
Warning: Line 34,   Failed to recognize the functionality of cell '%s'.
 (LIBG-10)
```

LIBG-16

(warning) The '%s' Pin/bus on the '%s' cell has no 'function' attribute.\n \tThe cell becomes a black box.

Feedback

Description

This warning is issued when any output of a given cell does not have a valid function(missing or wrong information associated with the function of the pin). A function can be defined either by a *function* attribute, a *three_state* attribute, a *memory_read* group, or an *internal_node* attribute.

What Next

Check your library for missing or wrong attributes.

Examples

```
cell(libg16) {
  area : 1 ;
  pin (I0) {
        direction : input ;
        capacitance : 0 ;
  }
  pin ("Y") {
        direction : output ;
/*      function : "I0" ;  */
        timing() {
                related_pin     : "I0" ;
                intrinsic_rise  : 1.0 ;
                rise_resistance : 0.0 ;
                intrinsic_fall  : 1.0 ;
                fall_resistance : 0.0 ;
        }
  }
```

Examples

```
Warning: Line 39, The 'Y' Pin/bus on the 'libg16' cell has no 'function'
 attribute.
        The cell becomes a black box. (LIBG-16)
```

LIBG-17

(error) The 'function' of the '%s' pin/bus on the '%s' cell\n \tcan only be '%s' or '%s'.

Description

This error is issued when either the noninverted output (first variable) or the inverted output (second variable) of a sequential model, defined by a ff, a ff_bank, a latch, or a latch_bank group are not assigned to a primary output.

A function statement of each primary output must include either the first variable or the second variable.

Feedback

What Next

Make the appropriate correction in your library, as indicated in the error message. For more information on sequential models, refer to the *Library Compiler Reference* and *User Guide Manuals*.

Examples

```
cell(libg17) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ1";       /* wrong, should be IQ */
        }
        pin(QN) {
                direction : output;
                function : "IQN";
        }
      }
```

Examples

```
Error: Line 23, The 'function' of the 'Q'  in/bus on the 'libg17' cell
        can only be 'IQ' or 'IQN'. (LIBG-17)
```

LIBG-18

(information) The '%s' equation on the '%s' cell is not recognized.

Description

This information is issued when the function is not recognized. The function can be a complex *state_function*, a corrupted string in a *three_state*, a *clocked_on*, or a *clocked_on_also* attribute.

Feedback

What Next

Check your library to determine under which case the information is given. It it is due to the previous error LIBG-4, fix the library. Otherwise, ignore it.

Examples

```
cell(libg18) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
        }
        pin(QN) {
                direction : output;
                function : "IQN";
                three_state : "Q"; /* non-input pin not used in
 function*/
        }
      }
```

Examples

```
Information: Line 218, The 'three_state' equation on the 'libg18' cell is
 not recognized. (LIBG-18)
```

LIBG-19

(warning) Failed to recognize the functionality of cell '%s'.

Description

Library Compiler fails to synthesize a netlist structure representing functionality of this cell. If the function of a cell is too complex for LC to recognize, the cell becomes a black box. In order to other cells to recognize the cell, user can specifiy the "user_function_class" attribute either in the .lib file or in Design Compiler.

Feedback

What Next

To specify "user_function_class" attribute as described above.

LIBG-20

(error) The '%s' equation on the '%s' cell evaluates\n \tto a '%s' constant.

Description

This message is generated when Library Compiler encounters a three-state cell whose enable signal string is 1 or always evaluates to 1.

What Next

Verify the cell and check the library description of the offending cell for correctness.

Examples

```
cell(libg20) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
        }
        pin(QN) {
                direction : output;
                function : "IQN";
                three_state : "1";
        }
      }
```

Examples

```
Error: Line 218, The 'three_state' equation on the 'libg20' cell
 evaluates
        to a '1' constant. (LIBG-20)
```

Feedback

LIBG-21

(error) The derived equality relationship between '%s' and \n \t'%s' pins conflicts with the user-specified 'pin_opposite' for the '%s' cell.

Description

This error is generated if a cell is read by the library compiler with a pin_opposite attribute that conflicts with the derived equality of the pins. The function statements associated with the pins are the same.

What Next

Check your library for a typo in the function strings of the cell or remove the pin_opposite attribute.

Examples

```
cell(libg21) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
        }
        pin(QN) {
                direction : output;
                function : "IQ";        /* typo, it should be IQN */
        }
          pin_opposite("Q","QN");         /* No, they're equal. */
      }
```

Examples

```
Error: Line 215, The derived equality relationship between 'QN' and
        'Q' pins conflicts with the user-specified 'pin_opposite' for the
 'libg21' cell. (LIBG-21)
```

Feedback

LIBG-22

(error) The derived opposite relationship between '%s' and \n \t'%s' pins conflicts with the user-specified 'pin_equal' for the '%s' cell.

Description

This error is generated if a cell is read by the library compiler with a pin_equal attribute that conflicts with the derived opposite relationship of the pins . The function statements associated with the pins are opposite.

What Next

Check your library for a typo in the function strings of the cell or remove the pin_equal attribute.

Examples

```
cell(libg22) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
        }
        pin(QN) {
                direction : output;
                function : "IQN";
        }
          pin_equal("Q QN");          /* No, they're opposite. */
      }
```

Examples

```
Error: Line 215, The derived opposite relationship between 'QN' and
        'Q' pins conflicts with the user-specified 'pin_equal' for the
 'libg22' cell. (LIBG-22)
```

Feedback

LIBG-24

(information) Unable to honor the 'prefer_tied' attribute onthe '%s' pin\n \tof the '%s' cell.

Description

Library Compiler honors as many prefer_tied attributes as possible while it is still able to implement D flip flop functionality. However, it cannot honor all of them. For example, if the library developer specified *prefer_tied : 0* on all the inputs, Library Compiler honors as many as possible and the rest are ignored. If they are ignored, this message is issued during read_lib.

The prefer_tied attribute also can be used to indicate which pin(s) are tied to fixed logic during three_state degeneration for three-state pad cell.

What Next

Check your library for the use of the prefer_tied attribute.

Examples

```
cell(libg24)  {
        area : 0.0;
        pad_cell : true;
        pin(Z)  {
            is_pad : true;
            direction : output;
            drive_current : 2.0;
            function : "A";
            three_state : "en tn";
            timing()  {
                timing_type : three_state_disable;
                intrinsic_rise : 0.1;
                intrinsic_fall : 0.1;
              related_pin : "tn";
            }
            timing()  {
                timing_type : three_state_disable;
                intrinsic_rise : 0.1;
                intrinsic_fall : 0.1;
              related_pin : "en";
            }
            timing()  {
                intrinsic_rise : 0.1;
                intrinsic_fall : 0.1;
                related_pin : "tn";
            }
            timing()  {
                intrinsic_rise : 0.1;
                intrinsic_fall : 0.1;
                related_pin : "en ";
            }
```

Feedback

```
            timing()  {
                intrinsic_rise : 0.1;
                intrinsic_fall : 0.1;
                related_pin : "A";
            }
        }
        pin(A)  {
            direction : input;
            capacitance : 0.0;
        }
        pin(en)  {
            direction : input;
            capacitance : 0.500;
        }
        pin(tn)  {
            prefer_tied : "0";  /* in this case the value should be 1 */
            direction : input;
            capacitance : 0.500;
        }
    }
```

Examples

```
Information: Line 306, Unable to honor the 'prefer_tied' attribute on the
  'tn' pin
       of the 'libg24' cell. (LIBG-24)
```

LIBG-25

(warning) Duplicated test signals of '%s' type is found on\n \tthe '%s' library cell.

Description

The test_cell has more than one of the following valid signal_types: - test_scan_in - test_scan_in_inverted - test_scan_enable - test_scan_enable_inverted - test_scan_out - test_scan_out_inverted - test_scan_clock - test_scan_clock_a - test_scan_clock_b - test_clock

This warning informs you that the port in the test_cell pointed to has more than one signal_type that are listed previously.

What Next

Vendors/Library developers should check the test_cell pointed to and make sure that it is the behavior they meant to have. Otherwise,r delete the duplicate signal_type.

If a designer finds this problem, he should contact the vendor or library developer and explain the problem. This problem can only be fixed by the vendor/library developer.

Feedback

Examples

```
cell(libg25) {
            area : 12;
            pin(D) {
              direction : input;
              capacitance : 1;
            }
            pin(CK,CK2,IH) {
              direction : input;
              capacitance : 1;
            }
            pin(A,B) {
              direction : input
                capacitance : 2;
            }
            pin(SI) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_falling;
                intrinsic_rise : 2.8000;
                intrinsic_fall : 2.8000;
                related_pin : "A";
              }
              timing() {
                timing_type : hold_falling;
                intrinsic_rise : 1.2000;
                intrinsic_fall : 1.2000;
                related_pin : "A";
              }
            }
            pin(Q) {
              direction : output;
              timing() {
                timing_type : rising_edge;
                intrinsic_rise : 2.5500;
                intrinsic_fall : 2.4000;
                rise_resistance : 0.0700;
                fall_resistance : 0.0300;
                related_pin : "CK IH CK2";
              }
              timing() {
                timing_type : falling_edge;
                intrinsic_rise : 2.5500;
                intrinsic_fall : 2.4000;
                rise_resistance : 0.0700;
                fall_resistance : 0.0300;
                related_pin : "B";
              }
            }
            pin(XQ) {
              direction : output;
```

Feedback

```
    }
    test_cell(){
      pin(D CK){
        direction : input;
      }
      pin(IH CK2){              /* duplicate test_clock */
        direction : input;
        signal_type : "test_clock";
      }
      pin(SI){
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(A){
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      pin(B){
        direction : input;
        signal_type : "test_scan_clock_b";
      }
      state("IQ","IQN"){
        clocked_on : "CK CK2";
        next_state : "D";
      }
      pin(Q){
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(XQ){
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, there are two test_clock attributes for both 'IH' and 'CK2' pins.

MESSAGE EXAMPLE

```
Warning: Line 67, Duplicated test signals of test_clock type is found on
        the 'libg25' library cell. (LIBG-25)
```

LIBG-26

(error) The '%s' test cell pin on the '%s' cell\n \thas no 'function' attribute. The test cell is removed.

Feedback

Description

The specified pin has neither a test *signal_type* nor a *function* attribute. This incomplete functional description results in a black-box test cell, which is removed from the library.

What Next

Add a proper *function* attribute or *signal_type* attribute to the faulty pin group.

Examples

```
cell(libg26) {
            area : 12;
            pin(D) {
              direction : input;
              capacitance : 1;
            }
            pin(CK IH) {
              direction : input;
              capacitance : 1;
            }
            pin(A,B) {
              direction : input
                capacitance : 2;
            }
            pin(SI) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_falling;
                intrinsic_rise : 2.8000;
                intrinsic_fall : 2.8000;
                related_pin : "A";
              }
              timing() {
                timing_type : hold_falling;
                intrinsic_rise : 1.2000;
                intrinsic_fall : 1.2000;
                related_pin : "A";
              }
            }
            pin(Q) {
              direction : output;
              timing() {
                timing_type : rising_edge;
                intrinsic_rise : 2.5500;
                intrinsic_fall : 2.4000;
                rise_resistance : 0.0700;
                fall_resistance : 0.0300;
                related_pin : "CK IH";
              }
              timing() {
                timing_type : falling_edge;
```

Feedback

```
        intrinsic_rise : 2.5500;
        intrinsic_fall : 2.4000;
        rise_resistance : 0.0700;
        fall_resistance : 0.0300;
        related_pin : "B";
      }
    }
    pin(XQ) {
      direction : output;
    }
    test_cell(){
      pin(D CK){
        direction : input;
      }
      pin(IH ){
        direction : input;
        signal_type : "test_clock";
      }
      pin(SI){
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(A){
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      pin(B){
        direction : input;
        signal_type : "test_scan_clock_b";
      }
      state("IQ","IQN"){
        clocked_on : "CK CK2";
        next_state : "D";
      }
      pin(Q){
        direction : output;
      }
      pin(XQ){
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, the pin 'Q' needs to have a function : "IQ" or signal_type : "test_scan_out" statement

MESSAGE EXAMPLE

```
Error: Line 385, The 'Q' test cell pin on the 'libg26' cell
        has no 'function' attribute. The test cell is removed. (LIBG-26)
```

Feedback

LIBG-27

(warning) The '%s' pin is eliminated from the '%s' pin \n \tfunction on the '%s' cell. The cell becomes a black box.

Description

This message is issued to warn users about the redundant ports in a function string. Redundant ports are ports which are eliminated from the boolean function due to normal boolean simplification.

What Next

Check the library for a possible error in the function string.

Examples

```
cell(libg27) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\
              -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
  }
  pin(QB) {
    direction : output;
    state_function : "D * 0";
  }
}
```

Examples

```
Warning: Line 448, The 'D' pin is eliminated from the 'QB' pin
        function on the 'libg27' cell. The cell becomes a black box.
 (LIBG-27)
```

Feedback

LIBG-28

(warning) The '%s' three state pin has no 'function' or\n \tthe function is too complex to be recognized;\n \tthe '%s' cell becomes a black box.

Description

This message identifies a cell for which one of its output pins with a three_state attribute has no valid function defined, or its function is too complex to be mapped onto. In this case the library compiler treats the cell as a black box.

What Next

Check your library and add the functional information, in case it is absent, to the tri-statable pin. The functional model can be defined by the 'function' attribute, or ff, latch, memory, or unigen statements.

Examples

```
cell(libg28) {
          area : 1;
          pin(A) {
            direction : input;
            capacitance : 0;
          }
          pin(TA) {
            direction : output;
            three_state : "A'"; /* missing a function attribute */
          }
        }
```

Examples

```
Warning: Line 34, The 'TA' three state pin has no 'function' or
        the function is too complex to be recognized;
        the 'libg28' cell becomes a black box.  (LIBG-28)
```

LIBG-29

(warning) The state group needs more statements to be\n \tmeaningful; cell becomes black-box.

Description

This message is issued when a clocked_on or a next_state statement is missing. This message also appears when a latch does not have a minimum of two force statements (force_00, force_01, force_10, and force_11). Library Compiler treats a cell without a functional model as a black-box.

Feedback

What Next

Check the library for a wrong model and add the missing statement of the corresponding group.

Examples

```
cell(libg29) {
            area : 12;
            pin(D) {
              direction : input;
              capacitance : 1;
            }
            pin(CK) {
              direction : input;
              capacitance : 1;
            }
            pin(Q) {
              direction : output;
            }
              state("IQ","IQN"){
                next_state : "D";       /* clocked_on : "CK"; missing */
              }
          }
```

Examples

```
Warning: Line 460, The state group needs more statements to be
        meaningful; cell becomes black-box. (LIBG-29)
```

LIBG-30

(warning) The '%s' equation on the '%s' cell evaluates\n \tto a constant '%s'. Since this implies the output will never become\n \t%s, this equation is ignored.

Description

The sequential library cell has both a force_00 and a force_11 declared. The translation algorithm cannot handle library cells with both of these declarations. This warning message is specific to structural models.

What Next

Declare instead either a pair of force_10 and force_01, force_10 and force_11, force_00 and force_01, force_00 and force_10, or force_01 and force_11. The Q and QN outputs of the specified sequential cell are not complementary. Possible reasons for this are: 1. The library specifies that the outputs are not complementary; 2. The functions driving the force_00 and force_11 inputs of the degenerated sequential cell are not logical zero. For purposes of verification, every sequential cell is degenerated into a primitive sequential cell. The outputs (sourcepoints) of the primitive are Q and QN. The inputs (endpoints)

of the primitive are next_state, force_00, force_01, force_10, force_11, clocked_on, and clocked_on_also (for Master-slave cells only). The functions driving the force endpoints characterize the asynchronous properties of the primitive sequential cell. The library might also contain an attribute asserting that the outputs Q and QN are complementary. The force_01 function represents the conditions under which the Q pin can be driven to zero and the QN driven to 1 simultaneously. The other force inputs have a similar interpretation. When the attribute is not present, verification tries to determine that Q and QN are effectively complementary by establishing that both force_00 and force_11 are logically zero. The exact degeneration process depends on the library characterization of the sequential cell and is not described here.

Sequential cells should be modeled using the flip-flop and latch attributes. If you model sequential cells with state attributes, use a local function to describe the asynchronous behavior of each output pin. These functions are hard-coded as async_IQ and async_IQN. The async_IQ, async_IQN, and active functions are based on the forceXX expressions. An example is this flip-flop with Preset and Clear: state (IQ,IQN) { ... force00 : "!CD & ! SD" force01 : "!CD & SD" force10 : "CD & !SD" ... } When CD is low, Q is always 0, so the VHDL library generator ORs these two expressions together; instead of (!CD & SD) | (! CD & !SD), the equation becomes !CD. The ORed expression is simplified by Boolean algorithms, which use only 1 and 0 values. If you specify an X for one of these values, the library generator might modify the results.

Examples

```
cell(libg30) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
        }
        pin(QN) {
                direction : output;
                function : "IQN";
                three_state : "0";
        }
      }
```

Feedback

Examples

```
Warning: Line 218, The 'three_state' equation on the 'libg30' cell
 evaluates
        to a constant '0'. Since this implies the output will never
 become
        tri-stated, this equation is ignored. (LIBG-30)
```

LIBG-31

(warning) The test cell on cell '%s' does not have any function.

Description

This message indicates that no output port of the test cell has a function attribute.

What Next

An output port in the test cell must have a function attribute, a signal_type attribute, or both. At least one output port must have a function attribute. The function attribute can reflect only the nontest behavior of the cell.

LIBG-32

(error) The '%s' parallel sequential cell must use bus/bundle for outputs.

Description

One of the requirements of the parallel sequential cells that are described by the ff_bank or latch_bank groups, is that all the outputs are busses or bundles.

This message applies to a parallel sequential cell whose outputs are not busses or bundles. However, this message does not apply to a multibit scan cell with a single-bit output pin, when the *function* attribute is not specified on the pin.

What Next

Check your library for parallel sequential cells with single-bit output pins with the *function* attribute specified on them. Define these pins as busses or bundles.

Examples

```
cell (LSFDS) {
                area : 31.000000 ;
                dont_touch : true ;
                dont_use : true ;
                bus (D) {
                        bus_type : BUS4;
                        direction : input ;
                        capacitance : 2.000000 ;
```

Feedback

```
                }
                pin (CK) {
                        direction : input ;
                        capacitance : 1.000000 ;
                }
                ff_bank (IQ,IQN,4) {
                        next_state : "D" ;
                        clocked_on : "CK" ;
                }
                bus (Q) {
                        bus_type : BUS4;
                        direction : output ;
                        function : "IQ" ;
                }
                pin (SO) {
                        direction : output ;
                        function : "IQN" ;
                }
        }
```

In this case, the pin 'SO' must be defined as a bus of type BUS4.

Examples

```
Error: Line 168, The 'libg32' parallel sequential cell must use
bus/bundle for outputs. (LIBG-32)
```

LIBG-33

(warning) In the '%s' cell, the '%s' inout pin\n \tcannot have feedback in its function. The cell becomes a black box.

Description

The inout pin is in its own function. Library Compiler does not support combinational functions with feedback.

What Next

Either break the feedback or try to use a sequential definition.

Examples

```
cell (libg33) {
    pin(C) {
        direction : input;
    }
    pin(D) {
        direction : inout;
        function : "A'";
        three_state : "C";
    }
```

Feedback

```
    pin(A) {
        direction : inout;
        function : "D'";
        three_state : "C"; /* It will cause loop combinational function
 loop in the design.
                           * To break the loop, change "C" into "C'" */
    }
  }
```

Examples

```
Warning: Line 64, Cell 'libg33', In the 'libg33' cell, the 'A' inout pin
        cannot have feedback in its function. The cell becomes a black
 box. (LIBG-33)
```

LIBG-34

(error) The '%s' pin in the '%s' cell has the '%s' direction\n \tThe direction must be '%s'.

Description

The pin on the programmable cell must have the direction specified.

What Next

Replace the pin direction attribute by the correct direction.

LIBG-35

(warning) The 'nextstate_type' attribute on the '%s' pin/bus in\n \tthe '%s' cell is inconsistent with its function. The attribute is ignored.

Description

In a pin group, nextstate_type defines the type of a next_state attribute to be used in an ff group, a seq group, or a ff_bank group.

Any pin with the *nextstate_type* attribute must be in the *nextstate* function. A consistency check is also made between the pin's nextstate_type attribute and the nextstate function. This message is generated when the attribute 'nextstate_type' does not match the functional information specified in the cell's sequential state description.

What Next

Check your library for a pin with a nextstate_type attribute but not used in the next_state statement of a sequential group and correct the inconsistency.

Feedback

Examples

```
cell(libg35) {
        area : 6.50;
        pin(D) {
           direction : input;
           capacitance : 3.0;
        }
        pin(CLK) {
           direction : input;
           capacitance : 1.5;
        }
        pin(SET) {
           direction : input;
           nextstate_type : scan_in;
           capacitance : 3.0;
        }

        ff("IQ","IQN") {
           next_state : "D";
           clocked_on : "CLK";
           preset     : "SET'";
        }

        pin(Q) {
           direction : output;
           function : "IQ";
        }
        pin(QN) {
           direction : output;
           function : "IQN";
        }
   }
```

Examples

```
Warning: Line 153, The 'nextstate_type' attribute on the 'SET' pin/bus in
        the 'libg35' cell is inconsistent with its function. The
 attribute is ignored. (LIBG-35)
```

LIBG-36

(warning) In the '%s' cell, the '%s' input drives more than one\n \tfunction. The cell might not be optimally used.

Description

This warning is issued when more than one attribute inside ff, ff_bank, latch, latch_bank, or seq group share one or more inputs pin names, or when attribute function/ state_function and three_state on a port have common input pins.

Feedback

What Next

Check your library for shared input pins and associate a unique string to each of them.

Examples

```
cell(libg36) {
         area : 6.50;
         pin(D TE) {
           direction : input;
           capacitance : 3.0;
         }
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        ff("IQ","IQN") {
                next_state : "D TE";
                clocked_on : "CLK";
                preset     : "D'";
                }

        pin(Q) {
                direction : output;
                function : "IQ";
        }
        pin(QN) {
                direction : output;
                function : "IQN";
        }
      }
```

In this case, the input pin 'D' is present in the next_state's string and the preset's string.

Examples

```
Warning: Line 189, In the 'libg36' cell, the 'D' input drives more than
 one function.
        The cell might not be optimally used. (LIBG-36)
```

LIBG-37

(warning) The '%s' pin/bus is unused in the '%s' cell.\n

Description

This message is generated when an input pin is not used in the functionality of the cell.

What Next

Either delete the unused input pin or add it the functionality of the cell.

Feedback

Examples

```
cell(libg37) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
        }
        pin(QN) {
                direction : output;
                function : "IQN";
              }
  }
```

Examples

```
Warning: Line 202, The 'SET' pin/bus is unused in the 'libg37' cell.
 (LIBG-37)
```

LIBG-38

(warning) The '%s' enable pin with a three_state attribute in the\n \t '%s' cell should have non-unate timing arcs.

Description

Tri-state enable pins should have "non-unate" timing arcs because the transition depends on the data input. If incorrect timing sense is detected, a warning is issued.

What Next

Change the timing sense to "non-unate."

LIBG-39

(warning) The '%s' asynchronous input of the '%s' cell is inconsistent in active level.

Feedback

Description

The asynchronous input is inconsistent in "active" level. If "active low," the clear timing arc is *positive-unate*, the preset timing arc is *negative unate*, and the intrinsic fall in recovery constraint is *zero*.

If "active high," the clear timing arc is *negative-unate*, the preset timing arc is *positive-unate*, and the intrinsic rise in recovery constraint is *zero*.

Since the active level of asynchronous input is not explicitly specified, the warning message simply states that, due to inconsistency, the active level of the asynchronous pin cannot be determined by the set of associated timing groups. An inconsistency is found at the given line number.

This message can show up in situations when the clear/preset attribute inside ff/latch group is a complex Boolean expression of signal pins instead of a single input pin. Due to these complex Boolean values for the clear/preset attributes, user should ignore this warning message after making sure that all timing arc(s) have been modeled correctly. Even after generating this warning LC will store the user specified timing arcs as modeled in the library.

What Next

Determine the asynchronous pin active level. Check the current timing group, and, if inconsistent, make the modification. Otherwise, check other timing groups associated with this asynchronous pin, and change any inconsistency.

Examples

```
cell("libg39") {
  area : 5 ;
  state("IQ","IQN") {
    force_00 : "S*R" ;
    force_01 : "R*!S" ;
    force_10 : "S*!R" ;
  }
  pin("S") {
    direction : input ;
    capacitance : 0.145 ;
  }
  pin("R") {
    direction : input ;
    capacitance : 0.145 ;
  }
  pin("Q") {
    direction : output ;
    function : "IQ" ;
    timing() {
      timing_type       : preset ;
      timing_sense      : negative_unate ;
      rise_resistance   :  1.000 ;
```

Feedback

```
      related_pin       : "S" ;
    }
    timing() {
      timing_type       : clear ;
      timing_sense      : negative_unate ;
      intrinsic_fall    :  1.000 ;
      fall_resistance   :  1.000 ;
      related_pin       : "R" ;
    }
  }
  pin("QN") {
    direction : output ;
    function : "IQN" ;
    timing() {
      timing_type       : clear ;
      timing_sense      : negative_unate ;
      intrinsic_fall    :  1.000 ;
      fall_resistance   :  1.000 ;
      related_pin       : "S" ;
    }
    timing() {
      timing_type       : preset ;
      timing_sense      : positive_unate ;
      intrinsic_rise    :  1.000 ;
      rise_resistance   :  1.000 ;
      related_pin       : "R" ;
    }
  }
}
```

To fix the warning, the timing arc of S in the pin 'Q' has to be positive_unate.

Examples

```
Warning: Line 32, The 'S' asynchronous input of the 'libg39' cell is
 inconsistent in active level. (LIBG-39)
```

LIBG-40

(warning) The '%s' clock/gate input of the '%s' cell is inconsistent in active edge/level.

Description

A clock is consistent in triggering edge. If positive edge is triggered, only *rising_edge*, *setup_rising*, *hold_rising*, and *recovery_rising* timing types are allowed. If negative edge is triggered, only *falling_edge*, *setup_falling*, *hold_falling*, and *recovery_falling* timing types are allowed. Since the clock-pin triggering edge is not explicitly specified, the warning message simply indicates that, due to inconsistency, the triggering edge of the clock pin cannot be derived from its related timing-group data. An inconsistency is found at the given line number.

Feedback

A gate is consistent in active level. If "active low," only *non_unate*, *falling_edge*, *setup_rising*, *hold_rising*, and *recovery_rising* timing types are allowed. If "active high," only *non_unate*, *rising_edge*, *setup_falling*, *hold_falling*, and *recovery_falling* are allowed. Since the gate-pin active level is not explicitly specified, the warning message simply indicates that, due to inconsistency, the active level of the gate pin cannot be derived from its related timing group data. An inconsistency is found at the given line number.

There is one exception: *rising_edge* and *falling_edge* are not checked if the library cell is a black box.

What Next

For a clock pin, determine the triggering edge first. Check the current timing group data, and modify timing-group data if found to be inconsistent with clock-triggering edge. Otherwise, check other timing groups that are related to the clock pin, and, if inconsistency is found, make the change.

For a gate pin, determine the active level first, check the current timing-group data, and modify timing-group data if found to be inconsistent with gate-active level. Otherwise, check other timing groups that are related to the gate pin, and, if inconsistency is found, make the change.

Examples

```
cell(RAM1) {
        area : 4;
        pin(D) {
        direction : input;
        capacitance : 2;
        timing() {
              timing_type : setup_rising;
              intrinsic_rise : 1.00;
              intrinsic_fall : 1.00;
              related_pin : "WR";
            }
        }
        pin(WR) {
            direction : input;
            capacitance : 1;
        }
        state ("IQ","IQN") {
            force_01 : "D' WR";
            force_10 : "D WR ";
        }
        pin(QN) {
            direction : output;
            function : "IQN";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.00;
              intrinsic_fall : 1.00;
```

Feedback

```
            rise_resistance : 0.1000;
            fall_resistance : 0.1000;
            related_pin : "WR";
          }
        }
    }
```

Examples

```
Warning: Line 266, The 'WR' clock/gate input of the 'RAM1' cell is
 inconsistent in active edge/level. (LIBG-40)
```

LIBG-41

(warning) The 'when' attribute (%s) uses pins\n \tthat cannot be found in %s (%s).

Description

In a combinational cell, the following pins are allowed to appear in the *when* attribute of the state-dependent timing arc:

1) Pins in the *function* attribute for a combinational timing arc.

2) Pins in the *three_state* attribute for a three_state_disable timing arc.

This warning informs you that one of the previous restrictions has been violated.

What Next

Check the *when* attribute and correct any wrong information in the string or in the timing type.

Examples

```
cell(libg41) {
  area : 2;
  pin(D1 D0 S0 EN) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "S0'D0 + S0 D1";
    three_state : "EN";
    timing() {
      timing_sense : non_unate;
      timing_type : three_state_disable;
      intrinsic_rise : 1.00;
      intrinsic_fall : 1.00;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "EN";
```

Feedback

```
    }
    timing() {
      timing_sense : non_unate;
      intrinsic_rise : 1.00;
      intrinsic_fall : 1.00;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "EN D1 D0 S0";
    }
    timing() {
      when : "S0'D0 + S0 D1' + EN";
      sdf_cond : "(D1 == 1'b0 && S0 == 1'b1) || (D0 == 1'b1 && S0 ==
 1'b0)";
      timing_sense : positive_unate;
      intrinsic_rise : 1.00;
      intrinsic_fall : 1.00;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "S0";
    }
  }
}
```

In this case, the pin 'EN' is not included in the function string of the pin 'Z'.

Examples

```
Warning: Line 69, The 'when' attribute (S0'D0 + S0 D1' + EN) uses pins
        that cannot be found in function attribute (S0'D0 + S0 D1).
 (LIBG-41)
```

LIBG-42

(error) The '%s' related pin of the '%s' cell has clear/preset\n \ttiming arcs but is not asynchronous.

Description

The timing group is a clear/preset arc but the related pin is not asynchronous. The related pin must be in a force statement or in a clear/preset statement to be in a clear/preset timing arc.

What Next

Define the related pin as asynchronous in the functional description or remove the timing arc.

Examples

```
cell (libg42)  {
        area : 8.000;
        pin(D)  {
```

Feedback

```
                direction : input;
                capacitance : 0.100;
        }
        pin(CK)  {
                direction : input;
                capacitance : 0.100;
        }
        ff(IQ,IQB)  {
                next_state : "D";
                clocked_on : "CK";
        }
        pin(QB)  {
                direction : output;
                function : "IQB" ;
                timing()  {
                        timing_type : rising_edge;
                        intrinsic_rise : 2.000;
                        intrinsic_fall : 3.000;
                        rise_resistance : 8.000;
                        fall_resistance : 6.000;
                        related_pin : "CK";
                }
        }
        pin(Q)  {
                direction : output;
                function : "IQ" ;
                timing()  {
                        timing_type : clear ;
                        timing_sense : negative_unate ;
                        intrinsic_fall : 1.000;
                        fall_resistance : 4.000;
                        related_pin : "QB";
                }
        }
}
```

Examples

```
Error: Line 270, The 'QB' related pin of the 'libg42' cell has
 clear/preset
        timing arcs but is not asynchronous. (LIBG-42)
```

LIBG-43

(error) The '%s' related pin of this timing arc is an output pin and\n \tthe timing_sense is not specified.

Description

If the related pin of a timing arc is an output pin, provide the *timing_sense* attribute.

Feedback

What Next

Check the functionality of the cell, and provide the correct *timing_sense* to this timing arc.

Examples

```
cell(libg43) {
      area : 8.000;
      pin(A E) {
        direction : input;
        capacitance : 1.00;
      }
      pin(B) {
        direction : output;
        function : "!A";
        timing() {
          related_pin : "A";
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
        }
      }
      pin(C) {
        direction : inout;
        function : "A";
        three_state : "E";
        timing() {
          related_pin : "E";
          timing_type : three_state_disable;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
        }
        timing() {
          related_pin : "E";
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
        }
        timing() {
          related_pin : "B";
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
        }
      }
    }
```

In this case, a timing_sense attribute is missing in the timing group between the inout pin 'C' and the output pin 'B'.

Examples

```
Error: Line 75, The 'B' related pin of this timing arc is an output pin
 and
        the timing_sense is not specified. (LIBG-43)
```

Feedback

LIBG-44

(error) The logic represented by the 'when' string (%s) in this\n \ttiming group is not mutually exclusive with the logic represented by\n \tthe 'when' string (%s) in the timing group on line %d.

Description

The logic represented by the 'when' string of all state-dependent timing arcs between a pair of pins should be mutually exclusive. If it isn't, Library Compiler is not be able to determine which timing arc to use to propagate signal through the path when the condition causes both of them to be evaluated 'TRUE'.

What Next

Check the 'when' strings of both timing groups for wrong information and fix it.

Examples

```
cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "S0'D0 + S0 D1";
        timing() {
          timing_sense : non_unate;
          intrinsic_rise : 1.00;
          intrinsic_fall : 1.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : " D0 D1";
        }
        timing() {
          when : "S0'D0 + S0 D1'";
          when : "D1' S0 + S0'D0 ";
          sdf_cond : "(D1 == 1'b0 && S0 == 1'b1) || (S0 == 1'b0 && D0 ==
 1'b1)";
          timing_sense : positive_unate;
          intrinsic_rise : 1.00;
          intrinsic_fall : 1.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
        timing() {
          when : "D1 S0 + S0'D0";
          sdf_cond : "(D1 == 1'b1 && S0 == 1'b1) || (S0 == 1'b0 && D0 ==
 1'b0)";
```

Feedback

```
          timing_sense : non_unate;
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
        timing() { /* default */
          intrinsic_rise : 1.00;
          intrinsic_fall : 2.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
      }
    }
```

In this case, the second when attribute's string has a typo. It should be "D1 S0 + S0'D0'"; where the pin D0 should be ticked according to the sdf_cond attribute's string.

Examples

```
Error: Line 258, The logic represented by the 'when' string (S0'D0 + S0
 D1') in this
        timing group is not mutually exclusive with the logic represented
 by
        the 'when' string (D1 S0 + S0'D0) in the timing group on line
 268. (LIBG-
44)
```

LIBG-44w

(warning) The logic represented by the 'when' string (%s) in this\n \ttiming group is not mutually exclusive with the logic represented by\n \tthe 'when' string (%s) in the timing group on line %d.

Description

The logic represented by the 'when' string of all state-dependent timing arcs between a pair of pins should be mutually exclusive. If it isn't, Library Compiler is not be able to determine which timing arc to use to propagate signal through the path when the condition causes both of them to be evaluated 'TRUE'.

The following example shows an instance where this message occurs:

```
cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
        direction : input;
        capacitance : 1;
      }
```

Feedback

```
      pin(Z) {
        direction : output;
        function : "S0'D0 + S0 D1";
        timing() {
          timing_sense : non_unate;
          intrinsic_rise : 1.00;
          intrinsic_fall : 1.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : " D0 D1";
        }
        timing() {
          when : "S0'D0 + S0 D1'";
          when : "D1' S0 + S0'D0 ";
          sdf_cond : "(D1 == 1'b0 && S0 == 1'b1) || (S0 == 1'b0 && D0 ==
1'b1)";
          timing_sense : positive_unate;
          intrinsic_rise : 1.00;
          intrinsic_fall : 1.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
        timing() {
          when : "D1 S0 + S0'D0";
          sdf_cond : "(D1 == 1'b1 && S0 == 1'b1) || (S0 == 1'b0 && D0 ==
1'b0)";
          timing_sense : non_unate;
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
        timing() { /* default */
          intrinsic_rise : 1.00;
          intrinsic_fall : 2.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
      }
    }
```

In this case, the second when attribute's string has a typo. It should be "D1 S0 + S0'D0'"; where the pin D0 should be ticked according to the sdf_cond attribute's string.

The following is an example message:

```
Warning: Line 258, The logic represented by the 'when' string (S0'D0 + S0
 D1') in this
        timing group is not mutually exclusive with the logic represented
 by
```

Feedback

```
        the 'when' string (D1 S0 + S0'D0) in the timing group on line
 268. (LIBG-
44w)
```

What Next

Check the 'when' strings of both timing groups for wrong information and fix it.

LIBG-45

(error) The 'timing_sense' attribute is missing. It is required\n \tfor '%s' timing arc.

Description

For timing arcs of timing_type 'clear' or 'preset', timing_sense is a required attribute. It can be either 'positive_unate' or 'negative_unate' or 'non_unate'.

What Next

Check your logic between the input and output pins and put the appropriate timing_sense in the timing group.

Examples

```
cell(libg45) {
      area : 9;
      pin(D CP CD) {
        direction : input;
        capacitance : 1;
      }
      state("IQ","IQN") {
        next_state : "D";
        clocked_on : "CP";
        force_01   : "CD'";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        timing() {
          timing_type : clear;  /* timing_sense missing */
          intrinsic_fall : 0.77;
          fall_resistance : 0.0523;
          related_pin : "CD";
        }
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        timing() {
          timing_type : preset;
          timing_sense : negative_unate;
          intrinsic_rise : 0.87;
```

Feedback

```
          rise_resistance : 0.1523;
          related_pin : "CD";
        }
      }
    }
```

In this case, there is a missing timing_sense attribute with positive_unate for the 'clear' timing arc of the pin 'Q'.

Examples

```
Error: Line 256, The 'timing_sense' attribute is missing. It is required
        for 'clear' timing arc. (LIBG-45)
```

LIBG-46

(error) The '%s' pin of the '%s' cell is not a clock/enable pin and\n \tcannot be used in the 'related_pin' of timing arc with the \n \t'%s' timing_type.

Description

Pin in the 'related_pin' of the timing group with the timing_type rising_edge or falling_edge should be a clock/enable pin.

What Next

Check your library to see if you place the wrong pin in the 'related_pin' attribute or you have specified wrong 'timing_type'.

Examples

```
cell(libg46) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
    min_period : 99
    timing() {
      timing_type : rising_edge
      intrinsic_rise : 1.640000
      intrinsic_fall : 1.880000
      rise_resistance : 0.182000
      fall_resistance : 0.059000
      related_pin : "D"
    }
  }
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\
```

Feedback

```
            -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    inverted_output : FALSE;
    timing() {
      timing_type : rising_edge
      intrinsic_rise : 1.640000
      intrinsic_fall : 1.880000
      rise_resistance : 0.182000
      fall_resistance : 0.059000
      related_pin : "CP"
    }
  }
  pin(QB) {
    direction : output;
    internal_node : "Q";
    inverted_output : TRUE;
    timing() {
      timing_type : rising_edge
      intrinsic_rise : 1.640000
      intrinsic_fall : 1.880000
      rise_resistance : 0.182000
      fall_resistance : 0.059000
      related_pin : "CP"
    }
  }
}
```

Examples

```
Error: Line 120, The 'D' pin of the 'libg46' cell is not a clock/enable
 pin and
        cannot be used in the 'related_pin' of timing arc with the
        'rising_edge' timing_type. (LIBG-46)
```

LIBG-47

(warning) Cell(%s): The state table entries have been expanded.\n \tThe following %d %s of overlapping entries %s been found:\n %s\n \tFor each occurrence, the first "rule out" entry is used.

Description

This message informs the user that overlapping entries have been found in the state table, and that the first one encountered is being used. Overlapping entries can occur when entries (that is, rules) in the *table* attribute of the *statetable* group are expanded. Overlapping means that for a single input value combination, there are multiple next

Feedback

internal node combinations. During expansion, some entries might overlap with others; the entry highest in the table overrides those below it.

NOTE:

```
All inputs that are always don't care are not mentioned in
        the input string of occurrences.
```

What Next

You can avoid receiving this message by once explicitly listing the next internal node for every permutation of L and H for the current inputs, previous inputs, and current states.

Examples

```
statetable ( "D WR WRN", "Q QN") {
    table : "L/H H L : - - : L/H H/L,\\ /* rule 1 */
              -   - - : - - : N   N";   /* rule 2 */
  }
```

During the expansion of the table into an ordered table with L and H inputs and L, H, X, and N next internal nodes, rule 1 expands into

```
L H L : - - : L H /* rule 3 */
            H H L : - - : H L /* rule 4 */
```

and rule 2 expands into

```
L H L : - - : N N /* rule 5 */
            H H L : - - : N N /* rule 6 */
```

In this case, there is an overlap between rules 3 and 5 and rules 4 and 6.

Examples

```
Warning: Line 214, Cell(libg47): The state table entries have been
 expanded.
        The following 2 occurrences of overlapping entries have been
 found:
        occurrence 1: rule in: "L H L", rule out #1: "L H", rule out #2:
 "N N"
        occurrence 2: rule in: "H H L", rule out #1: "H L", rule out #2:
 "N N"
        For each occurrence, the first "rule out" entry is used.
 (LIBG-47)
```

LIBG-48

(warning) Cell(%s): The following %d %s, which includes\n \tcurrent and delayed input values in the state table, %s unspecified: %s\n \tOutputs are made unknown.

Feedback

Description

In the 'table' attribute of the 'statetable' group, some entries (rules) are unspecified. All permutations of the input nodes are not specified by the table. Therefore, the internal node is made unknown for all of the missing entries.

What Next

This warning can be eliminated by carefully specifying the state table to avoid unspecified entries.

NOTE:

```
The input edges symbols, {"R", "~R", "F", "~F"}, represent
        permutations of L and H for the delayed input and the current
        input. Every edge-sensitive input(one with at least one
        input edge symbol) is expanded into two level-sensitive
        inputs: the current input value and the delayed input value.
        For example, the input edge symbol "R" expands to "L" for the
        delayed input value and "H" for the current input value.
```

Examples

```
statetable ( "D CP", "Q QB") {
    table : "L R : - - : L H,\\\n
              - ~R : - - : N   N";
  }
```

During the table expansion, the output for the input permutation of CP* (delayed), CP, and D: "L H H" is not specified. The output is set to "X X".

Examples

```
Warning: Line 134, Cell(libg48): The following 1 entry, which includes
        current and delayed input values in the state table, is
 unspecified:
        inputs: CP*, CP, D
                "011"
        Outputs are made unknown. (LIBG-48)
```

LIBG-49

(error) Cell(%s): '%s' token in "%s" field is not recognized.

Description

The token is not a valid state table token for that field in the table. The valid tokens for input nodes are {L, H, -, L/H, H/L, R, F, ~R, and ~F}. The valid tokens for current internal nodes are {L, H, -, L/H, and H/L}. The valid tokens for next internal nodes are {L, H, L/H, H/L, X, and N}. Therefore, the table is deleted.

Feedback

What Next

Replace the invalid token with a valid one.

LIBG-50

(error) Cell(%s): Incorrect "%s" field size in table.\n \tSize found: %d, expecting: %d.

Description

In the 'table' attribute of the 'statetable' group, either the input nodes, the current internal nodes, or the next internal nodes has an incorrect number of tokens.

What Next

Fix the number of entries in the table.

Examples

```
statetable ( "D CP", "Q QB") {
    table : "L/H R  : - : L/H H/L,\\\n
             -   ~R : - : N   N";
  }
```

The current field must have 2 tokens instead of 1. Change the state table to

```
statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
  }
```

Examples

```
Error: Line 134, Cell(libg50): Incorrect "current" field size in table.
        Size Found: 1, expecting: 2. (LIBG-50)
```

LIBG-51

(error) Cell(%s): The '%s' port has too many port names in 'input_map'.\n \tNumber of ports specified is %d, the maximum number expected is %d.

Description

There are too many port names specified in the 'input_map' attribute of the port. The maximum number of ports in 'input_map' is equal to the number of input nodes plus the number of internal nodes plus the number of input nodes that are edge sensitive. Therefore, the table is deleted.

What Next

Remove some of the port names.

Feedback

Examples

```
statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
  }
  pin(Q) {
    direction : output;
    function : "IQ";
    internal_node : "Q";
    input_map : "D CP Q QB CP CP";
    ...
  }
```

The maximum number of port names expected in the input_map attribute is 5: 2 input nodes (D, CP), one delayed input (CP*), and 2 internal nodes(Q, QB).

Examples

```
Error: Line 139, Cell(libg51): The 'Q' port has too many port names in
 'input_map'.
       Number of ports specified is 6, the maximum number expected is 5.
 (LIBG-51)
```

LIBG-52

(error) Cell(%s): The '%s' port requires either 'internal_node' or\n \t'state_function'.

Description

The output or inout port does not have either an 'internal_node' attribute or a 'state_function' attribute even though a state table is defined. If a state table is defined, every output and inout port must have either an 'internal_node' or a 'state_function'. Therefore, the table is deleted.

What Next

Add either an 'internal_node' attribute or a 'state_function' attribute to the port.

Examples

```
statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    function : "IQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
```

Feedback

```
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
```

In this example, the pin Q is missing the *state_function* or the *internal_node* attribute.

Examples

```
Error: Line 139, Cell(libg52): The 'Q' port requires either
 'internal_node' or
        'state_function'. (LIBG-52)
```

LIBG-53

(error) Cell(%s): The 'internal_node' in the '%s' port\n \tdoes not match any internal node name in the state table.

Description

The 'internal_node' attribute on the port is not equal to the name of any internal node in the state table. Every 'internal_node' attribute must match one of the internal node names. Therefore, the table is deleted.

What Next

Change the 'internal_node' attribute to equal an internal node name, or change an internal node name to equal the 'internal_node' attribute.

Examples

```
statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    function : "IQ";
    internal_node : "Q1";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
```

Feedback

In this case, Q1 is not an internal node in the state table.

Examples

```
Error: Line 139, Cell(libg53): The 'internal_node' in the 'Q' port
        does not match any internal node name in the state table.
 (LIBG-53)
```

LIBG-54

(information) Cell(%s): The '%s' internal pin does not drive any\n \toutput or is unneeded. The pin is ignored.

Description

This message indicates that the specified internal pin does not directly or indirectly drive any output port, or that the pin can be deleted without affecting the functionality of the cell. An internal pin that is never visible is functionally useless. Every internal pin must have a unique functional relationship with an output port. The specified internal pin is ignored.

What Next

Either delete the internal pin or give it a unique functional relationship with an output port.

Examples

```
cell(libg54) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.9;
              intrinsic_fall : 0.9;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.4;
              intrinsic_fall : 0.4;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          statetable ( "D CP", "Q QB") {
            table : "L/H R  : - - : L/H H/L,\\\n
                     -   ~R : - - : N   N";
```

Feedback

```
    }

    pin(n1) {
      direction : internal;
      internal_node : "Q";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.34;
        intrinsic_fall : 1.54;
        rise_resistance : 0.0718;
        fall_resistance : 0.0347;
        related_pin : "CP";
      }
    }
    pin(Q) {
      direction : output;
      internal_node : "Q";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.34;
        intrinsic_fall : 1.54;
        rise_resistance : 0.0718;
        fall_resistance : 0.0347;
        related_pin : "CP";
      }
    }
    pin(QB) {
      direction : output;
      internal_node : "QB";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.34;
        intrinsic_fall : 1.54;
        rise_resistance : 0.0718;
        fall_resistance : 0.0347;
        related_pin : "CP";
      }
    }
  }
```

In this case, n1 is not functionally used.

Examples

```
Information: Line 139, Cell(libg54): The 'n1' internal pin does not drive
 any
        output or is unneeded. The pin is ignored. (LIBG-54)
```

LIBG-55

(error) Cell(%s): The 'input_map' in the '%s' port is not\n \tallowed with the 'state_function'. Deleting the table.

Feedback

Description

This message indicates that the specified port has both a *state_function* attribute and an *input_map* attribute. A port with a *state_function* attribute cannot have an *input_map* attribute. The *input_map* attribute can occur only with the *internal_node* attribute. Therefore, the table is deleted. However, the following combinations of attributes can be specified on the same port:

```
* state_function and three_state attributes
        * internal_node and input_map attributes
        * internal_node and three_state attributes
```

What Next

Either replace the *state_function* attribute with an *internal_node* attribute, or delete the *input_map* attribute.

Examples

```
pin(Q) {
    direction : output;
    state_function : "Q";
    input_map : "D CP";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
```

You cannot have both state_function and input_map attributes in the same pin group.

Examples

```
Error: Line 139, Cell(libg55): The 'input_map' in the 'Q' port is not
        allowed with the 'state_function'. Deleting the table. (LIBG-55)
```

LIBG-56

(error) Cell(%s): The '%s' node must be specified in\n \tthe 'input_map' of the '%s' port. Deleting the table.

Description

This message indicates that a node was specified as a don't care "-" in the 'input_map' of the port, but the node is necessary for the port. Every functionally related input node and current internal node must be specified. Therefore, the table is deleted.

Feedback

What Next

Investigate why the assumption that the node is functionally unrelated to the port is incorrect. Possible reasons might be that the wrong internal code is chosen, the state table is incorrectly specified, or the 'input_map' is incorrect.

Examples

```
statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "D -";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
```

The use of a dont'care, "-", in the input_map means that the inputs 'CP' and 'CP*' are not used for the outport port 'Q'. However, given the state table, the nodes 'CP' and 'CP*' (delayed) are necessary for 'Q' and must be specified in the input_map string.

Examples

```
Error: Line 139, Cell(libg56): The 'CP' node must be specified in
        the 'input_map' of the 'Q' port. Deleting the table. (LIBG-56)
```

LIBG-57

(error) Cell(%s): Duplicate '%s' names in the 'input_map' of the '%s' port.

Description

Two or more nodes have been mapped to the same name either implicitly or explicitly in the 'input_map' attribute of the port. Every node used in the table must be mapped to a unique port. Unspecified node names in the 'input_map' are implicitly mapped to the node names specified in the state table. Therefore, the table is deleted.

What Next

Change the 'input_map' attribute to eliminate duplicate names.

Feedback

Examples

```
statetable ( "D CP", "Q") {
    table : "L/H R  : - - : L/H,\\\n
             -   ~R : - - : N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "D D";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
```

In the previous case, the port name 'D' is explicitly duplicated for nodes D and CP.

```
statetable ( "D CP", "Q") {
    table : "L/H R  : - - : L/H,\\\n
             -   ~R : - - : N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "CP";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
```

In the previous case, the port name 'CP' is implicitly duplicated for nodes 'D' (explicitly specified in the input_map string) and 'CP' (implicitly mapped to the node name specified in the state table).

Examples

```
Error: Line 139, Cell(libg57): Duplicate 'D' names in the 'input_map' of
 the 'Q' port. (LIBG-57)
```

Feedback

LIBG-58

(error) Cell(%s): For the '%s' port, the '%s' node is mapped to\n \t'%s', which is not a port.

Description

After the state table node names have been explicitly and implicitly mapped to names, one of the mapped node names is not the name of a port. Every mapped node name must be the name of a port. Unspecified node names in the 'input_map' are implicitly mapped to the node names specified in the state table. Therefore, the table is deleted.

The state table is in a completely independent, isolated name space. The term "node" refers to the identifiers. The "input nodes" and the "internal nodes" can have any name made up of any character except white space and comments.

The node names are resolved to the real port names by each port with an internal_node attribute. This mapping occurs by a combination of the 'input_map' attribute and the 'internal_node' attribute. If a node name is not mapped explicitly to a real port name in the 'input_map', it automatically inherits the node name as the real port name. The internal node name specified by the 'internal_node' attribute maps implicitly to the output being defined.

After all node names have been mapped to real port names, the real port names are checked to verify that they exist and are of the right direction. That is why the error message occurs at the output port. This is when elaboration occurs.

What Next

Change the *input_map* attribute.

Examples

```
statetable ( "D CP", "Q") {
    table : "L/H R  : - - : L/H,\\\n
              -   ~R : - - : N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "data CP";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
```

Feedback

In this case, the port 'data' does not exist in the cell.

Examples

```
Error: Line 139, Cell(libg58): For the 'Q' port, the 'D' node is mapped
 to
        'data', which is not a port. (LIBG-58)
```

LIBG-59

(error) Cell(%s): The 'input_map' of the '%s' port maps\n \tthe '%s' input port to the '%s' internal node.

Description

The mapped internal node name refers to an input port. An internal node must be mapped to either an output, an internal pin, or an inout port but not to an input port. An input port cannot be driven. Therefore, the table is deleted.

What Next

Change the 'input_map' attribute.

Examples

```
pin(CP EN) {
    direction : input;
    capacitance : 1;
  }

  statetable ( "D CP", "Q QB") {
    table : "L/H R  : L - : L/H H/L,\\\n
             L/H R  : H - : L H,\\\n
             -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    internal_node : "Q";
    input_map : "D CP EN";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.34;
      intrinsic_fall : 1.54;
      rise_resistance : 0.0718;
      fall_resistance : 0.0347;
      related_pin : "CP";
    }
  }
```

In this case, The internal node 'Q' is mapped to an input port 'EN'. Remove 'EN' from the input_map, or change its direction.

Feedback

Examples

```
Error: Line 140, Cell(libg59): The 'input_map' of the 'Q' port maps
        the 'EN' input port to the 'Q' internal node. (LIBG-59)
```

LIBG-60

(warning) Cell(%s): translates into a combinational cell.\n \tThe State table information is not created.

Description

This message indicates that the library cell has a sequential description that actually represents a combinational function. The state table information is allowed only for describing sequential functions. This situation occurs only when reading in an old technology library DB file. Issuing this warning is controlled by the *dc_shell* or the *lc_shell* environment variable *read_db_lib_warnings*.

What Next

Update the original technology library source file and recompile.

Examples

```
Warning: Cell(libg60): translates into a combinational cell.
        The state table information is not created. (LIBG-60)
```

LIBG-61

(error) Cell(%s): Verification failure on the '%s' port. Deleting the table.

Description

When a cell has both a state table and the v3.1 format, the Library Compiler automatically converts the v3.1 format to UNIGEN. The UNIGEN generated from the v3.1 format is formally compared against the UNIGEN generated from the state table. They must match.

This message indicates that the state table description for the port does not match its sequential description. If both a state table description and a sequential description (ff, latch, ff_bank, or latch_bank) are specified for the library cell, they must match each other exactly. A listing of the differences is printed out. The maximum number of differences to be listed is controlled by the *dc_shell* environment variable *libgen_max_difference*.

What Next

Fix or delete the state table, or fix or delete the sequential description.

Feedback

Examples

```
cell(libg61) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          seq( IQ, IQN) {
            clocked_on : "CP";
            next_state : "D";
          }

          statetable ( "D CP", "Q QB") {
            table : "L/H F  : - - : L/H H/L,\\\n
                      -   ~F : - - : N   N";
          }

          pin(Q) {
            direction : output;
            function : "IQ";
            internal_node : "Q";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }
          pin(QB) {
            direction : output;
            function : "IQN";
            internal_node : "QB";
            timing() {
```

Feedback

```
            timing_type : rising_edge;
            intrinsic_rise : 1.0;
            intrinsic_fall : 1.0;
            rise_resistance : 0.1;
            fall_resistance : 0.1;
            related_pin : "CP";
          }
        }
      }
```

Examples

```
Error: Line 139, Cell(libg61): Verification failure on the 'Q' port.
 Deleting the table.  (LIBG-61)
  Both table inputs are: D*, CP*, CP
  List of differences between statetable vs. v3.1 table:
    001    N <=> L
    010    L <=> N
    101    N <=> H
    110    H <=> N
```

LIBG-62

(warning) Cell(%s): The '%s' input node is not required by any\n \tinternal node used. The input node is ignored.

Description

This message indicates that the specified input node is not functionally related to any internal node used. Therefore, the input node is unused. An input node must be related to at least one internal node. This warning is for informational purposes because of the possibility of a user error. This message is suppressed if the input node has always been specified with the don't care,"-", token.

What Next

Determine why the input node is unused, and correct the problem.

Examples

```
cell(libg62) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
```

Feedback

```
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.1;
      intrinsic_fall : 0.1;
      related_pin : "CP";
    }
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }

  ff( IQ, IQN) {
    clocked_on : "CP";
    next_state : "D";
  }

  statetable ( "D CP X", "Q QB") {
    table :  "L/H R  - : - - : L/H H/L,\\\n
              -   ~R L/H : - - : N   N";
  }

  pin(Q) {
    direction : output;
    function : "IQ";
    internal_node : "Q";
  timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
  pin(QB) {
    direction : output;
    function : "IQN";
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

Feedback

Examples

```
Warning: Line 134, Cell(libg62): The 'X' input node is not required by
 any
        internal node used. The input node is ignored. (LIBG-62)
```

LIBG-63

(error) Cell(%s): The '%s' internal node is combinational.

Description

In the table description of the internal node, there is no hold state "N". Every internal node should have a hold state "N". Otherwise, it is not a sequential node. Every internal node should be a single sequential storage element. Therefore, the table is deleted.

What Next

Add a hold state to the internal node or delete the internal node.

Examples

```
cell(libg63) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          statetable ( "D CP", "Q QB") {
            table : "L/H R  : - - : L/H H/L,\\\n
                      -   ~R : - - : L   N";
          }

          pin(Q) {
            direction : output;
```

Feedback

```
        internal_node : "Q";
        timing() {
          timing_type : rising_edge;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "CP";
        }
      }
      pin(QB) {
        direction : output;
        internal_node : "QB";
        timing() {
          timing_type : rising_edge;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "CP";
        }
      }
    }
```

In this case, the node 'QB' has a "N" state in the table but, the node 'Q' does not have an "N" state. All internal nodes in the table require at least one "N" state and at least one "non-N", or "non-X" state.

Examples

```
Error: Line 134, Cell(libg63): The 'Q' internal node is combinational.
 (LIBG-63)
```

LIBG-64

(error) Cell(%s): The '%s' port cannot have both 'internal_node'\n \tand 'state_function' attributes.

Description

The port has both an 'internal_node' attribute and a 'state_function' attribute. Ports can only have either an 'internal_node' attribute, which is a name of an internal node, or a 'state_function' attribute, which is the output logic. Therefore, the table is deleted.

A port can have the following combination of attributes:

```
* state_function and three_state attributes
        * internal_node and input_map attributes
        * internal_node and three_state attributes
```

Feedback

What Next

Remove either the 'internal_node' attribute or the 'state_function' attribute.

Examples

```
cell(libg64) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          statetable ( "D CP", "Q QB") {
            table : "L/H R  : - - : L/H H/L,\\\n
                      -   ~R : - - : N   N";
          }

          pin(Q) {
            direction : output;
            internal_node : "Q";
            state_function : "Q";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }
          pin(QB) {
            direction : output;
            internal_node : "QB";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
```

Feedback

```
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }
        }
```

Examples

```
Error: Line 139, Cell(libg64): The 'Q' port cannot have both
 'internal_node'
        and 'state_function' attributes. (LIBG-64)
```

LIBG-65

(error) Cell(%s): The '%s' internal pin cannot have a 'three_state' attribute.

Description

The internal pin has a 'three_state' attribute. Internal pins are not allowed to have a 'three_state' attribute. The attribute 'three_state' can only be specified on output or inout ports.

What Next

Either change the internal pin to a port or remove the 'three_state' attribute.

Examples

```
cell(libg65) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
            capacitance : 1;
          }
```

Feedback

```
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
}

pin(Q) {
    direction : internal;
    internal_node : "Q";
    three_state : "D";  /* not allowed for internal pin */
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }

  pin(QB) {
  direction : output;
    internal_node : "QB";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
  }
}
```

Examples

```
Error: Line 139, Cell(libg65): The 'Q' internal pin cannot have a
 'three_state' attribute. (LIBG-65)
```

LIBG-67

(warning) Cell(%s): The '%s' port has both the internal_node\n \tand the input_map specified. However, there is a mismatch in the mapping.\n \tThe '%s' port is mapped by the input_map instead of the '%s' port, \n \tthe name of the internal_node. The '%s' port, specified in the input_map, is used.

Description

The port mapped by 'input_map' to the internal node specified in internal_node is not equal to the name of the port being defined. The current state of an output port should be

Feedback

equal to the state of the output port, not another port. This condition should almost never be violated, but the user is given the freedom to do so with a warning.

What Next

Change the input_map attribute to map the current state to the port being defined.

Examples

```
cell(libg67) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          statetable ( "D CP", "Q QB") {
            table : "L/H R  : L - : L/H H/L,\\\n
                   L/H R  : H - : L H,\\\n
                     -   ~R : - - : N   N";
          }

          pin(Q) {
            direction : output;
            internal_node : "Q";
            input_map : "D CP QB";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }
          pin(QB) {
            direction : output;
```

Feedback

```
            internal_node : "QB";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }
        }
```

Examples

```
Warning: Line 140, Cell(libg67): The 'Q' port has both the internal_node
        and the input_map specified. However, there is a mismatch in the
 mapping.
        The 'QB' port is mapped by the input_map instead of the 'Q' port,
        the name of internal_node. The 'QB' port, specified in the
 input_map, is used. (LIBG-67)
```

LIBG-68

(error) Cell(%s): Mismatch in internal pins between\n \tthe v3.1 format and the state table. Deleting the table.

Description

UNIGEN generated from the v3.1 format is formally compared against UNIGEN generated from the state table. They must match.

This message indicates that the v3.1 format has an implied internal pin that cannot be mapped to an internal pin in the state table. There must be a one-to-one match between the internal pins of the state table and the v3.1 format.

What Next

Determine whether the state table is specified incorrectly or is missing an internal pin. Correct the problem.

Examples

```
cell(libg68) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
```

Feedback

```
      }
      timing() {
        timing_type : hold_rising;
        intrinsic_rise : 0.1;
        intrinsic_fall : 0.1;
        related_pin : "CP";
      }
    }
    pin(CP CP_ALSO) {
      direction : input;
      capacitance : 1;
    }

    ff( IQ, IQN) {
      clocked_on : "CP";
      clocked_on_also : "CP_ALSO";
      next_state : "D";
    }

    statetable ( "D CP", "Q QB") {
      table : "L/H R  : - -  : L/H H/L,\\\n
               -   ~R : - - : N   N";
    }

    pin(QB) {
      direction : output;
      function : "IQN";
      internal_node : "QB";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CP";
      }
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CP_ALSO";
      }
    }
  }
```

Examples

```
Error: Line 140, Cell(libg68): Mismatch in internal pins between
        the v3.1 format and the state table. Deleting the table.
 (LIBG-68)
```

Feedback

LIBG-69

(warning) Cell(%s): The '%s' input is specified as\n \tdelayed in the state table. It will be used.

Description

Delayed input nodes are specified in the state table description, and can be specified with the asterisk (*) suffix. Only advanced users should consider specifying delayed inputs because there is a potential for error and confusion.

What Next

Try to specify the state table without referring to delayed inputs.

Examples

```
cell(libg69) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
          capacitance : 1;
          }

          statetable ( "D CP* CP", "Q QB") {
            table : "L/H L  H  : - - : L/H H/L,\\\n
                     -   H  - : - - : N   N,\\\n
                     -   L  L : - - : N   N";
          }

          pin(Q) {
            direction : output;
            internal_node : "Q";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
```

Feedback

```
            intrinsic_fall : 1.0;
            rise_resistance : 0.1;
          fall_resistance : 0.1;
            related_pin : "CP";
          }
        }

        pin(QB) {
          direction : output;
          internal_node : "QB";
          timing() {
            timing_type : rising_edge;
            intrinsic_rise : 1.0;
            intrinsic_fall : 1.0;
            rise_resistance : 0.1;
            fall_resistance : 0.1;
            related_pin : "CP";
          }
        }
      }
```

Examples

```
Warning: Line 134, Cell(libg69): The 'CP' input is specified as
        delayed in the state table. It will be used. (LIBG-69)
```

LIBG-70

(warning) Cell(%s): Delayed inputs are specified in\n \tthe input_map of the '%s' port. They will be used.

Description

Delayed input ports are specified in the input_map attribute, and are specified after the undelayed inputs and the internal nodes. Only advanced users should consider specifying delayed inputs because there is a potential for error and confusion.

What Next

Try to specify the 'input_map' without mapping to delayed inputs.

Examples

```
cell(libg70) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
```

Feedback

```
        related_pin : "CP";
      }
      timing() {
        timing_type : hold_rising;
        intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
        related_pin : "CP";
      }
    }
    pin(CP) {
      direction : input;
      capacitance : 1;
    }

    statetable ( "D CP", "Q QB") {
      table : "L/H R  : - - : L/H H/L,\\\n
               -   ~R : - - : N   N";
    }

  pin(Q) {
      direction : output;
      inverted_output : FALSE;
      internal_node : "Q";
      input_map : "D CP Q - CP";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CP";
      }
    }

    pin(QB) {
      direction : output;
      internal_node : "QB";
      inverted_output : TRUE;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "CP";
      }
    }
  }
```

Examples

```
Warning: Line 139, Cell(libg70): Delayed inputs are specified in
        the input_map of the 'Q' port. They will be used. (LIBG-70)
```

Feedback

LIBG-71

(error) Cell(%s): The '%s' port was expected to be %s with\n \trespect to the '%s' port.

Description

The two ports are not the function of each other as expected. The expected behavior is derived from the v3.1 format, and the state table is expected to match. Therefore, the table is deleted.

What Next

Correct the state table or the v3.1 format.

Examples

```
cell(libg71) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }

          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          ff( IQ, IQN) {
            clocked_on : "CP";
            next_state : "D";
          }

          statetable ( "D CP", "Q QB") {
            table : "L/H R  : - -  : L/H H/L,\\\n
                      -   ~R : - -  : N   N";
          }

          pin(Q) {
            direction : output;
```

Feedback

```
            function : "IQ";
            internal_node : "Q";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }

          pin(QB) {
            direction : output;
            function : "IQ";            /* Wrong! function should be IQN
 */
            internal_node : "QB";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }
        }
```

In this case, the function descriptions for the two ports are inconsistent. From the v3.1 table, the two ports have the same function (notice the typo in the function of the pin 'QB', instead of 'IQN', the function string is 'IQ'). From the UNIGEN table they are inverted.

Examples

```
Error: Line 139, Cell(libg71): The 'Q' port was expected to be uninverted
 with
        respect to the 'QB' port. (LIBG-71)
```

LIBG-72

(error) Cell(%s): Cannot find an implicit internal pin in\n \tthe v3.1 format to match the '%s' internal pin.

Description

The internal pin does not have a corresponding internal pin in the v3.1 format. The internal pins of both the v3.1 format and the state table format must match. Therefore, the table is deleted.

Feedback

What Next

Correct the state table or the v3.1 format.

Examples

```
cell(libg72) {
          area : 10;
          pin(force11) {
            direction : input;
            capacitance : 1;
          }
          pin(force10) {
            direction : input;
            capacitance : 1;
          }
          pin(force01) {
            direction : input;
            capacitance : 1;
          }
          pin(force00) {
            direction : input;
            capacitance : 2;
          }
          pin(ck ck_also) {
            direction : input;
            capacitance : 2;
          }
          pin(next) {
            direction : input;
            capacitance : 2;
        }

          state("IQ","IQN") {
            next_state : "next";
            clocked_on : "ck";
            clocked_on_also : "ck_also";
            force_00   : "force00";
            force_01   : "force01";
            force_10   : "force10";
            force_11   : "force11";
          }

          statetable ("next ck force00 force01 force10 force11",\\\n
                      "int_net") {\n
             table : "-   -   H   L   L   L   : -   : L,\\\n
                      -   -   L   H   L   L   : -   : L,\\\n
                      -   -   L   L   H   L   : -   : H,\\\n
                      -   -   L   L   L   H   : -   : H,\\\n
                      -   ~R  L   L   L   L   : -   : N,\\\n
                      L/H R   L   L   L   L   : -   : L/H";
          }
```

Feedback

```
          pin(int_net) {
            direction : internal;
            internal_node : "int_net";
            input_map : "next ck_also force00 force01 force10 force11
int_net";
        }

          pin(Q) {
            direction : output;
            function : "IQ";
            internal_node : "int_net";
            input_map : "int_net ck_also force00 force01 force10 force11
Q";
          }
        }
```

Examples

```
Error: Line 165, Cell(libg72): Cannot find an implicit internal pin in
        the v3.1 format to match the 'int_net' internal pin. (LIBG-72)
```

LIBG-73

(warning) Cell(%s): Table inputs for the '%s' port exceed 16 inputs.

Description

The state table is stored with over 16 table inputs. There is an exponential cost in performance and memory as the number of table inputs increases. This warning tells the user about the excessive size of table inputs. To list the table, use the report_lib command with the *full_table* option.

What Next

If possible, take advantage of the input_map attribute to reduce the size of the table.

Examples

```
cell(libg73) {
          area : 10;
          pin(i0 i1 i2 i3 i4 i5 i6 i7 i8 j0 j1 j2 j3 j4 j5) {
            direction : input;
            capacitance : 1;
          }
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.9;
              intrinsic_fall : 0.9;
              related_pin : "CP";
```

Feedback

```
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.4;
              intrinsic_fall : 0.4;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          statetable ( "D i0 i1 i2 i3 i4 i5 i6 i7 i8 j0 j1 j2 j3 j4 j5
 CP", "Q ") {
            table : "H H H H H H H H H H H H H H H R   : - : H,\\\n
                     - - - - - - - - - - - - - - - - R   : - : L,\\\n
                     - - - - - - - - - - - - - - - - ~R  : - : N";
          }

          pin(Q) {
            direction : output;
            internal_node : "Q";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.34;
              intrinsic_fall : 1.54;
              rise_resistance : 0.0718;
              fall_resistance : 0.0347;
              related_pin : "CP";
            }
          }
        }
```

Examples

```
Warning: Line 149, Cell(libg73): Table inputs for the 'Q' port exceed 16
 inputs.
(LIBG-73)
```

LIBG-74

(error) Cell(%s): No internal_node output pin is found.

Description

A state table is defined for the library cell, but none of the output pins are defined as sequential. There must be at least one output with an internal_node attribute specified.

What Next

Remove the state table description or add an internal_node attribute to at least one output.

Feedback

Examples

```
cell(libg74) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
            related_pin : "CP";
            }
          }

          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          statetable ( "D CP ", "Q QB") {
            table : "L/H R  : - - : L/H H/L,\\\n
                      -   ~R : - - : N   N";
          }

          pin(Q) {
            direction : output;
            state_function : "D";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }

          pin(QB) {
            direction : output;
            state_function : "D";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
            intrinsic_fall : 1.0;
            rise_resistance : 0.1;
              fall_resistance : 0.1;
```

Feedback

```
            related_pin : "CP";
          }
        }
      }
```

In this case, both output pins 'Q' and 'QB' have state_function and no internal_node attribute.

Examples

```
Error: Line 137, Cell(libg74): no internal_node output pin is found.
 (LIBG-74)
```

LIBG-75

(error) Cell(%s): The state_function on the '%s' port has\n \tan invalid port in the expression.

Description

A valid port in a state_function expression is either an input port, an inout port with a three_state attribute, or an output port with the internal_node attribute. This error is issued if a port in the state_function is either an output port without an internal_node attribute or an inout port without a three_state attribute. Neither of these two kinds of ports is allowed in the state_function expression.

What Next

Change the state_function expression, or change the invalid port.

Examples

```
cell(libg75) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }
```

Feedback

```
            pin(CP) {
              direction : input;
              capacitance : 1;
            }

            statetable ( "D CP ", "Q QB") {
              table : "L/H R  : - - : L/H H/L,\\\n
                       -   ~R : - - : N   N";
            }

            pin(Q) {
              direction : output;
              internal_node : "Q";
              timing() {
                timing_type : rising_edge;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                rise_resistance : 0.1;
                fall_resistance : 0.1;
                related_pin : "CP";
              }
            }

            pin(QB) {
              direction : output;
              state_function : "Q";
              timing() {
                timing_type : rising_edge;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                rise_resistance : 0.1;
                fall_resistance : 0.1;
                related_pin : "CP";
              }
            }

            pin(QC) {
              direction : output;
              state_function : "QB"; /* 'QB' is an output without
internal_node*/
              timing() {
                timing_type : rising_edge;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                rise_resistance : 0.1;
                fall_resistance : 0.1;
                related_pin : "CP";
            }
            }
          }
```

Feedback

Examples

```
Error: Line 167, Cell(libg75): The state_function on the 'QC' port has
        an invalid port in the expression. (LIBG-75)
```

LIBG-76

(warning) The '%s' test cell pin on the '%s' cell\n \thas a timing arc. The timing arc is ignored.

Description

The test cell pin has a timing arc, but timing arcs are only valid on the library cell.

What Next

Move all timing arcs in the test cell to the top-level library cell.

Examples

```
cell(libg76) {
            area : 11;
            pin(D0) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_rising;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "CK1";
              }
              timing() {
                timing_type : hold_rising;
                intrinsic_rise : 0.1;
                intrinsic_fall : 0.1;
                related_pin : "CK1";
              }
            }
            pin(TI) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_rising;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "CK1";
              }
              timing() {
                timing_type : hold_rising;
                intrinsic_rise : 0.1;
                intrinsic_fall : 0.1;
                related_pin : "CK1";
```

Feedback

```
  }
}
pin(TE) {
  direction : input;
  capacitance : 1;
  prefer_tied : "0";
  timing() {
    timing_type : setup_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 0.1;
    intrinsic_fall : 0.1;
    related_pin : "CK1";
  }
}
pin(CK1) {
  direction : input;
  capacitance : 1;
}
pin(CK2) {
  direction : input;
  capacitance : 1;
}
statetable("D0 TE TI CK1 CK2", "n1 Q") {
  table : "-   -  -  -  L  : L/H - : - L/H,\\\n
           L/H L  -  L  -  : -   - : L/H -,\\\n
           -   H L/H L  -  : - - : L/H -,\\\n
           -   -  -  -  -  : - -  : N N";
}

pin(n1) {
  direction : internal;
  internal_node : "n1";
}

pin(Q) {
  direction : output;
  internal_node : "Q";
  timing() {
    timing_type : falling_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "CK2";
  }
}
pin(QN) {
  direction : output;
```

Feedback

```
                state_function : "Q'";
                timing() {
                  timing_type : falling_edge;
                  intrinsic_rise : 1.0;
                  intrinsic_fall : 1.0;
                  rise_resistance : 0.1;
                  fall_resistance : 0.1;
                  related_pin : "CK2";
                }
              }
              test_cell() {
                pin(D0) {
                  direction : input;
                }
                pin(TI) {
                  direction : input;
                  signal_type : "test_scan_in";
                  timing() {                        /* move  it to the cell
level*/
                    timing_type : setup_rising;
                    intrinsic_rise : 1.0;
                    intrinsic_fall : 1.0;
                    related_pin : "CK1";
                  }
                }
                pin(TE) {
                  direction : input;
                  signal_type : "test_scan_enable";
                }
                pin(CK1) {
                  direction : input;
                  capacitance : 1;
                }
                pin(CK2) {
                  direction : input;
                  capacitance : 1;
                }
                statetable("D0 CK1", "Q") {
                  table : "-   H : - : N,\\\n
                           L/H L  : - : L/H";
                }

                pin(n1) {
                  direction : internal;
                  internal_node : "Q";
                }
                pin(Q) {
                  direction : output;
                  internal_node : "Q";
                  input_map : "n1 CK2";
                  signal_type : "test_scan_out";
                }
                pin(QN) {
```

Feedback

```
            direction : output;
            state_function : "Q'";
            signal_type : "test_scan_out_inverted";
          }
        }
      }
```

Examples

```
Warning: Line 209, The 'TI' test cell pin on the 'libg76' cell
        has a timing arc. The timing arc is ignored. (LIBG-76)
```

LIBG-77

(error) The '%s' test cell pin on the '%s' cell\n \thas a conflicting pin type.

Description

This message indicates that the test cell has one of these invalid combinations:

```
Two pins, of which one has the signal_type attribute
           "test_scan_in" and the other has "test_scan_in_inverted";

        or  Two pins, of which one has the signal_type attribute
           "test_scan_enable" and the other has
 "test_scan_enable_inverted".
```

A test cell cannot have two pins whose *signal_type* attributes are the inversions of each other.

What Next

Change one of the *signal_type* attributes so that the test cell has only one of the pins in the above invalid combinations.

LIBG-78

(warning) The '%s' test cell pin on the '%s' cell\n \thas a conflicting pin type. Removing the test cell.

Description

This message indicates that the test cell has one of these invalid combinations:

```
Two pins, of which one has the signal_type attribute
           "test_scan_in" and the other has "test_scan_in_inverted";

        or  Two pins, of which one has the signal_type attribute
           "test_scan_enable" and the other has
 "test_scan_enable_inverted".
```

A test cell cannot have two pins whose *signal_type* attributes are the inversions of each other. The test cell has been removed; DFT Compiler will not use it.

What Next

Change one of the *signal_type* attributes so that the test cell has only one of the pins in the above invalid combinations. Then re-execute.

LIBG-79

(error) The '%s' test cell pin on the '%s' cell\n \thas a conflict between the function and the test type.

Description

The test cell pin either has a signal_type attribute of "test_scan_out" and a function of the inverted output (i.e. second variable) or the pin has a signal_type attribute of "test_scan_out_inverted" and a function of the non-inverted output (i.e. first variable).

If a pin has both a signal_type attribute and a function attribute, the two attributes must be consistent. A "test_scan_out" corresponds to the non-inverted output function and a "test_scan_out_inverted" corresponds to the inverted output.

What Next

Change either the signal_type attribute or the function.

LIBG-80

(warning) The '%s' test cell pin on the '%s' cell has a\n \tconflict between the function and the test type. The test cell is removed.

Description

The test cell pin either has a signal_type attribute of "test_scan_out" and a function of the inverted output (i.e. second variable) or the pin has a signal_type attribute of "test_scan_out_inverted" and a function of the non-inverted output (i.e. first variable).

If a pin has both a signal_type attribute and a function attribute, the two attributes must be consistent. A "test_scan_out" corresponds to the non-inverted output function and a "test_scan_out_inverted" corresponds to the inverted output.

The test cell is removed and DFT Compiler will not use it.

What Next

Change either the signal_type attribute or the function.

Feedback

LIBG-81

(error) Cell(%s): translates into a combinational cell.

Description

The library cell has a sequential description, which represents a combinational function. The state table information is only allowed on sequential library cells.

What Next

Change the sequential description.

Examples

```
cell(libg81) {
      area : 4;
      pin(Q) {
        max_fanout : 1.0;
        direction : output;
        function : "IQ";
        timing() {
          timing_type : rising_edge;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "CK";
        }
        timing() {
          timing_type : preset;
          timing_sense : "negative_unate";
          intrinsic_rise : 1.0;
          rise_resistance : 0.1;
          related_pin : "SETZ"
        }
      }
      pin(QZ) {
        direction : output;
        function : "IQZ";
        timing() {
          timing_type : rising_edge;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "CK";
        }
        timing() {
          timing_type : clear;
          timing_sense : "positive_unate";
          intrinsic_fall : 1.0;
```

Feedback

```
      fall_resistance : 1.0;
      related_pin : "SETZ";
    }
  }
  pin(CK) {
    direction : input;
    clock : true;
    min_period : 1.0;
    capacitance : 0.1;
  }
  pin(S) {
    direction : input;
    capacitance : 1.0;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK";
    }
  }
  pin_opposite("Q","QZ");
  state("IQ","IQZ") {
    next_state : "(S' A) + (S B)";
    clocked_on : "CK";
    force_01   : "SETZ";
    force_10   : "SETZ'";
  }
  pin(A) {
    direction : input;
    capacitance : 1.0;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK";
    }
  }
  pin(B) {
    direction : input;
    capacitance : 0.1;
    timing() {
```

```
          timing_type : setup_rising;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          related_pin : "CK";
        }
        timing() {
          timing_type : hold_rising;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          related_pin : "CK";
        }
      }
      pin(SETZ) {
        direction : input;
        capacitance : 0.1;
      }
    }
```

Examples

```
Error: Line 109, Cell(libg81): translates into a combinational cell.
 (LIBG-81)
```

LIBG-82

(error) The test cell on the '%s' cell is not DFT Compiler supported.

Description

This message indicates that the description of the specified test cell is not supported by DFT Compiler. DFT Compiler has restrictions on the non-test mode and test inputs; the test cell violates one or more of these restrictions. For details on these restrictions, refer to the *DFT Compiler Test Design Rule Checking User Guide*.

What Next

Revise the test cell description so that it conforms to DFT Compiler restrictions; or, remove the test cell.

LIBG-83

(warning) The test cell on the '%s' cell is not DFT Compiler supported.\n \tRemoving the test cell.

Description

The test cell has a description that is not supported by DFT Compiler. DFT Compiler has restrictions on the non-test mode and test inputs; the test cell violates one or more of

these restrictions. For details on these restrictions, refer to the *DFT Compiler Test Design Rule Checking User Guide*.

The test cell has been removed; DFT Compiler will not use this cell during scan insertion.

What Next

Obtain the technology library source and revise the test cell description so that it conforms to DFT Compiler restrictions; or, remove the test cell.

LIBG-84

(warning) The '%s' port in the '%s' cell does not\n \thave a function in the test cell descriptions. The cell is a black box.

Description

No function for that port can be derived from the test cells. The port function must be either explicitly specified or inferable from the test cell descriptions. The cell is a black box.

This warning is issued when reading a .db library and can be switched off by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-85.

What Next

Change the technology library source by explicitly or implicitly providing the function for that port.

LIBG-85

(error) The '%s' port in the '%s' cell does not\n \thave a function in the test cell descriptions.

Description

No function for that port can be derived from the test cells. The port function must be either explicitly specified or inferable from the test cell descriptions. Some functional information is described but not all. Either the cell is completely specified, or it is completely unspecified.

What Next

Change the technology library source by either describing the port function explicitly or implicitly in the test cell descriptions or removing all functional descriptions.

Feedback

Examples

```
cell(libg85) {
            area : 11;
            pin(D0) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_rising;
                intrinsic_rise : 1.3;
                intrinsic_fall : 1.3;
                related_pin : "CK1";
              }
              timing() {
                timing_type : hold_rising;
                intrinsic_rise : 0.3;
                intrinsic_fall : 0.3;
                related_pin : "CK1";
              }
            }
            pin(TI) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_rising;
                intrinsic_rise : 1.3;
                intrinsic_fall : 1.3;
                related_pin : "CK1";
              }
              timing() {
                timing_type : hold_rising;
                intrinsic_rise : 0.3;
                intrinsic_fall : 0.3;
                related_pin : "CK1";
              }
            }

            pin(TE) {
              direction : input;
              capacitance : 1;
              prefer_tied : "0";
              timing() {
                timing_type : setup_rising;
                intrinsic_rise : 1.3;
                intrinsic_fall : 1.3;
                related_pin : "CK1";
              }
              timing() {
                timing_type : hold_rising;
                intrinsic_rise : 0.3;
                intrinsic_fall : 0.3;
                related_pin : "CK1";
              }
```

Feedback

```
}
pin(CK1) {
  direction : input;
  capacitance : 1;
}

pin(Q) {
  direction : output;
  inverted_output : FALSE;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.09;
    intrinsic_fall : 1.37;
    rise_resistance : 0.1458;
    fall_resistance : 0.0523;
    related_pin : "CK1";
  }
}

pin(QN) {
  direction : output;
  inverted_output : TRUE;
timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.59;
    intrinsic_fall : 1.57;
    rise_resistance : 0.1458;
    fall_resistance : 0.0523;
    related_pin : "CK1";
  }
}

test_cell() {
  pin(D0) {
  direction : input;
  }
  pin(TE) {
    direction : input;
    signal_type : "test_scan_enable";
  }
  pin(TI) {
    direction : input;
    signal_type : "test_scan_in";
  }
  pin(CK1) {
    direction : input;
    capacitance : 1;
  }

  statetable("D0 CK1", "Q") {
    table : "L/H F : - : L/H,\
             -  ~F : - : N";
  }
```

```
            pin(Q) {
              direction : output;
              internal_node : "Q";
              signal_type : "test_scan_out";
            }
            pin(QN) {
              direction : output;
              signal_type : "test_scan_out_inverted";
            }
          }
        }
```

Examples

```
Error: Line 177, The 'QN' port in the 'libg85' cell does not
        have a function in the test cell descriptions. (LIBG-85)
```

LIBG-86

(warning) The '%s' port in the '%s' cell has a timing\n \tarc related to '%s' that is inconsistent.

Description

The timing type of the timing arc from the specified port to the related port is inconsistent with respect to other timing in the cell. For example, a port cannot have both a *rising_edge* timing type and a *falling_edge* timing type.

This warning occurs only when reading in a technology library DB file. Issuing this warning is controlled by the *dc_shell* or the *lc_shell* environment variable *read_db_lib_warnings*.

The same problem in a .lib library causes an error. See the .lib example for LIBG-88.

What Next

Update the original technology library source. Make timing arcs consistent.

Examples

```
Warning: The 'Q' in the 'libg86' cell has a timing
        arc related to 'D' that is inconsistent. (LIBG-86)
```

LIBG-87

(error) Cell(%s): the internal node has L/H or H/L but\n \tno input has L/H or H/L. Deleting the table.

Feedback

Description

In the *table* attribute of the *statetable* group, an internal node has either L/H or H/L specified but none of the input nodes have either L/H or H/L specified. If an internal node has either the L/H or H/L value, at least one input node must be L/H or H/L. Therefore, the table is deleted.

What Next

Change the *table* attribute to replace L/H or H/L for the internal node with either L, H, X, or N, or make one of the input nodes L/H or H/L.

Examples

```
cell(libg87) {
          area : 10;
          pin(D) {
            direction : input;
            capacitance : 1;
            timing() {
              timing_type : setup_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
            timing() {
              timing_type : hold_rising;
              intrinsic_rise : 0.1;
              intrinsic_fall : 0.1;
              related_pin : "CP";
            }
          }
          pin(CP) {
            direction : input;
            capacitance : 1;
          }

          statetable ( "D CP", "Q QB") {
            table :     "L R  : - - : L/H H/L,\\\n
                         - ~R : - - : N   N";
          }

          pin(Q) {
            direction : output;
            internal_node : "Q";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
```

Feedback

```
            }
          }

          pin(QB) {
            direction : output;
            internal_node : "QB";
            timing() {
              timing_type : rising_edge;
              intrinsic_rise : 1.0;
              intrinsic_fall : 1.0;
              rise_resistance : 0.1;
              fall_resistance : 0.1;
              related_pin : "CP";
            }
          }
        }
```

Examples

```
Error: Line 132, Cell(libg87): the internal node has L/H or H/L but
        no input has L/H or H/L. Deleting the table. (LIBG-87)
```

LIBG-88

(error) The '%s' port in the '%s' cell has a timing\n \tarc related to '%s' that is inconsistent.

Description

The timing type of the timing arc from the specified port to the related port is inconsistent with respect to other timing in the cell. For example, a port cannot have both a *rising_edge* timing type and a *falling_edge* timing type.

What Next

Update the technology library source to make the timing arcs consistent.

Examples

```
cell(libg88) {
            area : 13;
            pin(D) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_rising;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "C";
              }
              timing() {
                timing_type : hold_rising;
                intrinsic_rise : 0.1;
```

Feedback

```
    intrinsic_fall : 0.1;
  related_pin : "C";
  }
}
pin(C) {
  direction : input;
  capacitance : 2;
}
pin(D2) {
  direction : input;
  capacitance : 1;
  timing() {
    timing_type : setup_rising;
  intrinsic_rise : 1.0;
  intrinsic_fall : 1.0;
    related_pin : "C2";
  }
  timing() {
    timing_type : hold_falling;     /* error */
    intrinsic_rise : 0.0;
    intrinsic_fall : 0.0;
  related_pin : "C2";
  }
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(Q) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 0.1;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C";
  }
  timing() {
  timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 0.1;
  rise_resistance : 0.1;
  fall_resistance : 0.1;
    related_pin : "C2";
  }
}
pin(QN) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 2.0;
```

Feedback

```
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C";
      }
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 2.0;
        rise_resistance : 0.1;
      fall_resistance : 0.1;
        related_pin : "C2";
      }
    }
    test_cell() {
      pin(D) {
      direction : input;
    }
      pin(C) {
        direction : input;
    }
      pin(D2) {
        direction : input;
      signal_type : "test_scan_in";
    }
    pin(C2) {
      direction : input;
        signal_type : "test_scan_clock";
      }
    state ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
    }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

Examples

```
Error: Line 89, The 'D2' port in the 'libg88' cell has a timing
        arc related to 'C2' that is inconsistent. (LIBG-88)
```

Feedback

LIBG-89

(warning) The '%s' port in the '%s' cell has an inconsistent\n \tfunction in the test cells.

Description

The test_cells define different functions for the port. The port must have one unique function among all of the test cells.

When reading a .db library, Library Compiler uses the first test_cell to create the full functional description. The second test_cell is ignored.

This warning can be switched off by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-90.

What Next

The default behavior of selecting the first test_cell as the correct one should be correct in most cases.

Change the technology library source to make the function of the port in all of the test cells consistent.

LIBG-90

(error) The '%s' port in the '%s' cell has an inconsistent\n \tfunction in the test cells.

Description

This message indicates that the test cells define different functions for the specified port. The port must have one unique function among all test cells.

What Next

Update the technology library source so that the function of the port in all test cells is consistent.

Examples

```
cell(libg90) {
            area : 21;
            pin(D1) {
              direction : input;
              capacitance : 1;
            }
            pin(C1) {
              direction : input;
              capacitance : 2;
            }
```

Feedback

```
pin(D2) {
  direction : input;
  capacitance : 1;
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(C3) {
  direction : input;
capacitance : 1;
}

pin(Q1) {
  direction : output;
  timing() {
  timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 0.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C1";
  }
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 0.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C2";
  }
}
pin(Q2) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C3";
  }
}
test_cell() {
  pin(D1) {
    direction : input;
  }
  pin(C1) {
    direction : input;
  }
  pin(D2) {
    direction : input;
    signal_type : "test_scan_in";
```

Feedback

```
    }
    pin(C2) {
      direction : input;
      signal_type : "test_scan_clock_a";
  }
    pin(C3) {
      direction : input;
      signal_type : "test_scan_clock_b";
    }
    state("IQ","IQN") {
      force_10 : "C1 D1";
      force_01 : "C1 D1'";
    }
    pin(Q1) {
      direction : output;
    function : "IQ";
    }
    pin(Q2) {
      direction : output;
      signal_type : "test_scan_out";
    }
  }
  test_cell() {
    pin(D1) {
      direction : input;
    }
    pin(C1) {
      direction : input;
  }
    pin(D2) {
      direction : input;
      signal_type : "test_scan_in";
    }
    pin(C2) {
      direction : input;
      signal_type : "test_scan_clock_a";
  }
    pin(C3) {
      direction : input;
    }
    seq("IQ","IQN") {
      data_in  : "D1";
      enable : "C1";
      enable_also : "C3'";
    }
    pin(Q1) {
      direction : output;
  }
    pin(Q2) {
      direction : output;
      function : "IQ";
      signal_type : "test_scan_out";
    }
```

```
            pin(Q2N) {
              direction : output;
            function : "IQN";
              signal_type : "test_scan_out_inverted";
            }
          }
        }
```

For the pin 'Q2', the 'function' attribute is missing in the first test_cell.

Examples

```
Error: Line 175, The 'Q2' port in the 'libg90' cell has an inconsistent
        function in the test cells. (LIBG-90)
```

LIBG-91

(error) The '%s' attribute is required when both 'clear'\n \tand 'preset' are present in the sequential model and the %s '%s'\n \tis used in the function attribute of the output pin(s) of the cell.

Description

When both 'clear' and 'preset' are present in the sequential model, the *clear_preset_var1* and/or *clear_preset_var2* attributes are required, depending on which variable of the sequential model is used in the function attribute of the output pin(s) of the cell. For example, if the first variable is used, *clear_preset_var1* is required.

What Next

Make the appropriate correction in your library, as indicated in the error message.
For more information on the *clear_preset_var* attributes, refer to the *Library Compiler Reference Manual*, Vol. 1.

LIBG-92

(warning) The '%s' port in the '%s' cell has a circular dependency.

Description

There is an undelayed feedback loop to the output, inout, and internal port. This circular dependency is not allowed.

This warning is issued if the current port appears in the list of expanded inputs of the port.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-93.

Feedback

What Next

Break the feedback loop by delaying one of the inputs in the feedback path.

LIBG-93

(error) The '%s' port in the '%s' cell has a circular dependency.

Description

There is an undelayed feedback loop to the output port. This circular dependency is not allowed.

This error is issued if the current port appears in the list of expanded inputs of the port.

What Next

Break the feedback loop by delaying one of the inputs in the feedback path.

Examples

```
cell(libg93) {
          area : 7;
          pin(D) {
            direction : input;
            capacitance : 1;
          }
          pin(R) {
            direction : input;
            capacitance : 1;
          }

          statetable("D R CP", "Q") {
            table : "H/L L  R : - : H/L,\\\n
                       -  L ~R : - :  N,\\\n
                       -  H -  : - :  H";
          }

          /* internal sequential state_function */
          pin(E) {
            direction : internal;
            state_function : "Q1+R";
          }

          /* slave with sequential reset */
          pin(Q1) {
            direction : internal;
            internal_node : "Q";
            input_map : "D Q2 CP";
          }

          /* master driving Q1 */
```

Feedback

```
            pin(Q2) {
              direction : output;
              internal_node : "Q"
              input_map : "D E CP";
            }

            pin(CP) {
              direction : input;
              capacitance : 1;
            }

          }
```

In this case, there is a feedback loop for 'Q1'. To break the dependency, delay one of the inputs in the feedback path. The pins 'E' and 'Q2' in the cell group can be changed as follows:

```
pin(E) {
              direction : internal;
              state_function : "D+Q1";
            }
            pin(Q2) {
              direction : output;
              internal_node : "Q"
              input_map : "E R CP";
            }
```

Examples

```
Error: Line 274, The 'Q1' port in the 'libg93' cell has a circular
 dependency. (LIBG-93)
```

LIBG-94

(warning) The '%s' cell needs a noninverted output.

Description

The test cell does not have any noninverted output. This particular type of test cell requires at least one noninverted output to be defined.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-95.

What Next

Specify the full function or define an output to be noninverted.

Feedback

LIBG-95

(error) The '%s' cell needs a noninverted output.

Description

The test cell has no noninverted output. This particular type of test cell requires at least one noninverted output to be defined.

What Next

Specify the full function or define an output to be noninverted.

Examples

```
cell(libg95) {
             area : 15;
             pin(D) {
               direction : input;
               capacitance : 1;
             }
             pin(C) {
               direction : input;
               capacitance : 2;
             }
             pin(TSI) {
               direction : input;
               capacitance : 1;
             }
             pin(TSE) {
               direction : input;
               capacitance : 2;
             }
             pin(QN) {
               direction : output;
               capacitance : 2;
             }
             pin(TSO TSOI) {
               direction : output;
             }
             test_cell() {
               pin(D) {
                 direction : input;
               }
               pin(C) {
                 direction : input;
               }
               pin(TSI) {
                 direction : input;
                 signal_type : "test_scan_in";
               }
               pin(TSE) {
```

Feedback

```
            direction : input;
            capacitance : 2;
            signal_type : "test_scan_enable";
          }
          statetable("D C", "QN") {
            table : "L/H H : - : H/L,\\\n
                     -   L : - : N";
          }

          pin(TSOI) {
            direction : output;
            signal_type : "test_scan_out_inverted";
          }
          pin(TSO) {
            direction : output;
            signal_type : "test_scan_out";
          }
          pin(QN) {
            direction : output;
            internal_node : "QN";
          }
        }
      }
```

In this case, the cell is a latch. To fix the problem, add another noninverted pin. For example, the following change to the cell will fix the problem.

```
cell(libg95) {
            ...
            pin(Q) {
              direction : output;
              capacitance : 2;
            }
            ...
            test_cell() {
                ...
              statetable("D C", "Q QN") {
                table : "L/H H : - - : L/H H/L,\\\n
                         -   L : - - : N N";
              }
                ...
              pin(Q) {
                direction : output;
                internal_node : "Q";
              }
            }
        }
```

Examples

```
Error: Line 142, The 'libg95' cell needs a noninverted output. (LIBG-95)
```

Feedback

LIBG-96

(warning) The '%s' port in the '%s' cell is used in both test and\n \tnon test mode.

Description

The input port has a test attribute and is also used in the non test mode. This is not allowed.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-97.

What Next

Specify the full function of the test cell.

LIBG-97

(error) The '%s' port in the '%s' cell is used in both\n \ttest and non test mode.

Description

The input port has a test attribute and is also used in the non test mode. This is not allowed.

What Next

Specify the full function of the test cell.

Examples

```
cell(libg97) {
             area : 13;
             pin(D TSI) {
               direction : input;
               capacitance : 1;
             }
             pin(C TSE) {
               direction : input;
               capacitance : 2;
             }
             pin(Q TSO) {
               direction : output;
             }
             test_cell() {
               pin(D C) {
                 direction : input;
               }
               pin(TSI) {
```

Feedback

```
            direction : input;
            signal_type : "test_scan_in";
          }
          pin(TSE) {
            direction : input;
            capacitance : 2;
            signal_type : "test_scan_enable";
          }
          statetable("C D TSI", "Q") {
            table : "H L/H H/L : - : L/H,\\\n
                     L -  -  : - : N";
          }
          pin(Q) {
            direction : output;
            internal_node : "Q";
          }
          pin(TSO) {
            direction : output;
            signal_type : "test_scan_out";
  }
     }
   }
```

In this case, the input port 'TSI' has the "test_scan_in" attribute, and it is used in the state table input entry.

Examples

```
Error: Line 141, The 'TSI' port in the 'libg97' cell is used in both
        test and non test mode. (LIBG-97)
```

LIBG-98

(warning) The '%s' test cell has an incompatible non test mode.

Description

The non test mode of the test cell is incompatible with the test attributes of the test cell.

This warning appears after any of the following warning messages: LIBG-128, LIBG-129, LIBG-130, and LIBG-131. For more information, refer to the man page of the issued warning.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-99.

What Next

Specify the full function of the test cell.

Feedback

LIBG-99

(error) The '%s' test cell has an incompatible non test mode.

Description

This message indicates that the non test mode of the test cell is incompatible with the test attributes of the test cell.

This error is displayed for a cell in UNIGEN format after any of the following error messages: LIBG-158, LIBG-159, LIBG-160, and LIBG-161. For more information, refer to the man page of the issued error.

What Next

Update the non test mode description or the test mode description to make them consistent.

Examples

```
cell(libg99) {
            area : 11;
            pin(D1 D2 D3) {
              direction : input;
              capacitance : 1;
            }
            pin(CP SCK1 SCK2) {
              direction : input;
              capacitance : 1;
            }
            pin(SI) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_falling;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "SCK2";
              }
            }
            pin(Q) {
              direction : output;
            }
            pin(Q2) {
              direction : output;
              timing() {
                timing_type : rising_edge;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                rise_resistance : 0.1;
                fall_resistance : 0.1;
                related_pin : "CP SCK1";
```

Feedback

```
    }
  }
  test_cell() {
    pin(D1 D2 D3 CP) {
      direction : input;
    }
    pin(SCK1) {
      direction : input;
      signal_type : "test_scan_clock_b";
    }
    pin(SCK2) {
      direction : input;
      signal_type : "test_scan_clock_a";
    }
    pin(SI) {
      direction : input;
      signal_type : "test_scan_in";
    }
    statetable("C D ", "Q") {
      table :  "R  H/L : - : H/L,\\\n
               ~R   -  : - :  N";
    }
    pin(Q) {
      direction : output;
      internal_node : "Q";
      input_map : "CP D1";
      signal_type : "test_scan_out";
    }
    pin(Q2) {
      direction : output;
      internal_node : "Q";
      input_map : "CP D2";
      signal_type : "test_scan_out";
    }
  }
}
```

In this case, the pin 'Q' generated error LIBG-161, which generated this error.

MESSAGE EXAMPLE

```
Error: Line 62, The 'libg99' test cell has an incompatible non test mode.
 (LIBG-99)
```

LIBG-100

(warning) The '%s' port in the '%s' cell has both a function\n \tand a test attribute. The test_cell will be deleted.

Feedback

Description

This message indicates that the specified port has both a function statement and a test attribute. For this particular test cell type, a port cannot have both a function statement and a test attribute.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-101.

What Next

Remove either the function statement or the test attribute to correctly specify the test_cell.

LIBG-101

(error) The '%s' port in the '%s' cell has both a function\n \tand a test attribute.

Description

This messages is issued only for single-latch LSSD and muxed-latch scan cells. The port has both a function statement and a test attribute. For the particular test cell type, a port cannot have both a function statement and a test attribute.

A function statement can be a *function*, a *state_function*, or an *internal_node* attribute.

A test attribute can be a *test_scan_in*, a *test_scan_in_inverted*, a *test_scan_enable*, a *test_scan_enable_inverted*, a *test_scan_out*, a *test_scan_out_inverted* , a *test_scan_clock*, a *test_scan_clock_a*, a *test_scan_clock_b*, or a *test_clock*.

What Next

If you can access the original technology library source file, remove either the function statement or the test attribute to correctly specify the test_cell.

Examples

```
cell(libg101) {
            area : 13;
            pin(D SDI) {
              direction : input;
              capacitance : 1;
            }
            pin(C SE) {
              direction : input;
              capacitance : 2;
            }
            pin(QN) {
              direction : output;
            }
```

Feedback

```
test_cell() {
  pin(D C) {
    direction : input;
  }
  pin(SDI) {
    direction : input;
    signal_type : "test_scan_in";
  }
  pin(SE) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_enable";
  }
  statetable("D C", "QN") {
    table : "L/H H : - : H/L,\\\n
             -   L : - : N";
  }
  pin(QN) {
    direction : output;
    inverted_output : TRUE;
    internal_node : "QN";
    signal_type : "test_scan_out_inverted";
  }
 }
}
```

In this case, the pin 'QN' has both an *internal_node* and a *test_scan_out_inverted* attributes.

MESSAGE EXAMPLE

```
Error: Line 152, The 'QN' port in the 'libg101' cell has both a function
        and a test attribute. (LIBG-101)
```

LIBG-102

(warning) The '%s' cell has more than one clock.

Description

The auxiliary clocked LSSD cell has more than one clock. This is not supported by DFT Compiler.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-103.

What Next

This type of cell is not supported by DFT Compiler, so no further action is indicated.

Feedback

LIBG-103

(error) The '%s' cell has more than one clock.

Description

The auxiliary clocked LSSD cell has more than one clock. This is not supported by DFT Compiler.

What Next

This type of cell is not supported by DFT Compiler, so no further action is indicated.

Examples

```
cell(libg103) {
            area : 12;
            pin(D) {
              direction : input;
              capacitance : 1;
            }
            pin(CK,CK2,IH) {
              direction : input;
              capacitance : 1;
            }
            pin(A,B) {
              direction : input
                capacitance : 2;
            }
            pin(SI) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_falling;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "A";
              }
              timing() {
                timing_type : hold_falling;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "A";
              }
            }
            pin(Q) {
              direction : output;
              timing() {
                timing_type : rising_edge;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                rise_resistance : 0.1;
```

Feedback

```
        fall_resistance : 0.1;
        related_pin : "CK IH";
      }
      timing() {
        timing_type : falling_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "B";
      }
    }
    pin(XQ) {
      direction : output;
    }
    test_cell(){
      pin(D,CK,CK2){
        direction : input;
      }
      pin(IH){
        direction : input;
        signal_type : "test_clock";
      }
      pin(SI){
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(A){
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      pin(B){
        direction : input;
        signal_type : "test_scan_clock_b";
      }
      ff("IQ","IQN"){
        clocked_on : "CK CK2";
        next_state : "D";
      }
      pin(Q){
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(XQ){
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, there are two clocks, 'CK' and 'CK2', which is not allowed.

Feedback

MESSAGE EXAMPLE

```
Error: Line 162, The 'libg103' cell has more than one clock. (LIBG-103)
```

LIBG-104

(warning) The '%s' pin of the '%s' design is not a clock pin\n and should not be used in the 'related_pin' of '%s' timing arc.

Description

By definition, a pin in the *related_pin* attribute of the timing group with the *timing_type setup_rising, setup_falling, hold_rising* or *hold_falling* should be a clock pin. It is treated as a warning only for backward compatibility.

What Next

Check your library for a wrong pin in the *related_pin* attribute or for an incorrect *timing_type*.

Examples

```
cell(libg104) {
          area : 10;
          pin(CK) {
            direction : input;
            clock     : true;
            capacitance : 1.0;
          }
          pin(D) {
            direction : input ;
            capacitance : 1.0 ;
            timing() {
              related_pin : "CK";
              timing_type : setup_rising;
              intrinsic_fall : 1.0;
              intrinsic_rise : 1.0;
            }
            timing() {
              related_pin : "CK";
              timing_type : hold_rising;
              intrinsic_fall : 0.1;
              intrinsic_rise : 0.1;
            }
          }
          pin(P) {
            direction : input;
            capacitance : 1.0;
            timing() {
              related_pin : "CK";
              timing_type : setup_rising;
              intrinsic_rise : 0.0;
```

Feedback

```
        }
      }
      ff ("IQ", "IQN") {
         next_state : "D";
         clocked_on : "CK";
         preset : "P";
      }
      pin(Q) {
        direction : output;
        function  : "IQ";
        timing() {
          related_pin : "P";
          timing_type : setup_rising;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
        }
      }
    }
```

The timing group of the pin 'Q' contains the pin 'P' in the related_pin attribute. This caused the warning because the timing_type is *setup_rising*

MESSAGE EXAMPLE

```
Warning: Line 153, The 'P' pin of the 'libg104' design is not a clock pin
        and should not be used in the 'related_pin' of 'setup' timing
 arc. (LIBG-104)
```

LIBG-105

(error) There is a missing timing arc between the '%s' and '%s'\n \tpins in the '%s' cell. A timing arc of the right timing_type\n \tis expected between the two specified pins of the cell.

Description

A timing arc of the right timing_type is expected between the two specified pins of the cell. For example, a timing arc with timing_type rising_edge/falling_edge is required from the clock/enable pin to the output pin. This error might be generated by a previous warning or error such as: LIBG-104.

What Next

Specify or correct the timing arc to make the cell description complete.

Examples

```
cell(libg105) {
          area           : 10;
          pin(CK) {
            direction            : input;
```

Feedback

```
    clock                : true;
    capacitance          : 1.0;
  }
  pin(D) {
    direction            : input;
    capacitance          : 1.0;
    timing() {
      related_pin        : "CK";
      timing_type        : setup_rising;
      intrinsic_fall     : 1.0;
      intrinsic_rise     : 1.0 ;
    }
    timing() {
      related_pin        : "CK";
      timing_type        : hold_rising;
      intrinsic_fall     : 0.0;
      intrinsic_rise     : 0.0;
    }
  }

  pin(P) {
    direction            : input;
    capacitance          : 1.0;
    timing() {
      related_pin        : "CK";
      timing_type        : setup_rising;
      intrinsic_rise     : 0.0;
    }
  }
  ff ("IQ", "IQN") {
     next_state : "D";
     clocked_on : "CK";
     preset : "P";
 }
  pin(Q) {
    direction            : output;
    function             : "IQ";
    timing() {
      related_pin        : "CK";
      timing_type        : rising_edge;
      intrinsic_rise     : 1.0;
      intrinsic_fall     : 1.0;
    }
  }
}
```

A timing group is missing in the pin 'Q' for the pin 'P'.

MESSAGE EXAMPLE

```
Error: Line 151, There is a missing timing arc between the 'P' and 'Q'
        pins in the 'libg105' cell. A timing arc of the right timing_type
```

Feedback

```
       is expected between the two specified pins of the cell.
(LIBG-105)
```

LIBG-106

(warning) The '%s' timing type is invalid between the\n \ttwo specified pins.

Description

The specified *timing_type* attribute is invalid between the pin that has the timing group and the pin in the *related_pin* attribute specified. It is most likely that you have specified a "combinational" timing arc from the clock, enable, clear, or preset pin to the output pin, or that the *timing_type* attribute is missing.

What Next

Specify the correct timing_type attribute.

Examples

```
cell(libg106) {
          area            : 10;
          pin(CK) {
            direction             : input;
            clock                 : true;
            capacitance           : 1.0;
          }
          pin(D) {
            direction             : input;
            capacitance           : 1.0;
            timing() {
              related_pin         : "CK";
              timing_type         : setup_rising;
              intrinsic_fall      : 1.0;
              intrinsic_rise      : 1.0;
            }
            timing() {
              related_pin         : "CK";
              timing_type         : hold_rising;
              intrinsic_fall      : 0.0;
              intrinsic_rise      : 0.0;
            }
          }
          pin(P) {
            direction             : input;
            capacitance           : 1.0;
            timing() {
              related_pin         : "CK";
              timing_type         : setup_rising;
              intrinsic_rise      : 0.0;
            }
          }
```

Feedback

```
          ff ("IQ", "IQN") {
             next_state : "D";
             clocked_on : "CK";
             preset : "P";
          }
          pin(Q) {
            direction            : output;
            function             : "IQ";
            timing() {
              related_pin        : "CK";
              timing_type        : setup_rising;
              intrinsic_rise     : 1.0;
              intrinsic_fall     : 1.0
            }
          }
        }
```

In this case, there is a 'setup_rising' attribute between the output port 'Q' and the clock 'CK'.

MESSAGE EXAMPLE

```
Warning: Line 151, The 'setup_rising' timing type is invalid between the
        two specified pins. (LIBG-106)
```

LIBG-107

(error) The complex state_function is not allowed in the '%s' test cell.

Description

The test cell has a port with a complex state_function. A complex state_function is any expression not equivalent to a buffer or an inverter.

Currently, complex state_functions are not supported in test cells.

What Next

Either remove the state_function or make it into a buffer or an inverter.

Examples

```
cell(libg107) {
    area : 21;
    pin(D1 D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C1 C2 C3) {
      direction : input;
      capacitance : 2;
    }
```

Feedback

```
    pin(Q1 Q2 Q2N) {
      direction : output;
    }
    pin(Q1N) {
      direction : output;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C2";
      }
    }
    test_cell() {
      pin(D1 C1 C3) {
        direction : input;
      }
      pin(D2) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(C2) {
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      statetable ("C1 D1 C3", "Q1 Q2") {
        table : "H L/H - : H - : L/H -,\\\n
                   H - -   : L - : L -,\\\n
                 - -   H : L/H - : - L/H,\\\n
                   - -   - : - - : N   N";
      }

      pin(Q1) {
        direction : output;
        internal_node : "Q1";
      }
      pin(Q1N) {
        direction : output;
        state_function : "Q1'";
      }
      pin(Q2) {
        direction : output;
        internal_node : "Q2";
        signal_type : "test_scan_out";
      }
      pin(Q2N) {
        direction : output;
        /* This state_function is too complex, change it to a
buffer/inverter*/
        state_function : "Q2' + C1";
        signal_type : "test_scan_out_inverted";
      }
```

Feedback

```
    }
  }

}
```

Examples

```
Error: Line 134, The complex state_function is not allowed in the
 'libg107' test cell. (LIBG-107)
```

LIBG-108

(error) The three_state attribute is not allowed in the '%s' test cell.

Description

The test cell has a port with a three_state attribute.

Currently, the three_state attribute is not supported in test cells.

What Next

Remove the three_state attribute from the test cell.

Examples

```
cell(libg108) {
    area : 21;
    pin(D1 D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C1 C2 C3) {
      direction : input;
      capacitance : 1;
    }
    pin(Q1 Q2 Q2N) {
      direction : output;
    }
    pin(Q1N) {
      direction : output;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C2";
      }
    }
    test_cell() {
      pin(D1 C1 C3) {
```

Feedback

```
        direction : input;
      }
      pin(D2) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(C2) {
        direction : input;
        signal_type : "test_scan_clock_a";
      }
      statetable ("C1 D1 C3", "Q1 Q2") {
        table : "H L/H - : H - : L/H -,\\\n
                 H - - : L - : L -,\\\n
                 - -   H : L/H - : - L/H,\\\n
                 - -   - : - - : N   N";
      }

      pin(Q1) {
        direction : output;
        internal_node : "Q1";
      }
      pin(Q1N) {
        direction : output;
        state_function : "Q1'";
      }
      pin(Q2) {
        direction : output;
        internal_node : "Q2";
        signal_type : "test_scan_out";
      }
      pin(Q2N) {
        direction : output;
        state_function : "Q2'";
        /* three_state attribute is not allowed in test_cell */
        three_state : "C1";
        signal_type : "test_scan_out_inverted";
      }
    }
  }

}
```

Examples

```
Error: Line 169, The three_state attribute is not allowed in the
 'libg108' test cell. (LIBG-108)
```

LIBG-109

(warning) Asynchronous specifications in the '%s' cell are\n \tincompletely specified.

Feedback

Description

There is a set of input values for asynchronous inputs that causes more than one force_* condition to be true. The force_* conditions are not mutually exclusive; the cell is unspecified when more than one force_* condition is valid.

Design Compiler cannot support this cell and might generate invalid logic if the cell is used.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-110.

What Next

You can put the attributes *dont_touch* and *dont_use* on the library cell to prevent this cell from being used and potentially generating invalid logic.

Alternatively, you can change the source technology library. Change the force_* expressions so they are mutually exclusive. There should be no input condition for which more than one force_* statement is valid.

LIBG-110

(warning) Asynchronous specifications in the '%s' cell \n are incomplete or are not mutually exclusive.\n \tThe cell has been made a black box.

Description

There is a set of input values for asynchronous inputs that causes more than one force_* condition to be true.

The force_* conditions are not mutually exclusive; the cell is unspecified when more than one force_* condition is valid.

Design Compiler cannot support this cell; therefore, the cell has been made a black box.

What Next

Change the force_* expressions so they are mutually exclusive. There should be no input condition for which more than one force_* statement is valid.

Examples

```
cell(libg110) {
  area : 10;
  pin(force11) {
    direction : input;
    capacitance : 1;
  }
```

Feedback

```
  pin(force10) {
    direction : input;
    capacitance : 1;
  }
  pin(force01) {
    direction : input;
    capacitance : 1;
  }
  pin(force00) {
    direction : input;
    capacitance : 2;
  }
  pin(ck) {
    direction : input;
    capacitance : 2;
  }
  pin(next) {
    direction : input;
    capacitance : 2;
  }
  state("IQ","IQN") {
    next_state : "next";
    clocked_on : "ck";
    force_00   : "force00";
    force_01   : "force01";
    force_10   : "force10";
    force_11   : "force11";
  }
  statetable ("next ck ck* force00 force01 force10 force11", "out") {
    table : "- - - H L L L : - : L,\\\n
             - - - L H L L : L/H : L,\\\n
             - - - L L H L : - : H,\\\n
             - - - L L L H : - : H,\\\n
             L/H H L L L L L : - : L/H,\\\n
             - L L L L L L : - : N,\\\n
             - L H L L L L : - : N,\\\n
             - H H L L L L : - : N";
  }

  pin(Q) {
    function : "IQ";
    internal_node : "out";
    direction : output;
  }
}
```

Examples

```
Warning: Line 111, Asynchronous specifications in the 'libg110' cell
        are incomplete or are not mutually exclusive.
        The cell has been made a black box. (LIBG-110)
```

Feedback

LIBG-111

(warning) Design Compiler does not support the values for\n \tclear_preset_var? in the '%s' cell. The cell has been made a black box.

Description

The cell has invalid values (N, X or T) for clear_preset_var1 and clear_preset_var2.

Because of these values, Design Compiler cannot support the cell. The cell has been made a black box.

What Next

Change the N, X or T value to a L or H value.

Examples

```
cell(libg111) {
        area : 11;
        pin(D) {
                direction : input;
                capacitance : 1;
        }
        pin(CP) {
                direction : input;
                capacitance : 1;
        }
        pin(CLR) {
                direction : input;
                capacitance : 1;
        }
        pin(SET) {
                direction : input;
                capacitance : 1;
        }
        ff("IQ","IQN") {
                next_state : "D";
                clocked_on : "CP";
                clear   : "CLR'";
                preset   : "SET'";
                clear_preset_var1 : X;
                clear_preset_var2 : X;
        }
        pin(Q) {
                direction : output;
                function : "IQ";
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
```

```
                        fall_resistance : 0.1;
                        related_pin : "CP";
                }
                timing() {
                        timing_type : clear;
                        timing_sense : positive_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "CLR";
                }
                timing() {
                        timing_type : preset;
                        timing_sense : negative_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "SET";
                }
        }
        pin(QN) {
                direction : output;
                function : "IQN";
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
                        fall_resistance : 0.1;
                        related_pin : "CP";
                }
                timing() {
                        timing_type : preset;
                        timing_sense : negative_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "CLR";
                }
                timing() {
                        timing_type : clear;
                        timing_sense : positive_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "SET";
                }
        }
}
```

Examples

```
Warning: Line 111, Design Compiler does not support the values for
        clear_preset_var? in the 'libg111' cell. The cell has been made a
 black box. (LIBG-111)
```

Feedback

LIBG-112

(error) The timing check condition represented in this timing\n \tgroup is not mutually exclusive with the timing check condition\n \trepresented in the timing group on line %d.

Description

The timing check conditions represented by the 'when' string of all conditional period and pulse width timing checks should be mutually exclusive. A nonconditional timing check is assumed to have the implied '1' timing check condition (always *TRUE*). If timing check conditions are not mutually exclusive, Library Compiler cannot determine which timing check to use when the condition causes both timing check conditions to be evaluated *TRUE*.

What Next

Check the 'when' strings of both timing groups, and make corrections necessary to eliminate duplicate nonconditional timing checks or other erroneous information. Also, ensure that there is no nonconditional timing check defined when at least one conditional timing check of the same pins and timing type is defined.

Examples

```
cell(libg112) {
        area : 6.0;
        pin(CLK) {
                direction : input;
                capacitance : 1.0;
                minimum_period() {
                        constraint : 99;
                        when : " Q'";
                        sdf_cond : "SIG_5 == 1'b1 ";
                }
                minimum_period() {
                        constraint : 99;
                        when : " Q'"
                        sdf_cond : "SIG_5 == 1'b0 ";
                }
        }
        pin(SET) {
                direction : input;
                capacitance : 1.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
```

Feedback

```
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
                        fall_resistance : 0.1;
                        related_pin : "CLK";
                }
                timing() {
                        timing_type : preset;
                        timing_sense : negative_unate;
                        intrinsic_rise : 1.0;
                        rise_resistance : 0.1;
                        related_pin : "SET";
                }
        }
        pin(QN) {
                direction : output;
                function : "IQN";
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
                        fall_resistance : 0.1;
                        related_pin : "CLK";
                }
                timing() {
                        timing_type : clear;
                        timing_sense : positive_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "SET";
                }
        }
```

Examples

```
Error: Line 115, The timing check condition represented in this timing
        group is not mutually exclusive with the timing check condition
        represented in the timing group on line 120. (LIBG-112)
```

LIBG-112w

(warning) The timing check condition represented in this timing\n \tgroup is not mutually exclusive with the timing check condition\n \trepresented in the timing group on line %d.

Description

The timing check conditions represented by the 'when' string of all conditional period and pulse width timing checks should be mutually exclusive. A nonconditional timing check

Feedback

is assumed to have the implied '1' timing check condition (always *TRUE*). If timing check conditions are not mutually exclusive, Library Compiler cannot determine which timing check to use when the condition causes both timing check conditions to be evaluated *TRUE*.

The following example shows an instance where this message occurs:

```
cell(libg112) {
        area : 6.0;
        pin(CLK) {
                direction : input;
                capacitance : 1.0;
                minimum_period() {
                        constraint : 99;
                        when : " Q'";
                        sdf_cond : "SIG_5 == 1'b1 ";
                }
                minimum_period() {
                        constraint : 99;
                        when : " Q'"
                        sdf_cond : "SIG_5 == 1'b0 ";
                }
        }
        pin(SET) {
                direction : input;
                capacitance : 1.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
                        fall_resistance : 0.1;
                        related_pin : "CLK";
                }
                timing() {
                        timing_type : preset;
                        timing_sense : negative_unate;
                        intrinsic_rise : 1.0;
                        rise_resistance : 0.1;
                        related_pin : "SET";
                }
        }
        pin(QN) {
```

Feedback

```
                direction : output;
                function : "IQN";
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
                        fall_resistance : 0.1;
                        related_pin : "CLK";
                }
                timing() {
                        timing_type : clear;
                        timing_sense : positive_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "SET";
                }
        }
```

The following is an example message:

```
Warning: Line 115, The timing check condition represented in this timing
        group is not mutually exclusive with the timing check condition
        represented in the timing group on line 120. (LIBG-112w)
```

What Next

Check the 'when' strings of both timing groups, and make corrections necessary to eliminate duplicate nonconditional timing checks or other erroneous information. Also, ensure that there is no nonconditional timing check defined when at least one conditional timing check of the same pins and timing type is defined.

LIBG-113

(error) The timing check starting and ending conditions\n \trepresented in this timing group are not mutually exclusive with the\n \ttiming check starting and ending conditions represented in the \n \ttiming group on line %d.

Description

One of the following two conditions must be satisfied between two conditional timing checks of the same pins:

1. The timing check starting conditions represented by the **when_start** or **when** string of all conditional timing checks (setup, hold, recovery, removal and skew) are mutually exclusive.
2. The timing check ending conditions represented by the **when_end** or **when** string of all conditional timing checks (setup, hold, recovery, removal and skew) are mutually exclusive.

A nonconditional timing check is assumed to have the implied '1' timing check starting and ending condition (always *TRUE*). If both starting and ending conditions are not mutually exclusive, Library Compiler cannot determine which timing check to use when the condition enables both conditional timing check conditions.

What Next

Check the *when_start*, *when_end* and *when* strings of both timing groups and make any corrections necessary to eliminate duplicate nonconditional timing checks or other erroneous information. Also, ensure that there is no nonconditional timing check defined when at least one conditional timing check of the same pins and timing type is defined.

Examples

```
cell(libg113) {
    area : 10;
    pin(D) {
      direction : input;
      capacitance : 1;
      /* these two timing groups are not mutually exclusive */
      timing() {
        timing_type : setup_falling;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        when : " MQ ";
        sdf_cond : " MQ == 1'b1 ";
        related_pin : "MC";
      }
      timing() {
        timing_type : setup_falling;
        when : " MQ ";
        sdf_cond : " MQ == 1'b1 ";
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        related_pin : "MC";
      }
    }
    pin(MC) {
      direction : input;
      capacitance : 2;
    }
    statetable ( "D CP", "Q ") {
        table : "H/L  R : - : H/L,\\\n
                 -   ~R : - : N ";
    }

    pin (MQ) {
      direction : internal;
      inverted_output : FALSE;
      internal_node : "Q";
      input_map : "D MC MQ";
    }
```

Feedback

```
    pin(Q) {
      direction : output;
      internal_node : "Q";
      input_map : "MQ MC Q";
      inverted_output : FALSE;
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "MC";
      }
    }
 }
```

Examples

```
Error: Line 116, The timing check starting and ending conditions
        represented in this timing group are not mutually exclusive with
 the
        timing check starting and ending conditions represented in the
        timing group on line 124. (LIBG-113)
```

LIBG-115

(warning) The when attribute uses '%s' pins\n \tthat cannot be found in the %s %s.

Description

In a sequential cell, the following pins are allowed to appear in the *when* attribute of the *state-dependent* timing arc:

1) Pins used in *enable*, *enable_also*, and *data_in* in the *latch* group

2) Pins used in *clocked_on*, *clocked_on_also*, and *next_state* in the *ff* group for *timing_arc* with *timing_type* of *rising_edge/falling_edge*

If the timing arc's timing_type is clear/preset:

1) The related clear or preset attribute must be specified inside the sequential group.

2) The clear/preset pin must be used in related_pin or when attribute of the timing arc.

This warning informs you that one of the previous restrictions has been violated.

What Next

Check your *when* attribute, and correct any wrong information in the string or in the *timing_type*.

Feedback

Examples

```
cell(libg115) {
  area : 9;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  pin(CD) {
    direction : input;
    capacitance : 2;
  }
  ff("IQ","IQN") {
    next_state : "D";
    clocked_on : "CP";
    clear   : "CD'";
  }
  pin(Q) {
    direction : output;
    function : "IQ";
    timing() {
      when : "CD";
      sdf_cond : "D==1'b1";
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP";
    }
     timing() {
      timing_type : clear;
      timing_sense : positive_unate;
      intrinsic_fall : 1.0;
      fall_resistance : 0.1;
      related_pin : "CD";
    }
  }
}
```

Examples

```
Warning: Line 134, The when attribute uses 'CD' pins
        that cannot be found in the ff/latch group . (LIBG-115)
```

Feedback

LIBG-116

(warning) No test_scan_in/test_scan_in_inverted signal \n \ttypes exist on the '%s' test_cell cell. Converting the entire cell to a black box.

Description

To be able to accept scan data, each test_cell must have either a *test_scan_in* or *test_scan_in_inverted* signal type.

This warning informs you that the indicated test_cell does not have the *test_scan_in* or *test_scan_in_inverted* signal types. Thus, the test_cell is not valid, and the entire cell has been converted to a black box.

There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. you can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-147.

What Next

Check the library description to ensure that each test_cell has a *test_scan_in* or *test_scan_in_inverted* signal type. These signal types can be added within the test_cell using this syntax:

```
signal_type : test_scan_in (or test_scan_in_inverted)
```

LIBG-117

(warning) No test_scan_out/test_scan_out_inverted signal \n \ttypes exisit on the '%s' test_cell cell. Converting the entire cell to a black box.

Description

To be able to scan out data, each test_cell must have either a *test_scan_out* or a *test_scan_out_inverted* signal type.

This warning informs you that the indicated test_cell has neither the *test_scan_out* nor the *test_scan_out_inverted* signal types. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-148.

Feedback

What Next

Check the library description to ensure that each test_cell either has a *test_scan_out* or a *test_scan_out_inverted* signal type. These signal types can be added within the test_cell using this syntax:

```
signal_type : test_scan_out (or test_scan_out_inverted)
```

LIBG-118

(warning) The clocked_on_also function on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.\n \tConverting the entire cell to a black box.

Description

The *clocked_on_also* function for this test_cell is not specified on the correct pin. This function needs to be specified on the clock of the slave stage of a master-slave configuration.

This warning informs you that the test_cell pointed to has the *clocked_on_also* function specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. Other tools will not be able to use this cell if it is made into a black box.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-149.

What Next

Check the library description to ensure that each test_cell has specified the *clocked_on_also* function. To determine the correct function:

```
* Create a cell with the non test mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

LIBG-119

(warning) The test_scan_clock_b signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.\n \tConverting the entire cell to a black box.

Feedback

Description

The *test_scan_clock_b* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock of the slave stage of an LSSD configuration.

This warning informs you that the test_cell pointed to has the *test_scan_clock_b* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. Other tools will not be able to use this cell if it is made into a black box.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-150.

What Next

Check the library description to ensure that each test_cell has specified the *test_scan_clock_b* signal type.

LIBG-120

(warning) The test_scan_in signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.\n \tConverting the entire cell to a black box.

Description

The *test_scan_in* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that takes in the scan data. All scan types and, thus, all test_cells need to have either the *test_scan_in* or *test_scan_in_inverted* signal type.

This warning informs you that the test_cell pointed to has the *test_scan_in* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box . There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-151.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_in* signal type.

Feedback

LIBG-121

(warning) The test_scan_in_inverted signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.\n \tConverting the entire cell to a black box.

Description

The *test_scan_in_inverted* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that takes in the scan data. All scan types and, thus, all test_cells need to have either the *test_scan_in* or *test_scan_in_inverted* signal type.

This warning informs you that the test_cell pointed to has the *test_scan_in_inverted* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-152.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_in_inverted* signal type.

LIBG-122

(warning) The test_scan_enable signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.\n \tConverting the entire cell to a black box.

Description

The *test_scan_enable* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that switches the input mode of the cell between test and mission mode. Only multiplexed flip-flop requires this signal type. This signal type can also be used in clocked scan cells.

This warning informs you that the test_cell pointed to has the *test_scan_enable* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-153.

Feedback

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_enable* signal type.

LIBG-123

(warning) The test_scan_enable_inverted signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.\n \tConverting the entire cell to a black box.

Description

The *test_scan_enable_inverted* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that switches the input mode of the cell between test and mission mode. Only, multiplexed flip-flop requires this signal type. This signal type can also be used in clocked scan cells.

This warning informs you that the test_cell pointed to has the *test_scan_enable_inverted* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-154.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_enable_inverted* signal type.

LIBG-124

The test_scan_clock signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.\n \tConverting the entire cell to a black box.

Description

The *test_scan_clock* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the scan clock for clocked scan cells.

This warning informs you that the test_cell pointed to has the *test_scan_clock* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-155.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_clock* signal type.

LIBG-125

warning) The test_scan_clock_a signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.\n \tConverting the entire cell to a black box.

Description

The *test_scan_clock_a* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock of the master stage of an LSSD configuration.

This warning informs you that the test_cell pointed to has the *test_scan_clock_a* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-156.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_clock_a* signal type.

LIBG-126

(warning) The test_clock signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin. \n \tConverting the entire cell to a black box.

Description

The *test_clock* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock used for ATPG capture in auxiliary clock lssd cells.

This warning informs you that the test_cell pointed to has the *test_clock* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is

converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-157.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_clock* signal type.

LIBG-127

(warning) The '%s' clocked test cell is not valid \n \tbecause it has a master-slave cell as its nontest mode.\n \tConverting the entire cell to a black box.

Description

A clocked test cell has the following characteristics:

```
- signal types : test_scan_in/test_scan_in_inverted, test_scan_enable/
        test_scan_enable_inverted (optional), test_scan_clock,
        test_scan_out/test_scan_out_inverted

    - nontest modes : flip-flop or latch
```

This warning informs you that the signal types identify this cell as a clocked scan test cell, but it does not have a flip-flop or latch as its nontest mode. It is currently specified as a master-slave cell. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-174.

What Next

Check the library description to ensure that nontest modes and signal types are correctly pointed to by the test_cell. To determine why the nontest function is not one of the previous types,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

Feedback

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-128

(warning) Invalid nontest mode for test_cell on the '%s' cell;\n \tthere are more than 2 sequential elements. \n \tConverting the entire cell to a black box.

Description

The nontest mode for test_cells must be one of the following:

```
- A single flip-flop
        - A single latch
        - A single master-slave latch configuration using clocked_on and
                clocked_on_also
```

This warning informs you that the nontest mode of the test_cell has more than 2 distinct sequential elements, so the test_cell does not fit the previous requirements. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

What Next

Check the library description to ensure that each test_cell has properly specified the correct nontest mode. To determine why there are multiple sequential elements in this description,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-129

(warning) Invalid nontest mode for test_cell on the '%s' cell. \n \tThis mode describes a ganged cell.

Feedback

Description

The nontest mode for test_cells must be one of the following:

```
- A single flip-flop
        - A single latch
        - A single master-slave latch configuration using clocked_on and
                clocked_on_also
```

This warning informs you that the nontest mode of the test cell is a ganged cell, and it does not fit the previous requirements. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

What Next

Check the library description to ensure that each test_cell does not specify a ganged cell as its nontest mode. Ganged cells can be recognized by the keywords ff_bank or latch_bank.

LIBG-130

(warning) The nontest mode for test_cell on the '%s' cell is invalid.\n \tThe '%s' slave port does not directly feed the output.

Description

The nontest mode for test_cells must be one of the following:

```
- A single flip-flop
        - A single latch
        - A single master-slave latch configuration using clocked_on
          and clocked_on_also
```

This warning informs you that in nontest mode of the test cell, the slave does not directly feed the output. This means that it is not a master-slave latch configuration that the DFT Compiler supports. Thus, the test_cell is not valid, and the entire cell is a black box.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-160.

Feedback

What Next

Check the library description to ensure that the nontest mode of the test_cell is correctly specified. If you are using a master-slave configuration as the nontest mode, the only accepted description is the state description using

```
clocked_on : <master clock>
        clocked_on_also : <slave clock>
```

LIBG-131

(warning) The nontest mode for test_cell on the '%s' cell is invalid.\n \tThe '%s' state pin is not a latch for a master-slave configuration.

Description

The nontest mode for test_cells must be one of the following:

```
- A single flip-flop
        - A single latch
        - A single master-slave latch configuration using clocked_on
          and clocked_on_also
```

This warning informs you that the nontest mode of the test cell is an incorrect master-slave description. This stage of the master-slave configuration is not a latch, and it does not fit the previous requirements. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-161.

What Next

Check the library description to ensure that the nontest mode of the test_cell is correctly specified. If you are using a master-slave configuration as the nontest mode, the only accepted description is the state description using clocked_on : <master clock> clocked_on_also : <slave clock>

LIBG-132

(warning) The test cell for auxiliary clocked lssd '%s' cell is not\n \tvalid because its nontest mode is not a flip-flop.

Feedback

Description

An auxiliary clocked lssd test_cell has the following characteristics:

```
- signal types : test_scan_in/test_scan_in_inverted,
                         test_scan_out/test_scan_out_inverted,
                         test_scan_clock_a, test_scan_clock_b, test_clock
        - nontest mode : flip-flop
```

This warning informs you that the signal types point to this auxiliary clocked lssd test_cell, but it does not have a flip-flop as its nontest mode. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-175.

What Next

Check the library description to ensure that nontest modes and signal types are correctly pointed to by the test_cell. To determine why the nontest function is not one of the previous types,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-133

(warning) The test_cell on the '%s' cell cannot have more than one\n \ttest_scan_in/ test_scan_in_inverted signal type. This happens on \n \tthe '%s' port.

Description

Each test_cell must have only one test_scan_in or test_scan_in_inverted signal type. This signal type is specified on the pin that is used to take scan data into the cell.

This warning informs you that the test_cell pointed to has multiple test_scan_in(test_scan_in_inverted) signal types. The message points to the second port that has this signal type. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-162.

What Next

Check the library description to ensure that each test_cell has only one test_scan_in or test_scan_in_inverted signal type.

LIBG-134

(warning) The '%s' port in test_cell on the '%s' cell has a\n \ttest_scan_out signal type on an inverted output.

Description

The test_scan_out signal type can only be specified on a noninverted output. If the output is inverted, the proper signal type should be test_scan_out_inverted. This signal type specifies the polarity of the port with respect to the state.

This warning informs you that the test_cell pointed to has the test_scan_out signal type specified on an inverted output. When reading a .db library, Library Compiler ignores the scan_out attribute and creates the functional description of the cell using the function statement. In other words, that output is inverted in the functional description.

The same problem in a .lib library causes an error. See the .lib example for LIBG-163.

What Next

The default behavior of selecting the function over the signal_type to determine the inversion of the output is be correct in most cases.

Check the library description to ensure that the test_scan_out signal type is only placed on noninverted outputs. To determine if this is an inverted or noninverted output,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, an inverted output is not a state if it does not have N. Instead, the output contains an inversion of the state pin.

Feedback

LIBG-135

(warning) The '%s' port in test_cell on the '%s' cell has a\n \ttest_scan_out_inverted signal type on a noninverted output.

Description

The test_scan_out_inverted signal type can only be specified on an inverted output. If the output is noninverted, the proper signal type should be test_scan_out. This signal type specifies the polarity of the port with respect to the state.

This warning informs you that the test_cell pointed to has the test_scan_out signal type specified on an inverted output. When reading a .db library, the Library Compiler ignores the scan_out_inverted attribute and creates the functional description of the cell using the function statement. In other words, that output is noninverted in the functional description.

The same problem in a .lib library causes an error. See the .lib example for LIBG-164.

What Next

The default behavior of selecting the function over the signal_type to determine the inversion of the output is correct in most cases.

Check the library description to ensure that the test_scan_out_inverted signal type is only placed on inverted outputs. To determine if this is an inverted or noninverted output,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, an inverted output is not a state if it does not have N. Instead, the output contains an inversion of the state pin.

LIBG-136

(warning) The test cell on the '%s' cell cannot have more than one\n \ttest_scan_enable or test_scan_enable_inverted signal type. This \n \thappens on the '%s' port.

Description

Each test_cell must have only one test_scan_enable or test_scan_enable_inverted signal type. This signal type is specified on the pin that is used to select between scan and mission mode operation of the cell.

This warning informs you that the test_cell pointed to has multiple test_scan_enable(test_scan_enable_inverted) signal types. The message points to the

Feedback

second port that has this signal type. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-165.

What Next

Check the library description to ensure that each test_cell has only one test_scan_enable or test_scan_enable_inverted signal type.

LIBG-137

(warning) The test_scan_clock '%s' port in test_cell on the '%s' cell\n \tdoes not have an active sense.

Description

The test_scan_clock must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock is the scan clock in the clocked scan type.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell is recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error.

What Next

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

Feedback

LIBG-138

(warning) The test_scan_clock_a '%s' port in test_cell on the '%s' cell \n \tdoes not have an active sense.

Description

The test_scan_clock_a must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock_a is the scan clock for the master stage of the LSSD scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell is recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error.

What Next

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell,

```
* Create a cell with the non test mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

LIBG-139

(warning) The test_scan_clock_b '%s' port in test_cell on the '%s' cell\n \tdoes not have an active sense.

Description

The test_scan_clock_b must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock_a is the scan clock for the slave stage of the LSSD scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell is recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error.

What Next

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

LIBG-140

(warning) The test_clock '%s' port in test_cell on the '%s' cell does\n \tnot have an active sense.

Description

The test_clock must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_clock is the capture clock used by ATPG in the auxiliary clocked lssd scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell is recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error.

What Next

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

Feedback

LIBG-141

(warning) The '%s' port in test_cell for the '%s' cell has an invalid\n \tsignal type %s.

Description

The valid signal_types in test_cells are

```
- test_scan_in
        - test_scan_in_inverted
        - test_scan_enable
        - test_scan_enable_inverted
        - test_scan_out
        - test_scan_out_inverted
        - test_scan_clock
        - test_scan_clock_a
        - test_scan_clock_b
        - test_clock
```

This warning informs you that the port in the test_cell pointed to has a signal_type other than the ones listed previously. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

What Next

Check the test_cell pointed to, and change the invalid signal_type.

LIBG-142

(warning) The LSSD test_cell for the '%s' cell has neither\n \ta test_scan_clock_b signal type nor a master-slave configuration as its non test mode.

Description

LSSD scan styles must have the following test_cell characteristics:

```
clocked lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b
        - nontest mode: flip_flop
   auxiliary clock lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b,
                test_clock
        - nontest mode : flip_flop
   single-latch lssd
```

```
       - signal types : test_scan_in/test_scan_in_inverted,
test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
test_scan_clock_b
       - nontest mode: latch
  single-latch lssd
       - signal types : test_scan_in/test_scan_in_inverted,
test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
                test_scan_clock_b (optional)
       - nontest mode: master-slave (clocked_on & clocked_on_also)
```

This warning informs you that the other signal types point to the fact that this is an lssd scan style because it has test_scan_in or test_scan_in_inverted, test_scan_out or test_scan_out_inverted, and test_scan_clock_a signal types. However, it is invalid because it has neither a test_scan_clock_b signal type nor a master-slave configuration as its nontest mode. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-171.

What Next

Check the library description to ensure that each test_cell has correctly specified the nontest modes and signal types in the test_cell pointed to. If you do not understand why the nontest function is not one of the previous types,

```
* Create a cell with the nontest mode as the functional part
         of the cell.
       * Compile this cell.
       * Issue the following command:

            report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-144

(warning) The test_cell for the '%s' cell is not valid because\n \tit has missing or extra test signals.

Feedback

Description

The supported scan styles must have the following test_cell characteristics:

```
multiplexed flip-flop
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_enable/
                test_scan_enable_inverted,
 test_scan_out/test_scan_out_inverted
        - nontest mode : flip-flop, master slave latch pair, or latch
   clocked scan
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_enable/
                test_scan_enable_inverted (optional), test_scan_clock,
                test_scan_out/test_scan_out_inverted
        - nontest modes : flip-flop or latch
   clocked lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b
        - nontest mode: flip-flop
   auxiliary clock lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b,
                test_clock
        - nontest mode : flip-flop
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b
        - nontest mode: latch
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b
        - nontest mode: latch
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
                test_scan_clock_b (optional)
        - nontest mode: master-slave (clocked_on & clocked_on_also)
```

This warning informs you that the other signal types do not correspond to one of the previously supported scan styles. Because there are extra or missing signal types, this test_cell is not valid, and the entire cell is a black box.

Feedback

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-172.

What Next

Check the library description to ensure that each test_cell has correctly specified the nontest modes and signal types in the test_cell pointed to. If you do not understand why the nontest function is not one of the previous types,

```
* Create a cell with the non test mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by checking their functional description.

LIBG-145

(warning) Cannot derive full function based on test_cell\n \ton the '%s' cell in a library with DPCM vendor specific delay model.

Description

The Library Compiler generates a functional description of the entire cell based on the information in the test_cell. However, if the library is a DPCM library, no full function description will be generated.

This warning is not issued when reading a .db library.

What Next

Fill the full function with state table description.

LIBG-146

(warning) Cannot derive full function based on test_cell\n \ton the '%s' cell due to previous warnings or errors.

Description

The Library Compiler generates a functional description of the entire cell based on the information in the test_cell. However, if there are warnings or errors in the test_cell, a functional description of the entire cell cannot be generated.

Feedback

This warning informs you that the test_cell pointed to has previous errors or warnings. Thus, the test_cell is not valid, and the entire cell is a black box. There is functional information missing, and other tools cannot use this cell.

This warning is issued when reading a .db library. You can switch off the warning by setting the environment variable *read_db_lib_warnings* to FALSE (default).

The same problem in a .lib library causes an error. See the .lib example for LIBG-173.

What Next

Fix the previous problems in order to recognize both the test_cell and full cell functionality. You might have to add a state table description of the entire cell.

LIBG-147

(error) No test_scan_in/test_scan_in_inverted signal\n \ttypes exist on the '%s' test_cell cell.

Description

Each test_cell must have either a test_scan_in or test_scan_in_inverted signal type to be valid. Otherwise, this cell cannot accept scan data.

This warning informs you that the test_cell pointed to does not have the test_scan_in or test_scan_in_inverted signal types. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has a *test_scan_in* or *test_scan_in_inverted* signal type. These signal types can be added within the test_cell using the syntax:

```
signal_type : test_scan_in [ or test_scan_in_inverted]
```

Examples

```
cell(libg147) {
      area : 10;
      pin(D) {
        direction : input;
        capacitance : 1;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
      }
      pin(D2) {
```

Feedback

```
  direction : input;
  capacitance : 1;
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(C3) {
  direction : input;
  capacitance : 1;
}
pin(MQ) {
  direction : internal;
  internal_node : "MQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
          ~R   -  - H  -  : H/L - :  -  H/L,\\\n
          ~R   -  - L  -  : -   - :  -  N,\\\n
           R   -  H -  -  : -   - :  X  X,\\\n
           R   -  - H  -  : -   - :  X  X,\\\n
```

Feedback

```
                ~R   -  H - H/L : -   - : H/L -,\\\n
                ~R   -  L -  -  : -   - :  N  -";
        }
        test_cell() {
          pin(D) {
            direction : input;
          }
          pin(C) {
            direction : input;
            capacitance : 2;
            signal_type : "test_scan_clock";
          }
          pin(D2) {
          /* missing test_scan_in signal_type */
            direction : input;
          }
          pin(C2) {
            direction : input;
            capacitance : 2;
            signal_type : "test_scan_clock_a";
          }
          pin(C3) {
            direction : input;
            capacitance : 1;
            signal_type : "test_scan_clock_b";
          }
          ff ("IQ","IQN") {
            next_state : "D";
            clocked_on : "C";
          }
          pin(Q) {
            direction : output;
            function : "IQ";
            signal_type : "test_scan_out";
          }
          pin(QN) {
            direction : output;
            function : "IQN";
            signal_type : "test_scan_out_inverted";
          }
        }
      }
    }
```

Examples

```
Error: Line 177, No test_scan_in/test_scan_in_inverted signal
        types exist on the 'libg147' test_cell cell. (LIBG-147)
```

Feedback

LIBG-148

(error) No test_scan_out/test_scan_out_inverted signal\n \ttypes exist on the '%s' test_cell cell.

Description

Each test_cell must have either a test_scan_out or test_scan_out_inverted signal type in order to be valid. Otherwise, this cell cannot scan out data.

This warning informs you that the test_cell pointed to does not have the test_scan_out or test_scan_out_inverted signal types. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has a test_scan_out or test_scan_out_inverted signal type. These signal types can be added within the test_cell using the syntax:

```
signal_type : test_scan_out [ or test_scan_out_inverted]
```

Examples

```
cell(libg148) {
      area : 9;
      pin(D) {
        direction : input;
        capacitance : 1;
      }
      pin(C) {
        direction : input;
        capacitance : 1;
      }
      pin(SI) {
        direction : input;
        capacitance : 1;
      }
      pin(SE) {
        direction : input;
        capacitance : 2;
      }

      pin(Q) {
        direction : output;
        inverted_output : FALSE;

      }
      pin(QN) {
        direction : output;
```

```
        inverted_output : TRUE;
      }
      test_cell() {
        pin(D) {
          direction : input;
        }
        pin(C) {
          direction : input;
        }
        pin(SI) {
          direction : input;
          signal_type : "test_scan_in";
        }
        pin(SE) {
          direction : input;
          signal_type : "test_scan_enable";
        }

        ff ("IQ","IQN") {
          next_state : "D";
          clocked_on : "C";
        }

        pin(Q) {
          direction : output;
          function : "IQ";
          /*      signal_type : "test_scan_out"; */
        }
        pin(QN) {
          direction : output;
          function : "IQN";
          /*      signal_type : "test_scan_out_inverted";*/
        }
      }
    }
```

Examples

```
Error: Line 139, No test_scan_out/test_scan_out_inverted signal
        types exist on the 'libg148' test_cell cell. (LIBG-148)
```

LIBG-149

(error) The clocked_on_also function on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.

Description

The *clocked_on_also* function for this test_cell is not specified on the correct pin. This function needs to be specified on the clock of the slave stage of a master-slave configuration.

Feedback

This warning informs you that the test_cell pointed to has the *clocked_on_also* function specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has correctly used the *clocked_on_also* function. To determine the correct function,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

LIBG-150

(error) The test_scan_clock_b signal type on the '%s' port for \n \ttest_cell on the '%s' cell is not specified on the correct pin.

Description

The test_scan_clock_b signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock of the slave stage of an LSSD configuration.

This warning informs you that the test_cell pointed to has the test_scan_clock_b signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has correctly specified the test_scan_clock_b signal type.

Examples

```
cell(libg150) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
```

Feedback

```
  capacitance : 1;
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(C3) {
  direction : input;
  capacitance : 1;
}
pin(MQ) {
  direction : internal;
  internal_node : "MQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 0.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
           ~R   -  - H  -  : H/L - :  -  H/L,\\\n
           ~R   -  - L  -  : -   - :  -  N,\\\n
            R   -  H -  -  : -   - :  X  X,\\\n
            R   -  - H  -  : -   - :  X  X,\\\n
           ~R   -  H - H/L : -   - : H/L -,\\\n
```

```
            ~R   -  L -  -  : -   - :  N  -";
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_b";
      }
      pin(D2) {
        direction : input;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

Examples

```
Error: Line 181, The test_scan_clock_b signal type on the 'C' port for
         test_cell on the 'libg150' cell is not specified on the correct
 pin.(LIBG-150)
```

LIBG-151

(error) The test_scan_in signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.

Feedback

Description

The *test_scan_in* signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that takes in the scan data. All scan types, and therefore, all test_cells need to have either the *test_scan_in* or *test_scan_in_inverted* signal type.

This warning informs you that the test_cell pointed to has the *test_scan_in* signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has correctly specified the test_scan_in signal type.

Examples

```
cell(libg151) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
    }
    pin(C3) {
      direction : input;
      capacitance : 1;
    }
    pin(MQ) {
      direction : internal;
      internal_node : "MQ";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C C2";
      }
```

Feedback

```
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
           ~R   -  - H  -  : H/L - :  -  H/L,\\\n
           ~R   -  - L  -  : -   - :  -  N,\\\n
            R   -  H -  -  : -   - :  X  X,\\\n
            R   -  - H  -  : -   - :  X  X,\\\n
           ~R   -  H - H/L : -   - : H/L -,\\\n
           ~R   -  L -  -  : -   - :  N  -";
}
test_cell() {
  pin(D) {
    direction : input;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_in";
  }
  pin(D2) {
    direction : input;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_clock_a";
  }
  pin(C3) {
    direction : input;
```

```
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case the pin 'C' is a clock and should not have a test_scan_in signal_type attribute. The test_scan_in should be on the pin 'D2'.

Examples

```
Error: Line 182, The test_scan_in signal type on the 'C' port for
        test_cell on the 'libg151' cell is not specified on the correct
 pin. (LIBG-151)
```

LIBG-152

(error) The test_scan_in_inverted signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.

Description

The test_scan_in_inverted signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin which takes in the scan data. All scan types, and all test_cells need to have either the test_scan_in or test_scan_in_inverted signal type.

This warning informs you that the test_cell pointed to has the test_scan_in_inverted signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools will not be able to use this cell.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_in_inverted* signal type.

Feedback

Examples

```
cell(libg152) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
    }
    pin(C3) {
      direction : input;
      capacitance : 1;
    }
    pin(MQ) {
      direction : internal;
      internal_node : "MQ";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C C2";
      }
    }
    pin(Q) {
      direction : output;
      internal_node : "SQ";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C C3";
      }
    }
    pin(QN) {
      direction : output;
      state_function : "(Q)'";
      timing() {
        timing_type : rising_edge;
```

Feedback

```
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
           ~R   -  - H  -  : H/L - :  -  H/L,\\\n
           ~R   -  - L  -  : -   - :  -  N,\\\n
            R   -  H -  -  : -   - :  X  X,\\\n
            R   -  - H  -  : -   - :  X  X,\\\n
           ~R   -  H - H/L : -   - : H/L -,\\\n
           ~R   -  L -  -  : -   - :  N  -";
}
test_cell() {
  pin(D) {
    direction : input;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_in_inverted";
  }
  pin(D2) {
    direction : input;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_clock_a";
  }
  pin(C3) {
    direction : input;
    capacitance : 1;
    signal_type : "test_scan_clock_b";
  }
  ff ("IQ","IQN") {
    next_state : "D";
    clocked_on : "C";
  }
  pin(Q) {
    direction : output;
    function : "IQ";
    signal_type : "test_scan_out";
  }
  pin(QN) {
    direction : output;
    function : "IQN";
    signal_type : "test_scan_out_inverted";
  }
```

Feedback

```
    }
  }
```

In this case the pin 'C' is a clock and should not have a test_scan_in_inverted signal_type attribute. The test_scan_in_inverted should be on the pin 'D2'.

Examples

```
Error: Line 181, The test_scan_in_inverted signal type on the 'C' port
 for
       test_cell on the 'libg152' cell is not specified on the correct
 pin. (LIBG-152)
```

LIBG-153

(error) The test_scan_enable signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.

Description

The test_scan_enable signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that switches the input mode of the cell between test and mission mode. Only, a multiplexed flip-flop requires this signal type. This signal type can also be used in clocked scan cells.

This warning informs you that the test_cell pointed to has the test_scan_enable signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_enable* signal type.

Examples

```
cell(libg153) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
      capacitance : 1;
    }
```

Feedback

```
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(C3) {
  direction : input;
  capacitance : 1;
}
pin(MQ) {
  direction : internal;
  internal_node : "MQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
           ~R   -  - H  -  : H/L - :  -  H/L,\\\n
           ~R   -  - L  -  : -   - :  -  N,\\\n
            R   -  H -  -  : -   - :  X  X,\\\n
            R   -  - H  -  : -   - :  X  X,\\\n
           ~R   -  H - H/L : -   - : H/L -,\\\n
           ~R   -  L -  -  : -   - :  N  -";
}
```

Feedback

```
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_enable";
      }
      pin(D2) {
        direction : input;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

The pin 'C' is a clock and should not have a test_scan_enable signal_type attribute. The test_scan_enable should be on the pin 'D2'.

Examples

```
Error: Line 181, The test_scan_enable signal type on the 'C' port for
        test_cell on the 'libg153' cell is not specified on the correct
 pin. (LIBG-153)
```

Feedback

LIBG-154

(error) The test_scan_enable_inverted signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.

Description

The test_scan_enable_inverted signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the pin that switches the input mode of the cell between test and mission mode. Only a multiplexed flip-flop requires this signal type. This signal type can also be used in clocked scan cells.

This warning informs you that the test_cell pointed to has the test_scan_enable_inverted signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_enable_inverted* signal type.

Examples

```
cell(libg154) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
    }
    pin(C3) {
      direction : input;
      capacitance : 1;
    }
    pin(MQ) {
      direction : internal;
      internal_node : "MQ";
      timing() {
        timing_type : rising_edge;
```

Feedback

```
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
           ~R   -  - H  -  : H/L - :  -  H/L,\\\n
           ~R   -  - L  -  : -   - :  -  N,\\\n
            R   -  H -  -  : -   - :  X  X,\\\n
            R   -  - H  -  : -   - :  X  X,\\\n
           ~R   -  H - H/L : -   - : H/L -,\\\n
           ~R   -  L -  -  : -   - :  N  -";
}
test_cell() {
  pin(D) {
    direction : input;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_enable_inverted";
  }
  pin(D2) {
    direction : input;
  }
  pin(C2) {
```

Feedback

```
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

The pin 'C' is a clock and should not have a test_scan_enable_inverted signal_type attribute. The test_scan_enable_inverted should be on the pin 'D2.'

Examples

```
Error: Line 181, The test_scan_enable_inverted signal type on the 'C'
 port for
        test_cell on the  'libg154'cell is not specified on the correct
 pin. (LIBG-154)
```

LIBG-155

(error) The test_scan_clock signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.

Description

The test_scan_clock signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the scan clock for clocked scan cells.

This warning informs you that the test_cell pointed to has the test_scan_clock signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

Feedback

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_clock* signal type.

Examples

```
cell(libg155) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
    }
    pin(C3) {
      direction : input;
      capacitance : 1;
    }
    pin(MQ) {
      direction : internal;
      internal_node : "MQ";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C C2";
      }
    }
    pin(Q) {
      direction : output;
      internal_node : "SQ";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
        fall_resistance : 0.1;
        related_pin : "C C3";
      }
    }
```

Feedback

```
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
           ~R   -  - H  -  : H/L - :  -  H/L,\\\n
           ~R   -  - L  -  : -   - :  -  N,\\\n
            R   -  H -  -  : -   - :  X  X,\\\n
            R   -  - H  -  : -   - :  X  X,\\\n
           ~R   -  H - H/L : -   - : H/L -,\\\n
           ~R   -  L -  -  : -   - :  N  -";
}
test_cell() {
  pin(D) {
    direction : input;
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    signal_type : "test_scan_in";

  }
  pin(C2) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_clock_a";
  }
  pin(C3) {
    direction : input;
    capacitance : 1;
    signal_type : "test_scan_clock";
  }
  ff ("IQ","IQN") {
    next_state : "D";
    clocked_on : "C";
  }
  pin(Q) {
    direction : output;
    function : "IQ";
    signal_type : "test_scan_out";
  }
```

Feedback

```
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
}
```

The pin 'C3' is not a clock and should not have a test_scan_clock signal_type attribute.

Examples

```
Error: Line 195, The test_scan_clock signal type on the 'C3' port for
        test_cell on the 'libg155' cell is not specified on the correct
 pin. (LIBG-155)
```

LIBG-156

(error) The test_scan_clock_a signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified on the correct pin.

Description

The test_scan_clock_a signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock of the master stage of an LSSD configuration.

This warning informs you that the test_cell pointed to has the test_scan_clock_a signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_scan_clock_a* signal type.

Examples

```
cell(libg156) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
```

Feedback

```
  direction : input;
  capacitance : 1;
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(C3) {
  direction : input;
  capacitance : 1;
}
pin(MQ) {
  direction : internal;
  internal_node : "MQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C2";
  }
}
pin(Q) {
  direction : output;
  internal_node : "SQ";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
pin(QN) {
  direction : output;
  state_function : "(Q)'";
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "C C3";
  }
}
statetable("C D C2 C3 D2", "MQ SQ") {
  table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
           ~R   -  - H  -  : H/L - :  -  H/L,\\\n
           ~R   -  - L  -  : -   - :  -  N,\\\n
            R   -  H -  -  : -   - :  X  X,\\\n
            R   -  - H  -  : -   - :  X  X,\\\n
```

Feedback

```
                ~R   -  H - H/L : -   - : H/L -,\\\n
                ~R   -  L -  -  : -   - :  N  -";
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_clock_a";
      }
      pin(D2) {
        direction : input;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_in";
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

The pin 'C' is a clock and should not have a test_scan_clock_a signal_type attribute.

Examples

```
Error: Line 214, The test_scan_clock_a signal type on the 'C' port for
        test_cell on the 'libg156' cell is not specified on the correct
 pin. (LIBG-156)
```

Feedback

LIBG-157

(error) The test_clock signal type on the '%s' port for\n \ttest_cell on the '%s' cell is not specified correctly.

Description

The test_clock signal type for this test_cell is not specified on the correct pin. This signal type needs to be specified on the clock used for ATPG capture in auxiliary clock lssd cells.

This warning informs you that the test_cell pointed to has the test_clock signal type specified on an incorrect pin. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has correctly specified the *test_clock* signal type.

Examples

```
cell(libg157) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
    }
    pin(D2) {
      direction : input;
      capacitance : 1;
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
    }
    pin(C3) {
      direction : input;
      capacitance : 1;
    }
    pin(MQ) {
      direction : internal;
      internal_node : "MQ";
      timing() {
        timing_type : rising_edge;
        intrinsic_rise : 1.0;
        intrinsic_fall : 1.0;
        rise_resistance : 0.1;
```

Feedback

```
      fall_resistance : 0.1;
      related_pin : "C C2";
    }
  }
  pin(Q) {
    direction : output;
    internal_node : "SQ";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C3";
    }
  }
  pin(QN) {
    direction : output;
    state_function : "(Q)'";
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C C3";
    }
  }
  statetable("C D C2 C3 D2", "MQ SQ") {
    table :  "R  H/L L L  -  : -   - : H/L H/L,\\\n
             ~R   -  - H  -  : H/L - :  -  H/L,\\\n
             ~R   -  - L  -  : -   - :  -  N,\\\n
              R   -  H -  -  : -   - :  X  X,\\\n
              R   -  - H  -  : -   - :  X  X,\\\n
             ~R   -  H - H/L : -   - : H/L -,\\\n
             ~R   -  L -  -  : -   - :  N  -";
  }
  test_cell() {
    pin(D) {
      direction : input;
    }
    pin(C) {
      direction : input;
      capacitance : 2;
      signal_type : "test_scan_clock_a";
    }
    pin(D2) {
      direction : input;
    }
    pin(C2) {
      direction : input;
      capacitance : 2;
      signal_type : "test_clock";
```

Feedback

```
      }
      pin(C3) {
        direction : input;
        capacitance : 1;
        signal_type : "test_scan_clock_b";
      }
      ff ("IQ","IQN") {
        next_state : "D";
        clocked_on : "C";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

The pin 'C2' is not a clock and should not have a test_clock signal_type attribute.

Examples

```
Error: Line 233, The test_clock signal type on the 'C2' port for
        test_cell on the 'libg157' cell is not specified correctly.
 (LIBG-157)
```

LIBG-158

(error) Invalid nontest mode for test_cell on the '%s' cell.\n \tThere are more than 2 sequential elements.

Description

The nontest mode for test_cells must be one of the following:

```
- A single flip-flop
        - A single latch
        - A single master-slave latch configuration using clocked_on and
                clocked_on_also
```

This warning informs you that the nontest mode of the test cell has more than 2 distinct sequential elements. Thus, it does not fit the previous requirements. The test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

Feedback

What Next

Check the library description to ensure that each test_cell has properly specified the correct nontest mode. To determine the multiple sequential elements in this description,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

LIBG-159

(error) Invalid nontest mode for test_cell on the '%s' cell. \n \tThis describes a ganged cell.

Description

The nontest mode for test_cells must be one of the following:

```
- A single flip-flop
        - A single latch
        - A single master-slave latch configuration using clocked_on and
                clocked_on_also
```

This warning informs you that the nontest mode of the test cell is a ganged cell. Thus, it does not fit the previous requirements. The test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell does not specify a ganged cell as its nontest mode. Ganged cells can be recognized by the keywords ff_bank or latch_bank.

LIBG-160

(error) The nontest mode for test_cell on the '%s' cell is invalid.\n \tThe '%s' slave port does not directly feed the output.

Description

The nontest mode for test_cells must be one of the following:

```
- A single flip-flop
        - A single latch
```

```
        - A single master-slave latch configuration using clocked_on,
              clocked_on_also
```

This warning informs you that in nontest mode of the test cell, the slave does not directly feed the output. This means that this is not a master-slave latch configuration that DFT Compiler supports. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

What Next

Check the library description to ensure that the nontest mode of the test_cell is correctly specified. If you are using a master-slave as the non test mode, the only accepted description is the state description using

```
clocked_on : <master clock>
        clocked_on_also : <slave clock>
```

Examples

```
cell(libg160) {
      area : 10;
      bundle (D) {
        members(D1, D2);
        direction : input;
        capacitance : 1;
      }
      pin(G) {
        direction : input;
        capacitance : 1;
      }
      latch_bank ("IQ","IQN", 2) {
        data_in : "D";
        enable : "G";
      }
      bundle (Q) {
        members(Q1, Q2);
        direction : output;
        function : "IQ";
        timing() {
          timing_sense : positive_unate;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "D";
        }
        timing() {
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "G";
```

```
        }
      }
      test_cell() {
        pin(D1) {
          direction : input;
        }
        pin(G) {
          direction : input;
        }
        pin(D2) {
          direction : input;
          signal_type : "test_scan_in";
        }
        pin(Q1 Q2 ) {
          direction : output;
          function : "G D2 D1";
          signal_type : "test_scan_out";
        }
      }
    }
```

Examples

```
Error: Line 193, The nontest mode for test_cell on the 'libg160' cell is
 invalid.
        The 'Q1' slave port does not directly feed the output. (LIBG-160)
```

LIBG-161

(error) The nontest mode for test_cell on the '%s' cell is invalid\n \tThe '%s' state pin is not a latch for a master-slave configuration.

Description

The nontest mode for test_cells must be one of the following:

```
- A single flip-flop
        - A single latch
        - A single master-slave latch configuration using clocked_on and
                clocked_on_also
```

This warning informs you that the nontest mode of the test cell is an incorrect master-slave description. This stage of the master-slave configuration is not a latch, thus, it does not fit the previous requirements. The test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that the nontest mode of the test_cell is correctly specified. If you are using a master-slave as the nontest mode, the only accepted description is the state description using

Feedback

```
clocked_on : <master clock>
        clocked_on_also : <slave clock>
```

Examples

```
cell(libg161) {
      area : 11;
      pin(D1 D2 D3) {
        direction : input;
        capacitance : 1;
      }
      pin(CP) {
        direction : input;
        capacitance : 2;
      }
      pin(SCK1 SCK2) {
        direction : input;
        capacitance : 2;
      }
      pin(SI) {
        direction : input;
        capacitance : 1;
        timing() {
          timing_type : setup_falling;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          related_pin : "SCK2";
        }
        timing() {
          timing_type : hold_falling;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          related_pin : "SCK2";
        }
      }
      pin(Q) {
        direction : output;
        timing() {
          timing_type : rising_edge;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "CP SCK1";
        }
      }
      pin(Q2) {
        direction : output;
        timing() {
          timing_type : rising_edge;
          intrinsic_rise : 1.0;
          intrinsic_fall : 1.0;
          rise_resistance : 0.1;
```

Feedback

```
      fall_resistance : 0.1;
      related_pin : "CP SCK1";
    }
  }
  pin(Q3) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CP SCK1";
    }
  }
  test_cell() {
    pin(D1) {
      direction : input;
    }
    pin(D2) {
      direction : input;
    }
    pin(D3) {
      direction : input;
    }
    pin(CP) {
      direction : input;
    }
    pin(SCK1) {
      direction : input;
      signal_type : "test_scan_clock_b";
    }
    pin(SCK2) {
      direction : input;
      signal_type : "test_scan_clock_a";
    }
    pin(SI) {
      direction : input;
      signal_type : "test_scan_in";
    }
    statetable("C D ", "Q") {
      table :  "R  H/L : - : H/L,\\\n
               ~R   -  : - :  N";
    }
    pin(Q) {
      direction : output;
      internal_node : "Q";
      input_map : "CP D1";
      signal_type : "test_scan_out";
    }
    pin(Q2) {
      direction : output;
      internal_node : "Q";
```

```
          input_map : "CP D2";
          signal_type : "test_scan_out";
        }
        pin(Q3) {
          direction : output;
          internal_node : "Q";
          input_map : "CP D3";
          signal_type : "test_scan_out";
        }
      }
    }
```

Examples

```
Error: Line 218, The nontest mode for test_cell on the 'libg161' cell is
 invalid.
        The 'Q2' state pin is not a latch for a master-slave
 configuration. (LIBG-161)
```

LIBG-162

(error) The test_cell on the '%s' cell cannot have more than one\n \ttest_scan_in or test_scan_in_inverted signal type. This happens on the \n \t'%s' port.

Description

Each test_cell must have only one test_scan_in or test_scan_in_inverted signal type. This signal type is specified on the pin that is used to take scan data into the cell.

This warning informs you that the test_cell pointed to has multiple test_scan_in or test_scan_in_inverted signal types. The message points to the second port that has this signal type. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has only one test_scan_in or test_scan_in_inverted signal type.

Examples

```
cell(libg162) {
      area : 2;
      pin_opposite ( "Q", "NQ" );
      latch ( "QX" , "QY" ) {
        data_in   : " ((D*!SE) + (SI*SE)) ";
        enable  : " CK  ";
      }
      pin (D)    {
        direction : input;
        capacitance : 1;
```

Feedback

```
    }
    pin (SI, SIN, SE) {
      direction : input;
      capacitance : 1;
    }
    pin (CK)    {
      direction : input    ;
      capacitance :   2 ;
    }
    pin (Q)    {
      direction : output   ;
      function  : "QX" ;
    }
    pin (NQ)    {
      direction : output   ;
      function  : "QY" ;
    }
    test_cell() {
      latch ( "QX", "QY") {
        data_in : " D ";
        enable : " CK' ";
      }
      pin (D,CK) {
        direction : input;
      }
      pin (SI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin (SIN) {
        direction : input ;
        signal_type : "test_scan_in_inverted";
      }
      pin (SE) {
        direction : input ;
        signal_type : "test_scan_enable";
      }
      pin (Q) {
        direction : output ;
        function : " QX ";
        signal_type : "test_scan_out";
      }
      pin (NQ) {
        direction : output ;
        function : " QY ";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

Feedback

Examples

```
Error: The test_cell on the 'libg162' cell cannot have more than one
        test_scan_in or test_scan_in_inverted signal type. This happens
 on
        the 'SIN' port. (LIBG-162)
```

LIBG-163

(error) The '%s' port in test_cell on the '%s' cell has a\n \ttest_scan_out signal type on an inverted output.

Description

The test_scan_out signal type can only be specified on a noninverted output. If the output is inverted, the proper signal type is test_scan_out_inverted. This signal type specifies the polarity of the port with respect to the state.

This warning informs you that the test_cell pointed to has the test_scan_out signal type specified on an inverted output. Thus, the test_cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

The default behavior of selecting the function over the signal_type to determine the inversion of the output is correct in most cases.

Check the library description to ensure that the test_scan_out signal type is only placed on noninverted outputs. To determine if this is an inverted or noninverted output

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

Examples

```
cell(libg163) {
    area : 13;
    pin(D) {
      direction : input;
      capacitance : 1;
      timing() {
        timing_type : setup_falling;
        intrinsic_rise : 1.0;
```

Feedback

```
      intrinsic_fall : 1.0;
      related_pin : "C";
    }
    timing() {
      timing_type : hold_falling;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "C";
    }
  }
  pin(C) {
    direction : input;
    capacitance : 2;
  }
  pin(SDI) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "C";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.0;
      intrinsic_fall : 0.0;
      related_pin : "C";
    }
  }
  pin(SE) {
    direction : input;
    capacitance : 2;
  }
  pin(TQ) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C";
    }
  }
  pin(SDO) {
    direction : output;
    timing() {
      timing_type : falling_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
```

```
        related_pin : "C";
      }
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(C) {
        direction : input;
      }
      pin(SDI) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(SE) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_enable";
      }

      statetable("C D SDI", "Q") {
        table : "H L/H H/L : - : L/H,\\\n
                 L -  -  : - : N";
      }

      pin(TQ) {
        direction : output;
        internal_node : "Q";
      }
      pin(SDO) {
        state_function : "TQ";
        direction : output;
        signal_type : "test_scan_out";
      }
    }
  }
```

Examples

```
Error: Line 176, The 'SDO' port in test_cell on the 'libg163' cell has a
        test_scan_out signal type on an inverted output. (LIBG-163)
```

LIBG-164

(error) The '%s' port in test_cell on the '%s' cell has a\n \ttest_scan_out_inverted signal type on a noninverted output.

Feedback

Description

The test_scan_out_inverted signal type can only be specified on an inverted output. If the output is noninverted, the proper signal type is test_scan_out. This signal type specifies the polarity of the port with respect to the state.

This error informs you that the test_cell pointed to has the test_scan_out_inverted signal type specified on a noninverted output. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that the test_scan_out_inverted signal type is only placed on inverted outputs.

To determine if this is an inverted or noninverted output

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, an inverted output is a state only if it has N. Instead the output contains an inversion of the state pin.

Examples

```
cell(libg164) {
            area : 11;
            pin(D0) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_rising;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "CK1";
              }
              timing() {
                timing_type : hold_rising;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "CK1";
              }
            }

            pin(TI) {
              direction : input;
              capacitance : 1;
```

Feedback

```
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
  }

  pin(TE) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "CK1";
    }
  }

  pin(CK1) {
    direction : input;
    capacitance : 1;
  }
  pin(Q) {
    direction : output;
    inverted_output : FALSE;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CK1";
    }
  }

  pin(QN) {
    direction : output;
    inverted_output : TRUE;
    timing() {
      timing_type : rising_edge;
```

Feedback

```
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CK1";
    }
  }

  test_cell() {
    pin(D0) {
      direction : input;
    }
    pin(TE) {
      direction : input;
      signal_type : "test_scan_enable";
    }
    pin(TI) {
      direction : input;
      signal_type : "test_scan_in";
    }
    pin(CK1) {
      direction : input;
      capacitance : 1;
    }

    statetable("D0 CK1", "Q") {
      table : "L/H F : - : L/H,\\\n
               -  ~F : - : N";
    }

    pin(Q) {
      direction : output;
      inverted_output : FALSE;
      internal_node : "Q";
      signal_type : "test_scan_out";
    }

    pin(QN) {
      direction : output;
      inverted_output : TRUE;
      state_function : "Q";
      signal_type : "test_scan_out_inverted";
    }
    }
  }
```

Examples

```
Error: Line 220, The 'QN' port in test_cell on the 'libg164' cell has a
       test_scan_out_inverted signal type on a noninverted output.
 (LIBG-164)
```

Feedback

LIBG-165

(error) The test cell on the '%s' cell cannot have more than one\n \ttest_scan_enable or test_scan_enable_inverted signal type.\n \tThis happens on the '%s' port.

Description

Each test_cell must have only one test_scan_enable or test_scan_enable_inverted signal type. This signal type is specified on the pin that is used to select between scan and mission mode operation of the cell. Using the state table format, Library Compiler expects a single test_scan_enable or test_scan_enable_inverted signal type. Otherwise, Library Compiler generates a black box cell.

This warning informs you that the test_cell pointed to has multiple test_scan_enable or test_scan_enable_inverted signal types. The message points to the second port that has this signal type. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that each test_cell has only one test_scan_enable or test_scan_enable_inverted signal type. Otherwise, provide a full functional description of the non test_cell cell to bypass the multuple scan enable check.

Examples

```
cell(libg165) {
      area : 13;
      pin(D) {
        direction : input;
        capacitance : 1;
      }
      pin(G) {
        direction : input;
        capacitance : 2;
      }
      pin(D2) {
        direction : input;
        capacitance : 1;
      }
      pin(C2) {
        direction : input;
        capacitance : 2;
      }
      pin(SE) {
        direction : input;
        capacitance : 2;
      }
      pin(SEB) {
        direction : input;
        capacitance : 2;
```

Feedback

```
}
pin(Q) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "G C2";
  }
}
pin(QN) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "G C2";
  }
}
test_cell() {
  pin(D) {
    direction : input;
  }
  pin(G) {
    direction : input;
  }
  pin(D2) {
    direction : input;
    signal_type : "test_scan_in";
  }
  pin(C2) {
    direction : input;
    signal_type : "test_scan_clock";
  }
  pin(SE) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_enable";
  }
  pin(SEB) {
    direction : input;
    capacitance : 2;
    signal_type : "test_scan_enable_inverted";
  }
  state ("IQ","IQN") {
    force_01 : "G D'";
    force_10 : "G D";
  }
  pin(Q) {
```

```
          direction : output;
          function : "IQ";
          signal_type : "test_scan_out";
        }
        pin(QN) {
          direction : output;
          function : "IQN";
          signal_type : "test_scan_out_inverted";
        }
      }
    }
```

Examples

```
Error: The test cell on the 'libg165' cell cannot have more than one
        test_scan_enable or test_scan_enable_inverted signal type.
        This happens on the 'SEB' port. (LIBG-165)
```

LIBG-166

(error) The '%s' test_scan_clock port in test_cell on the '%s' cell\n \tdoes not have an active sense.

Description

The test_scan_clock must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock is the scan clock in the clocked scan type.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell are recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell

```
* Create a cell with the non test mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

LIBG-167

(error) The '%s' test_scan_clock_a port in test_cell on the '%s' cell\n \tdoes not have an active sense.

Feedback

Description

The test_scan_clock_a must have an active sense in the full cell description. The Library Compiler determines the active sense by checking the function of the full cell. The test_scan_clock_a is the scan clock for the master stage of the LSSD scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell are recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

LIBG-168

(error) The '%s' test_scan_clock_b port in test_cell on the '%s' cell\n \tdoes not have an active sense.

Description

The test_scan_clock_b must have an active sense in the full cell description. The active sense is determined by Library Compiler by checking the function of the full cell. The test_scan_clock_b is the scan clock for the slave stage of the LSSD scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell are recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

Feedback

LIBG-169

(error) The '%s' test_clock port in test_cell on the '%s' cell does \n \tnot have an active sense.

Description

The test_clock must have an active sense in the full cell description. Library Compiler determines the active sense by checking the function of the full cell. The test_clock is the capture clock used by ATPG in the auxiliary clocked lssd scan style.

Because the test_cell and the full cell have a discrepancy, neither the test cell nor the full cell are recognized. Both the test_cell and the entire cell are converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that the functional descriptions in the test_cell and full cell are correct and that the timing arcs are consistent. To report on the active sense and functions of the full cell

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

LIBG-170

(error) The '%s' port in test_cell for the '%s' cell has an invalid\n \tsignal type %s.

Description

The valid signal_types in test_cells are

```
- test_scan_in
        - test_scan_in_inverted
        - test_scan_enable
        - test_scan_enable_inverted
        - test_scan_out
        - test_scan_out_inverted
        - test_scan_clock
        - test_scan_clock_a
        - test_scan_clock_b
        - test_clock
```

This warning informs you that the port in the test_cell pointed to has a signal_type other than the ones listed previously. Thus, the test_cell is not valid, and the entire cell is converted to a black box.

Feedback

What Next

Check the test_cell pointed to and change the invalid signal_type.

LIBG-171

(error) The LSSD test_cell for the '%s' cell has neither\n \ta test_scan_clock_b signal type nor a master-slave as its nontest mode.

Description

LSSD scan styles must have the following test_cell characteristics:

```
clocked lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b
        - nontest mode: flip_flop
   auxiliary clock lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b,
                test_clock
        - nontest mode : flip_flop
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b
        - nontest mode: latch
   single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_out/
                test_scan_out_inverted, test_scan_clock_a,
                test_scan_clock_b (optional)
        - nontest mode: master-slave (clocked_on & clocked_on_also)
```

This error informs you that this cell is an lssd scan style because it has test_scan_in/ test_scan_in_inverted, test_scan_out/test_scan_out_inverted, and test_scan_clock_a signal types. However, it is invalid because it has neither a test_scan_clock_b signal type nor a master-slave as its nontest mode. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

Feedback

What Next

Check the library description to ensure that each test_cell has correctly specified the nontest modes and signal types in the test_cell pointed to. If you do not understand why the nontest function is not one of the previous types,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

Examples

```
cell(libg171) {
      area : 21;
             pin(D1) {
               direction : input;
               capacitance : 1;
             }
             pin(C1) {
               direction : input;
               capacitance : 2;
             }
             pin(D2) {
               direction : input;
               capacitance : 1;
             }
             pin(C2) {
               direction : input;
               capacitance : 2;
             }
             pin(C3) {
               direction : input;
             capacitance : 1;
             }

             pin(Q1) {
               direction : output;
               timing() {
               timing_type : rising_edge;
                 intrinsic_rise : 1.0;
                 intrinsic_fall : 0.0;
                 rise_resistance : 0.1;
                 fall_resistance : 0.1;
                 related_pin : "C1";
               }
               timing() {
                 timing_type : rising_edge;
```

```
      intrinsic_rise : 1.0;
      intrinsic_fall : 0.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C2";
    }
  }
  pin(Q2) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "C3";
    }
  }
  test_cell() {
    pin(D1) {
      direction : input;
    }
    pin(C1) {
      direction : input;
    }
    pin(D2) {
      direction : input;
      signal_type : "test_scan_in";
    }
    pin(C2) {
      direction : input;
      signal_type : "test_scan_clock_a";
  }
    pin(C3) {
      direction : input;
      signal_type : "test_scan_clock_b";
    }
    state("IQ","IQN") {
      force_10 : "C1 D1";
      force_01 : "C1 D1'";
    }
    pin(Q1) {
      direction : output;
    function : "IQ";
    }
    pin(Q2) {
      direction : output;
      signal_type : "test_scan_out";
    }
  }
  test_cell() {
    pin(D1) {
      direction : input;
```

Feedback

```
        }
        pin(C1) {
          direction : input;
      }
        pin(D2) {
          direction : input;
          signal_type : "test_scan_in";
        }
        pin(C2) {
          direction : input;
          signal_type : "test_scan_clock_a";
      }
        pin(C3) {
          direction : input;
        }
        state("IQ","IQN") {
          force_10 : "C1 C3' D1";
          force_01 : "C1 C3' D1'";
        }
        pin(Q1) {
          direction : output;
      }
        pin(Q2) {
          direction : output;
          function : "IQ";
          signal_type : "test_scan_out";
        }
      }
    }
```

Examples

```
Error: Line 229, The LSSD test_cell for the 'libg171' cell has neither
        a test_scan_clock_b signal type nor a master-slave as its nontest
 mode. (LIBG-171)
```

LIBG-172

(error) The test_cell for the '%s' cell is not valid because\n \tit has missing or extra test signals.

Description

The supported scan styles must have the following test_cell characteristics:

```
multiplexed flip-flop
        - signal types : test_scan_in/test_scan_in_inverted,
 test_scan_enable/
                test_scan_enable_inverted,
 test_scan_out/test_scan_out_inverted
        - nontest mode : flip-flop, master-slave latch pair, or latch
   clocked scan
```

```
        - signal types : test_scan_in/test_scan_in_inverted,
test_scan_enable/
                 test_scan_enable_inverted (optional), test_scan_clock,
                 test_scan_out/test_scan_out_inverted
        - nontest modes : flip-flop or latch
  clocked lssd
        - signal types : test_scan_in/test_scan_in_inverted,
test_scan_out/
                 test_scan_out_inverted, test_scan_clock_a,
test_scan_clock_b
        - nontest mode: flip-flop
  auxiliary clock lssd
        - signal types : test_scan_in/test_scan_in_inverted,
test_scan_out/
                 test_scan_out_inverted, test_scan_clock_a,
test_scan_clock_b,
                 test_clock
        - nontest mode : flip-flop
  single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted,
test_scan_out/
                 test_scan_out_inverted, test_scan_clock_a,
test_scan_clock_b
        - nontest mode: latch
  single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted,
test_scan_out/
                 test_scan_out_inverted, test_scan_clock_a,
test_scan_clock_b
        - nontest mode: latch
  single-latch lssd
        - signal types : test_scan_in/test_scan_in_inverted,
test_scan_out/
                 test_scan_out_inverted, test_scan_clock_a,
                 test_scan_clock_b (optional)
        - nontest mode: master-slave (clocked_on & clocked_on_also)
```

This warning informs you that the other signal types do not correspond to one of the previously supported scan styles. Extra or missing signal types point to the fact that the test_cell is not valid, and the entire cell is a black box.

What Next

Check the library description to ensure that each test_cell has correctly specified the nontest modes and signal types in the test_cell pointed to. If you do not understand why the nontest function is not one of the previous types,

```
* Create a cell with the nontest mode as the functional part
    of the cell.
  * Compile this cell.
  * Issue the following command:
```

Feedback

```
report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

Examples

```
cell(libg172) {
      area : 13;
      pin(D) {
        direction : input;
        capacitance : 1;
      }
      pin(C) {
        direction : input;
        capacitance : 2;
      }
      pin(SDI) {
        direction : input;
        capacitance : 1;
      }
      pin(SDOB) {
        direction : output;
      }
      test_cell() {
        pin(D) {
          direction : input;
        }
        pin(C) {
          direction : input;
        }
        pin(SDI) {
          direction : input;
          signal_type : "test_scan_in";
        }
        statetable("D C", "QN") {
          table : "L/H H : - : H/L,\
                  -   L : - : N";
        }

        pin(SDOB) {
          direction : output;
          inverted_output : TRUE;
          internal_node : "QN";
          signal_type : "test_scan_out_inverted";
        }
      }
    }
  }
```

Feedback

Examples

```
Error: Line 160, The test_cell for the 'libg172' cell is not valid
 because
        it has missing or extra test signals. (LIBG-172)
```

LIBG-173

(error) Cannot derive full function based on test_cell\n \ton the '%s' cell due to previous warnings or errors.

Description

Library Compiler generates a functional description of the entire cell based on the information in the test_cell. However, if there are warnings or errors in the test_cell, a functional description of the entire cell cannot be generated.

This error informs you that the test_cell pointed to has previous errors or warnings. Thus, the test_cell is not valid, and the entire cell is a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Fix the previous problems in order to recognize both the test_cell and full cell functionality. You might have to add a state table description of the entire cell.

Examples

```
cell(libg173) {
            area : 11;
            pin(D0) {
              direction : input;
              capacitance : 1;
              timing() {
                timing_type : setup_rising;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "CK1";
              }
              timing() {
                timing_type : hold_rising;
                intrinsic_rise : 1.0;
                intrinsic_fall : 1.0;
                related_pin : "CK1";
              }
            }

            pin(TI) {
              direction : input;
              capacitance : 1;
              timing() {
```

Feedback

```
    timing_type : setup_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
}

pin(TE) {
  direction : input;
  capacitance : 1;
  timing() {
    timing_type : setup_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
  timing() {
    timing_type : hold_rising;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    related_pin : "CK1";
  }
}

pin(CK1) {
  direction : input;
  capacitance : 1;
}
pin(Q) {
  direction : output;
  inverted_output : FALSE;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "CK1";
  }
}

pin(QN) {
  direction : output;
  inverted_output : TRUE;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
```

Feedback

```
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CK1";
    }
  }

  test_cell() {
    pin(D0) {
      direction : input;
    }
    pin(TE) {
      direction : input;
      signal_type : "test_scan_enable";
    }
    pin(TI) {
      direction : input;
      signal_type : "test_scan_in";
    }
    pin(CK1) {
      direction : input;
      capacitance : 1;
    }

    statetable("D0 CK1", "Q") {
      table : "L/H F : - : L/H,\\\n
               -  ~F : - : N";
    }

    pin(Q) {
      direction : output;
      inverted_output : FALSE;
      internal_node : "Q";
      signal_type : "test_scan_out";
    }

    pin(QN) {
      direction : output;
      inverted_output : TRUE;
      state_function : "Q";
      signal_type : "test_scan_out_inverted";
    }
    }
  }
```

In this case, the test_cell pointed to has the test_scan_out_inverted signal type specified on a noninverted output 'QN' (LIBG-164). Thus, the test_cell is not valid, and the entire cell is converted to a black box.

Feedback

Examples

```
Error: Line 189, Cannot derive full function based on test_cell
        on the 'libg173' cell due to previous warnings or errors.
 (LIBG-173)
```

LIBG-174

(error) The '%s' clocked test cell is not valid\n \tbecause it has a master-slave configuration as its nontest mode.

Description

A clocked test_cell has the following characteristics:

```
- signal types : test_scan_in/test_scan_in_inverted, test_scan_enable/
                 test_scan_enable_inverted (optional), test_scan_clock,
                 test_scan_out/test_scan_out_inverted
        - nontest modes : flip-flop or latch
```

This warning informs you that the signal types point to this cell as being a clocked scan test_cell, but it does not have a flip-flop or latch as its nontest mode; it is currently specified as a master-slave cell. Thus, the test cell is not valid, and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that nontest modes and signal types are correctly pointed to by the test_cell. To determine why the nontest function is not one of the previous types,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

Examples

```
cell(libg174) {
    area : 10;
    pin(D) {
      direction : input;
      capacitance : 1;
      timing() {
        timing_type : setup_falling;
```

Feedback

```
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "G";
    }
    timing() {
      timing_type : hold_falling;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "G";
    }
  }
  pin(G G2) {
    direction : input;
    capacitance : 1;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
    timing() {
      timing_type : setup_rising;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "C2";
    }
    timing() {
      timing_type : hold_rising;
      intrinsic_rise : 0.0;
      intrinsic_fall : 0.0;
      related_pin : "C2";
    }
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
  }
  pin(Q) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "G C2";
    }
  }
  pin(QN) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
```

```
        fall_resistance : 0.1;
        related_pin : " G2 G C2";
      }
    }
    test_cell() {
      pin(D) {
        direction : input;
      }
      pin(G G2) {
        direction : input;
      }
      pin(D2) {
        direction : input;
        signal_type : "test_scan_in";
      }
      pin(C2) {
        direction : input;
        signal_type : "test_scan_clock";
      }
      latch ("IQ","IQN") {
        data_in : "D";
        enable : "G";
        enable_also : "G2";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, the cell is a master-slave with an unknown test cell type.

Examples

```
Error: Line 208, The 'libg174' clocked test cell is not valid
        because it has a master-slave configuration as its nontest mode.
 (LIBG-174)
fi
```

LIBG-175

(error) The test cell for the '%s' auxiliary clocked lssd cell is not \n \tvalid because its nontest mode is not a flip-flop.

Feedback

Description

An auxiliary clocked lssd test_cell has the following characteristics:

```
- signal types : test_scan_in/test_scan_in_inverted, test_scan_out/
                 test_scan_out_inverted, test_scan_clock_a,
 test_scan_clock_b,
                 test_clock
        - nontest mode : flip-flop
```

This warning informs you that the signal types point to this cell as being a auxiliary clocked lssd test_cell, but it does not have a flip-flop as its nontest mode. This makes the test_cell invalid and the entire cell is converted to a black box. There is functional information missing, and other tools cannot use this cell.

What Next

Check the library description to ensure that nontest modes and signal types are correctly pointed to by the test_cell. To determine why the nontest function is not one of the previous types,

```
* Create a cell with the nontest mode as the functional part
          of the cell.
        * Compile this cell.
        * Issue the following command:

             report_lib -table <library name> <cell name>
```

In the report_lib command's report, determine which pins correspond to states (pins with an N output) by looking at their functional description.

Examples

```
cell(libg103) {
      area : 12;
      pin(D) {
        direction : input;
        capacitance : 1;
      }
      pin(CK,IH, CK1) {
        direction : input;
        capacitance : 1;
      }
      pin(A,B) {
        direction : input;
        capacitance : 2;
      }
      pin(SI) {
        direction : input;
        capacitance : 1;
        timing() {
          timing_type : setup_falling;
```

Feedback

```
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "A";
    }
    timing() {
      timing_type : hold_falling;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      related_pin : "A";
    }
  }
  pin(Q) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "CK IH CK1";
    }
    timing() {
      timing_type : falling_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "B";
    }
  }
  pin(XQ) {
    direction : output;
  }
  test_cell(){
    pin(D,CK,CK1){
      direction : input;
    }
    pin(IH ){
      direction : input;
      signal_type : "test_clock";
    }
    pin(SI){
      direction : input;
      signal_type : "test_scan_in";
    }
    pin(A){
      direction : input;
      signal_type : "test_scan_clock_a";
    }
    pin(B){
      direction : input;
      signal_type : "test_scan_clock_b";
    }
```

Feedback

```
        ff("IQ","IQN"){
          clocked_on : "CK";
          next_state : "D";
          clocked_on_also : "CK1";
        }

        pin(Q){
          direction : output;
          function : "IQ";
          signal_type : "test_scan_out";
        }
        pin(XQ){
          direction : output;
          function : "IQN";
          signal_type : "test_scan_out_inverted";
        }
      }
    }
```

Examples

```
Error: Line 196, The test cell for the 'libg175' auxiliary clocked lssd
 cell is not
       valid because its nontest mode is not a flip-flop. (LIBG-175)
```

LIBG-176

(error) Neither the memory_read nor the memory write group\n \tis allowed on scalar ports.

Description

Either the memory_read group or the memory_write group is specified on a scalar port. These groups are only allowed on bus groups.

What Next

Remove the memory_read and memory_write group from all scalar ports.

LIBG-177

(error) The '%s' cell is a ROM, and ROMs cannot have any\n \tmemory_write groups.

Description

The cell is defined as a ROM type in the memory group. ROM cells cannot have any memory_write groups because the memory block cannot be written to.

What Next

Either change the memory type to a ram type or remove the memory_write group.

Feedback

Examples

```
cell(libg177) {
            ...
            memory() {
              type : rom;
              address_width : 10;
              word_width : 8;
            }
             ...
            bus (data_in) {
                bus_type   : "bus8"
                direction : input;
                capacitance : 1.46;
                fanout_load : 1.46;

                memory_write() {          /* Not allowed on ROM cells */
                  address : ram_addr;
                 enable : WR;
                }
            }
             ...
          }
```

Examples

```
Error: Line 22, The 'libg177' cell is a ROM, and ROMs cannot have any
        memory_write groups. (LIBG-177)
```

LIBG-178

(error) The '%s' cell is a RAM, and RAMs must have at\n \tleast one memory_read port and at least one memory_write port.

Description

The cell is defined as a RAM type in the cell memory group. RAM cells must have at least one memory_read port and at least one memory_write port.

What Next

You can implement either of the following suggestions:

```
(1) Change the memory type to rom and ensure only the memory_read
group is provided.
(2) If the model is for a RAM, make sure that both the memory_read and
memory_write groups are provided.
```

Examples

```
cell (libg178) {
```

Feedback

```
        area : 2300.0;
        memory() {
          type : ram;
          address_width : 10;
          word_width : 8;
        }

        bus (ram_addr) {
             bus_type  : "bus10"; /* defined in the library */
             direction : input;
             capacitance : 1.0;
       }
       bus (data_in) {
             bus_type   : "bus8";  /* defined in the library */
             direction : input;
             capacitance : 1.0;
             memory_write() {
               address : ram_addr;
               enable : WR;
             }
       }
       pin (WR) {
         direction : input;
         capacitance : 1.0;
         clock : true;
       }

       bus(data_out){
         bus_type  : "bus8";
         direction : output;

      }
  }
```

In this case, the memory_read group is missing in the cell. Add the following group to the port 'data_out' :

```
memory_read() {
          address : ram_addr;
        }
```

Examples

```
Error: Line 22, The 'libg178' cell is a RAM, and RAMs must have at
        least one memory_read port and at least one memory_write port.
 (LIBG-178)
```

LIBG-179

(error) The '%s' cell is a ROM, and ROMs must have at\n \tleast one memory_read group.

Feedback

Description

The cell is defined as a ROM type in the cell memory group. ROM cells require at least one memory_read port.

What Next

Add the memory_read group to the data port.

Examples

```
cell (libg179) {

      area : 2300.0;
      memory() {
        type : rom;
        address_width : 10;
        word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;
     }
     pin (WR) {
       direction : input;
       capacitance : 1.13;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : output;
    }
 }
```

In this case, the memory_read group is missing in the cell. Add the following group to the port 'data_out' :

```
memory_read() {
         address : ram_addr;
       }
```

Examples

```
Error: Line 22, The 'libg179' cell is a ROM, and ROMs must have at
        least one memory_read group. (LIBG-179)
```

Feedback

LIBG-180

(error) The '%s' bus has a %s group, but the '%s' cell\n \thas no memory group.

Description

The cell is missing a memory group. The bus has memory specific syntax, which is not allowed.

What Next

Either add the memory group to the cell or remove the memory_read/write groups from the ports.

Examples

```
cell (libg179) {

      area : 2300.0;
      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;
           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : output;

    }
 }
```

Examples

```
Error: Line 38, The 'data_in' bus has a memory_write group, but the
 'lib180' cell
        has no memory group. (LIBG-180)
```

Feedback

LIBG-181

(error) In the '%s' cell, the '%s' data bus has a width of %d,\n \tbut the memory group has a word width of %d.

Description

The size of the data bus does not match the size of the memory group specified in the cell memory group. They must be consistent.

What Next

Change the library to make the data bus width and the memory group word's width consistent.

Examples

```
cell (libg181) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 8;
        word_width : 6;
      }

      bus (ram_addr) {
           bus_type  : "bus8"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       memory_read() {
         address : ram_addr;
       }
```

```
    }
  }
```

In this case, the width of the bus data_out is 8 and the word width in the memory group is 6. Change either the bus_data's width to 6 or the memory group's word width to 8 to make them consistent.

Examples

```
Error: Line 54, In the 'libg181' cell, the 'data_out' data bus has a
 width of 8,
        but the memory group has a word width of 6. (LIBG-181)
```

LIBG-182

(error) The '%s' memory_write data bus can not be an output.

Description

The bus is an input to the memory block because it has the memory_write group specified. Inputs to the memory block can not be an output type.

What Next

The direction of the bus must be changed to either input, inout, or internal.

LIBG-183

(error) In the '%s' cell, the '%s' address bus is not defined.

Description

The address bus specified in the group is not defined in the cell.

What Next

The address specification must refer to a bus defined in the cell.

Examples

```
cell (libg183) {
      area : 2300.0;

      memory() {
        type : ram;
        address_width : 8;
        word_width : 8;
      }
     bus (data_in) {
           bus_type   : "bus8" /* defined in the library */
           direction : output;
```

Feedback

```
            capacitance : 1.0;
            memory_write() {
              address : ram_addr;
              enable : WR;
            }
      }
      pin (WR) {
        direction : input;
        capacitance : 1.0;
        clock : true;
      }
      bus(data_out){
        bus_type  : "bus8";
        direction : output;
        memory_read() {
          address : ram_addr;
        }
     }
  }
```

In this case, define the ram_addr as a port in the cell as follows:

bus (ram_addr) { bus_type : "bus8"; /* defined in the library */ direction : input; capacitance : 1.0; }

Examples

```
Error: Line 58, In the 'libg183' cell, the 'ram_addr' address bus is not
 defined. (LIBG-183)
```

LIBG-184

(error) In the '%s' cell, the '%s' address bus has a width of %d,\n \tbut the memory group has an address width of %d.

Description

The size of the address bus does not match the address size of the memory group specified in the cell memory group. They must be consistent.

What Next

Change the library to make the address bus width and the memory group address width consistent.

Examples

```
cell (libg184) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 10;
```

Feedback

```
        word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus8"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       memory_read() {
         address : ram_addr;
       }
    }
  }
```

In this case, the width of the bus data_out is 8 and the address width in the memory group is 10. Either change the width of the ram_addr to 10 or change the memory group's address width to 8 to make them consistent.

Examples

```
Error: Line 58, In the 'libg184' cell, the 'ram_addr' address bus has a
 width of 8,
        but the memory group has an address width of 10. (LIBG-184)
```

LIBG-185

(error) The '%s' memory address can not be an output.

Description

The address bus is an input to the memory block. Inputs to the memory block can not be an output type.

Feedback

What Next

The direction of the bus must be changed to either input, inout, or internal.

LIBG-186

(error) In the '%s' cell, the '%s' memory_read data bus\n \tcannot be an input.

Description

The data bus is an output of the memory block because it has the memory_read group specified.

What Next

Change the direction of the bus that has the memory_write group to either output, inout, or internal.

Examples

```
cell (libg186) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 8;
        word_width : 8;
      }
      bus (ram_addr) {
           bus_type  : "bus8"; /* defined in the library */
           direction : output;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;
           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.13;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : input; /* should be output */
       memory_read() {
         address : ram_addr;
       }
```

Feedback

```
    }
  }
```

Examples

```
Error: Line 54, In the 'libg186' cell, the 'data_out' memory_read data
 bus
        cannot be an input. (LIBG-186)
```

LIBG-187

(error) In the '%s' cell, The %s '%s' attribute is not\n \tthe name of a port or bus.

Description

The attribute specified in the group is not defined in the cell as either a port or a bus.

You cannot specify an expression here, only a port or a bus is valid. If you need to model an expression(logic), create a pin with a state_function attribute and use that internal pin.

What Next

Make sure the specification refers to a port or a bus defined in the cell.

Examples

```
cell (libg187) {
      area : 1380.0;
      interface_timing : TRUE;

      memory() {
        type : ram;
        address_width : 10;
        word_width : 8;
      }

      bus (RA) {
        bus_type  : "bus10";
        direction : input;
        capacitance : 1.0;
      }

      bus (DI) {
        bus_type   : "bus8";
        direction : input;
        capacitance : 1.0;

        memory_write() {
          address : RA;
          enable : "WRE";
        }
      }
```

Feedback

```
      pin (WE) {
        direction : input;
        capacitance : 1.0;
        clock : true;
      }

      pin (CE) {
        direction : input;
        capacitance : 1.0;
        clock : true;
      }

      bus(DO){
        bus_type  : "bus8";
        direction : output;
        capacitance : 1.0;

        memory_read() {
          address : RA;
        }
      }
    }
```

In this case, the port 'WRE' can be defined :

```
1. as an internal pin
        2. is state_function defines the writing occurence only when
           WE and CE are active.

      pin (WRE) {
        direction : internal;
        capacitance : 1.0;
        state_function : "!(WE' * CE')";
        clock : true;
      }
```

Examples

```
Error: Line 43, In the 'libg187' cell, the enable 'WRE' attribute is not
        the name of a port or bus. (LIBG-187)
```

LIBG-188

(error) In the '%s' cell, the %s '%s' bus has a width of %d,\n \tbut the memory group has a word width of %d.

Description

The size of the bus does not match the word size of the memory block specified in the cell memory group. They must be consistent.

Feedback

What Next

Change the library to make the bus width and the memory group word width consistent.

Examples

```
cell (libg188) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 10;
        word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

           memory_write() {
             address : ram_addr;
             enable : WR;
           }
     }
     bus (WR) {
       bus_type   : "bus10"
       direction : input;
       capacitance : 1.0;
       fanout_load : 1.0;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       memory_read() {
         address : ram_addr;
       }
    }
 }
```

In this case, the bus type of the enable 'WR' is bus10. Change it to bus8.

Examples

```
Error: Line 42, In the 'libg188' cell, the enable 'WR' bus has a width of
 10,
        but the memory group has a word width of 8. (LIBG-188)
```

Feedback

LIBG-189

(error) In the '%s' cell, the memory_write group cannot\n \thave both the enable attribute and the clocked_on attribute.

Description

The memory_write group has both the enable attribute and the clocked_on attribute specified. The Library Compiler does not allow it.

What Next

If the memory write process is edge triggered, use the clocked_on attribute. If the memory write process is level-sensitive triggered, use the enable attribute. You cannot specify both at once.

Examples

```
cell (libg189) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 10;
        word_width : 8;
       }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8";
           direction : input;
           capacitance : 1.0;

           memory_write() {
             address : ram_addr;
             enable : WR;
             clocked_on : WR;
           }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;
       memory_read() {
```

Feedback

```
          address : ram_addr;
        }
    }
 }
```

For the bus 'data_in', you can either have the enable attribute or the clocked_on attribute defined in the memory_write, but not both.

Examples

```
Error: Line 40, In the 'libg189' cell, the memory_write group cannot
        have both the enable attribute and the clocked_on attribute.
 (LIBG-189)
```

LIBG-190

(error) In the '%s' cell, the v3.1 sequential syntax is not\n \tsupported on memory cells.

Description

The cell has both the memory syntax and the v3.1 sequential syntax defined by either the *function* attribute or the *ff* and *latch* groups. The two syntaxes are not compatible and cannot both be specified on the same cell.

What Next

Remove the v3.1 sequential syntax, and use the new state table syntax.

Examples

```
cell (libg190) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 10;
        word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

           memory_write() {
             address : ram_addr;
             enable : WR;
           }
```

Feedback

```
      }
      pin (WR) {
        direction : input;
        capacitance : 1.0;
        clock : true;
      }

      bus(data_out){
        bus_type  : "bus8";
        direction : output;
        function : "WR + data_in";
        memory_read() {
          address : ram_addr;
        }
      }
  }
```

The function attribute is defined for the pin 'data_out'. This message is displayed for each element of the bus data_out that has the function attribute. To fix the problem, temove the function attribute from the pin.

Examples

```
Error: Line 60, In the 'libg190' cell, the v3.1 sequential syntax is not
        supported on memory cells. (LIBG-190)
```

LIBG-191

(error) The '%s' memory output cannot have a function.

Description

The memory output has an internal_node or a state_function attribute. A memory output has its function defined by the memory_read group and cannot also have an internal_node or a state_function attribute.

What Next

Remove the internal_node or state_function attribute.

Examples

```
cell (libg191) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 10;
        word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
```

Feedback

```
            direction : input;
            capacitance : 1.46;
      }
      bus (data_in) {
            bus_type   : "bus8"
            direction : input;
            capacitance : 1.46;

            memory_write() {
              address : ram_addr;
              enable : WR;
            }
      }
      pin (WR) {
        direction : input;
        capacitance : 1.13;
        clock : true;
      }

      bus(data_out){
        bus_type  : "bus8";
        direction : output;
        state_function : "WR + data_in"; /* not allowed */
        memory_read() {
          address : ram_addr;
        }
     }
 }
```

This message is displayed for each element of the bus data_out that has the state_function attribute.

Examples

```
Error: Line 60, The 'data_out[0]' memory output cannot have a function.
 (LIBG-191)
```

LIBG-192

(error) The '%s' port that has both memory_read and memory_write\n \tmust have the inout direction.

Description

Buses with both memory_read and memory_write groups must have the direction inout.

What Next

Either change the direction of this bus to inout, or remove either the memory_read or memory_write group from this bus.

Feedback

Examples

```
cell (libg192) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 10;
        word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : output;      /* must be inout */
       memory_read() {
         address : ram_addr;
       }
       memory_write() {
          address : ram_addr;
          enable : WR;
       }
    }
 }
```

In this case, the direction of the bus 'data-out' is output. To fix the problem, set the direction to inout. This message is displayed for each element of the bus data_out.

Examples

```
Error: Line 62, The 'data_out[0]' port that has both memory_read and
 memory_write
        must have the inout direction. (LIBG-192)
```

Feedback

LIBG-193

(error) The '%s' port that has both memory_read and memory_write\n \tmust have a three_state expression.

Description

Buses with both memory_read and memory_write groups must have the *three_state* attribute. During the memory write cycle, when the new data value is driven in from outside the cell, the port associated with the memory_read group must have a three_state attribute.

What Next

Add a valid three_state expression to this bus, or remove either the memory_read or memory_write group from this bus.

Examples

```
cell (libg193) {
      area : 2300.0;
      memory() {
        type : ram;
        address_width : 10;
        word_width : 8;
      }

      bus (ram_addr) {
           bus_type  : "bus10"; /* defined in the library */
           direction : input;
           capacitance : 1.0;
     }
     bus (data_in) {
           bus_type   : "bus8"
           direction : input;
           capacitance : 1.0;

     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : inout;       /* must have three_state */
       memory_read() {
         address : ram_addr;
       }
       memory_write() {
          address : ram_addr;
```

Feedback

```
          enable : WR;
        }
    }
 }
```

In this case, the bus 'data_out' has both memory_read and memory_write groups, but no three_state attribute. This message is displayed for each element of the bus data_out. To fix the problem, add the three_state attribute to the bus as follows:

```
pin (CE) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }
     bus(data_out){
       bus_type  : "bus8";
       direction : inout;
       three_state : "CE";       /* new statement */
       memory_read() {
         address : ram_addr;
       }
       memory_write() {
          address : ram_addr;
          enable : WR;
       }
    }
```

Examples

```
Error: Line 62, The 'data_out[0]' port that has both memory_read and
 memory_write
        must have a three_state expression. (LIBG-193)
```

LIBG-194

(warning) The function attribute on the '%s' pin is ignored.

Description

This message indicates that the *function* attribute on the specified pin is ignored. If the pin is an internal pin, use *state_function* attribute. Internal pins are equal to internal nodes, which are single sequential elements. If the cell is a memory cell, it does not need a *function* attribute if the pin already has a *memory_read*, has a *state_function* attribute, or is an internal node.

What Next

Either change the internal pin to a output or inout port or remove the *function* attribute.

Feedback

Examples

```
cell(libg202) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
    inverted_output : FALSE;
    function : "Q";
    internal_node : "Q";
  }
  pin(QB) {
    direction : output;
    inverted_output : TRUE;
    internal_node : "QB";
  }
}
```

Examples

```
Warning: Line 127, the function attribute on the 'Q' pin is ignored.
 (LIBG-194)
```

LIBG-195

(warning) A bundle is not supported in the memory group.

Description

Currently, Library Compiler does not support memory cells with bundles.

What Next

Modify the bundle into a bus.

Examples

```
cell (libg195) {
      area : 2300.0;
      memory() {
```

```
        type : ram;
        address_width : 10;
        word_width : 8;
       }

       bundle (ram_addr) {
        members( D_1 D_2);
        direction : input;
        capacitance : 1.0;
      }
      bus (data_in) {
        bus_type   : "bus8"
        direction : input;
        capacitance : 1.0;
        memory_write() {
           address : ram_addr;
           enable : WR;
        }
      }
      pin (WR) {
        direction : input;
        capacitance : 1.0;
        clock : true;
      }
      bus(data_out){
        bus_type  : "bus8";
        direction : output;
        memory_read() {
          address : ram_addr;
        }
     }
  }
```

Examples

```
Warning: Line 94, A bundle is not supported in the memory group.
 (LIBG-195)
```

LIBG-196

(warning) The inverted_output attribute is not defined in the '%s' output port.

Description

Library Compiler uses the *inverted_output* attribute value to determine whether a sequential output pin is inverting or noninverting.

If this attribute is not defined. LC will make following assumptions: - For the output with "internal_node" == first output node in statetable, it is assumed to be noninverting; - For the output with "internal_node" == second output node in statetable, it is assumed to be inverting.

Feedback

What Next

Make sure each inout and output pin has its "inverted_output" attribute set.

Examples

```
cell(libg202) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
  }

  pin(Q) {
    direction : output;
/*    inverted_output : FALSE; */
    internal_node : "Q";
  }
  pin(QB) {
    direction : output;
    inverted_output : TRUE;
    internal_node : "QB";
  }
}
```

In this case, set the inverted_output value to FALSE in the port 'Q' to construct the correct logic for the Design Compiler. Without it, LC will make assumption that the port 'Q' is noninverting.

Examples

```
Warning: Line 127, The inverted_output attribute is not defined in the
 'Q' output port. (LIBG-196)
```

LIBG-197

(warning) In the '%s' cell, the '%s' and '%s'\n \tmemory read or memory write ports have the same address attribute.

Description

This message indicates that the same address attribute is used for both of the specified memory read or memory write ports. Each port must have a unique address attribute.

Feedback

What Next

Edit the cell description so that the specified ports have unique address attributes.

Examples

```
cell (libg197) {
      area : 2300.0;
      memory() {
       type : ram;
       address_width : 10;
       word_width : 8;
      }

      bus (ram_addr) {
       bus_type  : "bus10"; /* defined in the library */
       direction : input;
       capacitance : 1.0;
     }
     bus (data_in) {
       bus_type   : "bus8"
       direction : input;
       capacitance : 1.0;
       memory_write() {
          address : ram_addr;
          enable : WR;
       }
     }
     pin (WR) {
       direction : input;
       capacitance : 1.0;
       clock : true;
     }
     pin (EN) {
       direction : input;
       capacitance : 1.0;
     }

     bus(data_out){
       bus_type  : "bus8";
       direction : inout;
       three_state : "EN";
       memory_read() {
         address : ram_addr;
       }
       memory_write() {
          address : ram_addr;
          enable : WR;
       }
    }
 }
```

Feedback

In this case, the ports 'data_in' and 'data_out' have the same address attribute for the memory_write group. This message is displayed for each element of the bus data_in and the bus data_out.

Examples

```
Warning: Line 38, In the 'libg197' cell, the 'data_in[0]' and
 'data_out[0]'
        memory read or memory write ports have the same address
 attribute. (LIBG-197)
```

LIBG-198

(error) The '%s' pin of the '%s' design must be an '%s'.

Description

By definition, a pin in the *related_pin* attribute for timing constraints must be a input pin.

What Next

Check your library for a wrong pin in the *related_pin* attribute or for an incorrect *timing_type*.

Examples

```
Error: Line 153, The 'P' pin of the 'libg198' design must be an 'input'.
 (LIBG-198)
```

LIBG-199

(error) The '%s' input port in the '%s' cell cannot have timing arcs.

Description

Input ports cannot have timing arcs. There is a possible problem in the direction of the pin, which should be output or inout.

What Next

Check your library for a pin with a wrong direction. Change the direction to output or inout.

Examples

```
Error: Line 53, The 'D' input port in the 'libg199' cell cannot have
 timing arcs. (LIBG-198)
```

Feedback

LIBG-201

(error) The min_period and min_pulse_width attributes are not allowed on the '%s' port in the '%s' cell.

Description

This message indicates that the specified port has a *min_period*, *min_pulse_width_high*, or *min_period_width_low* attribute. These attributes are allowed only on clock enable ports.

What Next

Update the technology library source to remove the offending attributes.

LIBG-202

(information) In the '%s' cell, the '%s' internal pin is\n \treplaced with the inverted '%s' output pin.

Description

This message indicates that the specified internal pin is an inversion of the output pin. The internal pin is replaced by the inverted output pin. This deletion is done without affecting the functionality of the cell. An internal pin that is never visible is functionally useless. Every internal pin must have a unique functional relationship with an output port.

What Next

Either delete the internal pin or give it a unique functional relationship with an output port.

Examples

```
cell(libg202) {
  area : 10;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
    capacitance : 1;
  }
  statetable ( "D CP", "Q QB") {
    table : "L/H R  : - - : L/H H/L,\\\n
             -   ~R : - - : N   N";
  }

  pin(Q2) {
    direction : internal ;
```

Feedback

```
    internal_node : "QB" ;
  }
  pin(Q) {
    direction : output;
    internal_node : "Q";
  }
  pin(QB) {
    direction : output;
    state_function : "Q2'";
  }
}
```

In this case the internal node 'Q2' is an inversion of the output 'Q'.

Examples

```
Information: Line 125, In the 'libg202' cell, the 'Q2' internal pin is
        replaced with the inverted 'Q' output pin. (LIBG-202)
```

LIBG-203

(warning) The '%s' test cell has no function.

Description

One of the test_cells has no functional description. Each test cell needs a functional description (flip-flop or latch description). This is used to determine the full functionality of the cell and is also used for the command insert_test.

When reading a .db library, Library Compiler creates a full function if there is any test_cell with a functional description. If no test_cells have a functional description and there is no full cell functional description, the cell is converted to a black box.

What Next

Modify the library to specify a functional description within the test_cell group. If a full cell has the function description instead, the cell is no longer a black box, but the *insert_test* command will not be able to use the functional description.

LIBG-204

(error) The '%s' test cell has no function and the cell is black box.

Description

One of the test_cells has no functional description. Each test cell needs a functional description (ff or latch description). This is used to determine the full function of the cell and is also used for the command insert_test.

Feedback

This cell becomes a black box and read_lib cannot proceed with reading the library if this error is found.

What Next

Specify a functional description within the test_cell. If you specify a full cell description instead, the cell is no longer a black box but insert_test cannot use the functional description.

LIBG-205

(warning) Cell(%s): The function cannot be recognized \n\tduring functional optimization by Design Compiler.

Description

This warning message informs you that Library Compiler encountered one of the following problems:

1. Library Compiler failed to map the state table description of the cell to the flip-flop or latch group description due to the complexity of the function.
2. Library Compiler failed to degenerate a multiple flip-flop or latch group to a single flip-flop or latch group due to the complexity of the function.

The function cannot be recognized by Design Compiler. This cell becomes a black box cell during synthesis. However, it might not be a black box cell to DFT Compiler or other tools, depending on its test_cell description, if there is one.

What Next

For item 1 above, ignore this message if the intended function cannot be described in v3.1 flip-flop or latch syntax. Otherwise, correct the state table function.

For item 2 above, correct the multiple sequential description if it cannot be simplified to a single sequential descriptor by tied up disable values. Otherwise, ignore the message.

Examples

In the following example, the cell cannot be modeled in v3.1 format, so the warning message should be ignored:

```
cell(libg205) {
  area : 16;
  pin(D) {
    direction : input;
    capacitance : 1;
  }
  pin(CP) {
    direction : input;
```

```
    capacitance : 2;
  }
  pin (Q0) {
    direction : output;
    internal_node : "Q";
    input_map : "D CP";
    ...
  }
  pin (Q1) {
    direction : output;
    internal_node : "Q";
    input_map : "Q0 CP";
    ...
  }
  pin (Q2) {
    direction : output;
    internal_node : "Q";
    input_map : "Q1 CP";
    ...
  }
  pin (Q3) {
    direction : output;
    internal_node : "Q";
    input_map : "Q2 CP";
    ...
  }
  statetable( "D CP", "Q QN" ) {
    table : "- ~R : - - : N N,\\\n
             H/L R : - - : H/L L/H";
  }
}
```

This example generates the following warning message:

```
Warning: Line 21, Cell(libg205): The function cannot be
         recognized by Design Compiler. The cell becomes a black box.
         (LIBG-205)
```

In the following example, the cell cannot be simplified into one flip-flop description by giving disable values (NRESTORE = 1 and SAVE = 0):

```
cell(libg205_1) {
  latch ("p1",IQ,IQN) {
     data_in : "((D !SE) + (SE SI))";
     enable : "!p1 + SAVE";
     clear : "!CDN";
  }
  latch ("p1, p2",IQ1,IQN1) {
     data_in : "p2";
     enable : "p1 + NRESTORE";
     clear : "!CDN";
  }
  pin (inQ) {
```

```
      function : "IQ";
      reference_input : "CP";
   }
   pin (NRESTORE) {
      retention_pin("restore",1);
   }
   pin (Q) {
     function : "IQ1";
     reference_input : "CP inQ";
   }
   pin (SAVE) {
     retention_pin("save",0);
   }
}
```

This example results in the following warning message:

```
Warning: Line 21, Cell(libg205_1): The function cannot be
         recognized by Design Compiler. The cell becomes a black box.
         (LIBG-205)
```

LIBG-206

(warning) The logic represented by the 'when' string (%s) in this %s group is equivalent to logic %s.

Description

The logic represented by the 'when' string of state-dependent internal_power and leakage_power groups should not be logically equivalent to logic 0 or logic 1.

A power table with its 'when' condition equivalent to logic 0 is meaningless because it will always be ignored during power calculation.

A power table with its 'when' condition equivalent to logic 1 is valid all states and is therefore not state dependent. It should be represented by a power table without the 'when' condition.

What Next

Check the 'when' conditions in the internal power or leakage power group and check that that are not equivalent to logic 0 or 1. Since such condition values are typically meaningless, the power tables may have been characterized incorrecly. 'when' strings with conditons equivalent to logic 1 should be removed. Power tables with conditions equivalent to logic 0 should be removed. This warning may be promoted to an error in future releases.

Feedback

LIBG-207

(error) The logic represented by the 'when' string (%s) in this\n \t%s group is not mutually exclusive with the logic represented by\n \tthe 'when' string (%s) in the %s group on line %d.

Description

The logic represented by the 'when' string of all state-dependent or path-dependent internal_power groups between a pair of pins should be mutually exclusive. If it is not, Library Compiler is not be able to determine which internal_power group to use when propagating a signal through the path, if the condition causes both of them to be evaluated 'TRUE'.

The logic represented by the 'when' string of all state-dependent leakage_power groups should be mutually exclusive. If it is not, Library Compiler is not be able to determine which leakage_power group to use if the condition cause more than one condition to be evaluated 'TRUE'.

What Next

Check the 'when' strings of both timing groups for wrong information and fix.

Examples

```
cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "S0'D0 + S0 D1";
        timing() {
          timing_sense : non_unate;
          intrinsic_rise : 1.00;
          intrinsic_fall : 1.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : " D0 D1";
        }
        timing() {
          when : "S0'D0 + S0 D1'";
          when : "D1' S0 + S0'D0 ";
          sdf_cond : "(D1 == 1'b0 && S0 == 1'b1) || (S0 == 1'b0 && D0 ==
 1'b1)";
          timing_sense : positive_unate;
          intrinsic_rise : 1.00;
          intrinsic_fall : 1.00;
          rise_resistance : 0.1;
```

Feedback

```
          fall_resistance : 0.1;
          related_pin : "S0";
        }
        timing() {
          when : "D1 S0 + S0'D0";
          sdf_cond : "(D1 == 1'b1 && S0 == 1'b1) || (S0 == 1'b0 && D0 ==
 1'b0)";
          timing_sense : non_unate;
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
        timing() { /* default */
          intrinsic_rise : 1.00;
          intrinsic_fall : 2.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
      }
    }
```

In this case, the second when attribute's string has a typographical error. It should be "D1 S0 + S0'D0'"; where the pin D0 should be ticked according to the sdf_cond attribute's string.

Examples

```
Error: Line 258, The logic represented by the 'when' string (S0'D0 + S0
 D1') in this
        timing group is not mutually exclusive with the logic represented
 by
        the 'when' string (D1 S0 + S0'D0) in the timing group on line
 268. (LIBG-
44)
```

LIBG-207w

(warning) The logic represented by the 'when' string (%s) in this\n \t%s group is not mutually exclusive with the logic represented by\n \tthe 'when' string (%s) in the %s group on line %d.

Description

The logic represented by the 'when' string of all state-dependent or path-dependent internal_power groups between a pair of pins should be mutually exclusive. If it is not, Library Compiler is not be able to determine which internal_power group to use when

Feedback

propagating a signal through the path, if the condition causes both of them to be evaluated 'TRUE'.

The logic represented by the 'when' string of all state-dependent leakage_power groups should be mutually exclusive. If it is not, Library Compiler is not be able to determine which leakage_power group to use if the condition cause more than one condition to be evaluated 'TRUE'.

The following example shows an instance where this message occurs:

```
cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "S0'D0 + S0 D1";
        timing() {
          timing_sense : non_unate;
          intrinsic_rise : 1.00;
          intrinsic_fall : 1.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : " D0 D1";
        }
        timing() {
          when : "S0'D0 + S0 D1'";
          when : "D1' S0 + S0'D0 ";
          sdf_cond : "(D1 == 1'b0 && S0 == 1'b1) || (S0 == 1'b0 && D0 ==
 1'b1)";
          timing_sense : positive_unate;
          intrinsic_rise : 1.00;
          intrinsic_fall : 1.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
        timing() {
          when : "D1 S0 + S0'D0";
          sdf_cond : "(D1 == 1'b1 && S0 == 1'b1) || (S0 == 1'b0 && D0 ==
 1'b0)";
          timing_sense : non_unate;
          intrinsic_rise : 0.1;
          intrinsic_fall : 0.1;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
        timing() { /* default */
          intrinsic_rise : 1.00;
```

```
          intrinsic_fall : 2.00;
          rise_resistance : 0.1;
          fall_resistance : 0.1;
          related_pin : "S0";
        }
      }
    }
```

In this case, the second when attribute's string has a typographical error. It should be "D1 S0 + S0'D0'"; where the pin D0 should be ticked according to the sdf_cond attribute's string.

The following is an example message:

```
Warning: Line 258, The logic represented by the 'when' string (S0'D0 + S0
 D1') in this
        timing group is not mutually exclusive with the logic represented
 by
        the 'when' string (D1 S0 + S0'D0) in the timing group on line
 268. (LIBG-
207w)
```

What Next

Check the 'when' strings of both timing groups for wrong information and fix.

LIBG-208

(warning) Different number of pins on the '%s' test_cell are found.\n \tThe test_cell is removed.

Description

The cell and its associated test_cell must have the same number of pins.

This warning informs you that the test_cell pointed to has a different number of pins than its parent cell.

What Next

Check the library description to ensure that each test_cell has the same number of pins as the parent cell.

Examples

```
cell(lbdb128) {
      area : 13;
      pin(D) {
        direction : input;
        capacitance : 1;
      }
      pin(G) {
```

```
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
  }
  pin(Q) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "G C2";
    }
  }
  pin(QN) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "G C2";
    }
  }
  test_cell() {
    pin(D) {
      direction : input;
    }
    pin(G) {
      direction : input;
    }
    pin(D2) {
      direction : input;
      signal_type : "test_scan_in";
    }
    pin(C2) {
      direction : input;
      signal_type : "test_scan_clock";
    }
    pin(SE) {
      direction : input;
      capacitance : 2;
      signal_type : "test_scan_enable";
    }
```

Feedback

```
        state ("IQ","IQN") {
          force_01 : "G D'";
          force_10 : "G D";
        }
        pin(Q) {
          direction : output;
          function : "IQ";
          signal_type : "test_scan_out";
        }
        pin(QN) {
          direction : output;
          function : "IQN";
          signal_type : "test_scan_out_inverted";
        }
      }
    }
```

In this case, the 'SE' pin is defined in the test_cell, but it is not defined in the parent cell. To fix the problem, add the definition,

```
pin(SE) {
        direction : input;
        capacitance : 2;
      }
```

Examples

```
Warning: Line 124, Different number of pins on the 'lbdb128' cell are
 found.
        The test_cell is removed. (LIBG-208)
```

LIBG-209

(warning) Unable to find the '%s' pin on the '%s' test_cell.\n \tThe test_cell is removed.

Description

This message indicates that you specified a different pin name in the cell and its associated test_cell. This might be caused by a typo. The Library Compiler ignores the associated test_cell.

What Next

Check the library description to ensure that each test_cell has the same number of pins as the parent cell.

Examples

```
cell(lbdb129) {
      area : 13;
      pin(D) {
        direction : input;
```

Feedback

```
    capacitance : 1;
  }
  pin(G) {
    direction : input;
    capacitance : 2;
  }
  pin(D2) {
    direction : input;
    capacitance : 1;
  }
  pin(C2) {
    direction : input;
    capacitance : 2;
  }
  pin(SE) {
    direction : input;
    capacitance : 2;
  }
  pin(Q) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "G C2";
    }
  }
  pin(QN) {
    direction : output;
    timing() {
      timing_type : rising_edge;
      intrinsic_rise : 1.0;
      intrinsic_fall : 1.0;
      rise_resistance : 0.1;
      fall_resistance : 0.1;
      related_pin : "G C2";
    }
  }
  test_cell() {
    pin(D) {
      direction : input;
    }
    pin(G) {
      direction : input;
    }
    pin(D2) {
      direction : input;
      signal_type : "test_scan_in";
    }
    pin(C2) {
      direction : input;
```

Feedback

```
        signal_type : "test_scan_clock";
      }
      pin(SEB) {
        direction : input;
        capacitance : 2;
        signal_type : "test_scan_enable";
      }
      latch ("IQ","IQN") {
        data_in : "D";
        enable : "G";
      }
      pin(Q) {
        direction : output;
        function : "IQ";
        signal_type : "test_scan_out";
      }
      pin(QN) {
        direction : output;
        function : "IQN";
        signal_type : "test_scan_out_inverted";
      }
    }
  }
```

In this case, a pin is named 'SE' at the cell level and 'SEB' at the test_cell level. To fix the problem, give the pin the same name.

Examples

```
Warning: Line 124, Unable to find the 'SE' pin on the 'lbdb129'
 test_cell.
        The test_cell is removed. (LIBG-209)
```

LIBG-210

(error) The '%s' pin of the '%s' cell has conflicting signal_types\n \tbetween the cell and the test_cell.

Description

This message indicates that you specified conflicting signal_type attributes for the same pin on different test_cell groups.

What Next

Check the library description to ensure that each test_cell has no conflicting signal_type attributes on its pins.

Examples

```
cell(lbdb131) {
      area : 13;
```

```
pin(D) {
  direction : input;
  capacitance : 1;
}
pin(G) {
  direction : input;
  capacitance : 2;
}
pin(D2) {
  direction : input;
  capacitance : 1;
}
pin(C2) {
  direction : input;
  capacitance : 2;
}
pin(SE) {
  direction : input;
  capacitance : 2;
}
pin(Q) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "G C2";
  }
}
pin(QN) {
  direction : output;
  timing() {
    timing_type : rising_edge;
    intrinsic_rise : 1.0;
    intrinsic_fall : 1.0;
    rise_resistance : 0.1;
    fall_resistance : 0.1;
    related_pin : "G C2";
  }
}
test_cell() {
  pin(D) {
    direction : input;
  }
  pin(G) {
    direction : input;
  }
  pin(D2) {
    direction : input;
    signal_type : "test_scan_in";
  }
```

Feedback

```
    pin(C2) {
      direction : input;
      signal_type : "test_scan_clock";
    }
    pin(SE) {
      direction : input;
      capacitance : 2;
      signal_type : "test_scan_enable";
    }
    state ("IQ","IQN") {
      force_01 : "G D'";
      force_10 : "G D";
    }
    pin(Q) {
      direction : output;
      function : "IQ";
      signal_type : "test_scan_out";
    }
    pin(QN) {
      direction : output;
      function : "IQN";
      signal_type : "test_scan_out_inverted";
    }
  }
  test_cell() {
    pin(D) {
      direction : input;
    }
    pin(G) {
      direction : input;
    }
    pin(D2) {
      direction : input;
      signal_type : "test_scan_in";
    }
    pin(C2) {
      direction : input;
      signal_type : "test_scan_clock";
    }
    pin(SE) {
      direction : input;
      capacitance : 2;
      signal_type : "test_scan_enable_inverted";
    }
    state ("IQ","IQN") {
      force_01 : "G D'";
      force_10 : "G D";
    }
    pin(Q) {
      direction : output;
      function : "IQ";
      signal_type : "test_scan_out";
    }
```

```
        pin(QN) {
          direction : output;
          function : "IQN";
          signal_type : "test_scan_out_inverted";
        }
      }
    }
```

In this case, The 'SE' pin has a test_scan_enable signal_type in the first test_cell group and a test_scan_enable_inverted signal_type in the second test_cell group. To fix the problem, make the signal_type consistent between the two test_cell groups.

Examples

```
Error: Line 94, The 'SE' pin of the 'lbdb131' cell has conflicting
 signal_types
       between the cell and the test_cell. (LIBG-210)
```

LIBG-211

(warning) Cell '%s' contains unused input pin(s).\n\tIt is labeled dont_use and dont_touch.

Description

An input pin is unused if it does not appear in any functional statement, or state table input or input map, nor does it have any test signal_type description. Such cells may cause synthesis to generate errouneous logic because of incomplete modeling.

What Next

Either delete the unused input pin or add it the functionality of the cell.

Examples

```
cell(acell) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
                next_state : "IQ'";
                clocked_on : "CLK";
        }
        pin(Q) {
                direction : output;
                function : "IQ";
        }
```

Feedback

```
        pin(QN) {
                direction : output;
                function : "IQN";
              }
  }
```

Examples

```
Warning: Line 202, Cell 'acell' contains unused input pin(s).
        It is labeled dont_use and dont_touch. (LIBG-211)
```

LIBG-212

(warning) The logic represented by the '%s' when string in this %s group\n \tdoes not sensitize one or all pins in the '%s' related_pin attribute for the %s function attribute.

Description

This message indicates that the when attribute within an internal_power group does not make sense given the function associated with the output pin. Library Compiler warns you that allowing these extra tables in the library, you are unnecessarily increasing the size of the library and may be characterizing unnecessary data.

What Next

Check the 'when' string of internal_power group for wrong information and fix.

Examples

```
cell(libg212) {
      area : 2;
      pin(A B) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "A & B";
        internal_power() {
          related_pin : "B";
          when : "!A'";
           ...
        }
      }
    }
```

In this case, this internal power table will never be accessed. This is because in order for B to cause Z to change, pin A must be high.

Feedback

Examples

```
Warning: Line 191, The logic represented by the '!A' when string in this
 internal_power group
        does not sensitize one or all pins in the 'B ' related_pin
 attribute for the (A & B) function attribute. (LIBG-212)
```

LIBG-213

(warning) The default internal power is not needed for the %s pin.

Description

This message indicates that the set of 'when' attributes is complete for the internal_power and there is no need for the default internal power table.

What Next

Check the 'when' string of internal_power groups for wrong information and fix or remove the default internal power group.

Examples

```
cell(libg213) {
      area : 2;
      pin(A B) {
        direction : input;
        capacitance : 1;
      }

       pin ( Z ) {
         direction : output ;
         function : "A & B";
         internal_power () {
           when : "A";
           related_pin : "B";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
         }
         internal_power () {
           when : "B";
           related_pin : "A";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
         }
         internal_power () {
           related_pin : "A B";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
```

Feedback

```
        }
      }
    }
```

In this case, the default internal power table is not needed. This is because in the when attribute contains all possible paths which will sensitize the related_pin B to the output. Therefore, no default internal power table is needed.

Examples

```
Warning: Line 183, The default internal power is not needed for the A
 pin. (LIBG-213)
```

LIBG-214

(warning) The default internal power is required for the '%s' pin.

Description

This message indicates that the set of 'when' attributes is not complete for the internal_power and there is a need for the default internal power table.

What Next

Check the 'when' string of internal_power groups for wrong information and fix or add the default internal power group.

Examples

```
cell(libg214) {
      area : 2;
      pin(A B) {
        direction : input;
        capacitance : 1;
      }

       pin ( Z ) {
         direction : output ;
         function : "A & B";
         internal_power () {
           when : "A";
           related_pin : "B";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
         }
      }
    }
```

In this case, the default internal power table is needed for the related_pin A. This is because the when attribute does not contain all possible paths which will sensitize the

Feedback

related_pin A to the output. Therefore, you either add the power table associated with the related pin A and a when or add the default internal power table as show below:

either internal_power () { when : "B"; related_pin : "A"; power(power_template) { values (" 1.000000, 1.000000, 1.000000, 1.000000"); } } or internal_power () { related_pin : "B"; power(power_template) { values (" 1.000000, 1.000000, 1.000000, 1.000000"); } }

Examples

```
Warning: Line 183, The default internal power is required for the 'A'
 pin. (LIBG-214)
```

LIBG-215

(error) The '%s' when condition includes the '%s' related pin.

Description

This message indicates that the 'when' and 'related_pin' attributes contain the same pin. This condition does not make sense because the when attribute is a static state while the related_pin attribute is the transitioning pin.

Note that the 'related_pin' of a pin includes the pin itself.

What Next

Check the 'when' and the 'related_pin' strings of the internal_power group for wrong information and fix it.

Examples

```
cell(libg215) {
      area : 2;
      pin(A B) {
        direction : input;
        capacitance : 1;
      }

       pin ( Z ) {
         direction : output ;
         function : "A & B";
         internal_power () {
           when : "A";
           related_pin : " A B";
           power(power_template) {
           values (" 1.000000, 1.000000, 1.000000, 1.000000");
           }
         }
      }
    }
```

Feedback

In this case, the internal power table contains the A pin in both the when and the related_pin attributes. Either remove the A pin from the related_pin or change the when statement.

Examples

```
Error: Line 183, The 'A' when condition includes the 'A' related pin.
 (LIBG-215)
```

LIBG-220

(warning) The '%s' equation on the '%s' cell evaluates\n \tto a '%s' constant.

Description

This message is generated when Library Compiler encounters a three-stated pin, whose three_state attribute always evaluates to 1.

What Next

Verify the cell and check the library description of the offending cell for correctness.

Examples

```
cell(libg220) {
        area : 6.50;
        pin(A) {
                direction : input;
                capacitance : 1.5;
        }
        pin(Y) {
                direction : output;
                function : "A";
                three_state : "1";
        }
      }
```

Examples

```
Warning: Line 218, The 'three_state' equation on the 'libg220' cell
 evaluates
        to a '1' constant. (LIBG-220)
```

LIBG-221

(warning) Cell %s, referred to by cell %s, does not exist.

Description

The missing cell is referred to by the "single_bit_degenerate" attribute from a multibit cell. This attribute will be removed from the multibit cell.

Feedback

What Next

Correct the attribute value or remove the attribute, or add the required cell in the library.

Examples

```
cell(FDBBX4) {
    area : 18;
    single_bit_degenerate : FDBB;
    bus(D) {
      ...
    }
    ...
  }
```

In this case, cell FDBB is not in the library.

Examples

```
Warning: Line 258, Cell FDBB, referred to by cell FDBBX4, does not exist.
 (LIBG-221)
```

LIBG-222

(warning) Cell %s, referred to by cell %s, is multibit.

Description

The offending cell is referred to by the "single_bit_degenerate" attribute from a multibit cell. This cell must be a single-bit cell.

What Next

Correct the attribute value or remove the attribute, or add the required cell in the library.

Examples

```
cell(FDBBX4) {
    area : 18;
    single_bit_degenerate : FDBBX2;
    bus(D) {
      ...
    }
    ...
  }
```

In this case, cell FDBBX2 is a multibit cell.

Examples

```
Warning: Line 58, Cell FDBBX2, referred to by cell FDBBX4, is multibit.
 (LIBG-221)
```

Feedback

LIBG-223

(warning) Cells %s and %s have different interfaces.

Description

The first cell is referred to by the "single_bit_degenerate" attribute from the second cell. These cells must have the same interfaces.

What Next

Correct the interfaces.

Examples

```
cell(FDBBX4) {
    area : 18;
    single_bit_degenerate : FDBB;
    bus(D) {
      ...
    }
    pin(CP) {
    }
    bus(Q) {
    }
  }
  cell(FDBB) {
    pin(D) {
    }
    pin(clk) {
    }
    pin(Q) {
    }
  }
```

In this case, bus D and pin D, and bus Q and pin Q are matched. But pin CP and pin clk, are not. To correct, either change clk to CP, or change CP to clk.

Examples

```
Warning: Line 58, Cells FDBB  and FDBBX4 have different interfaces.
 (LIBG-223)
```

LIBG-224

(warning) Cell %s has unequal bus or bundle widths.

Description

To be eligible for having the "single_bit_degerate" attribute, the cell\n \tmust be a multibit black box, and all buses must have the same width.

Feedback

What Next

Correct the bus range.

Examples

```
type (downbus3) {
    base_type : array;
    data_type : bit;
    bit_width : 3;
    bit_from : 2;
    bit_to   : 0;
    downto   : true;
  }
  type (bus4) {
    base_type : array;
    data_type : bit;
    bit_width : 4;
    bit_from : 0;
    bit_to   : 3;
    downto   : true;
  }

  cell(FDBBX4) {
    area : 18;
    single_bit_degenerate : FDBB;
    bus(D) {
      bus_type : downbus3;
      ...
    }
    pin(CP) {
    }
    bus(Q) {
      bus_type : bus4;
    }
  }
```

In this case, bus D has pin from 3 to 0, bus bus Q has range from 0 to 3.

Examples

```
Warning: Line 224, Cell FDBBX4 has unequal bus or bundle
 widths.(LIBG-224)
```

LIBG-225

(warning) Errors have been detected. The single_bit_degenerate\n \tattribute is removed from cell %s.

Feedback

Description

The single_bit_degenerate attribute is removed from the cell because there is an error regarding the attribute specification on this cell or related cell.

What Next

To specify "single_bit_degenerate" on a cell, the cell must satisfy:

```
It is a multibit black box with bus/bundle pin
        The bus member must range from 0 to N-1 or N-1 to 0 (N is the
 width)
        The single-bit cell referred to must be a single-bit cell.
        The two cells must have identical interface naming.
```

Examples

```
cell(FDBBX2) {
  area : 18;
  single_bit_degenerate : FDBB;
  bundle(D) {
    members(D0, D1); ...
  }
  pin(CP) { ...  }

  bundle(Q) {
    members(Q0, Q1); ...
  }
  bundle(QN) {
    members(Q0N, Q1N); ...
  }
}

cell(FDBB) {
  area : 18;
  pin(Data)  { ...  }
  pin(CP) { ...  }
  pin(Q)  { ...  }
  pin(QN) { ...  }
}
```

The single_bit_denerate would be ok if pin "Data" is renamed to "D".

Examples

```
Warning: Line 225, Errors have been detected. Attribute
 single_bit_degenerate
        is removed from cell %s. (LIBG-225)
```

LIBG-226

(warning) Only cell %s has geometry_print %s.

Feedback

Description

It is of no use to put a geometry_print on a single cell.

What Next

Remove it or put it on other cells when appropriate.

Examples

```
cell(FDBBX2) {
  area : 18;
  geometry_print : GP1;
  bundle(D) {
    members(D0, D1); ...
  }
  pin(CP) { ...  }

  bundle(Q) {
    members(Q0, Q1); ...
  }
  bundle(QN) {
    members(Q0N, Q1N); ...
  }
}
```

GP1 only appears on FDBBX2.

Examples

```
Warning: Line 226, Onle cell FDBBX2 has geometry_print GP1. (LIBG-226)
```

LIBG-228

(warning) Failed to transform the function of cell '%s' to a netlist. The cell becomes a black box for Formality.

Description

Library Compiler fails to synthesize a netlist structure representing functionality of this cell. Library Compiler does not accept a derived statetable description when performing this netlist transformation. That is, if the full-function description is not specified in the .lib file, this warning message will be issued. Other causes of failure should have been reported by other warning messages. This netlist structure is referenced by Formality. Without this netlist, Formality can only treat this cell as a black box.

What Next

Check the statetable description and make sure it is specified correctly.

Feedback

LIBG-229

(warning) Cell '%s' has non-disjoint input.

Description

One or more input pins used in the statetable are used in more than one sequential function, such as clock and enable. As a result, this function cannot be transformed by Library Compiler to a netlist structure referenced by Formality.

What Next

Check the statetable description and correct all mistakes.

LIBG-230

(warning) Internal pin '%s' is dangling. The pin is removed.

Description

The internal pin is not associated with any statetable, it does not have a function or a state_function, it is not a memory port, nor is it part of any timing-arc specification. It is redundant and therefore being removed.

What Next

You can add the required element if it is accidentally missing. Or a dummy timing arc will serve the purpose of keeping the internal pin interface.

LIBG-231

(information) Internal pin '%s' is for dcm timing.

Description

The internal pin is labeled for dcm timing use only.

What Next

Make sure the pin is used for dcm timing only, not for any other purpose.

LIBG-232

(error) The 'function' attribute on the '%s' internal Pin/bus of the\n \t'%s' cell is not allowed.

Feedback

Description

This error is issued when any internal pin of a combinational cell defines a function attribute. In a combinational cell, a function attribute can only be defined on an output pin.

What Next

Check your library for wrong attributes.

Examples

```
cell(libg232) {
  area : 1 ;
  pin (A) {
        direction : input ;
        capacitance : 0 ;
  }
  pin (A_INT) {
        direction : internal ;
        function : A;
        capacitance : 0 ;
        timing() {
                related_pin     : "A" ;
                intrinsic_rise  : 1.0 ;
                rise_resistance : 0.0 ;
                intrinsic_fall  : 1.0 ;
                fall_resistance : 0.0 ;
        }
  }
  pin ("Y") {
        direction : output ;
        function : "A'" ;
        timing() {
                related_pin     : "A_INT" ;
                intrinsic_rise  : 1.0 ;
                rise_resistance : 0.0 ;
                intrinsic_fall  : 1.0 ;
                fall_resistance : 0.0 ;
        }
  }
```

Examples

```
Error: Line 10, The 'function' attribute on the 'A_INT' internal pin/bus
 of the
        'libg232' cell is not allowed. (LIBG-232)
```

LIBG-233

(error) The 'clock_gate_enable_pin' attribute is defined on more than one\n \tpin in the '%s' cell.

Feedback

Description

This error is issued when the clock_gate_enable_pin attribute is defined on more than one pin in a cell. In a clock gating cell, there should only be at most one pin with the clock_gate_enable_pin attribute defined.

What Next

Check your library and remove extra clock_gate_enable_pin attribute.

Examples

```
cell(libg233) {
  area : 1 ;
  is_clock_gating_cell : TRUE;
  pin (A) {
        direction : input ;
        capacitance : 0 ;
        clock_gate_enable_pin : TRUE;
  }
  pin (B) {
        direction : input ;
        capacitance : 0 ;
        clock_gate_enable_pin : TRUE;
  }
  pin ("Y") {
        direction : output ;
        function : "A' B'" ;
        timing() {
                related_pin     : "A B" ;
                intrinsic_rise  : 1.0 ;
                rise_resistance : 0.0 ;
                intrinsic_fall  : 1.0 ;
                fall_resistance : 0.0 ;
        }
  }
```

Examples

```
Error: Line 10, The 'clock_gate_enable_pin' attribute is defined on more
 than one
        pin in the 'libg233' cell. (LIBG-233)
```

LIBG-234

(error) The '%s' cell cannot be used as a clock gating cell.

Description

This error is issued when the is_clock_gating_cell attribute is defined on a cell with disallowed function.

Feedback

The is_clock_gating_cell attribute can be set on

- 2-input clock gates Examples of 2-input clock gates are AND, NAND, OR, and NOR library cells that are used to gate clocks.

- 1-input cells Examples of 1-input clock gates are buffer and inverter library cells that are used in the fanin and fanout of the 2-input clock gate.

- 2-input D latches These latches can be active high or low and must have a noninverting output.

What Next

Check your library and correct the error.

Examples

```
cell(libg234) {
  area : 1 ;
  is_clock_gating_cell : TRUE;
  pin (A) {
        direction : input ;
        capacitance : 0 ;
        clock_gate_enable_pin : TRUE;
  }
  pin (B) {
        direction : input ;
        capacitance : 0 ;
  }
  pin (C) {
        direction : input ;
        capacitance : 0 ;
  }
  pin ("Y") {
        direction : output ;
        function : "A B C" ;
        timing() {
                related_pin     : "A B C" ;
                intrinsic_rise  : 1.0 ;
                rise_resistance : 0.0 ;
                intrinsic_fall  : 1.0 ;
                fall_resistance : 0.0 ;
        }
  }
```

Examples

```
Error: Line 10, The 'libg234' cell cannot be used as a clock gating cell.
 (LIBG-234)
```

Feedback

LIBG-235

(error) The '%s' attribute is either not\n \tdefined on any pin in the integrated clock gated '%s' cell\n \tor it is defined on a wrong pin.

Description

This error is issued when the clock_gate_enable_pin or clock_gate_clock_pin or clock_gate_outp_pin attribute is either not defined on any pin in a cell or it is defined on the wrong pin. In a clock gating cell, there should only be at most one pin with the clock_gate_enable_pin or clock_gate_out_pin or clock_gate_clock_pin attribute defined.

What Next

Check your library and add the missing clock gate attribute.

Examples

```
cell(libg235) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge";
  dont_use : true;
  dont_touch : true;
  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,\
               L  H  : - : H ,\
               H  -  : - : N ";
  }
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
    direction : input;
    capacitance : 1.0;
  }
  pin(CP) {
    direction : input;
    capacitance : 1.0;
    min_pulse_width_low  : 0.319;
    clock_gate_clock_pin : TRUE;
  }
  pin(Z) {
    direction : output;
    state_function : "CP * IQ";
    max_capacitance : 1.0;
    clock_gate_out_pin : TRUE;
  }
```

Feedback

Examples

```
Error: Line 10, The 'clock_gate_enable_pin' attribute is either not
        defined on any pin in the integrated clock gated 'libg235' cell
        or it is defined on a wrong pin. (LIBG-235)
```

LIBG-236

(error) The '%s' clock gate cell has the wrong number of pins.

Description

This error is issued when the clock_gating_integrated_cell attribute is defined on a cell with disallowed function.

The clock_gating_integrated_cell attribute must have at most two inputs pins and two output pins.

What Next

Check your library and correct the error.

Examples

```
cell(libg236) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge";
  dont_use : true;
  dont_touch : true;
  statetable(" CP1 EN ", "IQ ") {
     table : " L  L  : - : L ,\
               L  H  : - : H ,\
               H  -  : - : N ";
  }
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
    direction : input;
    clock_gate_enable_pin : true;
    capacitance : 1.0;
  }
  pin(CP1) {
    direction : input;
    capacitance : 1.0;
    min_pulse_width_low  : 0.319;
  }

  pin(CP2) {
    direction : input;
    capacitance : 1.0;
```

Feedback

```
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    state_function : "CP1 * IQ";
    max_capacitance : 1.0;
  }
```

Examples

```
Error: Line 10, The 'libg236' clock gate cell has the wrong number of
 pins. (LIBG-236)
```

LIBG-237

(error) The '%s' clock gate cell has the wrong type of pins.

Description

This error is issued when the clock_gating_integrated_cell attribute is defined on a cell with the wrong pin types

The clock_gating_integrated_cell attribute expects the following attributes on its pins: - clock_gate_enable_pin - clock_gate_obs_pin - clock_gate_test_pin

What Next

Check your library and correct the error.

Examples

```
cell(libg237) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge_precontrol";
  dont_use : true;
  dont_touch : true;
  statetable(" CP EN CTL", "IQ ") {
     table : " L  L  L : - : L ,\
               L  L  H : - : H ,\
               L  H  L : - : H ,\
               L  H  H : - : H ,\
               H  -  - : - : N ";
  }
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
    direction : input;
    capacitance : 0.017997;
    clock_gate_enable_pin : true;
  }
```

Feedback

```
  pin(CTL) {
    direction : input;
    capacitance : 0.017997;
  }
  pin(CP) {
    direction : input;
    capacitance : 0.031419;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    state_function : "CP * IQ";
    max_capacitance : 0.500;
  }
}
```

The attribute clock_gate_test_pin is missing. You need to add it to the 'CTL' pin.

```
clock_gate_test_pin : true;
```

Examples

```
Error: Line 10, The 'libg237' clock gate cell has the wrong type of pins.
 (LIBG-237)
```

LIBG-238

(error) The '%s' clock gate cell is not of type '%s'.

Description

This error is issued when the clock_gating_integrated_cell attribute is defined on a cell with disallowed function.

Check the Library Compiler User Guide for the list of the clock gating integrated cell types.

What Next

Check your library and correct the error.

Examples

```
cell(libg238) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge";
  dont_use : true;
  dont_touch : true;
  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,\
               L  H  : - : H ,\
               H  -  : - : N ";
  }
```

Feedback

```
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
    direction : input;
    capacitance : 1.0;
  }
  pin(CP) {
    direction : input;
    capacitance : 1.0;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    state_function : "CP * IQ * EN";
    max_capacitance : 1.0;
  }
```

Examples

```
Error: Line 10, The 'libg238' clock gate cell is not of type 'latch_pos'.
 (LIBG-238)
```

LIBG-238w

(warning) The '%s' clock gate cell is not of type '%s'.

Description

This warning is issued when the clock_gating_integrated_cell attribute is defined on a cell with disallowed function.

Check the Library Compiler User Guide for the list of the clock gating integrated cell types.

The following example shows an instance where this message occurs:

```
cell(libg238) {
  area : 1;
  clock_gating_integrated_cell : "latch_posedge";
  dont_use : true;
  dont_touch : true;
  statetable(" CP EN ", "IQ ") {
     table : " L  L  : - : L ,\
               L  H  : - : H ,\
               H  -  : - : N ";
  }
  pin(IQ) {
    direction : internal;
    internal_node : "IQ";
  }
  pin(EN) {
```

Feedback

```
    direction : input;
    capacitance : 1.0;
  }
  pin(CP) {
    direction : input;
    capacitance : 1.0;
    min_pulse_width_low  : 0.319;
  }
  pin(Z) {
    direction : output;
    state_function : "CP * IQ * EN";
    max_capacitance : 1.0;
  }
```

The following is an example message:

```
Warning: Line 10, The 'libg238' clock gate cell is not of type
 'latch_pos'. (LIBG-238w)
```

What Next

Check your library and correct the warning.

LIBG-239

(information) The timing arc from '%s' to\n \t'%s' is resolved into the three_state_enable type.

Description

The timing arc is entered as combitional/sequential. But the related pin is a fanin to the three_state function only.

What Next

Add "timing_type : three_state_enable;" to the timing group. Or check if this arc is intended for three_state_enable.

LIBG-240

(warning) The phase relationship of the outputs of cell '%s'\n \tis different from that of its test cell at line %d.

Description

The two outputs of the full cell are equal, but the outputs of the test cell are opposite; or vice versa.

Feedback

What Next

If you intended that the outputs of the full cell differ from the outputs of the test cell, no action is required. Otherwise, change the specification of one of the cells so that they agree.

Examples

```
cell (SCAN) {
    ff(IQ, IQN) {
      ...
    }
    pin (Q1) {
      direction : output;
      function  : IQ;
      ...
    }
    pin (Q2) {
      direction : output;
      function  : IQ;
      ...
    }
    ...
    test_cell() {
      ff(IQ, IQN) {
        ...
      }
      pin (Q1) {
        direction : output;
        function  : IQ;
        ...
      }
      pin (Q2) {
        direction : output;
        function  : IQN;
        ...
      }
      ...
    }
  }
```

EXAMPLE MESSAGES

```
Warning: Line 200, The phase relationship of the outputs of cell 'SCAN'
is different from that of its test cell at line %300. (LIBG-240)
```

LIBG-241

(warning) The '%s' cell has %d pins which exceeds the limit 16.\n \tThe state table is not generated.

Feedback

Description

The cell has over 16 pins. There is an exponential cose in performance and memory as the number of pins increases. This warning tells the user about the excessive size of the table that is being generated.

What Next

If possible, take advantage of the state table group and the input_map attribute to reduce the size of the table.

Examples

```
cell (libg241) {
latch(iq,iqn) {
    data_in : "((c1 *d1_b') +(c2 *d2_b') +(c3 *d3_b') +(c4 *d4_b')
 +(c5 *d5_b') +(c6 *d6_b') +(c7 *d7_b') +(c8 *d8_b') +(c9 *d9_b') +(c10
 *d10_b') +(c11 *d11_b') + (c12 * d12_b'))" ;
    enable : "(c1 +c2 +c3 +c4 +c5 +c6 +c7 +c8 +c9 +c10 +c11 +c12)" ;
    clear : "!rb";
    preset : "s";
    clear_preset_var1 : "L";
    clear_preset_var2 : "H";
}

      pin ( q ) {
         direction : output ;
         function : "iq";
        timing () {
            related_pin : "d1_b d2_b d3_b d4_b d5_b d6_b d7_b d8_b
d9_b d10_b d11_b d11_b " ;
            cell_rise ( prop1 ) {
               values ("0.102565, 0.092949, 0.117635, 0.129560");
            }
            rise_transition ( trans1 ) {
               values ("0.090691, 0.085401, 0.117467, 0.143013");
            }
            cell_fall ( prop1 ) {
               values ("0.099571, 0.101830, 0.122101, 0.129110");
            }
            fall_transition ( trans1 ) {
               values ("0.100989, 0.083367, 0.104448, 0.185206");
            }
         }

         timing () {
            related_pin : "c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12" ;
            cell_rise ( prop1 ) {
               values ("0.101839, 0.105114, 0.140100, 0.165207");
            }
            rise_transition ( trans1 ) {
               values ("0.097529, 0.087806, 0.104830, 0.119332");
            }
```

Feedback

```
            cell_fall ( prop1 ) {
               values ("0.117794, 0.121551, 0.145506, 0.159811");
            }
            fall_transition ( trans1 ) {
               values ("0.099574, 0.088423, 0.085064, 0.108336");
            }
            timing_type : rising_edge ;
         }

         timing () {
           related_pin : "s" ;
            cell_rise ( prop1 ) {
               values ("0.111990, 0.110565, 0.144589, 0.173835");
            }
            rise_transition ( trans1 ) {
               values ("0.102461, 0.097734, 0.129652, 0.175103");
            }
            timing_type : preset ;
            timing_sense : positive_unate ;
         }

         timing () {
            related_pin : "rb" ;
            cell_fall ( prop1 ) {
               values ("0.135732, 0.139003, 0.193663, 0.182614");
            }
            fall_transition ( trans1 ) {
               values ("0.090745, 0.091247, 0.107943, 0.171294");
            }
            timing_type : clear ;
            timing_sense : positive_unate ;
         }
      }

      pin(d1_b d2_b d3_b d4_b d5_b d6_b d7_b d8_b d9_b d10_b d11_b d12_b
rb s){
         direction : input ;
         capacitance : 0.1 ;

      }

       pin ( c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12) {
         direction : input ;
         capacitance : 0.1 ;
         clock : true ;
      }
   }
```

Examples

```
Warning: The 'libg241' cell has 26 pins which exceeds the limit of 16.\n
        The state table is not generated. (LIBG-241)
```

Feedback

LIBG-242

(warning) The '%s' cell has pins with 'x_function' attribute and\n \tit becomes a black box.

Description

For combinational cells with x function, th function id is set to be "unknown".

What Next

Make sure the description is correct.

Examples

```
cell(test) {
          area : 1;
          pin(A) {
            direction : input;
            capacitance : 0;
          }
          pin(B) {
            direction : input;
            capacitance : 0;
          }
          pin(O) {
            direction : output;
            function : "A'";
            x_function : "B";
          }
        }
```

Examples

```
Warning: Line 34, The 'test' cell has pins with 'x_function' attribute
 and
        it becomes a black box. (LIBG-242)
```

LIBG-243

(warning) The '%s' cell is missing the 'nextstate_type' attribute\n \tfor some input pin(s) specified in 'next_state' of its ff/ff_bank group.

Description

This warning message occurs when the attribute *nextstate_type* is not defined in the input pin included in the *next_state* attribute from the cell's sequential state description. In a pin group, *nextstate_type* defines the type of a *next_state* attribute to be used in an *ff* group, a sequential group, or an *ff_bank* group.

Feedback

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, check the library for each input pin used in the *next_state* statement of a sequential group and add the *nextstate_type* attribute if necessary.

Examples

```
cell(libg243) {
        area : 6.50;
        pin(D) {
           direction : input;
           capacitance : 3.0;
        }
        pin(CLK) {
           direction : input;
           capacitance : 1.5;
        }
        pin(SET) {
           direction : input;
           nextstate_type : scan_in;
           capacitance : 3.0;
        }

        ff("IQ","IQN") {
           next_state : "D CLK";
           clocked_on : "CLK";
           preset     : "SET'";
        }

        pin(Q) {
           direction : output;
           function : "IQ";
        }
        pin(QN) {
           direction : output;
           function : "IQN";
        }
   }
```

Examples

```
Warning: Line 153, The 'libg243' cell is missing the 'nextstate_type'
 attribute
        for some input pin(s) specified in 'next_state" of its ff/ff_bank
 group. (LIBG-243)
```

Feedback

LIBG-244

(warning) The values for clear_preset_var1 and \n \tclear_preset_var2 in the '%s' cell are opposite. \n \tThis may cause incorrect DC optimization.

What Next

Change the value of clear_preset_var1 or clear_preset_var2.

Examples

```
cell(libg111) {
        area : 11;
        pin(D) {
                direction : input;
                capacitance : 1;
        }
        pin(CP) {
                direction : input;
                capacitance : 1;
        }
        pin(CLR) {
                direction : input;
                capacitance : 1;
        }
        pin(SET) {
                direction : input;
                capacitance : 1;
        }
        ff("IQ","IQN") {
                next_state : "D";
                clocked_on : "CP";
                clear   : "CLR'";
                preset   : "SET'";
                clear_preset_var1 : L;
                clear_preset_var2 : H;
        }
        pin(Q) {
                direction : output;
                function : "IQ";
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
                        fall_resistance : 0.1;
                        related_pin : "CP";
                }
                timing() {
                        timing_type : clear;
                        timing_sense : positive_unate;
                        intrinsic_fall : 1.0;
```

Feedback

```
                        fall_resistance : 0.1;
                        related_pin : "CLR";
                }
                timing() {
                        timing_type : preset;
                        timing_sense : negative_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "SET";
                }
        }
        pin(QN) {
                direction : output;
                function : "IQN";
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
                        fall_resistance : 0.1;
                        related_pin : "CP";
                }
                timing() {
                        timing_type : preset;
                        timing_sense : negative_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "CLR";
                }
                timing() {
                        timing_type : clear;
                        timing_sense : positive_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
                        related_pin : "SET";
                }
        }
}
```

Change the value of clear_preset_var1 to H or the value of clear_preset_var1 to L.

Examples

```
Warning: Line 244, The values for clear_preset_var1 and \n
\tclear_preset_var2 in the 'libg111' cell are opposite.\n
\tThis may cause incorrect DC optimization. (LIBG-244)
```

LIBG-245

(information) Cell(%s) test scan type is %s. DFT Compiler\n \tshould be able to infer this cell during compile -scan. \n \tIt is not a black box for DFT Compiler.

Feedback

Description

Library Compilier recognizes test scan type for the scan cell according to\n its test_cell description.

What Next

report_lib also reports scan type for test scan cell.

LIBG-246

(warning) Cell(%s) test scan type is not recognized by Library Compiler. It becomes a black box for DFT Compiler.

Description

Library Compiler fails to recognize test scan type of the scan cell according to its test_cell description.

What Next

Check the signal type of each pin in test_cell description and correct it if it is wrong.

LIBG-247

(error) In test_cell of Cell(%s) clocked_on pin's polarity is opposite from the cell's definition.

Description

The test_cell's non-test mode behavior has to be consistent with what is defined in the cell section. Library Compiler detects that the clocked_on pin in test_cell has opposite polarity than the cell's defintion.

What Next

Correct test_cell's clocked_on pin's polarity to be consistent with the cell.

Examples

```
cell (TNB) {
          ff ("IQ","IQZ")  {
             next_state : " (D SCAN') + (SD SCAN) ";
             clocked_on : "CLK'";
          }
          test_cell() {
            ff ("IQ","IQZ")  {
            next_state : "D";
            clocked_on : "CLK";
          }
```

Feedback

```
        ...
    }
```

In this case the cell TNB is falling-edge triggered but its test_cell describes a rising-edge triggered flip-flop.

LIBG-248

(warning) The '%s' cell's %s groups for %s '%s' \n \tdo not cover all the states represented by the 'when' string, and the default \n \tleakage_power group is not defined for %s '%s', thus 0 will be used as \n \tthe leakage_power value for the missing states of %s '%s'.

Description

This message indicates the leakage_power information defined in a cell does not cover all the states for the power_level(power_rail value). For the missing states of the power_level, 0 will be used as the leakage_power value.

It is also used to check for related_pg_pin-based leakage_power information.

What Next

Add the missing leakage_power information for the power_level.

Examples

```
cell(AN2) {
      leakage_power () {
        power_level : "VDD1";
        when : "A";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD1";
        when : "!A";
        value : 1.5;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "A";
        value : 1.0;
      }
      ...
  }
```

In this case, the leakage_power for the state '!A' of power_level 'VDD2' is missing, . To fix the problem, add the leakage_power for the missing state in the cell group:

```
cell(AN2) {
      leakage_power () {
        power_level : "VDD1";
```

Feedback

```
        when : "A";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD1";
        when : "!A";
        value : 1.5;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "A";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "!A";
        value : 1.2;
      }
      ...
  }
```

Examples

```
Warning: Line 12, The 'AN2' cell's leakage_power groups for power_level
 'VDD2'
       do not cover all the states represented by the 'when' string, and
 the default
       leakage_power group is not defined for power_level 'VDD2', thus 0
 will be used as
       the leakage_power value for the missing states of power_level
 'VDD2'. (LIBG-248)
```

LIBG-249

(error) The '%s' cell does not specify the %s group \n \twith the 'when' string (%s) for the power_level '%s'.

Description

This message indicates the leakage_power information defined in a cell does not cover the state('when' string) for the power_level(power_rail value). For the power-level specific leakage power modeling, for each 'when' statement which appears in the leakage_power groups of a cell, there must exist a leakage_power group with that 'when' statement for every modeled power_level.

The same rule applies for the internal_power groups.

What Next

Add the missing leakage_power information for the power_level.

Feedback

Examples

```
cell(AN2) {
      leakage_power () {
        power_level : "VDD1";
        when : "AB";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD1";
        when : "!AB";
        value : 1.5;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "AB";
        value : 1.0;
      }
      ...
  }
```

In this case, the leakage_power for the state '!AB' of power_level 'VDD2' is missing, . To fix the problem, add the leakage_power for the missing state in the cell group:

```
cell(AN2) {
      leakage_power () {
        power_level : "VDD1";
        when : "AB";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD1";
        when : "!AB";
        value : 1.5;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "AB";
        value : 1.0;
      }
      leakage_power () {
        power_level : "VDD2";
        when : "!AB";
        value : 1.2;
      }
      ...
  }
```

Examples

```
Error: Line 12, The 'AN2' cell does not specify the leakage_power group
        with the 'when' string (!AB) for the power_level 'VDD2'.
 (LIBG-249)
```

Feedback

LIBG-250

(error) The logic represented by the 'when' string (%s) in this\n \t%s group is not equal to or mutually exclusive with the logic represented by\n \tthe 'when' string (%s) in the %s group on line %d.

Description

The logic represented by the 'when' string of all state-dependent or path-dependent internal_power groups between a pair of pins should be either equal or mutually exclusive for different power_levels. If it is not, Power Compiler will not be able to determine correctly which internal_power group to use when propagating a signal through the path.

What Next

Check the 'when' strings of both internal_power groups for wrong information and fix.

Examples

```
cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "S0'D0 + S0 D1";
        ...
        internal_power() {
          power_level : VDD1;
          when : "S0'D0 + S0 D1'";
          when : "D1' S0 + S0'D0 ";
          related_pin : "S0";

          power(scalar) { values ( "1.0" ); }
        }
        internal_power() {
          power_level : VDD2;
          when : "D1 S0 + S0'D0";
          related_pin : "S0";
          power(scalar) { values ( "2.0" ); }
        }
      }
    }
```

In this case, the second when attribute's string has a typographical error. It should be "D1 S0 + S0'D0'"; where the pin D0 should be ticked according to the sdf_cond attribute's string.

Feedback

Examples

```
Error: Line 258, The logic represented by the 'when' string (S0'D0 + S0
 D1') in this
       internal_power group is not equal to or mutually exclusive with
 the logic represented by
       the 'when' string (D1 S0 + S0'D0) in the internal_power group on
 line 268. (LIBG-250)
```

LIBG-251

(error) The '%s' group has conflicting 'related_pin' with the \n \t'%s' group on line %d.

Description

The "related_pin" in different internal_power groups with the same power_level of the same pin must not share pins. Similarly, the related_pin in different internal_power groups without power_level definition of the same pin must not share pins.

One exception is that, for the above 2 cases, if the pins specified in the "related_pin" of the first internal_power are all included in the "related_pin" of the second internal_power, then Library Compiler will issue LBDB-107 warning and the second internal_power will overwrite the first one.

What Next

Correct the 'related_pin' strings of both internal_power groups.

Examples

```
cell(libg44) {
      area : 2;
      pin(D1 D0 S0) {
        direction : input;
        capacitance : 1;
      }
      pin(Z) {
        direction : output;
        function : "S0'D0 + S0 D1";
        ...
        internal_power() {
          power_level : VDD1;
          related_pin : "S0";

          power(scalar) { values ( "1.0" ); }
        }
        internal_power() {
          power_level : VDD1;
          related_pin : "S0 S1";
          power(scalar) { values ( "2.0" ); }
        }
```

```
      }
    }
```

In this case, the second internal_power group's 'related_pin' conlficts with that of the first internal_power group. One fix can be that replacing the 'related_pin' of the second internal_power group from "S0 S1" to "S1".

Examples

```
Error: Line 251, The 'internal_power' group has conflicting 'related_pin'
 with the
        'internal_power' group on line 268. (LIBG-251)
```

LIBG-252

(error) The 'function' of the '%s' pin/bus on the '%s' cell\n \tis not correctly defined.

Description

This error is issued when the function is not correctly defined. A valid function statement in the sequential model must satisfy the following 2 conditions:

For a ff/latch, the noninverted is called teh first variable and the inverted output is called the second variable. A function statement of each primary output must include either the first variable or the second variable.

1. It must include and can only include the the first variable or the second variable or a the valid input pins defined for the cell in addition to the boolean operators.
2. All the component insider the function statement should be separated by a space or spaces.

What Next

Make the appropriate correction in your library, as indicated in the error message. For more information on sequential models, refer to the *Library Compiler Reference* and *User Guide Manuals*.

Examples

```
cell(libg17) {
        area : 6.50;
        pin(CLK) {
                direction : input;
                capacitance : 1.5;
        }
        pin(SET) {
                direction : input;
                capacitance : 3.0;
        }
        ff("IQ","IQN") {
```

Feedback

```
                next_state : "IQ'";
                clocked_on : "CLK";
                preset     : "SET'";
        }
        pin(Q) {
                direction : output;
                function : "IQ1";       /* wrong, should be IQ */
        }
        pin(QN) {
                direction : output;
                function : "IQN";
        }
      }
```

Examples

```
Error: Line 23, The 'function' of the 'Q'  in/bus on the 'libg17' cell
        is not correctly defined. (LIBG-252)
```

LIBG-253

(error) Cell(%s): The '%s' pin is a duplicate of '%s' internal pin.

Description

This message indicates that the specified internal pin is a duplicate of the other relative pin. For statetable-based sequential cells, the "IQ" function can only be defined in an internal pin with internal_node : "IQ".

What Next

Combine the information of the two pins into the internal pin and remove the other pin.

Examples

```
cell(libg253) {

                ...
                statetable(" CEN CLK ", " IQ  "){
                        table : "\
                        L L : - : L , \
                        H L : - : H , \
                        - H : - : N " ;
                }
                ...
                pin(IQ){
                        direction : internal;
                        internal_node : "IQ";
                        ...
                }
                pin(Y){
                        direction : output;
```

Feedback

```
                        state_function : "IQ";
                        ...
                }
                ...
        }
```

In this case, internal pin IQ and pin Y are duplicate. The correct model should be:

cell(libg253) {

... statetable(" CEN CLK ", " IQ "){ table : "\ L L : - : L , \ H L : - : H , \ - H : - : N " ; } ... pin(IQ){ direction : output; internal_node : "IQ"; ... } ... }

Examples

```
Warning: Line 139, Cell(libg253): The pin 'SOSV' is a duplicate of the
 'IQ' internal pin. (LIBG-253)
```

LIBG-254

(error) An invalid '%s' %s string in the '%s' cell.

Description

The string given is not valid for representing a boolean logic defined in Synopsys format.

What Next

Refer to your Library Compiler Reference Manual to find out the valid format of the string. It is described in the "function simple attribute" under the "Cell Group Description and Syntax".

Examples

```
cell(sample) {
  switch_cell_type : coarse_grain;
  area : 1 ;
  pg_pin ("VVDD") {
        pg_type : internal_power;
        pg_function : "(IO" ;
  }
  ...
```

In this simple case, the closing parenthesis is missing in the function string.

Examples

```
Error: Line 400, An invalid '(IO' pg_function string in the 'sample'
 cell. (LIBG-254)
```

Feedback

LIBG-255

(error) A bad '%s' pg_pin name in the '%s' cell.

Description

The error gets detected during the *read_lib*, *update_lib*, and *check_library* commands. This error occurs when either the pg_pin name is not found or an incorrect pin name in one or more attributes of the pin group is detected. The pg_pin group is not recognized and the pin name is labeled as bad.

What Next

Check your library for an incorrect pin name in a related attribute or for an incorrect pin group.

Examples

```
cell (libg3) {
    pg_pin(VSS) {
        pg_type : primary_power;
        voltage_name : VSS;
    }
    pg_pin(VDD) {
        pg_type : primary_power;
        voltage_name : VDD;
    }
    pg_pin(VVDD) {
        pg_type : internal_power;
        voltage_name : VDD1;
        pg_function : "E";       /* <-- This is wrong */
    }
 }
```

Examples

```
Error: Line 426, A bad 'E' pg_pin name in the 'libg3' cell. (LIBG-255)
```

LIBG-256

(error) The '%s' group is overlapping with the '%s' group on line %d.

Description

This message indicates that two *dynamic_current* groups in ccs power are overlapping with each other.

Feedback

If following three conditions is true, then two groups are considered to be overlapped :

1. Two groups have at least one pin specified in *related_inputs* attribtue is identical.
2. Both have same list of pins specified in *related_outputs* or both have no *related_outputs* attribtue.
3. *When* atrributes specified in both groups are not mutually exclusive, or both groups have no *when* attribute.

What Next

Check *related_inputs*, *related_outputs*, and *When* attributes for all *dynamic_current* groups to see if any of them breaks above rules, and make the necessary correction.

Examples

```
cell(libg256) {
  ...
  pin(A1) {
    direction : input;
    ...
  }
  pin(A2) {
    direction : input;
    ...
  }
  pin(A3) {
    direction : input;
    ...
  }
  pin(A4) {
    direction : input;
    ...
  }
  pin(A5) {
    direction : input;
    ...
  }
  pin(ZN1) {
    direction : output;
    ...
  }
  pin(ZN2) {
    direction : output;
    ...
  }
  ...
  dynamic_current() {
    when : "A2";
    related_inputs : "A5 A4";
    related_outputs : "ZN2 ZN1";
    switching_group() {
```

Feedback

```
      pg_current(V2) {
      ...
      }
      ...
    }
  }
  dynamic_current() {
    when : "!A1";
    related_inputs : "A4 A3";
    related_outputs : "ZN1 ZN2";
    switching_group() {
      pg_current(V2) {
      ...
      }
      ...
    }
  }
  ...
```

In this case, "A2" and "!A1" specified in two when attributes respectively are not mutually exclusive, pin "A4" is specified in both related_inputs groups, and same list of pins ("ZN1" and "ZN2") is specified in both related_outputs groups. Two dynamic_current are overlapping. You can modify any of these attributes to fix the problem. For example : change "A4 A3" to "A2 A3".

Examples

```
Error: Line 79, The 'dynamic_current' group is overlapping with the
 'dynamic_current' group on line 88. (LIBG-256)
```

LIBG-257

(error) The %s must be set to 0.0 or omitted.

Description

There are two attributes, input_high_value and input_low_value, within a gate_leakage group. The input_high_value is to specify gate leakage current on a pin when this pin is set to high. The input_low_value is to specify gate leakage current on a pin when this pin is set to low. If the 'when' statement inside leakage_current or va_leakage_current implies that the pin high never occurs, then input_high_value shall be set to 0.0 or ignored. If the 'when' statement implies that the pin low shall never occur, then input_low_value must be set to 0.0 or ignored.

What Next

Check *input_low_value* and *input_high_value*, and make the necessary correction.

Feedback

Examples

```
leakage_current() {
     when : "A1 & A2 & !ZN";
     ...
     gate_leakage(A2) {
       input_high_value : 2.1;
       input_low_value : -1.7;
     }
     gate_leakage(A1) {
       input_high_value : 7.1;
       input_low_value : -8.7;
     }
  }
```

In this case, we have when condition "A1 & A2 & !ZN", which means pins A1 and A2 shall never set to low because they will never occur within this leakage_current. So, input_low_value is meaningless for both pins. We shall set both to 0.0 or comment them out.

Examples

```
Error: Line 210, The input_low_value must be set to 0.0 or omitted.
 (LIBG-257)
```

LIBG-258

(error) No %s is allowed within an intrinsic_parasitic\n \tif power_cell_type is %s.

Description

If the power_cell_type is macro, then followings groups can't be specified within an intrinsic_parasitic : state-dependent condition, intrinsic_resistance and intrinsic_capacitance.

If the power_cell_type is standard cell or there is no power_cell_type specified, then total_capacitance can't be specified within an intrinsic_parasitic.

What Next

Check the library source file, and make the necessary correction.

Examples

```
cell (test) {
  intrinsic_parasitic() {
    when : "!A1 & A2 & !ZN";
    total_capacitance(V2) {
       value : 9.0;
    }
  }
```

Feedback

```
 ...
}
```

In this case, there is no power_cell_type specified under cell "test", meaning power_cell_type is defaulted to standard cell. The total_capacitance is not allowed within an intrinsic_parasitic group.

```
cell (test) {
  power_cell_type : macro;
  intrinsic_parasitic() {
    when : "!A1 & A2 & !ZN";
    intrinsic_resistance(G1) {
       related_output : "ZN";
       value : 9.0;
    }
    intrinsic_capacitance(G1) {
       value : 8.2;
    }
  }
 ...
}
```

In this case, 'when' attribute, 'intrinsic_resistance' and 'intrinsic_capacitance' are not allowed in an 'intrinsic_parasitic' group because the 'power_cell_type' is 'macro'.

Examples

```
Error Line 272, No intrinsic_resistance is allowed within an
 intrinsic_parasitic
        if power_cell_type is macro. (LIBG-258)
```

LIBG-259

(error) The power_cell_type must be macro if\n \tmin_input_switching_count and max_input_switching_count are defined.

Description

If min_input_switching_count and max_input_switching_count are defined within switching_group, then power_cell_type defined in cell must be macro.

What Next

Check the library source file, and make the necessary correction.

Examples

```
cell (test) {
 ...
 power_cell_type : stdcell;
 dynamic_current() {
   ...
```

```
   switching_group() {
      min_input_switching_count : 1;
      max_input_switching_count : 9;
      ...
   }
   ...
 }
 ...
}
```

In this case, min_input_switching_count and max_input_switching_count both are defined under one of switching_group groups within a dynamic_current, and power_cell_type is standard cell, which is wrong. We shall change "stdcell" to "macro" to avoid the error.

Examples

```
Error Line 272, The power_cell_type must be macro if
        min_input_switching_count and max_input_switching_count are
 defined. (LIBG-259)
```

LIBG-260

(error) The logic represented by the %s string is not equal\n \tto or mutually exclusive with the logic represented by the %s string.

Description

The logic represented by one programmable driver type string must be not equal to or mutually exclusive with the logic represented by other programmable driver types under the same pin.

Examples

```
cell(libg260) {
     pad_cell : true;
     ...
      pin(A1) {
       direction : input;
       is_pad : true;
      ...}
      pin(A2) {
       direction : input;
       ...}
      pin(A3) {
        direction : input;
       ...}
      pin(ZN1) {
       direction : inout;
       max_capacitance : 0.1;
       pull_up_function : "!A1 * !A2 * !A3";
       pull_down_function : "A1 * A2 * !A3";
```

Feedback

```
        bus_hold_function : "A1 * !A2 * !A3";
        open_drain_function : "!A1 * A2 * !A3";
        open_source_function : "!A1 * !A2 * A3";
        resistive_function : "A1 * A2 * A3";
        resistive_0_function : "A1 * A2";
        resistive_1_function : "!A1 * A2 * A3";
       ...}
    }
```

In this case, the resistive_0_function is not mutually exclusive with pull_down_functioni and resistive_function. To fix the problem, you might want to change it as following :

resistive_0_function : "A1 * !A2 * A3";

Examples

```
Error: Line 102, The logic represented by the resistive_0_function string
 is not equal
        to or mutually exclusive with the logic represented by the
 pull_down_function string. (LIBG-260)
Error: Line 102, The logic represented by the resistive_0_function string
 is not equal
        to or mutually exclusive with the logic represented by the
 resistive_function string. (LIBG-260)
```

LIBG-261

(error) The programmable driver type can only be defined on a pad cell.

Description

The programmable driver type can only be defined a pad cell, which has either pad_cell or auxiliary_pad_cell attribute.

What Next

Check the library source file, and make the necessary correction.

Examples

```
cell (libg261) {
    ...
    pin (A) {
      direction : input;
      pull_up_function : "p1 * p2";
      ...
    }
   ...}
```

In this case, a programmable driver type, pull_up_function, is defined on pin A, which is under a cell, ligb261. The cell is not a pad cell, which is wrong. To fix the problem, please

Feedback

either add pad_cell attribute under cell level or remove pull_up_function attribute from the pin.

Examples

```
Error: Line 94, The programmable driver type can only be defined on a pad
 cell. (LIBG-261)
```

LIBG-262

(information) Cell(%s) is recognized as one-hot mux cell.

Description

This message is issued when a cell is recognized as one-hot mux cell.

One-hot mux cells have following characteristic: 1. Two equal sized, disjoint sets of input pins, one is select pins(e.g. "S0,S1"), another set is data input pins(e.g. "D0,D1"). 2. Have cell attribute "contention_condition", e.g. Fc = S0'*S1 + S0*S1. That is there could be one and ONLY one select pin can be logic 1, others are logic 0. 3. There is only one output pin defined and its function is defined with respect to all of its inputs, e.g. Fo = S0*D0 + S1*D1;

What Next

The one-hot mux cell will be used in DC logical synthesis.

Examples

```
cell(OHMUX2) {

  ...
  contention_condition : "( S0 S1 + S0' S1' )";
  pin(D0) {
    direction : input;
    capacitance : 1;
  }
  pin(D1) {
    direction : input;
    capacitance : 1;
  }
  pin(S0) {
    direction : input;
    capacitance : 1;
  }
  pin(S1) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
```

Feedback

```
    function : "(S0 D0 + S1 D1)";
    ...
  }
}
```

Examples

```
Warning: Line 139, Cell(OHMUX2) is recognized as one-hot mux
 cell.(LIBG-262)
```

LIBG-263

(warning) Cell(%s) is not recognized as one-hot mux cell.

Description

This message is issued when there is cell level attribute "contention_condition" defined, but it does not match with output pin function as a one-hot mux cell.

One-hot mux cells have following characteristic: 1. Two equal sized, disjoint sets of input pins, one is select pins(e.g. "S0,S1"), another set is data input pins(e.g. "D0,D1"). 2. Have cell attribute "contention_condition", e.g. Fc = S0'*S1 + S0*S1. That is there could be one and ONLY one select pin can be logic 1, others are logic 0. 3. There is only one output pin defined and its function is defined with respect to all of its inputs, e.g. Fo = S0*D0 + S1*D1;

This warning message is reported in step 3, when it find the output function with restiction of contention function does not match with the function of one-hot mux cell.

What Next

If users intend to define the cell as one-hot mux cell, and use it later on in logical synthesis, check the cell contention_condition definition and output pin function, modify to make them match the definition of one-hot mux cell.

If users won't use the cell as one-hot mux cell, just ignore this warning.

Examples

```
cell(OHMUX2) {

  ...
  contention_condition : "( S0 S1 + S0' S1' )";
  pin(D0) {
    direction : input;
    capacitance : 1;
  }
  pin(D1) {
    direction : input;
    capacitance : 1;
  }
```

```
  pin(S0) {
    direction : input;
    capacitance : 1;
  }
  pin(S1) {
    direction : input;
    capacitance : 1;
  }
  pin(Z) {
    direction : output;
    function : "(S0 D0 + S1 D1 + D0' D1)";
    ...
  }
}
```

In this case, the contention function matches with one-hut mux cell select pin restriction, but the output pin function is not a function of one-hot mux cell.

Examples

```
Warning: Line 139, Cell(OHMUX2) is not recognized as one-hot mux
 cell.(LIBG-263)
```

LIBG-264

(warning) ICG cell '%s' function can not be recognized during functional optimization by Power Compiler.

Description

A cell with attribute "clock_gating_integrated_cell" defined as "generic" is called a generic ICG cell.

Library Compiler will try to resolve ICG type of a generic ICG cell. Valid resolved types are,

latch_(posedge | negedge | posedgeactivelow | negedgeactivelow)_ (precontrol | postcontrol| *)_(obs | *)_(invgclk | *) or none | (posedge | negedge | posedgeactivelow | negedgeactivelow)_ (control | *)_(invgclk | *).

Please refer to Library Compiler User Guide for the corresponding schematics of these types.

If a generic ICG cell can't be resolved as any exact type, Library Compiler will resolve them as blackbox. It means this generic ICG will not be auto inferred by Power Compiler and understood by Formality and other client tools that need to understand the function of such cells.

FF-based ICG cell won't be supported by Power Compiler, either.

Feedback

What Next

Change the cell to be one of the valid ICG types.

Examples

```
Warning: ICG cell 'cell1' function can not be recognized during
 functional optimization by Power Compiler. (LIBG-264)
```

LIBG-265

(information) Derived ICG type for cell '%s' is '%s'.

Description

A cell with attribute "clock_gating_integrated_cell" defined as "generic" is called a generic ICG cell.

Library Compiler will try to resolve ICG type of a generic ICG cell. If successful, the value of attribute "clock_gating_integrated_cell" will be updated.

Examples

```
Information: Derived ICG type for cell 'cell1' is 'latch_posedge'.
 (LIBG-265)
```

LIBG-266

(warning) The 'data_in_type' attribute on the '%s' pin/bus in\n \tthe '%s' cell is inconsistent with its function. The attribute is ignored.

Description

This warning message occurs when the *data_in_type* attribute does not match the functional information specified in the cell's sequential state description.

In a pin group, *data_in_type* defines the type of *data_in* attribute to be used in an ff group, a seq group, or a ff_bank group. Any pin with the *data_in_type* attribute must be in the *data_in* function. The tool performs a consistency check between the pin's *data_in_type* attribute and the *data_in* function and generates this warning when inconsistencies are found.

What Next

This is only a warning message. No action is required.

However, to avoid this warning, check your library for a pin that has a *data_in_type* attribute but is not used in the *data_in* statement of a sequential group. After making your changes, run the command again.

Feedback

Examples

```
Warning: Line 153, The 'data_in_type' attribute on the 'SET' pin/bus in
        the 'libg35' cell is inconsistent with its function. The
 attribute is ignored. (LIBG-266)
```

LIBG-267

(error) The power_down_function attribute should not be specified inside the test_cell's ff/latch/statetable group.

Description

This error message occurs because the *power_down_function* attribute must be specified in a cell's ff/latch/statetable group, not specified inside the test_cell.

What Next

Check your library to delete the *power_down_function* attribute in test_cell.

Examples

The following example results in this error message:

```
test_cell () {
         pin (Q) {
            direction : output;
            function : "IQ";
            signal_type : test_scan_out;
         }
         pin (CK) {
            direction : input;
         }
         pin (D) {
            direction : input;
         }
         pin (SI) {
            direction : input;
            signal_type : test_scan_in;
         }
         pin (SE) {
            direction : input;
            signal_type : test_scan_enable;
         }
         ff (IQ,IQN) {
            clocked_on : "!(CK)";
            next_state : "D";
            power_down_function : "!VDD + VSS"; /* <-- This is wrong */
         }
      }
```

Feedback

Examples

Error: Line 426, Cell 'test', The power_down_function attribute should not be specified inside the test_cell's ff/latch/statetable group. (LIBG-267)

LIBG-268

(error) A function cannot point to two different flip-flop or latch groups.

Description

This error message occurs when the Boolean expression in the *function* attribute of this pin contains more than one internal node of flip-flop or latch. Only one internal node is allowed.

What Next

Specify individual internal nodes separately as shown in the following example:

```
pin(temp) {
   direction :internal;
   function : "Q1";
   reference_input : "RET CK q1";
   ...
pin(Q) {
   direction : output;
   function : "Q2 + temp";
   reference_input : "RET CK q1";
   ...
}
```

LIBG-269

(error) The '%s' has a count of %d, which does not match\n \tthe size %d specified.

Description

This error message occurs when the specification of the total number of reference_input is not matched to total number of internal nodes specified in ff/latch/ff_bank/latch_banck group.

What Next

Check the library source file and correct the problem by grouping the values together in the required format.

LIBG-270

(error) The variable in the Boolean expression is not allowed.

Feedback

Description

This error message occurs because some variables, such as IQ or IQN, in flip-flop or latch groups cannot be specified in a functional expression if the group is referred by reference_input defined in the pin.

What Next

Check the library source file, and correct the problem by grouping the values together in the required format.

Examples

In the following example, latch 1 is referred by 2 pins, internal_1 and internal_2. That means the variables IQ_0 and IQN_0 can be referred by either the internal_1 or internal_2 pin. In latch 2, data_in is connected to IQ_0, which is not allowed because it could be either the internal_1 or internal_2 pin.

```
pin(output_1) {
    direction : "output";
    function : "IQ_1";
    reference_input : "IQ_0";
  }
  pin(internal_1) {
    direction : "internal";
    function : "IQ_0";
    reference_input : "D CP";
  }
  pin(internal_2) {
    direction : "internal";
    function : "IQ_0";
    reference_input : "D1 CP1";
  }
  latch ("p1 p2","IQ_0","IQN_0") {   /* latch 1 */
     data_in : "p1";
     enable : "p2";
  }
  latch ("p1", "IQ_1","IQN_1") {     /* latch 2 */
     data_in : "p1";
     enable : "CP";
  }
```

Examples

```
Error: Line 160, The variable in boolean expression is not allowed.
 (LIBG-270)
```

LIBG-271

(warning) The disable value of the retention pin might not be valid.

Feedback

Description

This warning message occurs because the disable value that you provided might be incorrect. The tool ties up the disable values from all logic expression functions to see if the results are reasonable.

What Next

Check the library source file to see if the disable value is valid.

Examples

The following example shows that data_in becomes logic "0" when the RESTORE pin is tied up to disable value "0". The 2 valid pins in data_in are "D" and "RESTORE". The expected data_in after tie up to the disable value is "D", not logic "0". So, in this case, the tool issues the warning message because it is possible that the disable value might be invalid.

```
pin (RESTORE) {
    direction : "input";
    retention_pin("restore",0);
    ...
  }
  pin (D) {
    direction : "input";
    ...
  }
  latch ("IQ","IQN") {
     data_in : "D * RESTORE";
     ...
  }
```

Examples

```
Warning: Line 160, The disable value of retention pin might not be valid.
(LIBG-271)
```

LIBG-272

(information) Library '%s' is being compiled with pin_number recomputation enabled.

Description

The pin number of the cells in this library will be assigned by a consistent rule, so the pin number can be assigned consistently when the cells are logically equal but have different function expression or pin orders in .lib are different.

Examples

```
Information:  Library 'lib_example' is being compiled with pin_number
 recomputation enabled.(LIBG-272)
```

Feedback

LIBG-273

(error) the logic represented by the %s string \n \t(%s) is not mutually exclusive with the logic represented by\n \tthe %s string (%s) on line %d.

Description

The logic represented by the clamp_*_function and illegal_clamp_condition string should be mutually exclusive. If it is not, Library Compiler is not be able to determine which value the cell will clamp to.

What Next

Check the clamp_*_function and illegal_clamp_condition strings of both timing groups for wrong information and fix.

Examples

```
cell(libg273) {
      area : 2;
      ...
      pin(Z) {
        direction : output;
        function : "S0'D0 + S0 D1";
        clamp_0_function : "D0";
        clamp_1_function : "D0";
        clamp_latch_function : "!D0";
        ...
      }
    }
```

In this case, the clamp_0_function string is not exclusive with clamp_1_function string.

Examples

```
Error: Line 258, Cell 'libg273', pin 'Z', the logic represented by the
clamp_0_function string (D0) is notmutually exclusive with the logic
 represented
by the clamp_1_function string (D0) on line 268. (LIBG-273)
```

LIBG-274

(error) You are not allowed to specify the function attribute on the single-bit output pin of the test_cell group of a parallel sequential cell.

Description

In parallel sequential cells, the single-bit output pin is only a test output pin. Therefore, do not specify the *function* attribute on this pin, in the *test_cell* group.

This message identifies a parallel sequential cell that has a single-bit output pin with the *function* attribute.

What Next

Check your library, and delete the *function* attribute specified on the single-bit output pin.

Examples

```
cell (LSFDS) {

  ...

  test_cell() {
    bus (D) {
      bus_type : BUS4;
      direction : input ;
      capacitance : 2.000000 ;
    }
    pin (CK) {
      direction : input ;
      capacitance : 1.000000 ;
    }
    ff_bank (IQ,IQN,4) {
      next_state : "D" ;
      clocked_on : "CK" ;
    }
    bus (Q) {
      bus_type : BUS4;
      direction : output ;
      function : "IQ" ;
    }
    pin (SO) {
      direction : output ;
      signal_type : "test_scan_out";
      function : "IQ[3]" ;
    }
  }
}
```

In this example, the *function* attribute should not be defined on the pin 'SO'.

Examples

```
Error: Line 302, Cell 'test', You are not allowed to specify the function
 attribute on the
single-bit output pin of the test_cell group of a parallel sequential
 cell. (LIBG-274)
```

Feedback

LIBG-275

(information) Complex function sequential cell will skip\n sequential cell timing consistency check.

Description

This message is to infer user that a complex function seuqential cell\n which contains mux/xor/maj with Boolean logic\n will skip sequential cell timing consistency check.

What Next

The cell timing consistency need to be checked by user.

Examples

```
cell (test) {

    ...

    ff(IQ,IQN) {
      clocked_on : "CK" ;
      next_state : "RETN & ((SE SI) + (!SE D))" ;
    }
}
```

Examples

```
Information: Line 118, Cell 'SDRFFQ_X1M_A12TR', Complex function
 sequential cell will skip sequential cell timing consistency check.
 (LIBG-275)
```

LIBG-276

(error) Port '%s', only one %s can be the synchronized load enable pin in the cell.

Description

The synchronized load enable pin is the pin with attribute *nextstate_type : load*. A synchronized load enable register cell should have only one load enable pin. So only one pin/bus/bundle should be specified with this attribute.

This message identifies a sequential cell that has more than one pin/bus/bundle being specified with attribute *nextstate_type : load*.

What Next

Check your library, and correct the *nextstate_type : load* attribute specified on the wrong pin.

Feedback

Examples

```
cell (test) {

  ...

  ff (IQ,IQN) {
      next_state : "E*D + !E*IQ" ;
      clocked_on : "CK" ;
  }
  pin (D) {
      direction : input ;
      nextstate_type : load ;
  }
  pin (E) {
      direction : input ;
      nextstate_type : load ;
  }
  pin (CK) {
      direction : input ;
      capacitance : 1.000000 ;
  }
  bus (Q) {
      direction : output ;
      function : "IQ" ;
  }
}
```

In this example, the *nextstate_type : load* attribute should not be defined on the pin 'D', only pin 'E' should have this attribute.

Examples

```
Error: Line 302, Cell 'test', Only one pin/bus/bundle can be the
 synchronized load enable pin in the cell. (LIBG-276)
```

LIBG-277

(warning) The port '%s' is not working as a synchronized load enable pin,\n \tthe cell can not be degenerated into non-synchronized load enable register cell.

Description

The synchronized load enable(SLE) pin is the pin with attribute *nextstate_type : load*. When SLE pin is active, the register allows new values to load at the data input. When SLE pin is inactive, the register output is holding unchanged.

So when the load enable pin is at inactive level, the simplified next_state should be a Boolean expression with IQ; when the load enable pin is at active level, the simplified next_state should be a Boolean expreassion without IQ, but not tie to "1" or "0".

This message identifies the SLE pin doesn't satisfy the above conditions.

What Next

Check your library, and correct the "next_state" attribute or the SLE pin.

Examples

```
cell (test) {

  ...

  ff (IQ,IQN) {
      next_state : "E*D + IQ" ;
      clocked_on : "CK" ;
  }
  pin (D) {
      direction : input ;
      nextstate_type : data ;
  }
  pin (E) {
      direction : input ;
      nextstate_type : load ;
  }
  pin (CK) {
      direction : input ;
      capacitance : 1.000000 ;
  }
  bus (Q) {
      direction : output ;
      function : "IQ" ;
  }
}
```

In this example, the *next_state* attribute should be correct to "E*D + !E*IQ"

Examples

```
Warning: Line 302, Cell 'test', The port 'E' is not working as a
 synchronized load enable pin, the corresponding non-SLER degenerated
 model can’t be generated. (LIBG-277)
```

LIBG-278

(warning) The sequential element %s variable '%s' is unused in the cell function,\n \tthe '%s' attribute should not be specified and will be removed.

Description

This message indicates the sequential cell has both clear_preset_var1 and clear_preset_var2, but one of them is unused and will be removed from the library.

Feedback

If the sequential element second var (e.g. IQN) is unused in cell function, then we don't need clear_preset_var2 to be specified. If the sequential element first var (e.g. IQ) is unused in cell function, then we don't need clear_preset_var1 to be specified.

You will get this message if you specify the unused clear_preset_var, and it will be removed in the process.

The following example shows an instance where this message occurs:

```
cell(libg278) {
        area : 11;
        pin(D) {
                direction : input;
                capacitance : 1;
        }
        pin(CP) {
                direction : input;
                capacitance : 1;
        }
        pin(CLR) {
                direction : input;
                capacitance : 1;
        }
        pin(SET) {
                direction : input;
                capacitance : 1;
        }
        ff("IQ","IQN") {
                next_state : "D";
                clocked_on : "CP";
                clear   : "CLR'";
                preset   : "SET'";
                clear_preset_var1 : L;
                clear_preset_var2 : L;  /* this is unsed as IQN is unused
 */
        }
        pin(Q) {
                direction : output;
                function : "IQ";
                timing() {
                        timing_type : rising_edge;
                        intrinsic_rise : 1.0;
                        intrinsic_fall : 1.0;
                        rise_resistance : 0.1;
                        fall_resistance : 0.1;
                        related_pin : "CP";
                }
                timing() {
                        timing_type : clear;
                        timing_sense : positive_unate;
                        intrinsic_fall : 1.0;
                        fall_resistance : 0.1;
```

Feedback

```
                related_pin : "CLR";
        }
        timing() {
                timing_type : preset;
                timing_sense : negative_unate;
                intrinsic_fall : 1.0;
                fall_resistance : 0.1;
                related_pin : "SET";
        }
    }
}
```

The following is an example message:

```
Warning: Line 111, The sequential element second variable 'IQN' is unused
 in the cell function,\n
\tthe 'clear_preset_var2' attribute should not be specified and will be
 removed. (LIBG-278)
```

What Next

Edit the .lib and remove the unused clear_preset_var1/var2

LIBG-280

(information) The cell '%s' contiains memory/memory_read/memory_write groups which are deprecated, use the is_memory_cell attribute instead.

Description

The groups are now obsolete and are no longer used by Synopsys tools. Use is_memory_cell attribute for memory cell. For example: cell (my_memory_cell) { is_memory_cell : true ; }

By default, bypass the checking for the groups(memory/memory_read/memory_write) for the same reason. Set the gvar lc_enable_memory_group_check to true to bring back the checking.

What Next

Remove the deprecated groups(memory/memory_read/memory_write) and add is_memory_cell attribute for the cell.

LIBSETUP

LIBSETUP-001a

(information) The cell %s with library cell %s is a %s.

Description

This information message appears after a LIBSETUP-001 message occurs. The message informs you of the type of the specified cell. The cell can be any of the following:

- `isolation cell`
- `level-shifter cell`
- `switch cell`
- `retention register cell`
- `normal cell`

The normal cells are not power-design specific cells, which includes standard cells and macro cells.

What Next

This is an information-only message. No action is required.

See Also

- MV-001

LIBSETUP-001b

(information) The cell %s(%s) has %s.

Description

This information message appears after a LIBSETUP-001 message occurs. The message helps to identify the cause of the earlier LIBSETUP-001 message. It reports the pg_pins whose voltage values do not match with the voltage of the connected supply net. The message also reports the pg_pins for which a matching operating condition voltage or a supply net to match voltage levels could not be identified.

What Next

Check the exception connections for the cell. You should connect the correct supply net so that the voltage between the pg_pin and supply net matches. Please check the set_voltage and the connect_supply_net commands and make sure that the voltage specified for the supply net matches the voltage specified for the pg_pin in the library.

Feedback

Examples

```
Information: The cell a(macro_cell) has pg_pin (VDD, 0.900000) driven by
 supply net (vdd_sn, 1.300000). (LIBSETUP-001b)

Information: The cell a(macro_cell) has pg_pins (VDD2, 1.080000), (VDD,
 0.900000) driven by supply net (vdd_sn, 1.300000). (LIBSETUP-001b)

Information: The cell pad_in(od_pd) has pg_pin (VDD, 3.500000) driven by
 supply net (VDD1, 1.650000), pg_pin (VDD3, 3.900000) driven by supply
 net (VDD2, 0.900000) and pg_pin (VDDL, 2.100000) with no matching
 operating condition voltage or have no supply net to match the voltage
 level. (LIBSETUP-001b)
```

See Also

- LIBSETUP-001
- report_lib
- report_supply_net

LIBSETUP-001c

(information) The cell %s(%s) has %s.

Description

This information message appears after a LIBSETUP-001 message occurs. The message helps to identify the cause of the earlier LIBSETUP-001 message. It reports the input_signal_level of the cell whose voltage value do not match with the related supply net. The message also reports the input_signal_level for which a matching operating condition voltage or a supply net to match voltage level could not be identified.

What Next

Please check the set_voltage and set_operating_conditions commands and make sure that the driver supply voltage matches the voltage of input_signal_level of the cell.

Examples

```
Information: The cell a(macro_cell) has signal_level (VDD2, 1.900000)
 which do not match the voltage level of the supply net (PNT, 1.300000).
 (LIBSETUP-001c)

Information: The cell a(macro_cell) has signal_levels (VDD3, 1.900000),
 (VDD2, 1.500000) which do not match the voltage level of the supply net
 (PNT, 1.300000). (LIBSETUP-001c)
```

Feedback

```
Information: The cell b_UPF_ISO_0(LSUPENX8) has signal_levels (VL,
 0.700000), (VH, 1.080000) with no matching operating condition voltage
 or have no supply net to match the voltage level. (LIBSETUP-001c)
```

See Also

- LIBSETUP-001
- report_lib
- report_supply_net

LIBSETUP-001

(warning) cell %s(%s) was constrained to operate under the operating\n \tcondition %s, \n \tbut the library cell %s matching this characterization has not been\n \tused. Instead, library cell %s\n \tfrom %s:%s (voltage = %s, process = %s, temperature = %s)\n \thas been used. %s

Description

This warning message occurs when the specified block or cell has been required to operate under a certain supply voltage (using the *set_operating_conditions* command), but this particular cell cannot be linked to a library cell that was characterized under this supply voltage.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, check the operating condition for the specified block or cell. Set the proper operating condition using the *set_operating_conditions* command or check the library.

See Also

- set_operating_conditions
- set_voltage

LIBSETUP-010a

(warning) The target_library_subset -clock_path %s does not contain an inverter characterized for operating condition %s.

Feedback

Description

This warning message occurs because for a multivoltage design it is required that each target_library_subset that is set on clock_path has an inverter that is characterized for the operating conditions of the instances. In absence of that the clock path logic will be mapped to default library cells.

What Next

Make sure the library characterized for the operating condition is included in the target library subset, and add an inverter to the library for that operating condition if none exists.

See Also

- report_target_library_subset
- set_target_library_subset

LIBSETUP-010

(error) The target_library_subset %s does not contain an inverter characterized for operating condition %s.

Description

This error message occurs because for a multivoltage design it is required that each target library subset that is set on instances has an inverter that is characterized for the operating conditions of the instances.

What Next

Make sure the library characterized for the operating condition is included in the target library subset, and add an inverter to the library for that operating condition if none exists.

See Also

- report_target_library_subset
- set_target_library_subset

LIBSETUP-011a

(warning) The target_library_subset -clock_path %s does not contain all required gates for the operating condition %s. Either a NOR, or an AND and an OR gate (two-input) is required for mapping.

Feedback

Description

This warning message occurs because when performing mapping, it is required that each target_library_subset that is set on clock_path have at least the minimum set of gates. In absence of that the clock path logic will be mapped to default library cells.

What Next

Add all the required gates to the target_library_subset and run the command again.

See Also

- report_target_library_subset
- set_target_library_subset

LIBSETUP-011

(error) The target_library_subset does not contain all required gates for the operating condition %s. Either a NOR, or an AND and an OR gate (two-input) is required for mapping.

Description

This error message occurs because when performing mapping, it is required that each target_library_subset that is set on instances have at least the minimum set of gates.

What Next

Add all the required gates to the target_library_subset and run the command again.

See Also

- report_target_library_subset
- set_target_library_subset

LIBSETUP-012

(error) Library filename '%s' specified in target library subset on cell '%s' is not in global target library list.

Description

This error message occurs because all libraries specified using *set_target_library_subset* command must be listed in the global target library list.

What Next

Either add the specified libraries to the *target_library* TCL variable, or remove them from the target_library_subset.

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

LIBSETUP-013

(error) There is a mismatch between the target library subset and the operating condition specified on cell '%s'.

Description

This error message occurs because there must be at least one library in the defined target_library_subset on a block which has nominal process, voltage and temperature (PVT) the same as the PVT parameters of the operating condition defined on that block.

What Next

Either modify the target_library_subset that is defined on that particular block or modify the operating condition on that block.

See Also

- report_target_library_subset
- set_operating_conditions
- set_target_library_subset

LIBSETUP-014

(warning) The library cell of cell %s is not from the target_library_subset being used on that block.

Description

This warning message occurs because the target_library_subset defined on a block is used when a new cell is created during optimization. Existing mapped cells are not required to come from this subset. However, the *check_target_library_subset* command issue this message to advise you that such a situation exists.

Feedback

What Next

This is only a warning message. No action is required.

However, based on your requirements, you can either ignore the message, modify the target_library_subset on the block, or manually translate that cell to use a library cell from the target_library_subset.

See Also

- report_target_library_subset
- set_target_library_subset

LIBSETUP-015

(Information) Relaxed pvt matching is enabled for power domain %s.

Description

The information appears when all the required matching opcond libraries are not available for specified power domain. DE shell ignores the library setup problem, and invokes relaxed pvt matching to help compile_exploration not to abort because of LIBSETUP problems.

LIBSETUP-016

(Information) Only pre-instantiated cells are considered as part of relax_pvt support.

Description

The information appears when all the required matching opcond libraries are not available for specified power domain. DE shell ignores the library setup problem, and invokes relaxed pvt matching to help linker not to issue LIBSETUP-001 and link to a non-matching opcond cell.

LIBSETUP-017

(Information) Relax pvt data computed during compile_exploration is reused for power domains %s.

Description

The information appears when all the required matching opcond libraries were not available for specified power domain during compile_exploration. Relaxed pvt matching was invoked to help not aborting compile_exploration in DE. Same relaxed pvt settings are used after compile_exploration.

Feedback

LIBSETUP-018

(Information) Relax pvt data is outdated because of link_library change.

Description

The information appears when user has updated link_library variable. Relaxed pvt data is re-compute.

LIBSETUP-022

(Error) A total of %s operating condition problems %s; %s Delay calculation will be incorrect if these problems are not fixed. %s

Description

This is a summary message for a number of operating condition problems detected in the design linking, check_mv_design, or compile/physopt commands. It tells you how many operating condition problems have been detected by the tools, and what libraries have been searched in a prior attempt to link the design.

What Next

Check the operating condition for the particular block or cell. Set the proper operating condition using the *set_operating_conditions* command or check the library.

See Also

- set_operating_conditions

LIBSETUP-024

(error) Found '%d' occurrence(s) of target library subset specification(s) with conflicting operating conditions.

Description

This error message provides the number of target library subset specifications that conflict with the operating conditions specified on their respective blocks. The conflict occurs if none of the libraries in a target library subset has nominal process, voltage and temperature values (PVT values) that agree with the PVT values specified in the operating condition.

Feedback

What Next

Run the *check_target_library_subset* command to get details on incorrect target library subset specifications. Then make sure each specification has at least one library that matches the operating condition specified on the block.

See Also

- report_target_library_subset
- set_operating_conditions
- set_target_library_subset

LIBSETUP-025

(warning) You have used set_target_library_subset, but the design already contains %d cells mapped to libraries outside the subset. The target_library_subset will apply to new cells created or modified during optimization.

Description

This warning message occurs because prior to optimization, your design already contains some cells that are mapped to libraries outside of the target_library_subset you requested.

Depending on your requirements, this may or may not be a problem.

The target_library_subset only affects cells that are created or modified during optimization. Existing mapped cells are not required to come from this subset.

If you are getting this message, and did not want to allow existing cells to be mapped to libraries outside the subset, you need to manually translate those cells using the *change_link* command, or recompile the block on its own using a more restrictive $target_library. This situation should not arise if you set the target_library_subset prior to the initial compile from RTL.

What Next

This is only a warning message. No action is required.

Based on your requirements, you may ignore the message, or you may need to manually translate existing cells. Use the *check_target_library_subset* command for details about the cells outside the subset.

Feedback

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

LIBSETUP-026

(warning) No default operating condition is defined for library %s.

Description

This warning message occurs because all libraries used for multivoltage designs must have the *default_operating_conditions* attribute defined. This requirement is also in force for designs that use the *set_target_library_subset* or *define_scaling_lib_group* command.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure the *default_operating_conditions* attribute is defined for the library. After making your corrections, use Library Compiler to regenerate the .db file for the library.

See Also

- set_target_library_subset

LIBSETUP-027

(warning) The nominal operating conditions (process = %.3f, voltage = %.3fV, temperature = %.3f) of library %s do not match the values (process = %.3f, voltage = %.3fV, temperature = %.3f) of its default operating conditions %s.

Description

This warning message occurs because all libraries used for multivoltage design must have their nominal process, voltage and temperature values match that of their default operating conditions, respectively. This requirement is also in force for designs that use the *define_scaling_lib_group* command.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure the library has the correct nominal process, voltage and temperature, and that they match the values defined in the

default operating condition. After making any changes, use Library Compiler to regenerate the .db file for the library.

LIBSETUP-029

(error) Either no operating condition has been applied for the current design (warning MV-028), or the libraries have improper operating condition characteristics, as reported in warnings LIBSETUP-026 or LIBSETUP-027.

Description

This error message occurs because the libraries might not have the *default_operating_conditions* attribute defined, or the nominal process, voltage and temperature values of the libraries do not match. Make sure that the *set_operating_conditions* command has been used to explicitly apply an operating condition onto the current design.

What Next

Check and correct the library problems shown in warning LIBSETUP-026 or LIBSETUP-027. Also check that an operating condition has been applied to the current design. After making any corrections, run the command again.

See Also

- set_operating_conditions

LIBSETUP-030

(error) lib_cells %s and %s are distinguished only by set_link_library_subset, but have different arcs.

Description

When using set_link_library_subset to distinguish macros that would otherwise be ambiguous (because they are characterized for the same process, voltage, temperature), we require the macros to have matching timing arcs. For example, we don't allow one lib_cell to have different "when" conditions than another lib_cell.

In particular, if the macros are ETM's created from different modes, it is necessary to first merge the ETM's with PrimeTime's merge_models command.

What Next

If the macros are ETM's extracted from different modes, run PrimeTime's merge_models.

Feedback

LIBSETUP-031

(error) set_link_library_subset lists file %s which is not in $link_library.

Description

set_link_library_subset should specify a list of library files belonging to $link_library. However, one or more of the names in the list is not a library file in $link_library.

What Next

Correct your set_link_library_subset command.

LIBSETUP-049

(warning) Block '%s' contains %d instances of lib_cells that are not part of the target library subset '%s' specified on it.

Description

This warning message advises you of the number of technology cells linked to libraries that are not part of target library specification set on that block.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, you can modify the target library subset specification on the block and run the command again.

See Also

- report_target_library_subset

LIBSETUP-050

(warning) %s %s specified for %s %s,\n \t does not match %s on library cell %s.

Description

This warning message occurs when the specified cell has been required to operate under a certain process and/or temperature value (using the *set_operating_conditions* command), but this particular cell cannot be linked to a library cell that was characterized under this process and/or temperature value.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, check the operating condition for the specified cell or its containing block. Set the proper operating condition using the *set_operating_conditions* command or check the library.

See Also

- set_operating_conditions

LIBSETUP-051

(warning) %s\n \t%s of %s %s \n \t (library cell: %s).

Description

This warning message occurs when the specified cell has been required to operate under a certain supply voltage, but this particular cell cannot be linked to a library cell that was characterized under this supply voltage.

It reports the PG pins whose voltage values do not match with the voltage of the connected supply net. The message also reports the PG pins for which a matching operating condition voltage or a supply net to match voltage levels could not be identified.

What Next

Check the exception connections for the cell. You should connect the correct supply net so that the voltage between the PG pin and supply net matches. Please check the set_voltage and the connect_supply_net commands and make sure that the voltage specified for the supply net matches the voltage specified for the PG pin in the library.

Examples

```
Warning: There is a voltage mismatch on the
         supply net (vdd_sn, 1.300000) explicitly connected to pg pin
 (VDD, 0.900000) of macro cell ram_a
         (library cell: macro_cell_1.db:macro_cell_1/macro_cell).
 (LIBSETUP-051)

Warning: There is a voltage mismatch on the
         supply net (vdd_sn, 1.300000) explicitly connected to pg pin
 (VDD, 0.900000),
         supply net (vdd2_sn, 1.500000) explicitly connected to pg pin
 (VDD2, 1.080000) of macro cell ram_a
         (library cell: macro_cell_2.db:macro_cell_2/macro_cell).
 (LIBSETUP-051)

Warning: There is a voltage mismatch on the
         supply net (vdd_sn, 1.700000) explicitly connected to pg pin
 (VDD, 1.200000), (VDD1, 1.500000),
         supply net (vdd2_sn, 1.300000) explicitly connected to pg pin
 (VDD2, 1.080000) of macro cell ram_a
```

Feedback

```
        (library cell: macro_cell_3.db:macro_cell_3/macro_cell).
 (LIBSETUP-051)
```

See Also

- connect_supply_net
- report_lib
- report_supply_net
- set_operating_conditions
- set_voltage

LIBSETUP-052

(warning) %s\n \t %s of %s %s \n \t (library cell: %s).

Description

This warning message occurs when the specified cell has been required to operate under a certain supply voltage, but this particular cell cannot be linked to a library cell that was characterized under this supply voltage.

It reports the input_signal_level/output_signal_level of the cell whose voltage value do not match with the driver supply net. The message also reports the input_signal_level/ output_signal_level for which a matching operating condition voltage or a supply net to match voltage level could not be identified.

What Next

Please check the set_voltage and set_operating_conditions commands and make sure that the driver supply voltage matches the voltage of input_signal_level/ output_signal_level of the cell.

Examples

```
Warning: There is a voltage mismatch between the driver
         supply net (PNT, 1.300000) and input_signal_level (VDD2,
 1.900000) on pin PD of macro cell ram_a
         (library cell: macro_cell_4.db:macro_cell_4/macro_cell).
 (LIBSETUP-052)

Warning: There is a voltage mismatch between the driver
         supply net (PNT, 1.300000) and input_signal_level (VDD3,
 1.900000) on pin MI, input_signal_level (VDD2, 1.500000) on pin PD of
 macro cell ram_a
         (library cell: macro_cell_5.db:macro_cell_5/macro_cell).
 (LIBSETUP-052)
```

Feedback

See Also

- report_lib
- report_supply_net
- set_operating_conditions
- set_voltage

LIBSETUP-053

(warning) %s %s specified for %s %s,\n \t does not match %s on library cell %s%s

Description

This warning message occurs when the specified block or cell has been required to operate under a certain voltage value (using the *set_operating_conditions* command), but this particular cell cannot be linked to a library cell that was characterized under this voltage value.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, check the operating condition for the specified block or cell. Set the proper operating condition using the *set_operating_conditions* command or check the library.

See Also

- set_operating_conditions
- set_voltage

LIBSETUP-054

(warning) %s cell %s of %s %s does not match the\n \tlink_library_subset %s used on the block.

Description

This warning message occurs when the mapped cell does not come from the link_library_subset defined on a block.

What Next

This is only a warning message. No action is required.

Feedback

However, based on your requirements, you can either ignore the message, modify the link_library_subset on the block,

LIBSETUP-120

(warning) Overriding existing target_library_subset on top design '%s'.

Description

This warning message occurs because when the *set_target_library_subset* command is used to apply a subset to a design or hierarchical cell, any subset already defined there will be replaced. This warning is a reminder that the old subset is replaced, rather than extended.

What Next

This is only a warning message. No action is required.

However, you might want to review the subsets that you want to define for the hierarchy.

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

LIBSETUP-121

(warning) Overriding existing target_library_subset on instance '%s'.

Description

This warning message occurs because when the *set_target_library_subset* command is used to apply a subset to a design or hierarchical cell, any subset already defined there will be replaced. This warning reminds you that the old subset is replaced, rather than extended.

What Next

This is only a warning message. No action is required.

However, you might want to review the subsets that you want to define for the hierarchy.

Feedback

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

LIBSETUP-122

(error) '%s' is not a hierarchical cell.

Description

This error message occurs because the *set_target_library_subset* command may only be applied to the top design and/or hierarchical cells.

What Next

Review the subsets that you want to define and run the command again.

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

LIBSETUP-123

(information) '%s' appears in both -dont_use and -only_here. The -only_here option will take effect.

Description

The set_target_library_subset command was issued with a lib_cell appearing in both the -dont_use and -only_here options. The lib_cell will be considered as -only_here.

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

Feedback

LIBSETUP-124

(information) '%s' appears in set_target_library_subset -only_here, but this lib_cell has \n attribute dont_use in library %s. The lib_cell will not be used.

Description

The set_target_library_subset -only_here command was issued. One of the lib_cells in the -only_here list currently has attribute dont_use set on it in the library. The library attribute has precedence and wins out over the -only_here request.

What Next

If you want to allow the lib_cell to be used in certain parts of the design, via the -only_here option, you can remove the dont_use attribute from the library with the remove_attribute command.

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

LIBSETUP-125

(information) Options -dont_use and -only_here ignore library name prefixes (after wildcard expansion). \n These options apply to lib_cells with the given names across all libraries.

Description

The set_target_library_subset -dont_use and -only_here options take lists of lib_cell names. If you specify an explicit library name as part of the lib_cell name (e.g. lib1/AN2), this message will appear to remind you that the library portion of the name is ignored. These options apply to all lib_cells with the given names, across all libraries.

The one situation where a library name prefix is used is to help guide wildcard expansion in the name. Wildcards in the lib_cell name are expanded according to the lib_cells in memory, including any library name if given. (The library name may itself contain wildcards). But after expansion has been done, the resulting lib_cell names are considered dont_use or only_here across all libraries, not just the ones originally specified.

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

LIBSETUP-126

(information) define_libcell_subset ignores library name prefixes (after wildcard expansion). \n This command apply to lib_cells with the given names across all libraries.

Description

The define_libcell_subset take lists of lib_cell names. If you specify an explicit library name as part of the lib_cell name (e.g. lib1/AN2), this message will appear to remind you that the library portion of the name is ignored. These options apply to all lib_cells with the given names, across all libraries.

The one situation where a library name prefix is used is to help guide wildcard expansion in the name. Wildcards in the lib_cell name are expanded according to the lib_cells in memory, including any library name if given. (The library name may itself contain wildcards). But after expansion has been done, the resulting lib_cell names are considered across all libraries, not just the ones originally specified.

LIBSETUP-127

(warning) '%s' appears in define_libcell_subset, but this lib_cell has \n attribute dont_use in library %s. The lib_cell will not be used.

Description

The define_libcell_subset command was issued. One of the lib_cells in the -libcell_list currently has attribute dont_use set on it in the library. The library attribute has precedence and wins out over the potential set_libcell_subset request.

What Next

If you want to allow the lib_cell to be used in certain parts of the design, via the set_libcell_subset, you can remove the dont_use attribute from the library with the remove_attribute command.

LIBSETUP-128

(warning) Overriding existing set_libcell_subset on instance '%s'.

Feedback

Description

This warning message occurs because when the *set_libcell_subset* command is used to apply a family to a cell, any family already defined there will be replaced. This warning reminds you that the old family is replaced, rather than extended.

What Next

This is only a warning message. No action is required.

However, you might want to review the family that you want to define for the cell.

LIBSETUP-129

(warning) The library cell %s/%s has a negative leakage value, and will be skipped.

Description

The library cell has a negative leakage value, so it will be set dont_use at the library setup stage. The library cell will not be used in the synthesis.

What Next

In your target library, examine the library cell for the unexpected attributes.

LIBSETUP-130

(warning) The library cell %s/%s has a negative or zero area value, and will be skipped.

Description

The library cell has a negative or zero area value, so it will be set dont_use at the library setup stage. The library cell will not be used in the synthesis.

What Next

In your target library, examine the library cell for the unexpected attributes.

LIBSETUP-131

(warning) The library cell %s/%s has a negative or zero drive strength value, and will be skipped.

Description

The library cell has a negative or zero drive strength value, so it will be set dont_use at the library setup stage. The library cell will not be used in the synthesis.

Feedback

What Next

In your target library, examine the library cell for the unexpected attributes.

LIBSETUP-132

(warning) Overriding existing link_library_subset on top design '%s'.

Description

This warning message occurs because when the *set_link_library_subset* command is used to apply a subset to a design or cell, any subset already defined there will be replaced. This warning is a reminder that the old subset is replaced, rather than extended.

What Next

This is only a warning message. No action is required.

However, you might want to review the subsets that you want to specify.

LIBSETUP-133

(warning) Overriding existing link_library_subset on instance '%s'.

Description

This warning message occurs because when the *set_link_library_subset* command is used to apply a subset to a design or cell, any subset already defined there will be replaced. This warning reminds you that the old subset is replaced, rather than extended.

What Next

This is only a warning message. No action is required.

However, you might want to review the subsets that you want to define.

LIBSETUP-134

(error) '%s' is not a hierarchical cell, macro, or pad cell.

Description

This error message occurs because the *set_link_library_subset* command may only be applied to the top design and/or hierarchical cells, macros, and pad cells.

What Next

Review the subsets that you want to define and run the command again.

Feedback

LIBSETUP-135

(warning) A negative leakage value was found on cells in library %s. Leakage optimizations using this library will assume the maximum leakage value of the library for the cells. Please correct the leakage characterization of your library.

Description

A negative leakage value was found on cells in the library. Leakage optimizations using this library will assume the maximum leakage value of the library for the cells.

What Next

In the target library, please correct the leakage characterization.

LIBSETUP-136

(warning) The library cell %s has a negative leakage value.

Description

A negative leakage value was found on cells in the library. Leakage optimizations using this library will assume the maximum leakage value of the library for the cells.

What Next

In the target library, please correct the leakage characterization.

LIBSETUP-137

(information) '%s' appears in both -dont_use and -use. The -use option will take effect.

Description

The set_target_library_subset command was issued with a lib_cell appearing in both the -dont_use and -use options. The lib_cell will be considered as -use.

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

Feedback

LIBSETUP-138

(information) '%s' appears in set_target_library_subset -use, but this lib_cell has \n attribute dont_use in library %s. The lib_cell will not be used.

Description

The set_target_library_subset -use command was issued. One of the lib_cells in the -use list currently has attribute dont_use set on it in the library. The library attribute has precedence and wins out over the -use request.

What Next

Remove the dont_use attribute from the library with the remove_attribute command. Then, you can add the lib_cell to a target library subset via the -only_here or -use options, and restrict it from other parts of the design via the -dont_use option.

See Also

- remove_target_library_subset
- report_target_library_subset
- set_target_library_subset

LIBSETUP-139

(warning) Model library file '%s' is not supported.

Description

Model file is not supported in Design Compilier. It should not be included in the target_library or link_library list.

What Next

Remove the model file from the target_library or link_library list.

See Also

- link_library

LIBSETUP-750

(information) The '%s' variable will become obsolete in a future release. Please use 'set_opcond_inference' command instead.

Feedback

Description

This message informs you that the specified variable in the error message will be obsolete in a future release. You are advised to use the 'set_opcond_inference' command instead.

What Next

Please use the 'set_opcond_inference' command instead.

LIBSETUP-751

(information) Apply operating condition %s (voltage = %s, process = %f, temperature = %f) to cell %s.

Description

This information message occurs when an operating condition is automatically applied to a cell. For each type of operating condition a maximum of 10 messages are allowed by default. Use the *libsetup_max_auto_opcond_message* variable to change the total number of allowed messages.

What Next

This is an information-only message. No action is required.

However, the automatic application of the operating condition might have eliminated some LIBSETUP-001 errors previously shown. You can use the *check_mv_design* command to display the updated list of LIBSETUP-001 errors.

Also, if you do not want automatically-applied operating conditions, use the *set_operating_conditions* command to prevent the automatic application of operating conditions by the tool.

See Also

- set_operating_conditions

LIBSETUP-752

(information) A total of %d operating condition inferences (LIBSETUP-751) have occurred, %d of them have been reported above.

Description

This is a summary message for LIBSETUP-751 information messages.

What Next

This is an information-only message. No action is required.

However, for each type of operating condition a maximum of 10 messages are allowed by default. You can use the *libsetup_max_auto_opcond_message* variable to change the total number of reported messages.

LIBSETUP-753

(warning) Invalid value of '%s' for variable '%s'. The previous value of '%s' is assumed by the tool.

Description

Invalid value have been set for an opcond inference level. The invalid value has been ignored, and the previous value for the variable assumed to be applicable during opcond inference.

What Next

Lookup the supported values for the respective opcond inference level, and reset the variable to one of its supported value so that this message is not shown.

LIBSETUP-754

(information) A total of %d operating conditions have been inferred.

Description

This message prints the total number of inferred operating conditions on cells. If there are multiple scenarios, operating conditions can be inferred on the same cell for different scenarios. This is in addition to the LIBSETUP-751 message that prints detailed information. However, these messages are limited to 10 by default. The LIBSETUP-754 message provides a quick summary of how many cells have inferred operating conditions.

What Next

This is an information-only message. No action is required.

However, the automatic application of operating conditions might have eliminated some LIBSETUP-001 errors previously shown. You can use the *check_mv_design* command to display the updated list of LIBSETUP-001 errors.

Also, if you do not want automatically-applied operating conditions, change the operating condition inference level.

LIBSETUP-755

(error) set_pg_pin_model -%s not in pair with -pg_pin_name specified.

Feedback

Description

This erro message occurs in set_pg_pin_model command when the option specified does not include same pair of arguments as -pg_pin_name specified.

What Next

Make sure the option has the same pair of arguments as -pg_pin_name specified. e.g. if -pg_pin_name with three pins, need to specify three arguments for the option.

LIBSETUP-756

(error) update_lib_pg_pin_model -%s not in pair with -pin_name specified.

Description

This erro message occurs in update_lib_pg_pin_model command when the option specified does not include same pair of arguments as -pin_name specified.

What Next

Make sure the option has the same pair of arguments as -pin_name specified. e.g. if -pin_name with three pins, need to specify three arguments for the option.

LIBSETUP-757

(Warning) Cell %s is skipped due to invalid cell type.

Description

This error message occurs when the cell type of the specified cell is invalid. By default, the set_opcond_inference command accepts only macro, pad, switch and hierarchical cells. If the -applies_to option is specified, only the specified cell types and hierarchical cells are allowed.

What Next

Check the cell type of the specified cell.

LIBSETUP-2001

(Information) set_level_shifter_cell cell %s does not have level shifter type,\n \tit will be set as default type LH_HL.

Description

set_level_shifter_cell on the cell which does not have level shifter type defined, by default the type will be set to LH_HL.

Feedback

What Next

Check the level shifter cell type, correct it to the right type if necessary.

See Also

- report_lib

LIBSETUP-3001

(warning) Library %s already has voltage %s defined; \n \tit will be overwritten by new the specification.

Description

This warning message occurs when the library already has the same voltage defined as defined with the *set_voltage_map* command with the the *-voltage* option. If the voltage value is different, the new specification will overwrite the old value in the library.

What Next

Check the library and the voltage value set with *set_voltage_map* to make sure the new specified voltage value is correct.

See Also

- report_lib

LIBSETUP-3002

(warning) Cell %s PG pin %s was defined as std_cell_main_rail PG pin, \n\twhich conflicts with the new specification.

Description

This warning message occurs when the *set_level_shifter_cell* command defines a valid PG pin as *-std_cell_main_rail_pg_pin*, but another PG pin has this attribute already. The older PG pin attribute is cleaned up.

What Next

This is only a warning message. No action is required.

See Also

- report_lib

Feedback

LIBSETUP-3003

(warning) Level shifter cell %s has more than one enable pin: %s, %s are reset.

Description

This warning message occurs because the currently supported enable level shifter cell can have only one enable pin. Multiple enable pins found in the cell are all reset as input pins.

What Next

Check the library cell and set the correct pin as the enable pin.

See Also

- report_lib

LIBSETUP-3004

(warning) Level shifter cell %s has more than one data pin: %s, %s.

Description

This warning message occurs because the current level shifter cell is allowed to have only one input data pin, but multiple data pins were found in the cell.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, check the library cell and set the correct pin as a data pin or an enable pin.

See Also

- report_lib

LIBSETUP-3005

(warning) Cell %s PG pin %s already exists; attributes specified will be overwritten.

Description

This warning message occurs when the *set_pg_pin_cell* command specifies an existing PG pin. The attributes specified in the command will overwrite the existing attributes in the library.

Feedback

What Next

This is only a warning message. No action is required.

However, to avoid this message, check the library cell to make sure the PG pin setting is correct.

See Also

- report_lib

LIBSETUP-3006

(warning) Overwriting cell %s pin %s related_%s_pin with %s.

Description

This warning message occurs when the related power, ground, or bias pin of the cell pin already exists. The *set_pin_model* command is specifying another PG pin, and overwriting the old related pin.

What Next

This is only a warning message. No action is required.

However, you can avoid this warning message by checking the library cell and ensuring that the PG pin setting is correct.

See Also

- report_lib

LIBSETUP-3007

(warning) Resetting the library voltage map will cause all cell PG pins to be invalid in library %s.

Description

This warning message occurs because resetting the voltage map causes all cell PG pins to be invalid in the library.

What Next

This is only a warning message. No action is required.

However, you can verify that the voltages are defined correctly after performing the reset.

Feedback

See Also

- report_lib

LIBSETUP-3008

(warning) No reference library set for update_lib_model in FRAM mode.

Description

This warning message occurs when no reference library setting is found for the *update_lib_model* command when FRAM mode is specified.

What Next

If using FRAM mode for *update_lib_model*, set the reference library correctly. The reference library can be set in the Milkyway design library, or with the *reference_library* Tcl variable.

LIBSETUP-3009

(warning) %s cell %s type not defined.

Description

This warning message occurs when the specified cell type is not defined for the library cell.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, check the library cell to make sure the type is defined or use the appropriate command to specify the correct cell type.

See Also

- report_lib

LIBSETUP-4000

(error) Libraries are already loaded into memory; cannot remodel db libraries.

Description

This error message occurs because the libraries are already loaded into memory and the design is already linked. The tool cannot remodel the db libraries by doing a library conversion or command-line specifications.

Feedback

What Next

Remove the libraries and the design using the *remove_design* command with the *-all* option. Prepare the libraries before reading in and linking the design.

See Also

- remove_design

LIBSETUP-4001

(error) No link library specified. Library model specification failed.

Description

This error message occurs when the link library is not set.

What Next

Set the correct search path with the *search_path* variable, and set the correct link library with the *link_library* command.

See Also

- search_path

LIBSETUP-4002

(error) No matching library found for %s.

Description

This error message occurs when the tool fails to load the library matching the name pattern. Set the correct *search_path* variable and *link_library* or *target_library* command. Valid libraries should be found in the link_library or target_library list.

What Next

Set the correct *search_path* and *link_library* or *target_library* and correct the library name pattern.

See Also

- search_path

Feedback

LIBSETUP-4003

(error) Library loading failed.

Description

This error message occurs when no library can be loaded successfully.

What Next

Use the *search_path* variable and *link_library* command to set the correct search path and link library.

See Also

- search_path

LIBSETUP-4004

(error) Cannot find library cell matching name %s. %s failed.

Description

This error message occurs when no library cell can be found matching the name specified in the command.

What Next

Check the library setting and correct the name specified in the command.

LIBSETUP-4005

(error) %s %s not supported. %s failed.

Description

This error message occurs when the specified command option is not supported.

What Next

Correct or remove the option and run the command again.

See Also

- report_lib

Feedback

LIBSETUP-4006

(error) %s {%0.3f %0.3f} not valid. set_level_shifter_cell %s not set.

Description

This error message occurs when the *set_level_shifter_cell* cell level or pin level voltage range option is invalid; for example, the lower value of the voltage range is higher than the upper value specified.

What Next

Change the incorrect voltage range in the command.

See Also

- report_lib

LIBSETUP-4007

(error) Cannot find the PG pin %s on cell %s; set_level_shifter_cell -std_cell_main_rail_pg_pin not set.

Description

This error message occurs when the *set_level_shifter_cell* command with the *-std_cell_main_rail_pg_pin* option does not specify a valid PG pin of the cell. The command cannot set it as the *-std_cell_main_rail_pg_pin* for the level shifter cell.

What Next

Check the library cell PG pin definition. Correct the *set_level_shifter_cell* command option to set the *-std_cell_main_rail_pg_pin* on the correct PG pin.

See Also

- report_lib

LIBSETUP-4008

(error) PG pin %s is not a primary power or ground pin of cell %s. set_level_shifter_cell -std_cell_main_rail_pg_pin not set.

Description

This error message occurs when the *set_level_shifter_cell* command with the *-std_cell_main_rail_pg_pin* option does not specify a primary power or ground PG pin of the cell. The *-std_cell_main_rail_pg_pin* is not set for the level shifter cell.

What Next

Check the library cell PG pin definition and correct the *set_level_shifter_cell* command option to set the *-std_cell_main_rail_pg_pin* on the correct PG pin. The PG pin to be specified as *-std_cell_main_rail_pg_pin* must be a primary power or ground pin.

See Also

- report_lib

LIBSETUP-4009

(error) Cannot find pin with name %s of cell %s. %s failed to set %s pin for cell %s.

Description

This error message occurs when the named pin cannot be found in the cell. The command cannot set the pin as requested.

What Next

Check the library cell pins and the command option and for the correct pin name.

See Also

- report_lib

LIBSETUP-4010

(warning) Level shifter cell %s has more than one output pins: %s, %s.

Description

The current level shifter cell can have only one output pin, but multiple output pins were found in the cell.

What Next

This is only a warning message. No action is required.

However, to avoid this warning message, check the library to make sure the correct level shifter cells are defined.

See Also

- report_lib

Feedback

LIBSETUP-4011

(error) Level shifter %s_signal_level %s not defined in library %s voltage map. \n \tset_level_shifter_cell %s_signal_level on cell %s failed.

Description

The input_signal_level, enable_signal_level, and/or output_signal_level voltage is not defined in the library voltage map. The specified signal level is not set for the cell by the *set_level_shifter_cell* command.

What Next

Check the library to make sure the voltage is defined, and check the *set_level_shifter_cell* command to make sure the correct voltage name is specified as the input, enable, or output signal level.

See Also

- report_lib

LIBSETUP-4012

(error) Level shifter cell %s does not have %s pin.

Description

This error message occurs because the specified level shifter cell does not have the required pin.

What Next

Check the library cell to make sure the pins are modeled correctly. Check the *set_level_shifter_cell* command to ensure that the correct cell names are specified.

See Also

- report_lib

LIBSETUP-4013

(error) Level shifter cell %s (cell_)input_voltage_range and (cell_)output_voltage_range \n \tshould be defined together. \n\tBoth cell_%s_voltage_range and %_voltage_range are missing.

Feedback

Description

The level shifter cell level or pin level input voltage range and output voltage range should be defined in pairs. For this particular cell, the input and output voltage ranges are not defined as a pair.

What Next

Check the library cell to make sure the input voltage range and output voltage range are defined as a pair. The pair can be defined either at the cell level or the pin level.

See Also

- report_lib

LIBSETUP-4014

(error) Level shifter cell %s type is LH. input_voltage_range lower bound %0.3f is not \n \tless than output_voltage_range upper bound %0.3f.

Description

This error message occurs because when the level shifter cell is type LH, the *input_voltage_range* lower bound must be less than *output_voltage_range* upper bound. The *input_voltage_range* and *output_voltage_range* can be defined from the cell level or the pin level. The pin level definition always overrides the cell level definition.

What Next

Check the library cell to make sure the input output voltage ranges are defined correctly.

See Also

- report_lib

LIBSETUP-4015

(error) Level shifter cell %s type is HL; input_voltage_range upper bound %0.3f is not \n \tgreater than output_voltage_range lower bound %0.3f.

Description

This error message occurs because when HL is the type of level shifter cell, the *-input_voltage_range* upper bound must be greater than the *-output_voltage_range* lower bound. The *-input_voltage_range* and *-output_voltage_range* can be defined from the cell level or the pin level. The pin level definition always overrides the cell level definition.

Feedback

What Next

Check the library cell to make sure the input output voltage ranges are defined correctly.

See Also

- report_lib

LIBSETUP-4016

(error) set_pg_pin_model command does not have %s specified for PG pins.

Description

This error message occurs when the *set_pg_pin_model* command does not have the voltage name and/or PG pin type specified for the defined PG pins. If the voltage name and PG pin type are not specified, the command cannot do the PG pin setting.

What Next

Run *set_pg_pin_model* again with the *-pg_voltage_name* and *-pg_pin_type* options.

See Also

- report_lib

LIBSETUP-4017

(error) set_pg_pin_model with wrong %s %s specified for PG pin %s. \n
\tset_pg_pin_model failed to set %s as PG pin.

Description

This error message occurs when the option specified with the *set_pg_pin_model* command is incorrect. The command failed to set the named pin as the PG pin.

What Next

Run the command again and specify the correct option for *set_pg_pin_model*.

See Also

- report_lib

Feedback

LIBSETUP-4018

(error) set_pg_pin_model PG pin %s voltage %s is not defined in the library %s voltage map. set_pg_pin_model failed to set %s as cell %s a PG pin.

Description

This error message occurs when an incorrect voltage for a PG pin is specified with the *set_pg_pin_model* command. The command fails to set the named pin as a PG pin.

What Next

Specify the correct voltage for the PG pin using the *set_pg_pin_model* command. The voltage must be defined in the library voltage map.

See Also

- report_lib

LIBSETUP-4019

(error) The power_down_function can only be set on an output pin. \n\tPin %s of cell %s is not an output pin. set_pin_model failed to set power_down_function on the pin.

Description

This error message occurs when the *set_pin_model* command is attempting to set the power_down_function on a non-output pin. The power_down_function can only be set on an output pin.

What Next

Check the *set_pin_model* command and the pin specified to set the power_down_function. Make sure to set the power_down_function only on an output pin.

See Also

- report_lib

LIBSETUP-4020

(error) Cannot find PG pin %s for cell %s. set_pin_model failed\n\t to set related_%s_pin for pin %s.

Description

This error message occurs when the specified PG pin does not exist in the cell. The tool cannot set the related power or ground pin to the specified PG pin.

What Next

Check that the library cell PG pin is correctly set. Make sure that the *set_pin_model* command specifies the correct PG pin name.

See Also

- report_lib

LIBSETUP-4021

(error) Cell %s bias PG pin %s has wrong type; set_pin_model failed to set \n \trelated_bias_pin for pin %s.

Description

This error message occurs because the specified bias pin does not have the correct PG bias pin type. The *set_pin_model* command failed to set it as related_bias_pin. The supported PG bias pin types are pwell, nwell, deeppwell, and deepnwell.

What Next

Check that the library cell PG pin is correctly set. Also, check the *set_pin_model* command to specify the correct PG pin name.

See Also

- report_lib

LIBSETUP-4022

(error) Cannot find PG pin %s for cell %s. set_power_switch_cell failed \n\tto set functions for PG pin %s.

Description

This error message occurs when the specified PG pin does not exist in the cell. The *set_power_switch_cell* command cannot set the functions for a non-existent PG pin.

What Next

Check that the library cell PG pin is correctly set. Make sure that the *set_power_switch_cell* command specifies the correct PG pin name.

See Also

- report_lib

Feedback

LIBSETUP-4023

(error) Retention pin for retention cell cannot be set on output pin; \n\tpin %s of cell %s is not an output pin. set_retention_cell failed to set the pin as a retention pin.

Description

This error message occurs when the *set_retention_cell* command attempts to set a retention pin on an output pin. A retention pin cannot be set on an output pin of a retention cell.

What Next

Check the library cell and the command option and make sure the correct pin is specified to be set as a retention pin.

See Also

- report_lib

LIBSETUP-4024

(error) Retention pin %s disable value %s not valid. \n set_retention_cell failed to set retention pin disable value.

Description

This error message occurs when running the *set_retention_cell* command with the *-retention_pin* option disable value set to an invalid value.

The supported disable values for *-retention_pin* are 0 and 1.

What Next

Run the command again with the *-retention_pin disable value set to either 0 or 1.*

LIBSETUP-4025

(error) Cell %s is not buffer or inverter.\n\t set_always_on_cell failed to set cell %s as always-on cell.

Description

This error message occurs when the *set_always_on_cell* command is specifying a cell that is neither an inverter cell nor a buffer cell. The *set_always_on_cell* command cannot set the cell as an always-on cell.

What Next

The specified library cell must be either an inverter or a buffer cell. Check the *set_always_on_cell* command to make sure the correct cell name is specified.

See Also

- report_lib

LIBSETUP-4026

(error) Cell %s pin %s is not an input pin.\n \tThe set_isolation_cell command failed to set pin %s as %s pin.

Description

This error message occurs when you use the *set_isolation_cell* command to specify a data or enable pin that is not an input pin. The isolation cell data or enable pin must be an input pin.

What Next

Check the library cell and make sure the correct input pin is specified to be set as a data or enable pin.

See Also

- report_lib

LIBSETUP-4027

(error) update_lib_model -reference_mode %s is not supported.

Description

This error message occurs when the *update_lib_model* command *-reference_mode* option specifies an unsupported reference mode. Supported reference modes are *FRAM* and *TCL*.

What Next

Run the command again, and specify either FRAM or TCL mode.

LIBSETUP-4028

(error) No library found to be converted.

Feedback

Description

This error message occurs when there is no library in memory to be converted.

What Next

Check the library setting and run the command again.

See Also

- search_path

LIBSETUP-4029

(error) update_lib_model failed with library %s.

Description

This error message occurs when the conversion of the library fails. See previous messages for details about the cause of the failure.

What Next

Correct the errors reported during the conversion and run the command again.

See Also

- report_lib

LIBSETUP-4030

(error) Cannot open file %s to write.

Description

This error message occurs because the file cannot be opened in write mode. The command cannot complete.

What Next

Check the path and the file name, make sure the directory can be accessed, and make sure the file can be opened in write mode.

LIBSETUP-4031

(error) Library %s is old syntax library with power_supply defined. %s failed.

Feedback

Description

This error message occurs because the library is an old syntax library with *power_supply* and *rail_connection* defined. The command cannot succeed on the library.

What Next

Convert the old library to a Liberty PG library and then run the command again.

LIBSETUP-4032

(error) update_lib_model -reference_mode FRAM is not supported in WLM mode.

Description

This error message occurs when the *update_lib_model* command *-reference_mode FRAM* option is specified in WLM mode. The supported reference mode in WLM mode is *TCL*.

What Next

If *-reference_mode FRAM* is intended, run the command again in topographical mode. If not, specify *TCL* as the *-reference_mode* option in WLM mode.

LICSVR

LICSVR-1

(error) Variable '%s' has invalid value '%s'.\n\tAllowed values are: 'package', 'individual', 'package individual'\n\tand 'individual package'.

LICSVR-2

(error) Could not obtain a license.

Description

The license for the feature being run could not be obtained.

What Next

Check the key file to see if the feature exists. Check the location of the keyfile, either the default location or at $SYNOPSYS_KEY_FILE. It could also be that all the licenses are in use.

Feedback

LICSVR-3

(error) SYNOPSYS_DS is not set. You must set this environment\n\tvariable to the root of the installed Synopsys software.

Description

SYNOPSYS_DS variable should be set inorder for the application to find the default location.

What Next

Set the SYNOPSYS_DS environment variable to SYNOPSYS root.

LICSVR-4

(error) DISPLAY is not set. You must set this environment\n\tvariable before running the Synopsys software.

Description

The DISPLAY environment variable displays the application on the terminal on which it was brought up.

What Next

Check to see if this environment variable is set to the correct value.

LICSVR-5

(error) Can't initialize the license server.

Description

The vendor daemon will be brought up by the Flexlm license manager lmgrd on the SERVER mentioned in the keyfile. The machine must be accessible.

What Next

Check to see if the machne is up and running. If you are starting the license server from a machine other than the server, then you must be able to ping and rsh to the SERVER.

LICSVR-6

(error) The Synopsys License Server has crashed.

Feedback

Description

The license server went down due to some reason. This may cause the lmgrd and synopsysd processes to hang.

What Next

If the machine is down, the machine needs to be up and running. If the license server is being brought up from the startup script, check to make sure that the lmgrd and synopsysd processes have icome up cleanly. Use lmstat to check. If you have to bring up the license server daemons manually, make sure that you do not have any zombie processes for lmgrd and synopsysd. Start the license manager using lmgrd.

LINK

LINK-1

(error) Can't find %s port '%s' on reference to '%s' in '%s'.

Description

This message indicates that the specified port has no corresponding port on the design to which the reference is to be linked. Therefore, the reference cannot be linked to the design.

This situation could arise if extra pin names were specified in the name-based instantiation of the cell in the source file. Alternatively, the name of the design port might be misspelled or incorrectly specified in the cell instantiation.

Another, less likely possibility is that there are design name conflicts that caused the linker to attempt to link the reference to the wrong design.

What Next

Check the original source file for one or both of the above problems in the cell instantiation, and edit the file to correct the pin names. Check also for incorrect design names and correct them. Then re-execute *link*.

LINK-2

(error) Too many ports on reference to '%s' in '%s'.

LINK-3

(error) Width mismatch on port '%s' of reference to '%s' in '%s'.

Feedback

Description

The reference above could not be resolved due to a port size mismatch. The linker found a design that matches the requested reference name, but the port sizes do not match.

What Next

Check that the ports of the target design or library cell are compatible with the reference.

LINK-4

(error) Too few ports on reference to '%s' in '%s'.

Description

This error occurs when a reference to a module has fewer ports than the module has.

This can occur when you use positional port connections instead of named port connections to instantiate a module, but the number of ports in the instantiation is less than the number of ports provided by the module.

As an example, consider an RTL submodule with the following ports:

```
module sub (CLK, A, Z);
input   CLK;
input   [15:0]   A;
output  [15:0]   Z;
```

During DFT insertion, the tool adds additional test ports for DFT signals that are not predefined:

```
module sub ( CLK, A, Z, test_si, test_se );
  input [15:0] A;
  output [15:0] Z;
  input CLK, test_si, test_se;
```

The top-level instance of this block uses positional port connections:

```
sub Usub (CLK, A, Z);
```

This results in a LINK-4 error:

```
Error: Too few ports on reference to 'sub' in 'top'. (LINK-4)
Warning: Unable to resolve reference 'sub' in 'top'. (LINK-5)
0
```

What Next

If the message is unexpected, verify the port count and order of the module against the instantiation.

Feedback

If ports are added during module synthesis, convert the instantiation to use named connections instead:

```
sub Usub (.CLK(CLK), .A(A), .Z(Z));
```

LINK-5

(warning) Unable to resolve reference '%s' in '%s'.

Description

This warning is issued when a suitable design can not be found to link a cell reference to. This will result in any cells using that reference being left as "black boxes". Generally this will happen because of one of two reasons: (1) either a design with the same name as the reference does not exist in the database, link libraries and the directories specified by the search_path, or, (2) the design exists but there are port mismatches between the reference and the design. In the second case an additional error message indicating the exact nature of the mismatch would be given.

If this error occurs while building a synthetic library part, you probably need to use "set_local_link_library" within your implementation description. Please refer to the section "Adding Hierarchy-Control Directives" in the DesignWare Developer Guide.

What Next

If there are additional error messages indicating the name and nature of the port mismatches, modify the original souce to make the port specifications match in the instantiation and the design. If there are no such messages, find the library or the directory on which the required design resides. If it is a library, then add that library to the *link_library* variable, and the location of the library to the *search_path* variable. If it is in a design file, add its directory to the *search_path* variable. After doing this, run the *link* command again.

LINK-6

(error) Could not find pin '%s' on design '%s' for cell '%s'.

LINK-7

(error) Recursive hierarchy detected in design '%s'.

LINK-8

(error) Cannot resolve enumeration for cell '%s' on design '%s'.

Feedback

LINK-9

(warning) Unable to resolve reference to synthetic module '%s' in '%s'.

LINK-10

(error) '%s' was not identified as a synthetic library module\n \tand could not be successfully elaborated from design library '%s'.

Description

The reference above could not be resolved to a synthetic library module in your current *link_library* variable. The design also could not be elaborated from a design that had been analyzed into the given design library. This causes linking to fail for parameterized instances.

What Next

If the reference should resolve to a synthetic library module, you should double check that the appropriate synthetic library is in your *link_library* and that the library contains the given module. If other libraries precede your synthetic library in the *link_library* list, be sure that the two libraries do not contain a cell of the same name. Note that VHDL references are case-insensitive; for example, you could erroneously link to a cell named *ADD* from a technology library when you intended to link to a module *add* from a synthetic library.

If the reference should resolve to a parameterized part, you must analyze that part into an appropriate design library before linking. There may have been an error in the actual elaboration. Check the error messages that preceded this one.

LINK-11

(error) Unconstrained port '%s' in design referenced by '%s' in '%s'.\n \tThis version does not support unconstrained ports.

LINK-12

(warning) Unable to find library '%s'. This was probably caused by bad Synopsys installation.

LINK-13

(warning) design library '%s' was used in design '%s'\n \tbut it was never defined. Ignoring.

Feedback

Description

Your VHDL source code contains a library clause for the given design. This library has not been defined in Design Compiler.

What Next

Define the library using *define_design_lib*.

LINK-14

(warning) Instance of '%s' is defined in both libraries\n \t'%s' and '%s', which are both visible in design '%s'.\n \tThe first library will be used.

Description

Your VHDL source code for the given design contains a library clause for both libraries listed above. Both libraries define an entity for the instance given. Technically, this is an error in VHDL. We are using the entity from the first library listed.

What Next

There is nothing to do for now. In the future, it will be important to choose an entity explicitly in a VHDL configuration.

LINK-15

(error) Cannot continue with auto_link disabled. Set 'auto_link_disable = false'.

Description

The *auto_link_disable* variable is only to be used for speeding up long sequences of *set_load*, *set_resistance*, and *set_annotated_delay* commands. The current command cannot be executed while auto_link is disabled.

What Next

Set *auto_link_disable* = false, and re-execute the command.

LINK-16

(warning) Parameter mismatch in linking reference '%s' by name.\n \tLinked to '%s', which has the correct parameters.

Feedback

Description

An attempt was made to link a parameterized reference by name, but the name of the reference pointed to a design with incorrect parameters. The link process resolved the reference to the design above, which had the correct parameters.

What Next

To avoid this message, you should attempt to keep your design names unique. This is done by keeping your parameter values below the *hdl_naming_threshold*, and by including special naming parameters in your HDL designs. For details, refer to the *VHDL Compiler Reference Manual*.

LINK-17

(warning) Design '%s' was renamed to '%s' to avoid\n \ta conflict with another design that has the same name but\n different parameters.

Description

A design was automatically elaborated by HDL Compiler, but the name generated for the new design was already in use by another design. The new design was renamed to avoid overwriting the existing design.

What Next

To avoid this message, ensure that your design names are unique by keeping your parameter values below the *hdl_naming_threshold*, and by including special naming parameters in your HDL designs. For details, refer to the *VHDL Compiler Reference Manual*.

LINK-18

(warning) Parameter mismatch in linking reference '%s' by name.\n \tCan't find design.

Description

An attempt was made to link a parameterized reference by name, but the name of the reference pointed to a design with incorrect parameters. The processing that follows this message will attempt to elaborate a new design with the correct parameters. If it fails, this reference will remain unresolved.

What Next

To avoid this message, you should attempt to keep your design names unique. This is done by keeping your parameter values below the *hdl_naming_threshold*, and by including special naming parameters in your HDL designs. For details, refer to the *VHDL Compiler Reference Manual*.

Feedback

LINK-19

(warning) "Port '%s' was unresolved on reference to '%s' in \ '%s'.

Description

This warning is issued when a port can not be resolved on a reference. Ports in the given reference may be duplicate by ignoring cases. If it fails, this reference will remain unresolved.

What Next

To avoid this message, you should attempt to keep your ports in a reference unique. Check for attribute value dblink_case_insensitive in the warning reference.

LINK-20

(warning) "Attempting to resolve reference '%s'\n\ \tfrom non-synthetic design library '%s'.

Description

This warning is issued when a reference suspected to be a DesignWare part fails to link from a DesignWare library such as dw02.sldb. However, the reference may still successfully link from a non-DesignWare library.

What Next

Often this warning results from neglecting to specify the required synthetic libraries using the link_library variable. This can be quickly fixed using the following shell script line:

link_library = link_library + synthetic_library

This ensures that the link_library variable specifies the necessary DesignWare libraries for your design. Also check that the variable, synlib_library_list, specifies the correct design library names for DesignWare parts. Note that if you are using an external implementation of a DesignWare part, you may receive this warning during normal use.

LINK-21

(warning) Design '%s' has %d extra %s port(s) than \n\t reference '%s' in '%s'.

Description

You receive this message if the external netlist used by the preserved function has extra ports that are not defined in the preserved function. These ports are unused.

Feedback

What Next

To avoid this message, use a netlist with I/O ports exactly matching the I/O ports specified in the preserved function.

LINK-22

(error) Reference '%s' in '%s' is a preserved function and \n\t cannot have inout ports.

Description

This error is issued when a port can not be resolved on a reference because the direction of the port is inout. Bidirectional ports are not allowed with preserved functions and external netlists.

What Next

To avoid this error, change the direction of the port to make it either an input or output port.

LINK-23

(error) Design '%s' used to resolve reference '%s' in \n\t '%s' is a external netlist and cannot have inout ports.

Description

You receive this message if a port cannot be resolved on a reference. In the external netlist used to resolve the reference, the direction of the corresponding port is inout. Bidirectional ports are not allowed with preserved functions and external netlists.

What Next

To avoid this error, use a netlist that has only input or output ports that match the ports of the preserved function.

LINK-24

(error) Port '%s' of reference '%s' in '%s' \n\t is connected to port '%s' of the external netlist '%s'. \n\t The directions of these two ports are not compatible.

Description

This error is issued when a port can not be resolved on a reference because the direction of the corresponding port of the netlist is different. Note that 'inout' ports are not allowed in preserved functions and external netlists.

Feedback

What Next

To avoid this error, input ports in the preserved function must be same as the input ports in the external netlist. Similarly, output ports in the preserved function must be same as the output ports in the external netlist.

LINK-25

(error) Unable to match ports of cell %s ('%s') to '%s'.

Description

The tool issues this error message because it encountered problems when attempting to match the ports of the cell's existing reference to the new reference.

What Next

Check that the ports of the target design or library cell are compatible with the cell's current reference. You may need to modify the original source to make the port specifications match in the instantiation and the design.

See Also

- link

LINK-26

(warning) Design '%s' was renamed to '%s' to resolve\n \ta long name which is not supported by some down stream tools.

Description

Down stream tools have limitation for the length of design name. The design name generated by HDL compiler is shortened, then the design can be accepted by down stream tools.

What Next

To avoid this message, ensure that your design names do not exceed the limit.

LINK-27

(warning) Width mismatch on port '%s' of reference to '%s' in '%s'.

Description

The linker found a design that matches the requested reference name, but the port sizes do not match. This is usually a design error, and should be corrected.

Feedback

Due to a special request, the linker will resolve the mismatch rather than leaving the reference unlinked. The port and connected value will be right-aligned. Any excess bits in the left side of the connected value will be truncated. Any excess bits in the left side of the port will be driven by 0 (for input ports) or left unconnected (for out and inout ports).

Note this amounts to zero-extension rather than sign-extension, regardless of the type of the connected value.

What Next

Check that the ports of the target design or library cell are compatible with the reference.

LINK-28

(warning) In design '%s', %s port '%s' is not being used according to its stated direction. Run the check_design command.

Description

This message is obsolete and has been replaced by LINT-68. Refer to the man page for that message.

See Also

- LINT-68

LINK-29

(error) Connection from net '%s' to internal pin '%s' is not allowed and is ignored.

Description

This error message occurs when a net is being connected to a pin having a direction of internal. Connection of an internal pin to a net is not allowed.

What Next

Correct the design so that internal pins are not connected to any wire in RTL.

LINK-30

(warning) Bit-blasted bus '%s' in the library reference in design '%s' was reconstructed into a vector.

Description

This warning message occurs when the linking process matched by name a bit-blasted bus to a bus that is not bit-blasted.

Feedback

LINK-31

(error) RTL PG is not enabled. Connection to PG pin %s/%s is being dropped.

Description

This error message occurs in DC when a net is being connected to a PG pin. By default, DC does not allow connections to PG pins. You can allow such connections in limited cases by setting the variable dc_allow_rtl_pg to true. Doing so will limit your choice of outputs from DC.

What Next

Correct the design to remove connections to PG pins, or set dc_allow_rtl_pg to true.

LINK-32

(error) PG connection to lib_cell %s is not permitted. Connection to PG pin %s/%s is being dropped.

Description

This error message occurs in DC when a net is being connected to a PG pin of a lib_cell that is not supported for RTL PG connections. Supported lib_cells are macros and power management cells.

What Next

Correct the design to remove connections to these PG pins.

LINK-33

(warning) Ignored bus naming style difference ('%s' vs '%s') when linking cell '%s'.

Ignored bus naming style difference ('%s' vs '%s') when linking cell '%s'.

Description

This warning message occurs when the linking process matched a bus in an instance cell with a bus in the target cell, and the bus naming styles where different.

A[31:0] vs A<31:0>

LINK-34

(warning) Used pin name synonym - '%s' - to link pin '%s' on cell '%s'..

Feedback

Description

Used a pin name synonym mapping to match a pin name during linking.

LINK-35

(warning) All references to module '%s' are ignored and treated as black boxes.

Description

Ignored all references to a module per user request, and treated as a black box.

LINK-36

(Error) Cannot link block abstraction subdesign %s outside of its block abstraction hierarchy.

Description

This error message occurs when you attempt to link a subdesign of a block abstraction outside of its block abstraction hierarchy. If you attempt to instantiate such a subdesign at the top level, or anywhere else outside of its own block abstraction's hierarchy, the link will fail.

This error typically occurs when there were multiple instantiations of the subdesign before you created the block abstraction, and at least one of the instantiations was outside of the subhierarchy that was turned into the block abstraction.

What Next

To avoid the conflict, the recommended practice is to rename all the subdesigns of the block abstraction at the block level before running the *create_block_abstraction* command. To do this, set the *uniquify_naming_style* variable and then run the *uniquify* command as in this example:

```
set_app_var uniquify_naming_style "${DESIGN_NAME}_%s_%d"
uniquify -force
change_names -rules verilog -hierarchy
create_block_abstraction
write_file -format ddc -hierarchy -output block_design.ddc
```

LINK-37

(error) Failed to link physical library with link library.

Feedback

Description

This error message occurs when there is no valid link library specified to link reference libraries and logical libraries.

LINK-901

(warning) '%s' pin on '%s' cell in the '%s' design is associated with the '%s' pin on '%s' reference in the '%s' %s

Description

This warning message occurs when the linking process matched a pin by name and ignored a case mismatch or used a user provided, pin name synonym mapping.

See Also

- link_allow_design_mismatch

LINK-902

(warning) '%s' pin on '%s' cell in '%s' design is missing from the '%s' reference%s.

Description

This warning message occurs when the linking process was unable to find a pin on a reference.

See Also

- link_allow_design_mismatch

LINK-903

(warning) Unable to connect '%s' net to the '%s' pin of '%s' cell in '%s' design.

Description

This warning message occurs when the linking process was unable to match a pin and to connect it to its net.

See Also

- link_allow_design_mismatch

Feedback

LINK-904

(warning) The width [%d] of '%s' bus on '%s' cell in '%s' design is mismatched with the width [%d] of '%s' bus on the '%s' reference%s.

Description

This warning message occurs when the linking process matched a bus by name and ignored a width mismatch.

See Also

- link_allow_design_mismatch

LINK-905

(warning) '%s' pin on '%s' cell in the '%s' technology library is missing in the '%s' physical library.

Description

This message occurs because the data in physical library and logical library do not match. There are more pins in logical library than in physical library. The tool is creating a temporary FRAM which contains the original pins and the missing pins. Definition of the missing pin(s) is taken from the logical library.

This feature is meant to allow the flow to continue without running into error dirty linking mode.

What Next

Fix both physical and logical libraries so that their contents match.

See Also

- link_allow_design_mismatch
- report_design_mismatch

LINK-906

(warning) Ignored pin direction mismatch for '%s' pin on '%s' cell in %s' physical library. Defaulting to the direction specified in the '%s' technology library.

Feedback

Description

This message occurs because the data in physical library and logical library do not match. The indicated pin has direction mismatch between logical library and physical library. The tool creates a temporary FRAM with pin direction specified by the logical library pin.

This feature is meant to allow the flow to continue without running into error in dirty linking mode.

What Next

Fix both physical and logical libraries so that their contents match.

See Also

- link_allow_design_mismatch
- report_design_mismatch

LINK-907

(warning) '%s' pin on '%s' cell in the '%s' technology library is associated with '%s' pin in the '%s' physical library.

Description

This warning message occurs when the pin names in the physical and logical libraries do not match. The tool creates a temporary FRAM and rename the pins to match that of logical library pins.

This feature is meant to allow the flow to continue without running into error in dirty linking mode.

What Next

Fix both physical and logical libraries so that their contents match.

See Also

- link_allow_design_mismatch
- report_design_mismatch

LINK-908

(warning) The logical cell (%s) does not have a physical view.

Feedback

Description

This message occurs because the data in physical library and logical library do not match. The indicated logical library has no physical library. The tool creates a temporary FRAM based on the data from logical library cell.

This feature is meant to allow the flow to continue without running into error in feasibility mode.

What Next

Fix physical library so that it content match with the logical library.

See Also

- link_allow_design_mismatch
- report_design_mismatch

LINK-909

(warning) couldn't link '%s' cell to reference '%s'.

Description

This warning message occurs when the linking process couldn't find a reference.

See Also

- link_allow_design_mismatch

LINK-910

(warning) '%s' pin on '%s' cell in the '%s' technology library is associated with '%s' pin in the '%s' physical library.

Description

This message occurs because the data in physical library and logical library do not match. The indicated bus pin has bus naming mismatch between logical library and physical library. The tool creates a temporary FRAM to match the bus naming style of the logical library cell.

This feature is meant to allow the flow to continue without running into error in feasibility mode.

What Next

Fix both physical library so that it contents match with the logical library.

Feedback

See Also

- link_allow_design_mismatch
- report_design_mismatch

LINK-911

(warning) Linker anchor cell inserted for unconnectable pin on '%s' cell.

Description

This warning message occurs when the linking process inserted a cell to anchor unconnectable nets due to missing pins on a logical cell. The tool also creates a temporary anchor FRAM to preserve the connection.

This feature is meant to allow the flow to continue without running into error in feasibility mode.

What Next

Fix either the netlist or both physical and logical library and so that the connections match with what is defined in the libraries.

See Also

- link_allow_design_mismatch
- report_design_mismatch

LINK-912

(warning) Automatically reconstructed '%s' bus with width of %d from { %s } bit-blasted bus pins in '%s' %s.

Description

This warning message occurs when the linking process reconstructed a bus from individual pins.

See Also

- link_allow_design_mismatch

Feedback

LINK-914

(warning) Automatically reconstructed '%s' bus with width of %d from { %s } bit-blasted bus pins in '%s' %s.

Description

This warning message occurs when the physical linking process reconstructed a bus from individual pins.

See Also

- link_allow_design_mismatch

LINK-915

(warning) Missing logical referenced cell, create logical library cell (%s).

Description

This message occurs because the indicated cell is instantiated in the design but the logical reference does not exist. The tool creates a temporary logical reference library and store it in the current working directory.

This feature is meant to allow the flow to continue without running into error in feasibility mode.

What Next

Provide the missing logical library, and add this temporary library as part of the link_library lists.

See Also

- link_allow_design_mismatch
- report_design_mismatch

LINK-916

(warning) Physical library cell pin are bit blasted, rename pin (%s:%s - %s).

Description

This message occurs because the data in physical library and logical library do not match. The indicated cell pin bus has is bit blasted in physical library and is not bit blasted in logical library.

Feedback

This feature is meant to allow the flow to continue without running into error in feasibility mode.

What Next

Fix physical library so that it content match with the logical library.

See Also

- link_allow_design_mismatch
- report_design_mismatch

LINK-917

(warning) Ignored bus naming style difference ('%s' vs '%s') when linking cell '%s'.

Ignored bus naming style difference ('%s' vs '%s') when linking cell '%s'.

Description

This warning message occurs when the linking process matched a bus in an instance cell with a bus in the target cell, and the bus naming styles where different.

A[31:0] vs A<31:0>

See Also

- link_allow_design_mismatch

LINK-918

(warning) reference '%s' in the '%s' design is associated with the '%s' reference.

Description

This warning message occurs when the linking process matched a reference by name and ignored a case mismatch.

See Also

- link_allow_design_mismatch

LINK-919

(warning) automatically inferred pin directions for instance '%s' blackbox '%s'.

Feedback

Description

This warning message occurs when the linking process automatically inferred pin directions for blackbox cell.

See Also

- link_allow_design_mismatch

LINT

LINT-0

(warning) In design '%s', input pin '%s' of leaf cell '%s' is not connected to any net. %s assumed.

Description

This message appears when a leaf cell has an unconnected input pin. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

What Next

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

LINT-1

(warning) In design '%s', cell '%s' does not drive any nets.

Description

This warning alerts you that the output(s) of a component is not connected to any load nets. This usually indicates that a design has not been correctly specified. The Design Compiler may remove such components from your design unless they are protected by a *dont_touch* attribute.

What Next

Make sure that you really want the named component to exist in the given design, even though it has no output pins connected. If so, add a *dont_touch* attribute with the *dont_touch* command to keep the component from being removed.

Feedback

LINT-2

(warning) In design '%s', net '%s' driven by pin '%s' has no loads.

Description

This warning message occurs when a net is driven by an output pin (or pins) but has no load pins connected to it. This usually indicates that a design is not correctly specified. The Design Compiler may remove such nets and their driving components from your design unless they are protected by a don't touch attribute.

What Next

This is only a warning message. You can eliminate this warning message by following the instructions below.

Make sure that you want the named net to exist in the given design, even though it has no load pins connected. If so, add a don't touch attribute with the *dont_touch* command to keep the net from being removed.

Check the value of the *hdlin_keep_signal_name* variable. For some settings, signals without drivers or loads are preserved in the elaborated design. Check the *hdlin_keep_signal_name* man page for more information.

LINT-3

(warning) In design '%s', net '%s' has no drivers. %s assumed.

Description

This warning message occurs when there is a net that is not driven by any source pins. Synopsys tools will assume a logical value, such as logic zero or logic one) for these unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

What Next

This is only a warning. You can eliminate this warning message by the following the instructions below.

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating net to the correct logical value in your design.

Check the value of the *hdlin_keep_signal_name* variable. For some settings, signals without drivers or loads are preserved in the elaborated design. Check the *hdlin_keep_signal_name* man page for more information.

Feedback

LINT-4

(information) In design '%s', net '%s' has multiple drivers. Wired AND assumed.

Description

This warning indicates that *check_design* has found a net with multiple source pins. Synopsys tools must make an assumption regarding the functionality of such wired-logic nets. This message indicates which wired-logic net (for example, wired-AND, wired-OR) will be used for this particular net. The assumption is made based on a description of wired-logic functionality in the technology library that you are using.

What Next

Make sure that you intended to have multiple drivers on the given net. Errors in specifying a design could lead to this message in a situation where wired logic is not intended.

You could also use *set_attribute* and *remove_attribute* commands to specify or remove the wired logic type for a given net.

For example,

set_attribute [get_nets z] wired_and true -type boolean

would set 'wired_and' attribute on net 'z'. While

remove_attribute [get_nets z] wired_and

would remove the 'wired_and' attribute on net 'z'.

LINT-5

(warning) In design '%s', output port '%s' is not driven.

Description

This error message occurs when the *check_design* command finds the specified output port for the design is not driven by any signal.

What Next

Check your design to be sure that it is connected correctly, and then run the command again.

LINT-6

(warning) In design '%s', input port '%s' drives wired logic; the port direction may have been specified incorrectly.

Feedback

Description

This warning message occurs when the *check_design* command encounters an input port connected to a net that has multiple drivers. The input port (which acts as a driver on the net) is part of a wired-logic gate.

What Next

This is only a warning message. No action is required.

However, you can make sure that you want multiple drivers on the net driven by the indicated port. Errors in specifying a design can lead to this message in a situation where wired logic is not intended. For example, if the direction of an output port is accidentally specified as input, then this message could occur.

Otherwise, you have encountered a situation where the optimizer has created wired logic on a design boundary. Check the components created by the optimizer to ensure that this is the functionality that you originally intended. Use the *Formality* command to compare the design you currently have with the original design, in addition to simulating the synthesized design to ensure correctness.

LINT-7

(error) Recursive hierarchy detected in design '%s'.

Description

The *check_design* command traces the hierarchy of your design to ensure that "recursive hierarchy" does not occur. The term "recursive hierarchy" means that a module in a design instantiated a sub-module that, in turn, instantiated the original module. Hierarchically recursive designs cannot be handled by the Design Compiler. This is an error message, not a warning.

What Next

This error usually occurs when a design has been incorrectly described. Modify your design description to remove the recursive hierarchy.

LINT-8

(warning) In design '%s', input port '%s' is unloaded.

Description

The *check_design* command issues this warning when it finds an unconnected (for example, "unloaded") input port on a design. This means that the given input port does not connect to any logic inside the design.

Feedback

What Next

Make sure that you intended that the specified port be unused in your design.

LINT-10

(warning) In design '%s', cell '%s' has no output pins.

Description

This warning message indicates that *check_design* has found a cell with no output pins. Unless such cells are protected through the use of the *dont_touch* command, the *compile* command will remove them from the design, since they have no functionality.

What Next

This warning probably appeared because of an error in specifying a component in your design, or a component in your technology library. Check the design/library to find the problem, and correct the description of the given cell/design.

LINT-11

(fatal) In design '%s', db_object '%s' does not have a '%s' attribute.

Description

This is a fatal error in the *check_design* command. An object in the Synopsys internal database for your design has become corrupt or does not have information regarding signal direction (for example, input, output or bidirectional).

What Next

Recreate or re-read your design. If you specified a component pin without a direction attribute, you can fix the problem by making sure that a direction exists for the given pin. Otherwise this error could indicate that there is an internal problem in the Synopsys software that needs to be reported to the Synopsys Hotline.

LINT-12

(fatal) Unable to db_gen_init '%s' from db_object '%s'.

Description

This is a fatal error in the *check_design* command. An object in the Synopsys internal database for your design has become corrupt, or that an object in your design does not have ports attached to it.

What Next

Recreate or re-read your design. If you specified a component without ports, you can fix the problem by making sure that ports exist for the given pin. Otherwise this error could indicate that there is an internal problem in the Synopsys software that needs to be reported to the Synopsys Hotline.

LINT-20

(error) In design '%s', cell '%s' does not have a reference.

Description

This error describes a problem in the database representation for your design. The error means that a particular instantiation of a component (or "cell" in Synopsys terms) does not indicate which type of component it actually is. In Synopsys terminology "reference" describes the part of a design representation that points to the actual component for a given instantiation or cell. If you have an inverter (INV) in your technology library, and you've instantiated that inverter in your design as cell13 and cell23, then each of the instantiations (cells) should own a pointer (reference) to the actual component (in this case INV). This error indicates that, for some reason, the reference does not exist on the cell.

What Next

Make sure that your design specifies the type of the given cell. If you specified a cell without a type, fix the problem by changing your design description. Otherwise this error could indicate that there is an internal problem in the Synopsys software that needs to be reported to the Synopsys Hotline.

LINT-21

(fatal) Unable to db_new_attribute to db_object '%s'.

Description

This is a fatal error in the *check_design* command. Synopsys tools were unable to allocate memory to create an object in the Synopsys internal database description for your design. The *check_design* command creates small markers on your design as it traverses the design checking for errors. These small markers are removed after *check_design* is finished. This error indicates that an attempt to create a marker failed for some reason. This is probably due to a lack of memory, in which case the fatal error was accompanied by an "out of memory" error message. It is.also possible that this message could occur in a badly mangled design which has recursive hierarchy.

Feedback

What Next

Check the message for an "out of memory" error to determine if your platform needs more virtual memory. Otherwise, the problem is likely to be a faulty design or an internal Synopsys error.

LINT-22

(warning) In design '%s', ref '%s' was not used.

Description

This warning indicates that there is a dangling "reference" with the given name on your design. In Synopsys terminology "reference" describes the part of a design representation that points to the actual component for a given instantiation or cell. If you have an inverter (INV) in your technology library, and you've instantiated that inverter in your design as cell13 and cell23, then each of the instantiations (cells) should own a pointer (reference) to the actual component (in this case INV). Sometimes, during the process of building or modifying a design, a reference will remain, even though all cells that refer to it have been removed or changed. Although this is a waste of memory, it should not impair the functionality of the design or the operation of Synopsys tools.

What Next

A large number of dangling references in your design can increase the memory size of the design. Sometimes these can be removed by writing the entire design out (in Synopsys database "db" format) and then reading it to Synopsys tools again. Otherwise, make a note of when the message occurs and pass the problem and an example to the Synopsys support Hotline. Dangling references indicate that the tool is not managing memory efficiently.

LINT-23

(fatal) Unable to remove attribute '%s' from db_object '%s'.

Description

This is a fatal error in the *check_design* command. Synopsys tools were unable to deallocate memory to free an object in the Synopsys internal database description for your design. The *check_design* command creates small markers on your design as it traverses the design checking for errors. These markers are removed after *check_design* is finished. This error indicates that an attempt to remove a marker failed for some reason. This is probably due to an internal memory error in Synopsys tools.

Feedback

What Next

The problem is either a faulty design or an internal Synopsys error. The *check_design* command may have destroyed your design. Report the problem to the Synopsys Hotline.

LINT-25

(warning) Design '%s' does not have any output ports.

Description

This warning message indicates that *check_design* has found a design with no output pins. Unless such designs are protected through the use of the *dont_touch* command, the *compile* command will remove instances of such designs, since they have no functionality.

What Next

This warning probably appeared because of an error in specifying a component in your design, or a component in your technology library. Check the design/library to find the problem, and correct the description of the given cell/design.

LINT-26

(fatal) Unable to db_set_attribute to db_object '%s'.

Description

This is a fatal error in the *check_design* command. Synopsys tools were unable to allocate memory to create an attribute in the Synopsys internal database description for your design. The *check_design* command creates small markers on your design as it traverses the design checking for errors. These markers are removed after *check_design* is finished. This error appears when an attempt to create a marker failed for some reason. This is probably due to a lack of memory, in which case the fatal error was accompanied by an "out of memory" error message. It is also possible that this message could occur in a badly mangled design which has recursive hierarchy.

What Next

Check the message for an "out of memory" error to determine if your platform needs more virtual memory. Otherwise, the problem is likely to be a faulty design or an internal Synopsys error.

LINT-27

(error) Object '%s' is not of class dd_design, and should not be seen by db_lint.

Feedback

Description

This message indicates that the *check_design* command has been called on a database object that is not a design. It indicates an internal problem in the user-interface for the *check_design* command, or a corrupted design database.

What Next

Recreate or re-read your design, and then run *check_design*. If this does not work, then there is probably an internal problem in the Synopsys software that should be reported to the Synopsys Hotline.

LINT-28

(warning) In design '%s', port '%s' is not connected to any nets.

Description

This warning alerts you that a port in a design is not connected to any nets. This usually indicates that a design has not been correctly specified. However, there are some situations where, as a designer, you choose to specify a port on a design for compatibility reasons, even though the port is not internal to design use. The Synopsys tools leave unconnected ports alone, with one exception; that is, you specified that a given input port is opposite or equal to another input port in a design.

What Next

Make sure that you want the named port to exist in the given design, even though it has no nets connected. Remove the port from your design if you choose.

LINT-29

(warning) In design '%s', input port '%s' is connected directly to output port '%s'.

Description

This warning alerts you to a situation where an input port in a design is directly connected to an output port. This warning is issued because some technologies do not allow such a connection. Many ASIC vendors stipulate that a buffer must be used to connect an input to an output. This restriction might or might not apply to your technology.

What Next

If directed to do so, *compile* inserts the necessary buffering to prevent a direct connection of an input port and an output port. To do this, set the boolean variable *compile_fix_multiple_port_nets* to TRUE, then compile your design. This variable also instructs *compile* to make sure that multiple output ports are not connected to the same electrical net. See the manual page on *compile_variables* for more information.

Feedback

LINT-30

(warning) In design '%s', %s.

Description

This is the terse version of a *check_design* warning message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of warnings.

What Next

Use *check_design* to obtain more information about the warning.

LINT-31

(warning) In design '%s', output port '%s' is connected directly to output port '%s'.

Description

This warning alerts you to a situation where an output port in a design is connected directly to another output port. This warning is issued because some technologies do not allow such a connection. This restriction might or might not apply to your technology.

What Next

If directed to do so, *compile* inserts the necessary buffering to make sure that multiple output ports are not connected to the same electrical net. To do this, set the boolean variable *compile_fix_multiple_port_nets* to TRUE, then compile your design.

This variable also instructs *compile* to prevent a direct connection of an input port and an output port. See the manual page on *compile_variables* for more information.

LINT-32

(warning) In design '%s', a pin on submodule '%s' is connected to logic 1 or logic 0.

Description

check_design issues this warning when it finds an instance of a hierarchical design (for example, a sub-module) that has an input connected to a logic constant. This warning is issued to verify that this is a desired connection on the submodule. Be aware that *compile* can remove logic in a design that is redundant. So, *compile* can produce designs that display this warning if it has optimized and eliminated the logic driving a submodule.

Feedback

What Next

Verify that you want the given submodule input connected to logic one or zero. If you have run *compile*, you might want to use *verify* to verify the optimized design with your original. Or, use the -verify option to *compile*, whenever feasible.

LINT-33

(warning) In design '%s', the same net is connected to more than one pin on submodule '%s'.

Description

check_design issues this warning when it finds an instance of a hierarchical design (for example, a sub-module) that has more than one input connected to the same net. This warning is issued to verify that these are desired connections on the submodule. Be aware that *compile* can remove logic in a design that is redundant. So, *compile* can produce designs that display this warning if it determines that multiple inputs on a submodule are driven by the same logical signal.

What Next

Verify that you want the given submodule inputs connected to the same logical signal. If you have run *compile*, you might want to use *verify* to verify the optimized design with your original. Or, use the -verify option to *compile* whenever feasible.

LINT-34

(warning) In design '%s', three-state bus '%s' has non three-state driver '%s'.

Description

Synopsys libraries contain descriptions of three-state driving pins on components. Synopsys tools classify a net as a three-state net if it is driven by at least one pin that has this three-state attribute. Normally, if there are multiple drivers on such nets, it is assumed that all driving pins should be three-state drivers, for correct operation of the three-state bus. This warning message indicates a situation where at least one non-three-state driver appears on a three-state net.

What Next

Verify that this is what you have intended for the given net. If the *non-three-state* driver pin specified in the message is really on a three-state driver in your ASIC technology, verify that the technology library description is correct.

Feedback

LINT-35

(information) In design '%s', net '%s' has multiple drivers. Wired OR assumed.

Description

This warning message indicates that *check_design* has found a net with multiple source pins. Synopsys tools make an assumption regarding the functionality of such *wired logic* nets. This message gives the interpretation (for example, Wired-And, Wired-Or) that will be used for this particular net. This assumption is made based on a description of wired logic functionality in the technology library used.

What Next

Make sure that you intend to have multiple drivers on the given net. Errors in specifying a design could lead to this message in a situation where wired logic is not intended.

You could also use *set_attribute* and *remove_attribute* commands to specify or remove the wired logic type for a given net.

For example,

set_attribute [get_nets z] wired_and true -type boolean

would set 'wired_and' attribute on net 'z'. While

remove_attribute [get_nets z] wired_and

would remove the 'wired_and' attribute on net 'z'.

LINT-38

(warning) In design '%s', net '%s' has multiple drivers (unknown wired-logic type).

Description

This warning message indicates that *check_design* has found a net with multiple source pins. Synopsys tools must make an assumption regarding the functionality of such *wired logic* nets. This message indicates that the tool was unable to determine the wired-logic type of the net. The assumption about wired-logic type is made based on a description of wired logic functionality in the technology library that you are using. This message could indicate that wired-logic information was not correctly specified in your technology library, or that the description of the design is incorrect.

What Next

Examine the net(s) in question, the descriptions of the components connected to the net, and their respective technology library descriptions. Make sure that the net is not the result of an error in specifying a design. Design Compiler is capable of creating wired logic

during optimization, but only in the situation where the logical *function* of that wired logic is understood (for example, Wired-OR).

You could also use *set_attribute* command to specify the wired logic type for a net with multiple drivers. The possible wired types include 'wired_and', 'wired_or' and 'three_state'.

For example,

set_attribute [get_nets z] wired_and true -type boolean

would set 'wired_and' attribute on net 'z'.

LINT-39

(warning) In design '%s', net '%s' has %s emitters, exceeding the maximum of %s.

Description

This warning message indicates that *check_design* has found a wired logic net that is illegal. Wired logic nets in ECL have a limit on the number of emitters that can legally be connected together. This limit is given by the *max_wired_emitters* attribute in the technology library.

What Next

Make sure that you intend to have this many emitters on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net of this size is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library to be sure that the specification for the maximum number of wired emitters is correct.

LINT-40

(warning) In design '%s', net '%s' has drivers with conflicting wired connection classes.

Description

This warning message indicates that *check_design* has found a wired logic net that is illegal. Wired logic nets in ECL have to meet *connection class* requirements that ensure that all drivers on the net may be legally connected together. All drivers on a wired logic net must share the same wired connection class. Each driver's class is defined in the technology library description for the driver by the *wired_connection_class* attribute.

What Next

Make sure that you intend to have these drivers on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these

drivers is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library, to be sure that the connection classes for the given components are correct.

LINT-41

(warning) In design '%s', pin '%s' is not allowed to drive wired logic.

Description

This warning message indicates that *check_design* has found a wired logic net that is illegal. All driving pins on a wired logic net must be capable of driving wired logic. The technology library description for driving pins includes the *multiple_drivers_legal* attribute, which will be TRUE if the driving pin can legally drive wired logic, and FALSE otherwise. This attribute also exists at the library level and gives a default value for components in the library.

What Next

Make sure that you intend to have these drivers on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these drivers is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a *dont_touch* attribute. Finally, you might want to check your technology library to be sure that the *multiple_drivers_legal* attributes for the given component is correct.

LINT-42

(warning) In design '%s', pin '%s' is not allowed to be driven by wired logic.

Description

This warning message indicates that *check_design* has found a wired logic net that is illegal. All load pins on a wired logic net must be capable of being driven by wired logic. The technology library description for pins includes the *multiple_drivers_legal* attribute, which will be TRUE if the driving pin can legally drive wired logic, and FALSE otherwise. This attribute also exists at the library level to give a default value for components in the library.

What Next

Make sure that you intend to have these loads on the given net. Errors in specifying a design can lead to this message in a situation where a wired logic net with these loads is not intended. The Synopsys ECL Compiler can build wired logic to meet design constraints and will legalize illegal wired logic, unless the wired logic net is protected by a

dont_touch attribute. Finally, you might want to check your technology library to be sure that the *multiple_drivers_legal* attributes for the given component is correct.

LINT-44

(information) In design '%s', %s.

Description

This is the terse version of a *check_design* informational message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of some important information.

What Next

Use *check_design* to obtain more information about the informational message.

LINT-45

(information) Design '%s' is instantiated %d times.

Description

This information message indicates that a single design is instantiated more than once in the design hierarchy below the current design. This message is issued when "check_design -multiple_designs" is used in XG mode.

What Next

Right now all DC commands handle designs with multiple instances. Each command may invoke *uniquify* under the hood to uniquify user designs if necessary.

LINT-46

(warning) Design '%s', cell '%s', pin '%s' is illegally connected,\n \tsince primary output '%s' is unconnected.

Description

This warning message occurs for ECL designs in ECL technologies that use the *primary output* designator for paired ECL outputs. By designating an output as a *primary output* your ASIC vendor has indicated that the given output must be connected before any other outputs of the same polarity are used. As an example, suppose that a component NOR2 has two positive phase outputs, X1 and X2. Suppose that the technology library description for the gate shows X1 as a primary output. Designating X1 as a primary output means that it is illegal to connect output X2 to a net unless X1 is already connected to a different net. This warning indicates a case where (to use this example) output X2 is

connected but output X1 is not connected. This is a violation of the design rule described in the technology library.

What Next

Be sure that your design was created correctly. If the Design Compiler or DFT Compiler have created an illegal design, check the technology library to be sure that the *primary_output* attribute is used properly for the given technology. If everything is correct in the technology library and *compile* has created an illegal design, contact the Synopsys Hotline with a test case.

LINT-47

(warning) In design '%s' net '%s' has a connection class violation:

Description

This warning message indicates that *check_design* has found a net that does not meet the connection class requirements described in the technology library. These connection class requirements ensure that all pins on a net can legally be connected. All pins connected together on a net must share at least one connection class in common. Each pin's class is defined in the technology library description for the pin, through the *connection_class* attribute.

What Next

Determine whether the design you are checking was (1) created manually as a netlist, or (2) created by Design Compiler (possibly from a high-level description) or DFT Compiler. If (1) is true, investigate the violation to be sure that you have specified the net correctly in your design. If (2) is true, examine the illegal net(s) created by the tool. It might not always be possible for the given net to be legalized. For example, a net might connect though hierarchy to pins whose connection classes cannot be matched. Or, other design rules, such as fanout restrictions or transition time restrictions might have made legalization for connection rules impossible. Also, check your technology library to determine whether there are level shifting components available to convert between the given connect classes.

LINT-48

(error) Not a valid part and speed grade %s for %s.

Description

This error message indicates that *check_design* has found that the part specified on the design does not exist in the technology library.

Feedback

What Next

Do a *report_library* on the technology library to get the list of parts supported. Select the one you want and attribute on the design.

LINT-49

(warning) The part %s has fewer I/O ports %d than that required by the design %d.

Description

This warning message indicates that *check_design* has found that the part specified on the design does not have enough number of input/output ports to hold the design.

What Next

Do a *report_library* on the technology library to get the list of parts supported. Select the bigger part and attribute it on the design.

LINT-50

(warning) The part %s has fewer flip-flops %d than that required by the design %d.

Description

This warning message indicates that *check_design* has found that the part specified on the design is unable to accomodate the number of flip-flops present in your design.

What Next

Do a *report_library* on the technology library to get the list of parts supported. Select the part which has more number of flip-flops than the previous part and attribute it on the design.

LINT-51

(warning) Part related checkings is not supported for the technology library.

Description

This warning message indicates that *check_design* has found that the technology library doesn't have any parts information specified in it.

What Next

Part specific checking is supported only for FPGA technology library. Make sure that you are using FPGA technology library and they have part information specified in them.

Feedback

If there is no part information, ask your vendor to supply a technology library with part information.

LINT-52

(warning) In design '%s', output port '%s' is connected directly to '%s'.

Description

This warning alerts you to a situation where an output port in a design is connected directly to Logic 1 or Logic 0. This warning is issued because some technologies do not allow such a connection. This restriction might or might not apply to your technology. Most case it is a design error.

What Next

Please check the net list carefully to make sure this case is desired, and discuss with your technology team to make sure it is allowed.

LINT-53

(error) In design '%s', net '%s' is driven by both logic 0 and logic 1.

Description

This error is issued when the check_design command encounters a shorted power ground net, which is connected to both logic 0 and logic 1. By default, only the first net of the netgroup will be reported for this error.

LINT-54

(warning) In design '%s', multiply-driven net '%s' is driven by constant %s.

Description

A multiply-driven net has a constant as one of its drivers. This is likely to be a design error.

If you intended to drive the net with a pullup/pulldown, instantiate a pullup/pulldown cell in your design instead.

What Next

Please revisit your design and make corrections.

LINT-55

(information) Design '%s' does not contain any cells or nets.

Feedback

LINT-56

(error) In design '%s', net '%s' has multiple drivers (unknown wired-logic type).

Description

This error message indicates that *check_design* has found a net with multiple source pins. Synopsys tools must make an assumption regarding the functionality of such *wired logic* nets. This message indicates that the tool was unable to determine the wired-logic type of the net. The assumption about wired-logic type is made based on a description of wired logic functionality in the technology library that you are using. This message could indicate that wired-logic information was not correctly specified in your technology library, or that the description of the design is incorrect.

What Next

Examine the net(s) in question, the descriptions of the components connected to the net, and their respective technology library descriptions. Make sure that the net is not the result of an error in specifying a design. Design Compiler is capable of creating wired logic during optimization, but only in the situation where the logical *function* of that wired logic is understood (for example, Wired-OR).

You could also use *set_attribute* command to specify the wired logic type for a net with multiple drivers. The possible wired types include 'wired_and', 'wired_or' and 'three_state'.

For example,

set_attribute [get_nets z] wired_and true -type boolean

would set 'wired_and' attribute on net 'z'.

To reduce the severity of this error message to a warning, set the variable *check_design_allow_unknown_wired_logic_type* to *true*.

LINT-57

(error) In design '%s', %s.

Description

This is the terse version of a *check_design* error message. This message is displayed when Synopsys command *check_design -summary* performs a design check and gives a summary of errors.

What Next

Use *check_design* to obtain more information about the error.

Feedback

LINT-58

(warning) In design '%s', input pin '%s' of leaf cell '%s' is connected to undriven net '%s'.

Description

This message appears when leaf cell input pin has a connected net, but the net has no driver.

LINT-59

(warning) In design '%s', input pin '%s' of hierarchical cell '%s' has one or more internal loads, but is not connected to any nets. '%s' is assumed.

Description

This message appears when hierachical cell input pin has internal load, but no driver. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

What Next

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

LINT-60

(warning) In design '%s', input pin '%s' of hierarchical cell '%s' has no internal loads and is not connected to any nets.

Description

This message appears when hierarchical cell input pin has no internal load and no driver. Synopsys tools assume a logical value (for example, logic zero or logic one) for such unconnected signals, based on the type of technology library you are using. This warning message is a notification of the assumption that is being made for the named input pin in the named design.

What Next

Verify that the assumption made by Synopsys regarding the logical value for the given signal is correct. If the assumption is not correct, then connect the floating input pin to the correct logical value in your design.

Feedback

LINT-61

(warning) In design '%s', cell '%s' is unmapped

Description

This message appears when a cell in the design is found to be unmapped

What Next

If the design has not undergone synthesis, this warning can be ignored. Otherwise, you should examine the cell that is reported to see why it is still unmapped.

LINT-62

(error) In design '%s', three-state bus '%s' has non three-state driver '%s'.

Description

Synopsys libraries contain descriptions of three-state driving pins on components. Synopsys tools classify a net as a three-state net if it is driven by at least one pin that has this three-state attribute. Normally, if there are multiple drivers on such nets, it is assumed that all driving pins should be three-state drivers, for correct operation of the three-state bus. This Error message appears when at least one non-three-state driver appears on a three-state net.

What Next

Verify that this is what you have intended for the given net. If the *non-three-state* driver pin specified in the message is really on a three-state driver in your ASIC technology, verify that the technology library description is correct.

To reduce the severity of this error message to a warning, set the variable *check_design_allow_non_tri_drivers_on_tri_bus* to *true*.

LINT-63

(warning) Net '%s' has a single tri-state driver.

Description

You receive this warning message when the *check_design* command detects that a net is driven by a single tri-state driver.

LINT-64

(warning) In design '%s', output port '%s' is driven from the outside.

Feedback

Description

This error message occurs when the *check_design* command finds the specified output port for the design is driven from the outside.

What Next

Check your design to be sure that it is connected correctly, and then run the command again.

LINT-65

(error) In design '%s', input port '%s' is connected to a multiply-driven net and the drivers include a hierarchical output port/pin.

Description

This error message occurs when the *check_design* command encounters an input port connected to a net that has multiple drivers and one or more of the drivers is a hierarchical output port or pin.

What Next

Make sure that you intend to have multiple drivers on the net driven by the indicated port.

Check that design ports are specified correctly. For example, if the direction of an output port is accidentally specified as input, then this message occurs.

Check the design to ensure that this is the functionality that you originally intended.

If you want to skip this checking, set the *check_design_allow_multiply_driven_nets_by_inputs_and_outputs* variable to *true*.

LINT-66

(error) In design '%s', net '%s' is a wire loop.

Description

This error message occurs when the *check_design* command encounters a wire loop, which is a timing loop with no cells in it.

What Next

Make sure that you break the wire loop. Wire loops might cause further problems later.

If you want to skip this checking, set the *check_design_check_for_wire_loop* variable to *false*.

LINT-67

(error) In design '%s', leaf cell output pin '%s' is connected to constant net '%s'.

Description

This error message occurs when the *check_design* command encounters an cell output pin attempting to drive a constant net. This likely reflects a design error.

What Next

Please modify the design, so the output pin is not connected to a constant.

LINT-68

(warning) In design '%s', %s port '%s' is not being used in accordance with its stated direction.

Description

This warning message occurs when a port is not being used in accordance with its stated direction. An example is when a module assigns a value to an input port. These situations can cause bad logic.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, search the source RTL for the offending assignment and correct it. The VER-1005 error message may also indicate a problem. Run the *check_design* command to verify consistency.

LINT-69

(error) In design '%s', %s port '%s' is not being used in accordance with its stated direction.

Description

This error message occurs when a port is not being used in accordance with its stated direction. An example is when a module assigns a value to an input port. These situations can cause bad logic.

What Next

Search the source RTL for the offending assignment and correct it. The VER-1005 error message may also indicate a problem. Run the *check_design* command to verify consistency.

Feedback

To bypass this error, set check_design_allow_inconsistent_input_port true. Use caution, however, because bad logic may result.

LINT-78

(information) Design '%s' has multiply instantiated designs. Use the '-multiple_designs' switch for more information.

Description

This message indicates that the current_design has one or more multiply instantiated designs. To get a list of all the multiply instantiated designs with the instance names, use *-multiple_designs* switch.

What Next

Use *-multiple_designs* to obtain more information about the multiply instantiated designs.

LINT-97

(warning) %s is not a valid error id for 'check_design' command

Description

This message indicates that the specified error id is not a valid LINT error id for *check_design* command

What Next

No action required.

LINT-98

(information) Use the 'check_design' command for \n\t more information about warnings.

Description

This message indicates that a terse version of informational messages or warnings on a design has just been displayed. To obtain more complete information, use *check_design*. This message is displayed when user used *check_design -summary* to get a summary of the potential design problems.

What Next

Use *check_design* to obtain more information about the design.

LINT-99

(information) There are %d potential problems in your design. Please run 'check_design' for more information.

Description

This message indicates that there are %d potential design problems in the user design. To obtain detailed information, use *check_design*. This message is displayed when Synopsys commands like *compile* perform a design check as part of their operation. If *compile* issued the message but completed its operation, the design might have to be read again for *check_design* to report what was wrong initially.

What Next

Use *check_design* to obtain more information about the design.

LINT-100

(warning) The design does not have back-annotated delays.

Description

check_design -post_layout issues this warning when it finds that the design does not have back-annotated delays.

What Next

To back-annotate delays onto the design, use the *read_timing* command or a series of *set_annotated_delay* command.

LINT-101

(warning) Missing %s delay annotation between pins '%s' and '%s' on cell '%s'.

Description

check_design -post_layout issues this warning when it finds a timing arc on a cell that does not have back-annotated delay.

What Next

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-102

(warning) The design does not have back-annotated cluster assignments.

Feedback

Description

check_design -post_layout issues this warning when it finds that the design does not have back-annotated cluster assignments (The clusters corresponds to the physical hierarchy of the design).

What Next

To back-annotate cluster assignments onto the design, use the *read_clusters* command to read in the *PDEF* file.

LINT-103

(warning) Missing cluster annotation on cell '%s'.

Description

check_design -post_layout issues this warning when it finds a cell which is not assigned to a cluster.

What Next

Modify the *PDEF* file before applying *read_clusters* command such that cells with missing cluster assignment are correctly assigned to a cluster.

LINT-104

(warning) The design does not have back-annotated cell locations.

Description

check_design -post_layout issues this warning when it finds that the design does not have cell locations back-annotated.

What Next

To back-annotate cell locations onto the design, use the *read_clusters* command to read in the *PDEF* file with cell location (i.e., *PDEF* version 2.0 or later)..

LINT-105

(warning) Missing cell location for cell '%s'.

Description

check_design -post_layout issues this warning when it finds a cell which does not have cell location back-annotated.

Feedback

What Next

Modify the *PDEF* file before applying *read_clusters* command such that cells with missing cell locations are correctly assigned a cell location.

LINT-106

(warning) Missing %s delay annotation from pin '%s/%s' to pin '%s/%s' on net '%s'.

Description

check_design -post_layout issues this warning when it finds a net timing arc that does not have back-annotated delay.

What Next

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-107

(warning) The design does not have back-annotated net capacitances.

Description

check_design -post_layout issues this warning when it finds that the design does not have back-annotated net capacitances.

What Next

To back-annotate net capacitances on the design, use a series of *set_load* command.

LINT-108

(warning) Missing capacitance annotation on net '%s'.

Description

check_design -post_layout issues this warning when it finds a net that does not have back-annotated capacitance.

What Next

To back-annotate capacitances on nets with missing capacitance annotation, use a series of *set_load* command.

Feedback

LINT-109

(warning) Missing orientation annotation on cluster '%s'.

Description

check_design -post_layout issues this warning when it finds a leaf level cluster that does not have back-annotated row-orientation.

What Next

Modify the *PDEF* file before applying *read_clusters* command such that clusters with missing orientations are correctly assigned an orientation.

LINT-110

(warning) Missing bounding box for cluster '%s'.

Description

check_design -post_layout issues this warning when it finds a leaf level cluster that does not have back-annotated bounding box.

What Next

Modify the *PDEF* file before applying *read_clusters* command such that clusters with missing bounding box are correctly assigned a bounding box.

LINT-111

(warning) Missing %s delay annotation for *setup* arc from pin '%s' to pin '%s' on cell '%s'.

Description

check_design -post_layout issues this warning when it finds a *setup* timing arc on a cell that does not have back-annotated delay.

What Next

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-112

(warning) Missing %s delay annotation for *hold* arc from pin '%s' to pin '%s' on cell '%s'.

Feedback

Description

check_design -post_layout issues this warning when it finds a *hold* timing arc on a cell that does not have back-annotated delay.

What Next

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-113

(warning) Missing %s delay annotation for 'preset' or 'clear' timing arc from pin '%s' to pin '%s' on cell '%s'.

Description

check_design -post_layout issues this warning when it finds a *preset* or *hold* timing arc on a cell that does not have back-annotated delay. If the warning message indicates a missing *rise* delay annotation, the timing arc with missing annotation is a *preset* timing arc; otherwise, it is a *clear* timing arc.

What Next

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-114

(warning) Missing %s delay annotation from port '%s%s' to pin '%s/%s' on net '%s'.

Description

check_design -post_layout issues this warning when it finds a net timing arc from a *port* to a pin that does not have back-annotated delay.

What Next

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-115

(warning) Missing %s delay annotation from pin '%s/%s' to port '%s%s' on net '%s'.

Feedback

Description

check_design -post_layout issues this warning when it finds a net timing arc from a pin to a *port* that does not have back-annotated delay.

What Next

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-116

(warning) Missing %s delay annotation from port '%s%s' to port '%s%s' on net '%s'.

Description

check_design -post_layout issues this warning when it finds a net timing arc from a *port* to a *port* that does not have back-annotated delay.

What Next

Modify the *SDF* file such that the missing delay is correctly described or annotate the delay directly with the *set_annotated_delay* command.

LINT-117

(warning) The design does not have any back-annotation information.

Description

You receive this warning message when the *check_design -post_layout* command is executed and it detects that the design does not have any back-annotation information.

What Next

To back-annotate delays onto the design, use the *read_sdf* command or a series of *set_annotated_delay* commands. To back-annotate cluster assignments onto the design, use the *read_clusters* command to read in the PDEF file. To back-annotate net capacitances on the design, use a series of *set_load* commands.

LINT-118

(warning) The design has '%d' cells which do not have cluster annotation on them. The cells with missing annotations represent '%f' of all cells.

Feedback

Description

You receive this warning message when the *check_design -post_layout -summary* command detects that the design has cells that do not have cluster information back-annotated on them. The message reports the total number of all such cells, and prints the percentage of cells with missing annotations.

The *check_design -only_post_layout -summary* command also issues this warning message when it finds cells with missing cluster annotations.

What Next

To back-annotate cluster assignments onto the design, correct the PDEF file and use the *read_clusters* command to read in the PDEF file.

LINT-119

(warning) The design has '%d' cells which do not have locations annotation on them. The cells with missing annotations represent '%f' of all cells.

Description

You receive this warning message when the *check_design -post_layout -summary* command detects that the design has cells that do not have location information back-annotated on them. The message reports the total number of all such cells and gives the percentage of the cells with missing annotations.

The *check_design -only_post_layout -summary* command also issues this warning when it finds cells with missing location annotations.

What Next

To back-annotate location assignments onto the design, correct the PDEF file, and use the *read_clusters* command to read in the PDEF file.

LINT-120

(warning) The design has '%d' cells annotated with clusters which have no orientation. The cells with this type of missing annotations represent '%f' of all cells.

Description

You receive this warning message when the *check_design -post_layout -summary* command detects that the design has cells that are annotated with clusters that have no orientation. The warning message reports the total number of all such cells and prints the percentage of the cells with missing annotations.

The *check_design -only_post_layout -summary* command also issues this warning message when it finds cells annotated with clusters that have no orientation.

What Next

To back-annotate cluster assignments with orientation onto the design, correct the PDEF file and use the *read_clusters* command to read in the PDEF file.

LINT-121

(warning) The design has '%d' cells annotated with clusters which have no bounding box. The cells with this type of missing annotations represent '%f' of all cells.

Description

You receive this warning message when the *check_design -post_layout -summary* command detects that the design has cells that are annotated with clusters that have no bounding box. The command reports the total number of all such cells and prints the percentage of cells with missing annotations.

The *check_design -only_post_layout -summary* command also issues this warning when it detects cells annotated with clusters that a have missing bounding box.

What Next

To back-annotate cluster assignments with a bounding box onto the design, correct the PDEF file and use the *read_clusters* command to read in the PDEF file.

LINT-122

(warning) The design has '%d' cells which have missing delay arc annotations. The cells with missing annotations represent '%f' of all cells.

Description

You receive this warning message when the *check_design -post_layout -summary* command detects that the design has cells that have missing delay arc annotations. The command reports the total number of all such cells and prints the percentage of cells with the missing annotations.

The *check_design -only_post_layout -summary* command also issues this warning when it finds cells with missing delay arc annotations.

What Next

To back-annotate delays onto the design, use the *read_sdf* command, or a series of *set_annotated_delay* commands.

Feedback

LINT-123

(warning) The design has '%d' nets which have missing delay arc annotations. The nets with missing annotations represent '%f' of all nets.

Description

You receive this warning message when the *check_design -post_layout -summary* command detects that the design has nets that have missing delay arc annotations. The command reports the total number of all such nets and prints the percentage of nets with the missing annotations.

The *check_design -only_post_layout -summary* command also issues this warning when it finds nets with missing delay arc annotations.

What Next

To back-annotate delays onto the design, use the *read_sdf* command or a series of *set_annotated_delay* commands.

LINT-124

(warning) The design has '%d' nets which do not have capacitance annotation on them. The nets with missing annotations represent '%f' of all nets.

Description

You receive this warning message when the *check_design -post_layout -summary* command detects that the design has nets that do not have capacitance information back-annotated on them. The command reports the total number of all such nets and prints the percentage of nets with missing annotations.

The *check_design -only_post_layout -summary* command also issues this warning message when it finds nets with missing capacitance annotations.

What Next

To back-annotate net capacitances on the design, use a series of *set_load* commands.

LLE

LLE-001

(Warning) Overlay file has duplicated definition at file %s line %d for the corner, this line will be ignored.

Feedback

Description

LLE overlay side file definition is based on cell namd and TR number, this warning means the same definition(same cell name and same TR number) has already been defined for the same corner. This line's duplicated definition will be ignored.

What Next

Check and correct the lle overlay side files.

LLE-002

(Warning) Cannot find .so files and no .so files is loaded!

Description

Cannot find any .so files.

What Next

Check whether the file is existing on the disk.

LLE-003

(Error) File error: %s!

Description

Cannot load .so file successfully.

LLE-004

(Warning) Overlay side file %s error! This file is ignored.

Description

LLE overlay side file definition has some severe error so this file is ignored.

What Next

Pay attention to the previous error or warning messages. Check and correct the lle overlay side files.

LLE-005

(Error) %s is not correct for loading, some functions is not found for %s.

Feedback

What Next

Check with the .so provider.

LLE-006

(Warning) File %s Line %d, %s, ignore this line.

Description

LLE overlay side file definition has some syntax error on specific lines and the line is not parsed.

What Next

Check and correct the lle overlay side files.

LLE-007

(Error) Corner name %s is used with another .so file.

Description

Corner name is already associated with one .so file.

What Next

Use a different corner.

LNK

LNK-001

(error) Cannot read link_path file '%s'.

Description

The file, specified in the *link_path* variable, cannot be read. Either the file does not exist or it is not a database file.

What Next

Check the existence of the file in the search_path using the *which* command.

Feedback

See Also

- which
- link_path

LNK-002

(information) Design '%s' is already linked.

Description

The specified design has already been linked.

What Next

Verify that this is the design that you wanted to link.

LNK-003

(information) Design '%s' was not successfully linked: %d unresolved references.

Description

A summary message indicating that the link process failed for your design.

What Next

For more information, see previous error messages.

LNK-004

(error) Unsupported LSI reference '%s' to '%s' cannot be resolved

Description

The linker tried to resolve a reference that was derived from an LSI netlist, and the reference is a form that is unsupported in the tool. This tool only supports fully name-based references from LSI netlists. Order-based or mixed order and name based references are unsupported.

What Next

Use another Synopsys tool to read the database, link it, and write it out to a new database file. This resolves the naming issue.

Feedback

LNK-005

(warning) Unable to resolve reference to '%s' in '%s'.

Description

During the link process, a reference in the design could not be resolved. This means that no match was found for the reference using the semantics of the *link_path* variable.

This message is generated only for the first instance of the reference. To see all of the instances that are unresolved, use the *link_design -verbose* command.

What Next

Examine the *link_path* variable and log messages, and use the *which* command to find out which files were loaded.

See Also

- which
- link_path

LNK-006

(warning) Cannot resolve instance %s/%s (%s).

Description

During the link process, a reference in the design could not be resolved. This message is for the instance that was trying to link to the reference.

This message is displayed only in the verbose mode.

What Next

Examine the *link_path* variable, log messages, and use the *which* command to find out which files were loaded.

See Also

- which
- link_path

LNK-007

(error) Cannot instantiate design '%s' in '%s'.

Feedback

Description

During the link process, a reference was resolved; however, the design where it was resolved cannot be instantiated due to errors in the read process.

This message is generated only for the first instance of the reference. To see all of the instances of this design that could not be instantiated, use the *link_design -verbose* command.

What Next

Examine the output of the tool when design files were loaded to see what caused the design to be in a state that cannot instantiate.

See Also

- link_design

LNK-008

(error) Cannot find port '%s' on design '%s', referenced by instance '%s'.

Description

During the link process, an instance in the design could not be resolved because a port on the instance was not found in the design. This indicates a mismatch between the pinout of the instance and the design to which it should have resolved. For example, if you have only these three instances of an FD1 in a design:

```
FD1 u1 ( .Q(n1), .CP(clock1), .D(data1));
  FD1 u2 ( .Q(n2), .CP(clock2), .D(data2));
  FD1 u3 ( .Q(n3), .CK(clock3), .D(data3));
```

There is a typo in the third instance, listing "CK" instead of "CP". By default, you receive the LNK-008 message only for the first instance.

```
Error: Cannot find port 'CK' on design 'FD1',
       referenced by instance 'u1'. (LNK-008)
```

This might seem confusing, since that instance does not have a CK port. But for a name-based reference, each instance expects at least the total of all listed ports. To see all instances that cannot be resolved, use the *-verbose* option of the *link_design* command. An example of the output

```
Warning: Cannot resolve instance top/u1 (FD1). (LNK-006)
Warning: Cannot resolve instance top/u2 (FD1). (LNK-006)
Warning: Cannot resolve instance top/u3 (FD1). (LNK-006)
```

The LNK-006 messages are generated in addition to the LNK-008 message.

Feedback

What Next

Examine the *link_path* variable, log messages, and use the *which* command to find out which files were loaded. This message could also be due to a typo in the netlist source.

See Also

- link_design
- LNK-006

LNK-009

(error) Reference '%s' to '%s' is missing the following ports: %s.

Description

The linker tried to resolve a reference that had the correct number of ports, but was unable to match the ports on the reference to those on the target design or library cell. This is an indication of a mismatch between the library and the netlist.

What Next

Verify that the library and netlist are in sync.

LNK-010

(error) Too few ports on instance '%s' of '%s' in '%s'.

Description

The specified reference to a design or library cell does not have enough ports. This indicates a mismatch between the library and the netlist.

What Next

Make sure the library is correct. Next, verify that the netlist is referencing the correct cell.

LNK-011

(error) Too many ports on instance '%s' of '%s' in '%s'.

Description

The specified reference to a design or library cell has too many ports. This usually indicates a mismatch between the library and the netlist. It can also indicate that there are multiple conflicting references to the same library cell or black box. One such conflict is two references with different pin counts.

Feedback

What Next

This error causes the link to fail. Make sure the library is correct. Next, verify that the netlist is referencing the correct cell.

If this message occurs during a black box creation, you would see additional messages. For example,

```
Error: Too many ports on instance 'u1' of '*SELECT_OP' in 'd1'. (LNK-011)
 ...Could not create black box for u1; incompatible with existing
 references
```

The first instance of *SELECT_OP for which a black box was created had fewer pins than this reference. This often happens with generic logic. Other than GTECH, generic logic is unsupported in PrimeTime. In this case, the solution is to remove the design containing the generic logic from the link path, or add a wrapper design that creates a black box at a higher level.

LNK-012

(error) Width mismatch on port '%s' of reference to '%s' in '%s'.

Description

The linker matched a bused port on an instance with a bused port on a library cell; however, the bus width is different between the two. This could indicate an incorrect library or a netlist that is out-of-date with the library.

What Next

Verify that your source is in sync with the library.

LNK-013

(error) Could not resolve %s port '%s' of reference to '%s' in '%s'.

Description

The linker could not find a port (bused or not) on an instance while resolving a reference with a target library cell. This could indicate an incorrect library or a netlist that is out of date with the library or the library is using bus type and the netlist is using bit blast type or vice versa.

What Next

Verify that your source is in sync with the library.

Feedback

LNK-014

(error) Could not resolve direction of port '%s' of reference to '%s' in '%s'.

Description

The linker matched a port on an instance with a port on a library cell, but the directions do not match. This might indicate an incorrect library or a net list that is out of date with the library.

What Next

Verify that your source is in sync with the library.

LNK-015

(Warning) Could not swap '%s' ('%s') with '%s'%s.

Description

You tried to swap a cell with a new design or library cell, and this action failed. Additional information might be included in this message and in the previous messages.

What Next

Take action based on the reasons provided in the message text.

LNK-016

(Information) %s failed due to previous errors.

Description

This is a summary message indicating that the given action was not accomplished.

What Next

Take action based on the reasons given in the text of the previous messages.

LNK-018

(Error) Cannot swap cells; design is not linked.

Description

The current design is either unlinked or partially linked. Swapping a cell for a new library cell or design can only be done in the context of a linked design.

Feedback

What Next

Link the current design, then retry your swap operation.

LNK-019

(Error) Can only swap in a single target object.

Description

The specification for the design or library cell to the *swap_cell* command resulted in more than one object. Either you specified a list or used a collection that matched multiple objects.

What Next

Narrow the search parameters so only a single object is selected.

See Also

- swap_cell

LNK-020

(Error) Cannot swap in '%s': it is the current design.

Description

The design you specified is in the current design. You cannot instantiate a design within itself.

What Next

Select a different design.

LNK-021

(Information) Previous messages occurred while trying to do: '%s'.

Description

While linking the design, an attempt was made to transfer some information from the source design files that you read to the final linked design; however, a diagnostic issue occurred. This message shows you what was attempted that caused the diagnostics.

What Next

Take action based on the messages referenced.

Feedback

LNK-023

(error) Recursive hierarchy detected in design '%s': %s.

Description

The linker detected recursive hierarchy in the design that is being linked. This is a design error. The message lists the designs that create the recursion. For example, if design A has an instance of B and design B has an instance of A, that is a recursive loop.

What Next

Remove the recursion, reread the designs, and link again.

LNK-024

(Warning) All timing information (backannotation, exceptions, etc.) is being removed from design '%s'. User-created annotations must be restored after relinking this design.

Description

When a design is linked and there is another design currently linked, the current design is unlinked before the new design is linked. When this occurs, all annotations on the currently linked design are removed. This includes any timing information loaded from the database or added with commands.

The next time the design is linked, information originally loaded from the database is automatically restored. For example, clocks stored in the database that were read in to PrimeTime are recreated on the design. However, any information that was added to the design after the link can only be restored if it was saved using the *write_script* command. For example, if you used the *create_clock* command to create a new clock, this clock is not automatically restored.

What Next

To save the state of the design before linking a new design, use the *write_script* command. Next, after relinking the design, source the script that was written to restore all annotations.

' ' '

See Also

- create_clock
- write_script

Feedback

LNK-025

(information) Link interrupted. Unlinking design: please wait...

Description

You clicked control-C to interrupt the link before it was complete. The design that was being linked will be unlinked.

What Next

No action is required.

LNK-026

(error) min library '%s' found in link_path.

Description

During the link process, a library has been found in the link path that is in use as a minimum library. This library is not put into the link path. Only the maximum library is used in the link path for minimum and maximum analysis with the *set_min_library* command.

What Next

Remove the minimum library from the value of the *link_path* variable, and ensure that the maximum library is in the link path.

See Also

- set_min_library
- link_path

LNK-028

(Warning) unable to apply some database constraints because they were cached in file '%s' and that file no longer exists.

Description

While linking the design, an attempt was made to transfer some information from the source design database files that you read to the final linked design. When this information (constraints, exceptions, and so on) is large, it is cached to the disk after an initial link. On a subsequent link, that data is reloaded and reapplied. If the file has been deleted between the first link and the subsequent link, this message is issued.

Feedback

What Next

Examine why the file was deleted, and examine why you are linking a second time. Usually this is a bug in a script, for example, executing a command that does an implicit link, followed by an explicit link. It is usually best to pick one style: implicit or explicit. Synopsys recommends that you build the design explicitly, that is, read the files that you want, then issue a *link_design* command.

See Also

- link_design

LNK-030

(information) Using '%s' as link path for instance '%s'

Description

This informational message tells you that the *link_path_per_instance* variable has been used, and a match has been found for an instance. The link path and the instance name are shown in the message. The link path should match your setting in the *link_path_per_instance* variable for the instance.

This message is displayed only if the *-verbose* option is used with the *link_design* command.

What Next

No action is required. This is strictly for your information.

See Also

- link_design
- link_path_per_instance

LNK-031

(warning) Replacing link path for '%s' with '%s'

Description

This message warns you that you have the same instance listed multiple times in the setting for the *link_path_per_instance* variable. In the following example, the *i2* instance is listed twice.

```
set link_path_per_instance [list \
   [list i2 "* lib1.db"] \
```

Feedback

```
[list i2 "* lib2.db"] \
[list i2/u1/u1 "* lib1.db"]]
```

What Next

Examine the setting for the *link_path_per_instance* variable, and ensure that only one valid link path exists per instance.

See Also

- link_path_per_instance

LNK-033

(error) Incorrect format for link_path_per_instance:%s

Description

This message tells you that the format for the *link_path_per_instance* variable is incorrect. Various things can be wrong. The variable must be a list. Each element is itself a list of exactly two elements, where the first subelement is a list of instances and the second is a valid link path. The content of the message isolates where the problem exists.

What Next

Correct the setting for the *link_path_per_instance* variable.

See Also

- link_path_per_instance

LNK-034

(information) Removing %d unneeded designs.....

Description

This message tells you that a number of designs are being deleted following a successful link. This message is issued when you issue the *link_design* command without using the *-keep_sub_designs* option, or when you issue a command that performs an implicit link.

What Next

No action is required. This is for your information.

See Also

- link_design

Feedback

LNK-035

(error) Failed to read the Verilog file in path %s.

Description

This message informs you that the read of the netlist mapped in the *set_hyperscale_config* command failed. The full netlist is used in the link instead.

What Next

Ensure that the setting in the *set_hyperscale_config* command are correct.

See Also

- link_design

LNK-036

(error) Failed to find the corresponding hierarchy configuration for the current design.

Description

This message tells you that the top level configuration in the *set_hyperscale_analysis_mode* command does not match the configuration in the *set_hyperscale_config* command. This might cause the hierarchical analysis to fail.

What Next

Check if the settings in the *set_hyperscale_analysis_mode* command are correct.

See Also

- link_design

LNK-037

(warning) Pin "%s" of cell "%s" of reference "%s" in design "%s" is dirty because %s.

Description

For you to obtain useful information, PrimeTime allows the linker to link even when an out-of-sync scenario occurs and the *link_allow_design_mismatch* variable is set to *true*. This message tells you that linker located some pins that are "dirty" because of the given reason.

Feedback

What Next

To sign-off chips, fix your design or library so this message does not occur.

See Also

- link_allow_design_mismatch

LNK-038

(warning) Pin "%s" of cell "%s" of reference "%s" in design "%s" is dirty because %s. Ignoring this pin.

Description

For you to obtain useful information, PrimeTime allows the linker to link even when an out-of-sync scenario occurs and the *link_allow_design_mismatch* variable is set to *true*. This message informs you that the linker located some pins that are "dirty" because of the given reason, and this pin is ignored during linking. That is the pin will not exist in the linked design.

What Next

To sign-off chips, fix your design or library so this message does not occur.

See Also

- link_allow_design_mismatch

LNK-039

(Information) Module '%s' in file '%s' is not used in the %s.

Description

To improve performance and capacity, HyperScale automatically replaces module netlists read by commands such as the *read_verilog* and *read_ddc* with reduced netlists created by HyperScale runs of the subblock. This message indicates that a module's HyperScale representation was successfully loaded.

Reduced netlists are automatically loaded during linking at the top level in the HyperScale technology; therefore, it is not required to read the original netlists explicitly in your scripts. However, in order to use the same scripts for all PrimeTime flows, it is strongly recommended to keep them in the scripts to get the most benefit in current and future HyperScale and PrimeTime flows.

Feedback

What Next

No action required.

LNK-040

(Information) Net %s has been identified as a power/ground net.

Description

PrimeTime delets power/ground nets after design is linked. It also applies correct constant value to all the leaf signal pins previously connected to the net.

What Next

No action is necessary.

See Also

- link_design

LNK-041

(Information) Loading library '%s' data due to accessing lib cells not linked in the current design.

Description

Timing and power data of unused library cells are not kept in memory in order to improve capacity. When those unused library cells are accessed, their data are loaded into memory. This could cause performance and capacity degradation.

What Next

Check if the data of these library cells are really needed. Remove the unused library cells from the commands if the data is not needed. If the data is needed, a better performance and capacity alternative is to use the DB.2010.03 library format.

LNK-042

(Error) Pin "%s" of cell "%s" of reference "%s" in design "%s" is dirty because %s.

Description

This message informs you that the linker located some pins that are mismatched because of the given reason.

Feedback

What Next

To sign-off chips, fix your design or library so this message does not occur.

See Also

- link_allow_design_mismatch

LNK-043

(information) Creating black box for %s/%s...

Description

This message informs you that the linker is creating "black boxes" for unresolved cells.

What Next

To sign-off chips, fix your design or library so this message does not occur.

See Also

- LNK-005
- link_path
- link_design

LNK-044

(information) Design: %s...

Description

This message informs you on the name of the design used for linking.

What Next

This information is for user to debug and check if anything is un-expected at link stage or not.

See Also

- link_path
- link_design

Feedback

LNK-045

(information) %d (%5.2f%%) library cells are unused in library %s.....

Description

This message informs you about the unused library cells in the library

What Next

This information is for user to debug and check if anything is un-expected at link stage or not.

See Also

- link_path
- link_design

LNK-046

(information) total %d library cells are unused

Description

This message informs you about the total unused library cells

What Next

This information is for user to debug and check if anything is un-expected at link stage or not.

See Also

- link_path
- link_design

LNK-047

(information) There are %lu leaf cells, ports, hiers and %lu nets in the design

Description

This message informs you about the total number of leaf cells, ports, hiers and nets in the linked design

Feedback

What Next

This information is for user to debug and check if anything is un-expected at link stage or not.

See Also

- link_path
- link_design

LNK-048

(warning) The direction of pin "%s" of cell "%s" of reference "%s" in design "%s" is %s which is incorrect. The pin direction is changed to %s.

Description

For you to obtain useful information, PrimeTime allows the linker to link even the direction of a pin of a cell does not match with the direction specified in the reference. In this scenario, Prime time automatically corrects the pin direction as specified in the reference.

What Next

To sign-off chips, fix your design or library so this message does not occur.

See Also

- link_allow_design_mismatch

LNK-049

(information) Main library is not specified. Please specify main library.

Description

Main library is not specified.

What Next

This information is for user to debug and check if anything is un-expected at link stage or not.

See Also

- link_path
- link_design

Feedback

LNK-056

(error) Instance '%s' specified in link_path_per_instance doesn't match any cells.

Description

Non Existing cell set for link path per instance which did not match with any of the cells present in the Design.

What Next

Make sure that you have used existing cell set for link path per instance.

LNK-057

(Warning) The '%s' has reached tool capacity.contact synopsys support.

LNK-064

(error) In library %s, no block views exist for block %s.

Description

The nlib directory specified to set_eco_options does not have valid blocks.

What Next

Check the existence of the ndm file provided to the set_eco_options in the search_path using the *which* command.

LNK-065

(warning) Conflicting logic on net '%s' due to pin '%s'.

Description

During linking, conflicting logic values on a net were detected.

For example, a conflict arises if two strong drivers drive a net with one carrying case analysis 0 and the other carrying case analysis 1.

In this situation, linking resolves the logic conflict to 0. This message warns you that a logic conflict occurred at the specified pin and it has been resolved to the specified logic value.

Feedback

What Next

Make sure the library and design have correct logic constant specifications. Next, verify that the netlist is referencing the correct cell.

LNK-066

(warning) Could not resolve net '%s' to either power or ground.

Description

pwell/nwell nets are not connected to any power or ground pins till Top hier. Hence, resolving them to power/ground was not possible.

What Next

Make sure that pwell/nwell are connected to power or ground net.

LNK-067

(warning) Ignoring %s in verilog file %s, as another module with same name is read already.

Description

The module name is duplicate. PrimeTime expects module names to be unique. If module name is duplicate, only the module which is read first is considered.

What Next

Please consider removing or renaming the module.

LNK-068

(error) *link_path_per_instance* variable is already set, *set_link_lib_map* command is not allowed.

Description

This error message is thrown when the *link_path_per_instance* variable setting is not empty during *set_link_lib_map* command. *set_link_lib_map* command and *link_path_per_instance* variable are mutually exclusive.

What Next

Ensure to clear setting for the *link_path_per_instance* variable.

Feedback

LNK-069

(warning) Replacing link library map file for module/instance '%s' with '%s'.

Description

This message warns you that you have previously specified the link library map file for the given module/instance with *set_link_lib_map* command.

What Next

Ensure that only one valid link library map file exists per module/instance.

LNK-070

(warning) Replacing link library map file for the top design with '%s'.

Description

This message warns you that you have previously specified the link library map file for the top design with *set_link_lib_map* command.

What Next

Ensure that only one valid link library map file exists for top design.

LNK-071

(warning) Ignoring instance library path '%s' due to incorrect format in library map file '%s' for module/instance '%s'.

Description

This message warns you that you have specified the instance library path incorrectly in library map file, this warning is issued mostly due to missing colon(:) in instance library path or missing space around the colon(:).

What Next

Ensure that each instance library path in the input file is valid.

LNK-072

(warning) Replacing link path for a instance '%s' with '%s' of module/instance '%s'.

Feedback

Description

This message warns you that you have the same instance listed multiple times in the library map file of module/instance

What Next

Ensure that only one valid link path exists for a instance in the specified library map file of module/instance.

LNK-073

(error) link library map file was set with *set_link_lib_map* command before, setting *link_path_per_instance* variable is not allowed.

Description

This error message is thrown when the link library map file was set already with *set_link_lib_map* command before set *link_path_per_instance* variable. *set_link_lib_map* command and *link_path_per_instance* variable are mutually exclusive.

What Next

Ensure no *set_link_lib_map* command issued before.

LNK-074

(warning) Conflicting pg type for %s, %s.

Description

This warning is issued when there is a conflict in deducing the PG type for a PG pin. This happens when a PG Pin defined as Power in library is connected to 1'b0 or vice versa.

What Next

Ensure consistency in PG connection.

LNK-075

(Information) Conflicting definitions found for module %s while linking and HyperScale model definition is being used.

Description

This information is issued for an instance when there are conflicting definitions found during linking of HyperScale model. Preference would be given to the definition coming from technological library rather than the one present in memory.

Feedback

What Next

link_path

MC

MC-100

(warning) Nested '%s' command detected and will be executed in serial mode.

Description

Only top-level parallel execution is supported for commands such as *redirect -bg*, *parallel_execute*, and *parallel_foreach_in_collection*. When these commands are nested, the inner command has no effect, and its contents are executed in serial order, within the context of the outer level parallel execution.

What Next

If you want to perform the nested commands in parallel mode, make sure that they are issued at the top level. Otherwise, there are no actions needed from you.

See Also

- parallel_foreach_in_collection
- post_eval

MC-101

(Severe) A change command is detected within parallel execution context and the subprocess is stopped.

Description

Cross command parallel execution directives *redirect -bg* and *parallel_execute* launch subprocesses to perform the commands in parallel. It is required that these subprocesses do not change the shared pre-computed timing data while performing their work. Therefore, change commands that can invalidate the timing status of the design and trigger incremental analysis is not allowed.

Consequently, execution of this subprocess is stopped immediately when a change command is detected. The effects of the change command are not propagated back to main process, nor are they propagated to any other commands or subprocesses executed in parallel.

Feedback

What Next

Remove the change commands from the parallel execution scope, or move them to the main process so they are execute in serial mode.

See Also

- parallel_execute
- parallel_foreach_in_collection
- post_eval
- redirect

MC-102

(Severe) A timing or noise analysis is triggered within parallel execution context and the sub process is stopped.

Description

Cross command parallel execution directives *redirect -bg* and *parallel_execute* launch subprocesses to perform the specified commands in parallel. It is required that these subprocesses do not change the shared pre-computed timing or noise data while performing their work. Therefore, commands that trigger timing and noise analysis inside subprocess and invalidate the original data of the design is not allowed.

Consequently, execution stops immediately when the command triggering timing or noise update is detected. The analysis is not performed, and the command is discarded immediately.

What Next

Remove the analysis commands requiring timing or noise update from the parallel execution scope. If they are necessary, move them out of parallel execution scope and into the main process to be executed in serial mode, only perform reporting in the subprocess.

See Also

- parallel_execute
- parallel_foreach_in_collection
- post_eval
- redirect

Feedback

MC-103

(Severe) %s is detected within parallel execution context and the subprocess is stopped.

Description

Cross command parallel execution directives *redirect -bg* and *parallel_execute* launch subprocesses to perform the specified commands in parallel. It is required that these subprocesses do not change the shared library, design, annotation, and any pre-computed timing or noise data while performing their work. To ensure this, only a subset of the PrimeTime commands and features are supported in this parallel execution mode, exceptions are detected and prohibited in the subprocess.

Consequently, parallel execution in the subprocess terminates immediately when such exception is detected, without performing any further analysis.

What Next

Remove the noted exception from the parallel execution scope. If they are necessary, leave them in the main process to be executed in serial mode, and only perform reporting commands in the parallel subprocesses.

See Also

- parallel_execute
- parallel_foreach_in_collection
- post_eval
- redirect

MC-104

(error) Command '%s' requires a linked design but linking failed.

Description

Parallel commands such as *redirect -bg*, *parallel_execute*, and *parallel_foreach_in_collection* require a design to be loaded and linked. If a design is loaded but not linked, an attempt is made to automatically link the design. This message signifies that either no design was loaded, or automatic linking has failed, and as a result execution of this command cannot continue.

What Next

Ensure that a design is properly loaded and linked.

Feedback

See Also

- link_design
- parallel_execute
- parallel_foreach_in_collection
- post_eval
- redirect

MC-105

(warning) 'redirect -bg' runs in the foreground in a distributed manager or worker process.

Description

Cross command parallel execution directive *redirect -bg* launches a subprocess to perform the specified command in the background which is not supported in a distributed manager or worker process. The specified command will instead run in the foreground and subsequent commands will only run after the *redirect* execution has completed.

What Next

No action is required because the same script should run successfully with functionally equivalent results.

See Also

- redirect

MC-106

(error) %s.

Description

See the message for details.

What Next

Ensure that the noted error is corrected and reissue the command.

See Also

- parallel_execute
- parallel_foreach_in_collection

Feedback

- post_eval
- redirect

MC-107

(warning) %s.

Description

See the message for details.

What Next

Check your setting or environment for the noted issue.

See Also

- parallel_execute
- parallel_foreach_in_collection
- post_eval
- redirect

MC-108

(error) A post_eval statement was not detected during parsing.

Description

PrimeTime pre-parses the contents of parallel iteration loops to detect and identify post_eval statements. This message signifies that an undetected post_eval statement was reached during execution. This post_eval statement cannot be executed.

What Next

Review the script containing this post_eval statement and ensure that it is used correctly.

See Also

- parallel_foreach_in_collection
- post_eval

MC-109

(error) post_eval cannot be issued from outside of a parallel iterator.

Feedback

Description

The post_eval statement can only be issued from within the context of a parallel iterator such as *parallel_foreach_in_collection*.

What Next

Review the script containing this post_eval statement, and ensure that it is used correctly.

See Also

- parallel_foreach_in_collection
- post_eval

MC-110

(error) Failed to byte-compile %s.

Description

PrimeTime byte-compiles the Tcl script body of parallel iterators and post_eval statements ahead of execution. This message signifies that an error was encountered in this process.

What Next

Review the script containing this parallel iterator to locate and fix the problem reported above.

See Also

- parallel_foreach_in_collection
- post_eval

MC-111

(warning) %s

Description

PrimeTime has encountered a problem while transferring variables between processes in the context of a parallel iterator and has issued a warning. Execution will continue, but you should review your scripts and fix the problem.

What Next

Review the script containing this parallel iterator to locate and fix the problem reported above.

Feedback

See Also

- parallel_foreach_in_collection
- post_eval

MC-112

(error) %s

Description

PrimeTime has encountered a problem while transfering variables between processes in the context of a parallel iterator and has issued an error. Execution cannot proceed and has been stopped.

What Next

Review the script containing this parallel iterator to locate and fix the problem reported above.

See Also

- parallel_foreach_in_collection
- post_eval

MC-113

(error) %s

Description

PrimeTime pre-parses the contents of parallel iteration loops to detect and identify post_eval statements and variables to transfer. This message signifies that parsing has failed due to a syntax error.

What Next

Review the script containing this parallel iterator to locate and fix the problem reported above.

See Also

- parallel_foreach_in_collection
- post_eval

Feedback

MC-114

(error) A design change command has been detected in the body of parallel_foreach_in_colection.

Description

Change commands that affect the design state are not allowed in the body of *parallel_foreach_in_collection*. The body is executed at worker processes in parallel and changes to the design state in the body could lead to unpredictable results due to the parallel nature of the iteration execution.

What Next

Review the loop body and remove the change command if possible. If the change command is intended use the *post_eval* command to execute the change command at the manager process.

See Also

- parallel_foreach_in_collection
- post_eval

MC-115

(error) %s detected during parallel_foreach_in_collection %s.

Description

Design updates (timing, noise, power, graph-based refinement, etc) and parasitics sever termination are not allowed during *parallel_foreach_in_collection*.

What Next

Review the *parallel_foreach_in_collection* loop. Ensure that the design is updated before the loop by invoking the appropriate update command. In the case of graph-based refinement it may be necessary to set the variable timing_update_include_graph_based_refinement to "always" prior to invoking *update_timing*

If the loop requires an update during execution, then it is not a candidate for *parallel_foreach_in_collection*.

See Also

- parallel_foreach_in_collection
- timing_update_include_graph_based_refinement

Feedback

MC-116

(error) A *set_user_attribute* command has been detected in the body of parallel_foreach_in_colection.

Description

The setting of user attributes is not allowed in the body of *parallel_foreach_in_collection*. The body is executed at worker processes in parallel and changes to user attributes will not persist after the loop.

What Next

Review the loop body and remove the set_user_attribute if possible or else use the *post_eval* command to execute the *set_user_attribute* command at the manager process.

See Also

- parallel_foreach_in_collection
- post_eval

MC-117

(warning) Parallel execution of command '%s' is not supported while parasitics are being read in the background. Execution will proceed sequentially instead.

Description

PrimeTime does not support parallel execution of *parallel_foreach_in_collection* while parasitics are being read in the background. Execution will proceed sequentially instead.

What Next

No action is required because the same script will run successfully with functionally equivalent results.

See Also

- parallel_foreach_in_collection

MC-118

(warning) 'parallel_execute' runs serially in a distributed manager.

Feedback

Description

Cross command parallel execution directive *parallel_execute* launches subprocesses to perform the specified commands in parallel which is not allowed in a distributed manager process. The specified commands will run serially.

What Next

No action is required because the same script should run successfully with functionally equivalent results.

See Also

- parallel_execute
- parallel_foreach_in_collection
- post_eval
- redirect

MC-119

(Severe) A graph-based refinement analysis is triggered within parallel execution context and the sub process is stopped.

Description

Cross command parallel execution directives *redirect -bg* and *parallel_execute* launch subprocesses to perform the specified commands in parallel. It is required that these subprocesses do not change the shared pre-computed graph-based refinement data while performing their work. Therefore, commands that trigger graph-based refinement analysis inside subprocess and invalidate the original data of the design are not allowed.

Consequently, the graph-based refinement analysis will not be performed. The command that invoked the analysis will complete as if graph-based refinement analysis were disabled. Execution stops immediately after this command.

What Next

To avoid this error please ensure that the graph-based refinement analysis is up to date before the parallel execution by setting the variable *timing_update_include_graph_based_refinement* to "always".

See Also

- timing_update_include_graph_based_refinement
- timing_enable_graph_based_refinement

Feedback

- parallel_execute
- parallel_foreach_in_collection
- post_eval
- redirect

MC-120

(error) %s detected during multi-user client task execution.

Description

Design updates (timing, noise, power, graph-based refinement, etc) and parasitics sever termination are not allowed during task execution of *Multi-User clients*.

What Next

Review the command called by *Multi-User client*. Ensure that the design is updated before starting Multi-User session by invoking the appropriate update command.
In the case of graph-based refinement it may be necessary to set the variable timing_update_include_graph_based_refinement to "always" prior to invoking *update_timing*

MC-121

A design change command detected during multi-user server task execution.

Description

Change commands that affect the design state are not allowed to be called in *Multi-User Server* shell.

What Next

Review the command called by *Multi-User Server*. Ensure that all global variables which can update the state of the design are set before starting Multi-User session.

MC-130

(error) Command '%s' is not supported in Distributed analysis.

Description

Multi-User commands are not supported in Distrubuted analysis (Hypergrid and Distributed Multi Scenario Analysis).

Feedback

What Next

Fix the reason of failure.

MC-131

(error) Command '%s' cannot be called outside multi-user mode.

Description

Multi-User commands (report_multi_user_server, stop_multi_user_server and stop_multi_user_client) are not supported in non Multi-User mode. It can be called only after starting Multi-User session using *start_multi_user_server* command.

What Next

Review the command flow and ensure that *Multi-User* commands are only called after switching into Multi-User mode. In case the error is still seen after calling *start_multi_user_server* command, review the command logs and see if the Multi-User session terminated due to other reasons.

MC-132

(error) Command '%s' is not supported in subprocesses.

Description

Cross command parallel execution directives redirect -bg and parallel_execute launch subprocesses to perform the commands in parallel. These subprocesses are not allowed to start Multi-User session or execute any Multi-User commands.

What Next

Remove the specified command from subprocess running in parallel, and move them to main parent process so that they are executed in serial mode.

MC-133

(error) multi-user session is already active. There is nothing to start.

Description

A Multi-User session is already active. Cannot run more than one Multi-User session at the same time.

Feedback

What Next

If the start command is invoked to change the configuration of the active Multi-User session, terminate it using *stop_multi_user_server* command and call this start command again.

MC-134

(error) Insufficient cores to start multi-user session %s

Description

Could not start Multi-User session as the minimum core required is not met.

What Next

Set desired number of cores using *set_host_options -max_cores* command and try again. If the error is due to *-max_client* requirement of the Multi-User session, try lowering the value.

See Also

- set_host_options

MC-135

(error) Invalid access group '%s'

Description

UNIX group provided with *start_multi_user_server -access_group* is invalid.

What Next

Review the value provided with -access_group option and fix it.

MC-136

(error) Failed to start multi-user server

Description

Multi-User session could not start due to one or more issues.

What Next

Review the log and fix the reason of failure.

Feedback

MC-137

(error) Failed to start multi-user client

Description

Multi-User client could not start due to one or more issues.

What Next

Review the log and fix the reason of failure.

MC-138

(error) Maximum client limit '%d' reached. Cannot start more clients.

Description

Multi-User client could not start as the maximum clients allowed in the current session are already running.

What Next

Users can queue the client by using *-queue* option with *start_multi_user_client* script. This option will enqueue the client request for the ongoing Multi-User session and the client will be started once a running client has completed execution.

MC-139

(error) %s is not accessible.

Description

Multi-User client could not start as the specified script file or output log directory does not exist, or could not be opened due to permission issues.

What Next

If the error is seen for script file, ensure it exists in the specified location and has Read access to UNIX group members. If the errors is seen for log directory, review the path specified for log file and ensure that it exists. If it still shows the error, check the permissions set on the directory and ensure group Read/Write access is enabled.

MC-140

(error) Failed to open multi-user session at client user's display.

Feedback

Description

Multi-User Client could not start as the display value provided is invalid or does not have XDisplay access permissions enabled.

What Next

Review the display environment and ensure that value set is correct. If the display value is correct and the error is still seen, check if Server user has permission to access Client user's XDisplay.

XDisplay permissions can be enabled using UNIX command *xhost +SI:localuser:serverUserName*.

MC-141

(info) Setting '%s' as display for multi-user client.

Description

Multi-User clients can be started in either Interactive (GUI) or non-interactive (batch) mode.

For interactive mode, users can specify the XDisplay configuration using *-display* option. For non-interactive mode, users have to specify the script file using *-file* option.

In case none of the options are provided, Multi-User client script picks the current display configuration and opens an interactive session on it. This message prints the display configuration picked.

What Next

In case the display value is incorrect, please update value of environment variable 'display' and try again. Alternatively, users can provide display using *-display* option.

MC-142

(error) Session ID '%s' is invalid.

Description

This message is printed in one of the following cases: 1) The multi-user session ID is incorrect. 2) The server session associated with the ID is no longer running. 3) The server session is not running on the same host as the client user.

What Next

Please fix the reason of failure and try again.

Feedback

See Also

- start_multi_user_server
- start_multi_user_client

MC-143

(error) %s does not meet access group requirements.

Description

Multi-User feature allows different client users to connect and execute commands on design run by Server user. As it involves multiple users, it relies on UNIX group ownership of files to allow different users to read/write script and log files.

To ensure smooth functioning of access requirements, the Multi-User feature has the following set of pre-requisites:

- The Server user must provide a valid UNIX group with *-access_group* option while starting Multi-User session.
- The Client user must ensure that their working directory is under group ownership of access group and group members have Read-Write access to it.
- The Client user must ensure that the group bit of their working directory is set so that files written inside it will pick up the correct group ownership.
- In case Client user provides a script file (using *-file* option), they must ensure that it is under ownership of access_group and group members have Read access to it.
- In case the log file specified by Client (using *-output* option) already exists, the user must ensure that it is under group ownership of access_group and group members have Read-Write access to it.

The above mentioned requirements ensure that output logs are written with group ownership of *access_group* and different users (Server and Clients) have permissions to read, write or delete the file.

The requirements are also necessary for input scripts to ensure that Server user can read or source client files properly.

Feedback

What Next

Please ensure that all pre-requisites are met and make neccessary changes. Use the following UNIX commands to meet requirements:

- To change group ownership of a file or directory: *chgrp [GROUP_NAME] [FILE_NAME]*
- To provide Read-Write permissions to group members and set group bit: *chmod g+rws [FILE]*

MC-144

(Information) Client logs will be available at '%s'

Description

Logs for the current Multi-User Client session can be found at the given location.

What Next

Please check the logs to know the status of the current client.

MC-145

(Error) multi-user interactive mode is not supported after 'gui_start' command is called.

Description

Running GUI session of PrimeTime before starting Multi-User session initializes GUI infrastructure in a way that is not compatible with running Multi-User in Interactive mode.

What Next

This session will not support Multi-User Interactive feature. To run Multi-User in interactive mode, a new non-GUI session of PrimeTime will be required.

MC-146

(Warning) Interactive client will not be supported in the current multi-user session.

Description

Running GUI session of PrimeTime before starting Multi-User session initializes GUI infrastructure in a way that is not compatible with running Multi-User in Interactive mode.

What Next

This session will not support Multi-User Interactive feature. To run Multi-User in interactive mode, a new non-GUI session of PrimeTime will be required.

Feedback

MC-147

(Error) multi-user server could not start client due to one or more reasons.

Description

The current Multi-User Client could not start due to one or more issues (i.e, max_client limit reached, display_port not accessible by Server, etc). Please check the Server log for more details.

What Next

Please check the Server log or Server console for more details and fix the reason of failure.

MC-150

(Information) Switching %s multi-user mode.

Description

PrimeTime has been switched into (or out of) the Multi-User mode.

What Next

This is an informational message. No action is required.

MC-151

(Information) Shutting down client '%s'

Description

Multi-User client has been terminated.

What Next

This is an informational message. No action is required.

MC-152

(Information) Starting multi-user client.

Description

Multi-User client has been started.

Feedback

In interactive mode, a PrimeTime GUI instance will be started on the display environment provided. In batch mode, the output log of the commands will be dumped in the log file provided.

What Next

This is an informational message. No action is required.

MC-153

(error) Multi User session is not supported when GUI console is active.

Description

Multi-User session is only supported in non-GUI PrimeTime console.

What Next

To start Multi-User session, terminate the running GUI console using "gui_stop" command and try again.

See Also

- gui_start
- gui_stop

MC-154

(error) Cannot update variable '%s' in active multi-user session.

Description

Multi-User variables change the properties of a Multi-User session and needs to be set before starting Multi-User Server.

What Next

Try setting the variable again after stop_multi_user_server command is called.

MC-155

(warning) Log file '%s' will not be created as the multi-user log level is set as 'none'.

Description

The log file specified with *start_multi_user_server -log* option will not be created as the variable *multi_user_logging_level* is set as 'none'.

Feedback

What Next

Restart the Multi-User session after setting the variable multi_user_logging_level to a different value.

MC-156

(warning) Multi user client (%s) could not start due to process fork failure.

Description

Multi user client could not start due to process fork failure from the operating system. The client will be enqueued to pending client list and server will re-try to fork a child process to execute the specified client request.

If the client does not wish to wait in the pending queue, please use the *stop_multi_user_client* command at the server shell.

The most common reasons for fork failures are listed below:

```
* Fork failed to allocate the necessary kernel structures because there
 are not enough memory resources available.
    Fork typically requires enough memory to allow worst-case scenario of
 doubling memory consumption.
  * Not enough memory for kernel to copy page tables and other accounting
 information of parent process.
  * Global process limit could be blocking creation of the process.
```

Please refer to the fork man page for more info.

What Next

Check your system or environment settings and take necessary actions.

See Also

- start_multi_user_server
- start_multi_user_client

MC-157

(information) Multi user client has been terminated by the server.

Description

Multi user client process has been terminated by the server using either *stop_multi_user_client* or *stop_multi_user_server* command.

Feedback

What Next

Check the reason of termination from the server user.

See Also

- start_multi_user_server
- start_multi_user_client

MC-158

(warning) Starting multi-user session with -allow_remote_clients may have security implications.

Description

By default multi-user analysis requires the client user to be logged in to the host where the server is running. This allows the server user to control access to the access to the multi-user analysis by controlling access to the host machine upon which the server is running by leveraging standard and trusted system security protocols (e.g. SSH).

By using the *-allow_remote_clients* option the server listens for and accepts incoming client connection requests from remote hosts. This can bypass normal security protocols (such as SSH) that may have been enabled on the server host.

This option should be used with caution particularly if any restricted information is being loaded by the multi-user server.

What Next

Review if *-allow_remote_clients* is required and if not, restart multi-user session by using *stop_multi_user_server* and *start_multi_user_server* commands.

See Also

- start_multi_user_server
- stop_multi_user_server

MC-201

(error) Variable '%s' was read before being written in an iteration of body.

Description

This message signifies that PrimeTime has identified a variable access problem during execution of one iteration of the body of a parallel iterator construct.

Feedback

When a variable is both read and written within the body block, every read must be preceded by a write in the same iteration. Otherwise, reading a variable in one iteration could potentially return a value written by a previous iteration, and since the relative order in which body iterations are executed is unspecified in the context of parallel iterators, this could lead to unpredictable results.

Here is an example of a script for which this message is issued:

```
set total_max_slack 0
  parallel_foreach_in_collection iter [get_pins] {
    set iter_max_slack [get_attribute $iter max_slack]
    if {$iter_max_slack > 0} {
       continue
    }
    set new_total [expr $total_max_slack + $iter_max_slack]; # read
 access
    if {$new_total > 100.0} {
      echo "Design has too much negative slack!"
      break
    } else {
      set total_max_slack $new_total; # write access
    }
  }
```

In the example above, the purpose of the total_max_slack variable is to aggregate results, and therefore both the read and write accesses to this variable in the context of the parallel iterator need to be moved to a post_eval statement.

This is a potential fix for the example script:

```
set total_max_slack 0
  parallel_foreach_in_collection iter [get_pins] {
    set iter_max_slack [get_attribute $iter max_slack]
    if {$iter_max_slack > 0} {
       continue
    }
    post_eval {
      set new_total [expr $total_max_slack + $iter_max_slack]
      if {$new_total > 100.0} {
        echo "Design has too much negative slack!"
        break
      } else {
        set total_max_slack $new_total
      }
    }
  }
```

What Next

Review the script containing this parallel iterator to locate and fix the problem reported above.

Feedback

See Also

- parallel_foreach_in_collection
- post_eval

MC-202

(error) Variable '%s' was both written in post_eval and read in body.

Description

This message signifies that PrimeTime has detected a specific access pattern on the reported variable which indicates confusion about the intended purpose of this variable.

When a variable is written within post_eval, in the context of a parallel iterator construct, it is considered to be an output of the loop. This is because the intent of post_eval statements is to aggregate results or make persistent changes to the state of the design, such as setting attributes.

Variables written in a post_eval statement should never be read elsewhere within body (except from another post_eval statement) as that would violate the assumption that the variable's intent is to serve as an output.

Additionally, since the relative order in which body and post_eval statements are executed is unspecified in the context of parallel iterators, this could lead to unpredictable results.

Here is an example of a script for which this message is issued:

```
set total_max_slack 0
  parallel_foreach_in_collection iter [get_pins] {
    set iter_max_slack [get_attribute $iter max_slack]
    if {$iter_max_slack > 0} {
       continue
    }
    set new_total [expr $total_max_slack + $iter_max_slack]; # read
 access
    post_eval {
      if {$new_total > 100.0} {
        echo "Design has too much negative slack!"
        break
      } else {
        set total_max_slack $new_total; # write access
      }
    }
  }
```

In the preceding example, the purpose of the total_max_slack variable is to aggregate results, and therefore both the read and write accesses to this variable in the context of the parallel iterator need to be moved to a post_eval statement.

Feedback

This is a potential fix for the example script:

```
set total_max_slack 0
  parallel_foreach_in_collection iter [get_pins] {
    set iter_max_slack [get_attribute $iter max_slack]
    if {$iter_max_slack > 0} {
       continue
    }
    post_eval {
      set new_total [expr $total_max_slack + $iter_max_slack]
      if {$new_total > 100.0} {
        echo "Design has too much negative slack!"
        break
      } else {
        set total_max_slack $new_total
      }
    }
  }
```

What Next

Review the script containing this parallel iterator to locate and fix the problem reported above.

See Also

- parallel_foreach_in_collection
- post_eval

MC-203

(error) Variable '%s' was written both in body and in post_eval.

Description

This message signifies that PrimeTime has detected a specific access pattern on the reported variable which indicates confusion about the intended purpose of this variable.

When a variable is written within post_eval in the context of a parallel iterator construct, it is considered to be an output of the loop. This is because the purpose of post_eval statements is to aggregate results or make persistent changes to the state of the design, such as setting attributes.

On the other hand, variables written within body are considered to be temporary variables. These variables are not guaranteed to persist after the parallel iterator construct has completed. Additionally, variables modified in body might be automatically sampled and transfered from body to post_eval at the time of post_eval submission if they are found to be referenced in post_eval. See details of this mechanism in the man page for parallel_foreach_in_collection.

Feedback

Variables should never be both written in a post_eval statement and written within body (except from another post_eval statement) as those represent conflicting intentions.

Here is an example of a script for which this message is issued:

set has_non_vio_endpoint false set num_pba_recalculations 0 parallel_foreach_in_collection endpoint [all_registers -data_pins] { if {[get_attr $endpoint max_slack] >= 0.0} { # Definitely non-violating - jump to next iteration set has_non_vio_endpoint true continue } set worst_path [get_timing_path -to $endpoint -pba path] if {[get_attr $worst_path slack] >= 0.0} { post_eval { set has_non_vio_endpoint true incr num_pba_recalculations } } else { echo "found violating endpoint [get_attr $endpoint full_name]" } }

In the preceding example, the purpose of the has_non_vio_endpoint variable is to aggregate results, and therefore all accesses to this variable in the context of the parallel iterator need to be moved to a post_eval statement.

This is a potential fix for the example script:

```
set has_non_vio_endpoint false
  set num_pba_recalculations 0
  parallel_foreach_in_collection endpoint [all_registers -data_pins] {
    if {[get_attr $endpoint max_slack] >= 0.0} {
      # Definitely non-violating - jump to next iteration
      post_eval {
        set has_non_vio_endpoint true
      }
      continue
    }
    set worst_path [get_timing_path -to $endpoint -pba path]
    if {[get_attr $worst_path slack] >= 0.0} {
      post_eval {
        set has_non_vio_endpoint true
        incr num_pba_recalculations
      }
    } else {
      echo "found violating endpoint [get_attr $endpoint full_name]"
    }
  }
```

What Next

Review the script containing this parallel iterator to locate and fix the problem reported above.

See Also

- parallel_foreach_in_collection
- post_eval

Feedback

MC-204

(error) Variable '%s' has not been transfered before being read in post_eval in this iteration.

Description

This message signifies that PrimeTime has identified a variable access problem during execution of one iteration of a parallel iterator construct.

The variable mentioned was both written in the body and read in *post_eval*, but *post_eval* read a stale value because the variable had not been transfered.

This message is issued under the following conditions:

- The variable being read in *post_eval* was not written in the body *in this iteration*, even though it was written in body in other iterations. For example:

```
parallel_foreach_in_collection pin $pin_collection {
  if {[get_attribute $pin is_hierarchical] == true} {
    set slack [get_attr $pin max_slack]
  }
  post_eval {
    echo "[get_attr $pin full_name] : $slack"
    report_timing -to $pin
  }
}
```

  Since the slack variable is not written in every iteration, some iterations of *post_eval* can read a stale value from the previous iteration. Here is a potential fix for the preceding example:

```
parallel_foreach_in_collection pin $pin_collection {
  if {[get_attribute $pin is_hierarchical] == true} {
    set slack [get_attr $pin max_slack]
    post_eval {
      echo "[get_attr $pin full_name] : $slack"
      report_timing -to $pin
    }
  }
}
```

- PrimeTime is unable to identify and transfer the variable to *post_eval*.

  References to variables in *post_eval* are found by parsing the script upfront, and only variable references beginning with a '$' can be identified. *post_eval* can call Tcl procedures, but the parsing mechanism for variable identification does not follow

Feedback

called Tcl procedures. Under some situations, it might be necessary to add additional references to variables in order for them to be detected.

For details about the variable identification mechanism, see the man page for *post_eval*.

What Next

Review the script containing this parallel iterator to locate and fix the problem reported above.

See Also

- parallel_foreach_in_collection
- post_eval

MC-205

(warning) Parallel processing cannot proceed due to process fork failure (%s).

Description

Parallel processing fork attempt failed with the given error code from the operating system. The most common error codes are listed below:

```
- ENOMEM
      * fork failed to allocate the necessary kernel structures because
 there are not enough memory resources available.
        Fork typically requires enough memory to allow worst-case
 scenario of doubling memory consumption.
  - EAGAIN
      * Not enough memory for kernel to copy page tables and other
 accounting information of parent process.
      * Global process limit could be blocking creation of the process.
```

Please refer to the fork man page for more info.

What Next

Check your system or environment settings that correspond to the reported error code.

See Also

- parallel_execute
- parallel_foreach_in_collection
- post_eval
- redirect

Feedback

MC-206

(information) Up to %d workers ran in parallel.

Description

This message shows the maximum number of workers that ran in parallel during the execution of *parallel_execute* or *parallel_foreach_in_colection*.

See Also

- parallel_execute
- parallel_foreach_in_collection

MC-207

(error) Multi user session cannot start due to insufficient resource to fork a client process (%s).

Description

The current session does not meet memory or core requirement to fork a multi user client process. The given error was issued from the operating system while attempting to fork a process. The most common error codes are listed below:

```
- ENOMEM
      * fork failed to allocate the necessary kernel structures because
 there are not enough memory resources available.
        Fork typically requires enough memory to allow worst-case
 scenario of doubling memory consumption.
  - EAGAIN
      * Not enough memory for kernel to copy page tables and other
 accounting information of parent process.
      * Global process limit could be blocking creation of the process.
```

Please refer to the fork man page for more info.

What Next

Check your system or environment settings that correspond to the reported error code.

See Also

- start_multi_user_server

MC-208

(error) No available ports found in the specified range.

Feedback

Description

Multi-user server was unable to find any available port in the specified range to establish a communication channel between server and client session.

What Next

Please check the specified range and provide a valid rage of available ports. Please check if the specified range of ports are already in use or have any firewall restrictions applied on them.

See Also

- start_multi_user_server

MC-209

(error) Failed to setup socket connection at server host to listen for client connection requests %s.

Description

Multi-user server failed to setup socket connection due to one or more reasons. Please review the possible causes below and try again: 1) A firewall or security setting on the system may block or restrict the socket's ability to create, bind or listen for connection. 2) The system may have limitations on the number of sockets that can be created or the number of connections that be listened to simultaneously. 3) Networking issues such as network hardware failures, misconfiguration or high network traffic. 4) The ports specified using -port option are already in use or require administrative privileges.

What Next

Please review the possible reasons of failure and resolve them.

See Also

- start_multi_user_server

MC-210

(error) The range of ports specified [%s] is invalid.

Description

Multi user server was unable to start a listening socket at the specified range ports due to one of the following reasons: 1) The minimum port number in the specified range may be greater than the maximum port number. 2) The range specified does not include any valid

Feedback

port i.e, min port > 65535. 3) The range specified contains more than 1 '-' characters. Eg: 100-200-300. The expected syntax is -port "min_port-max_port".

What Next

Please correct the specified port range and try again.

See Also

- start_multi_user_server

MDBG

MDBG-2

(error) Did not specify either the -from or -to option.

Description

You receive this message because you executed the *report_etm_arc* command and did not specify a *-from* option *from_object* value or a *-to* option *to_object* value. For the *-from* option, you must specify one of the following valid values: *-fall_from*, *-from*, or *-rise_from*. For the *-to* option, you must specify one of the following valid values: *-fall_to*, *-rise_to*, or *-to*.

What Next

Reexecute the *report_etm_arc* command, specifying the missing option.

See Also

- report_etm_arc

MDBG-3

(Error) Specified invalid 'from' object. No port/clock matched.

Description

You receive this message because you executed the *report_etm_arc* command and did not specify a valid port/clock as the value for the *-from*, *-rise_from*, or *-fall_from* option.

What Next

Reexecute the *report_etm_arc* command, specifying a valid startpoint (port/clock).

Feedback

See Also

- report_etm_arc

MDBG-4

(error) Specified invalid 'to' object. No port/clock matched.

Description

You receive this message because you executed the *report_etm_arc* command and did not specify a valid port/clock as the value for the *-to*, *-rise_to*, or *-fall_to* option.

What Next

Reexecute the *report_etm_arc* command, specifying a valid endpoint (port/clock).

See Also

- report_etm_arc

MDBG-5

(error) Specified invalid value for -arc_type option.

Description

You receive this message because you executed the *report_etm_arc* command and specified an invalid *arc_type* value for the *-arc_type* option. Valid values are: *clock_gating_hold*, *clock_gating_setup*, *hold*, *max_combo_delay*, *max_seq_delay*, *min_seq_delay*, *min_combo_delay*, *recovery*, *removal*, and *setup*.

What Next

Reexecute the *report_etm_arc* command, specifying a valid *arc_type* value for the *-arc_type* option.

See Also

- report_etm_arc

MDBG-6

(warning) Cannot open the file '%s' for the ETM report.

Feedback

Description

You receive this message because you executed the *report_etm_arc* command and specified an invalid file name for the *er_file_name* value of the *-etm_report* option.

What Next

Reexecute the *report_etm_arc* command, specifying a valid file name for the *er_file_name* value of the *-etm_report* option.

See Also

- report_etm_arc

MDBG-7

(warning) Cannot open the file '%s' for the netlist report.

Description

You received this message because you executed the *report_etm_arc* command and specified an invalid file name for the *nr_file_name* value of the *-netlist_report* option.

What Next

Reexecute the *report_etm_arc* command, specifying a valid file name for the *nr_file_name* value of the *-netlist_report* option.

See Also

- report_etm_arc

MDBG-8

(error) Cannot specify more than one object to -from and -to options.

Description

You receive this message because you executed the *report_etm_arc* command and specified more than one value for either the *from_object* value of the *-from* option or the *to_object* value of the*-to* option.

What Next

Reexecute the *report_etm_arc* command, specifying one object for both the *-from* and the*-to* options. You can issue this command more than once to get multiple arcs.

Feedback

See Also

- report_etm_arc

MDBG-9

(error) Specified invalid path_name '%s' for the -include option.

Description

You receive this message because you executed the *report_etm_arc* command and specified an invalid *path_type_list* value for the *-include* option. The only valid values are *clock_path* and *netlist_path*.

What Next

Reexecute the *report_etm_arc* command, specifying one (or both) of the valid *path_type_list* values for the *-include* option.

See Also

- report_etm_arc

MDBG-10

(error) Specified invalid options for a constraint arc.

Description

You receive this message because you executed the *report_etm_arc* command and specified a value for the *-arc_type* option that does not agree with the *-from* option *from_object* value or the *-to* option *to_object* value. Specify a port for the *-from* option and a clock for the *-to* option to obtain the constraint arc.

What Next

Reexecute the *report_etm_arc* command, specifying valid values for the *-from* and *-to* options.

See Also

- report_etm_arc

MDBG-11

(error) Specified invalid options for a sequential arc.

Feedback

Description

You receive this message because you executed the *report_etm_arc* command and specified an argument for the *-arc_type* option that does not agree with the *-from* option *from_object* value or the *-to* option *to_object* value. Specify a clock for the *-from* option and a port for the *-to* option to obtain the sequential arc.

What Next

Reexecute the *report_etm_arc* command, specifying valid values for the *-from* and *-to* options.

See Also

- report_etm_arc

MDBG-12

(error) Specified invalid options for a combinational arc.

Description

You receive this message because you executed the *report_etm_arc* command and specified an argument for the *-arc_type* option that does not agree with the *-from* option *from_object* value or the *-to* option *to_object* value. Specify a port for the*-from* option and a port for the *-to* option to obtain the combinational arc.

What Next

Reexecute the *report_etm_arc* command, specifying valid options for the *-from* and *-to* options.

See Also

- report_etm_arc

MDBG-13

(error) Specified invalid options for a non-sequential check arc.

Description

You receive this message because you executed the *report_etm_arc* command and specified an argument for the *-arc_type* option that does not agree with the *-from* option *from_object* value or the *-to* option *to_object* value. Specify a port for the*-from* option and a port for the *-to* option to obtain the non-sequential check arc.

Feedback

What Next

Reexecute the *report_etm_arc* command, specifying valid options for the *-from* and *-to* options.

See Also

- report_etm_arc

MENU

MENU-001

(Error) Menu name is empty.

Description

An empty string was given as the menu name option value.

What Next

Provide a non-empty menu name.

MENU-002

(Error) The menu name needs to be a full hierarchical menu name.

Description

A full hierarchical menu name needs to be specified for the menu name. An example: "&File->Exit".

What Next

Check the option value of the -menu option.

MENU-003

(Error) The -anchor_offset option value needs to be a positive/negative integer and not zero.

What Next

Correct the option value of the -anchor_offset option.

Feedback

MENU-004

(Error) -anchor_offset option needs to be specified when -anchor_item option is present.

MENU-005

(Error) %s option value is specified incorrectly.

What Next

Check and correct the option value for the specified option.

MENU-006

(Error) -anchor_item option needs to be specified when -anchor_offset option is present.

MENU-007

(Error) Anchor menu item '%s' not found.

What Next

Check the spelling of the option value of the -anchor_menu option. Make sure that the anchor menu item already existed before using it as anchor_menu option value in the gui_create_menu command call.

MENU-008

(Error) Menu bar items must be popup menus.

Description

First-level items on the menu bar must be popup menus.

What Next

Check and correct the option value of the -menu option.

MENU-012

(Error) Menu root: %s not found.

What Next

Check and correct the option value of the -menu_root option.

Feedback

MENU-013

(Warning) Hotkey string: %s is either not supported or reserved by system for other use.

What Next

Please check and correct the option value of the -hot_key option. This hotkey key combination may not be supported or has been reserved by the application for some other use.

MENU-014

(Error) Duplicate menu item: %s .

Description

Another existiing menu item already has this menu name.

MENU-015

(Error) %s option is specified with invalid value: %s.

What Next

Check and correct the option value of the specified option.

MENU-016

(Error) Cannot specify both -anchor_offset and -position options.

MENU-017

(Error) -position option value must not be a negative integer.

Description

Position option value must be zero or a positive integer. It specifies the position of the menu item within the parent popup menu.

MENU-018

(Warning) Specified hotkey %s for this menu item %s will be ignored. Hotkey is already in use for %s menu item.

Feedback

Description

This hotkey has already been mapped to another existing menu item. It will be ignored and not set for this menu item.

What Next

Change the -hotkey option value to specify another hotkey or remove this option.

MENU-019

(Error) Menu item '%s' not found.

Description

The specified menu item was not found in the currently active window. It could not be executed.

What Next

Check the menu name to make sure it matches an existing menu item in the active window.

MENU-020

(Error) There is no active main window.

Description

No active main window was found.

What Next

Activate a main window before executing this command.

MENU-021

(Error) Menu %s is not a popup menu item.

What Next

Add menu items to a popup menu, not to an item with associated command or action. Popup menus are created implicitly by specifying a full hierarchical menu name.

MENU-022

(Warning) Menu bar items must be popup menus. %s not added.

Feedback

Description

First-level items on the menu bar must be popup menus.

What Next

Do not explicitly create popup menus in hierarchical menus. Pop-up menus are created implicitly by creating command menu items with full hierarhcical names. For example, creating a menu with the menu name "&File->&Open..." creates the "File" pop-up menu in the menu bar.

MENU-023

(Error) Window named %s provided for the -window option was not found.

Description

The provided window name is not valid.

What Next

Check the spelling of the window name. If you omit the -window option, the currently active top-level main window will be used.

MENU-024

(Error) Window named was not provided and there is no active main window.

Description

When no window name is provided for the -window option, the currently active top-level window is used. However, no active top-level main window eixsts.

What Next

Create an instance of the top-level main window on which you wish to operate, then provide its name with the -window option or activate the window and omit the -window option.

MENU-025

(Warning) There are no toolbars in the specified window.

Description

Since there are no toolbars in the specified window, the operation resulted in no action.

Feedback

MENU-026

(Error) There is no toolbar with the name %s.

Description

A toolbar with the given name could not be found. Therefore, the operation resulted in no action.

MENU-028

(Error) Options %s are not supported with the -window option.

Description

Supported options for menu attribute setting in a specific window are: -menu_text, -tooltip, and -help_string.

MEXT

MEXT-1

(error) Design '%s' does not have any connections between cells. Model extraction is not allowed on such designs.

Description

You received this message because you executed the *extract_model* command but the extractor detects that the netlist to be extracted does not have any effective net connectivities among the cells that are instantiated from the library.

What Next

Please inspect the netlist and make sure there are effective connectivities among cell instances. This is to avoid improperly exposing timing related information in the libraries you are using.

MEXT-2

(warning) Variable 'extract_model_use_conservative_current_slew' is set to 'true' while design is in 'worst_arrival' slew propagation mode.The variable is not effective in this mode and therefore ignored in extraction.

Feedback

Description

You received this message because you executed the *extract_model* command with variable 'extract_model_use_conservative_current_slew' set to 'true' while the design is in 'worst_arrival' slew propagation mode. The 'worst_arrival' slew propagation mode makes this model extraction variable not effective and therefore its value is ignored and it will have no impact on model extraction.

What Next

Please decide what model you want. If you want the model to propagate the worst conservative slew calculated from the context slews set on input ports, put the design in 'worst_slew' mode and set the model extraction variable to 'true'. If you want the model to propagate real path specific slew regardless of any context slews propagated from other paths, set the model extraction variable to 'false'. This makes the model match the netlist better if the timing report of the netlist is performed in 'worst_arrival' slew propagation mode.

MEXT-03

(error) The value '%s' set for the modeling environment variable '%s' is illegal.

Description

You receive this message because the value you set for the specified variable is illegal. If it is for number of table index points, it has to be a positive integer; if it is for the maximum limit of the table index, it has to be a non-negative floating point number.

What Next

Adjust the settings of these PrimeTime environment variables before executing model extraction.

MEXT-3

(warning) The %s '%s' timing arc extracted from pin '%s' to pin '%s' has only '%s' tables. They are copied to make the missing '%s' tables.

Description

You received this message because the sequential paths contribute to the specified timing arc only have the specified transition applicable. The resulting timing arc is half-unate. It could be caused by disable timing, false paths or cells with half-unate timing arcs in the path. Because there are tools, such as LibraryCompiler, etc. which do not accept half unate sequential arcs. The extracted model has copied the existing half to create the missing half.

Feedback

What Next

Please verify the path setup and confirm that the arcs are what you expected.

MEXT-4

(warning) Detected max_transition violation in the circuit to be extracted.

Description

You receive this message if the circuit you are currently extracting has max_transition violations. The resulting model can do max_transition checking only at its boundaries; therefore, the model will be inaccurate because it does not reproduce the errant behavior.

The current problem might be caused by an unrealistically low value of the maximum transition time. Many ASIC libraries supply a *default_max_transition* or a *max_transition* attribute on the gate outputs. If a gate in the design does not have a *max_transition* attribute in its library definition, the *extract_model* command uses the value of the *extract_model_transition_limit* variable; the default is 5.0.

What Next

Correct the violations using timing analysis and synthesis on the original circuit, or reset the maximum transition time to a higher value. Then reexecute *extract_model*.

MEXT-5

(warning) Some pins do not have clock defined. One example is pin '%s'. Paths to and from such pins are ignored. Run check_timing for details.

Description

You receive this message because the *extract_model* command did not find a clock for some pins. Transparent latches and flip-flops in a design you want to extract must have a clock defined for them. This message warns you that *extract_model* is ignoring all paths to and from such pins that have no clock.

What Next

If it is acceptable to you for *extract_model* to ignore paths to and from such pins, no action is required on your part. Otherwise, use the *create_clock* command to define all design clocks on the pins or clock networks. Then reexecute *extract_model*.

In the future, to prevent receiving this message, first execute the *check_timing* command to detect any clock pins that are missing clocks. Create the missing clocks, then execute *extract_model*.

Feedback

MEXT-6

(warning) Environment variable '%s' has not been set during this session. Using default value '%s'.

Description

You receive this message if the specified environment variable is not set. This message informs you that the default value is being used.

What Next

If it is acceptable to you for the specified default value to be used for this environment variable, no action is required on your part. Otherwise, set this variable to one of its allowed values using the command *set variable value*. If you want to set the value only for the current session, you can enter this command at the pt_shell prompt or place it in a script file, which you then execute. If you want the variable value to persist, you can enter it in your .synopsys_pt.setup file.

MEXT-7

(warning) Environment variable 'extract_model_tolerance' has a value that is too low. Using minimum value '%s'.

Description

You receive this message if the *extract_model_tolerance* variable is set with a value less than 0.02. The behavior of the extractor degrades sharply when tolerances are below these values. This message informs you that the specified minimum value is being used instead.

What Next

If it is acceptable to you for the *extract_model* command to use the specified minimum value, no action is required on your part. Otherwise, set the *extract_model_tolerance* variable to a value greater than 0.02. Then reexecute *extract_model*.

MEXT-8

(warning) Environment variable 'extract_model_tolerance' has a value that is unreasonably high. Using maximum value '%s'.

Description

You receive this message if the *extract_model_tolerance* variable is set with a value greater than .50. There is little benefit in extractor speed or output file size beyond 50%

tolerance. This message informs you that the specified maximum value is being used instead.

What Next

If it is acceptable to you for the *extract_model* command to use the specified maximum value, no action is required on your part. Otherwise, set the *extract_model_tolerance* variable to a value less than 0.50. Then reexecute *extract_model*.

MEXT-9

(error) extract_model is not supported when %s.

Description

This message indicates that *extract_model* cannot be performed because certain flow settings or features are in use.

For example,

- In a block-level HyperScale analysis that has top-level context data applied, the *extract_model* command cannot evaluate the boundary timing across different I/O slew or load conditions.
- When the constraint extraction flow is enabled, detailed delay calculation and SI analysis are disabled, and thus the *extract_model* command is unable to compute realistic timing for the model.

For example, in a block-level analysis of a HyperScale flow

What Next

If an ETM must be created, disable the indicated feature before extracting the model.

MEXT-10

(error) Unknown format '%s' for the -format option.

Description

You received this message because you executed the *extract_model* command and specified an argument for the *-format* option that was neither *db* or *lib*. These are the only valid arguments for the *-format* option; you can use one or both.

What Next

Reexecute *extract_model* and specify one or both of *-format db* or *-format lib*.

Feedback

MEXT-11

(error) Invalid operating condition '%s' specified.

Description

You receive this message if the operating condition you specified using *extract_model -operating_conditions* cannot be found in any library. The operating condition must exist in some library that is in the *link_path*.

This error could be caused by a spelling error or typo, or by the appropriate library not being in the *link_path*.

What Next

First, examine the libraries, design files, and library files listed in the *link_path* variable, to ensure that the intended operating condition appears in one of them. (Use the *report_lib* command to list operating conditions defined in a single library.) If so, note the correct spelling. If not, add the appropriate library to the *link_path*. Next, reexecute *extract_model -operating_conditions* using the correct operating condition name.

MEXT-12

(warning) Pin '%s' is an internal start or end point. Ignoring paths to and from this pin.

Description

You receive this message if the *extract_model* command finds a pin that is an external start or end point, indicating that the pin is participating in a timing exception or has an input delay specified on it. Because of an extracted model (ETM) limitation, *extract_model* does not support such qualifiers.

What Next

Remove all *max_delay*, *min_delay*, and external delays from the pin. Then reexecute *extract_model*.

MEXT-16

(warning) No master clock exists for generated clock '%s'.

Description

You receive this message because the *extract_model* command found a generated clock without a master clock defined.

Feedback

What Next

If it is acceptable to you for *extract_model* to ignore paths to and from the named generated clock, no action is required on your part. Otherwise, use the *report_clock* command to see the source pin that needs a clock defined on it.

MEXT-17

(warning) Zero (or negative) max capacitance on library pin. Assuming %f for library cell %s output %s.

Description

You receive this message if the *extract_model* command finds a 0.0 or negative maximum capacitance specified on a library cell pin. You cannot have a zero or negative maximum capacitive loading for a library output pin. This message warns you that *extract_model* is assuming the specified value for max capacitance instead.

Many ASIC libraries supply a maximum allowable capacitance on gate outputs. If a gate in the design does not have a *max_capacitance* attribute in its library definition, the *extract_model* command uses the value of the PrimeTime *extract_model_capacitance_limit* variable. The default is 64.

What Next

Correct the library to specify a maximum capacitance for all arcs. Or, use the PrimeTime variable *extract_model_capacitance_limit* to set a maximum allowable capacitance for all gate outputs in the design. Then reexecute *extract_model*.

MEXT-18

(information) extract_model is executed when %s.

Description

This message is issued to indicate that *extract_model* command is executed to generated a black-box ETM from HyperScale flow, please double check whether all the settings are properly configured.

What Next

Please review the settings and flow configuration, either correct the setting or avoid generating ETM's from this run.

MEXT-19

(information) Clock '%s' has multiple sources.

Feedback

Description

You receive this message to inform you that the specified clock has multiple sources, potentially causing longer runtime and higher memory use than a clock with a single source. Timing arcs are extracted from all clock sources, so a larger model will result because of an increase in the number of timing arcs.

What Next

Consider redeclaring your clocks with a single source pin per clock. For information about the implications of delaring clocks with multiple sources, see the user guide.

MEXT-20

(warning) Clock '%s'has source on hierachical pin '%s'. Consider moving to: %s

Description

The specified clock has a source on the specified hierarchical pin. This message warns you that PrimeTime might not be able to extract a propagated delay for this clock.

What Next

If it is acceptable to you for PrimeTime not to extract a propagated delay for the clock, no action is required on your part. Otherwise, to avoid ambiguity of design intent, move the clock source back to an output pin of the physical driver circuit, then reexecute *extract_model*. The list of possible driver pins to use are those that drive the net containing the hierarchical pin.

MEXT-21

(error) Cannot compute generated clock propagated delay. Cannot compute delay from pin '%s' to hierarchical pin '%s'.

Description

You receive this message if a clock pin has a source specified on a hierarchical pin of a net containing RC data. The model extractor cannot compute the propagated delay to this logical node on the net. This message is related to the MEXT-20 warning message.

What Next

Move clock sources back to output pins of the physical clock divider circuit to avoid delays to non-physical pins, then reexecute *extract_model*. Warning MEXT-20 might have been issued previously with a list of driver pins on the net with the hierarchical pin.

Feedback

MEXT-22

(warning) A path from generated clock '%s' back to its master clock is ignored because its length exceeded %d arcs.

Description

A path from the specified generated clock back to the master clock was found to exceed the specified number of arcs. This message warns you that the path(s) is being ignored. The propagated delay to the generated clock will include only the paths shorter than this length. Thus, the propagated delay might not represent the correct min or max path value.

What Next

If it is acceptable to you for the path(s) to be ignored, no action is required on your part. Otherwise, check the design topology for excessively long (false) paths from a master clock to a generated clock, and make changes if necessary. Then reexecute *extract_model*.

MEXT-23

(warning) No net is connected to generated clock '%s' %s pin '%s'.

Description

The specified generated clock has no net connected to either the master clock pin or a clock source pin, as the message indicates. Generated clocks must have net connections even if the clocks are not set to be propagated.

What Next

Review the circuit to ensure that all clock specification points are properly connected within the design. Make necessary corrections, then reexecute *extract_model*.

MEXT-24

(error) Internal error found while creating a generated clock.

Description

You receive this message if an internal error is detected during the creation of a generated clock.

What Next

Execute the *report_clocks* command on both the original netlist and the extracted model. Verify that the period and edges of the generated clocks in the model match those in the original netlist.

Feedback

MEXT-28

(warning) More than %d boundary nets have detailed parasitics and multiple drivers or load pins.

Description

This message is issued to limit the number of MEXT-27 messages you receive, and warns you of the total number of boundary nets that have detailed parasitics and multiple drivers or load pins.

Model extraction sometimes combines the RC characteristics of one fanout or fanin with the constraint characteristics of another. This can lead to an inaccurate model.

What Next

If possible, buffer the net, then reexecute *extract_model*. Always verify the model if you receive this warning.

MEXT-29

(error) ETM Limitation - Arcs between operating conditions do not match. No model will be written. The first mismatch is from '%s' to '%s'.

Description

You receive this message if *extract_model* cannot write a model because the arcs between the various operating conditions do not match. For correct DB format, arcs between the different operating conditions of the same model must match exactly.

This error could be caused by a difference in naming of internal nodes, or by the merging of arcs being different between operating conditions.

What Next

Write the models for each condition to separate files, or use an interface logic model (ILM) instead of an extracted model (ETM).

MEXT-30

(warning) ETM Limitation - Option '-operating_conditions' is not recommended. The extracted models may not be able to be combined into one db file.

Description

You receive this message if you issue the *extract_model* command with the *-operating_conditions* option. Using this option is not recommended, because there might be a mismatch between extracted arcs for various operating conditions of the same model.

Feedback

DB format requires that the arcs match exactly between the different operating conditions of the same model. If the arcs do not match, an error message is generated and the model is not written.

Mismatch errors could be caused by a difference in naming of internal nodes, or by the merging of arcs differing between operating conditions.

What Next

Write the models for each condition to separate files or use an interface logic model (ILM) instead of an extracted model (ETM).

MEXT-35

(warning) ETM Limitation - -remove_internal_arcs option is not recommended.

Description

You receive this message if you issued the *extract_model* command with the *-remove_internal_arcs* option. This option removes all internal pins from the extracted model without moving the constraints or generated clocks to external pins, and its use is not currently recommended.

What Next

Reexecute *extract_model* without the *-remove_internal_arcs* option.

MEXT-36

(warning) A core-cell stamp model will be written. The stamp model must be used with a wrapper design.

Description

The stamp model written without using the *-library_cell* option models only the core of the design being extracted. Boundary nets are modeled in a separate wrapper model. This default behavior was different in previous releases.

What Next

If you want a stamp model that includes the boundary nets, rerun the *extract_model* with the *-library_cell* option.

See Also

- extract_model

Feedback

MEXT-37

(error) extract_model -parasitic_format option has unknown format '%s'.

Description

The valid formats for the *-parasitic_format* option of the *extract_model* command are *spef*, *dspf*, and *binary*. Any other option is invalid.

What Next

Use only the *spef*, *dspf*, and *binary* formats.

See Also

- extract_model

MEXT-38

(error) -parasitic_format cannot be used with the -library_cell option.

Description

The *-parasitic_format* option controls the format for boundary net parasitics. When you use the *-library-cell* option, the boundary nets are included in the model and no parasitics can be written for them.

What Next

Remove either the *-parasitic_format* option or the *-library-cell* option, and execute the *extract_model* command again.

See Also

- extract_model

MEXT-40

(warning) ETM Limitation - the -latch_level option is recommended only when you know the latch-borrowing behavior at the interface. Use -context_borrow instead.

Description

You receive this message if you execute *extract_model* and use the *-latch_level* option. This option is provided for backward compatibility and is not recommended for general use.

Feedback

What Next

Reexecute the *extract_model* command and use the *-context_borrow* option instead of *-latch_level*.

MEXT-43

(information) When tracing paths from %s '%s', borrowing level-sensitive latches ('%s') were traversed through.

Description

You receive this message to inform you that the tracing for model extraction started from the indicated port/clock has gone through some borrowing level-sensitive latches.

What Next

If you observe timing discrepancies, this message might be helpful in debugging.

MEXT-44

(information) Sequential arc '%s' is added only as an '%s' transition. Transition ('%s') is being copied from the existing transition.

Description

You receive this message to inform you that in the process of extracting the named sequential arc, either the rising output or falling output is not a valid path. PrimeTime does not support this type of arc. The invalid transition is being added to the model by giving it the same values as the valid transition.

What Next

You can set false paths when using this model to avoid using the invalid transition.

MEXT-45

(warning) ETM Limitation - hold value for -arc_types specified without specifying setup value. Clock gating hold arcs will not be extracted.

Description

You receive this message because you specified *hold*, but not *setup*, among your values for the *-arc_types* option of the *extract_model* command. Clock gating hold arcs will not be extracted without relevant setup arcs. As a result, your model will not include clock gating hold arcs. All other hold arcs will be extracted.

What Next

If you want clock gating hold arcs, reissue the *extract_model* command with the *-arc_types* option specifying both setup and hold values.

See Also

- extract_model

MEXT-46

(warning) The requested number of delay table points %d does not fit into the %3.4f to %3.4f index range that is set on, or derived for, %s %s.

Description

You receive this message because the requested number of delay table points is so big or the min/max bounds for the table index are so tight that the delay table points cannot be reasonably divided into the requested number of pieces. For SI analysis, the transition set on block input ports is used as the maximum transition table point; if the input transition is zero, then this message will result. When this message is issued, extact_model will automatically adjust the max bound so that the requested number of delay table points can fit into the index range.

What Next

Adjust the settings of the PrimeTime environment variables before executing model extraction. For SI analysis, check the transition value on input ports and increase it to the expected maximum value.

MEXT-47

(error) You must adjust the value of the environment variable '%s' or '%s' before model extraction can proceed. The range is too tight to fit in the requested number of table points.

Description

You receive this message because the requested number of delay table points is so big or the max bound for the table index is so small that it cannot be reasonably divided into the requested number of pieces.

What Next

Adjust the settings of these PrimeTime environment variables before executing model extraction.

Feedback

MEXT-48

(error) You must adjust the value of the environment variable '%s' or '%s' before model extraction can proceed. The product of these two variables %d indicates that the requested size of delay tables is bigger than 100.

Description

You receive this message because the requested number of delay table points is too big. The size of delay tables in the extracted model is limited to less than 100 (for example, less than a 10 by 10 table).

What Next

Adjust the settings of these PrimeTime environment variables before executing model extraction.

MEXT-49

(warning) The model extraction environment variable %s is obsolete and has no effect on model extraction.

Description

You received this message because you have set the indicated model extraction environment variable to some value before you execute the model extraction.

If the vairable warned is 'extract_model_transition_limit', start from the PrimeTime 2002.03 release, this variable is obsolete and replaced by two new variables "extract_model_data_transition_limit" and "extract_model_clock_transition_limit".

If the variable warned is 'extract_model_core_cell_stamp', start from PrimeTime 2001.08 release, the behavior has changed and the models will always be the same regardless of output format. The model is totally controlled by the "-library_cell" option of command *extract_model*.

If the variable warned is 'extract_model_min_delay_threshold', start from PrimeTime 2001.08 release, the variable has been obsolete and all minimum delay and hold timing arcs are extracted.

What Next

Please remove the settings of the old variable and use the new variables to set up the environment for model extraction if applicable.

Feedback

MEXT-50

(error) ETM Limitation - The design has multiple clocks on the same source. Clock '%s' defines multiple clocks on source %s.

Description

Because you defined multiple clocks on the same source, extraction cannot be performed on the design.

What Next

Eliminate the definition of multiple clocks on a single source. To do this, remove all but one clock on the clock source.

See Also

- remove_clock

MEXT-51

(error) ETM Limitation - Path borrowing is not supported for short paths during extraction.

Description

You received this message because you set "timing_allow_short_path_borrowing" variable to TRUE. Path borrowing is not supported for min paths during extraction.

What Next

Set the variable "timing_allow_short_path_borrowing" to FALSE.

MEXT-53

(warning) The model generated is a context-dependent w.r.t clock frequency on certain clocks. This is done because certain constraints had to be moved to the closing edge of latch. Example: %s.

Description

You receive this message because the model extraction process found that the design has a specific set of non-borrowing latch arrangements where it was necessary to move the constraint from the opening to the closing edge. Hence, the model arc embodies a half-a-clock-cycle and, so, is not a context-independent w.r.t clock frequency.

Feedback

What Next

If you observe timing discrepancies at a different clock frequency, this message might be helpful in debugging.

MEXT-54

(warning) The model generated is a context-dependent w.r.t clock frequency on certain clocks. This is done because some of the MCP exceptions could not be moved to the boundary. Example: %s.

Description

You receive this message because the model extraction process found that the design has a specific set of multi-cycle path exceptions where it was not possible to move the MCP out to boundary. Hence, the model arc embodies the MCP shift and, so, is not a context-independent w.r.t clock frequency.

This means that the ETM arc has had the current clock period subtracted from the arcs effected by this MCP. When validating the module, use the default slack mode. The option -timing_type arc should not be used for write_interface_timing.

What Next

Use write_interface_timing -timing_type slack to validate the model. Do not use write_interface_timing -timing_type arc, or the model arc will differ from the netlist arc, my the MCP adjustment value.

If you observe timing discrepancies at a different clock frequency, create a new ETM for the new clock frequency.

MEXT-55

(warning) The -ignore_ports is obsolete.

Description

You receive this message because you have used the -ignore_ports option. This option will reduce the amount of the design that arcs are extracted for, but may in some cases extract some arcs for the ignored ports.

What Next

Use the report_etm_arc command to debug the model.

Feedback

MEXT-56

(Warning) Model cannot create a valid noise table for pin %s.

Description

You received this message because the noise immunity table for one or more noise regions of this pin cannot be created. This can occur either because there's no noise immunity table defined for the given region or because the effective capacitance loading of the first level cell(s) or the noise width points is far outside the bounds of its library cell characterization. Only one message is output per *extract_model* command, so other pins may also be missing one or more noise immunity tables in the model.

What Next

If there's no noise immunity table defined for the given noise region, then use *set_noise_immunity_curve* or *set_noise_margin* for that region.

If there is a noise immunity table for the given noise region, there are several options:

1. If possible, re-characterize the library to expand the width and capacitance range of the pertinent library cell to include the width/capacitance value used in this design. 2. Use *set_load* to override the load capacitance of the library cell(s) affecting the pin of interest. 3. Set the variable *extract_model_noise_width_points* to the same set of widths used for the *noise_immunity_table* of interest. 4. Use *set_noise_immunity_curve* or *set_noise_margin* for the given pin for the problematic region(s).

MEXT-57

(error) The -operating_conditions option can not be used with min_library.

Description

You receive this message because you have used the -operating_conditions option while the -min_library option was used for the set_operating_condition command. The -operating_conditions option to extract_model is obsolete and does not work correctly when the -min_library option to set_operating_condition is used.

What Next

Either produce one ETM for bc_wc or on_chip_variation mode, or create one ETM for each desired operating condition by using the set_operating_condition command followed by extract_model.

MEXT-58

(warning) The -operating_conditions option is obsolete.

Feedback

Description

You receive this message because you have used the -operating_conditions option. This option is being phased out because it can not support all the functionality of set_operating_condition. Today, it will produce a model for each of the operating conditions listed in single analysis mode. It can not support min_library or multi-voltage options.

What Next

Convert your script to call extract_model once for each desired operating condition. Use set_operating_condition and related commands to set the operating conditions between each call to extract_model.

MEXT-59

(warning) The -update option is obsolete.

Description

You receive this message because you have used the -update option. This option is being phased out because support for the scaled cell model it produces is being phased out.

What Next

Create separate models for each operating condition.

MEXT-61

(warning) Model does not support noise steady state current tables.

Description

You received this message because some cell(s) in the design that reach an output port contain steady state current tables for noise analysis. This feature is not supported yet. Steady-state resistance will be used if it's available either in the cell library or added via user-defined commands.

What Next

Either re-characterize the affected cell libraries with steady state resistance or set steady-state resistance via noise commands on the output pins of interest.

MEXT-62

(warning) Model cannot create a valid noise I-V curve for pin %s.

Feedback

Description

You received this message because the steady-state current table (i.e., I-V curve) for one or more noise regions of this pin cannot be created. This may occur because the voltage bounds or number of points need to be adjusted. Only one message is output per extract_model command, so other pins may also be missing one or more noise steady-state current tables in the model.

What Next

Use the extract_model variables for noise I-V tables to adjust the number of points or the range of voltages.

MEXT-63

(warning) No input noise defined on port %s.

Description

You received this message because there was no positive input noise defined on the specified input port. It is assumed that all input ports are set to their worst-case input noise level in order to ensure a conservative noise model. Only one message is output per extract_model command, so other input ports may also have no input noise defined.

What Next

Use set_input_noise to define an input noise for the specified port.

MEXT-64

(warning) Conflicting clock sense at model pin: %s

Description

You received this message because a pulse clock sense propagates the model pin in the message, but there is a conflicting clock sense that also propagates to this pin. No pulse_clock attribute was added to the model at this pin.

What Next

In using the model add generated clocks to model the different pulse clock generators internal to this model.

MEXT-65

(information) Found logic constant value '%s' at output boundary pin/port '%s' due to propagation of case analysis value.

Feedback

Description

You receive this message to inform you that model extractor detected the specified logic constant has propagated to the output boundary of the block due to certain case analysis settings for the block.

What Next

Some tools treat logic constant values differently depending on the values are caused by user set case analysis or intrinsic functional constant of the circuit. By default, ETM writes out .lib and .db files the resulting logic constants from both cases as 'function' attributes for relevant pins. If this behavior is not desired, you can optionally use variable *extract_model_write_case_values_to_constraint_file* to write the user case analysis caused constant values to the ETM constraint files. Note logic value due to functional constant propagation is always written in the .lib and .db ETM files as "function" attribute for pin.

MEXT-66

(error) -validate is used in an old version of modeling.

Description

You receive this message to inform you -validate option is used in an old version of modeling. The version of modeling is specified by variable *hier_modeling_version*. If it is less than 2.0, -validate option cannot be used.

What Next

Set the variable *hier_modeling_version* to 2.0 to allow the automatic model validation.

MEXT-67

(warning) There is a min/max delay constraint between port %s and port %s. Ignoring this constraint.

Description

Min/max delay constraint between ports is considered as part of top level constraints, and it is always ignored in *extract_model*.

What Next

Delete this constraint and do extraction again.

Feedback

MEXT-68

(warning) No voltage is found for supply net %s. This supply net is connected to an upf port and the voltage must be set. The pg_pin data is not extracted in the timing model.

Description

You receive this message because pg_pin extraction has been enabled for this *extract_model* command and at least one supply net does not have the voltage set. The model will continue to be extracted without pg_pin information.

What Next

Set voltage(s) using *set_voltage* on all supply nets needed in order to get the pg_pins extracted for this ETM.

MEXT-69

(warning) Signal port %s has %s and %s, both upf ports, as related power (ground) pins. Inconsistent upf data. The pg_pin data is not extracted in the timing model.

Description

You receive this message because pg_pin extraction has been enabled for this *extract_model* command and at least a signal port relates to multiple upf ports. The model will continue to be extracted without pg_pin information.

What Next

Check the upf network.

MEXT-70

(warning) Signal port %s has been assigned %s supply net as related power (ground) pin because no other supply net was found to be related.

Description

You receive this message because pg_pin extraction has been enabled for this *extract_model* command and at least a signal port was found without any related supply nets.

What Next

Check the port connectivity and the upf data.

Feedback

MEXT-71

(warning) Supply net %s has been assigned a voltage value of 0.0 because no voltage was set and it is a primary ground supply net.

Description

You receive this message because pg_pin extraction has been enabled for this *extract_model* command and at least a supply net was not assigned a voltage.

What Next

Check the upf network.

MEXT-72

(warning) Supply net %s has been assigned a voltage value of %g because no voltage was set and it is a primary power supply net. The voltage has been deduced from library data.

Description

You receive this message because pg_pin extraction has been enabled for this *extract_model* command and at least a supply net was not assigned a voltage.

What Next

Check the upf network.

MEXT-73

(warning) Supply net %s has been assigned a pg type because no known type has been assigned.

Description

You receive this message because pg_pin extraction has been enabled for this *extract_model* command and at least a supply net was not assigned a known type (primary_power or primary_ground).

What Next

Check the upf network.

MEXT-74

(error) Supply port %s is also in the signal port list. Supply port will be extracted as a signal port in the ETM.

Feedback

Description

You receive this message because pg_pin extraction has been enabled for this *extract_model* command and at least a supply port is also on the signal port list. The model extraction will not be performed.

What Next

Disabling the pg_pin extraction will allow extraction of the timing model, although without pg_pin information. Removing the upf ports from the list of signal ports will allow extraction of the timing model with pg_pin information.

MEXT-75

(warning) port '%s' is connected with both input and output pins, this may impact the accuracy of arcs associated with it in the extracted model.

Description

You receive this message to warn you that model extractor detected the noted port is connected with both input and output pins. This happens most often for unbuffered output port with net looping back into timing paths and end points internal to the block. When *-libraray_cell* is used, this can result in potential accuracy degradation of the extracted model, because the timing paths looped back into the block are impacted by the port load external to the block; and the net arc delays between the outgoing and loop back branches may be different.

What Next

Please verify the connectivity of the noted port. It is recommended that the port be properly buffered to isolate impact from external loading effects to the internal loop back timing paths.

MEXT-76

(information) Multiple clocks %s are defined on the same source pin %s.

Description

You receive this message because you perform extract_model on a design with multiple clock sources defined.

What Next

Exercise care to make sure that all clocks that were defined on a single source pin are correctly defined when the extracted model is instantiated.

Feedback

MEXT-77

(Error) The clock source latency arc to pin %s cannot be created for generated clock %s.

Description

You receive this message because of unexpanded generated clocks or untraceable source networks (often resulting in error or warning messages during update timing, such as UITE-461, PTE-075, PTE-021, PTE-022, PTE-023, PTE-025, PTE-103). There are multiple reasons :

1. No physical paths exist between a generated clock and its master. 2. Edges or senses are incorrect given the circuit between a generated clock and its master. 3. An ambiguous source network exists between a generated clock and its master. For example, paths forming loops.

It is strongly recommended that the generated clock definitions follow a cascading topology, particularly when the intermediate generated clocks block the original master from directly reaching downstream sources.

What Next

Check for the generated clock definition to see if the generated clock is correctly defined.

MEXT-78

(error) Index values should be positive, monotonically increasing and unique. Specified index value '%g' violates this criteria.

Description

Values specfieid should be monotonically increasing, unique and non-negative.

What Next

Use 'set_extract_model_indexes' to correct the index values specified.

MEXT-79

(warning) Specified index value '%g' for port '%s' violates min/max (%g/%g) '%s' specified in the main library. Defaulting to auto indexing.

Description

Value should be within bounds set for max and min capacitance(or transition).

Feedback

What Next

Use 'set_extract_model_indexes' to correct the index values on the mentioned port or reset all index values using 'reset_extract_model_indexes'.

MEXT-80

(warning) Variable si_filter_keep_all_port_aggressors is set to FALSE

Description

You receive this message because you did not set si_filter_keep_all_port_aggressors to TRUE before update_timing. In order to obtain better port stage modeling, the aggressors to the port net should be all preserved.

What Next

It is recommended to set si_filter_keep_all_port_aggressors to true before update_timing to ensure SI bounding of the generated ETM

See Also

- extract_model

MEXT-81

(warning) The driving cell at port '%s' is insensitive to input slew

Description

You receive this message because the output slew of the driving cell is insensitive to its input slew, or the output slew change is too small for numerical stability. Both delay/constraint and transistion time tables related to this port will be flat.

What Next

Use proper driving cells on the input ports.

See Also

- extract_model

MEXT-82

(warning) Model cannot create a valid CCS noise table for pin %s.

Feedback

Description

You received this message because the library cell voltage corresponding to the pin and the operating voltages do not match. If UPF is enabled, the mismatch is between the related pg_pin and the library cell voltage.

What Next

Use the same operating voltage as the library cell voltage. Use check_timing to find any voltage mismatch.

MEXT-083

(information) Specifying %g %s timing margin

Description

You receive this message to inform you the timing margin set by 'set_extract_model_margin'.

MEXT-83

(error) Margin values should be positive. Specified value '%g' violates this criteria.

Description

Values specfieid should be non-negative.

What Next

Use 'set_extract_model_margin' to correct the value specified.

MEXT-84

(error) Number of index values does not match the set capacitance points/transition points .

Description

Index list should have the same number of points specfiied using set_extract_model_num_capacitance_points/set_extract_model_num_transition_points. For default index count please refer to set_extract_model_num_capacitance_points and set_extract_model_num_transition_points man pages.

What Next

Use 'set_extract_model_num_capacitance_points', 'extract_model_num_data_transition_points',

Feedback

'extract_model_num_clock_transition_points', to correct the index value count and retry set_extract_model_indexes.

MEXT-85

(warning) isolation_enable_condition cannot be accurately modeled for output port '%s'

Description

You receive this message because the isolation enable condition is defined on an output port. isolation_enable_condition cannot be accurately modeled for output pins on macro cells and is being skipped.

What Next

Use proper set_isolation_control options to defined isolation_signal on input ports

See Also

- extract_model

MEXT-86

(error) pin '%s" voltage "%f" is not in range with input voltage range ('%f' , '%f')

Description

You receive this message because the pin voltage is not in range with input voltage range. Input voltage range will be commented out in the lib file.

What Next

check set_voltage for the supply net. Check input voltage range of level shifter connected to the pin.

See Also

- extract_model

MEXT-087

(warning) *extract_model* is not fully supported when *set_advanced_analysis* is executed.

Description

You receive this message to inform you *extract_model* is not fully supported when *set_advanced_analysis* is executed.

Feedback

What Next

Do not use *set_advanced_analysis* before *extract_model*. Alternatively, user can set timing_enable_auto_mux_clock_exclusivity to false and set si_xtalk_delay_analysis_mode to all_paths.

MEXT-88

(information) Case analysis static logic values not captured in extract_model.

Description

You receive this message to inform you that case analysis *static* logic values were not captured in *extract_model* because *extract_model_write_case_values_to_constraint_file* is set to *false*.

What Next

To enable case analysis *static* logic values to be captured, please set *extract_model_write_case_values_to_constraint_file* to *true*.

MEXT-89

(warning) report_etm_arc command is not recommended to use.

Description

You received this message because report_etm_arc command is not recommended to be used. It is only useful for basic debugging of ETM to netlist differences. The features not supported in this command include: SI, PBA, new latch, POCV, AOCV, noise, multi-clocks on ports, CCST, etc.

MEXT-90

(warning) The clock '%s' is skipped in extract_model because its source pin is on the fanout of another source pin of the same clock.

Description

This warning is issued when extract_model is extracting a clock whose source pin is reached from another clock source pin of the same clock. Please make sure that the clock source pins of multi-source clocks are not defined in such manner.

Feedback

See Also

- create_clock
- create_generated_clock

MEXT-91

(warning) Failed to create CCST driver model for pin '%s' because %s

Description

You receive this message because extract_model is unable to generete a CCST driver model for the specified pin due to non-ideal library data.

The corresponding NLDM will still be written.

What Next

Check for RC-xxx messages.

See Also

- extract_model

MEXT-92

(information) No parasitics on net %s, copy CCS noise table from library for port %s.

Description

You receive this message to inform you that the CCS noise table is copied from library because there is no parasitics on the net.

What Next

Use *read_parasitics* to load the parasitics. Use *report_annotated_parasitics* to check the parasitics annotated on the net.

MEXT-93

(information) The maximum number of levels of transparent latches from a port to trace through is limited to 1

Description

You receive this message if you execute *extract_model* and use the *-latch_level* option with a value larger than 1 or use the *-context_borrow* option

Feedback

What Next

If the actual levels of borrowing latches is greater than 1, the ETM will be more pessimistic than the netlist timing

---

MEXT-94

(warning) Found multi-cycle path exception(s) applicable to timing path(s) from pin '%s' to pin '%s'; ignored in arc tables.

Description

You receive this message because extract_model is set to ignore multi-cycle path exceptions.

What Next

Please review the related exceptions, and apply such exceptions to the timing arcs during top level run if necessary.

See Also

- extract_model
- set_multicycle_path

MEXT-95

(warning) Found multi-cycle path exception(s) applicable to timing path(s) from pin '%s' to pin '%s'; applied in arc tables.

Description

You receive this message because extract_model is set to apply multi-cycle path exceptions.

See Also

- extract_model
- set_multicycle_path

MEXT-096

(information) Elapsed time for %s: %u seconds

Feedback

Description

You receive this message to inform you the elapsed time during extract_model.

MEXT-96

(information) Start extracting arcs for port '%s' %s ...

Description

You receive this message to inform you the port is extracing in extract_model.

MEXT-97

(warning) port '%s' and '%s' are connected to the same net (shorted).

Description

You receive this warning message to because timing model extraction detected the 2 noted logical ports are connected on the same net, meaning they are electrically shorted. This may impact the accuracy when they are convered into relevant timing arcs in the resulting model.

What Next

Please verify the connectivity of the noted ports. It is recommended that the port be properly buffered for better black box modeling.

MEXT-98

(warning) HyperScale hierarchical flow is enabled or HyperScale context is loaded.

Description

You receive this message because HyperScale analysis flow is enabled or HyperScale context is loaded. This is not the recommended flow for model extraction.

What Next

Disable HyperScale.

See Also

- extract_model

Feedback

MEXT-100

(Information) Input signal level for port %s is extraction as it is connected to pin %s.

Description

In ETM input_signal_level attribute is extracted for a port if it is connected to a pin which has input_signal_level. This message indicates the source of input_signal_level for the port.

See Also

- extract_model

MEXT-101

(warning) Variable "extract_model_ccs_keep_voltage_corner" has been set as %s, but %s is not given in command set_voltage for pg_pin %s.

Description

You receive this message because the min/nominal voltage is not given, while the variable *extract_model_ccs_keep_voltage_corner* has been set as min/nominal.

What Next

Check the variable setting or adjust the set_voltage command.

MEXT-102

(error) min voltage and/or max voltage are not within 5 percent of the nominal voltage for pg_pin %s.

Description

You receive this message because the variable *extract_model_ccs_keep_voltage_corner* has been set as nominal, but the min voltage and/or max voltage are not within 5 percent of nominal voltage.

What Next

Change the variable setting or adjust the set_voltage command.

MEXT-103

(error) trying to set_extract_model_indexes before update_timing.

Feedback

Description

You received this message because you try to use *set_extract_model_indexes* command before *update_timing*.

What Next

Change your command order so that when using set_extract_model_indexes, the design is up to date.

MEXT-104

(error) Found min_capacitance %6.4f larger than max_capacitance %6.4f for library pin %s; assigning min_capacitance to %6.4f.

Description

You received this message because the *min_capacitance* requirement was larger than the *max_capacitance* requirement for the indicated library pin. To resolve it, the *min_capacitance* requirement was adjusted.

MEXT-105

(information) For model extraction, min_period and min_pulse_width arcs are extracted at the context slew.

Description

You receive this message as a reminder that during model extraction, clock minimum period and minimum pulse width arcs are extracted at the context slew (the slew value of the current analysis).

MEXT-106

(information) Wrote user-defined %s in %s.

Description

This messages indicates that user-defined noise information has been written to the extracted ETM:

- Steady-state resistance
- DC margin
- Noise immunity curve

Feedback

MEXT-107

(warning) The final signal voltage of the %s is %g and it does not reach beyond the 2nd slew threshold voltage, which is %g for the %s.

Description

For each *output_current_rise* or *output_current_fall* vector, the final signal voltage must reach the maximum of the slew thresholds for the *output_current_rise* vectors, and the minimum of the slew thresholds for the *output_current_fall* vectors).

If *output_signal_level_low* and *output_signal_level_high* are defined,

```
volt_low = output_signal_level_low;
volt_high = output_signal_level_high;
```

otherwise

```
volt_low = VSS;
volt_high = VDD;
```

For an *output_current_rise* vector,

```
Vfinal = volt_low
         + (0.5/Cout)*(I[2]+I[1])*(T[2]-T[1])
         + (0.5/Cout)*(I[3]+I[2])*(T[3]-T[2])
         + ...
         + (0.5/Cout)*(I[n]+I[n-1])*(T[n]-T[n-1])
Verr = volt_low
       + MAX(slew_lower_threshold_pct_rise,
             slew_upper_threshold_pct_rise,
             output_threshold_pct_rise) * (volt_high-volt_low) * 0.01
```

Vfinal must NOT be less than Verr, or this message is issued.

For an *output_current_fall* vector,

```
Vfinal = volt_high
         + (0.5/Cout)*(I[2]+I[1])*(T[2]-T[1])
         + (0.5/Cout)*(I[3]+I[2])*(T[3]-T[2])
         + ...
         + (0.5/Cout)*(I[n]+I[n-1])*(T[n]-T[n-1])
Verr = volt_low
       + MIN(slew_lower_threshold_pct_fall,
             slew_upper_threshold_pct_fall,
             output_threshold_pct_fall) * (volt_high-volt_low) * 0.01
```

Vfinal must NOT be greater than Verr, or this message is issued.

Feedback

What Next

Check the logic associated with the extracted arc to see if it has voltage characteristics that match the input or output port associated with it.

MEXT-108

(warning) The CCSN %s vector is out of the range of the corresponding model pin %s related power voltage.

Description

The CCSN *output_voltage_rise* or *output_voltage_fall* vector is out of the range of the corresponding model pin's related power voltage. In other words, the voltage swing exceeded the range that was expected.

What Next

Check the logic associated with the extracted arc to see if it has voltage characteristics that match the input or output port associated with it.

MEXT-109

(information) extract_model will use transition drc or limit from user setting.

Description

You received this message because you executed the *extract_model* and cannot use pin slew to bound input transitions.

MEXT-110

(information) No parasitics on port %s.

Description

You receive this message to inform you that there is no parasitics on the port net.

What Next

Use *read_parasitics* to load the parasitics. Use *report_annotated_parasitics* to check the parasitics annotated on the port net.

MEXT-111

(warning) CCS %s model extraction failed on port %s%s.

Feedback

Description

You receive this message because the extraction of the CCS model failed.

What Next

Please check and resolve any calculation warning and/or error message(s) during *update_timing* related to this port.

MIS

MIS-001

(information) Advanced MIS analysis mode is enabled.

Description

You have received this message because you have enabled the advanced MIS analysis mode.

What Next

This is an informational message only. No action is required on your part.

MIS-002

(error) Advanced MIS analysis mode is not enabled.

Description

This feature requires that the advanced MIS analysis mode be enabled.

What Next

Enable the advanced MIS analysis mode.

MIS-003

(warning) Advanced waveform propagation is not enabled; skipping advanced MIS analysis.

Description

Advanced MIS analysis uses waveforms to characterize the multi-input switching speedup of a cell. Usage of this feature requires that the advanced waveform propagation mode be enabled.

Feedback

What Next

Enable the advanced waveform propagation mode using variable *delay_calc_waveform_analysis_mode*.

MIS-004

(information) Advanced MIS models created for %d library cells.

Description

Advanced MIS models are created internally by PrimeTime for performing advanced MIS analysis. This message indicates that advanced MIS models are successfully derived for the specified number of library cells.

What Next

This is an informational message only. No action is required on your part.

MIS-005

(warning) Advanced MIS modeling failed for %d library cells.

Description

Advanced MIS models are created internally by PrimeTime for performing advanced MIS analysis. This message indicates that the advanced MIS model creation failed for the specified number of library cells.

What Next

Look for other warning messages with the details on the library cells for which the derivation failed and take any necessary action.

MIS-006

(warning) Advanced MIS analysis failed for '%s'.

Description

Advanced MIS analysis could not be performed for the specified cell. This can happen if there are issues with the delay models of the underlying library cells.

What Next

Check for any previous errors or warnings related to this cell or library cell. If this warning is expected, exclude the library cell from advanced MIS analysis and/or set a conservative MIS coefficient on this library cell as a fall back.

Feedback

MIS-007

(warning) Could not derive advanced MIS models for '%s'; excluding library cell from advanced MIS analysis.

Description

Derivation of advanced multi-input switching (MIS) models failed for the specified library cell. As a result, this library cell cannot be used for advanced MIS analysis.

This message is always followed by other MIS-* messages (MIS-008, MIS-013) indicating the specific reason(s) for modeling failure.

What Next

If this is an expected result for this library cell, no action is needed. If not, check for any inconsistencies in the library data (such as missing *when* conditions, missing library models, unexpected arc senses) and fix them.

MIS-008

(warning) No associated arc found for MIS pin '%s' (when: %s); ignoring pin for advanced MIS modeling.

Description

The specified library pin cannot be part of any advanced MIS model because no associated arc is found for the pin.

What Next

Check if all the when conditions are enumerated and fix the library, if necessary.

MIS-009

(warning) For '%s' (%s), %d timing arc(s) have no 'when' conditions; excluding library cell from advanced MIS analysis.

Description

Some of the timing arcs of the specified library cell have no when conditions that are required for creation of advanced MIS models.

What Next

Check the library cell and update its when conditions for it to be considered for advanced MIS analysis.

Feedback

MIS-010

(warning) Failed to use advanced MIS model for '%s' (%s) in delay calculation.

Description

Some inconsistencies were found with the delay models of the specified library cell and it cannot be used for advanced MIS analysis.

What Next

Check the delay models of this library cell for any issues. If the library is expected to be part of a scaled library group, check if the definition of the library group was successful. If this warning is expected, exclude the library cell from advanced MIS analysis and/or set a conservative MIS coefficient on this library cell as a fall back.

MIS-011

(warning) For '%s', no arc-based CCSN models found; excluding library cell from advanced MIS analysis.

Description

The specified library cell does not have any arc based CCSN models. These are required for performing advanced MIS analysis.

What Next

Provide arc based CCSN models for the library cell for it to be considered for advanced MIS analysis.

MIS-012

(warning) Could not calculate advanced MIS delta for '%s' -> '%s' arc of cell '%s'; excluding arc from advanced MIS analysis.

Description

Simulation to calculate the advanced MIS delay on the specified arc failed. This could have been the result of any previous warnings or errors related to the library or library cell. It is also possible that the input slew is very large that the output waveform did not cross 50% VDD point for delay computation.

What Next

Check for any previous errors or warnings related to this arc, cell or library cell. Ensure that there are no large NLDM vs. CCSN characterization errors for this library cell. If this

warning is expected, exclude the library cell from advanced MIS analysis and/or set a conservative MIS coefficient on this library cell as a fall back.

MIS-013

(information) For arc '%s' of '%s', the arc sense cannot cause the required input '%s' and output '%s' transitions; excluding this arc from advanced MIS analysis.

Description

You receive this message if a library cell's logical function would normally support advanced multi-input switching (MIS) analysis, but the arc sense of the indicated arc cannot cause the required input and output transitions needed to exhibit a multi-input switching (MIS) speedup effect.

For example, consider a specially-designed cell with an OR logical function. Normally, an OR gate would have positive-unate arcs that provide both rise-to-rise and fall-to-fall transitions from input to output. However, if a specially-designed cell (that happens to have an OR function) has fall-to-fall arcs instead of positive-unate arcs, then simultaneous rise-to-rise transitions across the inputs cannot occur.

What Next

If the indicated cell is specially-designed and is intended to lack the required arc senses, then this message is expected.

If the indicated cell is expected to be a regular library cell for its logical function type, then this message is not expected and the indicated arc should be checked for correctness.

MIS-014

(information) MIS analysis will use the following order of precedence: %s.

Description

You have received this message because you have set multi-input switching analysis modes and their precedence.

What Next

This is an informational message only. No action is required on your part.

MIS-015

(warning) For '%s' (%s), when condition for arc %s refers to pin (%s) that is not part of the output function; excluding library cell from advanced MIS analysis.

Feedback

Description

When condition for a timing arc is expected to refer only to the input pins of the corresponding output function. If this condition is not met, the corresponding library cell cannot be considered for advanced MIS.

This scenario is generally seen on multi-bit combo cells. For example, for a multi-bit combo cell with an AOI gate and an inverter, if any arcs of the AOI gate have when conditions referring to the input pin of the inverter, this warning is thrown.

What Next

Update the arcs and when conditions of the library cell for it to be considered for advanced MIS analysis.

MIS-016

(warning) Value '%s' for option '%s' not in range (%s). The library cell user-defined coefficient is changed to 0.

Description

The lib_cell analysis mode allows you to define delay-scaling coefficients on library cells. These coefficients must be defined in the range of 0 to 1.

What Next

Set the library cell user-defined coefficient in the range of 0 to 1.

See Also

- si_enable_multi_input_switching_analysis
- si_multi_input_switching_analysis_mode
- set_multi_input_switching_coefficient

MIS-017

(warning) Invalid pin number %s for pin set "%s". The pin set will use default pin set (all input pins).

Description

The lib_arc analysis mode allows you to define delay-scaling coefficients on individual library cell timing arcs. These coefficients can be provided in a library or applied by a script file and the pin sets should be provided with the correct syntax.

Some examples of the correct syntax for the pin set are shown below.

Feedback

```
mis_pin_set_rise : "A1 B1 B2";
mis_pin_set_rise : "A1 A2 + A1 B1 B2";
mis_pin_set_rise : "A1 A2+A1 B1 B2";
```

What Next

Define the pin sets with the correct syntax.

See Also

- si_enable_multi_input_switching_analysis
- si_multi_input_switching_analysis_mode

MIS-018

(Information) Enabled %s tied-input filter for MIS analysis; The MIS analysis is performed only for gates with %s.

Description

You have received this message because you have set multi-input switching tied input filter variable.

What Next

This is an informational message only. No action is required on your part.

See Also

- si_enable_multi_input_switching_analysis
- si_multi_input_switching_analysis_mode
- si_multi_input_switching_tied_input_filter

MKW

MKW-001

(error) Could not open Milkyway library %s.

Description

The specified Milkyway library could not be opened.

Feedback

What Next

Check the location of Milkyway library and reissue the command.

MKW-002

(error) Could not open Milkyway CEL view file %s.

Description

The specified Milkyway library could be opened but the given CEL view file could not be opened.

What Next

Check the name of the file name and reissue the command.

MKW-003

(error) Could not get the top level cell instance from the Milkyway CEL.

Description

Something is wrong in the Milkyway CEL database. The command will be aborted.

What Next

Check the name of the Milkyway library and the name of CEL file and reissue the command.

MKW-004

(warning) Could not resolve library cell '%s'. Any non-physical instances will be black boxes.

Description

A library cell exists in the Milkyway database that could not be located in the logical technology libraries. All the non-physical instances of this library cell will be created as black boxes.

What Next

Check link_path, search_path variables and the name of Milkyway library and the name of CEL file and reissue the command.

Feedback

MKW-005

(warning) Resolved library cell '%s' has greater number of pins in logical library.

Description

A library cell exists in the Milkyway database that was resolved successfully to a library cell in logical library. Usually, it happens that the number of pins in Milkyway database are greater than the number of pins in logical library due to the presence of physical pins. However in this particular case, the library cell in the logical library has more number of pins than the library cell in Milkyway database.

What Next

No action required but please check the link_path and search_path variables.

MKW-006

(information) Creating black box for cell '%s'.

Description

The library cell corresponding to the given cell could not be resolved and hence a black box is being created.

What Next

No action required but please check the link_path and search_path variables.

MKW-007

(warning) Found a hierarchical library cell pin %s with invalid direction for library cell %s.

Description

The MW database has an invalid direction for the given library cell pin.

What Next

No action required but please check the validity of MW CEL view.

MKW-008

(warning) Found a design port %s with invalid direction.

Description

The MW database has an invalid direction for the given port.

Feedback

What Next

No action required but please check the validity of MW CEL view.

MKW-009

(warning) link_create_black_boxes is not supported in the Milkyway flow.

Description

You are getting this message since you disabled the creation of black boxes and are using "read_milkyway" command. The Milkyway database is a physically linked database. When it is read into PT/PTSI, a linked database is read in. For this reason, a linking step does not occur in the "read_milkyway" flow. Any unresolved library cells will be created as black boxes.

What Next

No action required.

MKW-010

(error) Scenario name %s supplied when no scenarios stored

Description

A *read_milkyway* command was issued with a scenario name argument, but there were no scenarios stored in the milkyway database.

What Next

Either re-generate the milkyway database with the scenario, re-issue the *read_milkyway* command as *-netlist_only* to ignore all constraints, or re-issue the *read_milkyway* command without the scenario to pick up the non-scenario constraints.

MKW-011

(error) Scenario name %s did not match an available scenario %s.

Description

A *read_milkyway* command was issued with a scenario name that did not match any of the scenarios in the milkyway database. A list of available scenarios is listed.

What Next

Choose one of the available scenarios and re-issue the *read_milkyway* command with the chosen scenario.

Feedback

MKW-012

(error) Cannot read all constraints from Milkyway%s.

Description

The *read_milkyway* command could not read all of the constraints from the given Milkyway design.

What Next

Ensure that the constraints were written to the Milkyway database correctly and with the correct scenario name(s) if scenarios are being used.

The most likely cause of this is an incompatible version of IC Compiler or the CEL was generated from Astro. PrimeTime does not support reading constraints written by Astro into a CEL.

If the CEL was generated from Astro, you can write out the SDC for the CEL in Astro and then read the SDC into PrimeTime.

MKW-013

(error) Cannot find bussed port %s.

Description

The Milkyway Database defines a port in the bus section but not in the regular ports section. The bus will not include the given port.

What Next

Check the creation of Milkyway database and re-run.

MKW-014

(error) net %s is declared twice

Description

The net was declared twice in the design. This can happen if two net names are the same except for escape characters.

What Next

Regenerate the design using net names that are unique.

Feedback

MKW-015

(error) Milkyway database is corrupted.

Description

A serious error occured while reading Milkway, the results of read_milkyway will be best effort to be tolerant to the error but check with the writer of the Milkyway.

What Next

Regenerate the MW database.

MMODE

MMODE-001

(error) At least two modes should be provided for merging.

Description

You issued the command to merge individual modes but did not provide enough modes. This means one of the following errors occured:

- No scenarios were created.
- Scenarios were not created with the *-mode* or *-corner* option but were created with the previous *-name* style.
- Scenarios are all created with a single mode.

What Next

Issue all *create_scenario* commands before issuing the mode merging command.

MODEL

MODEL-1

(error) Cannot write the updated model to the db file. The scaled cell model has different ports from the original model saved in the db file %s.

Description

You receive this message if you execute *extract_model* with the *-update* option, and the ports or timing arcs of the updated model are different from those of the original model.

Feedback

Two models written to the same db file must have exactly the same ports and number and order of arcs; the only difference allowed is in the timing values. This message informs you that *extract_model* did not update the db file with the new information.

Some possible reasons why the two models are different could include these:

- You might have used a slightly different version of the design when performing the update.
- The design might have different false path definitions, which could result in different timing arcs.
- You might have inadvertently used a different design when performing the update.
- You might have used different options (for example, *-library_cell* or *-ignore_ports*) for the original and for the updated model.

What Next

Ensure that the original and the updated model have the same timing arcs and ports. Then reexecute *extract_model* with the *-update* option.

See Also

- extract_model

MODEL-2

(error) Port name %s found in %s design is not found in %s design (operating_condition - %s).

Description

You receive this message if *extract_model* detects a port in the nominal model (that is, at nominal operating condition) that is not in the scaled cell (at a different operating condition). The scaled cell must contain the same ports and arcs as the nominal model.

What Next

Ensure that the scaled cell model contains the same ports as the nominal model, then reexecute the command.

See Also

- extract_model

Feedback

MODEL-3

(warning) A scaled cell for operating condition %s already exists. Replacing it with the new cell.

Description

You receive this message if *extract_model* finds that a scaled cell is already present for the specified operating condition. This message warns you that the existing scaled cell is being replaced by the new one.

What Next

This is a warning message only; no action is required on your part. In the future, before executing this command, save a copy of the *_lib.db file so that you can restore any cells that are unintentionally overwritten.

See Also

- extract_model

MODEL-4

(error) Cannot generate a report; cell %s is not an interface timing specification (ITS) cell.

Description

You receive this message if *report_model* finds in the design an instantiated cell that is not an interface timing specification (ITS) cell. *report_model* generates reports only for designs that are composed entirely of ITS cells. You create such designs using *extract_model*.

What Next

Ensure that your design contains only ITS cells. Then reexecute *report_model*.

See Also

- extract_model

MODEL-5

(error) Cannot generate a report; the design %s does not instantiate a PrimeTime model.

Description

You receive this message if *report_model* finds that the design does not instantiate a PrimeTime model. The design might contain more than one cell; a PrimeTime model contains one cell per library. *report_model* generates reports only for PrimeTime designs.

Feedback

What Next

You cannot use *report_model* on this design.

MODEL-6

(Information) Min delay arc from '%s' to '%s' missing for operating_condition '%s'; substituting with a max_delay arc.

Description

The extractor did not extract the min delay arc between the two points for the operating condition. This min delay arc is present in other operating conditions.

What Next

No further action is needed.

MODEL-7

(Error) Cannot open file %s for writing.

Description

You receive this message if the command could not write to the specified file. You might be in a directory where you do not have write permission, or perhaps the file exists and is write-protected.

What Next

Either change the permissions on the file or directory so that you can write to it, or use another file and directory for which you have write permission. Then reexecute the command.

See Also

- extract_model
- save_qtm_model
- write_interface_timing

MODEL-8

(information) STAMP %s file %s was successfully compiled.

Feedback

Description

This is an informational message indicating the STAMP file has been compiled succussfully.

What Next

No action is needed.

MODEL-9

(Error) You must use the -library_cell option with the -remove_internal_arcs option.

Description

You receive this message if you execute *extract_model* with the *-remove_internal_arcs* option and did not also use the *-library_cell* option. You cannot use *-remove_internal_arcs* without also using *-library_cell*.

What Next

Reexecute *extract_model* and use the *-library_cell* option along with the *-remove_internal_arcs* option.

See Also

- extract_model

MODEL-10

(warning) The -test_design option is valid only with the -library_cell option. Ignoring the -test_design option.

Description

You receive this message if you execute *extract_model* and use the *-test_design* option without the *-library_cell* option. The *-test_design* option specifies that a test design instantiating the model lib_cell is to be generated; therefore, *-test_design* is invalid without the *-library_cell* option. This message warns you that the *-test_design* option is being ignored.

What Next

If it is acceptable to you that the *-test_design* option is ignored, no action is required on your part. However, if you still want to use the *-test_design* option, reexecute the *extract_model* command and use both the *library_cell* and *-test_design* options.

Feedback

See Also

- extract_model

MODEL-11

(warning) Cannot update library %s; that library does not exist.

Description

You receive this message if you execute *extract_model* with the *-update* option, but the specified library does not exist. *extract_model* therefore cannot update the library.

What Next

If it is acceptable to you that the specified library was not updated, no action is required on your part. Otherwise, do one of the following:

1. Reexecute *extract_model -update* and specify the name of an existing library that is consistent with the current design; or
2. Reexecute *extract_model* without the *-update* option and write a new library.

See Also

- extract_model

MODEL-12

(information) %s.

Description

This is a general purpose modeling related informational message usually issued to indicate the progress or status of the program.

What Next

No action is needed.

MODEL-13

(warning) Cannot write generated clock %s to the model because all of the clock's derived sources are on internal pins and the *-remove_internal_arcs* option was specified.

Feedback

Description

You receive this message if you execute *extract_model* with the *-remove_internal_arcs* option, but one or more generated clocks have their derived sources on internal pins. This message warns you that if internal arcs are removed, the specified clock cannot be written to the extracted model.

What Next

If it is acceptable to you that the specified generated clock is not written to the extracted model, no action is required on your part. However, if you want the generated clock to be written, reexecute *extract_model* and do not use the *-remove_internal_arcs* option.

See Also

- extract_model

MODEL-14

(warning) Cannot write generated clock %s to the model because the clock's master pin is on an internal pin, and the *-remove_internal_arcs* option was specified.

Description

You receive this message if you execute *extract_model* with the *-remove_internal_arcs* option, but the specified generated clock has its master pin on an internal pin. This message warns you that if internal arcs are removed, the specified clock cannot be written to the extracted model.

What Next

If it is acceptable to you that the specified generated clock is not written to the extracted model, no action is required on your part. However, if you want the generated clock to be written, reexecute *extract_model* and do not use the *-remove_internal_arcs* option.

See Also

- extract_model

MODEL-16

(warning) The models to be merged have different design names %s and %s, respectively, use %s."

Description

This is to warn that the design names defined in the models to be merged are not the same.

Feedback

What Next

Please check if the names are actually correct. This is a warning message, the models will still be merged.

MODEL-17

(Information) extract_model: %-40s

Description

This message shows the progress of the *extract_model* command. The body of each message reflects a specific aspect of the process.

What Next

This is an informational message only; no action is required on your part. However, if you want to suppress the display of these messages, or change the level of messages that are displayed, set the *extract_model_status_level* variable to a different value. Allowed values are none, low, medium, or high.

See Also

- extract_model
- extract_model_status_level

MODEL-19

(error) The %s defined in the models are different.

Description

This is a general error indicating that the named object(s) defined in the models to be merged are not the same. Model merging cannot proceed with the difference.

What Next

Please make sure that the named object(s) are defined the same across all the models to be merged.

MODEL-20

(error) Found %s '%s' in the models defined with different %s, cannot merge them.

Feedback

Description

This is a general error indicating that the named object(s) defined in the models are not the same. Model merging cannot proceed with the difference.

What Next

Please make sure that the named object(s) are defined the same across all the models to be merged.

MODEL-21

(error) %s '%s' is not defined in all models, cannot merge.

Description

This is a general error indicating that the named object is not defined in all the models. Model merging cannot proceed with the difference.

What Next

Please make sure that the named object is defined across all the models to be merged.

MODEL-22

(error) The port/pin number %d is different in the models. They are defined as %s and %s, respectively.

Description

This is an error message indicating that the port/pin defined at the specified position in the models are not the same. Model merging cannot proceed with the difference.

What Next

Please make sure that the order of pins of direction INPUT/OUTPUT/INOUT/TRIOUT are are defined the same across all the models to be merged. INTERNAL pin order is not important.

MODEL-23

(error) Cannot merge %s '%s' with different '%s' %s and %s in the models.

Description

This is an error indicating that the named attribute defined for the named object are not the same. Model merging cannot proceed with this difference.

Feedback

What Next

Please make sure that the named attribute is defined to have the same values across all the models for the named object.

MODEL-24

(warning) Found %s '%s' with different '%s' %s and %s in the models, use %s.

Description

This is a warning indicating that the named attribute defined for the named object are not the same. Model merging will use the value specified.

What Next

Please check if the named attribute should have the same values for the named object.

MODEL-25

(error) The bit number %d in bus %s is different in the models. They are defined as %s and %s, respectively.

Description

This is an error message indicating that the specified bit of the bus in the models are not the same. Model merging cannot proceed with the difference.

What Next

Please make sure that the bits and the order of bits are the same in the bus across all models to be merged.

MODEL-26

(information) Found unique internal pin '%s' in one of the models, copied into the merged model.

Description

This is an informational message.

What Next

No action required.

Feedback

MODEL-27

(error) %s.

Description

This is a general purpose modeling related error message usually issued to indicate the reason why model merging cannot proceed.

What Next

Please invetigate the models to be merged and fix the identified problems and try merge them again.

MODEL-28

(warning) Found %s '%s' with conflict '%s' '%s' and '%s' set in the models, no constant is set for it in the merged model.

Description

This is a warning indicating that the named attribute defined for the named object are not the same. Model merging will use the value specified.

What Next

Please check if the named attribute should have the same values for the named object.

MODEL-29

(Warning) The %s command will be discontinued in future releases. Changes to model validation has made this command unecessary

Description

A command has been rendered unnecessary by changes to model validation commands. The old command is being supported temporarily but will cause syntax errors in future releases

What Next

Use the new functionality instead of the discontinued command.

MODEL-30

(error) Cannot merge models because no model files were specified

Feedback

Description

You receive this message if you execute *merge_models* without specifying model files through either the -model_files or -lib_files option.

What Next

Add model files to the command using either the *-model_files* or *-lib_files* option.

See Also

- merge_models

MODEL-31

(error) Cannot merge models because no data files were specified

Description

You receive this message if you execute *merge_models* without specifying any data files in conjunction with the *-model_files* optoin. The *merge_models* command requires data files when *-model_files* is present.

What Next

Add data files to the command using the *-data_files* option.

See Also

- merge_models

MODEL-32

(error) Cannot merge models because no mode names were specified

Description

You receive this message if you execute *merge_models* without specifying any mode names. The *merge_models* command requires one mode name for each input file.

What Next

Add mode names to the command using the *-mode_names* option.

See Also

- merge_models

Feedback

MODEL-33

(Error) Cannot merge models because the number of model files does not match the number of data files.

Description

The *merge_models* command requires the number of model and data files match. One model and data file combine to define a model in STAMP format, so *merge_models* requires a one for one correspondance.

What Next

Adjust the *-data_files* or *-model_files* as needed so the list lengths match.

See Also

- merge_models

MODEL-34

(Error) Cannot merge models because the number of mode names does not match the number of model files.

Description

The *merge_models* command requires the number of mode names to match the number of model files. The model files are specified with either the *-model_files* or *-lib_files* option. A combination of model file and mode name defines a model to merge, so the number in each list must match.

What Next

Adjust the mode names or the number of models so that the list lengths match.

See Also

- merge_models

MODEL-35

(Error) Cannot merge models because there are duplicate mode names.

Description

The *merge_models* command requires that the mode names be unique. There cannot be any duplicates.

Feedback

What Next

Change the duplicate mode names to be unique.

See Also

- merge_models

MODEL-36

(error) Cannot merge models because of an empty %s list

Description

A list for *merge_models* is empty. All lists must have at least one element in them.

What Next

Add elements to the list, or remove the option for the list from the command line.

See Also

- merge_models

MODEL-37

(error) Cannot use %s in conjunction with %s

Description

You cannot specify both of these options for *merge_models* at the same time.

What Next

Remove one or both of these options from the command.

See Also

- merge_models

MODEL-38

(error) Cannot merge models because there are data files with no model files.

Description

The *merge_models* command cannot have *-data_files* without corresponding *-model_files*.

Feedback

What Next

Either add *-model_files* to merge STAMP files, or remove the *-data_files* to merge LIB files.

See Also

- merge_models

MODEL-39

(error) Library file was not extracted.

Description

When the *merge_models* command read in one of the files in the *-lib_files* list of library files, it did not see at least one required attribute. Each of the library files must be the result of the *extract_models* command.

What Next

Ensure that all of the library files are the output of the *extract_model* command.

See Also

- merge_models
- extract_model

MODEL-40

(error) Library file is invalid for merging.

Description

When the *merge_models* command read in one of the files in the *-lib_files* list of library files, it found that one of the libraries was missing some expected attributes, had inconsistant attributes, or had unexpected attributes. Each of the library files must be the result of the *extract_models* command.

What Next

Ensure that all of the library files are the output of the *extract_model* command.

See Also

- merge_models
- extract_model

Feedback

MODEL-41

(error) The %s and %s arguments are mutually exclusive

Description

The *merge_models* command cannot be invoked with both of the arguments at the same time, only one is allowed.

What Next

Remove one of the arguments and invoke the command again.

MODEL-42

(Warning) The -test_design option is valid only without the -validate option. Ignoring the -test_design option.

Description

You receive this message if you execute *extract_model* and use the *-test_design* option with the *-validate* option. The *-test_design* option specifies that a test design instantiating the model lib_cell is to be generated; the *-validate* option will create the same test design; therefore, *-test_design* has no effect with the *-validate* option. This message warns you that the *-test_design* option is being ignored.

See Also

- extract_model

MODEL-43

(error) %s.

Description

This is a generic error message.

What Next

Please note and confirm the specific reason indicated by the error message, modify your setting(s) accordingly, re-issue the command(s)

MODEL-44

(warning) %s.

Feedback

Description

This is a generic warning message.

What Next

Please note and confirm the specific reason indicated by the error message, modify your setting(s) accordingly, re-issue the command(s).

See Also

- extract_model

MODEL-45

(warning) PG pin data extraction and merging is not supported for DB output format.

Description

The PG pin data contained in the design or the models to be merged will not be saved in the .DB format. Only the .LIB output format supports PG pin data for model extraction or model merging.

What Next

Please use the .LIB output format if you require PG pin data in the extracted and/or merged model.

See Also

- extract_model

MODEL-46

(error) Port/pin number %d with name '%s' does not have a match.

Description

This is an error message indicating that the port/pin defined at the specified position in the models are not the same and we can't find a match by name either. Model merging cannot proceed with the difference.

What Next

Please make sure that the orders and names of the pins are defined the same across all the models to be merged.

Feedback

MODEL-47

(warning) No UPF wrapper will be generated.

Description

You receive this message if you execute *extract_model* with the *-test_design* option and you set *extract_model_include_upf_data* to TRUE, but you don't specify any UPF commands. So UPF wrapper file will not be generated.

What Next

Load your UPF file.

See Also

- extract_model

MODEL-48

(Warning) Found different values defined for attribute slew_threshold_pct, the models to be merged will be scaled

Description

This is a warning indicating that the *slew_threshold_pct* attribute defined for the models to be merged are not the same. The first model listed in *merge_model* command will be the reference model and all the other models to be merged will be scaled to the same *slew_threshold_pct* used in the reference model. *-keep_all_arcs* mode will be used and the resulting models can be very large.

MODEL-49

(Warning) The option "-export" only supports clases "design" and "port".

Description

This is a warning indicating the class of defined user attribute is not supporing for exporting to extract_model design pr library database.

MODEL-50

(error) A valid merge_models command must have one (and only one) option of: %s and %s.

Feedback

Description

The *merge_models* command must have one and only one of the two options.

What Next

Add one of the arguments and invoke the command again.

MODEL-51

(error) Cannot merge_models because format not corrent in option *merge_pg_pin*

Description

You receive this message if you execute *merge_models* with incorrect format in option *merge_pg_pin*. Here is an example: -merge_pg_pin {voltagae_name [voltage_option]}

What Next

Correct merge_pg_pin arguments and invoke the command again.

MODEL-53

(Error) Cannot merge models because the number of list in mode_names does not match the number of group_names.

Description

The *merge_models* command requires the number of list in mode names to match the number of group names. The model files are specified with either the *-model_files* or *-lib_files* option. Each element in group names defines a mode group name, and each list in mode names defines a list of modes belong to one mode group. Therefore, the number of list in mode names must be the same as the number of element of group names.

What Next

Adjust the mode names or the number of group names so that the number of list in mode names and the number of elements in group names match.

See Also

- merge_models

MODEL-54

(Warning) The pg pin %s specified by option -merge_pg_pin is the related pg_pin of pin %s

Feedback

Description

This is a warning indicating that the *pg_pin* specified by -merge_pg_pin option is the related pg_pin of a signal pin.

MODEL-56

(warning) Generated clock '%s' in mode '%s' is renamed to '%s' in order to resolve a conflict.

Description

You receive this message when generated clocks do not match across the modes.

Generated clocks with the same name must match exactly across the modes (period, generated clock type, and so on). In this case, a same-named generated clock did not match across the modes; as a result, the indicated generated clock was renamed to resolve the conflict.

What Next

This is a warning message only; no action is required on your part.

MODEL-57

(warning) Invalid slew_*_threshold_pct_* value found; the transition tables cannot be scaled.

Description

You receive this message because during model merging, an invalid slew threshold percentage value was found in the input ETM models to be merged.

What Next

Check the *slew_*_threshold_pct_** values in the input models for correctness.

MODEL-58

(error) Found duplicated group name '%s' in group name list.

Description

You receive this message because the *merge_models* command detected a duplicate value in the *-group_names* list.

What Next

Ensure that the *-group_names* option contains a list of unique names.

Feedback

See Also

- merge_models

MODEL-62

(Warning) The mds attribute %s has unknown type.

Description

the mds attribute has unknown type, will be skipped.

What Next

No further action is needed.

MS

MS-001

(Information) Switching %s Distributed Multi Scenario Analysis mode.

Description

PrimeTime has been switched into (or out of) the Distributed Multi Scenario Analysis (DMSA) mode.

What Next

This is an informational message. No action is required.

MS-002

(Error) Switching %s DMSA mode failed: %s.

Description

Switching into (or out of) the Distributed Multi Scenario Analysis (DMSA) mode failed due to the reported reason.

What Next

Fix the reason of the failure.

Feedback

MS-003

(Warning) Following scenarios are reset: %s.

Description

Calling *current_session* resets all scenarios to the way they were at the start. After any call to *current_session* all scenarios in focus are rebuild from the scripts or images used to originally define them.

MS-004

(Warning) The current session has been terminated.

Description

The last scenario in the current session has been removed, therefore the current session has been terminated.

MS-005

(Warning) The search_path entry %s could not be resolved.

Description

The manager was unable to find the directory location of an entry in the *search_path*. The erroneous entry will not be sent to the worker.

What Next

Remove or correct the erroneous *search_path* entry.

MS-006

(error) The worker process was unable to resolve the working directory %s.

Description

The working directory is specified during the setup phase of the manager in the Distributed Multi-Scenario Analysis (DMSA). At that stage a check is done to verify that the working directory is accessable and writable by the manager process. This error occurred because the worker process could not resolve the location of the working directory.

What Next

Change the multi_scenario_working_directory variable to point to a location which can be resolved by the worker process.

Feedback

MS-007

(error) The PrimeTime multi-scenario manager process detected worker instances that encountered fatal errors. The manager and all worker processes will now terminate.

Description

While executing commands in multi-scenario analysis one or more PrimeTime worker instances encountered fatal errors requiring them to exit. In this situation the manager cannot proceed accepting user commands. The manager will complete the last command issued and issue the reporting information that has been processed.

What Next

Re-run the current session excluding the scenario in which the problem occurred.

MS-008

(error) '%s' cannot be changed because multi-scenario session is defined.

Description

The variable cannot be changed if the multi-scenario session is defined.

What Next

Set the variable before using the *current_session* command.

See Also

- create_scenario

MS-009

(warning) Failed to exchange timing path data with the manager.

Description

This warning refers to the timing path printed directly after this warning. While exchanging timing path information with the manager process, a pin was found in the path that was not explicitly mentioned in the netlist and hence is unknown to the manager. As a result the timing information in the path will not be included in the merged timing report produced at the manager. Typically these pins are unconnected pins.

What Next

Identify the unconnected pin from the timing report and explicitly mention it in the netlist.

Feedback

MS-010

(Error) The PrimeTime multi-scenario manager exceeded the task processing limit.

Description

This errors occurred because the manager submitted tasks outside the range of tasks that can be processed in a single PrimeTime instance. Currently, the manager process can manage up to 4900 tasks; PrimeTime cannot process tasks beyond this range.

What Next

This is a limitation of the current multi-scenario capability.

MS-011

(error) %s image generation failed.

Description

The multi-scenario image generated failed validation.

What Next

Examine the worker log files for the cause of the failure and correct the problem.

MS-012

(error) Cannot set multi_scenario_working_directory variable after a distributed farm has been launched.

Description

It is forbidden to change the working directory, once the create_distributed_farm command has been successfully issued.

What Next

Change the multi_scenario_working_directory before issuing the create_distributed_farm command

MS-013

(warning) Setting all scenarios in the current session into command focus for the '%s' command.

Feedback

Description

One or more scenarios in the current session was not in command focus. The command requires that all scenarios in the current session be in command focus before the command can be executed. All scenarios in the current session have been put in command focus to allow the command to execute.

What Next

No further action is required.

MS-014

(information) Implicitly specifying the '-base_names' option with the get_alternative_lib_cells command, because the command has been called in a manager context.

Description

This message is issued if you have called the *get_alternative_lib_cells* command in a manager context and have not specified the *-base_names* option. This option must be used in a manager context and thus has been implicitly specified.

What Next

To obtain a collection of valid alternative library cells for a cell in one scenario, call the command in a worker context on that scenario.

To obtain a list of valid alternative library cell base names for a cell in one scenario, call the command in a worker context with the *-base_names* option on that scenario.

To obtain a list of valid alternative library cell base names for a cell common to all scenarios, call the command in a manager context with the *-base_names* option.

See Also

- get_alternative_lib_cells

MS-015

(information) Removing the scenario %s from the session.

Description

The scenario indicated was removed from the current session. See the man page of the *current_session* command for more details on the current session.

Feedback

What Next

This is an information message, there is no need to act on it unless the scenario was not intentionally removed.

MS-016

(error) Errors detected during distributed task processing.

Description

One or more worker processes encountered an error in processing a task that can give rise to incomplete results.

What Next

Examine the errors reported during the manager/worker task processing and correct any problem found. Further information about the error encountered can be found in the multi-scenario merged error log as specified by the multi_scenario_merged_error_log variable if it was set.

MS-017

(error) failed to create current session with '%d' scenarios. Maximum allowable scenarios in a session using common data '%d'. Maximum allowable scenarios in a session not using common data '%d'.

Description

When setting the current session, the number of scenarios being used to create the session is beyond the number supported. When any scenario has common data, the number of scenarios supported is less than when no scenario has any common data. The limits are as specified above.

What Next

Reduce the number of scenarios being used to form a session within the limits specified above.

MS-018

(warning) Removing the following terminate scenarios from the session. %s

Description

When scenarios abnormally terminate, they are removed from any further subsequent analysis in the current session.

Feedback

What Next

If the terminated scenarios are to be re-analyzed, create a new session, including the terminated scenarios, and analyze them as normal.

MS-019

(warning) Removing the current session.

Description

The resource requirements for the existence of a session have been invalidated so the current session was removed.

What Next

See the *current_session* command for the resource requirements needed to create the current session and how to check the availability of those resources.

MS-020

(warning) Removing the following scenarios from the session. %s

Description

The scenarios indicated were removed from the current session because the scenarios providing baseline images for them to use abnormally terminated while producing the images. These scenarios cannot start-up without the baseline images and must be excluded from further analysis.

What Next

If the scenarios are to be re-analyzed, create a new session including the scenarios and analyze them as normal. If the issue continues to arise, remove the scenario that is failing to produce the baseline image from the session and re-analyze as normal.

MS-021

(fatal) Internal system error in scenario '%s'

Description

While executing commands in multi-scenario analysis the scenario indicated experienced a critical internal error causing it to terminate.

What Next

Re-run the current session excluding the scenario in which the problem occurred.

Feedback

MS-022

(error) Insufficient hosts online to perform requested operation. (%d scenario(s) in focus, %d host(s) online)

Description

There are insufficient hosts online to perform the operation requested on the scenarios in command focus.

What Next

Reduce the number of scenarios in command focus to be at or below the number of hosts online.

If the distributed farm has been created and there are hosts not online yet, wait for them to come online before performing the operation. If all hosts are online, then add sufficient hosts to match the number of scenarios in command focus and bring them online.

MS-023

(error) Failed to checkout '%s' license required for execution.

Description

The scenario previously required the license indicated but the manager can no longer access that license from the server either because the license has expired or the user has set the limit on that license to zero during the flow.

What Next

Ensure the license indicated has not expired.

If the the manager sets the limit on the license to zero ensure this is done from the start of the flow rather during the flow so that the scenario never depends on the license.

MS-024

(Information) Entering Distributed Path-Based Analysis.

Description

The Distributed Path-Based Analysis has been activated. If there are more available distributed hosts in the *ONLINE* state than there are active scenarios in the current session, duplicate scenarios will be created to distribute Path-Based Analysis work.

Feedback

See Also

- report_host_usage

MS-025

(Information) Distributed Path-Based Analysis is disabled.

Description

The Distributed Path-Based Analysis has been disactivated.

See Also

- report_host_usage

MS-026

(Error) The variable multi_scenario_common_data_directory %s.

Description

The *multi_scenario_common_data_directory* variable must be specified as an absolute path, not a relative path. PrimeTime will create a directory in the location specified by this path if one does not already exist. A non-directory file is not a valid value for this variable. The directory specified will be used for the storage of multi-scenario *save_session* common data.

See Also

- save_session

MS-027

(Error) Failed to create common data directory %s.

Description

PrimeTime will attempt to create a common data directory in order to reduce the disk usage of saved sessions. This will be created either in the multi-scenario working directory or, in the case of an explicit save, in the saved image directory. Possible causes of a failure to create this directory include missing write permissions or insufficient disk space.

See Also

- save_session

Feedback

MS-028

(Warning) The affinity of scenario '%s' has been updated.

Description

The affinity specification for the scenario identified has changed.

See Also

- remove_multi_scenario_design
- remove_host_options

MS-029

(Warning) The affinity of scenario '%s' has been removed.

Description

The affinity specification for the scenario identified has been removed becasue all the host options making up the specification for the affinity have been removed.

The scenario will be free to execute on any available worker process in subsequent current sessions just as if the scenario had been created with no affinity specification.

See Also

- create_scenario
- remove_host_options

MS-030

(Error) The current session has been terminated because the affinity of one of its scenarios has changed.

Description

The removal of host opitons has altered the affinity specification of one of the scenarios in the session so the session has termianted.

See Also

- remove_host_options

Feedback

MS-031

(warning) scenario '%s' excluded from the current session because its affinity requirements cannot be satisfied.

Description

The scenario indicated was excluded from the current session because there were no worker processes online that can satisfy its affinity requirements. The current session will be created and the analysis will proceed without this scenario.

What Next

Use the *report_multi_scenario_design* command to view the affinity specification of the scenario and the *report_host_usage* command to view the status of the workers for the host options specified by the scenario's affinity. If need be remove the scenario using the *remove_scenario* command and re-create the scenario with a different affinity specification such that there is at least one worker online capable of running the scenario.

See Also

- current_session
- create_scenario
- report_host_usage
- report_multi_scenario_design

MS-032

(error) failed to create the current session because all scenarios were exclude due to unsatisfied affinity requirements.

Description

All scenarios specified to create the current session were excluded from the session because their affinity requirmenets could not be satisfied by the worker processes currently online.

In order for a session to be created at least one scenario must be capable of running in the session. Where a scenario specifies an affinity, at least one worker process for one of the host options specified in the affinity must be online. Where a scenario specifes no affinity then at least one worker process for any host options must be online.

What Next

Use the *report_multi_scenario_design* command to view the affinity specification of the scenarios used to create the session and use the *report_host_usage* command to view the

Feedback

status of the workers for the host options specified for all those scenarios affinities. Where a scenario's affinity cannot be satisfied, remove the scenario using the *remove_scenario* command and re-create the scenario with a different affinity specification such that there is at least one worker online capable of satisfying the scenario's affinity specification.

See Also

- current_session
- create_scenario
- report_host_usage
- report_multi_scenario_design

MS-033

(Error) The design loaded is different to the design loaded in other scenarios.

Description

When the *multi_scenario_license_mode* variable is set to '*core', all scenarios being analysed in the current session must contain the same design. The scenario issuing this error has detected that its design is different to that of other scenarios in the current session and is causing the current session to terminate.*

What Next

Set the *multi_scenario_license_mode* variable to '*scenario' to proceed with the analysis of the scenarios with different designs. Alternatively, ensure that all scenarios have the same design.*

See Also

- current_session
- multi_scenario_license_mode

MS-034

(Error) The current session is terminated because the scenarios being analysed are for different designs.

Description

When the *multi_scenario_license_mode* variable is set to '*core', all scenarios being analysed in the current session must contain the same design. If they do not, then the current session will terminate as soon as the scenarios load their designs.*

Feedback

What Next

Set the *multi_scenario_license_mode* variable to '*scenario' to proceed with the analysis of the scenarios with different designs. Alternatively, ensure that all scenarios have the same design.*

See Also

- current_session
- multi_scenario_license_mode

MS-035

(Error) Restore session at manager failed due to: %s.

Description

When restoring a session at the manager a save session could be initiated at the scenario to be restored at the manager.

What Next

Check if there is enough space for the save session to succeed

---

MS-036

(Error) The command *%s* could not be found.

MS-037

(Error) Restore session at manager failed due to: %s.

Description

A netlist inconsistency was detected. You can only restore a session when all the scenarios have identical netlists.

What Next

Ensure that all scenarios have identical netlists.

MS-038

(Error) Restore session at manager failed due to: %s.

Feedback

Description

You cannot restore a "timing path only" session at the manager. This is a session saved with the *save_session* command using the *-only_timing_paths* option.

What Next

To restore a "timing path only" session, use a regular PrimeTime shell session, not a DMSA manager.

MS-039

(Error) Restore session at manager failed due to: %s.

Description

When restoring a session at the manager, a save session could be initiated at the scenario to be restored at the manager.

What Next

See if the DMSA working directory is valid and has enough disk space to save the session.

MS-040

(Error) Loading of design data at DMSA manager failed because current session is not set.

Description

Loading of desing data from a DMSA scenario into the DMSA manager is not possible if the current DMSA session is not set.

What Next

Set the current session before loading desing data at the DMSA manager. Use the *current_session* command.

MS-041

(Error) Restore session at DMSA manager does not support one or more of the specified command options.

Description

When restoring a session at the manager, only the option to specify a scenario name can be used. Any additional options cannot be used with the *restore_session* command.

Feedback

What Next

When restoring a session at the manager, use the *restore_session* command only with the name of a DMSA scenario.

MS-042

(Error) Loading of design data at DMSA manager failed because a design is already loaded.

Description

You cannot load desing data at the DMSA manager when a design is already loaded.

What Next

Remove the existing design before attempting to load the data again.

MS-043

(Error) Loading of design data at DMSA manager failed because '%s' does not match a name of any scenario in session.

Description

The scenario to be used a source of DMSA manager's desing data must be in the current session.

What Next

Using the *current_session* command, check to see if the scenario is in the current session. If not, check to see if this is the intended scenario, or add the scenario to the current session using the *current_session* command.

MS-044

(Error) Loading of a design at the DMSA manager failed due to licensing requirements.

Description

Loading of a design at the Distributed Multi-Scenario Analysis (DMSA) manager process failed because the licensing requirements could not be met.

What Next

Allocate at least two PrimeTime license keys to the DMSA manager process.

Feedback

MS-045

(error) Application variable '%s' is not supported at the multi-scenario manager.

Description

You have attempted to set the indicated variable at the multi-scenario manager. However, this variable is supported only at the scenarios; its value at the manager is ignored.

What Next

Update your scenario scripts to directly apply the variable setting. This approach is best for settings that should be used for the entire analysis.

Alternately, use the *remote_execute* command to push the setting to the scenarios:

```
remote_execute {
  set_app_var application_variable {value}
}
```

With this method, consider whether the variable you are setting has any ordering requirements (for example, must be set before link) or runtime impact (triggers a timing or noise update).

MV

MV-001

(warning) Port '%s' is unconstrained.

Description

You receive this message because a port has been found to be unconstrained while running the *write_interface_timing* command. Unconstrained ports leave the paths connected to that port unevaluated, so any modeling issues associated with these paths would be hidden.

What Next

Use the *check_timing* command on the current design or *report_port* on a specific port to verify the port constraints before running *write_interface_timing*.

Feedback

See Also

- check_timing
- report_port
- write_interface_timing

MV-002

(error) Path group list is empty for design '%s'.

Description

You receive this message because no path groups were defined when running the *write_interface_timing* command. This should occur only if all path groups were removed (for example, by running the *remove_path_group* command with the *-all* option).

What Next

Use the *report_path_group* command to verify that path groups are defined before using *write_interface_timing*. Path groups should be left in their default state during model creation and validation.

See Also

- remove_path_group
- report_path_group
- write_interface_timing

MV-003

(warning) Unknown -ignore option '%s'.

Description

You receive this message because an entry in the *-ignore* option *ign_list* in the *compare_interface_timing* command line was invalid.

What Next

Check the spelling of the option used and compare it against the names listed in the *compare_interface_timing* command man page or *-help* list.

See Also

- compare_interface_timing

Feedback

MV-004

(warning) Unknown -include option '%s'.

Description

You receive this message because an entry in the -include option *cmp_list* in the *compare_interface_timing* command line was invalid.

What Next

Check the spelling of the option used and compare it against the names listed in the *compare_interface_timing* command man page or *-help* list.

See Also

- compare_interface_timing

MV-005

(warning) The format of the timing file '%s' is nonstandard.

Description

You receive this message because one of the timing files specified in the *compare_interface_timing* command line does not exactly follow the *write_interface_timing* output format.

What Next

This should occur only if the timing file has been modified or if it was created by some means other than by using the *write_interface_timing* command. Compare the nonstandard timing file with one generated by *write_interface_timing* to determine what condition might be causing the warning.

See Also

- compare_interface_timing
- write_interface_timing

MV-006

(warning) The design name was missing from the timing file '%s'.

Feedback

Description

You receive this message because one of the timing files specified in the *compare_interface_timing* command line is missing the Design field.

What Next

This should occur only if the timing file has been modified or if it was created by some means other than by using the *write_interface_timing* command. Compare the nonstandard timing file with one generated by *write_interface_timing* to determine what condition might be causing the warning.

See Also

- compare_interface_timing
- write_interface_timing

MV-007

(warning) An unknown attribute '%s' was found in a timing file.

Description

You receive this message because one of the timing files specified in the *compare_interface_timing* command line contains an unknown path attribute.

What Next

This should occur only if the timing file has been modified or if it was created by some means other than by using the *write_interface_timing* command. Refer to the *write_interface_timing* command man page for a list of acceptable attributes.

See Also

- compare_interface_timing
- write_interface_timing

MV-008

(error) No data is found in section '%s' of timing file '%s'.

Description

You receive this message because one of the timing files specified in the *compare_interface_timing* command line is missing one of the following four sections: slack, transition_time, capacitance, or design_rules.

Feedback

What Next

This should occur only if the timing file has been modified or if it was created by some means other than by using the *write_interface_timing* command.

See Also

- compare_interface_timing
- write_interface_timing

MV-009

(warning) The -include option '%s' should not be used with '%s' data.

Description

You receive this message because one of the timing files specified in the *compare_interface_timing* command line contains a different type of timing data than is specified in the *-include* option.

What Next

Match the timing data name with a keyword in the *cmp_list* specified in the *-include* option.

See Also

- compare_interface_timing

MV-010

(error) Arc data '%s' cannot be compared with slack data '%s'.

Description

You receive this message because the two timing files specified in the *compare_interface_timing* command line contain different timing data types: arc data in the first and slack data in the second.

What Next

Determine that the *-timing_type* option of *write_interface_timing* was set correctly when the command was used to create these two files. To compare the other data sections, use the *compare_interface_timing* command with the *-include* option to list the sections you want.

Feedback

See Also

- compare_interface_timing
- write_interface_timing

MV-011

(warning) No data was written for section '%s'.

Description

You receive this message because the particular data section of *write_interface_timing* will be empty.

What Next

This warning indicates that the design is not properly setup to do model validation. To identify the problem, run *check_timing* or look for errors/warnings that preceded this command.

See Also

- write_interface_timing
- check_timing

MV-012

(warning) Pin '%s' is an internal start or end point. Ignoring paths to and from this pin.

Description

You receive this message if the *write_interface_timing* command finds a pin that is an internal start or end point, which indicates that the pin is participating in a timing exception such as by *set_max_delay* or *set_min_delay* specified on it. Because of *extract_model* does not support such qualifiers, *write_interface_timing* does not check it.

What Next

Use *report_exceptions* to identify all *max_delay*, *min_delay*, remove them, and re-execute *write_interface_timing*.

See Also

- write_interface_timing
- extract_model

Feedback

- set_max_delay
- set_min_delay
- report_exceptions

MV-013

(Information) all model validation immediate outputs are stored in directory '%s'.

Description

Auto model validation creates a set of immediate files (e.g., the validation results after graph-based analysis) that help the validation. All these files are stored in the directory mentioned in this message. If a different directory is needed, please set *model_validation_working_directory*.

MV-014

(Error) model validation failed.

Description

Model validation failed because of the reasons that are shown during the validation.

See Also

- hier_modeling_version
- create_ilm
- extract_model

MV-015

(Warning) the topologies of these two paths are different, so another path comparison is done: the path in the block whose topology is exactly the same with the topology of the path from the model is compared againt the path from the model.

Description

One type of model validation failure is the topologies of critical paths from the block and the model are different. In order to see why different critical paths are selected, a path whose topology is exactly the same with the topology of the path from the model is selected from the block, and is compared against the path from the model.

Feedback

See Also

- hier_modeling_version
- create_ilm
- extract_model

MV-016

(Warning) Detailed path comparison cannot be performed because this model is a wrapper plus core style ETM.

Description

For wrapper plus core style ETM, there maybe multiple paths between ports, but the detailed path comparison requires that the path is unique. Please use *report_etm_arc* if detailed debugging is needed.

See Also

- hier_modeling_version
- create_ilm
- extract_model
- report_etm_arc

MV-017

(warning) PBA and detailed path comparison on mismatched paths cannot be performed because of transparent latches on boundary.

Description

PBA and detailed path compasion cannot be done if transparent latches are on boundary, and the model is created with -context_borow or positive latch_level.

What Next

Delete -context_borrow or change the latch_level to 0.

See Also

- create_ilm
- extract_model

Feedback

MV-018

(Warning) PBA and detailed path comparison on mismatched paths cannot be performed because the analysis type of the design is not on_chip_variation.

Description

PBA and detailed path compasion cannot be done if the analysis type of the design is not on_chip_variation.

See Also

- hier_modeling_version
- set_operating_conditions
- create_ilm
- extract_model

MV-019

(Information) PBA and detailed path comparison on mismatched paths will not be performed because SI is disabled in this ILM.

Description

PBA and detailed path compasion will not be performed if SI is diabled during the creation of ILM. For non-SI ILM, PBA does not have significant impact on reducing the number of failures for PT-ILM, and thus it is disabled.

See Also

- hier_modeling_version
- create_ilm

MV-020

(error) Model validation cannot be performed in a DMSA worker run and will be skipped.

Description

During create_ilm or extract_model, automatical model validation cannot be performed in a DMSA worker run. Model generation will continue without auto validation.

Feedback

What Next

create_ilm or extract_model in a non-DMSA run.

See Also

- create_ilm

MV-021

(Warning) Cell instance %s does not have needed supply group %s for use with define_cell_alternative_lib_mapping -dvfs_scenarios.

Description

The *-dvfs_scenarios* option of the *define_cell_alternative_lib_mapping* command can be used on cells only when the DVFS scenarios depend entirely on the supply groups attached to the cell.

What Next

Modify the DVFS scenario specification to be relevant only to the supply groups attached to the cell.

See Also

- timing_enable_cross_voltage_domain_analysis
- define_cell_alternative_lib_mapping

MV-022

(Information) Building multi voltage information for entire design.

Description

Voltage information is required for delay calculation and this information is created whenever commands which alter the voltage, for example, set_voltage are issued. The message informs the user whenever the voltage infomation is re-built. The message is issued in both single voltage or multi-voltage designs.

See Also

- set_voltage
- get_lib_cell
- update_timing

Feedback

MV-023

(Warning) Multiple output pins exists on the driving cell of port %s. Voltage is picked from voltage map of libpin %s.

Description

While picking the voltage for ports having driving lib cells, PT will use the votlage map of output pin's related_power_pin of the driving libcell. If there are multiple output pins, it will pick up the first one. This message will warn the user about this.

See Also

- set_voltage
- set_driving_cell

MV-024

(Information) %s detailed analysis of failed paths.

Description

This message is to inform the status change of detailed analysis of failed paths.

MV-025

(error) Must specify timing_cross_voltage_domain_analysis_mode to capture_reduced_model before using write_xdoamin_design.

Description

During generating the reduced cross-domain design using *write_xdomain_design* command, you must specify *timing_cross_voltage_domain_analysis_mode* to *capture_reduced_model*.

What Next

Specify *timing_cross_voltage_domain_analysis_mode* to *capture_reduced_model*.

See Also

- write_xdomain_design
- timing_cross_voltage_domain_analysis_mode

Feedback

MVOLT

MVOLT-001

(error) Set_voltage failed on %s.

Description

Cannot find the power net or PG pin to set voltage on.

What Next

Ensure that the object exists. To create a power net, use the *create_power_net_info* command. For a PG pin, use Liberty libraries that consider PG information.

MVOLT-051

(information) Cross-voltage domain analysis is enabled. Within domain timing paths are not reported.

Description

You received this message because the *timing_enable_cross_voltage_domain_analysis* variable is set to *true*. As a result, paths that are within the same supply net domain are not reported.

What Next

First, determine whether you want to see only cross-domain paths. If yes, then no action is required on your part. If no, then set the *timing_enable_cross_voltage_domain_analysis* variable to *false*.

MVOLT-052

(error) Power net %s does not exist.

Description

Cannot find the power net.

What Next

To create a power net, use the *create_power_net_info* command.

Feedback

MVOLT-065

(error) Cell %s already belongs to power domain %s.

Description

A cell cannot belong to more than one power domain.

What Next

Review all *create_power_domain -object_list* commands, and make sure that they define non-overlapping sets of objects.

MVOLT-066

(Warning) Set_voltage failed on cell %s as the pg pin %s is either disabled or excluded.

Description

Cannot set the voltage on specified PG Pin as the pg pin is either disabled using set_disable_pg_pins or the rail is excluded in DSLG command.

What Next

Ensure that the object exists. To create a power net, use the *create_power_net_info* command. For a PG pin, use Liberty libraries that consider PG information.

MVOLT-067

(Information) Setting voltage on pg_pin %s same as the pg pin %s due to the existence of PG function.

Description

This message is issued when instance specific set_voltage is done. If voltage is set on a pg_pin, then the voltage on internal pins of the cell, whose PG function is defined to be the specified pg_pin in the set_voltage command, are set to the specfied value.

MVOLT-068

(Warning) Nominal voltage for scaling usage set on lib cell of %s but none specified in set_voltage command. Attribute will be ignored.

Description

This message is issued when a lib cell has user defined attribute to use nominal voltage for scaling, but nominal field was not specified in *set_voltage* command. The lib cell attribute will be ignored and it falls back to original flow.

Feedback

What Next

Ensure *-nominal* field exists in *set_voltage* command for setting voltage to supply net or supply group, if lib cell has *use_nominal_voltage_slg* attribute. If issue still exists, please report it so the testcase can be debugged.

NDM

NDM-001

(error) %s

Description

This message indicates an internal data model error.

What Next

Send the log to Synopsys.

NDM-002

(error) %s

Description

Permission denied.

What Next

Please set proper access right and rerun.

NDM-003

(error) %s

Description

The object already exists.

What Next

Please don't create an object with name/id of an existing object.

NDM-004

(error) %s

Feedback

Description

Input has invalid argument.

What Next

Please send the log to Synopsys.

NDM-005

(error) %s

Description

Operation interrupted.

What Next

Please send the log to Synopsys.

NDM-006

(error) %s

Description

Is a directory.

What Next

Please check and use the right file name.

NDM-007

(error) %s

Description

No such file or directory.

What Next

Please check and use the right file/directory name.

NDM-008

(error) %s

Feedback

Description

Out of memory.

What Next

Please pick a machine with large enough memory and rerun.

NDM-009

(error) %s

Description

Not a file.

What Next

Please check and use the right file name.

NDM-010

(error) %s

Description

Not a directory.

What Next

Please check and use the right directory name.

NDM-011

(error) %s

Description

Not (yet) implemented.

What Next

Please send the log to Synopsys.

NDM-012

(error) %s

Feedback

Description

Operation timed out.

What Next

Please check and retry.

NDM-013

(error) %s

Description

File open/lock/read/write error

What Next

This is an internal error. Please report to Synopsys.

NDM-014

(error) %s

Description

Object not exists

What Next

This is an internal error. Please report to Synopsys.

NDM-015

(error) %s

Description

Invalid Object

What Next

Internal message, please report to Synopsys.

NDM-016

(error) NDM file version %s is no longer supported. Current compatible version is %s.

Feedback

Description

This version of the NDM file is not supported.

What Next

Re-generate design and library data with the latest binary.

NDM-017

(error) Failed to read %s object from file %s.

Description

The specified object could not be read correctly read from file because of an I/O error.

What Next

Re-create the file with the latest executable.

NDM-018

(error) Failed to restore %s object from file %s.

Description

The object cannot be correctly restored from file because of an I/O error.

What Next

Re-create the file with the latest executable.

NDM-019

(error) Cannot save the library or block because it is in read-only mode.

Description

The library or block cannot be saved to disk because it was opened in read mode.

What Next

Close the library or block and reopen it in edit mode.

NDM-020

(error) '%s' is not a valid NDM binary file

Feedback

Description

The file cannot be read because not in valid NDM binary format.

What Next

Verify the file location is correct or re-create it with the latest binary.

NDM-021

(warning) re-binding failed for %s '%s'.

Description

Re-binding a cell to a valid reference block failed during *open_block*.

Binding failed either because the target reference block could not be found, or because the target reference block port interface has changed since the last time this cell was bound.

What Next

If the target block was not found, verify that the search_path location or reference library list setting correctly identifies the target block and try again.

If the target block port has changed, use the *link_block* command to update the cell's pin interface to match the referenced block's new port interface.

NDM-022

(warning) '%s' is logical only. Placement status is not available.

Description

Placement status cannot be set on a logical only cell/port.

NDM-023

(error) Placement status cannot be set on object type '%s'.

Description

Placement status can only be set on cells and ports.

NDM-024

(error) Invalid %s placement status '%s'.

Feedback

Description

For ports, valid status values are unplaced, placed, fixed, and locked. For cells, valid status values are unplaced, placed, legalize_only, application_fixed, fixed, and locked.

What Next

Specify a valid placement status.

NDM-025

(error) The value %f is too %s causing an arithmetic overflow error.

Description

The specified value cannot be represented within the database. It is either too large or too small, causing an arithmetic overflow error when converted into internal database units.

What Next

Check the technology units and specify a valid value.

NDM-026

(error) Can not create hier_boundary as the cell already has a hier_boundary.

Description

The hierarchical cell already has a hier_boundary associated with it, therefore hier_boundary creation has failed.

What Next

Please provide proper input to command.

NDM-027

(error) Can not create partition as the cell is already a partition.

Description

The hierarchical cell is already a partition, therefore partition creation has failed.

What Next

Please provide proper input to command.

Feedback

NDM-028

(warning) Block '%s.%s' is out of sync with the '%s' view. '%s' view has changed since last synced.

Description

The specified block view has changed since it was set to be in-sync with its source view.

What Next

please re-sync the (derived) block with its source view.

NDM-029

(error) '%s' failed. Block '%s' is being edited by process %d %s@%s.

Description

The specified operation failed because write acccess is held by another process.

What Next

Please coordinate with the user holding the block for edit about saving and releasing the write access.

NDM-030

(error) %s for design %s does not match design %s: found '%s', expected '%s'

Description

While comparing two designs, the function id does not match.

What Next

If running the library manager, this design will be removed from the library in question. However, libraries with this sort of error are probably out of date and should not be used.

NDM-031

(error) Port %s missing on %s

Description

While comparing two designs, a port was found on one but not the other.

Feedback

What Next

If running the library manager, this design will be removed from the library in question. However, libraries with this sort of error are probably out of date and should not be used.

NDM-032

(error) Direction '%s' for port %s on %s\n \tdoes not match expected value '%s' from %s

Description

While comparing two designs, a port has a different direction in each design.

What Next

If running the library manager, this design will be removed from the library in question. However, libraries with this sort of error are probably out of date and should not be used.

NDM-032w

(warning) Direction '%s' for port %s on %s\n \tdoes not match expected value '%s' from %s

Description

While comparing two designs, a port has a different direction in each design.

What Next

If running the library manager, this design will be removed from the library in question. However, libraries with this sort of error are probably out of date and should not be used.

NDM-033

(Error) %s '%s' for pin %s on %s does not match the expected value '%s' from %s.

Description

The tool issues this warning message if it detects a pin that has a different *port_type* or *pg_type* attribute when comparing two designs. The *port_type* attribute identifies the type of the library cell pin, such as *signal*, *power*, or *ground*. The *pg_type* attribute identifies the type of a PG pin, such as *backup*, *internal*, or *primary*.

- The *check_workspace* command issues this message for *pg_type* mismatches between two designs in the library workspace.
- The *compare_db* command issues this message for both *port_type* and *pg_type* mismatches between the design in the base library and the comparison library.

Feedback

What Next

If you get this message during library preparation, by default, the design is removed from the reference library. To modify this behavior, set a mismatch configuration.

If you get this message during library validation, the library is probably out-of-date and you not should use it.

NDM-034

(error) Cannot locate block %s for instance %s.

Description

The instance is attempting to bind to a physical block, but the requested view of the physical block cannot be located, so the instance is unbound.

What Next

A number of things can go wrong when looking for a view of a block.

Verify that the block exists, and is in a library that is loaded into the session.

Verify that the library is on the reference library list of the library containing the top block.

The desired view may be obscured by another block in an earlier library. Look at the viewtype requested for that instance. Verify that the desired view (DESIGN ABSTRACT OUTLINE) exists for that block in the first reference library that contains a block of that name.

NDM-035

(error) NDM_LOCK_FAIL_ACTION `%s' not one of: `off', `complain', or `die'. Turning off.

Description

This is a internal error. Please report to Synopsys.

What Next

Internal error, please report to Synopsys.

NDM-036

(info) %s lock check failed!.

Description

This is a internal message. Please report to Synopsys.

Feedback

What Next

Internal message, please report to Synopsys.

NDM-037

(warning) Conn count of instance '%s' does not match reference module '%s'

Description

The conn count of the specified instance '%s' does not match its reference module. This could be caused by a change in the port interface after the instance was created.

What Next

Verify the port interface of the reference module matches the instance.

NDM-038

(warning) power_domain '%s' is already associated with a voltage_area.

Description

The specified power_domain is already associated with a voltage_area.

What Next

Specify a different power_domain and try this command again.

NDM-039

(warning) Top-level power_domain '%s' is reserved for default voltage_area.

Description

The specified top-level power_domain is reserved for the default voltage_area.

What Next

Specify a different power_domain and try this command again.

NDM-040

(information) NDM file '%s', version %s does not match current version %s.

Description

The NDM file is of an earlier version than the current version.

Feedback

NDM-041

(info) Net '%s' has been created.

Description

This is a verbose message indicating the named net has been created.

NDM-042

(info) Port '%s' has been created.

Description

This is a verbose message indicating the named port has been created.

NDM-043

(info) Net '%s' has been connected to %s '%s'.

Description

This is a verbose message indicating the net has been connected to the pin/port.

NDM-044

(info) Net '%s' has been disconnected from %s '%s'.

Description

This is a verbose message indicating the net has been disconnected from the pin/port.

NDM-045

(error) Unable to create net '%s'. A net of that name already exists.

Description

This is an internal error. Please report to Synopsys.

NDM-046

(warning) Connection from net '%s' to %s '%s' is not consistent with supply net '%s'.

Feedback

Description

The intended connection is not consistent with supply net, but the manually specified connection has been made.

NDM-047

(warning) Unable to create net '%s'. A net of that name already exists. Net is renamed to '%s'.

Description

Net has been renamed in order to make specified connection.

NDM-048

(error) MV data is not ready.

Description

MV data is not ready to run this command. Please run commit_upf.

NDM-049

(error) The conflicts between PG network (%s'%s') and UPF (%s'%s') have not been resolved.

Description

The conflicts between PG network and UPF must be resolved before running this command.

NDM-050

(error) Unable to create port '%s'. A port of that name already exists.

Description

This is an internal error. Please report to Synopsys.

NDM-051

(error) Unable to determine the supply net to connect to the tie net '%s'.

Description

This is an internal error. Please report to Synopsys.

Feedback

NDM-052

(error) Cannot push into partition '%s'.

Description

The partition cannot become current block.

NDM-053

(error) Unable to determine supply net to connect to %s '%s'.

Description

Supply net cannot be determined to make tie connection.

What Next

Fix your power constraints and try again.

NDM-054

(warning) Unable to determine supply net to connect to %s '%s'. %s

Description

Supply net cannot be determined to make tie connection. This could be due to related power/ground pin is not defined for the signal pin in library or supply net connection cannot be determined for the related power/ground pin by UPF.

What Next

Check whether related power/ground pin is defined for the signal pin in library or supply net connection for the related power/ground pin is defined in UPF. If the pin is a macro input pin that is related to an internal pg pin, consider to set the app option "mv.upf.use_preswitched_supply_for_macro_pins" to use the pre-switched supply to determine the supply net for the tie connection.

NDM-055

(info) In block '%s', uniquifying module '%s' from '%s' for cell '%s'.

Description

This is a verbose message indicating the multiply instantiated module (MIM) has been automatically split into two modules so that changes to that instance of the module for that logical cell will not be replicated into all cells that reference that module.

Feedback

A cell's module can be auto-uniquified whenever the contents of the cell are changed. Only multiply instantiated cell modules (MIMs) will be auto-uniquified. Physical blocks and lib cells are never uniquified.

What Next

This message can be enabled or disabled by setting the *design.verbose_uniquify* app option.

You can get a cell's reference module with the *ref_name* attribute.

You can get all the modules in a block with the *get_modules* command.

See Also

- get_attribute
- cell_attributes

NDM-056

(info) Port '%s' is removed.

Description

This is a verbose message indicating the port is removed.

NDM-057

(info) Net '%s' type is set to be '%s'.

Description

This is a verbose message indicating the net type is set.

NDM-058

(info) Net '%s' name is set to be '%s'.

Description

This is a verbose message indicating the net name is set.

NDM-059

(info) Net '%s' is removed.

Feedback

Description

This is a informational message indicating the net is removed when resolve_pg_nets resolves the conflicts between power intent (based on UPF) and pg net connections (from DEF or PG netlist).

What Next

Please check the power intent.

NDM-060

(info) Port '%s' direction is set to '%s'.

Description

This is a verbose message indicating the port direction is set.

NDM-061

(info) %s '%s' cannot be created because the %s is not PG type.

Description

This is a verbose message indicating that the named port/net cannot be created since the supply port/net is not PG type.

NDM-062

(warning) Block '%s.%s' is out of sync with the '%s' view. Both views have changed since last synced.

Description

The specified block views have changed since they were set to be in-sync.

What Next

please re-sync the block views.

NDM-063

(information) Block '%s' is not being saved because it is in read mode.

Description

The specified block view is not saved because it is open in read mode.

Feedback

What Next

Open the block in edit mode and try again.

NDM-064

(info) Creating block '%s', mode '%s'.

Description

This is a verbose message indicating the named block has been created with the named open mode.

A block can have one of three open modes: A new, unsaved block has an open mode of 'new'. A block open for modification has an open mode of 'edit'. A block open read-only has an open mode of 'read'.

What Next

This message can be enabled or disabled by setting the *design.verbose_io* app option.

You can get a block's open mode with the *open_mode* attribute.

See Also

- get_attribute

NDM-065

(info) Opening block '%s', mode '%s'.

Description

This is a verbose message indicating the named block has been read in from its library with the named open mode.

What Next

This message can be enabled or disabled by setting the *design.verbose_io* app option.

You can get a block's open mode with the *open_mode* attribute.

See Also

- get_attribute

Feedback

NDM-066

(info) Saving block '%s'.

Description

This is a verbose message indicating the named block has been written to its library.

What Next

This message can be enabled or disabled by setting the *design.verbose_io* app option.

See Also

- save_block

NDM-067

(info) Closing block '%s'.

Description

This is a verbose message indicating the named block has been closed and removed from memory.

What Next

This message can be enabled or disabled by setting the *design.verbose_io* app option.

NDM-068

(info) Changing block '%s' mode from '%s' to '%s'.

Description

This is a verbose message indicating the named block's open mode has been changed from its previous mode to a new mode.

A block can have one of three open modes: A new, unsaved block has an open mode of 'new'. A block open for modification has an open mode of 'edit'. A block open read-only has an open mode of 'read'.

What Next

This message can be enabled or disabled by setting the *design.verbose_io* app option.

You can get a block's open mode with the *open_mode* attribute.

Feedback

See Also

- get_attribute

NDM-069

(error) Cannot include read-only block '%s' as an editable part of abstract '%s'.

Description

When creating an editable abstract, all of the editable sub-blocks of the abstract must first be opened in edit mode. It is possible the the read-only block in question is already part of an existing abstract.

The new abstract cannot be created.

What Next

Use the reopen_block command to obtain edit permission for the given block. Alternatively, you could create a read-only abstract.

NDM-070

(error) Cannot include '%s' as a part of new abstract '%s'. Existing abstract '%s' must be merged or removed first.

Description

When creating a new abstract, none of the sub-blocks of the abstract may be part of an existing editable abstract. The abstract cannot be created.

What Next

You can merge the changes in the existing editable abstract by using the merge_abstract command. After running that command, the abstract will no longer be editable, and new abstracts can be created.

Alternatively, you can remove the existing editable abstract by using the remove_abstract command.

NDM-071

(information) Saving '%s' and adding it as a part of editable abstract '%s'.

Feedback

Description

The given block is now part of an editable abstract. The block has been written to disk, and has been set to read-only. The block will remain read only while the editable abstract still exists.

What Next

You might see future information messages that the read-only block cannot be saved. This is OK, because it was saved in this step.

In order to make your block editable again, you must either merge the changes in the editable abstract by using merge_abstract, or you can remove the existing editable abstract by using the remove_abstract command.

NDM-072

(warning) Non-editable abstract '%s' can only be opened as read-only

Description

An attempt was made to open a read-only abstract in edit mode. The abstract has been opened in read-only mode instead.

What Next

If you want to edit or optimize the logic inside of an abstract, you must create an editable abstract. Refer to the create_abstract man page for details.

NDM-073

(information) %s view of block '%s' is not being saved because it is in read mode.

Description

The specified block view is not saved because it is open in read mode.

What Next

Open the block in edit mode and try again.

NDM-074

(warning) Block '%s' can only be opened as read-only because it is part of an editable abstract '%s'.

Feedback

Description

When a block is included in an editable abstract, it becomes read-only. The abstract must be processed or deleted before the block may be edited again.

What Next

In order to make your block editable again, you must remove the existing editable abstract by using the remove_abstract command.

Alternatively, you may force the block to be editable by using "reopen_block -edit". If you do this, the editable abstract will be rendered unusable.

Changes made in the editable abstract view since its creation are automatically merged to the design view when the design view is loaded into memory.

NDM-075

(warning) Block '%s' was part of editable abstract '%s'. The abstract has been downgraded to read-only.

Description

When a block is included in an editable abstract, it becomes read-only. The abstract must be processed or deleted before the block may be edited again.

By using the reopen_block command, you have forced the block to be editable. This means that the editable abstract is no longer usable. You will not be able to perform the merge_abstract operation.

What Next

If you need a new editable abstract, you need to rerun the create_abstract command.

NDM-076

(error) The abstract for block '%s' is not editable. The merge_abstract operation is not possible.

Description

Only editable abstracts can be merged back into their parent block.

What Next

Please refer to the create_abstract man page for details about creating editable abstracts.

Feedback

NDM-077

(error) The abstract for '%s' depends on the design view of block '%s:%s', but the design view has changed or is missing. The merge_abstract operation is not possible.

Description

When using editable abstracts, it is important to preserve the original design view block hierarchy on which the abstract is based. It is not possible to merge changes from the abstract back to the design view, if the block has changed or you are using a different copy of the block.

What Next

It is possible that you changed the original design view hierarchy by using "reopen_block" or "remove_abstract". If the design view has changed, then you cannot run merge_abstract. Use remove_abstract on your top-level block to return it to a writable state.

It is also possible that you did not change your original design view hierarchy, but you are instead using a modified *copy* of your original design view. Try to find the copy of the block that was used to create the abstract.

NDM-078

(error) Cannot include view '%s' of block '%s:%s' in an abstract.

Description

When creating an abstract, the subblocks of the design must either be a "design" view or an "abstract" view.

What Next

Use the change_link command to include the proper view for the subblock.

NDM-079

(information) %s view of block '%s:%s' has been restored to edit mode.

Description

After merging or deleting an editable abstract, the blocks on which the abstract was based are reverted to edit mode.

What Next

No action is required.

Feedback

NDM-080

(warning) Orientation %s of cell %s is not allowed for grid %s.

Description

A snap to grid operation is called trying to move the specified cell instance to be on the specified grid. However, the current orientation of the cell instance is not allowed for the specified grid. The cell is not moved.

What Next

Check the cell's orientation, see if it needed to be rotated. Also check the association of the cell and the grid, see if the cell needs to be using another grid.

NDM-081

(warning) Cell %s is not associated with grid %s.

Description

A snap to grid operation is called trying to move the specified cell instance to be on the specified grid. However, the cell instance is not associated with the specified grid. The cell is not moved.

What Next

Check the association of the cell and the grid.

NDM-082

(warning) Problem exporting %s %s : %s.

Description

A problem was encountered when exporting the specified object to the specified format, likely due to differences between the object's configuration in the current database versus the configurability of the object in the target format.

NDM-083

(error) Write-access request for %s failed. Library '%s' is being edited by process %d %s@%s.

Description

Write ccess requested by the specified operation failed because the library is being edited by another process.

Feedback

What Next

Please either try again (write-access on libraries are only held for a short time during actual write-to-disk and read-from-disk operation), or coordinate with the user holding the library for edit about releasing it.

The maximum wait time is controlled by the app_option "lib.setting.max_wait_time". The default value is 3600 seconds.

NDM-084

(error) '%s' failed. Another process has modified and saved library '%s' while this process was running, or a library with the same name has been copied, renamed or unpacked into this save location.

Description

The specified operation failed because the library was modified and saved by another process while this process was running, or a library with the same name has been copied, renamed or unpacked into this save location.

What Next

Please use save_lib -as to save your work to another library, or move/remove the conflicting on-disk library.

NDM-085

(error) Cannot %s %s %s because %s.

Description

The specified remove, modify, or create operation for the named type of the object given at full path has failed for the reason stated. or a library with the same name has been copied, renamed or unpacked into this save location.

Examples

ERROR: Cannot remove net Reset because net is marked don't touch. (NDM-085)

What Next

Obey the restriction, which is meant to keep the user from making unsafe changes that will have side effects in the flow. If this is not practical, set the app option design.eco_restrictions to false, and the operation will be permitted. Note that in the case of permitted unsafe changes, the performance may suffer significantly due to the requirements for more detailed checking and updating or recreation of many parts of the system data.

Feedback

NDM-086

(error) NDM file version %s is newer than the currently supported version %s. Use '%s <new_name>' in your original %s program to create an NDM library which can be read by this version of %s. See the man page for '%s' for further details.

Description

The library version is newer than the currently supported version.

What Next

Use the original program that creates the library and save it to a supported version:

```
On IC Compiler II:

prompt> open_lib <lib_name>
prompt> save_lib -version J-2014.12 -as <new_name>

On IC Compiler II Library Manager:

prompt> create_workspace <workspace_name>
prompt> open_lib <lib_name>
prompt> commit_workspace -version J-2014.12
```

NDM-087

(warning) Block %s not found in current design, skipping.

Description

A block listed in the connect_pg_net -block option could not be found instantiated in the current design. Connect_pg_net will skip missing blocks.

What Next

To eliminate warnings, update -block list to include only blocks which are instantiated directly in current design.

NDM-088

(info) Attempting to acquire write access for library (max wait until timeout is %d seconds).

Description

Waiting to acquire write access on library which is held by another process.

Feedback

NDM-089

(error) Another process has modified attributes and saved library '%s' while this process was running.

Description

The specified operation failed because attributes in this library were modified and saved by another process while this process was running.

What Next

Please use save_lib -as to save your work to another library, or move/remove the conflicting on-disk library.

NDM-090

(error) Multiple processes have simultaneously attempted to create the same design '%s' and save to library '%s'.

Description

The specified operation failed because multiple processes attempted to simultaneously create and save the same design to a library.

What Next

Please use save_lib -as to save your work to another library, or move/remove the conflicting on-disk library.

NDM-091

(error) Another processes attempted to delete the open design '%s' (detected while saving to library '%s').

Description

The specified operation failed because another processes attempted to delete a design that is open in the current process.

What Next

Please use save_lib -as to save your work to another library, or move/remove the conflicting on-disk library.

NDM-092

(error) Unable to create %s '%s'. A %s already exists%s.

Feedback

Description

The specified operation failed because an object with the given name/attribute already exists.

What Next

Choose a different name/attribute for this new object.

NDM-093

(error) '%s' has an experimental schema version '%s' incompatible with this production binary. The binary schema version is '%s'.

Description

The file has an experimental schema version. It is meant only for testing and it can only be opened with binaries from the same experimental branch. This schema version is incompatible with regular release versions and cannot be opened with production binaries.

What Next

Try again with a binary from the same experimental branch.

NDM-094

(error) '%s' of experimental schema version '%s' is incompatible with this experimental binary from a different experimental branch. The binary schema version is '%s'.

Description

The file has an experimental schema version. It is meant for testing only and can be opened with binaries from the same experimental branch. This schema version is incompatible with regular release binaries or binaries with a different experimental suffix (The last portion of the schema version after .X).

What Next

Try again with a binary from the same experimental branch.

NDM-095

(warning) Could not restore binding for reference '%s'.

Description

During *open_block* a block or lib cell reference could not be restored.

Feedback

The block being opened contains a reference to another block or lib cell. A block or lib_cell of that name could not be found in that library. The binding to that referenced block or lib cell could not be restored.

What Next

Verify that the requested library is in the ref_lib list and is open.

Check the named library to verify that a block with that name exists.

Use the *link_block* command to restore the bindings of the references in this block.

See Also

- search_path

NDM-096

(warning) Could not restore binding. Cannot locate library for reference '%s'.

Description

During *open_block* a block or lib cell reference could not be restored.

The block being opened contains a reference to another block or lib cell. The binding to that referenced block or lib cell could not be restored because the referenced library could not be found in the current ref_lib list.

What Next

Verify that the search_path location or reference library list setting correctly identifies the target block and try again.

If the reference libraries have moved but are still in the search_path, update the path to the ref_libs and re-link the design:

```
prompt> set_ref_libs -rebind
prompt> link_block
```

If the search_path to ref_lib list needs to be updated, do so, then re-link the design:

```
prompt> set_ref_libs -ref_libs { ... }
prompt> link_block
```

See Also

- search_path

Feedback

NDM-097

(warning) Could not restore binding. Cannot locate block view '%s' for reference '%s'.

Description

During *open_block* a block or lib cell reference could not be restored.

The block being opened contains a reference to another block or lib cell. The binding to that referenced block or lib cell could not be restored because the referenced block view could not be found in that library.

What Next

Check the referenced library to see what views exist of that block:

```
prompt> get_blocks -all -lib_cells LIBRARY-NAME:BLOCK-NAME.*
```

If the desired block view is in another library, make that library part of the reference library list with the *set_ref_libs* command. Then re-link the design with the *link_block* command.

If a different block view is desired, change the cell's reference with the *change_view* or *set_reference* command.

See Also

- search_path

NDM-098

(warning) Could not restore binding. Port interface of block '%s' does not match reference '%s'.

Description

During *open_block* a block or lib cell reference could not be restored.

The block being opened contains a reference to another block or lib cell. The binding to that referenced block or lib cell could not be restored because the port interface of the referenced block has changed since the block was last saved.

What Next

Update the cell's pin interface to match the referenced block's new port interface using the *link_block* command:

```
prompt> link_block
```

Feedback

NDM-099

(info) Running auto PG connection.

Description

This is a message indicating auto PG connection is running.

NDM-100

(error) Another process deleted design '%s' (detected while syncing to library '%s').

Description

The specified operation failed because another process deleted a design that is not yet opened in the current process.

What Next

The specified design is no longer available. Check the flow or concurrent library environment.

NDM-101

(error) Cannot open block '%s'. Binding to technology library is missing.

Description

The reference technology library for this block is required but is missing. The block cannot be opened until this reference is resolved. Check the refLib list on the library and verify all refLibs are bound.

What Next

Use report_ref_libs to verify all refLibs are bound. Unbound refLibs are those refLibs whose name or location are not available. If there are unbound refLibs, modify the search_path so that the refLib paths are reachable and use set_ref_libs -rebind to restore the binding.

```
prompt> report_ref_libs
****************************************
Report : Reference Library Report
Library: 1
****************************************

   Name Path      Location
   -----------------------
   -    tech_lib  -
    "-" = Name and location not available
```

Feedback

```
1

prompt> set_ref_libs -rebind
```

NDM-102

(warning) Technology '%s' used for frame-view creation in library '%s', is inconsistent with the current technology '%s' of library '%s'. Please run derive_design_level_via_regions to generate up-do-date via region in the design library.

Description

The technology of the reference library is inconsistent with technology of the design library. Need to run derive_design_level_via_regions to generate up-do-date via region in the design library.

What Next

Update the library with consistent technology and try again. Or run derive_design_level_via_regions to generate up-do-date via region in the design library.

NDM-103

(info) %s Sparse View library '%s' %s base library '%s'.

Description

This is a message indicating set/update of the base library attribute of a Sparse View library.

NDM-104

(info) Updating %s of Sparse View library '%s' from base library '%s'.

Description

This is a message indicating synchronization of a Sparse View library to pull-in updates from its base library.

NDM-105

(info) Adding %s '%s' to Sparse View library '%s'.

Description

This is a synchronization message indicating addition of remote content to the Sparse View library from the local on-disk content of the base library.

Feedback

NDM-106

(info) Removing %s '%s' from Sparse View library '%s'.

Description

This is a synchronization message indicating removal of remote content from the Sparse View library because its local on-disk content doesn't exist in the base library.

NDM-107

(error) Cannot open '%s'. It is an internal file within a directory format library.

Description

The specified path is an internal data file within a directory format library. It cannot be opened directly.

What Next

Find out the name of the library and use open_lib to open it:

prompt> *open_lib <lib_path>*

NDM-108

(error) The given drc error file does not exist.

Description

This error message occurs when the specified file does not exist in the directory. It may be either misspelled or an empty string.

What Next

Verify that you specified the correct path for the file and the name string.

NDM-109

(error) Cannot restore site name on '%s'. Site definition '%s' is missing from technology.

Description

The specified site definition is missing. Add the missing site definition to the technology and try again.

Feedback

NDM-110

(information) Recycled %d file descriptors.

Description

The specified number of file descriptors have been recycled as the user-specified open file limit has been reached.

NDM-111

(warning) Frame views in library '%s' is inconsistent with technology '%s'.

Description

The technology of this library has changed after frame creation. Frame views in this library are out-of-sync with the technology and should be re-created.

What Next

Re-generate the frame views using a consistent technology.

NDM-112

(Information) Opening block '%s' in read-only mode.

Description

The block is being opened in read-only mode because system resources have been exhausted.

NDM-113

(Information) Changing block '%s' to read-only mode.

Description

The block is being changed to read-only mode because system resources have been exhausted.

NDM-114

(error) Invalid port to be %s the port bus.

Feedback

Description

Ports which have the same base name as port bus and are part of vector can be added or removed from the port bus.

What Next

Verify that you specified the correct port for the bus port.

NDM-115

(error) Port %s will create a hole in the port bus.

Description

Ports addition/removal should be done from the sides of the port bus. Post update there should not be any hole in the port bus.

What Next

Verify that you specified the correct port for the bus port.

NDM-116

(error) Port can not be removed from the port bus having single port.

Description

There should be non empty port bus post port removal.

What Next

Verify that bus port should not become empty post removal.

NDM-117

(Information) The specified row/column should not less than cut row/column number '%u/%u' of base vias inherited from the via def '%s'.

Description

The cut row/column number isn't specified or the specified number is too small resulting that the number less than the cut row/columhn inherited from the via def. The row/column change doesn't succeed.

NDM-118

(error) cannot change %s for the custom via def.

Feedback

Description

This command cannot change row/column/XPitch/YPitch of the specified base via. Base via must be simple base via, and simple base via cannot be changed to custom base via.

What Next

Please provide the correct input for simple base via only.

NDM-119

(error) Invalid net to be %s the net bus.

Description

Nets which have the same base name as net bus and are part of vector can be added or removed from the net bus.

What Next

Verify that you specified the correct net for the bus net.

NDM-120

(error) Net %s will create a hole in the net bus.

Description

Nets addition/removal should be done from the sides of the net bus. Post update there should not be any hole in the net bus.

What Next

Verify that you specified the correct net for the bus net.

NDM-121

(error) Net can not be removed from the net bus having single net.

Description

There should be non empty net bus post net removal.

What Next

Verify that bus net should not become empty post removal.

Feedback

NDM-122

(information) Loading M-2016.12 library '%s'.

Description

This message is to inform the user that a forward version library, created from M-2016.12 binary is being loaded. The library and its design data will be saved in M-2016.12 format by default, or can be down converted with the save_lib -as <lib_name> -version L-2016.03 command

NDM-123

(error) Can't create supernet bundle '%s' as another bundle exists by same name.

Description

Data was saved using a version that created supernet bundles and then was taken back into an older version with same schema that doesn't know about supernet bundles wherein new bundle was created with the same name as that of the supernet bundle. The data was saved in this older version and then brought back into current version.

What Next

Please use a different name than the name of supernet bundle while creating bundle in the older version.

NDM-124

(error) %s '%s' as an object of supernet bundle '%s' doesn't exist.

Description

Supernet bundle contains supernets and/or bundles of supernets. Data was saved using a version that created supernet bundles and then was taken back into an older version with same schema that doesn't know about supernet bundles.

If the message refers to another bundle of supernets then a new bundle was created in the older version with the same name as that of a supernet bundle. If message refers to a supernet then the supernet was removed in the older version. The data was saved in this older version and then brought back into current version.

What Next

If the message refers to another bundle of supernets then please use a different name than the name of supernet bundle while creating bundle in the older version. If message refers to a supernet then it is fine as it was removed in the older version by intent.

Feedback

NDM-125

(error)Specified row and column(%u %u) exceed via matrix size %u and %u for %s.

Description

The Specified row and column should be non negative and less than via matrix size.

What Next

Specify the row and column between 0 and via matrix size.

NDM-126

(warning) Hierarchical edit-control of uneditable (read-only) block %s is violated for modification of %s object %s(%d)%s.

Description

This message is issued when a read-only block is being modified. The hierarchical edit-control of the block doesn't allow edit but the reported object of such uneditable (read-only) block is being modified.

What Next

Report this issue to Synopsys.

NDM-127

(warning) Saving uneditable (read-only) block %s because it has already been modified.

Description

This message is issued when a read-only block is being saved. The hierarchical edit-control of the reported block doesn't allow edit but the uneditable (read-only) block has already been modified and requires save.

What Next

Report this issue to Synopsys.

NDM-128

(information) Uneditable (read-only) block %s is not being saved.

Feedback

Description

This message is issued when a read-only block is not being saved. The hierarchical edit-control of the reported block doesn't allow edit and hence the block doesn't require save.

NDM-129

(information) The hierarchical edit-control of committed block %s is set editable in the top-level context of %s.

Description

This message is issued when a physical hierarchy is being committed as a new block. The hierarchical edit-control of the reported block is set to allow edits.

NDM-130

(information) The hierarchical edit-control of uncommitted block %s is cleared from the top-level context of %s.

Description

This message is issued when a physical hierarchy is being uncommitted and its block disappears. The hierarchical edit-control of the reported block is cleared from its top-level context.

NDM-131

(information) Master lock use for library "%s" changed to "%s" due to detection of %s.

Description

This message is issued when the lock mechanism is changed from the user-defined value. This change is due to the detection of another lock mechanism in use for the lib.

What Next

If the resulting change causes an error, close the library and notify other session that are using the lib to close the library and either let you open the library first, or change their design.master_lock to the same value you are using.

NDM-132

(warning) Resulting %s bound has %d elements, suggested limit is %s.

Feedback

Description

This message is issued when the given type of bound has more than the suggested number of elements. The suggested number usually indicates a good threshold for maintaining good performance during placement operations.

What Next

If resulting placement operations slow down significantly consider reducing the number of elements in this bound.

NDM-133

(error) Repelling bound requires argument -dimension.

Description

A repelling bound must have dimensions set upon creation.

What Next

Create the bound with -dimension argument specified.

NDM-134

(error) Resulting repelling bound contains only port objects.

Description

A repelling bound cannot consist of only port objects as ports are fixed. As such a repelling bound containing only ports cannot respect a given repulsion dimension.

What Next

Try including at least one cell in the bound.

NDM-135

(information) Overwriting design '%s' in library '%s' created by another process.

Description

This info message is to alert the user that a design created by another process is being overwritten.

Feedback

NDM-136

(warning) The Path '%s' is an all angle path. The the boundary coordinates of the path will be displayed similar to 45 degree path.

Description

This message is issued when the input path shape is an all angle path. The polygon path will be dispalyed similar to all angle paths with 45 degree points.

What Next

If the returned path points are not desirable, the centre point coordinates can be modified to make it a 45 degree path.

NDM-137

(information) Setting blockage type to '%s' requires blocked percentage to be set as well. Blocked percentage is set to 100.

Description

Setting blockage type to above requires blocked percentage to be set as well. Blocked percentage is set to 100.

What Next

Please set blockage percentage using "set_attribute -object 'foo' -name blocked_percentage -value 'bar'"

NDM-138

(information) Setting blockage type to '%s' requires category name to be set as well. Category name is set to "".

Description

Setting blockage type to above requires category name to be set as well. Category name is set to "".

What Next

Please set category name using "set_attribute -object 'foo' -name category -value 'bar'"

NDM-139

(error) Can't create shield overhang '%s' as another constraint group exists by same name.

Feedback

Description

Data was saved using a version that created shield overhangs and then was taken back into an older version with same schema that doesn't know about shield overhangs wherein new constraint group was created with the same name as that of the shield overhang. The data was saved in this older version and then brought back into current version.

What Next

Please use a different name than the name of shield overhang while creating constraint group in the older version.

NDM-140

(error) %s '%s' as an object of shield overhang '%s' doesn't exist.

Description

Shield overhang contains objects of types nets, bundles or topology edge. Data was saved using a version that created shield overhangs and then was taken back into an older version with same schema that doesn't know about shield overhangs.

The mentioned object in the message was removed in the older version. The data was saved in this older version and then brought back into current version.

What Next

The mentioned object was removed in the older version by intent. It is no longer possible to have that object in the shield overhang constraint group.

NDM-141

(error) Unable to open_block '%s' due to license check failure. The license key '%s' is required.

Description

Ths block is license protected. Opening it requires certain licenses to be available. The tool was not able to check out the required licenses, so the block cannot be opened.

What Next

Please make sure the required licenses are available and can be checked out.

NDM-142

(error) Cannot add shape '%s' to via ladder because it is connected to a different net than other shapes in this via ladder.

Feedback

Description

The specified shape cannot be added to the via ladder because it is connetced to a different net than other shapes in this via ladder. All the shapes in a via ladder should be connected to the same net.

What Next

Pass a collection of shapes to the createViaLadder api command which belong to the same net and try again.

NDM-143

(error) Shape '%s' is a part of an existing via ladder object.

Description

A shape can only be a part of exactly one via ladder object.

What Next

Please remove this shape from the list of shapes for the current via ladder.

NDM-144

(error) Cannot delete rule '%s' since it is being referenced by group '%s' .

Description

There is some problem in remove. This could happen when object is getting referenced by some other object.

What Next

First remove the rule from group then remove rule.

NDM-145

(warning) The pin %s is not of any of the types specified in the rule.

Description

There is some problem in pin(s). This could happen when type of pin(s) does not match with the type(s) specified in the rule.

What Next

Specify the pin matching with the type specified in rule.

Feedback

NDM-146

(information) Layer %s (%d) in the source technology file %s does not match the layer of the same name in the destination library.

Description

You get this message when you apply a new technology file which has layer number and layer name different from current technology.

What Next

Make sure that the differences are expected or replace with correct technology file. If differences are expected then update various layer mapping files also e.g. related with read_parasitic_tech etc. as per layers in new technology file.

NDM-147

(information) Layer %s (%d) is in the destination library but not in the source technology file %s.

Description

You get this message when you apply a new technology file which is missing layer(s) which are present in the current technology.

What Next

Make sure that the differences are expected or replace with correct technology file. If differences are expected then update various layer mapping files also e.g. related with read_parasitic_tech etc. as per layers in new technology file.

NDM-148

(error) Resulting %s bound has %d cores, while the limit is %d.

Description

This message is issued when the given type of bound has more than the allowed number of cores. Cores are modelled as either hierarchical cells or repelling bound groups.

What Next

Reduce the number of cores in this bound.

NDM-149

(error) Failed to open the cell-rename map file '%s'.

Feedback

Description

The cell-rename map file could not be opened. Verify the file-permissions and retry.

NDM-150

(error) Required section '%s' was not found before section '%s'.

Description

The name mapping for mask-shifted cells comprises three sections: MASKSHIFTLAYER, MASKSHIFTPATTERN and CELLMAP. You need to define the sections in the order above.

What Next

Supply the required section.

NDM-151

(error) Invalid mask shift layer '%s'%s.

Description

This error message occurs when the specified mask shift layer is invalid, it must meet the following conditions. 1. Multiple cell mapping files should have the same mask shift layer, whether the number or the order of layer must be the same. 2. The layers must exist in the current library.

What Next

Please check and correct the mask shift layer, then try again.

NDM-152

(warning) Incorrect syntax '%s' specified for cell-rename entry. The entry will be ignored.

Description

The syntax for the cell-rename entry is not a valid one. Refer the man-page of write_verilog/write_gds for the appropriate syntax.

NDM-153

(error) Invalid mask shift pattern '%s'%s.

Feedback

Description

This error message occurs when the specified mask shift pattern is invalid, it must meet the following conditions. 1. Multiple cell mapping files should have the same mask shift pattern. 2. The number of the mask shift combination is equal to or less than pow(m, n), where n is the number of layers specified in MASKSHIFTLAYER and m is the count of the shift values. For 2-mask layers, valid shift values are 0 and 1, so m is 2. For 3-mask layers, valid shift values are 0, 1, 3, 4 and 5, so m is 5. When the shift value is 3, 4 or 5, the shifted layer must have fixed mask 1, 2 or 3, repectively and its number_of_masks must be more than 2. 3. MASKSHIFTPATTERN must contain the mask shift combination for the cell without any mask shifting.

What Next

Please check and correct the mask shift pattern, then try again.

NDM-154

(error) Invalid cell mapping value '%s'.

Description

The number of the cell mapping value is not consistent with the number of the specified mask shift pattern.

What Next

Please check and correct the cell mapping value, then try again.

NDM-155

(error) Mask shifted cell '%s' does not have its corresponding mapping in the map file.

Description

There is not a corresponding mapping for the mask shifted cell in the map file.

What Next

Please add the corresponding mapping to the map file and then try again.

NDM-156

(error) Mask shift property mismatch on cell '%s'.

Description

There is mask shift property mismatch between different map files.

Feedback

What Next

Please correct the mask shift property and then try again.

NDM-157

(error) Fail to find the pattern '%s' for cell '%s'.

Description

The pattern is not specified in MASKSHIFTPATTERN section.

What Next

Please check and correct it, and then try again.

NDM-158

(warning) The design '%s' with the view '%s' is not found in Library '%s'. But different views of the design exists in the library.

Description

The design with the specified name and view is not found in the searched library. But other views of the design exists in the Library.

What Next

Please specify the correct Library for the search.

NDM-159

(Info) Don't support alternating mask pattern.

Description

Don't support 'alternating' mask pattern. The valid mask pattern is one of uniform, arbitrary, alternate_rows, alternate_columns.

What Next

Please specify the valid mask pattern.

NDM-160

(warning) Cannot edit %s because it is part of via_ladder.

Feedback

Description

The specified object cannot be edited or deleted because it is member of a via ladder and via ladder protection is enabled.

What Next

Disable via ladder protection using app option design.via_ladder_protection or remove the object from its via ladder.

NDM-161

(error) Attempt to write '%s' failed due to '%s'.

Description

Unable to write a file.

NDM-162

(error) Cannot delete fsm '%s' since it is being referenced by rule or group '%s' .

Description

There is some problem in remove. This could happen when object is getting referenced by some other object.

What Next

First remove the rule or group then remove fsm.

NDM-163

(error) Invalid '%s' option usgae : It can only be used with '%s' type objects in the list.

Description

Command option '-original_parent' can only be used with cell type of objects in the list and not with port or module/block objects.

What Next

Please provide cell type of objects with '-original_parent' option otherwise don't use this option for other type of objects in the list.

NDM-164

(error) Reading from '%s' failed due to '%s'.

Feedback

Description

Error at reading a file

NDM-165

(information) Waiting to acquire write access for %s. Library '%s' is being edited by process %d %s@%s.

Description

Unable to acquire write access to the library because write access is held by another process. The specified operation will be retried until the maximum wait time is reached.

The maximum wait time is controlled by the app_option "lib.setting.max_wait_time". The default value is 3600 seconds.

NDM-166

(warning) Rail index %d is invalid on port %s.

Description

The rail index on the specified port is invalid, since it is corrupted data, the rail attribute on the port will be dropped when loading the reference library. To be specific, the input_signal_level and output_signal_level attributes on signal port will be lost, and rail attribute on power or ground port will be lost . There is a known issue in Library Preparation on 2019.12-SP2 release which leads to this error. The problem was fixed in 2020.09-SP6 release. The missing rail attributes on port could impact the result of downstream tools, so it is highly recommended to regenerate the reference libraries using 2020.09-SP6 or later releases.

What Next

Regenerate the reference libraries using 2020.09-SP6 or later releases.

NDM-167

(Error) The current shell cannot open designs of type '%s'.

Description

Some design types may only be opened in specific applications. For example designs specific to 3dic systems (3dic, package, substrate, bridge and interposer) may only be opened by the 3dic shell and not by Fusion Compiler and IC Compiler II.

Feedback

What Next

Open the design in the application used to create the design.

NDM-168

(Warning) This type of repelling group bounds for functional safety is deprecated and replaced by safety_core_groups.

Description

The use of repelling bounds for specifying dual-core lockstep for functional safety is deprecated and has been replaced by safety_core_groups.

What Next

Use create_safety_core_rule and create_safety_core_group commands to define dual-core lockstep (DCLS) functionality.

NDM-169

(warning) Cannot change net_type from %s to %s on net '%s'.

Description

The segment net is "*Logic0*" or "*Logic1*". These are reserved by Synopsys for the tie-low and tie-high constant nets. Their types cannot be changed.

What Next

No action is required.

NDM-170

(information) Restored app option '%s' with value '%s'.

Description

This info message is to alert the user that app option is restored.

NDM-171

(error) Could not find a system startup file '%s' in '%s' .

Description

There is some problem in sourcing system startup files. This could happen when the system startup file is not available or permission is not proper.

Feedback

What Next

Please check if the system startup file is available or if the file permissions are proper.

NDM-172

(warning) Block '%s' can only be opened as read-only because it is related to an editable view.

Description

When an outline is the source of an editable design, it becomes read-only.

What Next

In order to make your outline editable again, you must remove the existing editable design by using the remove_block command.

NED

NED-001

(error) Cannot size '%s' - it is not a leaf cell.

Description

The *size_cell* command will only work with leaf cells. The specified cell is hierarchical.

What Next

You can swap a hierarchical cell using the *swap_cell* command.

NED-002

(warning) Could not find alternative library cells for %s.

Description

Alternative library cells could not be found for the cell or library cell specified. Perhaps there were no equivalent library cells in the libraries searched. The criteria used to determine that a library cell is an alternative for another library cell is the same which is used by the size_cell command.

What Next

Perhaps specify other libraries using the -libraries option.

Feedback

See Also

- size_cell

NED-003

(warning) Both the -estimate and -exact option cannot be specified.

Description

Both the -estimate and -exact options cannot be specified at the same time for the report_alternative_lib_cells command.

What Next

Specify either -estimate or -exact.

NED-004

(warning) The -weighted_design_cost or -total_design_cost options cannot be be used when -estimate is specified.

Description

The -weighted_design_cost and -total_design_cost options are only applicable when -exact is specified.

What Next

Either use -exact, or do not use the -weighted_design_cost or -total_design_cost options.

NED-005

(Error) Could not size '%s' ('%s') with '%s'%s.

Description

You tried to size a cell, and this action failed. Additional information might be included with this message and previous messages. A typical reason is that the target library cell is not compatible with the existing cell because it has a different pin count, or different pin directions, and so on.

What Next

Action based on reasons given in message text. Use the *get_alternative_lib_cells* command to determine what library cells can be used to size your cell.

Feedback

NED-006

(Error) Can only have a single target object.

Description

The specification for the target library cell to commands like *size_cell*, *insert_buffer*, and *create_cell* resulted in more than one object. Either you specified a list or used a collection that matched multiple objects.

What Next

Narrow the search parameters so only a single library cell is selected.

NED-007

(error) Cannot specify the '%s' option and explicitly specify the library in which the library cell exists.

Description

This message is produced if either the '-current_library' option or the '-libraries' option is specified while explicitly specifying the library in which the library cell exists.

What Next

Either explicitly specify the library in which the library cell exists using the syntax 'lib_name/lib_cell_name'; or specify the library cell name only with the option needed to resolve the library name.

See Also

- insert_buffer
- create_cell
- size_cell

NED-008

(information) Renamed cell '%s' to '%s' in %s.

Description

The *rename_cell* command was issued to rename a cell.

What Next

For more information, see the user guide.

Feedback

NED-009

(information) Renamed net '%s' to '%s' in %s.

Description

The *rename_net* command was issued to rename a net.

What Next

For more information, see the user guide.

NED-010

(error) Could not insert '%s' - %s.

Description

You tried to insert a buffer, and the action failed for the reason given. A typical reason is that the library cell chosen is not classified as a buffer. A buffer must have one input, and each output must be functionally input or !input.

What Next

Action based on the reason.

NED-011

(error) Cannot insert buffer '%s' with%s %s

Description

You tried to insert a buffer, and the command options are inconsistent. Either you specified the -inverter_pair option and the library cell does not have an inverting output, or you did not specify the -inverter_pair option, and the library cell has only inverting outputs.

What Next

Check the library cell to see what output pins are available.

NED-012

(error) Could not insert a buffer on %s '%s': %s

Description

You tried to insert a buffer, and the action failed for the given reason. An example reason would be trying to insert a buffer on a port when current instance is not at the top of the

Feedback

hierarchy. Another example would be trying to insert a buffer on a pin which is out of scope (that is, the pin is not in or below the current instance).

What Next

Check the arguments to the command.

NED-013

(warning) Duplicate argument (%s '%s') to %s ignored

Description

You tried to use a netlist editing command, and you specified the same argument more than once. This is just a warning.

What Next

Verify that the argument was specified correctly.

NED-014

(information) Created cell '%s' in %s with '%s'.

Description

The *create_cell* command was issued to create a new cell using the specified library cell.

What Next

For more information, see the user guide.

NED-015

(information) Removed cell '%s'.

Description

The *remove_cell* command was issued to remove the specified cell.

What Next

For more information, see the user guide.

NED-016

(information) Created net '%s' in %s.

Feedback

Description

The *create_net* command was issued to create a new net.

What Next

For more information please refer to PrimeTime User Guide.

NED-017

(information) Removed net '%s'.

Description

The *remove_net* command was issued to remove a net.

What Next

For more information please refer to PrimeTime User Guide.

NED-018

(information) Connected '%s' to '%s'.

Description

The *connect_net* command was issued to connect a net to a pin.

What Next

For more information please refer to PrimeTime User Guide.

NED-019

(information) Disconnected '%s' from '%s'.

Description

The *disconnect_net* command was issued to disconnect a net from a pin.

What Next

For more information please refer to PrimeTime User Guide.

NED-020

(error) Could not rename design '%s' to '%s': %s

Feedback

Description

An attempt to rename a design failed. The reason is given in the message text. Given that you tried to rename *a* to *b*, one reason the rename would fail would be that there is already a design named *b* associated with the file of *a*. Another reason would be that there are instances of *a* in a linked design.

What Next

Choose a name which does not conflict with existing design names. Also, renaming designs in PrimeTime should be done prior to any linking to avoid the case of instantiation conflicts.

NED-021

(error) Could not rename %s to '%s': %s%s.

Description

You tried to rename a cell or net, and it could not be renamed for the reason given. A typical reason is that a cell or net by that name already exists at that point in the hierarchy.

What Next

Action based on the reason.

NED-022

(error) Cannot insert more than one buffer at a time when -new_cell_names and -new_net_names are specified.

Description

You have recevied this message because you have attempted to insert multiple buffers at different pins in the design and have also specified the -new_cell_names and -new_net_names options. The -new_cell_names and -new_net_names options can only be specified when you insert one buffer one inverter pair at a pin in the design.

What Next

Remove the -new_cell_names and -new_net_names options from the insert_buffer command.

NED-040

(error) No changes made.

Feedback

Description

This is a summary message for netlist editing. It indicates that no changes were made by the command. For example, no cells were created, or no pins were disconnected from a net.

The netlist editing commands succeed if at least one change is made. This message is only issued if no changes were made.

What Next

None.

NED-041

(error) Could not create %s '%s': %s%s.

Description

You tried to create a cell or net, and it could not be created for the reason given. A typical reason is that a cell or net by that name already exists at that point in the hierarchy.

What Next

Action based on the reason.

NED-042

(error) Could not connect '%s' to '%s' %s

Description

This message is issued by the *connect_net* command if the net could not be connected to the given object. The reason is given in the message. Reasons include: the object is already be connected to a net; the connection would cross a hierarchical boundary; attempted to connect a port to a net which is not in the top level of the hierarchy.

What Next

Action based on the reason.

NED-043

(error) Object '%s' is not connected to net '%s'

Description

This message is issued by the *disconnect_net* command if the target object is not connected to the net.

Feedback

What Next

Verify that the target object was specified correctly.

NED-044

(error) Argument to %s (%s'%s') is invalid: %s

Description

This message is issued by the netlist editing commands if the object is not valid for the command. The reason is given in the message. Many netlist editing commands use this message when the object is not in scope - the object must be in or below the current instance.

The *remove_buffer* command uses this extensively to indicate many problems. For example,

- The cell is not a buffer.
- The cell has too many or too few pins connected.
- The cell needs to be an inverter, but isn't.
- The cell is an inverter, paired with another argument. But, they are not connected, or the intermediate net has too many connections.
- The output net has too many drivers.

What Next

Action based on the reason.

See Also

- remove_buffer

NED-045

(information) Sized '%s' with '%s'.

Description

The *size_cell* command was issue to size the specified cell with a target library cell.

What Next

For more information please refer to PrimeTime User Guide.

Feedback

NED-046

(information) Inserted %s at %s with %s.

Description

The *insert_buffer* command was issued to buffer specific pins with a target library cell. In the case of an inverter pair two cells will have been inserted.

What Next

For more information please refer to PrimeTime User Guide.

NED-047

(information) Removed buffer %s.

Description

The *remove_buffer* command was issued to remove a specific buffer or inverter pair.

What Next

For more information please refer to PrimeTime User Guide.

NED-048

(error) The variable %s cannot be set to '%s'

Description

You received this message because you have tried to set the variable to a value that violates the rules set down for its value.

What Next

See the man page for the variable and set its value appropriately.

NED-049

(warning) disconnecting port-connected net from output pin/port '%s'.

Description

You received this message because you have performed a buffer insertion (using the insert_buffer command) at a hierarchical pin or port. This command disconnected a port-connected net from a hierarchical pin or port of the same name.

Feedback

PrimeTime warns about this operation because third-party verilog readers will infer that the net and pin/port are still connected as they share the same name. This would result in a shorting out of the buffer that has just been inserted in the third-party tool.

What Next

To avoid the warning, rename the port-connected net (using the rename_net command) to some name that is not the pin/port name before inserting the buffer.

NED-050

(error) Cannot disconnect a port-connected net from pin/port '%s', because the net has the same name as the pin/port.

Description

You received this message because you have performed a disconnect_net command at a hierarchical pin or port. The command attempted to disconnect a port-connected net from a hierarchical pin or port of the same name.

This operation is not allowed because third-party verilog readers will infer that the net and pin/port are still connected as they share the same name. This would result in a shorting out of any object that is subsequently reconnected to the net in the third-party tool.

What Next

To continue with the disconnection of the port-connected net, you must first rename the port-connected net (using the rename_net command) to some name that is not the pin/port name.

NED-051

(error) This netlist editing command ('%s') is not supported in IC Compiler.

Description

You received this message because you are writing netlist eco changes for IC Compiler, but the command is not supported in IC Compiler. The requested changes is commented out, to show you what PrimeTime did. Because the command will not be executed in IC Compiler, you may get different results from your run in PrimeTime.

What Next

Please do not use this netlist editing command in PrimeTime, if you intend to write the changes for IC Compiler.

Feedback

NED-052

(error) This netlist editing command ('%s') is not fully supported in IC Compiler.

Description

You received this message because you are writing netlist eco changes for IC Compiler, but the command is not fully supported in IC Compiler: the "-exact" option cannot be used. The write_changes output file contains the command, but not the "-exact" option. Because the command will not be executed in IC Compiler exactly as in PrimeTime, you may get different results from your run in PrimeTime.

What Next

Please do not use this netlist editing command with the "-exact" in PrimeTime, if you intend to write the changes for IC Compiler.

NED-053

(error) This netlist editing command ('%s') is not fully supported in IC Compiler.

Description

You received this message because you are writing netlist eco changes for IC Compiler, but the command is not supported in IC Compiler: the net name cannot contain wildcard character, or the hiearch separator. Because the command will not be executed in IC Compiler, you may get different results from your run in PrimeTime.

What Next

Please do not use this netlist editing command with the restricter characters in the net name, if you intend to write the changes for IC Compiler.

NED-054

(information) write_changes: change_list redundancy removal results: ('%s')

Description

This information message gives the details of how many change commands were redundant.

What Next

For more information please refer to PrimeTime User Guide.

Feedback

NED-055

(warning) Buffer cell %s is dont_touched.

Description

A *dont_touch* has been detected on the indicated buffer cell. Although this buffer type can still be sized and inserted into the design, it becomes *dont_touched* for further optimization once it has been inserted into the design. This might place restrictions on the optimization process.

What Next

It might be desirable to use the *set_dont_touch* command to set a *dont_touch* value of *false* on the affected buffer library cells.

NED-056

(error) %s estimation at '%s' failed.

Description

An *estimate_eco* operation has failed on the specified design object, meaning that optimization might be limited or impossible at this object.

What Next

Try performing a manual *estimate_eco* operation at the specified design object to determine if there is a problem. If needed, contact your Synopsys support representative for assistance.

See Also

- estimate_eco

NED-057

(warning) Library cell %s has dont_use attribute.

Description

This warning message occurs when the specified library cell for *insert_buffer* or *size_cell* command has a *dont_use* attribute.

Feedback

What Next

This is just a warning message. If result is not what you expected, you can either use other equivalent library cell that does not have *dont_use* attribute or remove the *dont_use* attribute of the library cell by using *set_dont_use* command.

See Also

- insert_buffer
- size_cell
- set_dont_use

NED-058

(warning) The icc2tcl format will be obsoleted in future release, icctcl can be used in IC Compiler II starting from J-2014.12-SP1-1 release.

Description

This warning message occurs when the *icc2tcl* format is given.

What Next

This is just a warning message. Consider using *icctcl* format if possible.

See Also

- write_changes

NED-059

(error) Current PrimeTime session is in Galaxy Incremental ECO mode. All PrimeTime ECO commands are disabled in order to keep the netlist consistent with the design in IC Compiler II. Save the session using save_session command before executing any PrimeTime ECO commands.

Description

This error message occurs if any PT ECO command is executed on the PT session that has ICC2 changes consumed through read_eco_changes command.

What Next

None.

Feedback

NED-060

(error) Netlist editing changes through read_eco_changes command should be applied either on top hier or full MIM instances.

Description

This is a summary message for netlist editing. It indicates that user should apply netlist diting changes through read_eco_changes command either on top hier or full MIM instances.

What Next

None.

NED-061

(error) Current PrimeTime session is in Galaxy ECO flow. read_eco_changes command can not be executed after executing any PT ECO command.

Description

This error message occurs if read_eco_changes command is executed in PT session after executing any PT ECO command.

What Next

None.

NED-062

(error) Cannot find %s in the comments while reading incremental netlist changes from ICC2.

Description

This error message occurs if read_eco_changes command can not find block name or (current or previous) signature in commnents while reading incremental netlist changes from ICC2.

What Next

None.

NED-063

(error) Cannot source file %s.

Feedback

Description

This error message occurs if read_eco_changes command cannot source the specified input file. The error has occured due to one of the netlist editing commands specified in input file.

What Next

None.

NED-064

(error) %s signature (specified by ICC2 in %s file) for block %s does not match with the signature stored with current PT session.

Description

This error message occurs if in a Galaxy ECO iteration, the current/previous signature (specified by ICC2) for a block does not match with the signature stored with current PT.

What Next

None.

NED-065

(error) Could not rename %s to '%s': %s%s.

Description

You tried to rename a hierarchical pin(port), and it could not be renamed for the reason given. A typical reason is that a port by that name already exists at that point in the hierarchy.

What Next

Action based on the reason.

NED-066

(error) Could not create %s '%s': %s%s.

Description

You tried to create a hierarchical pin(port), and it could not be created for the reason given. A typical reason is that a port by that name already exists at that point in the hierarchy.

Feedback

What Next

Action based on the reason.

NED-067

(error) This netlist editing command ('%s') is not supported for output format '%s'.

Description

You received this message because create_port command is supported only for output format icctcl.

What Next

Please do not use this netlist editing command with any output format other than icctcl.

NED-068

(information) Replaying ECO changes for design %s.

Description

This information message shows the design name of the replaying changes.

What Next

For more information please refer to PrimeTime User Guide.

NED-069

(information) Created hierarchal pin/port '%s' in %s.

Description

The *create_port* command was issued to create a new hierarchical pin/port on the given hierarchy with given name.

What Next

For more information, see the user guide.

NED-070

(Error) The -all_mim_instances option of the %s command cannot be used when the eco_enable_mim variable is set to false.

Feedback

Description

The *-all_mim_instances* option of the editing command cannot be used because the all-instance MIM editing feature has not been enabled.

What Next

Set the *eco_enable_mim* variable to *true* before you use the *-all_mim_instances* option of the editing command.

NED-071

(Info) The -all_mim_instances option of the %s command is ignored because the module is not multiply instantiated.

Description

The *-all_mim_instances* option of the editing command is ignored becuase the change is being performed on a module that is not a multiply instantiated module (MIM).

What Next

No further action is required. If you intended to apply the change to all modules of a MIM group, check the MIM groups in the design by running the *report_eco_mim_instances* command.

NED-072

(Information) The %s command is applied to all instances of each MIM group because the eco_mim_preserve variable is set to true.

Description

The *fix_eco_timing*, *fix_eco_drc*, or *fix_eco_power* command is applied to all instances of each multiply instantiated module (MIM) group because the *eco_mim_preserve* variable is set to *true*.

What Next

If you want to apply the editing command to only a subset of a MIM group, set the *eco_mim_preserve* variable to *false*. In that case, editing the subset breaks the MIM grouping.

NED-073

(warning) Removing buffer '%s' which is marked as %s.

Feedback

Description

The *remove_buffer* command removed a buffer that had a restriction attribute set, such as the *size_only* attribute set by the *set_size_only* command. Warning example,

- Removing buffer 'buf' which is marked as size_only.

What Next

No further action is required if you intended to remove the buffer. Otherwise, you can restore the desired buffer using the *insert_buffer* command.

See Also

- remove_buffer
- set_size_only

NED-074

(error) insert_buffer command is ignored because the specified buffer location is outside the physical boundary of the design.

Description

The coordinates provided in the insert_buffer command are not within the boundary of the design in which the buffer is being inserted.

NED-075

(warning) HyperScale annotation at pin %s is removed because newly inserted buffer removes direct connection from port to load pin. Note that the HyperScale annotations will not be restored if the buffer is removed.

NED-076

(warning) Library cell '%s' is part of a -dont_use subset specification that applies to cell '%s'.

Description

This warning message occurs when the specified library cell for *insert_buffer* or *size_cell* command is part of *dont_use* list in the parent hierarchy.

What Next

This is just a warning message. If result is not what you expected, you can either use other equivalent library cell that is not part of *dont_use* list in the parent hierarchy

Feedback

or remove the library_cell from the *dont_use* list of the parent hierarchy by using *remove_target_library_subset_command* command.

See Also

- insert_buffer
- size_cell
- remove_target_library_subset

NED-077

(error) insert_buffer command is ignored because part of the newly inserted buffer will lie outside the physical boundary of the design.

Description

The buffer to be created based on the coordinates and the lib cell provided in the *insert_buffer* command will not lie in the boundary of the design completely.

NED-078

(Error) HyperScale annotation at pin %s is not removed because no valid driver driving this pin.

NED-079

(warning) HyperScale annotation at pin %s is not removed because it is not connected to driving port.

NED-080

(Warning) Inserted buffer %s is not associated with a programmable spare cell.

Description

You are attempting to write an ECO changelist in the freeze_silicon physical mode involving an inserted buffer which has not been assigned to a programmable spare cell. This situation may arise when there is no programmable spare cell at the specified location, or when one exists but is already associated with other buffers.

What Next

Check the quality of the ECO changes you are attempting to write.

Feedback

NED-081

(warning) Timing exceptions are defined on the pin '%s'.

Description

This warning message occurs when user tries to remove a buffer that has timing expections defined on its pins. Timing exceptions may have been defined on the pin using *set_false_path*, *set_sense* or *set_data_check* command.

What Next

This is just a warning message. If result is not what you expected, you can either suppress this message or remove the timing exceptions applied on the pin.

See Also

- suppress_message
- set_false_path
- set_sense
- set_data_check
- remove_buffer

NED-082

(warning) Sizing '%s' relaxing library arc check%s.

Description

The cell has been sized with the library cell provided in the command. However, this message is to warn you that the target library cell is not completely compatible with the old library cell because it has difference in lib arcs as indicated with the message.

What Next

If this is not intended to happen, Use the *get_alternative_lib_cells* command to determine what library cells can be used to size your cell. Also, check the behavior of the public variable *eco_strict_lib_arc_equivalence*.

NED-083

(warning) Overriding dont_touch attribute in manual ECO command.

Feedback

Description

dont_touch attribute was set on a netlist object like cell, net, or pin. However, manual ECO operation will override the *dont_touch* attribute and the intended command will be executed.

What Next

ECO commands like *fix_eco_timing* and *fix_eco_power* honor the *dont_touch* attribute, however, manual ECO commands like *insert_buffer* and *size_cell* etc. don't honor the *dont_touch* attribute by default.

NED-084

(Error) Honoring dont_touch attribute in manual ECO command.

Description

dont_touch attribute was set on a netlist object like cell, net, or pin. However, manual ECO operation is set to honor the *dont_touch* attribute by a setting and the intended command will not be executed.

What Next

ECO commands like *fix_eco_timing* and *fix_eco_power* honor the *dont_touch* attribute, however, manual ECO commands like *insert_buffer* and *size_cell* etc. don't honor the *dont_touch* attribute by default. But, the manual ECO behavior has been altered here.

NED-085

(Warning) Using the manager library cell instead of physical variant for current ECO operation.

Description

The message warns that the current ECO operation like size_cell, swap_cell or insert_buffer is using the manager library cell instead of physical variant.

NED-086

(Warning) The VMF file does not contain timing information.

Description

The VMF file passed to the *read_vmf_file* command does not contain timing information needed to describe the VMF attacker nets.

Feedback

What Next

Review the VMF file.

NED-087

(Error) Cannot find library cell '%s' containing pin '%s'.

Description

The specified library cell and/or pins in the VMF file are not found. The corresponding VMF Attacker net will not be created.

What Next

Review the VMF file and/or search paths for library cells.

NED-088

(Error) Failed to parse VMF file: %s.

Description

The VMF file contains syntax errors. Please refer to the message above for more details.

What Next

Fix the syntax error.

NOISE

NOISE-001

(information) Activating steady state resistance estimation mode for library %s.

Description

You received this informational message because during the noise analysis the steady state resistance estimation was activated for one of the library cells in this library.

This estimation mode is activated during the noise analysis update, when no steady state resistance or I-V curve could be determined from the library or specified by the command *set_steady_state_resistance*. Steady state resistance estimation makes use of the existing delay and slew tables in the library.

Feedback

What Next

Use the *check_noise* command to report on the completeness of noise library data in the analysis. If some libraries are missing noise information, noise characterization should be performed for those libraries. If most library cells have noise data and a few special cells or macrocells are missing noise data, you can use the *set_noise_lib_pin* command to apply the noise characteristics of one noise-characterized library pin to another library pin. The output of the *check_noise* command includes any library pin where noise information has been aliased with the *set_noise_lib_pin* command.

See Also

- check_noise
- set_noise_lib_pin

NOISE-002

(warning) Steady state resistance estimation failed for %s %s.

Description

You received this informational message because during the noise analysis the steady state resistance estimation was activated and failed for the library pin or port shown above. A fixed steady state resistance value is being used.

This estimation mode is activated during the noise analysis update, when no steady state resistance or I-V curve could be determined from the library or specified by the command *set_steady_state_resistance*. Steady state resistance estimation makes use of the existing delay and slew tables in the library.

What Next

This message indicates that for the library pin or port mentioned above, there was no steady state I-V curve or steady state resistance, and our steady state resistance estimation mode has failed and a fixed value has been used. Therefore, it is recommended that this information be characterized for this library pin or port, and the library DB be regenerated. If this is not possible, the characterized steady state resistance can be directly set using the *set_steady_state_resistance* command.

NOISE-003

(warning) Noise height constraint value of %.2f for pin %s is out of valid range.

Feedback

Description

You received this informational message because during noise analysis the height constraint value for the library pin or port shown above is negative. This condition can occur when a noise bump width is outside the characterization range of the noise immunity table. In this situation, the immunity curve specified by the table is extrapolated to obtain the noise height constraint. If the curve is monotonically decreasing in the extrapolated area, a negative value may result. PrimeTime will replace this negative height constraint with zero so that any such condition will be flagged as a noise violation. The area slack in these cases will be the negative of the bump height area.

What Next

This warning indicates a characterization problem for the noise immunity tables in the library. Noise immunity height is expected to remain constraint when extrapolation is required. Please contact your library vendor.

You may also override the library-specified noise immunity table by using the *set_noise_immunity_curve* command.

See Also

- set_noise_immunity_curve

NOISE-004

(information) Starting incremental noise update.

Description

Update of noise data is done incrementally (faster than full default update). The incremental updates are faster because only the affected parts of the design are updated. That includes the nets directly affected by design changes (such as size_cell), their aggressors, and nets where timing windows changed.

Due to iterative nature of signal integrity updates the incremental update may not perfectly match the full update. The difference should be marginal in most cases but if significant then please perform full update.

What Next

This is an informational message. No action is required on your part. However, you can trade off accuracy for performance by forcing full update by e.g., *update_noise -full*

Feedback

See Also

- update_timing
- update_noise
- XTALK-016

NOISE-005

(error) The command is available only in report_at_endpoint noise analysis mode.

Description

You received this error message because this command works only in report_at_endpoint noise analysis mode.

What Next

Please use *set_noise_parameters* command to set noise analysis mode to report_at_endpoint. You also may need to run *noise_update* to see correct results.

See Also

- set_noise_parameters
- report_noise
- report_noise_violation_sources

NOISE-006

(information) Setting report_at_endpoint analysis mode enables noise propagation.

Description

You received this informational message because you have specified report_at_endpoint noise analysis mode.

The report_at_endpoint mode requires noise propagation because violations are reported at endpoints after injected noise bumps propagate from violation sources to endpoints.

What Next

If noise propagation is not desired, switch to report_at_source mode by using *set_noise_parameters* command.

Feedback

See Also

- set_noise_parameters

NOISE-007

(warning) Cannot calculate noise immunity for library pin %s due to invalid CCS-noise information.

Description

You received this warning message because the indicated pin does not have valid CCS-noise information to calculate noise immunity.

You may have to set noise immunity on the pin manually by yourself. Otherwise, you may miss a violation if no slack value is available from the pin.

What Next

Check if the characterization on this pin has been done properly.

See Also

- report_noise_calculation
- report_noise

NOISE-008

(warning) %s is not an endpoint. Only an endpoint can be reported in report_at_endpoint mode.

Description

You received this error message because the indicated pin is not an endpoint, but you tried to run *report_noise command* on the pin.

The report_noise command reports only endpoints in the report_at_endpoint mode.

What Next

Use *report_noise_calculation* command to report noise infomration on the pins that are not endpoints.

Feedback

See Also

- set_noise_parameters
- report_noise_calculation
- report_noise

NOISE-009

(warning) %d percent of the rail voltage is assumed for the noise height constraint value of library pin %s because no noise immunity information is available for the pin.

Description

You received this warning message because during noise analysis any height constraint value for the library pin or port shown above is not available.

PrimeTime SI will assume 40% of the rail voltage as noise immunity value, which might be more pessimistic than the real value.

What Next

This warning indicates a characterization problem for the pin. Please check your library, or contact your library vendor.

If you know the noise immunity value for the pin, you may use *set_noise_margin* command to specify the right value.

You may also override the value by using the *set_noise_immunity_curve* command.

See Also

- set_noise_margin
- set_noise_immunity_curve

NOISE-010

(Information) Updating %-35s

Description

Shows the progress of update noise. The update of noise can happen explicitly by calling *update_noise* or implicitly by calling one of the commands that need update noise such as *report_noise*.

Feedback

NOISE-011

(warning) %d percent of the rail voltage is assumed for the noise height constraint value of pin %s because no noise immunity information is available for the pin.

Description

You received this warning message because during noise analysis any height constraint value for the library pin or port shown above is not available.

PrimeTime SI will assume 40% of the rail voltage as noise immunity value, which might be more pessimistic than the real value.

What Next

This warning indicates a characterization problem for the pin. Please check your library, or contact your library vendor.

If you know the noise immunity value for the pin, you may use *set_noise_margin* command to specify the right value.

You may also override the value by using the *set_noise_immunity_curve* command.

See Also

- set_noise_margin
- set_noise_immunity_curve

NOISE-012

(Error) Signal integrity analysis is disabled.

Description

You received this error message because the *si_enable_analysis* variable has been set to *false* while the command requires signal intgegrity analysis.

What Next

First, determine whether you want to perform signal integrity analysis. If you do, then set *si_enable_analysis* to *true*.

See Also

- update_noise
- si_enable_analysis

Feedback

NOISE-013

(Information) In HiCap mode, please use report_noise_calculation for individual noise bumps.

Description

You received this error message because the *report_noise -verbose* won't report individual noise bumps under HiCap mode. Please use *report_noise_calculation* for individual noise bumps.

What Next

First, determine whether you need individual noise bumps. If you do, then use *report_noise_calculation*.

See Also

- report_noise
- report_noise_calculation

NOISE-014

(information) Starting crosstalk aware static noise analysis.

Description

Static crosstalk aware noise analysis is being performed.

What Next

This is an informational message. No action is required on your part. For more information please refer to the PrimeTime User Guide.

NOISE-015

(information) Net %s was not analyzed for detailed noise analysis.

Description

You received this message because this net does not have any detailed information for noise reporting purpose. In the violators focussed type of noise analysis, only nets which are deemed potentially violating are considered for detailed noise analysis. Nets that cannot cause noise violations are not analyzed in detail and have no detailed reporting information.

Feedback

What Next

This is an informational message. If you want to see detailed information for this net consider using the all analysis type of the *set_noise_parameters* command.

See Also

- set_noise_parameters

NPLDRC

NPLDRC-001

(info) Analyzing PG structure for %ld layers using %d cores.

Description

The tool is analyzing the PG and user route shapes and vias so it can check for DRC violations between placed lib_cells and the PG grid.

The result of the PG structure analysis will be saved with the design in its NDM library so it can be re-used in later runs.

In future runs if the PG structures have changed then the PG structure analysis will be re-run on the updated PG structures.

What Next

If the design has been freshly read and not yet been saved to an NDM library, there is no place for the analysis to be saved. The analysis will re-run each time PG DRC checking is done.

Try saving the design to its NDM library after reading the design:

```
prompt> save_block
```

See Also

- save_block

NPLDRC-002

(info) Saving PG structure for '%s'.

Feedback

Description

The tool is saving the PG structure analysis in the design's NDM library so it can be re-used in later runs.

In future runs if the PG structures have changed then the PG structure analysis will be re-run on the updated PG structures.

What Next

The tool can now check for DRC violations between placed lib_cells and the PG grid.

NPLDRC-003

(info) Reading PG structure for '%s'.

Description

The tool is reading the PG structure analysis saved in the design's NDM library from a previous run.

Since the power structures have not changed since the previous run the PG structure analysis results can be re-used.

What Next

The tool can now check for DRC violations between placed lib_cells and the PG grid.

NPLDRC-004

(info) Updating unknown PG structure for '%s'.

Description

The tool could not read the saved PG structure analysis for this design from the NDM library because the file format was not recognized.

The tool will re-analyze the PG and user route shapes and vias so it can check for DRC violations between placed lib_cells and the PG grid.

The result of the PG structure analysis will be saved with the design in its NDM library so it can be re-used in later runs.

What Next

The tool will automatically re-run the PG structure analysis for this design.

Feedback

NPLDRC-005

(info) Updating PG structure for '%s'.

Description

The tool could not re-use the saved PG structure analysis for this design from the NDM library because the PG structures have changed since that run.

Changing the PG grid or user route shapes causes the tool to re-run the PG structure analysis before checking for DRC violations.

The tool will re-analyze the PG and user route shapes and vias so it can check for DRC violations between placed lib_cells and the PG grid.

The result of the PG structure analysis will be saved with the design in its NDM library so it can be re-used in later runs.

What Next

To avoid unneeded PG structure analysis, make all updates to the PG grid and setting clock tree and other user routes at once instead of incrementally.

The tool will automatically re-run the PG structure analysis for this design.

NPLDRC-006

(warning) Could not read PG structure for '%s'.

Description

The tool could not read the saved PG structure analysis for this design from the NDM library because the file contents were not recognized.

The tool will re-analyze the PG and user route shapes and vias so it can check for DRC violations between placed lib_cells and the PG grid.

The result of the PG structure analysis will be saved with the design in its NDM library so it can be re-used in later runs.

What Next

The tool will automatically re-run the PG structure analysis for this design.

NPLDRC-007

(warning) Detected a sector %s on layer %s with %d metal and/or via shapes.

Feedback

Description

Unusual PG grid definition consisting of combinations of small straps and inlaid vias or vias with abutting enclosures create huge sectors that are usually long and consist of many shapes. This might cause long runtime because the tool must merge these shapes to perform legality checks.

What Next

Check the PG grid definition and reformat if possible.

NPLDRC-008

(warning) place.legalize.auto_adjust_drc_rules_for_short_pin disables %s rule in %s layer..

Description

The tool detects short pins in the design and automatically disables color_based_end_of_line_alignment rule in M1.

What Next

The tool would not report Color-Based End-of-line Alignment rule on M1 short pins which can be patched or extended during detail_route.

NPLDRC-009

(Warning) Net name changed from %s to %s in cache.

Description

Net name cached by tool has been changed.

What Next

This is legitimate. Nothing needs to be done.

NPLDRC-010

(Warning) Net %s removed from cache.

Description

Net cached by tool has been removed.

What Next

This is legitimate. Nothing needs to be done.

Feedback

NPLDRC-011

(Warning) Technology file error. Via layer %s cut definition properties, cutNameTbl(%d), cutWidthTbl(%d), cutHeightTbl(%d), do not match size. Skipping processing of via layer.

Description

Error in technology file via layer cut definition.

What Next

Fix technology file.

PA

PA-001

(Error) The PrimeTime manager process detected PrimeTime worker instances that encountered fatal errors. The manager and all worker processes will now terminate. The fatal errors detected are listed below.

Description

While executing commands, one or more PrimeTime worker processes encountered fatal errors requiring the process to exit. In this situation, the manager cannot proceed, and the entire session is terminated.

PA-002

(error) Insufficient hosts added for command '%s' ('%d' added, '%d' required)

Description

The PrimeTime manager encountered a command requiring a minimum number of hosts to be added before allowing it to proceed. Since the number of hosts added was below the minimum, the command could not execute successfully.

What Next

Use the *set_host_options* command to set up the host options. See the man page for the specific command to determine its host requirements.

See Also

- set_host_options

Feedback

PA-003

(error) Insufficient hosts online for command '%s' ('%d' online, '%d' required)

Description

The PrimeTime manager encountered a command requiring a minimum number of hosts to be online before allowing it to proceed. Since the number of hosts online was below the minimum, the command could not execute successfully.

What Next

Use the *start_hosts* command to start remote host processes. If you have already used the *start_hosts* command, view a detailed report that describes all host options that you have created with the *report_host_usage* command. Examine how many hosts have come online. After the *start_hosts* command has returned you to the pt_shell prompt, hosts will come online in the background. Until sufficient hosts have come online, the command specified cannot proceed.

See Also

- start_hosts
- report_host_usage

PA-004

(Warning) Multi-scenario worker report logging enabled.

Description

For several merged reporting commands, the output of the command issued to the individual scenarios is not written out to the worker output logs by default. This helps limit the size of the worker log, as the information is only useful for debugging purposes.

PA-005

(Error) Distributed report message size must be greater than 0.

Description

Distributed report message size must be greater than 0.

PA-006

(Error) '%s' cannot be changed after worker processes have been launched.

Feedback

Description

The working directory in which remote processes are working cannot be changed after the processes have been launched.

PARA

PARA-001

(error) Cannot open file '%s'.

Description

The file name provided to *read_parasitics* cannot be opened.

What Next

Validate that the file name is correct.

PARA-003

(information) The net '%s' has many (%d) nodes, which might result in long runtime.

Description

You receive this message if the number of nodes in an annotated parasitic network exceeds the value of the *parasitics_warning_net_size* variable (default 10000). This message warns you that extended runtime could occur.

If the number of nodes exceeds the value of *parasitics_rejection_net_size* (default 20000), the network is rejected and automatically replaced by a lumped capacitance to avoid extended runtime. You receive a message (PARA-004) warning you of that action.

The value of *parasitics_warning_net_size* is ignored if it is greater than or equal to the value of *parasitics_rejection_net_size*.

The values of these variables are checked every time *read_parasitics* is issued.

What Next

This is an informational message only. No action is required on your part. To avoid receiving this message, you can increase the value of the *parasitics_warning_net_size* variable, or modify your parasitic network so that it contains fewer nodes.

See Also

- PARA-004

Feedback

PARA-004

(warning) The net '%s' has too many (%d) nodes, so a lumped capacitance will be used instead.

Description

You receive this message if the number of nodes in an annotated parasitic network exceeds the value of the *parasitics_rejection_net_size* variable. This message warns you that the detailed network is being replaced by a lumped total capacitance to avoid extended runtime.

If the number of nodes exceeds the value of the *parasitics_warning_net_size* variable (default 10000), you receive a message (PARA-003) warning you that extended runtime could occur.

The value of *parasitics_warning_net_size* is ignored if it is greater than or equal to the value of *parasitics_rejection_net_size*.

The values of these variables are checked every time *read_parasitics* is issued.

What Next

If it is acceptable to you for your detailed network to be replaced by a lumped total capacitance, no action is required on your part. Otherwise, you can increase the value of the *parasitics_rejection_net_size* variable, or modify the annotated parasitic network so that it contains fewer nodes.

See Also

- PARA-003

PARA-005

(error) Cannot use -keep_capacitive_coupling with %s format.

Description

You specified the *read_parasitics* command with the *-keep_capacitive_coupling* option, and the file format does not support it. Detailed Standard Parasitic Format (DSPF) and Reduced Standard Parasitic Format (RSPF) do not support *-keep_capacitive_coupling*.

What Next

To read this file, reenter the *read_parasitics* command without using the *-keep_capacitive_coupling* option.

Feedback

PARA-006

(error) %s pin '%s' is missing in the RC annotation for net '%s'. Ignoring the incomplete RC annotation.

Description

You receive this message if *report_annotated_parasitics* detects an incompletely back-annotated RC network in the current design. The message informs you that the RC network annotation on the specified net is being ignored because it is incomplete; the specified pin is not physically connected to the RC network annotation.

An incomplete RC network might be caused by errors in the parasitics file, or by missing information from the tool that generated the parasitics file. For example, a parasitics file generated by a place and route tool that has parasitics only for the top level (between the blocks) would generate this error, because PrimeTime requires the RC network to connect all leaf drivers to all leaf nodes.

This message is not issued for unconnected hierarchy pins; when these are missing in RC annotations, warning message PARA-007 is issued and the annotation is not ignored during delay calculation.

What Next

Examine the SPF or SPEF file to determine why the specified RC network is incomplete. If the error is caused by a valid incomplete network, you can complete it using the parasitics completion feature *read_parasitics -complete_with* or *complete_net_parasitics*. For other errors, you must correct the parasitics file manually. You might need to estimate the missing segments and manually add them. After you have corrected the SPF or SPEF file, reexecute *read_parasitics*.

To determine whether the parasitics file contains a valid incomplete RC network, start from a driver and try to reach all loads through resistances. If all missing segments of a net are between two pins, you can complete them using the parasitics completion feature; otherwise, you must correct the SPF or SPEF file manually.

See Also

- PARA-007
- read_parasitics
- report_annotated_parasitics
- complete_net_parasitics

Feedback

PARA-007

(warning) Unconnected hierarchy pin '%s' is missing in the RC annotation for net '%s'.

Description

You receive this message if *read_parasitics* or *report_annotated_parasitics -check* detects an incompletely back-annotated RC network in the current design. PrimeTime can tolerate missing unconnected hierarchy pins in RC annotations, so the annotation is not ignored during delay calculation. This message is only a warning; it can be suppressed with the *suppress_message* command.

If a missing pin is not an unconnected hierarchy pin, error message PARA-006 is issued instead and the RC annotation is ignored during delay calculation.

What Next

If you have not intentionally disconnected hierarchy pins from networks with exisiting RC annotations, investigate the source of the disconnection. Some tools temporarily add routing ports and fail to remove those unused after routing, and others disconnect test ports during scan-chain reordering.

See Also

- PARA-006
- read_parasitics
- report_annotated_parasitics
- complete_net_parasitics

PARA-008

(error) The RC annotation for net '%s' has too many near-zero elements.

Description

This message is shown if *report_annotated_parasitics* detects that the RC annotation has too many near-zero elements. Too many near-zero elements can lead to numeric instability in calculations.

A resistor with value less than or equal to 0.01 ohm is considered near-zero.

A capacitor with value less than or equal to 0.001 femtofarad is considered near-zero.

PrimeTime allows up to ten-thousand near-zero resistors and up to ten-thousand near-zero capacitors before rejecting the annotation.

Please note that near-zero capacitor elements can occur in an annotation due to specifying resistors without specifying the capacitors at resistors' nodes. In such cases PrimeTime will automatically create such capacitors with values of 0.001 femtofarad.

What Next

The only known instance of this problem is trying to annotate a gigantic clock-tree as a single net (i.e. with tens of thousands of fanouts) with near-zero placeholder data. The annotation must make physical sense in order to be used in RC delay calculations. Either the near-zero data must be changed or the net must be broken-up into smaller segments.

See Also

- read_parasitics
- report_annotated_parasitics
- complete_net_parasitics

PARA-010

(error) multiple occurrences of net '%s' in this file. Removed parasitics from this net.

Description

You read a binary parasitics (SBPF) file and there were multiple occurrences of some nets in that file, which is illegal. This is a very serious error. Either the netlist does not match the parasitics file, or there is a problem with the writer of the file. Each of these nets with corrupt parasitics has had its parasitics removed, generating this message. Further, all coupling for the entire file is ignored.

The binary parasitics file is expected to be an image of parasitics. That is, it is meant to be restored to the same netlist from which it was generated. Attempting to restore a binary parasitics file to a different netlist is an unsupported flow.

What Next

This condition has put the parasitics annotated on the design into an incomplete state. This may lead to inaccurate or incorrect results. You should discontinue the current session and determine if this is a mismatch between the file and the netlist, or if there is a problem with the provider of the binary parasitics file.

See Also

- read_parasitics
- PARA-011

Feedback

PARA-011

(error) Due to previous errors, all effects of coupling have been ignored from '%s'

Description

You receive this message in conjunction with PARA-010. You read a binary parasitics (SBPF) file and there were multiple occurrences of some nets in that file, which is illegal. Because of this problem, any effects of coupling were ignored for the file being read. If you were using *-keep_capacitive_coupling*, no new coupling capacitors would be added. If you were not using *-keep_capacitive_coupling*, no coupling capacitors would be reduced. They are simply ignored.

What Next

It is not recommended that you continue at this point. See the documentation for PARA-010 for mode details.

See Also

- read_parasitics
- PARA-010

PARA-020

(warning) -keep_capacitive_coupling not specified for a design which already has coupling.

Description

You receive this message from the *read_parasitics* command if you did not specify the *-keep_capacitive_coupling* option, but you previously issued a *read_parasitics* command to read an SPEF file (for the same design) and did use the *-keep_capacitive_coupling* option. This message warns you about a possible inconsistency between multiple *read_parasitics* commands.

What Next

If you intended not to use the *-keep_capacitive_coupling* option, no action is required on your part. Otherwise, reissue *read_parasitics* and use the *-keep_capacitive_coupling* option.

PARA-027

(error) Cannot specify both the -coupling_reduction_factor and the -keep_capacitive_coupling options.

Feedback

Description

The *read_parasitics* command found that both the *-coupling_reduction_factor* and the *-keep_capacitive_coupling* options are set.

What Next

Choose either the *-coupling_reduction_factor* or the *-keep_capacitive_coupling* option, but not both. If you specify the *-coupling_reduction_factor* option, the coupling capacitors are reduced to ground with the factor specified by the *factor* value, which conflicts with the use of the *-keep_capacitive_coupling* option. If you intend to keep the coupling capacitors, you do not need to specify the *-keep_capacitive_coupling* option.

See Also

- read_parasitics

PARA-040

(Warning) Coupling capacitor (%s %s %g) on net %s is discarded because %s

Description

The *read_parasitics* command found a problem with a coupling capacitor and the capacitor was discarded. The reason is given in the message. Typical reasons include missing objects (nets, pins), both nodes being in the same net (self-coupling of nets is not supported), or a capacitance value less than or equal to zero.

Note that in the case of self-coupling, this message will be issued whether or not the *-keep_capacitive_coupling* option is specified.

What Next

Examine the Standard Parasitic Exchange Format (SPEF) file for correctness.

See Also

- read_parasitics

PARA-041

(Warning) Coupling capacitor (%s %s %g) on net %s is reduced because %s

Description

You receive this message if the *read_parasitics* command found a coupling capacitor in a SPEF file which specifies a nonexistent aggressor sub-node. This error could be caused

Feedback

by a large RC network that was discarded by PrimeTime. This message warns you that the coupling capacitor connected being reduced (grounded).

What Next

This is a warning message only. If it is acceptable to you that the specified coupling capacitor is grounded, no action is required on your part. Otherwise,check the consistency between the netlist and SPEF file, and check for the presence of a large RC network. Make any changes necessary, then reexecute *read_parasitics*.

PARA-043

(warning) Invalid coupling capacitor (%s %s %g) on net %s: %s

Description

While reading a SPEF file, the *read_parasitics* command found an invalid coupling capacitor. This is usually due to a semantic error in the specification of the capacitor.

What Next

The reason is given in the body of the message.

See Also

- read_parasitics

PARA-044

(error) Invalid %s (%s %g) on net %s: %s

Description

The *read_parasitics* command found a capacitor or resistor which is invalid. This is usually due to a mismatch between the netlist and the parasitics file. The reason is given in the body of the message.

What Next

Examine the parasitics file for correctness.

See Also

- read_parasitics

Feedback

PARA-045

(Information) Merging parallel capacitor on net %s from %s %s with value %g: new total value %g.

Description

The *read_parasitics* command found a capacitor in parallel with another capacitor. This could be due to duplicate entries in a parasitics file, or a reduced coupling capacitor in a SPEF file.

What Next

No action necessary.

See Also

- read_parasitics

PARA-046

(Warning) No matching coupling capacitor found with value %g for victim net %s and aggressor net %s: Ground this coupling capacitor.

Description

The *read_parasitics* command found a coupling capacitor in the SPEF file in a victim D_NET which does not have a complementary entry in the referenced aggressor D_NET. In this case, the coupling capacitor is grounded. This is the behaviour of PrimeTime before version F-2011.06.

What Next

Correct SPEF calls for symmetric entries. Validate that this is an expected behavior of your extraction application.

See Also

- read_parasitics

PARA-047

(Warning) Net %s has been annotated with %s %s using the %s command. This takes precedence over values from parasitics.

Feedback

Description

The *read_parasitics* command found a network which already has annotated lumped capacitance or resistance set using the *set_load* or *set_resistance* commands, respectively. Lumped values from these commands take precedence over the values from parasitics files.

What Next

To use the total capacitance or resistance read in from a parasitics file, you must remove the existing values by using the *remove_capacitance* or *remove_resistance* commands.

PrimeTime then reverts to the detailed (or other) RC network.

See Also

- read_parasitics
- remove_capacitance
- remove_resistance
- set_load
- set_resistance

PARA-050

(information) Merged %d parallel coupling capacitors to total %g pf between file nodes '%s' and '%s'.

Description

While reading a SPEF file, the *read_parasitics* command found parallel coupling capacitors between two nets which needed to be merged. These parallel coupling capacitors are replaced by a single coupling capacitor with the capacitance equal to the sum of the capacitance of the parallel coupling capacitors. The number of capacitors, and the resulting total capacitance, are shown in the message.

What Next

No action necessary.

See Also

- read_parasitics

Feedback

PARA-051

(warning) Self-coupling for net '%s' is discarded

Description

The *read_parasitics* command found coupling from a net to itself in a Synopsys Binary Parasitics Format (SBPF) file. PrimeTime does not support self-coupling, so this coupling is discarded. Note that this message will be issued whether or not the *-keep_capacitive_coupling* option is specified.

What Next

No action is necessary. However, the user should determine if the application which wrote the binary parasitics file has a mode which will suppress self-coupling.

See Also

- read_parasitics

PARA-052

(warning) Net '%s' will be overwritten with %s parasitics from '%s'

Description

The net in question already has parasitics. This message is issued if the current file has reduced parasitics for the net, or if the net has reduced parasitics and the current file has detailed parasitics for the net. In any of these cases, the parasitics for the net are removed, and the parasitics from the file overwrite what was there.

What Next

No action is necessary.

See Also

- read_parasitics

PARA-053

(error) %s '%s' exists but is not connected to net '%s'

Description

The *read_parasitics* command was used to read binary parasitics. There is a mismatch between the binary parasitics file and the netlist. The data in the file indicates that the

Feedback

named pin or port is connected to the specified net, but it is not. This error will prevent the parasitics from being annotated on this net.

What Next

Ensure that you are applying the correct binary parasitics file to the correct netlist.

See Also

- read_parasitics

PARA-057

(warning) GPD Eco signature does not match with %s.

Description

The GPD Eco signature does not match with the mentioned design signature in the Galaxy ECO flow. This is checked to verify the consistency of the generated Eco GPD file.

What Next

Verify the generation of Eco GPD file.

PARA-058

(warning) Time-stamp signature missing in SPEF file.

Description

The time-stamp signature is missing in the comments section of the SPEF file. This is necessary to derive the correct paths in the ECO annotation for the hierarchical modules.

What Next

Check the comments in the SPEF header.

PARA-059

(Warning) Time-stamp signature mismatch between full and incremental SPEF.

Description

The time-stamp signature in the incremental (post-eco) SPEF does not matches the time-stamp of the full (pre-eco) SPEF. This information is checked for full vs incremental SPEF file consistency.

Feedback

What Next

Check the consistency between the full and incremental SPEF files.

See Also

- read_parasitics

PARA-060

(Warning) Failed to re-anchor parasitics on net '%s'

Description

An *insert_buffer* command was issued to buffer either the load or driver side pin of a net with parasitics. The parasitics are re-anchored on either the driver or load side of the buffer being inserted. If the re-anchoring failed all the parasitics of the orignial net will be removed. When this happens both the driver and load side nets of the inserted buffer will have no parasitics.

What Next

Parasitics will only be preserved if a single load or driver pin is being buffered. Although multiple pins can be buffered parasitics will not be preserved if more than one pin is buffered.

Use *set_load* to try and compensate for the removed parasitics.

See Also

- insert_buffer

PARA-061

(Warning) failed to re-anchor parasitics on net '%s'

Description

A *remove_buffer* command was issued and parasitics were present on the driver and/or load side nets connected to the buffer. The parasitics with the worst ground capacitance are moved to the net resulting after the buffer removal. If the re-anchoring failed all the parasitics of the driver and/or load side nets originally connected to the buffer will be removed. When this happens the resulting net after the buffer removal will have no parasitics.

Feedback

What Next

Use *report_net* to examine the pins of load and driver side nets of the buffer being removed.

Use *set_load* to try and compensate for the *removed_parasitics*

See Also

- remove_buffer

PARA-062

(error) The -original_file_name option was used without the -eco option.

Description

The *-original_file_name* option can only be used together with the *-eco* option to specify which original parasitics file that the given ECO file corresponds to.

What Next

Use the *-eco* option together with the *-original_file_name* option if you are reading ECO parasitics files. If not, do not use the *-original_file_name* option.

See Also

- read_parasitics

PARA-063

(Error) An ECO file cannot be read without reading original parasitics in SPEF or in version 3 (or later) of SBPF.

Description

The *-eco* option is used to load parasitics incrementally for an ECO change after original analysis is performed. The original parasitics should be present before one can read the ECO parasitics. Also, even if the original parasitics were read using version 2 or version 1 of SBPF, ECO operation cannot be applied. Only the version 3 or later versions of SBPF can be used for ECO operations.

What Next

Read the original parasitics before reading the ECO parasitics.

Feedback

See Also

- read_parasitics

PARA-064

(Error) Cannot auto-determine original file name for the ECO.

Description

The *-eco* option is used to load ECO parasitics corresponding to a particular extraction database. In the current session, parasitics were read in using multiple files. The attempt to auto-determine the original file name failed. Use *-original_file_name* option to distinguish which parasitic file that this ECO file corresponds to.

What Next

Give the *-original_file_name* option.

See Also

- read_parasitics

PARA-065

(Error) The specified original file cannot be found.

Description

The specified original file can not be found. If you used *-path* option while reading the original file, please issue the same *-path* for reading the ECO file also.

What Next

Check the file name given to *-original_file_name* option.

See Also

- read_parasitics

PARA-066

(Information) Attempting to read the ECO file to determine original file name.

Description

The *-eco* option is specified without specifying the *-original_file_name* option. Since parasitics are annotated into the current session using multiple parasitic files, it is

Feedback

necessary to determine which file does the ECO file correspond to. An attempt is being made to determine this information by looking at the ECO file.

What Next

If you do not want PTSI to auto determine this information, please provide *-original_file_name* option.

See Also

- read_parasitics

PARA-067

(Information) Attempting to read the parasitic file to auto-determine location transformation factors.

Description

The *-path* option was specified to read a parasitic file with locations without specifying the locations transformation factors. An attempt is being made to determine this information by looking at the parasitic file.

What Next

This is just information message, no action required.

See Also

- read_parasitics

PARA-068

(information) Locations of block %s are being transformed for '%s' rotation, '%s' flip, '%i' X offset and '%i' Y offset, the source is %s.

Description

This message gets issued only when you are reading parasitics with locations turned on via the variable 'read_parasitics_load_locations'. It was determined that the given block is rotated, flipped and/or offset before being placed at the chip-level. Hence, the locations will be automatically transformed to global co-ordinates. Global co-ordinates are determined by looking at the file that was read in without the -path option.

What Next

This is just an information message.

Feedback

See Also

- read_parasitics

PARA-069

(error) Invalid '%s' scale factor '%f'.

Description

A parasitic scale factor is defined as a floating point number greater than ZERO. You get this message when you specified a parasitic scale factor that is less than or equal to ZERO.

What Next

Make sure you specify correct scale factors and re-run the command.

See Also

- scale_parasitics

PARA-070

(error) There are no parasitics loaded.

Description

You have attempted to perform an operation like scale_parasitics that requires parasitics to have been loaded but no parasitics are set on this current design.

What Next

Read the parasitics first and re-run the command.

See Also

- read_parasitics
- scale_parasitics

PARA-071

(error) No net-specific scaling has been done.

Feedback

Description

You have attempted to reset scaling for few nets. But, reset_scale_parasitics on certain number of nets works only if there has been some previous net-specific scaling done. This message indicates that no such scaling has been done previously.

What Next

You may not want to issue reset_scale_parasitics, you may want to use scale_parasitics instead with factors equal to 1.0.

See Also

- scale_parasitics
- reset_scale_parasitics

PARA-072

(warning) No net-specific scaling has been done for net '%s'.

Description

You have attempted to reset/report scaling for few nets. But, reset_scale_parasitics or report_scale_parasitics on certain number of nets works only if there has been some previous net-specific scaling done. This message indicates that no such scaling has been done previously.

What Next

You may not want to issue reset_scale_parasitics, you may want to use scale_parasitics instead with factors equal to 1.0.

See Also

- scale_parasitics
- reset_scale_parasitics
- report_scale_parasitics

PARA-073

(error) No scaling has been done.

Feedback

Description

You have attempted to reset scaling of parasitics. But, reset_scale_parasitics works only if there has been some previous parasitic scaling done. This message indicates that no such scaling has been done previously.

What Next

You may not want to issue reset_scale_parasitics.

See Also

- scale_parasitics
- reset_scale_parasitics

PARA-074

(error) Invalid ECO SBPF found.

Description

You have attempted to read an ECO SBPF file. PTSI determined that the ECO file does not correspond to the original parasitic file. No coupling will be read from this current file.

What Next

You may not want to make sure you are using correct ECO SBPF file.

See Also

- read_parasitics

PARA-075

(error) Could not resolve net '%s'.

Description

This message gets issued when you are reading parasitics and a net name is found in the parasitic file that could not be resolved to any real net in the design. This happens when your physical design does not match the logical design. Net is searched by the net name and may also be searched by pin names associated on the net. This message tells you that all the searching did not the net name to any net or it resolved it to more than one net in the design.

What Next

Make sure your parasitic file matches the design.

Feedback

See Also

- read_parasitics

PARA-076

(error) Failed to create on-disk-caching files.

Description

The program failed to create temporary files for on disk caching. This can be due a number of reasons like the lack of write permissions on the specified cache directory, lack of disk space and so on.

What Next

Verify the permissions, disk space and reissue the command

PARA-077

(information) Coupling separations are set on the design that might overwrite the annotated cross-couplings.

Description

This message gets issued to inform you that you have set coupling separations for cross-talk or noise analysis and are reading parasitics. The coupling separation constraints take precedence and will overwrite the annotated cross-couplings for the specific nets.

What Next

This is just an information. No action is required.

See Also

- read_parasitics
- set_coupling_separation
- report_si_delay_analysis
- report_si_noise_analysis

PARA-078

(error) Could not find pin/port '%s' in design.

Feedback

Description

You get this message when you are trying to read parasitics and a specified pin/port cannot be found in the design.

What Next

Check the parasitic file/parasitic extractor for errors.

See Also

- read_parasitics

PARA-079

(error) Could not find net connected to pin/port '%s' in design.

Description

You get this message when you are trying to read binary parasitics and an unconnected pin/port is being annotated in the design.

What Next

Check the parasitic file/parasitic extractor for errors.

See Also

- read_parasitics

PARA-080

(error) Cannot read variation-aware parasitics when parasitics are already present.

Description

You get this message when you are trying to read variation-aware parasitics and the design is already annotated with parasitics. This is a limitation for now, and will be supported in future.

What Next

Remove the annotated parasitics and re-issue the read_parasitics command.

See Also

- read_parasitics
- remove_annotated_parasitics

Feedback

PARA-081

(error) Cannot read regular parasitics as variation-aware parasitics are already annotated on the design.

Description

You get this message when you are trying to read non-variation aware parasitics and variation-aware parasitics are already annotated on the design.

What Next

Remove the annotated parasitics and re-issue read_parasitics command.

See Also

- read_parasitics
- remove_annotated_parasitics

PARA-082

(error) Cannot open parasitic corner file '%s'.

Description

You get this message when you issue set_parasitic_corner command and the corner file cannot be opened for reading.

What Next

Check the file permissions and re-issue the command.

See Also

- set_parasitic_corner
- report_annotated_parasitics

PARA-083

(error) Unexpected data at line number '%d'.

Description

You get this message when you issue set_parasitic_corner and the parasitic corner file has unexpected contents.

Feedback

What Next

Check the file contents and re-issue the command.

See Also

- set_parasitic_corner
- report_annotated_parasitics

PARA-084

(error) Variation-aware parasitics are not loaded.

Description

You get this message when you perform an operation that requires variation-aware parasitics to be set and there are no such parasitics currently annotated.

What Next

Read the variation-aware parasitics and re-issue the command.

See Also

- set_parasitic_corner
- remove_parasitic_corner
- read_parasitics
- report_annotated_parasitics

PARA-085

(error) Parasitic corner is not set previously.

Description

You get this message when you issue 'remove_parasitic_corner' to remove the parasitic corner set for analysis in the presence of variation-aware parasitics and the tool determines that no parasitic corner was set previously.

What Next

No action is required.

Feedback

See Also

- remove_parasitic_corner
- set_parasitic_corner
- read_parasitics
- report_annotated_parasitics

PARA-086

(error) Parasitic corner cannot be found.

Description

You get this message when you issue 'set_parasitic_corner' to set the parasitic corner but the specified corner name cannot be found in the specified corner file.

What Next

Check the corner file and re-issue the command.

See Also

- set_parasitic_corner
- remove_parasitic_corner
- read_parasitics
- report_annotated_parasitics

PARA-087

(warning) Variation multiplier value for '%s' is outside the bounds at line '%d'.

Description

You get this message when you issue 'set_parasitic_corner' to set the parasitic corner but the specified corner in the corner file contains invalid variation multiplier values. These values are supposed to be within -3.0 to +3.0.

What Next

Check the corner file.

Feedback

See Also

- set_parasitic_corner
- remove_parasitic_corner
- read_parasitics
- report_annotated_parasitics

PARA-088

(error) Corner file does not match the base corner - aborting the reading. This is occuring while reading ground capacitances/resistances of net '%s'.

Description

You get this message when you are trying to read multiple corner parasitics but it is found that the current corner topology does not match the base corner.

What Next

Check the corner parasitic file and re-issue the command.

See Also

- read_parasitics

PARA-089

(warning) Ignoring the temperature parameter or unknown process variation parameter '%s'.

Description

You get this message when you are trying to read a corner file for variation-aware parasitics but the variation parameters given in the file do not match with the defined parasitic parameters. This can also happen for temperature corner setting because PrimeTime VX does not currently support temperature as a variation.

What Next

You may want to check the corner parasitic file.

See Also

- set_parasitic_corner
- report_annotated_parasitics

Feedback

PARA-090

(error) The "-create_default_variations" option can be used only along with "-keep_variations" option.

Description

You get this message when you are trying to read parasitics without keeping variation sensitivities but trying to generate default variation parameters.

What Next

Re-issue the command without the "-create_default_variations" option.

See Also

- read_parasitics

PARA-091

(warning) Failed to create node map information for the parasitic file.

Description

You get this message when you are trying to read parasitics with keeping coupling but PT was unable to create node map information between the parasitic file and PT. This node map information is usually not needed for the operation of PT, unless when you try to read in an ECO parasitic file via "read_parasitics -eco" in future.

What Next

You do not need to do anything.

See Also

- read_parasitics

PARA-092

(error) Cannot read variation-aware parasitics as regular parasitics are already annotated on the design.

Description

You get this message when you are trying to read variation-aware parasitics and non-variation-aware parasitics are already annotated on the design.

Feedback

What Next

Remove the annotated parasitics and re-issue read_parasitics command.

See Also

- read_parasitics
- remove_annotated_parasitics

PARA-093

(error) Number of variation parameters do not match. Aborting the reading.

Description

You get this message when you are trying to read variation-aware parasitics and the number of variation parasitics do not match the previous annotation. It is assumed that all parasitic extractions are done with the same variation-ITF file, hence the number of variation parameters, their names and order is supposed to match across all parasitic files.

What Next

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

See Also

- read_parasitics
- remove_annotated_parasitics

PARA-094

(error) Number of variation parameters do not match. Aborting the reading.

Description

You get this message when you are trying to read variation-aware parasitics and the number of variation parasitics do not match the previous annotation. It is assumed that all parasitic extractions are done with the same variation-ITF file, hence the number of variation parameters, their names and order is supposed to match across all parasitic files.

What Next

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

Feedback

See Also

- read_parasitics
- remove_annotated_parasitics

PARA-095

(error) Number of corners do not match for multi-corner read.

Description

You get this message when you are trying to read multi-corner binary parasitic file but the number of corners from the file do not match what is set previously. Aborting the read.

What Next

Check the parasitic files, the writer and figure out the reason for the mismatch and re-issue the command.

See Also

- read_parasitics

PARA-096

(information) Scaling parasitics to operating temperature of '%f'.

Description

You get this message when you are trying to read variation-aware parasitic files that have temperature sensitivities. If the operating condition temperature is different than the (global) extraction temperature, then this message is issued to inform you that the parasitics will be scaled to the given operating temperature.

What Next

No need of any action.

See Also

- read_parasitics

PARA-097

(error) All instance paths in the -path option should correspond to valid and same sub-design.

Feedback

Description

You get this message when you are trying to read parasitic files with a list of paths specified in the -path option and not all the paths correspond to the same sub design or some of the paths do not correspond to a valid hierarchical instances.

What Next

Reissue the command with proper paths in the -path option.

See Also

- read_parasitics

PARA-098

(warning) Detected semantically incorrect SPEF in coupling section.

Description

You get this message when you are trying to read parasitic files where the coupling capacitances are written in semantically incorrect manner. According to IEEE Std SPEF, coupling should be written so that current net comes first followed by coupled net. The application will read the file but runtime may be slower. Also, the support is not guaranteed in future versions.

What Next

No action needed for now, but please check with the SPEF writer tool to see why it is not following the standard.

See Also

- read_parasitics

PARA-099

(error) Loading locations with simultaneous hierarchy reading is currently not supported.

Description

You get this message when you are trying to read parasitic files by loading the files simulataneously using multiple instances in the -path option but have also enabled loading locations. For loading locations, you have to issue each instance separately in -path option.

Feedback

What Next

Please re-issue read_parasitics command with one -path at a time.

See Also

- read_parasitics

PARA-100

(Warning) No matching coupling capacitor found with value %g for victim net %s and aggressor net %s: Forcing symmetry for this coupling capacitor.

Description

The *read_parasitics* command found a coupling capacitor in the SPEF file in a victim D_NET which does not have a complimentary entry in the referenced aggressor D_NET. In this case, the coupling capacitor is forced to be symmetric, that is, a coupling capacitor of that value is created between the two nets at the given nodes. If there are similar records in the two D_NETs, but the values are dissimilar, then the result will be a single coupling capacitor with a value that is the sum of the two dissimilar values.

What Next

Correct SPEF calls for symmetric entries. Validate that this is an expected behavior of your extraction application.

See Also

- read_parasitics

PARA-101

(error) read_parasitics -eco can only be used when the program is in ECO mode.

Description

The *read_parasitics* command with -eco option can only be used in ECO mode.

What Next

Use set_program_options -enable_eco to enable the ECO mode.

See Also

- set_program_options

Feedback

PARA-102

(information) Reading parasitics file '%s' because parasitic information is required by the multicore manager.

Description

During a multicore analysis using PrimeTime, the manager process attempts to save runtime and memory by skipping the reading of parasitics, letting the remote processes perform this task instead. This saving is possible only when a single parasitics file, of any format other than PARA, DSPF or RSPF, is used within a session and the '-keep_capacitive_coupling', '-verbose', '-syntax_only', '-keep_variations', or '-path' options are not used with *read_parasitics*.

However, several subsequent ECO or reporting commands will force the manager to read the parasitics file: *complete_net_parasitics*, *connect/disconnect_net*, *insert/remove_buffer*, *report_annotated_parasitics*, *scale_parasitics*, *set_parasitic_corner* and *write_parasitics*.

What Next

No action is needed but, for optimal performance, check your script to see whether the command that forces the parasitics to be read is necessary.

See Also

- read_parasitics

PARA-103

(information) Parasitics file '%s' will be read by the remote processes.

Description

During a multicore analysis using PrimeTime, this message is outputted to indicate that the remote processes will read the parasitics file directly if it has not already been done so by the manager process.

What Next

No action necessary.

See Also

- read_parasitics
- PARA-102

Feedback

PARA-104

(error) Corner file does not match the base corner - aborting the reading. This occurs while reading coupling between nets '%s' and '%s'.

Description

You get this message when you are trying to read multiple corner parasitics but it is found that the current corner topology does not match the base corner in coupling section.

What Next

Check the corner parasitic file and re-issue the command.

See Also

- read_parasitics

PARA-105

(warning) Parasitics file '%s' was not read by the multicore manager because the multi_core_read_parasitics variable is set to 'disabled'.

Description

During a multicore analysis using PrimeTime, this warning is outputted to indicate that the manager did not read the parasitics file because the *multi_core_read_parasitics* variable is set to 'disabled'.

What Next

To allow the manager to read the parasitics file, set *multi_core_read_parasitics* to 'auto'.

See Also

- read_parasitics

PARA-106

(warning) Parasitics on net '%s' contain an unexpectedly large capacitance.

Description

While reading parasitics, parasitics on a node contain unexpectedly large capacitance

What Next

The value will be reduced to 1E+6 PF. Please check with parasitics generator tool.

Feedback

See Also

- read_parasitics

PARA-107

(information) Log for '%s' will be generated in '%s'.

Description

When parasitics are read in a side process, the log for parasitic commands will be generated in a new file as informed by this message.

What Next

No action is required.

See Also

- parasitics_log_file

PARA-108

(error) ECO parasitics should not be read in hierarchical analysis.

Description

It is not supported to read eco parasitics in hierarchical analysis.

What Next

Check if it is really necessary to read this eco parasitics.

PARA-110

(warning) Primetime detected multiple annotations for net segment %s.

Description

This error occurs when multiple annotations for the same net segment exist in the same parasitics file. Something is not right in the extraction.

What Next

Check extraction data.

Feedback

See Also

- read_parasitics
- PARA-114

PARA-111

(Warning) Parasitics on net '%s' contain an unshielded coupling '%f'. Ignoring this coupling.

Description

While reading parasitics, parasitics on a node contain an unshielded coupling, and this coupling is ignored in non-HyperScale flow.

What Next

Use HyperScale flow if this coupling needs to be used.

PARA-112

(Warning) Net "%s" already has parasitics, and its parasitics are overwritten.

Description

A net already has parasitics and its parasitics have not been augmented.

Some possible causes of this problem are:

1. multiple segments of a net occur in a single SPEF file. This is not legal SPEF. Something is not right in the extraction. 2. multiple parasitics files are read, and they annotate same segments of same nets. For this case, the annotation from the first file is kept.

See Also

- read_parasitics

PARA-113

(warning) The "-increment" option is obsolete and will be removed in the upcoming release.Please update your scripts or they will fail!

Description

Reading parasitics is always in incremental mode and the "-increment" is ignored.

Feedback

What Next

Please update the script to remove the "-increment" option.

See Also

- read_parasitics

PARA-114

(error) Parasitics of nets are double annotated (for example, net %s). Ignoring invalid double-annotated parasitics.

Description

This error occurs when the parasitics of a net were already complete, and you read additional parasitic data on the same net. This can happen if you read a file twice, read another file that contains the same content as the first file, or use the *read_parasitics -complete_with* command followed by another *read_parasitics* command.

If the second annotation does not occur on a terminal node, then PrimeTime considers it to be a valid annotation and stitches the parasitic data. In this case, PrimeTime does not issue an error message.

However, if the second annotation occurs on a terminal node, PrimeTime considers it to be an invalid annotation and ignores it. In this case, PrimeTime issues this error message.

What Next

Make sure parasitics files cover different parts of a design; if needed to complete parasitics, use the *complete_net_parasitics* command after reading all parasitic data.

See Also

- complete_net_parasitics
- read_parasitics

PARA-115

(Error) Location transformation failed for hierarchy '%s'.

Description

This message gets issued only when you are reading parasitics with locations turned on via the variable '*read_parasitics_load_locations*'. PrimeTime attempted to determine if the given block is rotated, flipped and/or offset before being placed within the parent hierarchy. PrimeTime could not find a way to automatically transform the local co-ordinates

Feedback

to global ones. When this error occurs, the block coordinates are used as is, without any transformation. This can lead to errors in Advanced OCV distance-based derating or statistical STA computations using spatial correlation.

What Next

Please check the location of the hirarchical pins in top level and block level parasitic files.

See Also

- read_parasitics

PARA-116

(error) The "-syntax_only" option can not be used once parasitics have been read.

Description

This error occurs when the command *read_parasitics* is used with the *-syntax_only* option after parasitics were already read and loaded. The *-syntax_only* option is provided to help troubleshoot your parasitics file and avoid generating error messages during the actual annotation, and should not be used in a production script.

What Next

Make sure you do not use the *-syntax_only* option after a regular call to *read_parasitics*.

See Also

- read_parasitics

PARA-117

(error) The number of arguments in the location options does not match the number of instances in the "-path_list" option. Aborting the reading.

Description

This error occurs when the number of arguments in any location option, i.e. "-x_offset", "-y_offset", "-axis_flip" or "-rotation" does not exactly match the number of arguments in the "-path_list" option.

What Next

Please check the arguments in the location options, fix the mismatch and re-issue the command.

Feedback

See Also

- read_parasitics

PARA-118

(Information) User-defined location transformation of parasitics for instance '%s' with '%s' rotation, '%s' flip, '%f' X offset and '%f' Y offset will be applied during top-level parasitics loading.

Description

Parasitics of HyperScale instances are automatically read by PrimeTime when these instances are instantiated at top level, and user-specified parasitics reading of these instances is automatically skipped. However, user-defined options for location transformation of hierarchical blocks are stored and will be applied to the specified blocks when the parasitics for the top level are loaded.

See Also

- read_parasitics

PARA-119

(error) Corner(s) must be specified before reading a multi-cornered parasitics file.

Description

This error occurs when a multi-cornered parasitics file is read, but no corner names are specified.

What Next

Specify the corner name by setting the variable *parasitics_corner*, before doing *read_parasitics*.

See Also

- read_parasitics

PARA-120

(error) Parasitics corner (%s) not found in parasitics file.

Description

This error occurs if the user specified corner is not found in the parasitics file.

Feedback

What Next

Check that the corner name(s) specified by variable *parasitic_corner_name* is actually present in the parasitics file.

See Also

- read_parasitics

PARA-121

(error) Cannot reset parasitics corner(s), design already annotated with previously set parasitics corner(s).

Description

This error occurs if the user attempts to change the parasitics corner in the course of *read_parasitics*. This is to prevent annotation of different parasitic corner values leading to an incoherent annotation.

What Next

Resetting the parasitic corner is allowed only after the annotated parasitics are removed.

See Also

- read_parasitics

PARA-122

(warning) Attempting to read parasitic corner(s), but file is not multi-cornered.

Description

This warning occurs if the user has set *parasitics_corner* but the parasitics file has no corner information (i.e., not multi-cornered).

What Next

Don't set *parasitics_corner* before reading a simple (i.e., not multi-corner) parasitics file. If *parasitics_corner* has been set by mistake, just unset it before doing *read_parasitics*.

See Also

- read_parasitics

Feedback

PARA-123

(warning) Reduced annotation reading must be enabled before reading a parasitics file which contains reduced annotations.

Description

This warning occurs when a parasitics file contains reduced annotations, but reduced annotation reading is not enabled.

What Next

Contact Synopsys Customer Support Center if needed.

See Also

- read_parasitics

PARA-124

(error) Cannot find %s '%s' in design '%s'

Description

The specified object cannot be found in the given design. This is seen while reading parasitics files. In this case, it could indicate a file which is out of sync with the design.

What Next

Verify that the file matches the design.

PARA-125

(warning) Location transformation offsets of hierarchy '%s' overridden by manual offsets.

Description

The tool issues this warning when you read parasitics with locations turned on with the *read_parasitics_load_locations* variable. The tool attempted to determine if the given block is rotated, flipped, or offset before being placed within the parent hierarchy. The location offsets were replaced by user-specified manual offsets from the *read_parasitics* command.

What Next

Verify that the manual offsets are correct.

See Also

- read_parasitics

PARA-126

(error) Missing -axis_flip information during automatic location transformation for hierarchy '%s'. Using default setting flip_none.

Description

The tool issues this error when you read parasitics with locations turned on with the *read_parasitics_load_locations* variable. The tool cannot automatically determine the flip axis information for this hierarchy. Automatic location transformation will proceed by using the default *flip_none* setting, but this can lead to incorrect orientation and offsets and generate errors in advanced on-chip variation (AOCV) distance-based derating or statistical static timing analysis (STA) computations using spatial correlation.

What Next

Specify the correct setting for the *-axis_flip* option of the *read_parasitics* command. If no flip is required, use the *-axis_flip flip_none* option.

See Also

- read_parasitics

PARA-127

(error) Could not find locations of net '%s' in previous read.

Description

The specified net was annotated in a previous read without locations. This is seen while reading parasitics files with locations reading enabled. This could mean that a parasitics file has been read with locations reading disabled.

What Next

Verify that locations reading is enabled for all parasitics files.

PARA-128

(error) GPIO error '%s' in SPEF to GPD converter.

Feedback

Description

Error Message:

CANNOT_CREATE_GPD_DIR : The GPD directory could not be created. *CANNOT_OPEN_FILE_FOR_WRITE* : The GPD file could not be opened for writing. *CELLS_PORTS_NETS_UNDEFINED* : Number of Cells, Ports, and Nets undefined. *ID_MAPPING_UNDEFINED* : Network id to index mapping undefined. *NULL_OBJECT* : The pointer to net being written is NULL. *INVALID_FUNCTION_FOR_CLIENT_MAPPING* : Invalid function for client mapping. *NET_INDEX_OUT_OF_BOUNDS* : Net index is out of bounds. *PORT_INDEX_OUT_OF_BOUNDS* : Port index is out of bounds. *CELL_INDEX_OUT_OF_BOUNDS* : Cell index is out of bounds. *UNKNOWN_ERR* : Unknown error.

What Next

Take action if possible to rectify error. Else contact owner of SPEF to GPD converter.

PARA-129

(warning) Net in SPEF file has no name.

Description

The net in the SPEF file being converted to GPD does not have any name.

What Next

There may be a problem with the SPEF file, please make sure it is valid.

PARA-130

(warning) No nets found in the SPEF file for the SPEF to GPD converter.

Description

The net list in SPEF file is empty.

What Next

There may be a problem with the SPEF file. Please make sure it is valid.

PARA-131

(warning) Net '%s' not found in SPEF to GPD converter.

Feedback

Description

The net was not found in the GPD design after parsing the SPEF file.

What Next

There may be a problem with the SPEF to GPD converter, contact the owner.

PARA-132

(warning) RC data for net '%s' could not be processed in SPEF to GPD converter. Cannot convert SPEF to GPD.

Description

There is a problem processing RC data for this net. Either the internal node, pin, port, or aggressor node or net could not be found.

What Next

There may be a problem with the SPEF file, check the net reported in the SPEF file and make sure it is valid. If is is valid, the problem could be with the SPEF to GPD converter, contact the owner.

PARA-133

(error) Sensitivity coefficient is not supported in SPEF to GPD converter.

Description

Sensitivity coefficient is detected in the SPEF file. This is not supported in SPEF to GPD converter.

What Next

Please check the SPEF file and remove any sensitivity coefficients.

PARA-134

(warning) Ground Cap for node is already set to %0.5f. New value %0.5f cannot be added. Cannot convert SPEF to GPD.

Description

There may be multiple values for ground cap for the same node in a net in SPEF file. Corresponding GPD cannot be generated using SPEF to GPD converter.

Feedback

What Next

Please use write_parasitics from PT or regenerate the SPEF file without multiple definitions of node Ground Cap.

PARA-137

(error) Found asymmetric coupling in SPEF file. Cannot convert SPEF to GPD.

Description

When asymmetric coupling is found in the input SPEF, corresponding GPD cannot be generated using SPEF to GPD converter.

What Next

Please use write_parasitics from PT or regenerate the SPEF file with symmetric coupling.

PARA-140

(error) GPD directory is not accessible or corrupted '%s'.

Description

The GPD directory your are trying to read is not accessible or has been corrupted.

What Next

Check the GPD directory access or try to re-generate it.

PARA-141

(error) Could not find '%s' '%s'.

Description

This message indicates a that missing object (Cell/Pin/Net) is detected during reading GPD.

What Next

Check that the generated GPD directory is in sync with the given design.

PARA-142

(error) Negative total %s ('%0.5f') for net '%s'.

Feedback

Description

This message indicates a that the specified total capacitance of the net has negative value.

What Next

Check the GPD directory or try to re-generate it.

PARA-143

(error) Bad '%s' value ('%0.5f') on net '%s'.

Description

This message indicates a that the value associated with the given object (Capacitor/Resistor) is not consistent.

What Next

Check the GPD directory or try to re-generate it.

PARA-144

(error) Pin '%s' is not connected to net '%s'.

Description

This message indicates that the specified pin is annotated as part of the specified net, but the pin is not connected to the net.

What Next

Check the GPD directory or try to re-generate it.

PARA-145

(error) Bad '%s' nodes ('%d', '%d') on net '%s'.

Description

This message indicates a that the specified object (Capacitor/Resistor) is associated with a node that does not exist.

What Next

Check the GPD directory or try to re-generate it.

Feedback

PARA-146

(error) Aggressor of net '%s' is missing.

Description

This message indicates a that an aggressor of the given net is missing. The couplings to that aggressor will be grounded.

What Next

Check the GPD directory or try to re-generate it.

PARA-147

(error) Hierarchy '%s' has been annotated in a previous read. Ignoring double-annotated hierarchy.

Description

The specified hierarchy in the -path option of a read_parasitics command was annotated in a previous read.

What Next

Verify that the hierarchical blocks are not double-annotated.

PARA-148

(warning) Hierarchy '%s' cannot be transformed because it does not correspond to a netlist hierarchy. Ignoring hierarchy transformation.

Description

The specified hierarchy transformation in GPD cannot be applied because the hierarchy specified, cannot be found in the netlist.

What Next

Verify that the GPD files correspond to the netlist.

PARA-149

(error) No layer was found with name '%s' in parasitic files.

Description

The specified parasitic variation cannot be applied because of the error.

Feedback

What Next

Verify that the layer names correspond to what is present in parasitic files.

PARA-150

(warning) MIM %s is enabled and is not compatible with the DHA or Hyperscale flows.

Description

This message gets issued only when you are reading parasitics with advanced automatic MIM features turned on via the variable 'read_parasitics_enable_mim_merging' or 'read_parasitics_enable_mim_reordering'.

These features are not compatible with the following flows, and might impact QoR: - Hyperscale - DHA - Reduced ressources ECO

What Next

Please check that you are not using any of the flows cited above, and disable the features if needed.

PARA-159

(Information) Primetime detected parasitics file with location transformation guidance.

Description

The current parsitics file contains transformation guidance for some of the sub-blocks. PrimeTime will use these transformations if the user didn't specify locations transformation.

What Next

This is just information message, no action required.

See Also

- read_parasitics

PARA-160

(error) Missing corners for multi-corner read_parasitics.

Description

This message gets issued only when you are reading parasitics with only one of -nominal_corner, -max_corner or -min_corner. Multi-corner flow requires at least two corners to be specified.

Feedback

What Next

Please provide at least 2 corners for the SMC GPD flow.

See Also

- read_parasitics

PARA-161

(warning) Missing nominal corner for multi-corner parasitics might impact accuracy.

Description

This message gets issued only when you are reading parasitics with -max_corner and -min_corner options, but without giving a Nominal corner as reference. Missing nominal corner might impact accuracy.

What Next

To ensure accuracy of results, please provide a nominal corner with -nominal_corner option.

See Also

- read_parasitics

PARA-162

(Warning) Coupling capacitor (%s %s %g) on net %s is grounded because %s

Description

The *read_parasitics* command found a problem with a coupling capacitor and the capacitor was grounded. The reason is given in the message. Typical reasons include missing objects (nets, pins), both nodes being in the same net (self-coupling of nets is not supported), or a capacitance value less than or equal to zero.

Note that in the case of self-coupling, this message will be issued whether or not the *-keep_capacitive_coupling* option is specified.

What Next

Examine the Standard Parasitic Exchange Format (SPEF) file for correctness.

See Also

- read_parasitics

Feedback

PARA-163

(error) Command '%s' requires parasitic explorer analysis to be enabled.

Description

The command requires the *parasitic_explorer_enable_analysis* variable to be set to *true*.

What Next

Decide whether you want to use parasitic explorer features. If you do, set the *parasitic_explorer_enable_analysis* variable to *true*.

See Also

- parasitic_explorer_enable_analysis

PARA-164

(error) Nodes '%s' and '%s' specified for path-based parasitics query must belong to the same net.

Description

You requested parasitics in a path specified by the *-from_node* and *-to_node* options, but the specified nodes are connected to different nets.

What Next

Make sure that the nodes specified by the *-from_node* and *-to_node* options are connected to the same net.

See Also

- get_resistors
- get_ground_capacitors
- get_coupling_capacitors
- parasitic_explorer_enable_analysis

PARA-165

(error) %s node range for net '%s' must be between '1' and '%d'

Feedback

Description

In the *-from_node* or *-to_node* option of the *get_resistors* command, you specified a node index value that was out of range for the net.

What Next

Specify a node index value that is between 1 and the total number of nodes in the net.

See Also

- get_resistors
- parasitic_explorer_enable_analysis

PARA-166

(warning) No path found from node '%s' (%d) to node '%s' (%d) for net '%s'.

Description

You used the *get_resistors* command with the *-from_node* and *-to_node* options, but there is no path between the specified nodes.

What Next

Make sure that a path exists from the *-from_node* to the *-to_node*.

See Also

- get_resistors
- parasitic_explorer_enable_analysis

PARA-167

(warning) Parasitic backgrounded reading terminated due to query of parasitic data by user, in command '%s'.

Description

You received this message because a query of parasitic data occurred during backgrounded reading of parasitics.

What Next

Correct your scripts such that no parasitic data is queried until update_timing is successfully finished.

Feedback

See Also

- get_resistors
- parasitic_explorer_enable_analysis

PARA-168

(Error) Cannot enable Parasitic Explorer because parasitics are already annotated on the design.

Description

You tried to enable the Parasitic Explorer feature (set the *parasitic_explorer_enable_analysis* variable to true) with parasitics already annotated on the design.

What Next

Start over and enable the Parasitic Explorer feature before you use the *read_parasitics* command.

See Also

- parasitic_explorer_enable_analysis

PARA-169

(Error) Cannot read parasitics file because of previous actions.

Description

You received this message because you tried to read in a parasitics file in a manner that is inconsistent with another parasitics file read in earlier. The inconsistency is related to the *parasitic_explorer_enable_analysis* variable setting used when reading the parasitics files. The following actions are not allowed:

- Reading a GPD file with the variable set to *true* after reading another GPD file with the variable set to *false*.
- Reading a GPD file with the variable set to *false* after reading another GPD file with the variable set to *true*.
- Reading a GPD file with the variable set to *true* after reading a non-GPD parasitics file with the variable also set to *true*.
- Reading a non-GPD parasitics file with the variable set to *false* after reading a GPD file with the variable set to *true*.

Feedback

What Next

Correct your scripts to set the *parasitic_explorer_enable_analysis* variable to *true* just before you read in GPD parasitics, and leave it set to *true* if you read in any additional parasitics (whether GPD or non-GPD).

See Also

- parasitic_explorer_enable_analysis

PARA-170

(Error) Command '%s' requires Parasitic Explorer analysis to be enabled when parasitic data is loaded.

Description

The command requires Parasitic Explorer data, which is available only if the *parasitic_explorer_enable_analysis* variable is set to *true* before you read in the GPD parasitics.

What Next

Correct your script to set the *parasitic_explorer_enable_analysis* variable to *true* before you use the *read_parasitics* command.

See Also

- read_parasitics
- parasitic_explorer_enable_analysis

PARA-171

(Error) Unable to read GPD parasitics.

Description

You tried to read parasitics in GPD format, but the data could not be found in the specified path.

What Next

Specify the correct path to the GPD data, and make sure that the StarRC tool correctly generated the GPD data for Parasitic Explorer usage.

Feedback

See Also

- read_parasitics
- parasitic_explorer_enable_analysis

PARA-172

(Error) Parasitics file incompatible with Parasitic Explorer.

Description

The Parasitic Explorer was enabled and you tried to read a parasitics file that was either not in GPD format or not created by the StarRC tool.

What Next

In the *read_parasitics* command, specify a GPD file that was generated by the StarRC tool, or disable the Parasitic Explorer mode.

See Also

- read_parasitics
- parasitic_explorer_enable_analysis

PARA-173

(Information) The 'read_parasitics' command is disabled during Constraints Consistency mode.

Description

If the Constraints Consistency mode is enabled by setting the 'pt_enable_constraint_consistency_mode' variable as true, the 'read_parasitics' command is disabled, since parasitics data is not used for constraints consistency checks.

PARA-174

(warning) SPEF xform comment on hierarchy '%s' was ignored.

Description

SPEF xform on a hierarchy A/B is not in the SPEF file of its parent hierarchy A, and hierarchy A/B had been already annotated.

Feedback

What Next

The xform comment had been ignored because A/B was already annotated. Possible solutions are: - Move xform comment to the SPEF file of the parent hierarchy, and adjust the transformation to be relative to parent - If xform comment is in top, you can use top-down flow to read xform comment first - if xform comment is in top, you can replace it by using manual locations in the read_parasitics command of hierarchy A/B

See Also

- read_parasitics

PARA-180

(Warning) SPEF corner name does not match previous read corner name.

Description

The current corner name in the SPEF file is different from the previous read in corner name. The corner name will be overwritten.

What Next

Check if the correct SPEF corner file is being read.

PARA-181

(Warning) Checking locations of net "%s" has been skipped because the net does not have valid parasitics.

Description

A net does not have valid parasitics, so checking the locations of its pins has been skipped.

Some possible causes of this problem are:

1. The net had too many nodes and it has been converted to lumped net. 2. The net does not have parasitic annotation due to errors.

See Also

- read_parasitics
- report_annotated_parasitics

Feedback

PARA-182

(Error) Difference in locations of net "%s" (e.g. pin "%s"). DEF locations in microns: ('%f' '%f'), SPEF/GPD locations in microns: ('%f' '%f').

Description

A discrepancy was found in the pin locations of a net, when comparing the locations from DEF versus the locations from SPEF/GPD. The message is printed for only one pin per net.

Some possible causes of this problem are:

1. SPEF/GPD locations are wrong. 2. DEF locations are wrong.

See Also

- read_parasitics
- report_annotated_parasitics

PARA-183

(warning) layer ID '%d' in '%s' does not exist in layer map. ID '-1' will be used instead.

Description

A layer ID found that does not correspond to any layer name.

What Next

Verify that the layer ID exists in the layer map section.

PARA-184

(warning) layer ID of %s is inconsistent with previously loaded layers. ID '%d' will be used instead of ID '%d'.

Description

An inconsistency in layer maps from different parasitics files has been detected. The conflicting layer will have a different ID automatically assigned.

What Next

The layer has been automatically assigned a different ID

Feedback

PARA-185

(Information) Coupling capacitor (%s:%d, %s:%d) on net %s has %g value

Description

The *read_parasitics* command found a problem with a coupling capacitor.

What Next

Examine the parasitics file for correctness.

See Also

- read_parasitics

PARA-187

(Error) Previously computed location values for hierarchy %s : (x_offset: %i, y_offset: %i, rotation: %s, flip: %s) are invalidated by user-set values. New manually given locations values are (x_offset: %i, y_offset: %i, rotation: %s, flip: %s).

Description

Previous location values of a hierachy were automatically computed and are now invalidated by new use-provided locations: boundary nets may have undetermistic locations.

See Also

- read_parasitics
- read_parasitics_load_locations

PARA-188

(Error) The layer-to-layer coupling capacitances scaling derate has encountered an error: %s The layer to layer coupling capacitances scaling derate has not been applied to the scaling of the parasitics.

Description

The layer-to-layer coupling capacitances scaling derate could not succeed due to a problem.

See Also

- scale_parasitics

Feedback

PARA-189

(Error) The coupling capacitances scaling could not be performed because: %s It is recommended to perform 'reset_scale_parasitics'.

Description

The coupling capacitances scaling could not be performed because of a problem.

See Also

- scale_parasitics

PARA-190

(warning) The via model ID '%d' in '%s' does not exist in the via model map. It is ignored.

Description

A via model ID was found that does not correspond to any via model name in the via model map declarations.

What Next

Verify that the via model ID exists in the via model map section **VIA_MODEL_NAME_MAP*.

PARA-191

(error) The number of unique via model names (%d) has exceeded the maximum limit in '%s'.

Description

Up to 32767 unique via model names are supported by the tool. However, the indicated file exceeds this limit.

What Next

If possible, reduce the number of different via model names in the indicated SPEF file.

PARA-401

(Warning) %d coupling capacitors on net %s are reduced because %s

Feedback

Description

The *read_parasitics* command found a problem with coupling capacitor and the capacitors were discarded. The reason is given in the message. This warning reports the number of times a net has dropped coupling capacitors for the specified reason. Typical reasons include missing objects (nets, pins), both nodes being in the same net (self-coupling of nets is not supported), or a capacitance value less than or equal to zero.

Note that in the case of self-coupling, this message will be issued whether or not the *-keep_capacitive_coupling* option is specified.

What Next

Examine the Standard Parasitic Exchange Format (SPEF) file for correctness.

See Also

- read_parasitics

PARA-501

(Warning) %d coupling capacitors on net %s were discarded because %s

Description

You receive this message if the *read_parasitics* command found a coupling capacitor in a SPEF file which specifies a nonexistent aggressor sub-node. This error could be caused by a large RC network that was discarded by PrimeTime. This warning reports the number of times a net has dropped coupling capacitors for this specific reason. The coresponding coupling capacitors connected are reduced (grounded).

What Next

This is a warning message only. If it is acceptable to you that the coupling capacitors are grounded, no action is required on your part. Otherwise,check the consistency between the netlist and SPEF file, and check for the presence of a large RC network. Make any changes necessary, then reexecute *read_parasitics*.

PDC

PDC-001

(Warning) Reference '%s' pin '%s' has no via regions. Using pin shape.

Feedback

Description

The pin specified does not contain via regions generated in the frame. Pin shape is used instead for legality checking.

What Next

Check your library preparation procedure for correctness.

PDC-002

(Error) Design '%s' has no associated Technology.

Description

The design specified is missing Technology file information. Legalization is thus unable to proceed.

What Next

Check your data preparation procedure for correctness.

PDC-003

(Warning) Routing direction of metal layer %s is neither "horizontal" nor "vertical". PDC checks will not be performed on this layer.

Description

This warning message indicates that no routing direction has been set on the metal layer. This may result in DRC violations due to illegal placement.

What Next

set_attribute [get_layer <layer>] routing_direction <horizontal/vertical>

PDC-004

(Warning) Technology file error detected. Excluded Spacing Range defined but corresponding Min Spacing Table and/or Parallel Length Table is not.

Description

This warning message indicates that a technology file error has been detected. This may result in DRC violations due to illegal placement.

What Next

Check and fix technology file.

Feedback

PDC-005

(Error) Power/Ground pin %s/%s shorts with unconnected metal shape %s.

Description

This error message indicates that a short between a cell's power/ground pin and an unconnected metal shape has been found which likely indicates a failure to properly connect the Power/Ground rails to their nets. This will result in legalization failure.

What Next

Fix Power/Ground rail connectivity.

PDC-006

(Warning) Technology file via layer %s definition has conflicting sizes of cut name, width, height tables.

Description

This warning message indicates that technology file fields "cutNameTbl", "cutWidthTbl" and "cutHeightTbl" in the given via layer definition are inconsistent with each other. Via spacing checking on this layer will be skipped.

What Next

Fix technology file.

PDC-007

(Warning) No tracks defined on metal layer %s. Pin access checking disabled for this layer.

Description

This warning message indicates that no track definition has been found in the NDM on the given metal layer. Pin access checking on this layer will be skipped.

What Next

Fix floorplan.

PDC-008

(Warning) Command set_legalizer_preroute_keepout encountered error in setting keepout on provided pins or lib_pins.

Feedback

Description

This warning message indicates the keepout could not be set on one or more of the named pins/lib_pins.

What Next

Review the pin/lib_pin list.

PDC-009

(Warning) Command set_legalizer_access_track_constraint encountered error in setting the constraint on provided pins or lib_pins.

Description

This warning message indicates the constraint could not be set on one or more of the named pins/lib_pins.

What Next

Review the pin/lib_pin list.

PDC-010

(Error) No site_defs found in top block.

Description

This error message indicates that there are no site_defs defined in the design block. Pre-routed net checking is disabled.

What Next

Review the floorplanning steps,

PDC-011

(Warning) Technology file field cut%dNameTbl in Design Rule for layers %s, %s has undefined cut name %s.

Description

This warning message indicates that the technology file definition for given Design Rule lists a cut name that is not defined in the Via layer section. Legalization will not be able to honor the associated rules.

Feedback

What Next

Fix the technology file.

PDC-012

(Warning) Pin %s of RefLib %s has different direction from preferred track.

Description

Pin/track alignment requires pin and track are always in the same direction. This message indicates some pin direction do not follow this rule.

What Next

Check input design to see if pin/track direction is set correctly.

PDC-013

(Warning) Grid %s is not found. Via0 alignment is disabled.

Description

The named via0 alignment grid is not found in NDM. User must provide valid via0 grid name to app_option "place.legalize.via0_alignment_grid_name" to enable the alignment to the via0 grid. The grid object is created by executing command "create_grid".

What Next

Check if command "create_grid" has been executed to create the via0 grid object.

PDC-014

(Warning) Pin-track color alignment checking skipped for layer %s.

Description

Pin-track color alignment is not defined for the named metal layer. Only metal layers with tech file field "hasRectangleOnly = 1" are appropriate for Pin-color alignment checking.

What Next

Check application options and technology file.

PDC-015

(Error) One or more metal/via layer has been deleted. Pre-routed net checking is disabled.

Feedback

Description

This error message indicates that there is at least one deleted metal or via layer from the database. Pre-routed net checking is disabled. Any legalization or check_legality results are unreliable.

What Next

Review the floorplanning steps,

PDC-016

(Warning) On layer %s found %d identical %s %s at location %s. Check for duplicate power grid.

Description

Multiple identical vias or metal shapes were found at the same location. This could mean that this design's power grid was created or loaded multiple times. A duplicated power grid can greatly increase run-time, and should be corrected.

What Next

Check the vias or metal shapes at the location. If there are multiple identical shapes, the power grid has been duplicated. Remove the power grid from the affected layers and reload or recreate it once for those layers. Check your design loading script for duplication.

PDC-017

(Warning) Cannot save PG structure analysis in block '%s' for reuse. Later runs must recompute PG data.

Description

After PG structure analysis the tool could not save the PG structure data to the block for reuse. Later runs of the tool cannot reuse the saved data, the PG structure analysis must be recomputed.

The PG structure analysis can take considerable time and memory. The tool saves the results in the block so that the PG structure can be quickly re-read and reused. If the data cannot be saved it must recomputed, sometimes several times in the same flow. This can take considerable time and memory.

What Next

The most common reason why the PG structure analysis cannot be saved in the block is that the block has not yet been saved to disk. Either the block was just read in, or the

block was copied but not yet saved to its library. Use *save_block* to save the current block to its library on disk.

Another reason why the PG structure analysis cannot be saved is that the current user does not have write permission to the library containing the block. Use *copy_block* to copy the block to a library with write permissions. Then use *save_block* to save the copied block to disk.

If the library Unix directories and files have lost write permissions, the permissions can be altered with the Unix *chmod* command. Use *chmod -R u+w /path/to/library* to add user write permissions to the library directories.

See Also

- save_block

PDC-018

(Warning) Cannot save %s cache to block '%s' for reuse. Later runs must recompute cache data.

Description

After completing legalization design rule checking, the tool could not save the DRC caches to the block for reuse. Later runs of the tool cannot reuse the saved data, those checks must be re-run.

There can be millions of design rule checks and each one takes time. The tool caches the result of each check so it does not have to re-run each check for each lib cell. At the end of a run, the DRC results are saved to the block. At the start of the next run the DRC cache is reloaded from the block to save the time of re-running those design rule checks.

What Next

The most common reason why the DRC cache cannot be saved in the block is that the block has not yet been saved to disk. Either the block was just read in, or the block was copied but not yet saved to its library. Use *save_block* to save the current block to its library on disk.

Another reason why the DRC cache cannot be saved is that the current user does not have write permission to the library containing the block. Use *copy_block* to copy the block to a library with write permissions. Then use *save_block* to save the copied block to disk.

If the library Unix directories and files have lost write permissions, the permissions can be altered with the Unix *chmod* command. Use *chmod -R u+w /path/to/library* to add user write permissions to the library directories.

Feedback

See Also

- save_block

PDC-019

(warning) Using 'ignored_pnet_shape_layers' from the design library instead of from the reference library for lib-cell '%s'.

Description

The tool picks up the ignored_pnet_shape_layers rules (see PRF flow) first from the design library, and then from the reference libraries. This message indicates that the layer definitions were found in the design library as well as in the reference libary of the given lib-cell. The ones from the reference library are ignored.

PEM

PEM-001

(error) A pin must be specified for get_em_max_toggle_rate command

Description

No pin is specified for the command.

What Next

Specify a valid pin.

PEM-002

(error) %d pins are defined, get_em_max_toggle_rate expects only 1 pin

Description

Query using get_em_max_toggle_rate is requested for more than one pin.

What Next

Specify only one pin.

PEM-003

(error) Could not find requested pin specified in get_em_max_toggle_rate command.

Feedback

Description

Query using get_em_max_toggle_rate is requested for non existence pin.

What Next

Specify a valid pin.

PEM-004

(error) %d related pins are defined, get_em_max_toggle_rate expects only 1 related pin

Description

Query using get_em_max_toggle_rate is requested for more than one related pin.

What Next

Specify only one related pin.

PEM-005

(error) Could not find requested related pin specified in get_em_max_toggle_rate command.

Description

Query using get_em_max_toggle_rate is requested for non existence related pin.

What Next

Specify a valid related pin.

PEM-006

(error) A related pin must be specified with -related_pin option in get_em_max_toggle_rate command

Description

No related pin is specified with -related_pin for the command.

What Next

Specify a valid related pin.

PEM-007

(error) PrimePower is not enabled for EM analysis.

Feedback

Description

To use any of the EM related PrimePower command, user must set the power_enable_em_analysis to true.

What Next

Set power_enable_em_analysis to true.

PEM-008

(error) Pin and related pin must be of same type.

Description

The command get_em_max_toggle_rate expects both pin and related pin to be either instance pin or library pin. User may not provide a instance pin and library pin togenther.

What Next

Specify both pin as either instance pin or library pin.

PEM-009

(error) Pin / related pin must be of leaf cell.

Description

The command get_em_max_toggle_rate expects both pin or related pin to be of leaf cell. User may not provide a hierarchical instance pin or port.

What Next

Specify leaf cell pin.

PEM-010

(error) Pin %s and related pin %s is not of same instance.

Description

The command get_em_max_toggle_rate expects both pin and related pin are of the same leaf instance. User may not provide related pin from different leaf instance.

What Next

Specify related pin from same instance.

Feedback

PEM-011

(error) Pin %s is not a %s pin.

Description

If a realted pin is used, the command get_em_max_toggle_rate expects the related pin to be a load pin and the pin to be a driver pin.

What Next

Specify related pin as load pin and pin as driver pin.

PEM-012

(warning) Could not find a transition time on pin %s, assuming a transition time to 0.0.

Description

If get_em_max_toggle_rate can not find transition time on a pin, it assumes 0.0 transition time on that pin.

What Next

User may specify desired transtion time using -transition_time option.

PEM-013

(warning) Pin %s is a dangling pin, using ceff as pin load.

Description

The get_em_max_toggle_rate command uses total load on the net connected to driver pin. If the pin is a dangling pin, effective cap on the pin is used as load.

What Next

Specify desired pin load using -output_load.

PEM-014

(error) Could not find corresponding library pin for the instance pin %s.

Description

The get_em_max_toggle_rate command expects that a library pin can be found corresponding to the given instance pin.

Feedback

What Next

Make sure the instance instantiate a library cell or use the command using library pin.

PEM-015

(error) Library pin %s and related library pin %s is not of same library cell.

Description

The command get_em_max_toggle_rate expects both library pin and related library pin are of the same library cell. User may not provide related pin from different library cell.

What Next

Specify related pin on same library cell.

PEM-016

(error) Undefined transition time on library pin.

Description

The command get_em_max_toggle_rate expects transition time to be defined if the query is made on library pin.

What Next

Specify transition time using -transition_time.

PEM-017

(error) Undefined load for library pin.

Description

The command get_em_max_toggle_rate expects load to be defined if the query is made on library pin.

What Next

Specify load using -output_load.

PEM-018

(error) No library EM data found for the given %s.

Feedback

Description

The command get_em_max_toggle_rate expects EM data to be present in the given cell library for the given pin / arc. For the given arc / pin, no library EM data found.

What Next

Use cell library with EM data.

PEM-019

(error) EM data table does not have axes of transition time and load.

Description

PrimePower expects EM data table having axes of transition time and load. If the table is two dimensional, the axes must be transition time and load. If the table is one dimensional the axis must be either transition time or load.

What Next

Use cell library with expected EM data table.

PEM-020

(error) Output pin %s does not have EM data table with load as axis.

Description

PrimePower expects EM data table having axis of load if the query is made on a output pin.

What Next

Use cell library with expected EM data table.

PEM-021

(error) Input pin %s does not have EM data table with transition time as axis.

Description

PrimePower expects EM data table having axis of transition time if the query is made on a input pin.

What Next

Use cell library with expected EM data table.

Feedback

PEM-022

(warning) IO pin %s has %s based table, but no %s is defined.

Description

For a IO pin if load based EM table is present, PrimePower expects a load to be used in query. On the other hand, if IO pin has transition time based EM table, PrimePower expects a transition to be used in the query. If required information is not present, there will be no lookup done.

What Next

User need to supply the required data.

PEM-023

(error) Cell %s has negative extrapolated max toggle rate as %f

Description

PrimePower expects a non -ve extrapolated EM max toggle rate value for an out-of-range data point in the EM table.

What Next

Use cell library with expected EM data table.

PEM-026

(error) Undefined transition time on library pin.

Description

The command get_em_max_capacitance expects transition time to be defined if the query is made on library pin.

What Next

Specify transition time using -transition_time.

PEM-028

(error) Undefined toggle rate on library pin.

Feedback

Description

The command get_em_max_capacitance expects transition time to be defined if the query is made on library pin.

What Next

Specify transition time using -toggle_rate.

PEM-031

(error) A pin must be specified for get_em_max_capacitance command

Description

No pin is specified for the command.

What Next

Specify a valid pin.

PEM-700

(error) Signal EM feature is not turned on.

Description

This error indicates that a signal EM analysis related command is called without turning on the signal EM feature.

What Next

Please turn on signal EM analysis feature in shell by set power_enable_signal_em_analysis true.

PEM-701

(error) EM rules are not loaded.

Description

This error indicates that the EM rules are not loaded.

What Next

Please load EM rules using read_em_rules command.

Feedback

PEM-702

(error) Design parasitic for signal EM analysis has not been loaded.

Description

This error indicates that the design parasitics for signal EM analysis is not loaded.

What Next

Please load parasitic using read_em_rules command. Make sure the parasitic loaded is extracted for signal EM analysis.

See Also

- read_parasitics

PEM-703

(error) Net %s has not been annotated with parasitic information.

Description

This error indicates that the parasitic for the net is not loaded. This means signal EM analysis will skip this net for any further analysis.

What Next

Please check if the parasitic file contains parasitics for the given net and load parasitic for the net.

See Also

- read_parasitics

PEM-706

(error) %s should be within 0.0-1.0 range.

Description

This error indicates that value used to set the variable is not within range 0.0-1.0.

What Next

Please set appropriate value in the range of 0.0-1.0.

Feedback

PEM-707

(error) %s should not be less than 1.0

Description

This error indicates that value used to set the variable is is less than 1.0.

What Next

Please set appropriate value not less than 1.0.

PEM-708

(error) Net %s has not been annotated physical information,

Description

This error indicates that the physical information for the net is not loaded. This means signal EM analysis will skip this net for any further analysis.

What Next

Please check if the parasitic file contains physical information for the given net and load parasitic for the net. If not, extraction needs to be done for signal EM analysis.

See Also

- read_parasitics

PEM-710

(Information) Running %s analysis...

Description

PrimePower is running signal EM analysis in the specified mode.

PEM-711

(Information) Skipping %s net %s.

Description

This information indicates that the net is skipped from analysis due to the net type as mentioned.

Feedback

What Next

Please check if net needs any fix.

See Also

- read_parasitics

PEM-713

(warning) Detailed current analysis could not be done for net %s ...

Description

Detailed current analysis was not done for the given net. This usually happen if parasitic information is missing for the net. Please check parasitic file for missing informaiton.

PEM-714

(warning) Pin %s has -ve %s slew, using 0ns slew for analysis...

Description

Signal EM analysis found -ve slew at the specified pin for the specified type of transition. Signal EM analysis will use 0ns slew for current computation for this pin for this type of transition.

PEM-715

(error) check_signal_em command is not done before this command.

Description

This error indicates that this command is used before 'check_signal_em' command is done.

What Next

Please use check_signal_em command before this command.

See Also

- check_signal_em

PEM-716

(error) Parasitic file is missing SPEF layermap informaiton.

Feedback

Description

This error indicates that the parasitic file is missing SPEF layer map section.

What Next

Please run read_parasitics with SPEF file with layer map section. read_parasitics reads layer map section and tail comments when signal em analysis is enabled. Please make sure to enable signal em analysis before running read_parasitics. The command to enable signal em analysis is "set power_enable_signal_em_analysis true"

PEM-717

(warning) No EM rule for layer number %d. Current limit calculation skipped.

Description

This warning indicates that there is no EM rule found for resistors on the reported layer number in parasitic file. Current limit calculation is skipped, since there is no EM rules on the layer.

What Next

Please check layer mapping file to make sure correct mapping between design layer names and EM rule layer names.

If layer number is 0, it's could be a short resistor generated by signal net parasitic extraction tool. Please check the tool options to avoid short resistors.

PEM-718

(warning) Failed to get voltage waveform of a driver pin %s.

Description

This warning indicates that no voltage waveform can be get from AWP (Advance waveform propagation). The reason might be no CCSN lib file or the driver pin is primary input port.

What Next

Check if the library cell of a driver pin exists in CCSN library file. Use set_driving_cell to set driver cell on primary input port.

PEM-719

(warning) no driver waveform for this net %s, using default voltage waveform to analyze EM.

Feedback

Description

This warning indicates that this net doesn't have driver voltage waveform. This net is analyzed by using driver voltage waveform with minimum or maximum slew among all signal nets. The result might be pessimistic to use driver voltage waveform with minimum slew or optimistic to use driver voltage waveform with maximum slew.

What Next

The reason why no driver voltage waveform could refer to EM-718

PEM-720

(error) ITF EM rule file is not loaded successfully.

Description

It is indicated that ITF format EM rule file is not successfully loaded into memory.

What Next

Please use read_signal_em_rules to load into memory before doing EM check. Check if it can be successfully loaded.

PEM-721

(warning) The delay_calc_waveform_analysis_mode variable should be set to "full_design" if all signal nets should be analyzed.

Description

Signal EM analysis required driver voltage waveform saved in AWP mode (Advanced waveform propagation). Set the delay_calc_waveform_analysis_mode variable to run AWP mode for full design. The delay_calc_waveform_analysis_mode variable cannot be set after linking or be reset. "set delay_calc_waveform_analysis_mode full_design"

For analyzing signal nets connected to input port, please set driver cell on input port by the "set_driving_cell" command.

What Next

Re-run update_timing to save driver voltage waveform for signal EM analysis.

PEM-722

(error) %s using temperature %g that ouside temperature derate table of EM rule file.

Feedback

Description

Both metal and via average EM rule would apply temperature derate value on EM limit value. If user temperature is outside temperature derate table, then tool would try to extrapolate a value by the two largest rating factors. If temperature derate value is smaller than 0.001, then this message is shown, and EM current ratio (current / current limit) would be considered as infinite.

What Next

adjust temperature setting and re-run signal EM analysis.

PEM-723

(warning) VIA layer=%s width=%g length=%g adopted ground rule.

Description

If a via doesn't match any EM rule by its via size, then the tool would apply EM rule of minimum via size on the same layer to the via.

What Next

adjust via size to match EM rule file and re-run signal EM analysis.

PG

PG-001

(Information) PG net %s is not connected to any top level port.

Description

The warning occurs in pg verilog or golden UPF flow when PG net is not connected to any top level port. This net will be tagged as internal net. ETM pg pin connected to this net will get direction as internal.

What Next

Check pg verilog netlist to see if the pg net connectivity is correct. Check if power switch is connected with it or not.

See Also

- enable_golden_upf

Feedback

PG-002

(Warning) PG pin %s is not connected to any pg net. It will be connected to primary supply of the power domain.

Description

This occurs in pg verilog or golden UPF flow when PG pin in verilog is not connected to any pg net. This pin will be connected to the primary supply of the power domain the cell belongs too.

What Next

Check pg verilog netlist to see if the pg pin connectivity is correct.

See Also

- enable_golden_upf

PG-003

(Warning) Power switch could not be inferred for cell %s as control pins are not connected.

Description

This occurs in pg verilog flow when power switches are present in verilog but no power switches can be inferred because the control pins are either not present or not connected to any net.

What Next

Check pg verilog netlist to see if the pg pin connectivity is correct.

PG-004

(Warning) Power switch could not be inferred for cell %s as both input and output supply nets are not connected.

Description

This warning condition occurs in the PG Verilog flow when power switches are present in Verilog but no power switches can be inferred because both input and output supply nets are either not present or not connected to power switch PG pins. The input PG pin is detected from the pg_function of the output PG pin.

What Next

Check the PG Verilog netlist to see if the PG pin connectivity is correct.

See Also

- link_keep_pg_connectivity

PG-005

(Warning) Unable to resolve internal PG pin %s to its PG function.

Description

In the PG Verilog or golden UPF flow, the PrimeTime tool was unable to resolve an internal PG pin to its PG function. This issue is likely due to a complex PG function in the library.

What Next

Check the pg_function attribute in the library for the complex PG function.

See Also

- enable_golden_upf

PG-006

(Information) Power switch not inferred for cell %s as no input or output PG pin is conected.

Description

This information occurs in the PG Verilog flow when a cell is marked as power switch in library and power switch cannot be inferred since no input and output PG pin is connected in the cell.

See Also

- link_keep_pg_connectivity

PG-007

(Warning) PG Net %s is shorted with the net %s in module %s.

Description

This message warns the user that two PG nets are shorted to each other using '=' statement in verilog. This may cause multiple supply nets to be shorted and created as one.

Feedback

See Also

- link_keep_pg_connectivity

PG-008

(Warning) Top level Nets %s and %s are considered equivalent.

Description

This message warns the user that two PG nets are considered equivalent at the top level as they may be connected in any internal hierarchies.

See Also

- link_keep_pg_connectivity

PG-009

(Error) Library cell %s is part of a scaling group; cannot disable PG pins after scaling group is defined.

Description

This error message occurs when lib_cells specified in the command *set_disable_pg_pins* already belong to any scaling lib group.

.SH "WHAT NEXT" *set_disable_pg_pins* should be used before *define_scaling_lib_group \P command.*

.SH "SEE ALSO" .nf set_disable_pg_pins(2) .fi

PG-010

(Error) %s is not a switch cell.

Description

This occurs in pg verilog flow when ignored switch is not a switch cell.

What Next

Check if a switch exists in the design.

Feedback

PLIB

PLIB-100

(warning) The direction of pin has been changed to of the corresponding cell from the %s.

Description

The pin direction in the design is inconsistent with that defined in the library.

What Next

Make sure the direction of pins from library and design are consistent.

PLIB-101

(error) The direction of pin is not consistent with that from the design!

Description

The pin direction in the design is inconsistent with that defined in the library.

What Next

Make sure the direction of pins from library and design are consistent.

PLIB-102

(error) Invalid direction for pin

Description

The pin direction of the cell defined in the library is invalid.

What Next

Check the pin direction of the cell in the library.

PLIB-103

(error) Can't find wire load model name.

Description

The wire load model name specified can not be found in Synopsys DB library.

Feedback

What Next

Check the name specified for the wire load model.

PLIB-104

(error) Can't set wire load before reading the library!

Description

set_wire_load_model command can not be used until Synopsys DB library has been read in.

What Next

Please read in the library first before use the command set_wire_load_model.

PLIB-105

(error) Can't find wire load model %s.

Description

The wire load model name specified can not be found in Synopsys DB library.

What Next

Check the name specified for the wire load model.

PLIB-106

(error) Mismatch in function definition.

Description

There is parathesis mismatching in cell function definition .

What Next

Check the integrity of the Synopsys DB library in use.

PLIB-107

(warning) Unknown function operator %c.

Description

There is unknown operator found in cell function definition.

Feedback

What Next

Check the integrity of the Synopsys DB library in use.

PLIB-108

(error) Can't find pin

Description

The pin specified in cell function can not be found in verilog cell definition.

What Next

Check the consistency between library and design.

PLIB-109

(warning) Pin

Description

The specific pin in the cell is not connected in the design netlist.

What Next

Check the consistency between the library and the design.

PLIB-110

(warning) Pin table is not specified for cell

Description

The cell pin information was not found in the design netlist.

What Next

Check the consistency between library and design.

PLIB-111

(error) Can't find power supply name

Description

The specified signal level cann't not be found in the library.

Feedback

What Next

Check the integrity of the library.

PLIB-112

(warning) Illegal direction on %s %s.

Description

The pin direction specified in the library is illegal. The possible pin direction can be: input output inout internal

What Next

Check the integrity of the library.

PLIB-113

(warning) Different directions defined for %s %s.

Description

Different directions defined for bus or bundle pins in the library.

What Next

Check the integrity of the library.

PLIB-114

(warning) No members defined for bundle %s.

Description

There is no member defined for bundle pin in the library.

What Next

Check the integrity of the library.

PLIB-115

(error) Can't find pin

Description

There is inconsistency in bundle pin definition.

Feedback

What Next

Check the integrity of the library.

PLIB-116

(error) Missing bus_type attribute in synopsys lib for bus %s!

Description

bus_type attribute is not specified for bus pin.

What Next

Check the integrity of the library.

PLIB-117

(error) Missing type group in synopsys lib for bus type %s!

Description

The specifid bus type is not defined in the library

What Next

Check the integrity of the library.

PLIB-118

(error) Can't find pin %s in bus %s!

Description

There is inconsistency in bus pin definition.

What Next

Check the integrity of the library.

PLIB-119

(warning) Can't find pin

Description

The pin specified in cell function can not be found in verilog cell definition.

Feedback

What Next

Check the consistency between library and design.

PLIB-120

(warning) in power table of cell %s!

Description

The power tables in the library are generated by power characterization tool. The when states in power table need to be mutually exclusive in order to represent power dissipation correctly during simulation.

What Next

Please verify the power characterization procedure.

PLIB-121

(warning) Illegal power template name

Description

The specified power template is not defined in the library.

What Next

Check the integrity of the library.

PLIB-122

(warning) cell=%s - size of lut values doesn't fit template %s.

Description

The size of power lut table doesn't fit the power template table.

What Next

Check the integrity of library.

PLIB-123

(warning) Illegal scaling_factors name: %s.

Description

The specified scaling_factors is not defined in the library.

Feedback

What Next

Check the integrity of library.

PLIB-124

(error) Can't find the related pin of timing group!

Description

The related pin is not specified for the timing arc. The attributes that can specify the related pin are related_pin and related_bus_pins.

What Next

Check the integrity of library.

PLIB-125

(warning) Rising and falling power table have different dimensions in cell

Description

The 3D power table is supported in PrimePower, but the rising and falling power tables have to be in the same dimension for a cell.

What Next

Adjust the power table in the library.

PLIB-126

(error) Can't find equal_or_opposite_out 3D power table in cell

Description

The equal_or_opposite_out pin can not be found in the 3D power table.

What Next

Check the integrity of library.

PLIB-127

(error) No the 3d power table in cell

Description

The equal_or_opposite_out attricute can not be found in the 3D power table.

Feedback

What Next

Check the integrity of library.

PLIB-128

(error) Can't find cell

Description

The cell is not defined in Synopsys DB library. Missing cell timing and power tables will cause inaccurate power analysis results.

What Next

Add the missing timing and power tables to the library.

PLIB-129

(warning) No %s specified in the library! Taking: %s = %g.

Description

The mentioned attribute is not specified in Synopsys DB library. PrimePower will take the default value during power simulation.

What Next

Add the attribute into the library.

PLIB-130

(error) Illegal default_operating_conditions name: '%s'.

Description

The attribute specified for default_operating_conditions is not recognizable by PrimePower. The following attributes are supported by PrimePower: process temperature voltage tree_type

What Next

Check the integrity of library. If you think that the specified attricute should be supported, please contact Synopsys support center.

Feedback

PLIB-131

(warning) Voltage from config command (%g) differs from default_operating_conditions voltage (%g) by more than 5 percent! Taking %g.

Description

The difference between default_operating_conditions voltage and nom_voltage specification is more than 5%.

What Next

Check the integrity of library.

PLIB-132

(warning) Temperature from config command (%g) differs from default_operating_conditions temperature (%g) by more than 100! Taking %g.

Description

The difference between the absolute values of default_operating_conditions temperature and nom_temperature specification is more than 100.

What Next

Check the integrity of library.

PLIB-133

(error) Illegal operating_conditions name: '%s'.

Description

The attribute specified for operating_conditions is not recognizable by PrimePower. The following attributes are supported by PrimePower: process temperature voltage tree_type

What Next

Check the integrity of library. If you think that the specified attricute should be supported, please contact Synopsys support center.

PLIB-134

(warning) Time unit synopsys library for PrimePower, use

Feedback

Description

The unit specified for time_unit is not recognizable by PrimePower. Only "ns" and "ps" are currently supported by PrimePower.

What Next

Check the integrity of library. If you think that the specified time unit should be supported, please contact Synopsys support center.

PLIB-135

(warning) Capacitance unit the synopsys library for PrimePower, use

Description

The unit specified for capacitive_load_unit is not recognizable by PrimePower. Only "ff" and "pf" are currently supported by PrimePower.

What Next

Check the integrity of library. If you think that the specified capacitance unit should be supported, please contact Synopsys support center.

PLIB-136

(warning) Voltage unit synopsys library for PrimePower, use

Description

The unit specified for voltage_unit is not recognizable by PrimePower. Only "V" and "v" are currently supported by PrimePower.

What Next

Check the integrity of library. If you think that the specified voltage unit should be supported, please contact Synopsys support center.

PLIB-137

(warning) Leakage power unit synopsys library for PrimePower, use

Description

The unit specified for leakage_power_unit is not recognizable by PrimePower. The following units are currently supported by PrimePower: mW uW nW pW

Feedback

What Next

Check the integrity of library. If you think that the specified leakage power unit should be supported, please contact Synopsys support center.

PLIB-138

(Warning) Can't find library name %s.

Description

Could not find the named library.

PLIB-139

(error) Failed to read synopsys library file.

Description

The Synopsys library name is not specified before reading in library data.

What Next

Use set link_path or target_library to specify the library to read in. For more information, please type "man link".

PLIB-140

(warning) Synopsys library file

Description

The specified library has already been read in by PrimePower. The repeating library load command will be ignored.

What Next

Check the command usage.

PLIB-141

(error) File name too long: %s.%s.

Description

The length of the library file name exceeds the limit of 1024 characters that PrimePower can currently handle.

Feedback

What Next

Rename the file with a shorter name.

PLIB-142

(error) Can't open file %s!

Description

Not able to open the specified library file for read.

What Next

Check the library name specified.

PLIB-143

(error) Operating condition %s is not defined. Using default.

Description

An operating condition is used but it is not defined in a technology library. The operating condition is specified by the command set_oprating_conditions. If the option of this command, -library, is not specified properly, e.g., the file name or library name is not correct, this error will also occur.

What Next

Check the library to make sure it is defined. Make sure that set_oprating_conditions is used correctly.

PLIB-144

(error) The '%s' library has not been read in yet.

Description

The command issued tries to access a library that does not exist in the database. The following command might trigger the generation of this error: report_lib.

What Next

Use list_libs to find all available libraries. Make sure the library name is among the ones being reported by list_libs. Please note that the library name can be different from the library filename. Load the library into the database using read_db for a db library file and then reissue the command.

MESSAGE Error: The 'cell_lib' library has not been read in yet. (SLIB-050)

Feedback

PLIB-145

(Information) PrimePower assumes that the fanout number for all the output ports be %s.

Description

Fanout number of output ports may affect the back annotation by way of wire load model. PrimePower has a default value.

PLIB-146

(Error) Operating condition as described below is used for power calculation: File : %s Library : %s Name : %s

Description

This message will help you to check if the operating conditions specified for power calculation is what you intended to set. Sometimes there could be multiple libraries read in pp_shell. And each library could have a operating conditions with the same name. By default, pp_shell will use the first one it finds. Use *-library* option of command *set_operating_conditions* to solve the ambiguity problem.

PLIB-147

(error) File

Description

The specified library needs to have .db as file extension.

What Next

Use the correct extension for synopsys DB library.

PLIB-148

(error) Unable to open DBVER files - $SYNOPSYS is not set.

Description

Need to specify environment variable $SYNOPSYS in order to access DBVER files.

What Next

Set your environment variable $SYNOPSYS to Synopsys tools' installation root directory.

Feedback

PLIB-149

(warning) Could not read library file

Description

Not able to read information from the specified library.

What Next

Check the integrity of the library.

PLIB-150

(warning) '%d' is not a valid argument type.

Description

The argument type in the library is not supported by PrimePower.

What Next

Please check the integrity of the library.

PLIB-151

(error) library name '%s' is ambiguous, use <file_name>:<library_name> to identify library

Description

The command issued tries to access a library by its name when at least another library with the same name has been read. The following command might trigger the generation of this error: report_lib.

What Next

Use <file_name>:<library_name> as the command argument represting the library, where <file_name> is the name of the file containing the required library. If you are not sure which file was used to read the required library then use list_libs -file. If libraries with the same name are read from files that also have the same name, then use the full pathname as the library filename.

MESSAGE Error: library name 'asic_lib' is ambiguous, use '<file_name>:<library_name>' to identify library (SLIB-104)

PLIB-152

(warning) Can not find library cell '%s' in technology libraries.

Feedback

Description

The specific cell is not defined in synopsys technology library. The internal power for such cell type will be zero.

What Next

Please check your read_db command. For more accurate power simulation results, a good and complete library is recommended.

PLIB-153

(warning) Can not find power table for library cell '%s' in technology libraries.

Description

The power table for the specific cell is not provided in technology library. The internal power for such cell type will be zero.

What Next

For more accurate power simulation results, a good and complete library is recommended.

PLIB-154

(warning) No library or power table in the technology library.

Description

No library is specified or no power table is found in the technology library. The internal power for the whole design will be zero. Only switching power will be reported!

Since no library is loaded, the pin capacitance may not be available. So, this could cause some error for back annotations. For example: set_load -subtract_pin_load report_wire -include_pin_cap

What Next

Please check your read_db command. For more accurate power simulation results, a good and complete library should be used.

PLIB-155

(error) No synopsys library file has been read in for reporting

Description

No synopsys library files have been read in. Need to read in libraries before reporting them.

Feedback

What Next

Please read in the libraries either using read_db or link command.

PLIB-156

(error) Could not find library '%s'.

Description

The specific library with the given name is not found in synopsys technology library.

What Next

Please check your library name. It may have been specified incorrectly. Or you may have not read the library file with the given name.

PLIB-157

(error) There are multiple libraries for the library name of '%s'.

Description

Could not find a unique synopsys library. There are multiple libraries with the same name. Do not know which library to report.

What Next

Please give the unique name of libraries while reading in the libraries.

PLIB-158

(error) Can't find cell '%s' in library '%s'.

Description

The cell is not defined in Synopsys DB library. Missing cell timing and power tables will cause inaccurate power analysis results.

What Next

Add the missing timing and power tables to the library.

PLIB-159

(warning) Do not support old internal power tables attached to cell '%s' in technology libraries.

Feedback

Description

For this release, PrimePower doesn't support old internal power tables attached to library cells in technology libraries. The internal power tables attached to library cells will be ignored. The internal power tables attached to ports will be used.

What Next

Check the integrity of library. If you think that the internal power tables attached to library cells should still be supported, please contact Synopsys support center.

PLIB-160

(Information) Do not support power calculation for DPCM library.

Description

PrimePower doesn't support power calculation for DPCM model.

PLIB-161

(Information) The power model is different from the delay model in the library.

Description

The delay and power models used in a technology library can be different. For example, you can use generic cmos delay model for timing tables and use non-linear power model for power tables in the library. Such kind of scenario is supported by PrimePower. The power model supported by PrimePower is non-linear power model (nlpm).

PLIB-162

(error) The design was not successfully linked. Please check if the link path is set and the libraries are installed properly.

Description

The design was not successfully linked. It has unresolved references.

What Next

Please check if the link path is set and the libraries are installed properly.

PLIB-163

(warning) There is neither 'related_outputs' nor 'related_input' specified under the cell-based internal power table attached to cell '%s' in technology libraries.

Feedback

Description

The old style cell-based internal power tables require either related_outputs or related_input attributes to indicate the pin which the tables belong to.

What Next

Check the integrity of library. Highly suggest switching to pin-based power model syntax.

PLIB-164

(warning) The contains only 0 or 1. Such table will be used as Non State-Dependent internal power table.

Description

The when condition of a power table should consist of valid pin states. Using constants as the when condition is not allowed.

What Next

Check the integrity of library and apply the proper when condition for the power table.

PLIB-165

(warning) The 'when' condition of a leakage power table for cell '%s' contains only 0 or 1. Such 'when' condition is ignored. This table will be used as default leakage power table.

Description

The when condition of a power table should consist of valid pin states. Using constants as the when condition is not allowed.

What Next

Check the integrity of library and apply the proper when condition for the power table.

PLIB-166

(warning) 'when' states are not mutually exclusive in internal power tables of cell '%s'!

Description

The power tables in the library are generated by power characterization tool. The when states in internal power tables need to be mutually exclusive in order to represent power dissipation correctly during simulation.

Feedback

What Next

Please verify the power characterization procedure.

PLIB-167

(warning) 'when' states are not mutually exclusive in leakage power tables of cell '%s'!

Description

The power tables in the library are generated by power characterization tool. The when states in leakage power tables need to be mutually exclusive in order to represent power dissipation correctly during simulation.

What Next

Please verify the power characterization procedure.

PLIB-168

(warning) Found overlapped rail specific internal power tables for library cell '%s'.

Description

PrimePower supports rail specific internal and leakage power tables. However, the rail specific power tables should not overlap.

What Next

Please check the integrity of the library.

PLIB-169

(warning) Found overlapped rail specific leakage power tables for library cell '%s'.

Description

PrimePower supports rail specific internal and leakage power tables. However, the rail specific power tables should not overlap.

What Next

Please check the integrity of the library.

PLIB-170

(warning) Power data can't be loaded from library file '%s'.

Feedback

Description

Libraries are loaded again to read in library power data for power analysis. However, the named library file can not be reloaded.

What Next

Please check the integrity of the library.

PLIB-171

(error) No library has been loaded for power analysis.

Description

Technology libraries are required for power analysis. Power analysis can not be continued without loading in library.

What Next

Please check the integrity of the library.

PLIB-172

(error) Power calculation can not be continued without loading in library.

Description

Technology libraries are required for power analysis. Power analysis can not be continued without loading in library.

What Next

Please check the integrity of the library.

PLIB-173

(error) Can't find pg_pin '%s' for library cell '%s'.

Description

The name specified for related_pg_pin attribute is not defined as a pg_pin for the named library cell.

What Next

Check the name specified for related_pg_pin attribute.

Feedback

PLIB-174

(warning) The internal power table for cell '%s' has related_ground_pin specified, but with no related_pg_pin specification.

Description

Distributed power tables (NLPM) are required to have related_pg_pin specification.

What Next

Check the NLPM power tables defined in the library

PLIB-175

(warning) The leakage power table for cell '%s' has related_ground_pin specified, but with no related_pg_pin specification.

Description

Distributed power tables (NLPM) are required to have related_pg_pin specification.

What Next

Check the NLPM power tables defined in the library

PLIB-176

(error) Library '%s' is not in PG pin synax. Disabling transit power analysis in PrimePower ...

Description

Transit power analysis in PrimePower provides the capability of reporting power consumption associated with ground nets (rails). As a requirement, technology library(ies) with NLPM power distribution tables in PG pin syntax must be provided.

What Next

Provide PG pin library with necessary NLPM power distribution tables for transit power analysis.

PLIB-177

(error) Missing distributed power tables for cell '%s'. Disabling transit power analysis in PrimePower ...

Feedback

Description

Transit power analysis in PrimePower provides the capability of reporting power consumption associated with ground nets (rails). As a requirement, technology library(ies) in PG pin syntax must be provided. For cells with multiple ground pins defined in the library, NLPM power distribution tables must be provided.

What Next

Provide PG pin library with necessary NLPM power distribution tables for transit power analysis.

PLIB-178

(error) Missing ground pin definition for cell '%s' in the library. Disabling transit power analysis in PrimePower ...

Description

Transit power analysis in PrimePower provides the capability of reporting power consumption associated with ground nets (rails). As a requirement, technology library(ies) in PG pin syntax must be provided. For cells with multiple ground pins defined in the library, NLPM power distribution tables must be provided.

What Next

Provide PG pin library with necessary NLPM power distribution tables for transit power analysis.

PLIB-179

(error) Can't find pg_pin '%s' for library cell '%s'.

Description

The name specified for related_ground_pin attribute is not defined as a pg_pin for the named library cell.

What Next

Check the name specified for related_ground_pin attribute.

PLIB-180

(Information) Using "zero" value for missing leakage current data in CCS Power model.

Feedback

Description

In CCS Power model, when the pg_current groups are specified, current conservation holds for every leakage_current group. If a single pg pin is omitted, the missing value can be derived. As default, the tool will derive the missing leakage value.

For complex cells with many PG Pins, it is OK to have leakage current values specified on some but not all PG pins. In this case, missing value indicates insignificant current value. When variable *power_ccsp_use_zero_for_missing_leakage* is to TRUE, the tool will use "zero" value for missing leakage data in the library.

PRECO

PRECO-001

(error) Cannot launch the executable specified by '%s.'

Description

This error message is issued when PrimeECO is not able to launch IC Compiler, Fusion Compiler, Library Manager, or StarRC executable specified by the *set_implement_options* command.

What Next

Please check if the specified path and executable is valid. You can launch the executable in a separate xterm and check if the executable is invoked successfully.

PRECO-002

(warning) Initialization already completed. Use the reset_implement_options command to re-initialize.

Description

This error message is issued when PrimeECO already completed initialization, but you intend to perform tasks that require re-initialization. Use the reset_implement_options command.

What Next

Use the reset_implement_options to reset and initialize again.

PRECO-003

(error) Parasitic corner is not set for the '%s' scenario

Feedback

Description

PrimeECO requires parasitic corner is set for each scenario in order to extract parasitics.

What Next

Please use the *set_implement_options* command to map scenarios to parasitic corners.

For example, suppose scenario S1 has corner_ss, and scenario S2 has corner_ff. The following example script shows how to set parasitic corner names.

pt_shell> set_implement_options \ -parasitic_corners { {S1 corner_ss} {S2 corner_ff} }

PRECO-004

(error) Cannot find the '%s' block from the '%s' physical library. Use the *report_eco_options* command to check if the specification is correct.

Description

This error message is issued when PrimeECO is not able find the specified block from the specified physical IC Compiler II library.

What Next

Please use the *report_eco_options* command to check if the block and IC Compiler II physical library are specified correctly.

PRECO-005

(error) Cannot find StarRC command file '%s'

Description

This error message is issued when PrimeECO is not able to locate the StarRC command file specified by the *set_implement_options* command.

What Next

Please check if the specified path and file name are valid.

PRECO-006

(error) Cannot find file '%s' specified to %s option.

Description

This error message is issued when PrimeECO is not able to locate the Tcl file specified to the *set_implement_options* command.

Feedback

What Next

Please check if the specified path and file name are valid.

PRECO-007

(error) %s failed.

Description

This error message is issued when a PrimeECO command fails to execute the named task.

What Next

Pleae review the logfile for information and prior error messages leading to the failure.

PRECO-008

(error) %s is incomplete. Run %s to complete %s.

Description

This error message is issued when a PrimeECO task cannot complete due to a required prior step that was not executed.

What Next

Please follow the instructions to ensure successful completion.

PRECO-009

(error) Cannot reset PrimeECO options because design changes have not been implemented.

Description

This error message is issued when you attempt to execute *reset_implement_options* while the design netlist has been optimized, but the physical changes have not been completed by *implement_eco*.

What Next

You can choose to discard design changes by using *reset_implement_option -force* option. Otherwise, please run *implement_eco*.

Feedback

PRECO-010

(error) Unsupported type '%s' for implementation.

Description

This error message is issued when the value specified to *set_implement_options -type* is not supported.

What Next

Please specify one of the supported values among *'netlist'*, *'wire'* or *'physical_only'*.

PRECO-011

(error) The work_dir cannot be changed once initialized.

Description

This error message is issued when you attempt to re-define *set_implement_options -work_dir* option to a new directory, after *check_eco* has completed.

Check_eco initializes the physical implementation flow by writing data in the folder specified by *-work_dir* option, hence it can not be changed.

What Next

If you really need to change work_dir location, please use *reset_implement_options* first.

PRECO-012

(error) The command is available in PrimeECO's eco_shell only

Description

This error message is issued when you attempt to run the commands that are available in *PrimeECO* and its *eco_shell* only.

What Next

Run *eco_shell* instead of *pt_shell*.

PRECO-013

(error) A fatal error has occurred and IC Compiler II features are unavailable.

Feedback

Description

This error message is issued when a fatal error has occurred and IC Compiler II features including placement legalization and ECO routing are not available.

What Next

The issue might be due to hardware issues like network glitch, disk out of space, out of memory, or other software issues like backgound process crash. Rerun the script and check if the issue is reproducible.

PRECO-014

(warning) %d nets do not have detailed parasitics annotated after implementation.

Description

This error message is issued when nets do not have annotated parasitics after the *implement_eco* command is executed. It can be caused by ECO router failure, parasitics extraction failure or mismatch between netlist and parasitics.

What Next

Review the log and identify the nets that do not have parasitics. The log shows a list nets that do not have parasitics. Investigate any routing or legalization errors in the log. Correct the issue and rerun the tool to check if the issue is addressed.

PRECO-015

(information) Advanced legalizer is not enabled in the '%s' physical block.

Description

This information message is issued when the advanced legalizer is not enabled in the physical block as a reminder to check the settings.

What Next

Check the legalization settings in the physical block are consistent with the settings used for this block during place and route implementation flow. If not consistent, apply the necessary legalization settings in the physical block.

The example below shows how to enable the advanced legalizer in *IC Compiler II*. Save the setting in the physical block and use it for subsequent *PrimeECO\P run.*

```
icc2_shell> set_app_options -name
 place.legalize.enable_advanced_legalizer -value true
```

Feedback

PRECO-016

(warning) Timing endpoint '%s' is not constrained for %s timing in hybrid views.

Description

This error message is issued when the specified endpoint is constrained in static views but cannot be constrained in live or hybrid views. For example, if live or hybrid view scenarios are all in functional mode and their test pins are unconstrained, but one of the static views is in test mode and has a violation. Then, the hybrid view cannot cover the static view because the endpoint cannot be constrained.

What Next

Use the *-include_scenarios* option of the *start_eco_scenarios* command to include the scenario that constrains the endpoint.

PRECO-017

(error) The change list has been generated for the design %s, while it is being replayed on the current design %s.

Description

The change list provided by the user has not been generated for the current design. The user should replay the change list generated for the current design.

What Next

Provide a valid change list name as input to the read_eco_changes command. Alternatively, the user can load the correct design for this change list.

PRECO-018

(warning) The '%s' net segment is a synonym net. Its net will be set dont_touch and excluded from fixing

Description

This error message is issued when the specified net segment is a synonym net to another net. It can potentially cause netlist inconsistency between the physical block and the timing session. In order to prevent such inconsistency, its net is set dont_touch to avoid any fixing for the net.

What Next

Identify why the specified net is a synonym net to another net. One of the reasons might be due to Verilog assign statement to handle a net connected to two separate output ports

or hierarchical pins. Use the *report_net -segments* command and option to examine the net in both PrimeTime and IC Compiler II.

Check if synonym nets are necessary in your design. Correct the configuration and check if both PrimeTime and IC Compiler II have consistent net segments.

PRECO-019

(error) No StarRC command file specified.

Description

This error message is issued when no StarRC command file is specified for parasitic extraction.

What Next

Please specify a valid StarRC command file using the *set_implement_options* command.

PRECO-020

(error) Found inconsistency between extraction corners defined in StarRC command file and parasitic corner(s) configured for %s.

Description

This error message is issued when extraction corners specified in StarRC command file(s) (*SELECTED_CORNERS* command) don't match with parasitic corners defined for the scenarios or the current session.

What Next

Review the *SELECTED_CORNERS* statement in StarRC command file(s) specified via *set_implement_options -starrc_cmd_files*, and make sure it is consistent with parasitic annotation corners. Parasitic annotation corners are either defined by *parasitic_corner_name* variable, or by *set_implement_options -parasitic_corners* configuration option.

The error message can also be raised when parasitic annotation corner is unspecified (eg, single corner) while StarRC command file specifies multiple extraction corners, creating an ambiguous situation.

PRECO-021

(error) Cannot reset parasitics corner to '%s' for %s, which is already annotated with previously set parasitics corner '%s'.

Feedback

Description

This error occurs during *check_eco* if the user defined the *set_implement_options -parasitic_corners* setting to attempt to change the parasitics corner while it is already set from a previous parasitics annotation operation. This is to prevent annotation of different parasitic corner values leading to an incoherent annotation.

What Next

Resetting the parasitics corner is allowed only after the annotated parasitics are removed. PrimeECO requires that multi-corner extraction setup defined in StarRC command file (specified through *set_implement_options -starrc_cmd_files*) aligns with parasitics annotation corner setup defined in scenarios. Possible actions are either:

- Reset parasitics corner in incoming PrimeTime session by rebuilding annotated parasitics and defining *parasitic_corner_name* variable so that it matches StarRC extraction corner in PrimeECO, or
- Revise corner specification in StarRC command file so that it matches annotation corner defined in scenarios.

See Also

- set_implement_options

PRECO-022

(error) IC Compiler II design library is not specified.

Description

PrimeECO requires an IC Compiler II design library to proceed with ECO physical implementation and parasitic extraction. This error is raised when no library is specified.

What Next

Please specify a valid IC Compiler II design library to *set_eco_options -physical_icc2_lib* command.

PRECO-023

(error) Invalid block name '%s'.

Description

Block name cannot contain ":", ".", "/", or empty spaces. The name of a block eventually becomes the directory name. So it cannot contain the "/" character or empty spaces. The

Feedback

":" character is used to delimit library and block names, and the "." character is used to delimit block and view names. So they cannot be in a block name either.

What Next

Remove invalid characters from block name.

PRECO-024

(information) Tuning ECO change for '%s'.

Description

This information message is issued when PrimeECO cannot meet all timing, DRC, and physical placement legalization requirements despite multiple attempts to place and legalize an insertion or resize ECO change in layout.

For example, if a buffer insertion is attempted in a dense area where all cells have critical timing, PrimeECO first tries to move cells to create space for the new buffer as long as the existing timing does not degrade. However, if the existing cells cannot be moved due to their timing criticality, PrimeECO cancels the buffer insertion to avoid timing degradation. A similar scenario applies to resize operations.

What Next

Review your ECO command options. For example, change the physical mode from *occupied_site* to *open_site*. Apply *dont_touch* to cells in dense areas or create placement blockages to avoid ECOs in those dense areas.

PRECO-025

(error) Parasitic corner is not set for the '%s' scenario. Please set parasitic_corner_name variable for this scenario.

Description

This error occurs during *read_implement_changes* when the parasitic corner name is undefined in one or more scenarios. The directory specified as argument to the *read_implement_changes* command contains multi corner parasitic data. The command requires parasitic corner name is defined for each scenario in order to annotate the correct set of parasitics.

What Next

Please set the \parasitic_corner_name variable for its corresponding scenario. For example, suppose scenario S1 has corner_ss, and scenario S2 has corner_ff. The following example script shows how to set parasitic corner names.

Feedback

```
pt_shell> current_scenario S1
pt_shell> remote_execute { set_app_var parasitic_corner_name corner_ss }
pt_shell> current_scenario S2
pt_shell> remote_execute { set_app_var parasitic_corner_name corner_ff }
pt_shell> current_scenario -all
```

See Also

- write_implement_changes

PRECO-026

(error) Parasitic corner '%s' set in scenario(s) '%s' can't be found in specified directory %s which contains parasitic data for corner(s) '%s'.

Description

This error occurs during *read_implement_changes* when there is a mismatch between:

- Parasitic corner(s) data contained in the directory specified as argument to the *read_implement_changes* command
- Parasitic corner name set for one or more scenario(s) in the current session.

The *read_implement_changes* command can't proceed with parasitic annotation for scenario(s) reported by the error message.

What Next

The directory specified as argument to the *read_implement_changes* command was generated by the *write_implement_changes -format block_to_top* command in a PrimeECO session. Please review the parasitic extraction setup of that PrimeECO session and make sure it is consistent with the parasitic annotation corner(s) of the current session.

See Also

- write_implement_changes
- read_parasitics

PRECO-100

(info) Starting %s

Feedback

Description

Starting message from implement_eco command indicating which stages of implement_eco will be run.

What Next

Information. No action needed.

PRECO-101

(info) Running %s

Description

Information of the currently running stage of implement_eco.

What Next

Information. No action needed.

PROF

PROF-001

(Information) Profiling has started. Output will be written to '%s'.

Description

Collection of data for the generation of profiling reports has started. Profiling reports will be written to the given directory.

PROF-002

(Error) TCL profiling is currently active.

Description

Profiling has already been activated.

What Next

To stop profiling, the command stop_profile can be used.

PROF-003

(Error) TCL profiling is not currently active.

Feedback

Description

Profiling has not been activated.

What Next

To start profiling, use the command start_profile.

PRPT

PRPT-095

(warning) Can't report power calculation for port '%s'.

Description

The message indicates that the port object is specified for the report_power_calculation command which is not allowed. report_power_calculation command only accepts cell, pin and net objects.

What Next

Specify the correct design objects and run the script again.

PRPT-097

(warning) Sequential cell

Description

By default, clock_network power includes the clock pin power of the registers. When different power derating factors are applied to clock_network and registers, PrimePower uses the power derating factors of clock_network to derate the clock pin power of registers when calculating clock_network power. However, when the power derating factors of registers are 0, clock_network power will ignore clock pin power from those registers.

What Next

Either set the register power derate to a non-zero value or set the clock network power derate to zero too.

PRPT-098

(warning) Cell '%s' is a constant cell. PrimePower does not calculate power for constant cells.

Description

PrimePower does not calculate power for constant cells. *report_power_calculation* command does not work for constant cells.

What Next

Please specify non-constant cell object for *report_power_calculation* command.

PRPT-099

(error) report_power_calculation command is only allowed in the activity based power analysis flow. Please set *power_analysis_mode* to *averaged*

Description

The report_power_calculation command is not allowed in the time-based power analysis flow. If *power_ui_backward_compatibility* is set to true, then the variable *power_force_saif_flow* can be set to true to cause the tool to run the activity based power analysis flow during *update_power*.

What Next

set the power analysis mode to *averaged* and re-run the command.

PRPT-100

(error) Could not get %s!

Description

The program is not able to get some necessary information for generating the power .rpt file.

What Next

Action based on the message text.

PRPT-101

(error) Run out of memory!

Description

The program is not able to allocate enough memory during report generation.

What Next

Action based on the message text.

Feedback

PRPT-102

(warning) Could not find module

Description

The program is not able to locate the specified module in the design by its name.

What Next

Please check if the instand name specified in analyze_power -inst option is a valid instance name in your design.

PRPT-103

(warning) Could not find module

Description

The program is not able to locate the specified module in the design by its name.

What Next

Please check if the instand name specified in analyze_power -inst option is a valid instance name in your design.

PRPT-104

(error) Could not open file

Description

The program is not able to open the file for reporting.

What Next

Check if you have the write permission in the current directory.

PRPT-105

(error) Could not open file

Description

The program is not able to append additional information at the end of .rpt file.

What Next

Check if the .rpt file is in the current run directory with open permission.

Feedback

PRPT-106

(error) Failed to create a signal for fsdb dumping.

Description

The program is not able to create signal handlers during power histogram generation.

What Next

Report this error to Synopsys Customer Service Center.

PRPT-107

(error) Can't report %s before reading the pif files!

Description

The design should be read first before dumping data.

What Next

Use 'read_pif' to read in the design first.

PRPT-108

(warning) Net %s does not exist!

Description

The net specified cann't be found in the design.

What Next

Check the node name specified in command 'report_net'.

PRPT-109

(error) String exceeds limit during generating file

Description

The string was too long and exceeded the buffer limit - 2048 Bytes during generating histogram report file.

What Next

Contact your local Synopsys Support Center.

Feedback

PRPT-110

(Warning) Histogram report file on simulation time %.0f ns. It was approaching the size limit: %ld bytes.

Description

The .out histogram report file will be closed if it is approaching the file size limit. No more power histogram data will be written out after that point. However, the time-based power histogram will still be calculated for the rest of simulation and peak powers will be reported in .rpt file.

The current size limit for .out file is 2GB.

What Next

There are several ways to reduce the histogram report file size:

1. use "-inst" option to select instance block(s) for power analysis 2. use "-level" option to print instances from root down to the specified level 3. use "-time" option to choose the specific time window(s) for power analysis 4. increase sampling interval to reduce the amount of data

PRPT-111

(error) Not able to get the status for file

Description

There was an error occurred during getting file size for histogram report file.

What Next

Make sure not to remove/touch the file during the run

PRPT-112

(error) Not able to create a buffered file system for

Description

The program is not able to open the file for reporting.

What Next

Contact your local Synopsys Support Center.

Feedback

PRPT-113

(error) Net name is not specified!

Description

PrimePower should be told which net to report.

What Next

Refer to man page of report_wire.

PRPT-114

(warning) Cannot report power for cell it's not covered by update_power.

Description

The cell is not covered at the power calculating stage. So there is no power to report. To set update_power coverage, refer to update_power man page, -instance option description.

What Next

Reset the power coverage and calculate power again.

PRPT-115

(error) Power is not calculated. Please run update_power before report_power.

Description

It is required that update_power be run before report_power.

What Next

Refer to man pages of update_power and report_power.

PRPT-116

(error) There is no current design specified for reporting.

Description

There is inconsistancy in the design data structure.

Feedback

What Next

Make sure the pif files are read correctly. Verify the integrity of the pif files, regenerate pif if needed.

PRPT-117

(warning) The total power is below reporting threshold of %.1f. Please check your setup.

Description

The total power of the design is less than the reporting threshold specified in report_power command (default: 0.0).

What Next

Please check your design setup and adjust the reporting threshold.

PRPT-118

(Warning) Sampling interval %g for waveform display is too small. Reset to %gns.

Description

It is required that sampling interval be no smaller than 0.01ns.

PRPT-119

(Warning) The digits after the second decimal point of sampling interval are ignored.

PRPT-120

(error) String exceeds limit during generating file "%s.out"!

Description

The string was too long and exceeded the buffer limit - 2048 Bytes during generating histogram report file.

What Next

Contact your local Synopsys Support Center.

PRPT-121

(Warning) Waveform report file "%s.out" has been closed on simulation time %.0f ns. It was approaching the size limit: %ld bytes.

Feedback

Description

The .out histogram report file will be closed if it is approaching the file size limit. No more power histogram data will be written out after that point. However, the time-based power histogram will still be calculated for the rest of simulation and peak powers will be reported in .rpt file.

The current size limit for .out file is 2GB.

What Next

There are several ways to reduce the histogram report file size:

1. use "-inst" option to select instance block(s) for power analysis 2. use "-level" option to print instances from root down to the specified level 3. use "-time" option to choose the specific time window(s) for power analysis 4. increase sampling interval to reduce the amount of data

---

PRPT-122

(Warning) Waveform report file "%s.fsdb" has been closed on simulation time %.0f ns. It was approaching the size limit: %ld bytes.

Description

The .out histogram report file will be closed if it is approaching the file size limit. No more power histogram data will be written out after that point. However, the time-based power histogram will still be calculated for the rest of simulation and peak powers will be reported in .rpt file.

The current size limit for .fsdb file is 2GB.

What Next

There are several ways to reduce the histogram report file size:

1. use "-inst" option to select instance block(s) for power analysis 2. use "-level" option to print instances from root down to the specified level 3. use "-time" option to choose the specific time window(s) for power analysis 4. increase sampling interval to reduce the amount of data

---

PRPT-123

(error) Not able to get the status for file

Description

There was an error occurred during getting file size for histogram report file.

Feedback

What Next

Make sure not to remove/touch the file during the run

PRPT-124

(warning) Mode expression is not true for the given set of vectors. Therefore, power estimation is not performed. All the power numbers will be reported to be zero.

Description

Given mode expression does not evaluate to true for the given set of vectors. Since the given mode is not excited no power will be consumed by the design.

What Next

Please check the set of vectors, and the modal condition.

PRPT-125

(Error) Cannot report power as rail sensitive command (e.g. set_current_rail or create_power_rail_mapping) has been issued after command update_power.
Please rerun update_power to recalculate power consumption data. Or you can "set pwr_force_reporting true" to generate power report anyway.

Description

This error message can be happened for a multi-rail design. Commands *set_current_rail* and *create_power_rail_mapping* can affect the power analysis results calculated by PrimePower. If any of the rail sensitive commands has been issued after command *update_power*, PrimePower will not report the power analysis results unless user has set variable *pwr_force_reporting* to be true.

What Next

1. rerun update_power to recalculate power consumption or 2. set *pwr_force_reporting* to be true to generate power report anyway.

PRPT-126

(error) No object list provided to report_power_calculation command. Please refer to command usage for more information on options.

Feedback

Description

Object list is a require argument to report_power_calculation command. Without this argument the command will not know the objects for which the power calculation information need to be reported.

What Next

Please refer to command usage for more information on options.

PRPT-127

(warning) Object '%s' does not match either port, pin, net or cell. No power calculation information will be reported.

Description

The object is neither a port, pin, net or a cell. In order to report power calculation information, object has to be one of these.

What Next

Please check if the correct object list is provided to the command.

PRPT-128

(warning) Leakage power table not found for cell: %s (%s) state: %s.

Description

No matching leakage power table was found for the specified cell with the specified state condition.

What Next

Please check if the correct options are specified in the command. Type "man report_power_calculation" to get more information on command usage.

PRPT-129

(warning) Cell '%s' is not a leaf-cell which doesn't have power table in the technology library.

Description

Only leaf-level cell object has corresponding power tables defined in technology library. The report_power_calculation command can only be issued for objects that are associated with leaf cells. This excludes reporting for hierarchical cells.

Feedback

What Next

Please specify leaf cell object for report_power_calculation.

PRPT-130

(warning) Please specify the related pin for output toggle pin %s of cell: %s (%s).

Description

If the toggle pin is an output pin, the option -path_source is required to specify the related input pin for such output toggle. The report_power_calculation command uses path source information to pick the correct internal power table and get the input transition value if needed. If the toggle pin is an input pin, option -path_source is not needed.

What Next

Please specify the related pin for the specified toggle pin through option -path_source.

PRPT-131

(warning) Related pin %s not found in cell: %s (%s).

Description

The specified related pin through option -path_source was not found in the cell.

What Next

Please check the pin name specified in option -path_source.

PRPT-132

(warning) Pin direction unknown for pin %s in cell: %s (%s).

Description

The specified toggle pin is neither input, inout, or output pin. The report_power_calculation doesn't know how to report power calculation information associated with it.

What Next

Please check the property of the pin in the design and report this error to Synopsys.

PRPT-133

(warning) Internal power table not found for cell: %s (lib cell: %s) pin: %s related_pin: %s state: %s.

Feedback

Description

No matching internal power table was found for the specified cell pin with the specified related pin and state condition.

What Next

Please check if the correct options are specified in the command. Type "man report_power_calculation" to get more information on command usage.

PRPT-134

(warning) Options -state_condition, -path_source, -rise, -fall, -negative_unateness and -verbose are not valid for net objects.

Description

The options in the above list is not valid options for net objects. They will be ignored during report_power_calculation.

What Next

Please check if the correct options are specified in the command. Type "man report_power_calculation" to get more information on command usage.

PRPT-135

(warning) Options -path_source, -rise, -fall and -negative_unateness are not valid for cell objects unless -verbose option is used.

Description

The options in the above list is not valid options for cell objects. They will be ignored during report_power_calculation.

What Next

Please check if the correct options are specified in the command. Type "man report_power_calculation" to get more information on command usage.

PRPT-136

(warning) Internal power table not found for cell: %s (lib cell: %s) pin: %s state: %s.

Description

No matching internal power table was found for the specified cell pin with the state condition.

Feedback

What Next

Please check if the correct options are specified in the command. Type "man report_power_calculation" to get more information on command usage.

PRPT-137

(information) -verbose option overwrites -state_condition option. It is equivalent to '-state_condition all -path_source all'.

Description

Once -verbose option is specified, -state_condition option will be ignored.

What Next

Type "man report_power_calculation" to get more information on command usage.

PRPT-138

(information) -verbose option overwrites -path_source option. It is equivalent to '-state_condition all -path_source all'.

Description

Once -verbose option is specified, -path_source option will be ignored.

What Next

Type "man report_power_calculation" to get more information on command usage.

PRPT-139

(error) Object '%s' is not a %s.

Description

The -only argument of the report_power command should contain a list of cells of the -cell flag is specified; a list of nets of the -net flag is specified; and a list of cells and nets if both -net and -cell are specified.

What Next

Re-invoke the command with a valid object list with the -only argument.

PRPT-140

(error) No valid %s specified.

Feedback

Description

The -only argument needs a list of cells if -cell is specified; a list of nets of -net is specified; and a list of nets and cells if both -cell and -net are specified. Note that if both -cell and -net are specified the -only argument should contain at least one cell and at least one net.

What Next

Re-invoke the command with a valid list of objects in the -only argument and with a valid combination of the -cell and -net flags.

PRPT-141

(error) No object list provided to report_activity_propagation command. Please refer to command usage for more information on options.

Description

Object list is a require argument to report_activity_propagation command. Without this argument the command will not know the objects for which the activity information need to be reported.

What Next

Please refer to command usage for more information on options.

PRPT-142

(warning) Cell '%s' is not a leaf-cell which doesn't have power table in the technology library.

Description

Only leaf-level cell object has corresponding power tables defined in technology library. The report_activity_propagation command can only be issued for objects that are associated with leaf cells. This excludes reporting for hierarchical cells.

What Next

Please specify leaf cell object for report_activity_propagation.

PRPT-143

(warning) Sampling resolution below 100fs is not supported. Resetting sampling interval from %g to %g.

Feedback

Description

Sampling resolution below 100fs is not supported.

PRPT-144

(warning) Cell '%s' is not connected to any supply net.

Description

Cell does not have any pgpin/pgnet.

What Next

Please refer to man page of the command for more information on options.

PS

PS-001

(warning) The %s will be skipped as ps_enable_analysis is set to false.

Description

It's required to set ps_enable_anlaysis to true to enable various PrimeShield features.

What Next

Set *ps_enable_analysis* to true to enable PrimeShield features.

See Also

- ps_enable_analysis

PSCR

PSCR-001

(error) PrimeShield should be enabled for cell robustness analysis.

Description

PrimeShield license is required to enable cell robustness analysis. Please set ps_enable_analysis before enabling ps_enable_save_timing_slack_data.

What Next

Please check if PrimeShield license exists.

See Also

- ps_enable_analysis

PSCR-002

(Information) ps_enable_save_timing_slack_data is changed to %s.

Description

You receive this message because you have changed ps_enable_save_timing_slack_data variable.

What Next

"This is an informational message only. No action is required on your part."

PSCR-003

(Information) ps_enable_save_timing_slack_data is changed to %s. This will %s efficient storage of timing slacks and also set timing_save_pin_arrival_and_slack to %s.

Description

You receive this message because you have changed ps_enable_save_timing_slack_data variable.

What Next

"This is an informational message only. No action is required on your part."

PSCR-004

(Warning) Skipping cell %s as number of pins (%d) is greater than the limit (%d).

Description

The cell robustness analysis will be skipped on cells with high complexity due to runtime overhead. The variable ps_cell_robustness_skip_cell_pin_limit can be used to increase the limit for skipping of cell.

Feedback

What Next

If it is acceptable to you for this cell to be excluded from the analysis, no action on your part is required.

PSCR-005

(Warning) No violated cells were found. %s

Description

The cell robustness analysis did not find any violated cells. This could happen if -slack_lesser_than setting is too restrictive.

What Next

If it is acceptable to you, try increasing the -slack_lesser_than value and re-run the analysis.

PSCR-006

(Warning) Voltage robustness analysis has detected at least one exact (or best) match scaling group. Cells with exact (or best) match will be skipped in the analysis.

Description

The define_scaling_lib_group has at least one exact (or best) match scaling group in the design. During voltage robustness analysis, any cells that only have exact (or best) match will be skipped in the analysis. The voltage robustness needs true DSLG scaling to be setup to perform analysis.

What Next

In order to perform voltage robustness analysis on the skipped cells, remove exact (and/or best) match and setup the DSLG to be true scaling groups.

PSCR-007

(Warning) Skipping cell %s as it is exact (or best) match scaling group.

Description

The voltage robustness analysis will be skipped on cells which have either exact of best match scaling group. The analysis requires true scaling in define_scaling_lib_group to be defined on the cell.

Feedback

What Next

In order to prevent cells from being skipped in voltage robustness analysis, true DSLG scaling must be defined on the cells.

PSCR-008

(Information) %d cells were skipped due to -slack_margin limit.

Description

The cell robustness analysis will be skipped on cells where the input pin timing slack is above the -slack_margin specified in the command. The default -slack_margin is infinity (i.e. no cell is filtered).

PSCR-009

(error) The -delay_type min is not supported for voltage robustness analysis.

Description

The min (or hold) analysis is not supported for voltage robustness. The IR drop increases delay on data paths (in general) and makes hold constraint easier to satisfy. So, unlike -delay_type max, performing voltage robustness for -delay_type min is not useful in identifying weak cells that are sensitive to IR drop.

See Also

- report_cell_robustness
- report_voltage_robustness

PSCR-010

(Warning) For -delay_type %s the shift_ratio (%f) is %s. It is recommended to use a %s shift ratio.

Description

For cell robustness analysis, when -delay_type max is used, the shift ratio should be positive i.e. an increase in the parameter is considered to identify weak cells that can cause potential setup timing violations. Similarly, when -delay_type min is used, a negative shift ratio should be used i.e. a decrease in parameter in order to identify weak cells on hold paths.

Feedback

What Next

Change the sign of the shift_ratio and rerun the report_cell_robustness analysis.

PSCR-011

(Information) %d out %d %s skipped in %s cell robustness analysis%s.

Description

The number of skipped cells out of the total number of cells searched is presented. The cell robustness analysis will be skipped with some reasons (referred on the message PSCR-012).

PSCR-012

(Information) %d %s skipped %s.

Description

The cell robustness analysis will be skipped on cells due to the reasons. This message shows the number of skipped cells and the reason for skipping are expressed.

PSCR-013

(warning) Delay impact (%f) is lesser than 0. [Cell: %s, From Pin: %s, To Pin: %s]

Description

In Cell robustness and voltage robustness, related information is reported when the pin-to-pin delay impact of a specific cell is smaller than 0.

PSCR-014

(warning) Timing slack (%f) is lesser than robustness slack (%f) for the case of positive timing slack. [Cell: %s, From Pin: %s, To Pin: %s]

Description

When the timing slack is positive, timing slack of a specific cell is lesser than the robustness slack.

PSCR-015

(warning) The %s option will be ignored; it applies only for %s.

Feedback

Description

In cell robustness analysis, only consistent sub-options are allowed according to specific -type.

PSCR-016

(Information) Running variation robustness in %s mode using report_sigma(%.2f) and high_sigma(%.2f) values.

Description

This describes whether variation robustness analysis is running in HSFR or robustness slack mode and what values are being used for report_sigma and high_sigma.

What Next

"This is an informational message only. No action is required on your part."

PSCR-017

(error) Hypergrid and distributed STA are currently not supported for cell robustness analysis.

Description

The Hypergrid and distributed STA features are currently not supported for cell robustness analysis. Please run cell robustness analysis with Hypergrid flow disabled.

See Also

- ps_enable_analysis

PSCR-018

(error) The hier %s was not found; please check if name is specified correctly.

Description

In cell robustness analysis, the hierarchical blocks specified with the variable "ps_cell_robustness_only_analyze_hiers" need to be valid names of blocks that exist in the current design.

PSCR-019

(information) The current top design (%s) was found in ps_cell_robustness_only_analyze_hiers setting. All cells in current top design were added for analysis.

Description

In cell robustness analysis, the hierarchical blocks specified with the variable "ps_cell_robustness_only_analyze_hiers" contain the name of current top design. All cells in current design will be added for analysis. Check if this was as intended.

PSCR-020

(error) No cell were found in the cell table. Analysis is skipped.

Description

There were no cells found in the cell table and the cell robustness analysis is skipped. Please check the -cells {}, the $paths or the setting of ps_cell_robustness_only_analyze_hiers variable.

See Also

- ps_enable_analysis

PSCTPM

PSCTPM-001

(Warning) An extrapolation exceeding %.2fX of library perturbation range has been detected on parameter %s%s.

Description

You receive this message because extrapolation out of parameter pertrubation range in sensitivity library has been detected.

What Next

For PrimeShield Project Sicily CTPM based flow, up to 2X extrapolation in physical parameter can be tolerated without accuracy concern. If the extrapolation is wider than that, the augmented library characterization range for parameter with extrapolation could be too tight, it will need to be widened and re-characterized. If library characterization

Feedback

range of parameter is wide enough and this message shows on all parameters, please check if there is any setup error.

PSCTPM-002

(Error) %s cannot be empty list.

Description

You receive this message because list is empty.

What Next

Check to ensure that focus_param_names or attributes are correct.

PSCTPM-003

(Error) %s param_names "%s" doesn't exist in %s.

Description

You receive this message because parameter names in focus_param_names do not exist.

What Next

Check if the parameter names in focus_param_names list exist in sensitivity side-file libraries, or related to BEOL layer. Modify the focus_param_names with the correct parameter names.

PSCTPM-004

(Error) Attribute "%s" is not defined%s.

Description

You receive this message because the attribute set by the *-attr* option of the *gen_ctpm* command is not defined for any lib cell, or because the attribute value is not set even though the attribute is defined.

What Next

Check the defined attributes by setting the -class option of the *list_attributes* command to lib_cell. If the attribute is not defined, define the attribute to be used with the *define_user_attribute* command as lib_cell. If it is defined, set the value of that attribute with the *set_user_attribute* command.

Feedback

See Also

- list_attributes
- define_user_attribute
- set_user_attribute

PSCTPM-005

(Error) Total number of attributes%s allowed for %s is %d.

Description

You receive this message because total number of attributes exceeds the limit of CTPM generation attribute requirement.

What Next

Check the total number of attributes set by the -attr option of the gen_ctpm command and modify it so that it does not exceed the limit.

PSCTPM-006

(Error) %slib_cell attribute "%s" for CTPM%s must be int/float/string.

Description

You receive this message because *gen_ctpm -attr* option only accepts lib_cell attributes with int, float or string types.

What Next

When defining a lib_cell attribute to be used in *gen_ctpm -attr* option, make sure the data type for attribute in *define_user_attribute* command to be int, float, or string.

See Also

- define_user_attribute

PSCTPM-007

(Error) No lib_cell has attribute "%s", please double check.

Description

You receive this message because none of the lib_cells has one of the attributes specified in attr_list used in *gen_ctpm -attr attr_list*.

Feedback

What Next

Attributes of lib_cell can be checked using *list_attribute* command. Fix typo in attr_list used in *gen_ctpm -attr attr_list* if there is any. Or define attributes on lib_cell as needed to do user-defined grouping of lib_cells in gen_ctpm. The process can be done by *define_user_attribute* and *set_user_attribute* commands.

See Also

- define_user_attribute
- set_user_attribute

PSCTPM-008

(Information) %spower supply voltage = %f, temperature = %f.

Description

This message informs the voltage and temperature of the training data for CTPM.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-009

(Error) read_ctpm already loaded, please reset_ctpm first.

Description

You receive this message because you have already consumed CTPM using read_ctpm command when attempting to create CTPM.

What Next

If you have previously used the read_ctpm command before using the gen_ctpm command, you must use the reset_ctpm command to remove the effects of CTPM.

PSCTPM-010

(Error) Multiple input files require %s.

Description

You receive this message if there is no voltage and temperature info in the multiple input files of CTPM or if the voltage and temperature values in each input file are different from each other.

Feedback

What Next

You should check that the voltage and temperature are correctly configured in CTPM's input files. Additionally, the voltage and temperature values in all input files must be indentical.

PSCTPM-011

(Warning) Only %d data points available for learning with %d parameters. Please include more data points to improve accuracy.

Description

You receive this message when the training data points used in Machine-Learning driven CTPM generation is smaller than the number of parameters required for learning. More data points are recommanded to have robust enough learning outcome.

What Next

To improve CTPM's accuracy, it is recommended to increase the number of training data points.

PSCTPM-012

(Information) CTPM is generated based on %s.

Description

This message informs you about what CTPM is based on.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-013

(Information) %sabs(mean)+3sigma error%s: pre-CTPM = %f,%s post-CTPM (est) = %f.

Description

This message informs you the error before CTPM and the error after CTPM.

What Next

This is an informational message. No action is required NEXT.

Feedback

PSCTPM-015

(Error) No %sdata loaded%s%s%s.

Description

You receive this message when the input files have not been loaded correctly.

What Next

If you intend to use golden CSV file as input, please check if the input option has been used and confirm that the correct file has been loaded.

PSCTPM-016

(Error) Conflict of input CTPM files. %s already defined as %g.

Description

You receive this message when there are duplicate parameters within the input CTPM files specified in "input_file_list" of *-input input_file_list*.

What Next

Check for duplicate parameters within the input CTPM files used, correct them and try again.

PSCTPM-017

(Error) pattern/attribute among CTPM files are not consistent.

Description

You receive this message when the patterns and attributes in the input CTPM files are not consistent across each files.

What Next

Adjust the pattern and attribute names with the input CTPM files to make them consistent.

PSCTPM-019

(Error) Spice2Design flow is not enabled.

Description

You receive this message when *ps_enable_spice2design_analysis* is not *true*, which is required for the feature you are running.

Feedback

What Next

Set the *ps_enable_spice2design_analysis* to true and retry.

PSCTPM-020

(Information) Loaded CTPM files for %s%s.

Description

This message informs the purpose of the CTPM files.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-025

(Warning) %s for %s already defined%s, skip duplicated %s.

Description

You receive this message when input file contains multiple same perturbation values or information.

What Next

Please check the multiple same perturbation values or informations in the input file and retain only one perturbation value or information while removing the others.

PSCTPM-027

(Information) %sCTPM saved at %s.

Description

This message informs you with the file where CTPM is saved.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-028

(Warning) Invalid data point for %s.

Feedback

Description

You receive this message in *gen_ctpm* Spice2Design basic CTPM generation flow when there is no matching arrival time for each label in the input file used for learning.

What Next

Please check that the arrival time for each label is correctly specified in the input file you have used, and if there are any mismatched lines, make the necessary corrections.

PSCTPM-029

(Error) No valid input data.

Description

You receive this message when *gen_ctpm* basic Spice2Design CTPM generation input file doesn't have any data.

What Next

Please make sure to correctly specify the label and arrival time within the input file you have used.

PSCTPM-030

(Information) %d %slearning data point read for learning.

Description

This message informs you of the number of data points read from the input file used for learning.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-031

(Error) pin/port %s doesn't exist.

Description

You receive this message when *gen_ctpm* input file contains a pin/port name doesn't exist in design.

What Next

Please make sure to correctly specify the pins/ports within the input file you have used.

Feedback

PSCTPM-032

(Error) rf "%s" in wrong format, must be rise or fall.

Description

You receive this message since only "rise" and "fall" are acceptable format for rf column of input file.

What Next

The rf should be specified as "rise" or "fall" within the input file you have used. Please make the necessary corrections.

PSCTPM-034

(Warning) Learning failed%s.

Description

You receive this message when the learning process to create CTPM fails.

PSCTPM-035

(Information) All lib_cells are in same bin, can be learned together without binning.

Description

This message informs you when all lib_cells in CTPM command with silicon2design type are grouped into the same bin.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-036

(Warning) parasitics_enable_tail_annotation needs to be TRUE to load BEOL parameters.

Description

You receive this message if there is a BEOL parameter among the device parameters used in gen_ctpm command, and *parasitics_enable_tail_annotation* variable is not set to TRUE.

What Next

When using the gen_ctpm command with BEOL device parameters, you should set the *parasitics_enable_tail_annotation* variable to TRUE.

PSCTPM-037

(Warning) Design doesn't have layer %s, %s skipped in CTPM.

Description

You receive this message when using the gen_ctpm command and there are metals in the loaded list that are not used in the design. In such cases, CTPM will not be generated for thoes metals, and they will be skipped.

What Next

Chek the loaded metal list and the list of metals used in the design when using gen_ctpm command, and make adjustment accordingly.

PSCTPM-040

(Error) lib_cell attributes based CTPM setup failed.

Description

You receive this message when the format of pattern is not correctly setup, or atttributes specified for learning is incorrect.

What Next

Check the defined attributes by setting the -class option of the *list_attributes* command to lib_cell. After removing the incorrect attribute using the *remove_user_attribute* command, define the correct attribute using the *set_user_attribute* command.

See Also

- list_attributes
- remove_user_attribute
- define_user_attribute

PSCTPM-041

(Error) %s does not have enough attributes defined in mapping.

Feedback

Description

You receive this message when using *gen_ctpm* command with spice configuration for basic CTPM generation with user defined attribute based grouping, the number of attributes in the loaded mapping file is not enough (v.s. the attributes specified in -attr option).

PSCTPM-042

(Error) "%s" is not a valid lib_cell name in available libraries.

Description

You receive this message when using *gen_ctpm* command with spice config flow, and the library cell used in the loaded mapping file is not found within the library.

What Next

Please check that the lib cell in the mapping file is correctly set and make adjustments if necessary.

PSCTPM-043

(Error) %s should always be in CTPM.

Description

You receive this message when using *gen_ctpm* command with spice configuration, the default device parameter is not available in generated CTPM. It should never happen. And fatal will be triggered for your attention.

What Next

Please file PrimeShield STAR if you see this error.

PSCTPM-045

(Error) CTPM not available%s%s.

Description

You receive this message when there is no content in the loaded CTPM file, making the CTPM file unusable.

What Next

Please check if the loaded CTPM file is properly configured.

Feedback

PSCTPM-046

(Error) Parameter count not consistent between bin 0 and bin %d for %s.

Description

You receive this message because here is a discrepancy in the number of parameters within each bin of the loaded CTPM file.

What Next

Please check whether each bin in the loaded CTPM file has the same parameter list and make the necessary corrections.

PSCTPM-047

(Error) %s doesn't exist bin 0 param_name_list.

Description

You receive this message due to a specific parameter is missing in one of the bins within the loaded ML-CTPM file.

What Next

Please check whether bin in the loaded CTPM file has the same parameter list and make the necessary corrections.

PSCTPM-048

(Error) %s required%s%s.

Description

You receive this message due to the absence of required data for *gen_ctpm*.

What Next

Please review the setup used in *gen_ctpm* and fix as needed.

PSCTPM-049

(Error) Could not find base library.

Description

This message indicates base library is needed for CTPM generation.

Feedback

What Next

Please make sure there are base library specified for the focused CTPM generation.

PSCTPM-050

(Error) Type in CTPM (%i) not consistent with user file_type input (%i)

Description

You receive this message because the type specified for the file_type option in the CTPM file does not match with the type of the loaded CTPM file.

What Next

Set the file_type option to match the type of the loaded CTPM file.

PSCTPM-051

(Error) Wrong user file_type is given.

Description

You receive this message when using the file_type option is wrong. Please fix the setup.

PSCTPM-052

(Error) Please provide a valid file_type.

Description

You receive this message when using the command with an invalid type set for the file_type option.

PSCTPM-055

(Error) Line is not split by ": ", "%s".

Description

You receive this message if in the spice_config file of the *gen_ctpm* command, there is a line that is not split by ": " with the name and context.

What Next

Modify your spice_config file to be split by colons as shown is the example below.
S2D_HEADER: header_file ...

Feedback

PSCTPM-056

(Error) spice_config format error "%s".

Description

You receive this message when a format error occurs in the spice config file used in *gen_ctpm* command.

What Next

Correctly modify the spice config file based on the cause of the issue.

PSCTPM-057

(Error) %sMAPPING_FILE is required in spice_config file.

Description

You receive this message because there is no mapping file in the spice config file used in *gen_ctpm* command.

What Next

In the spice config file, a mapping file is required, which sets the RO spice decks to RO name mapping.

PSCTPM-058

(Error) Mapping_file in spice_config %s.

Description

You receive this message when a format error occurs in the mapping file defined in spice config file of *gen_ctpm* command.

What Next

Correctly modify the mapping file based on the cause of the issue.

PSCTPM-059

(Error) Spice deck %s in the mapping file %s.

Description

You receive this message when a format error occurs in the mapping file specified in spice config file of *gen_ctpm* command.

What Next

Correctly modify the mapping file based on the cause of the issue.

PSCTPM-060

(Information) Please check to make sure the command is consistent with file %s/existing_cmd_file.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-061

(Warning) %s does not have side-file defined, skipped in CTPM.

Description

You receive this message when using the *gen_ctpm* for Silicon2Design ML-CTPM generation, but some base libraries lack a side-file.

What Next

Verify that the side-file is properly defined before use and define it correctly in dsml_file which is expected to contains*define_sensitivity_lib_mapping* for all base libraries.

PSCTPM-063

(Information) Start CTPM generation%s.

Description

This message notifies that CTPM generation starts when the *gen_ctpm* command is used.

What Next

This is an informational message. No action is required NEXT.

See Also

- gen_ctpm

PSCTPM-064

(Error) Spice config file is not set up successfully.

Feedback

Description

You receive this message when setup of the spice_config option fails in *gen_ctpm* command.

What Next

Check whether the spice config file loaded with the spice_config option is properly defined, and whether the context is with correct format.

PSCTPM-065

(Error) Cannot find %s.

Description

You receive this message when there is no measurement value for a certain path after performing HSPICE simulation when using *gen_ctpm* command.

What Next

Check the spice deck provided for each RO is correct and without header file included, check if there is any hspice licensing related error.

PSCTPM-066

(Warning) Parameter %s for %s sensitivity is zero, it might be expected if vt classes do not match.

Description

This message indicates the parameter does not have any impact on focused spice measurement of the RO spice deck.

What Next

This warning can be ignored if parameter is in a different vth class than the lib_cell used in current spice deck. Otherwise, please double check if the SPICE parameter sepcified in PERTURB_LIST in spice config file is correct.

PSCTPM-067

(Error) %s simulation results has no sensitivity for all parameters, please double check.

Feedback

Description

You receive this message when there is no sensitivity for all parameters after performing SPICE simulation when using *gen_ctpm* command. Machine learning cannot be done without any training data.

What Next

Please double check the per RO spice deck and parameter perturbation list provided in spice configuration file.

PSCTPM-068

(Error) user_param_names and user_param_values length mismatch (%d v.s. %d).

Description

You receive this message when the number of lists loaded in the user_param_names option and the user_param_value option used to set the parameters you will use during spice_config learning in *gen_ctpm* does not match.

What Next

Check whether the number of device parameters set in the user_param_names option and the number of values of each device parameter set in the user_param_value option are mapped correctly and then modify them.

PSCTPM-069

(Error) "%s" in user_param_names but missing in focus_param_names.

Description

You receive this message when both "-focus_param_names" and "-user_param_names" options are specified, but some parameter in user_param_names are missing in focus_param_names.

What Next

If focused_param_names option exist, parameters in user_param_names needs to be in focused_param_names list. After checking the device parameter lists set in the user_param_names option and focus_param_names option, modify the device parameter lists of user_parameter_names so that they can all be set in the focus_param_names option.

Feedback

PSCTPM-070

(Error) %s does not have sensitivity data.

Description

You receive this message if there is no sensitivity data in the library or if there is a device parameter without sensitivity data among the parameters set with *gen_ctpm -user_param_names*.

What Next

Check if there is sensitivity data in the side file, and check if there is any typo in parameter names covered by *gen_ctpm -user_param_names* option.

PSCTPM-071

(Warning) %s exists multiple times in list. Using first one.

Description

You receive this message when there are duplicate parameters in the device parameter list set in the -user_param_names option when using *gen_ctpm* command.

What Next

If there are duplicate device parameters in the device parameter list set with the user_param_names option, remove them, leaving only one.

PSCTPM-072

(Error) %sarc %s in lib %s %s.

Description

You receive this message when you try to set the nldm value in the library and arc already has a golden value. Or, in case of constraint arc, you receive this message when trying to set it as the trainsition value.

What Next

You cannot set the nldm value if the library arc already has a golden value. Or cannot set the value as a transition value if the library arc is a constraint arc.

PSCTPM-073

(Information) Trying to redefine %s %sbin %d for lib %s. Overwriting.

Feedback

Description

This message informs when you are setting the CTPM value of a specific bin which already has a CTPM value. Last one wins.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-074

(Error) lib %s doesn't have CTPM assigned.

Description

You receive this message when you try to complete user-defined CTPM related action but there is no ML-CTPM defined on library.

What Next

Please double check script and fix related setup.

PSCTPM-075

(Error) Golden indices vector is empty.

Description

This message indicate golden indices selection is empty.

What Next

Please double check run script and fix golden indices selection accordingly.

PSCTPM-076

(Warning) arc %s in lib %s doesn't have arc_id in CTPM.

Description

You receive this message if the arc in the library does not have an arc_id in CTPM.

What Next

Check if the arc exists in the library and CTPM.

PSCTPM-077

(Information) Library %s sensitization data.

Feedback

Description

This message informs the presence or absence of sensitization data in the library when using the *gen_ctpm* command.

What Next

This is an informational message. No action is required NEXT.

See Also

- gen_ctpm

PSCTPM-078

(Error) Wrong arc name: %s.

Description

You receive this message when using the *read_ctpm* or *report_ctpm* command if there is an incorrect arc name in the loaded CTPM file.

What Next

Check the arc names in the loaded CTPM file and use the CTPM file with the correct arc name.

See Also

- read_ctpm
- report_ctpm

PSCTPM-079

(Error) Cannot find base library name%s in CTPM file.

Description

You will receive this message if the base library associated with CTPM file is not used in design. Or there is no base library name specified in CTPM file.

What Next

Check whether CTPM file trying to be read/report is the correct only.

See Also

- read_ctpm
- report_ctpm

PSCTPM-080

(Error) bin_id = %d doesn't have any CTPM value.

Description

You receive this message when using the *read_ctpm* or *report_ctpm* command if there is no CTPM value at a specific bin in the loaded CTPM file.

What Next

Check if the CTPM is generated correctly without any error/warning. *gen_ctpm* run setup may need to be fixed.

See Also

- gen_ctpm
- read_ctpm
- report_ctpm

PSCTPM-081

(Information) %sCTPM for base library %s %s.

Description

This message notifies the start and end of loading the CTPM file during *read_ctpm* or *report_ctpm* command.

What Next

This is an informational message. No action is required NEXT.

See Also

- read_ctpm
- report_ctpm

Feedback

PSCTPM-082

(Information) Already have %sCTPM for lib %s. Overwriting.

Description

If there are multiple *read_ctpm* commands for the same library, the last one wins.

What Next

This is an informational message. No action is required NEXT.

PSCTPM-083

(Information) CTPM values for %s.

Description

This message informs the CTPM value report for rise or fall starts here.

What Next

This is an informational message. No action is required NEXT.

See Also

- report_ctpm

PSCTPM-084

(Information) Scheduling simulation run for %s, %d spice decks.

Description

This message informs you how many spice decks there are when running the simulation in *gen_ctpm* command.

What Next

This is an informational message. No action is required NEXT.

See Also

- gen_ctpm

PSCTPM-085

(Information) %s run directory = %s.

Feedback

Description

This message informs the run directory of simulation when using the *gen_ctpm* command.

What Next

This is an informational message. No action is required NEXT.

See Also

- gen_ctpm

PSCTPM-086

(Information) %s is the user_param_names.

Description

This message informs what the user_param_names is when writing the spice deck when using the *gen_ctpm* command. user_param_name is the same as the parameter list loaded with the user_param_names option when using the *gen_ctpm* command.

What Next

This is an informational message. No action is required NEXT.

See Also

- gen_ctpm

PSCTPM-087

(Information) %s write out for spice simulation, with %d sweep samples %s.

Description

This message informs the spice deck written for simulation when using the *gen_ctpm* command, and how many samples there are in the spice deck.

What Next

This is an informational message. No action is required NEXT.

See Also

- gen_ctpm

Feedback

PSCTPM-088

(Error) Cannot find job id %d in job table.

Description

You receive this message if simulation cannot be performed because a specific job ID cannot be found when simulating spice decks generated from *gen_ctpm* command.

See Also

- gen_ctpm

PSCTPM-089

(Information) job_id = %d, spice simulation results are from dir %s.

Description

This message informs the directory of the spice simulation results of the job_id when simulating the spice decks written using the *gen_ctpm* command.

What Next

This is an informational message. No action is required NEXT.

See Also

- gen_ctpm

PSCTPM-090

(Error) %s not available. Please check reason in %s/%s.

Description

You receive this message when the simulation result file does not exist after simulating a written spice deck when using the *gen_ctpm* command. The simulation failed and the result file does not exist in the corresponding path.

What Next

Check the simulation log file to determine the cause of failure.

See Also

- gen_ctpm

Feedback

PSCTPM-091

(Error) There are %s in %s.

Description

You receive this message when there is a failed result in the simulation result file after simulating a spice deck in *gen_ctpm* command.

What Next

Check the simulation log file to determine the cause of the failure.

See Also

- gen_ctpm

PSCTPM-092

(Error) job %d not simulated.

Description

You receive this message when the job_id is not simulated.

What Next

Check the simulation log file to determine the cause of failure.

See Also

- gen_ctpm

PSCTPM-093

(Error) File %s %s.

Description

You receive this message when using the *gen_ctpm* command if certain file needed to generate CTPM doesn't exist or the file is empty.

What Next

Check whether the file exists and is empty.

See Also

- gen_ctpm

Feedback

PSCTPM-094

(Warning) %s: spice base/lib %s %s vs. lib number error = %s > 3%.

Description

You receive this message when the error between the measurement base delay/transition value of spice simulation and the delay/transition value of the base library exceeds 3% when using the *gen_ctpm* command. It usually inidcate base spice header/subckt specified in gen_ctpm is not consistent with base library characterization setting.

What Next

Please follow-up with base library characterization team to fix the setting. Or remove base spice header/subckt from *gen_ctpm* command option.

See Also

- gen_ctpm

PSCTPM-095

(Warning) Due to sim failure in golden, fall back %s for %s.

Description

This message indicate fall back for the arc happens since spice simulation failure on the arc.

What Next

No further action required unless it causes accuracy degradation.

See Also

- gen_ctpm

PSCTPM-096

(Error) lcell %s no bin_id coverage! Need to manually define attribute for library %s.

Description

You receive this message when a specific lib_cell doesn't belong to any bins in gemerated CTPM for one library.

What Next

Ignore if this is expected, or use attributed based learning/global learning for lib_cells without MLCTPM coverage.

See Also

- gen_ctpm

PSCTPM-201

(Warning) SPICE simulation (%s) failed on arc %s.

Description

You receive this message when SPICE simulation fails for that arc in *gen_ctpm* or *validate_ctpm*.

What Next

When this message occurs on a given library timing arc, PrimeShield uses CTPM values from “closest-match” library timing arc with validate golden SPICE simulation results. “Closest-match” is determined using metrics including arc sense, rise/fall transition, CCSN arc type, base NLDM table values, sensitivity table values, etc.

If there are only a few of them, the closet match solution usually gives accurate enough solution and no need of further action.

If a lot of this warnings happen, check the SPICE simulation log file to determine the cause of failure and see if there is any setup related issue.

See Also

- gen_ctpm
- validate_ctpm

PSCTPM-202

(Warning) Invalid SPICE measurement (%s) on arc %s.

Description

You receive this message when the SPICE measurement, which is the result of SPICE simulation, is invalid in *gen_ctpm* or *validate_ctpm*.

What Next

When this message occurs on a given library timing arc, PrimeShield uses CTPM values from “closest-match” library timing arc with validate golden SPICE simulation results. “Closest-match” is determined using metrics including arc sense, rise/fall transition, CCSN arc type, base NLDM table values, sensitivity table values, etc.

If there are only a few of them, the closet match solution usually gives accurate enough solution and no need of further action.

If a lot of this warnings happen, check the SPICE simulation log file to determine the cause of failure and see if there is any setup related issue.

See Also

- gen_ctpm
- validate_ctpm

PSCTPM-203

(Error) Parameter %s perturbation in library is 0.0, which should not happen. Please fix sensitivity side file library.

Description

You receive this message when the perturbation of the parameter in the augmented library loaded in the side_file option using the *gen_ctpm* command is 0.0.

What Next

Check whether the perturbation value of the parameter in the loaded augmented library is 0.0. Augmented libraries with tables with a perturbation value of 0.0 cannot be used.

See Also

- gen_ctpm

PSCTPM-204

(Error) No base_lib/side_file available in -config_file

Description

You receive this message when there is no base_lib/side_file available config_file to generate bundle of scripts/folders (one per library) for *gen_ctpm* run. The format of config_file is base_lib_abs_path side_file_abs_path [lib_cell_list] lib_cell_list is optional, only needed if you only want to cover a few lib_cells (for pipeclean purpose).

Feedback

What Next

Fix config file and retry.

See Also

- gen_ctpm

PSCTPM-205

(Error) %s doesn't exist. Please fix config_file

Description

You receive this message when base_lib or side_file absolute path specified in config_file doesn't exist. The format of config_file is base_lib_abs_path side_file_abs_path [lib_cell_list] lib_cell_list is optional, only needed if you only want to cover a few lib_cells (for pipeclean purpose).

What Next

Fix config file and retry.

See Also

- gen_ctpm

PSCTPM-206

(Warning) subckt file %s doesn't exist. Simulation will fail for %s

Description

You receive this message in *gen_ctpm* since subckt file is missing.

What Next

If it's intended that some lib_cells doesn't have subckt, you can ignore. Otherwise, please provide subckt files for all lib_cells in library, or there is no CTPM value on all arcs of that lib_cell, which will cause mis-correlation in CTPM consumption flow.

See Also

- gen_ctpm

Feedback

PSCTPM-207

(Error) %s has less than %d words.

Description

You receive this message when there is required words in configurating file per line.

What Next

Fix config file and retry.

See Also

- gen_ctpm

PSCTPM-300

(Information) No CTPM to reset for %s.

Description

This message informs that no CTPM file is loaded right now. No need to do reset_ctpm.

What Next

This is an informational message. No action is required NEXT.

PSLIB

PSLIB-001

(Warning) %s %s doesn't exist in side file.

Description

You receive this message because certain type of data is missing in side-file.

What Next

Please check sensitivity side-file for the missing data and fix it.

PSLIB-002

(Warning) %s %s doesn't exist in original library.

Feedback

Description

You receive this message because certain type of data exists in side-file but not in original library.

What Next

Please check if extra data in side-file is intended.

PSLIB-003

(Warning) %s sensitivity loading failed for %s.

Description

You receive this message because certain type of data in side-file has problem and cannot be loaded.

What Next

Please check details in sensitivity data and fix it.

PSLIB-004

(Warning) Sensitivity of %s for %s is missing in side file.

Description

You receive this message because sensitivity of certain type of data is missing.

What Next

Please check side-file for the missing sensitivity data and fix it.

PSLIB-005

(Warning) Sensitivity of %s %s is all zero in side file.

Description

You receive this message because sensitivity of certain type of data is all zero.

What Next

Please check side-file for the zero sensitivity data and see if it's expected. Common reason of zero sensitivity could be typo in physical parameter name.

Feedback

PSLIB-006

(Warning) Pin-based CCST receiver model %s doesn't exist in side file for %s/%s.

Description

You receive this message because CCST receiver model in side-file has problem.

What Next

Please check CCST receiver model in sensitivity side-file and fix it if needed.

PSLIB-007

(Warning) Inconsistent nominal %s table values found at %s.

Description

You receive this message because inconsistent nominal table values in base library and side-file are found. Side-file characterization may not use consistent setting with base library, and it may cause inaccuracy.

What Next

Please check side-file characterization setting.

PSLIB-008

(Warning) Inconsistent indices found for arc %s.

Description

You receive this message because table index is not consistent for arc in base library and side-file.

What Next

Please revisit side-file characterization setting.

PSLIB-100

(Warning) CCSN Compensation failed for arc %s at [%d, %d] (%s_%s).

Description

You receive this message because CCSN compensation based on calibrated CCSN data from CTPM or PVT Explorer failed. PrimeShield still tries to get best possible CCSN

Feedback

compensation. You may ignore this message if gap between target and base SPICE model is not too big.

PSLIB-101

(Warning) Arc %s %s NLDM table is not monotonic at %s.

Description

You receive this message because NLDM table for an arc is not monotonic. If you are trying to validate PT v.s. PT accuracy v.s. a target library, the non-monotonic part of table may cause accuracy loss.

PSLLE

PSLLE-001

(Warning) Overlay file has duplicated definition at file %s line %d for the corner, this line will be ignored.

Description

Local Layout Effect (LLE) overlay side file definition is based on cell namd and TR number, this warning means the same definition(same cell name and same TR number) has already been defined for the same corner. This line's duplicated definition will be ignored.

What Next

Check and correct the lle overlay side files.

PSLLE-002

(warning) The check_eco command should be executed before update_timing. LLE aware timing calculation will be ignored.

Description

This message is issued when local layout effect (LLE) analysis is enabled and update_timing command is executed without executing the check_eco command. To check the timing considering the LLE influence, user must first run check_eco command and then run the update_timing command.

Feedback

PSLLE-003

(warning) The check_eco command should be executed before executing the command report_lle_coverage.

Description

This message is issued when local layout effect (LLE) analysis is enabled and report_lle_coverage command is executed without executing the check_eco command.

PSPR

PSPR-018

(warning) Clock only Vt mistracking analysis is not performed.

Description

The *vt_mistracking_enable_clock_only_analysis* is set to true for clock only Vt mistracking analysis. However, the path collection doesn't contain the clock path segments. So clock only Vt mistracking analysis is skipped. Only bounding analysis is performed if *vt_mistracking_enable_bounding_analysis* is true.

What Next

Please specify full_clock or full_clock_expanded for *-path_type* option in *get_timing_paths*.

See Also

- get_timing_paths
- vt_mistracking_enable_bounding_analysis

PSPR-019

(warning) No valid Vt types can be found, and Vt mistracking analysis is skipped.

Description

Vt mistracking analysis is not performed because no cells with valid vt types can be found in the input paths. This warning message can be triggered when any one of the following scenarios happens:

- The command *set_vt_mistracking_derate* is not set properly.
- The paths don't have any Vt cells that are specified in *set_vt_mistracking_derate*.

Feedback

- The paths don't have clock cells for clock only Vt mistracking analysis.
- No clock cells after CRP point on the same edge CRP path for clock only Vt mistracking analysis.

What Next

Please check *set_vt_mistracking_derate* and *get_timing_paths* commands to see whether any scenario listed above could happen.

See Also

- set_vt_mistracking_derate
- get_timing_paths

PSPR-101

(Information) interconnect skew analysis is enabled.

Description

You receive this message because you have enabled interconnect skew analysis.

What Next

"This is an informational message only. No action is required on your part."

PSPR-102

(warning) Interconnect skew analysis is not performed when -path_type full_clock_expanded is not specified.

Description

Interconnect skew analysis is only available for *-path_type full_clock_expanded* report.

What Next

To enable interconnect skew analysis, specify the *-path_type full_clock_expanded* option on *get_timing_paths*.

See Also

- get_timing_paths

Feedback

PSPR-103

(error) PrimeShield should be enabled for interconnect skew analysis.

Description

PrimeShield license is required to enabled interconnect skew analysis.

What Next

Please check if PrimeShield license exists.

PSPR-104

(error) get_timing_path found that there are no SPEF in the design.

Description

No SPEF information in interconnect skew analysis.

What Next

Please check read_parasitics if spef is loaded successfully.

See Also

- get_timing_paths

PSPR-105

(error) set_parasitics_range has not been issued before interconnect skew analysis.

Description

set_parasitics_range has not been issued before interconnect skew analysis.

What Next

Add set_parasitics_range before get_timing_path.

See Also

- get_timing_paths

PSPR-106

(error) There is no layer information in interconnect skew analysis.

Feedback

Description

No layer information in interconnect skew analysis.

What Next

Add tail annotation in spef.

See Also

- get_timing_paths

PSPR-107

(error) report_path_robustness can not found interconnect skew analysis results on the path.

Description

Interconnect skew analysis has not been performed on the path.

What Next

Perform interconnect skew anaylsis before using report_path_robustness.

PSPR-108

(warning) report_path_robustness can not show verbose information on the path from restore_timing_paths.

Description

save_timing_paths does not support saving verbose information. And verbose information is not available to restore_timing_paths command.

What Next

Perform interconnect skew anaylsis on this path before using report_path_robustness verbose mode.

PSPR-109

(error) set_parasitics_range referred to the scaling factors that cannot be negative.

Description

Interconnect skew analysis does not support the negative scaling factor.

Feedback

What Next

Set the scaling factor greater than 0.

See Also

- set_parasitics_range

PSPR-110

(error) set_parasitics_range referred to two scaling factors in the option are required.

Description

Interconnect skew analysis requires two scaling factors in the option.

What Next

Add two scaling factors in the option.

See Also

- set_parasitics_range

PSPR-111

(error) set_parasitics_range referred to the scaling factors that cannot be greater than 1, less than 1 at the same time.

Description

Interconnect skew analysis requires one of the scaling factors greater than 1, and the other one is less than 1.

What Next

Set one of the scaling factors to be greater than 1, and the other one to be less than 1.

See Also

- set_parasitics_range

PSPR-112

(error) set_parasitics_range referred to a layer <layer_name> that can not be found in the spef.

Feedback

Description

No data found about this layer in the design.

What Next

Check the layers in the design again and set the correct layer.

See Also

- set_parasitics_range

PSPR-113

(error) Interconnect skew analysis should be enabled.

Description

Interconnect skew analysis is required to enable this function.

What Next

Please enable interconnect skew analysis.

PSPR-114

(error) parasitics_enable_tail_annotation should be enabled for interconnect skew get_timing_path.

Description

parasitics_enable_tail_annotation is required to enable before callling interconnect skew get_timing_path.

What Next

Set parasitics_enable_tail_annotation to true and call get_timing_path again.

See Also

- get_timing_paths

PSPR-115

(warning) "-beol" is not specified when getting path collection, potentially causing longer runtime of interconnect skew analysis.

Feedback

Description

When the path collection is for interconnect skew analysis, we can specify "-beol" in the regular get_timing_path to collect paths with interconnect skew setup. This setup can reduce interconnect skew analysis runtime on this path collection.

What Next

set "-beol" in the regular get_timing_path when the path collection is going to perform interconnect skew analysis.

See Also

- get_timing_paths

PSPR-116

(error) set_parasitics_range referred to the scaling factors that cannot be the same.

Description

Interconnect skew analysis requires one of the scaling factors greater than 1, and the other one less than 1.

What Next

Set one of the scaling factors to be greater than 1, and the other one to be less than 1.

See Also

- set_parasitics_range

PSPR-117

(error) Parasitics margin meanshift flow is disabled by interconnect skew.

Description

Interconnect skew bounding flow cannot work with parasitics margin meanshift flow.

What Next

Remove set_parasitics_derate -*factor or turn off timing_enable_parasitics_margin.

PSPR-118

(error) The layer name '%s' could not be found in the layer map. The corresponding set_parasitics_range will be ignored.

Feedback

Description

The layer name specified with the -layers option, does not match any layer name loaded from the parasitics file.

What Next

Check the layer names described in the parasitics file and make sure the layer name specified matches one of these layers.

See Also

- read_parasitics
- set_parasitics_range

PSPR-119

(error) The layer '%s' in the hierarchy '%s' already has a parasitics range set. The corresponding set_parasitics_range will be ignored.

Description

The layer specified with the -layers option, already has a parasitics range set, in the hierarchy specified with the -objects option.

What Next

Check for *set_parasitics_range*(2) commands in the setup scripts that set a parasitics range for the same layer in the same hierarchy.

See Also

- set_parasitics_range

PSPR-120

(error) The specified cell '%s' is not a hierarchical cell. The corresponding set_parasitics_range will be ignored.

Description

The cell specified with the -objects option, is not a hierarchical cell, and only hierarchical cells are considered dies.

What Next

Check the name of the cell specified and make sure it corresponds to a hierarchical cell in the design.

Feedback

See Also

- set_parasitics_range

PSPR-121

(error) The interconnect skew PBA analysis for -delay_type max will be disabled when the interconnect skew hold-only GBA flow is enabled.

Description

When interconnect_skew_enable_gba_hold_only_analysis is set to true, the setup (or -delay_type max) timing is same as nominal timing. Running interconnect skew PBA analysis (interconnect_skew_enable_path_analysis true) in this flow is not recommended as PBA results will not be bound by GBA results. Therefore, interconnect skew PBA analysis will be disabled in this scenario.

What Next

Interconnect skew PBA analysis for -delay_type max is disabled when interconnect skew hold-only GBA is enabled.

PSPR-122

(error) Interconnect skew analysis does not support "pba_derate_only" flow.

Description

Interconnect skew analysis requires the variable "pba_derate_only" to be false to continue analysis.

What Next

Set "pba_derate_only" to false before running ISA.

PSPS

PSPS-018

(Error) %s already loaded, cannot co-exist with %s.

Description

You receive this message when there is already CTPM or PVT explorer loaded in design.

Feedback

What Next

Please do *reset_ctpm* if you need to switch from CTPM to PVT Explorer flow. Or do *reset_pvt_explorer_condition* if you need to switch from PVT Explorer to CTPM flow.

PSPS-021

(Information) Clean up existing %s.

Description

This message informs the process of cleaning existing data.

What Next

This is an informational message. No action is required NEXT.

PSPS-022

(Error) %svalue%s '%s' is not float%s.

Description

You receive this message if the voltage, temperature, or perturbation values in the input file for *read_ctpm* or *set_pvt_explorer_condition* command are not of type float.

You could also receive this message in *gen_ctpm* command if the perturbation value in the spice_config file is not a float, or arrival time in input file is not of type float.

What Next

Depending on the command you have used, please check that the voltage, temperature, perturbation value or arrival time in the input files are of type float and make the necessary adjustments to use float values.

PSPS-023

(Error) Invalid line "%s", need %d columns, but have %d columns.

Description

You receive this message when the number of header columns in the loaded input file does not match the number of columns required in the command.

What Next

Please check whether the number of header columns in the input files match the required number of columns, and make necessary adjustments to ensure they are the same.

Feedback

PSPS-024

(Warning) More than one header line (starts with #), first one will be used.

Description

You receive this message when loaded input file contains multiple header lines.

What Next

Please check the header lines in the input file used and retain only one header line while removing the others. These comamands use the header line from the first row.

PSPS-026

(Information) Load file %s successfully.

Description

This message informs you of the successfully loaded file.

What Next

This is an informational message. No action is required NEXT.

PSPS-033

(Information) %s = {%s}.

Description

This message informs you the attributes/pattern used in PVT Explorer or CTPM.

What Next

This is an informational message. No action is required NEXT.

PSPS-038

(Information) Only first sample is used in PVT Explorer GBA based flow.

Description

This message informs you that in the PVT Explorer GBA flow, only the data loaded from the first sample as input file is being used.

What Next

This is an informational message. No action is required NEXT.

Feedback

PSPS-039

(Error) %s %s is not correct format%s.

Description

You receive this message due to format of file/attribute/pattern is incorrect.

What Next

Please double check and fix setup as needed.

PSPS-044

(Information) lib %s has %sexisting side file%s.

Description

This message informs you that *define_sensitiivty_lib_mapping* is done on a library already have side-file.

What Next

This is an informational message. No action is required NEXT.

PSPS-053

(Information) %sPVT Explorer condition loaded%s.

Description

This message informs you about the status of loading the PVT Explorer condition when using the *set_pvt_explorer_condition* command.

What Next

This is an informational message. No action is required NEXT.

PSPS-101

(ERROR) Arc %s is in design but is missing in %s MLCTPM.

Description

You receive this message because this arc is in design but is missing in MLCTPM.

What Next

Please check if CTPM for this arc is set.

Feedback

PSPS-102

(Warning) Arc %s is not in design and is missing in %s MLCTPM.

Description

You receive this message because this arc is not in design and is missing in MLCTPM.

What Next

Please check if CTPM for this arc is set.

PSPS-103

(Warning) Arc %s/%s in lib is not linked in the design.

Description

You receive this message because this arc is not in design.

What Next

Please check if thia arc is in design.

PSW

PSW-090

(warning) Replace %s with %s in set_switching_activity

Description

Some options in set_switching_activity will be phased out in the next release. This warning indicates the first reported option should be replaced by the second. See set_switching_activity man page.

What Next

Check your script and replace the reported option.

PSW-100

(warning) Can not find instance "%s" in the design. Ignoring the switching information of nets/ports under this instance.

Feedback

Description

The instance got from the SAIF file can not be found in the netlist provided by the user. Therefore, the switching information (probability and toggle count present in SAIF file) of the nets/ports, hierarchically under this instance can not be asserted. The read_saif will ignore this instance cand continue to read the switching information of other instances.

What Next

Make sure that strip name given by option -instance_name is correct. Also, if the SAIF file is used for the wright design.

PSW-101

(error) Can not find top level cell. Aborting reading SAIF file.

Description

SAIF file reader asserts the switching information on the i instances/nets/ports which are hierarchically either at the same or lower level than the top level cell. Since, SAIF reader can not find the top level cell (or current design) it can not find the elements of the design and hence can not assert switching information.

What Next

Make sure that the correct netlist is read and also the correct top level design is set using the command current_design. Also, check if the SAIF file is used for the wright design.

PSW-102

(warning) Design name from SAIF file "%s" and top level design name from netlist "%s" are not same.

Description

The design name from the header of the SAIF file and the top level design name of the netlist does not match. The SAIF reader will ignore the design name from SAIF file and will keep on reading the SAIF file with the top level design name from netlist as the correct one.

What Next

Make sure that the correct netlist is read for this SAIF file. Also, check if the SAIF file is used for the wright design.

Feedback

PSW-103

(warning) Direction of SAIF file is not "backward". Please make sure if correct SAIF file is read.

Description

The direction of SAIF file is other than backward. PrimePower reads only backward SAIF file. Assuming the direction to be backward and continue to read the SAIF file.

What Next

Check if reading the correct SAIF file.

PSW-104

(warning) SAIFVERSION is "%s". Supported versions are "%s". Please check if the correct SAIF file is used for this design.

Description

The version of the SAIF file is different from the supported versions. This is not a cause of concern. Just letting the user know if they using the proper application to generate the SAIF file.

What Next

Check if reading the correct SAIF file.

PSW-105

(warning) Can not open file "%s" for reading. Please provide the correct file name.

Description

The file can not be open for reading.

What Next

Check if reading the correct SAIF file.

PSW-106

(warning) Time unit is not provided in SAIF file. USing default time unit of "%s".

Feedback

Description

Time unit is not defined in SAIF file. This time unit denotes the unit of the simulation time. Therefore, will assume the default time unit.

What Next

Check if the SAIF file was generated correctly.

PSW-107

(error) Time unit "%s" provided in SAIF file is wrong. It must be one of "ns", "us", "ms", "ps", "s", and "fs".

Description

Time unit defined in SAIF file should be one of "ns", "us", "ms", "ps", "s", and "fs". Can not resolve the time unit, hence the SAIF reader can not continue.

What Next

Check if the SAIF file was generated correctly.

PSW-108

(error) Time unit scale factor of "%d", provided in SAIF file is wrong. It must be one of "1", "10", and "100".

Description

Time unit scalar factor defined in SAIF file should be one of "1", "10", and "100". Not able to resolve the time unit scale factor, therefore can not continue reading SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-109

(error) Simulation time duration "%f" provided in SAIF file is zero or negative. Please check the SAIF file.

Description

The duration of simulation time period defined in SAIF file is zero or negative. The simulation time period must be greater than zero. The SAIF reader will stop reading SAIF file.

Feedback

What Next

Check if the SAIF file was generated correctly.

PSW-110

(warning) Instance "%s" is hierarchical. Can not put state and path dependent switching information on the instance.

Description

The state and path dependent switching information can only be put on the non-hierarchical (leaf-level) instances. In order to put state and path dependent switching information SAIF reader requires power table information from the technology library cell. Since, the instance is hierarchical, it is not mapped to any technology library cell. The SAIF reader will ignore the switching information for state and path, and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-111

(warning) Instance "%s" does not map to technology cell in the library. Can not put state and path dependent switching information on the instance.

Description

In order to put state and path dependent switching information on a instance SAIF reader requires power table information from the technology library cell. Since, the instance is not mapped to any technology library cell, this information is not available. The SAIF reader will ignore the switching information for state and path, and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-112

(error) Program run out of memory.

Description

No more memory available.

Feedback

What Next

Reduce the size of your design and run the tool again.

PSW-113

(warning) For instance "%s", can not find power table in technology library associated with pin "%s", having when condition "%s". Hence, switching information will not be asserted for this power arc.

Description

In order to put state and path dependent switching information on a instance SAIF reader requires power table information from the technology library cell. Since, the SAIF reader is not able to find the power table associated with the given pin, it can not assert switching information for this power arc. The SAIF reader will ignore the switching information for the power arc and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-114

(warning) For instance "%s", can not find pin "%s" in the design.

Description

Can not find the pin, therefore switching information on the pin will not be asserted. However, the SAIF reader will continue to read the SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-115

(warning) For instance "%s", can not find pin "%s" in technology library.

Description

Can not find the pin in the techonlogy library cell to which the instance is mapped to, therefore switching information on the pin will not be asserted. However, the SAIF reader will continue to read the SAIF file.

What Next

Check if the SAIF file was generated correctly.

Feedback

PSW-116

(warning) For instance "%s", can not find power arc in technology library associated with target pin "%s", and related pin "%s", having when condition "%s". Hence, switching information will not be asserted for this power arc.

Description

In order to put state and path dependent switching information on a instance SAIF reader requires power table information from the technology library cell. Since, the SAIF reader is not able to find the power table associated with the given target and related pin, it can not assert switching information for this power arc. The SAIF reader will ignore the switching information for the power arc and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-117

(warning) Can not find the local net for pin "%s". Hence, switching information is not asserted on the pin.

Description

Internally in the SAIF reader the switching information for a pin/port is stored on the net to which this pin is connected to. Since, this pin is not connected to any net, the SAIF reader will ignore the switching information for the pin. However it will continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-118

(warning) Can not find the global net for pin "%s". Hence, switching information is not asserted on the pin.

Description

Internally in the SAIF reader the switching information for a pin/port is stored on the net to which this pin is connected to. Since, this pin is not connected to any net, the SAIF reader will ignore the switching information for the pin. However it will continue to read other switching information in SAIF file.

Feedback

What Next

Check if the SAIF file was generated correctly.

PSW-119

(error) Pin "%s", has both state and path dependent switching information. It can have only one of these two.

Description

In a technology library cell a pin can have only one of: state dependent (SD), path dependent (PD), or state and path dependent (SDPD) power table. However, this pin has two or more of the above combination. Since, this scenario should not happen, the SAIF reader can not assert switching information on the pin and will stop reading SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-120

(warning) Can not find the global net for net "%s". Hence, switching information is not asserted on the net.

Description

Internally in the SAIF reader the switching information for a net is stored on the global net to which this net is connected to. Since, this net is not connected to any global net, the SAIF reader will ignore the switching information for the net. However it will continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-121

(warning) Can not find net/pin "%s" in the design. Hence, can not assert switching information on net/pin.

Description

Can not find the net/pin, therefore switching information on the net/pin will not be asserted. However, the SAIF reader will continue to read the SAIF file.

Feedback

What Next

Check if the SAIF file was generated correctly.

PSW-122

(warning) Virtual instance "%s" does not map to technology cell in the library. Can not assert switching information on the nets/ports of the instance.

Description

In order to put switching information on a instance SAIF reader requires instance to be mapped to technology library cell. Since, the virtual instance is not mapped to any technology library cell, this information is not available. The SAIF reader will ignore the switching information for this virtual instance, and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-123

(warning) Virtual instance "%s" is hierarchical. Can not assert switching information on the nets/ports of instance.

Description

The virtual instance defined in SAIF file has to be non-hierarchical. Since, the instance is hierarchical, the SAIF reader will ignore the switching information for net/ports of instance, and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-124

(warning) Virtual instance "%s" is defined to be sequential in SAIF file. However, it is mapped to non-sequential cell in technology library. Hence, switching information is not asserted on nets/ports of this instance.

Description

There is a mismatch bewtween the virtual instance defined in SAIF file and what it has been mapped to in technology library. Therefore, the SAIF reader will ignore the switching

Feedback

information for net/ports of instance, and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-125

(warning) Virtual instance "%s" is defined to be tri-state in SAIF file. However, it is mapped to non tri-state cell in technology library. Hence, switching information is not asserted on nets/ports of this instance.

Description

There is a mismatch bewtween the virtual instance defined in SAIF file and what it has been mapped to in technology library. Therefore, the SAIF reader will ignore the switching information for net/ports of instance, and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-126

(warning) For instance "%s", can not find leakage power table for state with when condition "%s". Hence, not asserting switching information for this state.

Description

In order to put switching information on leakage state of a instance, SAIF reader requires power table information from the technology library cell. Since, the SAIF reader is not able to find the power table associated with the given leakage state, it can not assert switching information on this leakage state. The SAIF reader will ignore the switching information for the leakage state and continue to read other switching information in SAIF file.

What Next

Check if the SAIF file was generated correctly.

PSW-127

(error) RTL object name is not given. Please provide RTL object name by using -rtl option.

Feedback

Description

RTL object name is required parameter for set_rtl_to_gate_name command. Without RTL object name the command will not know one of the mapping parameter between RTL object and gate level object.

What Next

Please provide RTL object name by using -rtl option.

PSW-128

(error) Gate level object name is not given. Please provide gate level object name by using -gate option.

Description

Gate level object name is required parameter for set_rtl_to_gate_name command. Without gate level object name the command will not know one of the mapping parameter between RTL object and gate level object.

What Next

Please provide gate level object name by using -gate option.

PSW-129

(error) Gate level object Therefore, will not be able to set mapping bewteen RTL and gate level objects.

Description

Gate level object can not be found in the netlist. Without gate level object the command will not know one of the mapping parameter between RTL object and gate level object.

What Next

Please check if correct gate level object name is provided.

PSW-130

(error) No switching activity has been annotated.

Description

No switching activity has been annotated. It could be the name of the instance of the current design given by option -strip_path is incorrect, the time window specified by -time is out of range, the VCD file is EVCD, or VCD has syntax errors.

Feedback

What Next

Please check SAIF/VCD file, make it's not EVCD, have correct syntax, and -strip_path and -time are correct.

PSW-131

(error) No object list provided to get_switching_activity command. Please refer to command usage for more information on options.

Description

Object list is a require argument to get_switching_activity command. Without this argument the command will not know the objects for which the switching activity information need to be retrieved.

What Next

Please refer to command usage for more information on options.

PSW-132

(warning) Object "%s" does not match either port, pin, net or a cell. Therefore, will not be able to retrieve switching activity information.

Description

The object is neither a port, pin, net or a cell. In order to retrieve switching activity information, object has to be one of these. The command will return value of -2 for toggle rate, glitch rate, and static probability, to indicate this.

What Next

Please check if the correct object list is provided to the command.

PSW-133

(warning) Need to provide state condition by using -state option, if path condition is provided using -path option.

Description

If path condition is provided using -path option, then state condition should also be provided using -state option. Using -path option indicate that user is interested in getting state dependent path dependent switching activity information. The command will return value of -2 for toggle rate and glitch rate to indicate this.

Feedback

What Next

Please provide state condition with -state option and run the command again.

PSW-134

(warning) -rise|-fall options only work when state condition is provided by using -state option. Ignoring -rise|-fall options.

Description

The transition edge type can be rise or fall. Therefore either -toggle_rate or -glitch_rate option should be provided as rise or fall is associated with a transition. Moreover, rise or fall transition values can be different only for state condition toggle or glitch rates. On a simple net/pin the number of rise and fall transitions will be equal. Hence, for a net/pin number of rise and fall transitions can be computed by dividing toggle rate or glitch rate by 2. Therefore, for -rise|-fall option to make sense, state condition should be provided. If -rise|-fall option is true and state condition is not given -rise|-fall options will be ignored.

What Next

Please refer to man page of the command for more information on options.

PSW-135

(warning) Can not get net connected to the pin "%s". Therefore, will not be able to retrieve switching activity information.

Description

For a pin switching activity information is stored on the net to which it is connected to. Since, the pin is not connected to any net, the switching activity information for this pin can not be retrieved. The command will return value of -2 for toggle rate, glitch rate and static probability to indicate this.

What Next

Please check if the correct pin object is provided to the command.

PSW-136

(warning) Pin "%s" is a port. A port can not have state condition associated with it.

Feedback

Description

Pin is a port and a port can not have state condition associated with it. Therefore, the switching activity information can not be retrieved for the given state condition. The command will return value of -2 for toggle rate and glitch rate to indicate this.

What Next

Please check if the correct pin object is provided to the command.

PSW-137

(warning) Instance "%s" is hierarchical. Can not retrieve state and path dependent switching activity information from the instance.

Description

State and path dependent switching activity information is present only on non-hierarchical instances. Since, this instance is hierarchical the switching activity information can not be retrieved for the given state and path conditions. The command will return value of -2 for toggle rate and glitch rate to indicate this.

What Next

Please check if the correct instance object is provided to the command.

PSW-138

(warning) Instance "%s" does not map to technology cell in the library. Can not retrieve state and path dependent switching information from the instance.

Description

State and path dependent switching activity information is present only on non-hierarchical instances. This non-hierarchical instance should be mapped to a technology cell in the library to associate state and path conditions. Since, this instance is not mapped to technology cell, the switching activity information can not be retrieved for the given state and path conditions. The command will return value of -2 for toggle rate and glitch rate to indicate this.

What Next

Please check if the correct instance object is provided to the command.

Feedback

PSW-139

(warning) Can not find power arc for pin "%s" associated with "%s" state condition. Therefore, can not retrieve switching activity information.

Description

The power arc associated with the state condition for the given pin can not be found from the technology library. Therefore, can not retrieve switching activity information for the given state condition. The command will return value of -2 for toggle rate and glitch rate to indicate this.

What Next

Please check if the correct pin object and state condition are provided to the command.

PSW-140

(warning) For instance "%s", can not find pin with name "%s". Therefore, can not retrieve switching activity information.

Description

The pin with the given name can not be found in the netlist. Therefore, can not retrieve switching activity information for the given pin. The command will return value of -2 for toggle rate and glitch rate to indicate this.

What Next

Please check if the correct pin name is provided to the command.

PSW-141

(warning) For instance "%s", can not find power arc from pin "%s",to pin "%s" with "%s" state condition. Therefore, can not retrieve switching activity information.

Description

The power arc for the given state condition and source and sink pins can not ne found in the technology library. Therefore, can not retrieve switching activity information for the state condition. The command will return value of -2 for toggle rate and glitch rate to indicate this.

What Next

Please check if the correct state condition and pin objects are provided to the command.

Feedback

PSW-142

(warning) None of the options -toggle_rate, -glitch_rate, or -static_prob are true. By default assuming all three options to be true.

Description

Since, none of the options are true, default is to print all the three values if present.

What Next

Please refer to man page of the command for more information on options.

PSW-143

(warning) For instance "%s", need to provide state condition by using -state option.

Description

When the cell object is provided to the command, the intend of user assume to be retrieving static probability on leakage state condition. Therefore, state condition needs to be provided. If the user want to print static probability for default when condition please use -state "default" option.

What Next

Please refer to man page of the command for more information on options.

PSW-144

(warning) For instance "%s", can not find leakage power table for state with state condition "%s". Hence, can not retrieve switching activity information for this state.

Description

The leakage power arc for the given state condition can not ne found in the technology library. Therefore, can not retrieve switching activity information for the state condition. The command will return value of -2 for toggle rate and glitch rate to indicate this.

What Next

Please check if the correct state condition and instance objects are provided to the command.

PSW-145

(error) Need to specify values of toggle rate and glitch rate together. Can not set one value at a time.

Feedback

Description

The toggle rate and glitch rate can not be set separately. This is a requirement of the command.

What Next

Please provide both values and run the command again. See command man page for more information.

PSW-146

(error) Glitch rate is negative. Should be >= 0.

Description

The glitch rate is defined as (# of glitch transitions) or (# of glitch transitions)/(simulation time in library time unit), depending upon if period/clock is not provided or provided, respectively. From the definition, it is clear that minimum number of glitch transitions can be 0.

What Next

Please provide correct value of glitch rate and run the command again.

PSW-147

(error) Toggle rate is negative. Should be >= 0.

Description

The toggle rate is defined as (# of glitch free transitions) or (# of glitch free transitions)/(simulation time in library time unit), depending upon if period/clock is not provided or provided, respectively. From the definition, it is clear that minimum number of glitch free transitions can be 0.

What Next

Please provide correct value of toggle rate and run the command again.

PSW-148

(error) Static probability value should be >=0 and <= 1.0.

Description

Static probability is defined as the (one time of signal)/(simulation time). In other words it is defined as the fraction of time the signal is at logic state 1 (or high). From the definition

it is clear that maximum and minimum values signal probability can have is 1.0 and 0.0 respectively.

What Next

Please provide correct value of signal probability and run the command again.

PSW-149

(error) State condition should be provided if path condition is provided using -path option. Please provide state condition using -state option.

Description

If path condition is provided using -path option, then state condition should also be provided using -state option. Using -path option indicate that user is interested in getting state dependent path dependent switching activity information, and for this state condition should also be provided.

What Next

Please provide state condition using -state option and run the command again.

PSW-150

(error) Rise ratio value should be >=0 and <= 1.0.

Description

Specifies the ratio of rise transitions to total transitions for the specified toggle/glitch rate with annotating pins that are characterized with both rise and fall internal power. The ratio_value argument is a floating point number between 0.0 (all transitions are falling) and 1.0 (all transitions are rising). You need to specify a toggle rate in order to use this option. The default value is 0.5.

What Next

Please provide correct value of rise ratio and run the command again.

PSW-151

(error) The value of period provided is negative. Should be > 0.

Description

Specifies the time period for which the number of transitions given by the -toggle_rate tr_value and -glitch_rate gr_value occur; When this argument is used, the tr_value/

Feedback

gr_value are divided by the given period value. It is clear from the definition that the period should be greater than 0.

What Next

Please provide correct value of period and run the command again.

PSW-152

(error) -hier option works only when select types are provided using -select option.

Description

-hier option specifies that all the objects in all the hierarchy that satisfy the selection criteria will be annotated. It can be used only with the -select argument.

What Next

Please provide select types using -select argument and run the command again. Please refer to command man page for more information.

PSW-153

(error) -instance option works only when select types are provided using -select option.

Description

-hier option specifies that all the objects in the given list of instances that satisfy the selection criteria will be annotated. It can be used only with the -select option.

What Next

Please provide select types using -select argument and run the command again. Please refer to command man page for more information.

PSW-154

(error) At a time can provide either select types or object list.

Description

The object list option for explicitly specifying the objects to be annotated, and the -select option for implicitly specifying the objects to be annotated, are mutually exclusive. They can not be specified together.

What Next

Please provide either select types using -select option or object list, and run the command again. Please refer to command man page for more information.

Feedback

PSW-155

(error) Neither object list or select types are provided. Please provide one of them and run the command again.

Description

Either the object list for explicitly specifying the objects to be annotated, or the select types for implicitly specifying the objects to be annotated, should be provided. .

What Next

Please provide either select types using -select option or object list, and run the command again. Please refer to command man page for more information.

PSW-156

(error) Both period and clock name are provided using -period and -clock options respectively. Can provide only one of them at a time.

Description

Both -period and -clock options specifed the time period for which the number of transitions occur. Therefore, if both options are specified the command will not know which period to use. Hence, can specify either -period or -clock options, not both.

What Next

Please use only one of -period or -clock options, and run the command again. Please refer to command man page for more information.

PSW-157

(error) More than one clock is provided. Multiple clocks are not supported.

Description

More than one clock is provided using -clock option. If nore than one clocks are provided, the command will not know which clock period should be used. Therefore, only one clock should be provided by -clock options.

What Next

Please provide only one clock name using -clock options, and run the command again. Please refer to command man page for more information.

Feedback

PSW-158

(error) Can not find the clock with name "%s".

Description

Can not find the clock with the given name.

What Next

Please provide correct clock name using -clock options, and run the command again. Please refer to command man page for more information.

PSW-159

(error) Period of the clock "%s" is 0. Please provide different clock.

Description

Time period of the clock with the given name is 0. Time period specifies the period for which the number of transitions occur. Therefore, period can not be 0.

What Next

Please check if correct clock name is provided. Moreover, a different clock name can be provided using -clock options, and command can be run again. Please refer to command man page for more information.

PSW-160

(warning) Wrong select type "%s" is provided using -select option.

Description

Possible select types are "regs/tris/inputs/outputs/inouts/ports/nets". When the -select option is used with one or more of the above options, all the objects in the current instance or list of instances that satisfy the selection criteria will be annotated with the specified switching activity.

What Next

Please provide correct select types using -select option and run the command again. Please refer to command man page for more information.

PSW-161

(warning) Instance "%s" can not be found in netlist. Therefore, will not be able to set switching activity information.

Feedback

Description

The instance provided by the -instance option can not be found in the netlist. The command will ignore this instance and continue with other instances if provided.

What Next

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-162

(warning) Instance "%s" can not be found in netlist. Therefore, will not be able to set switching activity information.

Description

The instance provided by the -instance option can not be found in the netlist. The command will ignore this instance and continue with other instances if provided.

What Next

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-163

(warning) Object "%s" does not match either port, pin, net or a cell. Therefore, will not be able to set switching activity information.

Description

The object is neither a port, pin, net or a cell. In order to set switching activity information, object has to be one of these.

What Next

Please check if the correct object list is provided to the command.

PSW-164

(warning) For instance "%s", can not find pin with name "%s". Therefore, can not set switching activity information.

Description

The pin with the given name can not be found in the netlist, therefore switching information can not be set on the pin.

What Next

Please check if the correct pin name is provided is provided to the command by -path option. Please refer to command man page for more information.

PSW-165

(warning) Can not get net connected to the pin "%s". Therefore, will not be able to set switching activity information.

Description

For a pin switching activity information is stored on the net to which it is connected to. Since, the pin is not connected to any net, the switching activity information for this pin can not be set.

What Next

Please check if the correct pin object is provided to the command.

PSW-166

(warning) Pin "%s" is a port. A port can not have state condition associated with it.

Description

Pin is a port and a port can not have state condition associated with it. Therefore, the switching activity information can not be set on the given state condition.

What Next

Please check if the correct pin object is provided to the command.

PSW-167

(warning) Instance "%s" is hierarchical. Can not set state and path dependent switching activity information on the instance.

Description

State and path dependent switching activity information is present only on non-hierarchical instances. Since, this instance is hierarchical the switching activity information can not be set for the given state and path conditions.

What Next

Please check if the correct instance object is provided to the command.

Feedback

PSW-168

(warning) Instance "%s" does not map to technology cell in the library. Can not set state and path dependent switching information on the instance.

Description

State and path dependent switching activity information is present only on non-hierarchical instances. This non-hierarchical instance should be mapped to a technology cell in the library to associate state and path conditions. Since, this instance is not mapped to technology cell, the switching activity information can not be set for the given state and path conditions.

What Next

Please check if the correct instance object is provided to the command.

PSW-169

(warning) Can not find power arc for pin "%s" associated with "%s" state condition. Therefore, can not set switching activity information.

Description

The power arc associated with the state condition for the given pin can not be found from the technology library. Therefore, can not set switching activity information for the given state condition.

What Next

Please check if the correct pin object and state condition are provided to the command.

PSW-170

(warning) For instance "%s", can not find power arc from pin "%s",to pin "%s" with "%s" state condition. Therefore, can not set switching activity information.

Description

The power arc for the given state condition and source and sink pins can not ne found in the technology library. Therefore, can not set switching activity information for the state condition.

What Next

Please check if the correct state condition and pin objects are provided to the command.

Feedback

PSW-171

(warning) For instance "%s", can not find leakage power table for state with state condition "%s". Hence, can not set switching activity information for this state.

Description

The leakage power arc for the given state condition can not ne found in the technology library. Therefore, can not set switching activity information for the state condition.

What Next

Please check if the correct state condition and instance objects are provided to the command.

PSW-172

(error) -period or -clock option can only be used if toggle and glitch values are provided using -toggle_rate and -glitch_rate options, respectively.

Description

-period or -clock options specify the time period for which the number of transitions given by the -toggle_rate and -glitch_rate options occur. If number of transitions are not given then the time period will not be used and hence not required.

What Next

Please provide number of transitions using -toggle_rate and -glitch_rate options, and run the command again. Please refer to command man page for more information.

PSW-173

(warning) No object is selected to set the specified switching activity.

Description

No objects can be found in the design to satisfy the criteria defined by the options given to the set_switching_activity command.

What Next

Give the correct options to the command.

PSW-174

(error) State condition should be provided if path condition is provided using -path option. Please provide state condition using -state option.

Feedback

Description

-path option works only if state condition is provided using -state option. Both the options are required for finding state dependent path dependent power arc. Using -path option user is specifying the swicting activity information on state dependent path dependent power arc to be reset.

What Next

Please provide the state condition and run the command again. Please refer to the command man pages for more information.

PSW-175

(error) State condition, using -state option, can be only be provided if the object list is non empty.

Description

-state option works only if the object list is provided. Using -state option indicates that user wants to reset either state dependent or state dependent path dependent information. For this the exact instance or pin object has to be provided to the command and this can only be done through object list.

What Next

Please provide object list and run the command again. Please refer to the command man pages for more information.

PSW-176

(error) At a time can provide either instance list or object_list, not both.

Description

The object list option for explicitly specifying the objects to be annotated, and the -instance option for implicitly specifying the objects to be annotated, are mutually exclusive. They can not be specified together.

What Next

Please provide either object list or instance list and run the command again. Please refer to the command man pages for more information.

Feedback

PSW-177

(error) Both state condition and instance list are provided using -state and -instance options respectively. Can provide only one of them at a time.

Description

-state option works only if the object list is provided. Using -state option indicates that user wants to reset either state dependent or state dependent path dependent information. For this the exact instance or pin object has to be provided to the command and this can only be done through object list.

What Next

Please provide either state condition or instance list and run the command again. Please refer to the command man pages for more information.

PSW-178

(error) -hier option works only when instance list is provided using -instance option.

Description

-hier option specifies that all the objects in all the hierarchy that will be annotated. It can be used only with the -instance option.

What Next

Please provide instance list using -instance option and run the command again. Please refer to command man page for more information.

PSW-179

(warning) Object "%s" does not match either port, pin, net or a cell. Therefore, will not be able to reset switching activity information.

Description

The object is neither a port, pin, net or a cell. In order to reset switching activity information, object has to be one of these.

What Next

Please check if the correct object list is provided to the command.

Feedback

PSW-180

(warning) Instance "%s" can not be found in netlist. Therefore, will not be able to reset switching activity information.

Description

The instance provided by the -instance option can not be found in the netlist. The command will ignore this instance and continue with other instances if provided.

What Next

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-181

(warning) For instance "%s", can not find pin with name "%s". Therefore, can not reset switching activity information.

Description

The pin with the given name can not be found in the netlist, therefore switching information can not be reset on the pin.

What Next

Please check if the correct pin name is provided is provided to the command by -path option. Please refer to command man page for more information.

PSW-182

(warning) Can not get net connected to the pin "%s". Therefore, will not be able to reset switching activity information.

Description

For a pin switching activity information is stored on the net to which it is connected to. Since, the pin is not connected to any net, the switching activity information for this pin can not be reset.

What Next

Please check if the correct pin object is provided to the command.

PSW-183

(warning) Pin "%s" is a port. A port can not have state condition associated with it.

Feedback

Description

Pin is a port and a port can not have state condition associated with it. Therefore, the switching activity information can not be reset on the given state condition.

What Next

Please check if the correct pin object is provided to the command.

PSW-184

(warning) Instance "%s" is hierarchical. Can not reset state and path dependent switching activity information on the instance.

Description

State and path dependent switching activity information is present only on non-hierarchical instances. Since, this instance is hierarchical the switching activity information can not be reset for the given state and path conditions.

What Next

Please check if the correct instance object is provided to the command.

PSW-185

(warning) Instance "%s" does not map to technology cell in the library. Can not reset state and path dependent switching information on the instance.

Description

State and path dependent switching activity information is present only on non-hierarchical instances. This non-hierarchical instance should be mapped to a technology cell in the library to associate state and path conditions. Since, this instance is not mapped to technology cell, the switching activity information can not be reset for the given state and path conditions.

What Next

Please check if the correct instance object is provided to the command.

PSW-186

(warning) Can not find power arc for pin "%s" associated with "%s" state condition. Therefore, can not reset switching activity information.

Feedback

Description

The power arc associated with the state condition for the given pin can not be found from the technology library. Therefore, can not reset switching activity information for the given state condition.

What Next

Please check if the correct pin object and state condition are provided to the command.

PSW-187

(warning) For instance "%s", can not find power arc from pin "%s",to pin "%s" with "%s" state condition. Therefore, can not reset switching activity information.

Description

The power arc for the given state condition and source and sink pins can not ne found in the technology library. Therefore, can not reset switching activity information for the state condition.

What Next

Please check if the correct state condition and pin objects are provided to the command.

PSW-188

(warning) For instance "%s", can not find leakage power table for state with state condition "%s". Hence, can not reset switching activity information for this state.

Description

The leakage power arc for the given state condition can not ne found in the technology library. Therefore, can not reset switching activity information for the state condition.

What Next

Please check if the correct state condition and instance objects are provided to the command.

PSW-189

(warning) Switching activity for constant net %s is ignored.

Description

The specified net is a constant net, meaning it is connected to VDD (logic 1) or VSS (logic 0), or it is set by set_case_analysis. The toggle rate for the net is always 0.0. The static

probability is 1.0 if it is logic 1, or 0.0 if it is logic 0. The switching activity set by user's set_switching_activity or read_saif is not correct. PrimePower will reset it.

What Next

This is a warning message. Make sure you specify the switching activity is correct.

PSW-190

(warning) Invalid switching activity annotation on constant net %s is being ignored.

Description

The design contains logic 0 or 1 nets, or cell pins driven by such nets, that have been annotated with invalid switching activity. Basically, for constants the annotated toggle rate value must be 0. The static probability for logic 1 objects must 1.0 and that of logic 0 must be 0.0.

Since the user annotation is clearly invalid, it is ignored and the correct switching activity values will be used for power calculation purposes.

What Next

This is a warning message. The invalid user annotation is being ignored during power calculation.

PSW-191

(warning) Net %s has user asserted toggle rate but not the static probability. For propagation the tool will use default static probability and user asserted toggle rate for this net.

Description

Ideally the net should have either both the toggle rate and static probability values either specified by the user or not specified by the user. When one value is specified by the user and other is not we make some assumptions for propagation of these values. In the case of the toggle rate user specified and static probability not, we use default static probability value and user specified toggle rate value, on this net, for propagation. If the static probability value is user specified and toggle rate value is not, then we ignore static probability value, on this net, for propagation.

What Next

This is a warning message. Make sure specifying only one value (either toggle rate or static probability) is intended behavior.

Feedback

PSW-192

(warning) Net %s has user asserted static probability but not the toggle rate. For propagation the tool will ignore static probability for this net.

Description

Ideally the net should have either both the toggle rate and static probability values either specified by the user or not specified by the user. When one value is specified by the user and other is not we make some assumptions for propagation of these values. In the case of the toggle rate user specified and static probability not, we use default static probability value and user specified toggle rate value, on this net, for propagation. If the static probability value is user specified and toggle rate value is not, then we ignore static probability value, on this net, for propagation.

What Next

This is a warning message. Make sure specifying only one value (either toggle rate or static probability) is intended behavior.

PSW-193

(warning) Both -gate and -rtl options are given. Command will report gate level SAIF information.

Description

By default if both -gate and -rtl options are given to the command, command assumes that the user wants to report gate level switching activity information. In other words, the command will assume that -rtl opttion was not given.

What Next

Please see the command man page for more information.

PSW-194

(warning) Instance "%s" can not be found in netlist. Therefore, will not be able to set switching activity information.

Description

The instance provided by the -instance option can not be found in the netlist. The command will ignore this instance and continue with other instances if provided.

What Next

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-195

(error) No switching activity information is annotated on the design. Therefore, can not report switching activity statistics.

Description

Since the user has not annotated switching activity information on nets/cells, the command will not report switching activity statistics.

What Next

Please annotate the design before using the command.

PSW-196

(error) Simulation period is negative. Should be >= 0.

Description

The tool internally stores the switching activity information in terms of signal probability and transition density. For writing out SAIF file the tool needs the simulation period for converting signal probability into one time (time for which the signal has logic state 1) and zero time (time for which the signal has logic state 0), and for converting transition density into toggle count. Simulation period is the duration for which the design is simulated for. It can not be negative.

What Next

Please provide correct value of simulation period and run the command again.

PSW-197

(error) Derating factor is negative. Should be >= 0.

Description

The derating factor is used for converting total glitch rate into inertial glitch portion. Since total number of glitches can not be negative, derating factor can not be negative.

What Next

Please provide correct value of derating factor and run the command again.

Feedback

PSW-198

(error) Can not get the full file name for writing.

Description

The command can not get the full file name for writing SAIF information. Full file name is required for write_saif command.

What Next

Please check the writing permissions and run the command again.

PSW-199

(warning) Instance "%s" can not be found in netlist. Therefore, will not be able to set switching activity information.

Description

The instance provided by the -instance option can not be found in the netlist. The command will ignore this instance and continue with other instances if provided.

What Next

Please check if correct instance is provided. Please refer to command man page for more information.

PSW-200

(warning) Instance "%s" is non hierarchical. The list of instances should only contain hierarchical instances. Therefore, switching activity information will not be reported for this instance.

Description

The instance list provided by the -instance option should contain only hierarchical instances. The command will ignore this instance and continue with other instances if provided.

What Next

Please check if correct instance is provided. Please refer to command man page for more information.

Feedback

PSW-201

(error) The list of SAIF files and weights is empty. Please provide the list of SAIF files and their weights.

Description

For merging the SAIF files the command requires the list of SAIF files and their corresponding weights.

What Next

Please provide the list of SAIF files and weights, and run the command again.

PSW-202

(error) In the list of SAIF files and weights, either -input option is not given or the order of -input and -weight options is incorrect.

Description

The list of SAIF files and their weigths, consists of {-input file_name -weight value}. So, either -input option is not given or the order of -input and -weight options is incorrect. -input option should always precedes -weight option for a given SAIF file.

What Next

Please provide the correct list of SAIF files and weights, and run the command again.

PSW-203

(error) In the list of SAIF files and weights, either -weight option is not given or the order of -input and -weight options is incorrect

Description

The list of SAIF files and their weigths, consists of {-input file_name -weight value}. So, either -weight option is not given or the order of -input and -weight options is incorrect. -input option should always precedes -weight option for a given SAIF file.

What Next

Please provide the correct list of SAIF files and weights, and run the command again.

PSW-204

(error) The value of weight should be between 0 and 100.

Feedback

Description

The value of weight should be between 0 and 100.

What Next

Please specify the correct weight value and run the command again.

PSW-205

(error) There should be equal number of -input and -weight options in the list of SAIF files and weights.

Description

The list of SAIF files and their weigths, consists of {-input file_name -weight value}. -input option is always followed by -weight option. Therefore, there should be equal number of -input and -weight options.

What Next

Please specify the correct list of SAIF files and weights and run the command again.

PSW-206

(error) The sum of all weight values should euqal to 100.

Description

The list of all weight values should be equal to 100.

What Next

Please specify the correct weight values and run the command again.

PSW-207

(Warning) Command is ignored because the given -rtl and -gate names are the same.

Description

The name mapping database in PrimePower does not include tuples where the simulation name and the gate level name are the same. In this case the set_rtl_to_gate_name command is ignored.

What Next

Ignore the warning.

Feedback

PSW-208

(warning) Switching activity for constant net %s is reset by SAIF/VCD.

Description

The specified net is a constant net, meaning it is connected to VDD (logic 1) or VSS (logic 0), it is set by set_case_analysis, or it is propagated by other logic constants. The toggle rate for the net is always 0.0. The static probability is 1.0 if it is logic 1, or 0.0 if it is logic 0. The switching activity set by user's SAIF or VCD conflicts with it. PrimePower will take SAIF or VCD values.

What Next

This is a warning message. Make sure you specify the switching activity is correct.

PSW-209

(warning) Switching activity at %s is consolidated.

Description

The specified pin or net is in a multi driver net. Its switching activity is consolidated.

Basically, if switching activity is set on driver's pins, then all uninitialized driver's pins will have 0 switching activity, and the net and load pins have sum of driver's switching activity. If switching activity is annotated to none of driver's pins, then the tool will look for the net's switching activity. If the net is annotated, then the switching activity will be evenly distributed to each driver's pins. The switching activity will aslo be copied to load's pins exactly. If the net is not annotated, then the tool will look at load pins. It calculates the average switching activity from all load pins, then evenly distributes the average switching activity to to each driver's pins and copies the average switching activity to the net and each load's pins.

What Next

This is a warning message. Make sure you specify the switching activity is correct.

PSW-210

(error) Switching activity cannot be set due to zero period of clock "s"

Description

PrimePower will set default switching activities according to clock's period. So clock's period cannot be zero.

Feedback

What Next

Give a non-zero clock period.

PSW-211

(Warning) Switching activity for %s %s is overwritten with different values

Description

The switching activity of the specified net or pin is overwritten with different values. If not intended, overwriting net or pin switching activity with different values, may be caused by mismatches between the activity file and the netlist. If annotation is applied to multiple pins which were connected in an earlier version of the netlist, but not the current version, will result in annotation mismatch on the nets they connect to now.

What Next

This is a warning message. If overwriting the activity was not intended, check the switching activity files provided, for entries which apply annotation to any of the objects connected to the net and apply the desired value.

PSW-212

(error) option '%s' is not valid for -compress.

Description

"write_saif" command with option '-compress' dumps compressed saif file. The only valid value is "gzip".

What Next

Please provide value 'gzip' for -compress.

PSW-213

(warning) Skipping annotation on constant net "%s".

Description

Annotation on constant nets is not allowed if activity file precedence is lower.

PSW-214

(warning) Ignorning activity of generated clock "%s (TR=%f, SP=%f)" and using the propagated activity from upstream master clock "%s (TR=%f, SP=%f)".

Description

When *power_enable_ignore_create_generated_clock-period* variable is set by the user, then generated clock activity set by the user using "create_generated_clock" command is ignored. Instead, propagated activity coming from the upstream logic is used. If the cell is a black box cell, then generated clock activity will be used and propagated activity will be ignored.

PSW-215

(warning) constant pin "%s" activity is overriden by set_switching_activity.

Description

constant pin activity is overriden by set_switching_activity.

PSW-216

(warning) power_enable_annotation_precedence_over_implied is true, implication from case constants cannot override direct annotated file activity.

Description

By default variable power_activity_file_precedence_over_sca and power_enable_annotation_precedence_over_implied are true. When power_activity_file_precedence_over_sca is set false, variable power_enable_annotation_precedence_over_implied will not allow implication from higher activity case constants override file activity. Also, forward implication has higher precedence over backward implication and doesn't depend on source of annotation.

PSW-217

(warning) Generated clock (%s) is defined at output of macro cell, using SDC annotated clock activity (TR=%f, SP=%f) instead of upstream propagated activity.

Description

When *power_enable_ignore_create_generated_clock-period* variable is set, and generated clock is defined by the user at the output of a black box cell, then generated clock activity set by the user using "create_generated_clock" will be used and propagated activity will be ignored. The propagated activity coming from the upstream logic is ignored if cell is a macro cell.

Feedback

PSW-218

(warning) Possible issue with annotation, check -strip_path argument.

Description

It could be the name of the instance of the current design given by option -strip_path is incorrect, the time window specified by -time is out of range, the VCD file is EVCD, or VCD has syntax errors.

What Next

Please check SAIF/VCD file, make it's not EVCD, have correct syntax, and -strip_path and -time are correct.

PSW-219

(Error) QM propagation is not enabled.

Description

get_switching_activity -qm_propagated will give invalid result when qm_propagation is disabled, kindly set power_enable_qm_propagation to true.

What Next

Please refer to man page of the command for more information on options.

PT

PT-001

(fatal) %s is not enabled.

Description

The application tried to reserve the specified license, but it was not available.

What Next

Verify that the key file is up to date and that sufficient licenses are available.

PT-002

(error) Unrecognized feature name '%s'.

Feedback

Description

You tried to get or remove a license that does not exist in the key file.

What Next

Verify that the key file is up to date and that the feature name is spelled correctly.

PT-003

(Information) There are already %d licenses checked out for feature %s.

Description

This error occurred because you specified the *-quantity* option with the *get_license command* command and the specified quantity is smaller than the number of licenses that are already checked out for the specified feature.

The value specified for *-quantity* is the total number of licenses that should be checked out after the command has completed, which might not be the same as the incremental number of licenses checked out by the command.

What Next

Verify that the feature name is spelled correctly in case it was a different feature that you wanted to get. Specify a quantity that is equal to or greater than the number of licenses that have already been obtained.

See Also

- get_license
- list_licenses

PT-004

(error) You don't have a '%s' license to remove.

Description

You tried to remove a license that is not checked out.

What Next

Verify that the feature name is spelled correctly in case it was a different feature that you wanted to remove.

Feedback

PT-005

(error) Can't remove your '%s' license: %s.

Description

You tried to remove a license that is locked by the application. For example, this might be the license that is required to launch the application, or the license might be required by a design that is in memory. The message will indicate the condition that triggered it.

What Next

Action based on the message text.

PT-006

(error) %s is not supported on '%s' platform.

Description

This is an error message indicating the command or option is not supported on the specified platform.

What Next

Please check the command manpage or product manuals for supported platforms. Make sure you run this command on the platforms that are supported.

PT-007

(warning) %s is deprecated; it will be obsoleted and removed starting with the %s release of PrimeTime.

Description

This is a warning message indicating the specified command, option, or variable is currently deprecated, and it will become obsoleted and removed in a future release of PrimeTime.

A "deprecated" feature is a feature that has not yet been removed but is planned to be removed in a future release. Thus, its use should be discontinued or transitioned to another feature.

An "obsoleted" feature is a feature that has been removed from the tool.

Feedback

What Next

Please check the command/variable manpages, product manuals, or release notes for more details about the deprecation, and whether there are alternative approaches or replacements for this deprecated feature.

PT-008

(error) %s was obsoleted starting with the %s release of PrimeTime; it is no longer supported.

Description

This is an error message indicating that the specified command, option, or variable has been obsoleted and is no longer supported.

What Next

Please check the command/variable manpages, product manuals, or release notes for more details about the obsolescence, and whether there are alternative approaches or replacements for this obsoleted feature.

PT-009

(warning) The BC_WC analysis mode will be phased out in future releases.

Description

The analysis mode you are setting, best case - worst case, is potentially inaccurate and should be avoided for sign-off. It will be obsoleted in a future release of PrimeTime.

For a thorough analysis, both setup and hold times should be checked at each corner of interest using the on_chip_variation analysis mode. In the BC_WC analysis mode, two corners are analyzed simultaneously. Hold times are checked at the fast (min) corner, and setup times are checked at the slow (max) corner. In the fast corner, fast slews are propagated along both the launch and capture sides of hold timing paths. As a result, worst-case slow timing cannot be guaranteed on the hold capture paths. In the slow corner, slow slews are propagated along both the launch and capture sides of setup timing paths. Again, worst-case fast timing cannot be guaranteed on the setup capture paths. In addition, the BC_WC analysis is incomplete because setup times are not cross-checked in the fast corner, and hold times are not cross-checked in the slow corner.

What Next

Migrate flows and scripts to avoid setting BC_WC analysis mode.

Feedback

PT-010

(error) %s is not enabled.

Description

The application tried to reserve the specified license, but it was not available.

What Next

Verify that the key file is up to date and that sufficient licenses are available.

PT-011

(Warning) Obtained %d of requested %d licenses for feature %s.

Description

This warning is printed out because you specified the *-quantity* option with the *get_license command* and the number of licenses that was obtained is less than the requested quantity of licenses the specified feature.

At least one license of the specified feature was obtained.

What Next

No action is necessary if it is acceptable to run the tool with less than requested number of licenses (this may have tool performance implications). Otherwise, check the number of licenses of the specified feature and their usage by other processes and re-run the command when there are enough licenses available.

See Also

- get_license
- list_licenses

PT-012

(Error) Only %d licenses are checked out for feature %s.

Description

This error occurred because you specified the *-keep* option with the *remove_license command and you specified a quantity that is greater than the number of licenses that have already been obtained for the specified feature.*

Feedback

What Next

Specify a quantity for the *-keep* option that is less than or equal to the number of licenses that are already checked out for the specified feature.

See Also

- get_license
- list_licenses

PT-014

(information) Successfully checked out feature '%s'.

Description

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

What Next

This is an informational message only. No action is required on your part.

See Also

- PT-018

PT-015

(information) Started queuing for feature '%s'.

Description

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

What Next

This is an informational message only. No action is required on your part.

See Also

- PT-018

PT-016

(information) Still waiting for feature '%s'.

Feedback

Description

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

What Next

This is an informational message only. No action is required on your part.

See Also

- PT-018

PT-017

(information) Timeout while waiting for feature '%s'.

Description

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in pt_shell.

What Next

This is an informational message only. No action is required on your part.

See Also

- PT-018

PT-018

(Information) License queuing is enabled.

Description

You receive this message because you have enabled license queuing.

The license queuing is enabled by setenv SNPSLMD_QUEUE TRUE

When enabled the following timeouts can be adjusted:

Timeout for the initial license: setenv SNPS_MAX_WAITTIME <number of seconds>

Timeout for all subsequent licenses: setenv SNPS_MAX_QUEUETIME <number of seconds>

Defaults are equivalent to setenv SNPS_MAX_WAITTIME 259200 setenv SNPS_MAX_QUEUETIME 28800

Feedback

What Next

This is an informational message only. No action is required on your part.

PT-019

(Information) Checked out license '%s'

Description

The application checked out 1 license of the feature specified.

PT-020

(Information) Checked in license '%s'

Description

The application checked in 1 license of the feature specified.

PT-021

(information) Setting license limit for feature '%s' to %d.

Description

The limit on number of licenses for the specified feature has been set.

What Next

This is an informational message only. No action is required on your part.

See Also

- get_license
- remove_license

PT-022

(warning) Failed to set license limit for feature '%s': existing license count is higher than limit (%d > %d).

Description

Failed to set the limit on number of licenses for the specified feature because the number of currently used licenses for the feature is higher than the specified limit.

Feedback

What Next

Reduce the license count for the specified feature to a number lower or equal of the given limit.

PT-023

(Warning) Requested '%d' licenses for feature '%s', '%d' checked out.

Description

Failed to checkout the requested number of licenses for the specified feature but did manage to check out some.

If the number of licenses requested is higher than the number already checked out, this occurs when the license server cannot fulfil the requests for the number of licenses due to a lack of licenses or because some of its licenses are already in use. The number of license indicated as checked out are all the license that can be acquired at this time.

If the number of licenses requested is lower than the number already checked out, this occurs because incremental licensing is not enabled.

PrimeTime can only check out licenses for a single feature from a single license server at a time. If the licenses for a feature are split across multiple license servers, the maximum number of licenses of that feature that PrimeTime can check out is determined by the license server with the largest number of licenses. PrimeTime cannot span its license check outs for a single feature across multiple license servers at this time. However, it can check out licenses for different features from different license servers.

What Next

If the warning is due to a failure to increase the number of licenses then increase the number of licenses available on the license server so that subsequent attempts to checkout licenses succeed.

PT-024

(information) Removing license limit for feature %s.

Description

The limit on number of licenses for the specified feature has been removed.

What Next

This is an informational message only. No action is required on your part.

Feedback

PT-025

(error) Cannot modify this variable after the first timing update.

Description

This variable can only be set prior to the initial timing update of the current design.

What Next

Please reconsider when to set this variable in your script or interactive run.

PT-026

(warning) %s has been made obsolete since the %s release of PrimeTime and is no longer supported.

Description

This is an error message indicating that the specified command, option or variable has been obsoleted and is no longer supported.

What Next

Please check the command/variable manpages, product manuals or release notes for more details about the obsolescence, and whether there are alternative approaches or replacements for this feature being obsleted.

PT-027

(error) Cannot set the license limit for the crucial feature '%s' to '%d'

Description

The limit on the number of licenses of the specified crucial feature cannot be set to the level specified. Typically this occurs when setting the limit to '0' which is not allowed as at least 1 license key of a crucial feature must remained checked out at all times during a session.

What Next

Specify a higher limit on the number of licenses.

PT-029

(information) Failed to checkout '%s' license ... exiting!

Feedback

Description

PrimeTime exited after failing to checkout a license for a feature required by commands in the users script. Typically this occurs when all the license keys for the required feature are in use.

Exiting under these conditions is a user selected behaviour, by default PrimeTime does not exit when a feature license is not available it continues execution without the commands/ capabilities enabled.

What Next

In order to prevent PrimeTime from exiting immediately when the feature license cannot be checked out, turn on license queuing to have the tool wait for a period of time for a license to become available. License queuing can be turned on by applying the following in the UNIX shell prior to launching PrimeTime.

setenv SNPSLMD_QUEUE TRUE

By default, the queuing timeout is 28800 seconds.

If license queuing is already enabled then the queuing time may be too short and can be set by applying the following in the UNIX shell prior to launching PrimeTime along with enabling license queuing.

setenv SNPS_MAX_QUEUETIME <number of seconds>

PT-030

(error) The '%s' license cannot be removed, it is a pre-requisite of the '%s' license.

Description

The license cannot be removed as it is a pre-requisite of another license which is currently checked out.

What Next

Remove the license that depends on this license before removing this license.

PT-031

(error) the '%s' license cannot be removed, it is required by the '%s' variable setting.

Description

The license cannot be removed as it is required by the analysis type enabled by the specified variable.

Feedback

What Next

Disable the analysis type specified by the variable and then remove the license.

PT-032

(error) The '%s' license limit cannot be set to '%d' '%s' is a prerequisite of the '%s' feature which already has '%d' licenses checked out.

Description

Where a feature is a prerequisite of another feature, the limit on the prerequiste feature cannot be less than the number of licenses already checked out for the feature with the license dependency.

What Next

Reduce the number of licenes checked out for the feature with the prerequisite dependency before reducing the limit on the prerequisite feature.

PT-033

(error) The '%s' license limit cannot be set to '%d' '%s' is a prerequisite of the '%s' feature whose limit is already set to '%d'

Description

Where a feature is a prerequisite of another feature, its limit cannot be set less than the limit set for the feature with the prerequisite dependency.

What Next

Reduce the limit on the feature with the prerequisite dependency before reducing the limit for the prerequisite feature.

PT-034

(Information) License filtering is enabled.

Description

You receive this message because you have enabled licensing filtering.

The license filtering is enabled by setting the following UNIX environmental variable before starting PrimeTime.

setenv SNPSLMD_DISABLE_NTA_LICENSE_CHECKS 1

Feedback

When enabled, this indicates to PrimeTime that the user is not interested in any capabilities associated with the PrimeTime New Technology feature licenses. As a result PrimeTime will not even query the license server for the existence of these licenses, it will be as if the feature keys are not present in the license server and any associated capabiliteis will remain disabled.

What Next

This is an informational message only. No action is required on your part.

PT-035

(error) Cannot reduce %s license count to %d because %d licenses of this feature are required for feature %s.

Description

This error occurred because you specified the *-keep* option with the *remove_license command, but the number of licenses for the specifed feature cannot be reduced because it is a pre-requisite of another feature.*

Where a feature is a prerequisite of another feature, its license count cannot be set to a lower number than the license count of the feature with the prerequisite dependency.

What Next

Reduce the license count on the feature with the prerequisite dependency before reducing the license count for the prerequisite feature.

See Also

- remove_license
- get_license
- list_licenses

PT-036

(error) Feature %s is limited to %d licenses.

Description

This error occurred because you specified the *-quantity* option with the *get_license command, but the number of licenses for the specifed feature is limited to a lower number than the requested number of licenses.*

The get_license *command will attempt to obtain licenses up to the limit.*

Feedback

What Next

Set higher limit or remove the limit for the specified feature using the set_license_limit *command.*

See Also

- set_license_limit
- get_license
- list_licenses

PT-037

(error) Cannot get more than %d licenses for feature %s due to pre-requisite limits.

Description

This error occurred because you specified the *-quantity* option with the *get_license command, but the number of licenses for the specifed feature cannot be set to a higher number than the license limit set on a feature the specified feature depends on.*

The get_license *command will attempt to obtain licenses up to the maximum allowable number.*

What Next

Set higher limit or remove the limit for the feature the specified feature depends on using the set_license_limit *command.*

See Also

- set_license_limit
- get_license
- list_licenses

PT-040

(information) Advanced waveform propagation is enabled.

Description

You receive this message because you have enabled the advanced waveform propagation mode.

Feedback

What Next

This is an informational message only. No action is required on your part.

PT-041

(information) Message '%s' %s limit (%d) exceeded. Remainder will be suppressed.

Description

You receive this message if the total number of warning messages of a particular message id exceeds a default (or user set) limit.

What Next

This is an informational message only. To avoid receiving this message, you can increase the default limit using the variable *sh_message_limit* or the command *set_message_info*.

See Also

- PT-041

PT-042

(information) No license limit set for feature %s.

Description

You are trying to remove the limit on the number of licenses set for a feature shown in the informational message, but the limit cannot be removed because it was not previously set.

What Next

This is an informational message only. No action is required on your part.

PT-043

(information) No limits are set on feature licenses.

Description

There are no limits on the number of licenses set for any feature.

What Next

This is an informational message only. No action is required on your part.

Feedback

PT-044

(Warning) Only one %s license can be checked out at a worker process.

Description

You have issued the *get_license* command with the *-quantity* option, requesting check out of more than one license for the given feature at a worker process. There is no need for worker processes to use more than one license of a feature, so *get_license* will attempt to check out only one of the requested feature licenses.

What Next

Check out the required number of licenses at the manager process instead of checking out licenses at worker processes. Alternatively, modify your scripts to check out no more than one license of the feature by a worker process.

PT-045

(Error) PrimeTime New Technology license %s cannot be checked out.

Description

You have issued the *get_license* command requesting check out of a PrimeTime New Technology license. PrimeTime does not require check out of New Technology feature licenses.

What Next

Remove the request to check out a PrimeTime New Technology license from your script.

PT-046

(Error) the '%s' feature license cannot be checked out.

Description

You have issued the *get_license* command requesting check out of the debug feature indicated, however the UNIX environmental variable *SNPSLMD_DISABLE_DEBUG_LICENSE_CHECKS* is set to 1 indicating that all debug licenses should be skipped for access.

What Next

Remove the request to check out the indicated feature from your script or unset the *SNPSLMD_DISABLE_DEBUG_LICENSE_CHECKS* UNIX environmental variable.

Feedback

PT-047

(error) Cannot set limit for dependent feature %s to %d which is higher than the limit %d set on a pre-requisite feature.

Description

This error occurred because you specified the *-quantity* option with the *set_license_limit command, but the limit of licenses for the specifed feature cannot be set to a higher number than the license limit set on a feature the specified feature depends on.*

What Next

Set higher limit or remove the limit for the feature the specified feature depends on using the set_license_limit *command.*

See Also

- set_license_limit
- report_license_limit

PT-048

(error) Checkout of these licensed features has failed: %s.

Description

The application tried to reserve the specified list of licensed features, but one or more of them was not available.

What Next

Verify that the key file is up to date and that sufficient licenses are available.

PT-049

(error) Cannot reduce the %s license count from %d to %d, %d licenses are in use for %s.

Description

This error occurred because you tried to reduce the number of licenses checked out, for the specified feature, to below the number of licenses currently in use for the analysis indicated.

Feedback

See Also

- remove_license
- get_license
- list_licenses

PT-050

(error) cannot checkout '%s' because it is suppressed.

Description

The feature license cannot be checked out because it has been suppressed for checkout by the user.

What Next

If the feature license is required, do not suppress it. Remove whatever suppression method has been applied.

PT-051

(error) cannot checkout '%s' because its prerequisite '%s' is suppressed.

Description

The feature license cannot be checked out because it one or more of its prerequisite features has been suppressed.

What Next

If the feature license is required, do not suppress any of its prerequisites. Remove whatever suppression method has been applied.

PT-052

(Information) License queuing is disabled.

Description

You receive this message because you have explicity disabled license queuing.

The license queuing is disabled by setenv SNPSLMD_QUEUE FALSE

What Next

This is an informational message only. No action is required on your part.

Feedback

PT-054

(Information) Changing the license checkout maximum wait time from '%d' seconds to '%d' seconds.

Description

You receive this message because you requested the maximum wait time for the initial license checkout to be changed to the specifed value.

What Next

This is an informational message only. No action is required on your part.

PT-055

(Information) Changing the license checkout maximum queue time from '%d' seconds to '%d' seconds.

Description

You receive this message because you requested the maximum queue time for license checkouts to be changed to the specifed value.

Where the process is a PrimeTime DMSA manager, it is recommended to set this value to a reaonably small value (< 300s) because where there are insufficient licenses available, each distributed command executed at the manager will incur queuing for licenses. The queuing will occur for every command until all the required licenes have been acquired impacting performance.

What Next

This is an informational message only. No action is required on your part.

PT-056

(Error) Failed to enable incremental licensing.

Description

You receive this message because the tool tried to enable incremental licensing internally and failed.

What Next

Contact the tool support team.

Feedback

PT-058

(Error) Failed to initialize critical licensing component.

Description

You receive this message because a critical licensing component failed to initialise and the tool cannot start up.

What Next

Please open a star with Synopsys specifying this error message.

PT-059

(Warning) could not load Itcl package.

Description

You receive this message because the Incremental Tcl (Itcl) package supplied as part of the PrimeTime installation cannot be loaded.

What Next

Please check your Primetime installation directories include the itcl package library.

PT-060

(Warning) Background process invalidates the -baseline_delta option of mem command

Description

The -set_baseline option of the mem command sets a baseline of the current memory used by PrimeTime. Subsequently, mem -baseline_delta returns the peak memory since the last baseline. If a background process is launched by the tool (e.g. by parallel_execute or redirect -background) after a baseline has been set, the memory used by the background proces will not be accounted in the result of mem -baseline_delta.

See Also

- mem

PT-061

(Error) Failed to initialize the licensing call-home functionality.

Feedback

Description

You receive this message because the licensing infrastructure failed to initialize a critical component necessary for checking out licenses.

What Next

Please file a STAR reporting the circumstances under which this occurred.

PT-063

(Error) Library Compiler executable path is not set.

Description

When you install the PrimeTime tool, you need to specify the path to the Library Compiler executable, which PrimeTime tool uses for reading Liberty (.lib) files. The Library Compiler executable cannot be found because no path was specified.

What Next

Do one or both of the following:

- Add the Library Compiler executable path to the existing PrimeTime installation by running the following script:

  ```
  $synopsys/admin/install/syn/bin/install_pt
  ```

  The script prompts you for the location of the Library Compiler root directory:

  ```
  Synopsys Library Compiler root directory:
  ```

  At the prompt, enter the root installation directory of the Library Compiler tool.
- Set the SYNOPSYS_LC_ROOT environment variable to the path to the Library Compiler executable before you invoke the PrimeTime shell.

PT-064

(Error) Incorrect argument %s passed to load : %s.

Description

You receive this message because an option passed to the *load* command is incorrect.

What Next

The the arguments passed to the *load* command.

Feedback

PT-065

(Error) Loading command %s failed limitations checking: %s.

Description

You receive this message because the *load* tried to define commands which do not conform to PrimeTime's requirements.

What Next

Modify the source code of the loaded shared library to make it compatible with Primetime's requirements.

PT-066

(fatal) Existing command %s was overwritten by load.

Description

You receive this message because the *load* command tried to overwrite one the existing PrimeTime commands.

What Next

Modify the source code of the loaded shared library to use command names different to the names of existing PrimeTime commands.

PT-067

(fatal) Failure to open file due to system error "%s".

Description

A file could not be opened because of operating system error.

What Next

Depending on the system error, take the appropriate action on your OS or in your scripts. For example, an error of "Too many open files" may indicate that file handles are being leaked (opened but not closed) in a tcl script. See the linux man page for 'errno' for more information.

PT-068

(warning) The dynamically loaded library was not linked against the collections library.

Feedback

Description

The dynamically linked library was not linked against the Synopsys supplied Collections API library. The load may still proceed, but this native Collections API functionality will be unavailable.

What Next

If you wish to access the Collections API functionality, please ensure you are following Synopsys supplied instructions for this, or contact Synopsys.

PT-072

(error) License checkout is not allowed in subprocesses.

Description

Cross command parallel execution directives *redirect -bg* and *parallel_execute* launch subprocesses to perform the commands in parallel. It is required that these subprocesses do not try to checkout additional license while performing their work. Therefore, commands and variables which implicitly try to checkout licenses are not executed and error is issued.

What Next

Remove the license checkout command from subprocesses running in parallel, and move them to the main parent process so they are executed in serial mode. The license checked-out by the parent process will be avilable for use to all the subprocesses.

PT-073

(error) Cannot request %d keys of %s in the In-Design Mode.

Description

In the In-Design mode an external application instructs the tool such as PrimeTime to manage licenses in the pre-programmed way. This error occurs if the number of license keys requested by the tool is larger than 1.

What Next

Remove the license checkout command from the script passed to the tool (e.g. PrimeTime) which requests multiple license keys. Alternatively, multiple keys may be requested internally by the tool due to enabling of some capability, in that case rewrite the script to request only a single key of the license.

Feedback

PT-074

(error) The license %s is not available in the In-Design Mode.

Description

In the In-Design mode an external application instructs the tool such as PrimeTime to manage licenses in the pre-programmed way. This error occurs if the reported license is not allowed to be checked out by the tool.

What Next

Remove the license checkout command from the script passed to the tool (e.g. PrimeTime) which requests the license.

PT-075

(error) %s or %s is not enabled.

Description

The application tried to reserve the specified license, but either one or both of them were not available.

What Next

Verify that the key file is up to date and that sufficient licenses are available.

PTANA

PTANA-001

(error) Cannot change the state of fast analysis mode because %s.

Description

This error message is issued when the attemp to change the state of fast analysis mode fails due to the reason indicated. Most often, it happens when you are trying to either enable or disable fast analysis mode after designs and/or libraries have already been loaded into PrimeTime.

What Next

Please verify the reason indicated by the error message, make sure you issue the command 'set_program_options' earlier, e.g. before any library/design is loaded.

Feedback

PTANA-002

(Information) Fast analysis mode is %s.

Description

This information message is issued when the state of fast analysis mode is changed.

PTANA-003

(error) %s.

Description

This is a generic error message.

What Next

Please note and confirm the specific reason indicated by the error message, modify your setting(s) accordingly, re-issue the command(s).

PTANA-004

(Warning) The value of variable %s cannot be changed under fast analysis mode.

Description

In fast analysis mode, the values of some variables are fixed in a range.

PTC

PTC-001

(Error) Cannot enable PrimeTime Constraint Analyser feature because '%s' license is not available.

Description

This error occurs when the required license is not available for switching into the PTC mode.

What Next

Check your licensing setup to ensure that the required license is available.

Feedback

PTC-002

(Information) Successfully enabled PrimeTime Constraint Analyser feature.

Description

This message is printed when PrimeTime has successfully switched into the PTC mode.

What Next

No action is needed.

PTCLCT

PTCLCT-001

(warning) The specified attribute is not consistently defined across the collection.

Description

For specific commands which operate on attributes of a collection the attribute must be consistently defined across the collection. That is, the attribute must be defined for each class type and the attribute must be of the same data type (string, float, boolean etc).

What Next

If the attribute is user defined then ensure the attribute for the class type(s) is consistently defined through the define_user_attribute command. If the attribute is internal but modifiable, then filter the collection accordingly.

PTE

PTE-001

(Error) There are no arcs from pin '%s' to pin '%s' on cell '%s'.

Description

This error occurs when any arc does not exist between the two pins specified by the -from option and the -to option of set_disable_timing or remove_disable_timing commands.

What Next

Make sure the pins really exist on the cell or the libcell.

Feedback

PTE-003

(Warning) Some timing arcs have been disabled for breaking timing loops or because of constant propagation. Use the 'report_disable_timing' command to get the list of these disabled timing arcs.

Description

This message is displayed when timing arcs are disabled by tool to break combinational feedback loops or when propagating constant value due to case analysis. It is not displayed for arcs that are manually disabled with the *set_disable_timing* command.

What Next

If you want to manually break a timing loop, examine the design to see why there is combinational feedback, then choose a different point at which to break the loop. To do this, use the *set_disable_timing* command instead of letting the tool automatically break the loop. To see details on the timing loops in the design, use *check_timing -inlcude loops -verbose*.

PTE-004

(error) The pin '%s', which is a generated clock pin, is either in a loop or is in the fanout of two clock sources.

Description

The generated clock pin is in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network, nor can you have a generated clock in the fanout of two clock sources.

What Next

If it is a loop, break the loop. If the generated clock is in the fanout of two clock sources, try to isolate it or use internal clocks instead.

PTE-005

(information) Invalidating all auto-disabled timing arcs.

Description

Some arcs have been enabled, forcing the tool to do loop detection from scratch. The tool therefore enables all auto-disabled arcs.

Feedback

What Next

To view all timing loops in your design, use *check_timing -loops*. To manually break the loops, use *disable_timing*.

PTE-006

(error) Cannot specify '%s' as the group name.

Description

Some path groups are internal and cannot be modified by you.

What Next

Use *group_path* with a valid group name.

PTE-007

(warning) Attempting to remove a clock gating check that was not previously set.

Description

Removal of clock gating check on an object is valid only if a clock gating check was set before on that object.

What Next

This command will be ignored. Please check the spelling of the object for the *remove_clock_gating_check* command.

PTE-008

(error) No%s timing arc in cell '%s(%s)' from pin %s'%s' to pin '%s'.

Description

Some cell timing arcs specified in the SDF file cannot be found in the current design.

What Next

Check if your SDF file is up-to-date with your design.

PTE-009

(Warning) No %s arcs from pin '%s'.

Feedback

Description

Delay annotation does not match netlist. The message is issued because some timing arcs specified in the SDF file, or by *set_annotated_delay* command cannot be found in the current design.

This can happen for example when SDF file was written for one design and applied with read_sdf to a different design.

The message is also issued if *set_annotated_delay* command is used to annotate timing arcs that do not exit. For example due to incorrect directions of ports, such as bidirectional pin u1/PAD being connected to a net with single input port IN. Then command *set_annotated_delay -net -from u1/PAD 10.2* results in PTE-009 because arc u1/PAD to IN does not exits.

The message is automatically suppressed when annotating only delta delay.

What Next

If the message occurs during read_sdf then check that your SDF file is up-to-date with your design. If the missing arc is due to false path (e.g., in the example above the path from u1/PAD to IN would never be functionally sensitized) then suppress the message.

See Also

- read_sdf
- set_annotated_delay
- suppress_message
- si_enable_analysis

PTE-010

(error) No %s arcs to pin '%s'.

Description

Some timing arcs specified in the SDF file cannot be found in the current design.

What Next

Check if your SDF file is up-to-date with your design.

PTE-011

(warning) No%s timing arc in cell '%s(%s)' with condition '%s' from pin %s'%s' to pin '%s'.

Feedback

Description

Some timing arcs specified in the SDF file cannot be found in the current design.

What Next

Check if your SDF file is up-to-date with your design.

PTE-012

(warning) A non-unate path in clock network detected. Propagating noninverting sense for clock '%s' to endpoints through pin '%s'.

Description

The clock tree for the specified clock contains non-unate paths. Clock networks normally do not contain cells such as exclusive-OR gates which have non-unate behavior. This implies that both inverting and noninverting clock waveforms reach the specified pin. Since it is ambiguous PrimeTime always uses the noninverting sense of clock at clock pins down stream from these pins.

What Next

If you want to control the sense of the clock used through this pin, use the command 'set_clock_sense'.

PTE-013

(warning) Some clock relationships result in a common base period which require clock waveforms to be expanded more than 1000 times. PrimeTime limits clock waveforms expansion to be no more than 1000. Please check your clocks and apply set_false_path between unrelated clock domains.

Description

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set).

If the large base period is due to the fact that clock periods do not divide evenly then PrimeTime tries to tweak the periods so that they divide evenly. Use *report_clock* to find out the exact clock period used. In any case, the PrimeTime restricts clock waveform expansion to no more than 1000.

Feedback

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large base period. You can disable clock-gating checks by setting the environment variable timing_disable_clock_gating_checks to "true".

What Next

Use *set_false_path* to declare that timing paths between unrelated clocks are false.

PTE-014

(error) No net timing arc from pin '%s' to pin '%s'.

Description

There were no timing arcs between the specified pins. You received this error because the net timing arcs specified in the SDF cannot be found in the current design, or the entered command requires the existance of a timing net arc between the two pins.

What Next

Check if both nets are connected to the same net. If the error is issued during reading of a SDF file, make sure that the SDF file is up-to-date with your design.

PTE-015

(error) Net delay from pin '%s' to pin '%s'cannot be annotated because of a timing assertion on hierarchical pin '%s'.

Description

When a timing assertion such as create_clock or a max_delay is specified on a hierachical pin, SDF annotation cannot be performed between the 'from_pin' and 'to_pin' of the net. This is because of the net segmentation performed on the hierarchical pin which is inbetween the 'from_pin' and 'to_pin'.

What Next

It is recommened that you do not specify timing assertion on hierarchical pins.

PTE-016

(information) Expanding clock '%s' to base period of %.3f (old period was %.3f, added %d edges).

Description

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and

CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set) and expands the clock waveforms to the base period.

What Next

It is recommened that you mark paths between unrelated clocks as false.

PTE-017

(information) Inferring %d clock-gating checks.

Description

PrimeTime automatically checks setup and hold violations on gating inputs. This ensures that the clock signal is not interrupted or clipped by the gate. Disable clock gating checks by setting the variable timing_disable_clock_gating_checks to true.

What Next

To disable automatic inferring of clock-gating checks, set the environment variable timing_disable_clock_gating_checks to true.

PTE-018

(information) Abandoning fast timing updates.%s

Description

PrimeTime has a built-in efficient algorithm to update the timing of a design, after it has been timed at least once, to accommodate a change that requires this update.

When the user makes a change that invalidates the timing of the design such as new assertions, exceptions, etc, PrimeTime automatically tries to do an incremental update_timing whenever a query is made that requires a timing update. When the number and severity of changes made since the last update is small, the incremental update provides over 10X runtime improvement over the initial timing update.

However, when those changes are large, the incremental update becomes inefficient. To ensure that the incremental update does not result in any slowdown, PrimeTime automatically switches to update from scratch a larger portion of the design than the portion immediately affected by the changes. This message informs the user of this switching. The incremental update remains faster than the update executed after an update_timing -full command.

PrimeTime provides the variable 'timing_update_effort', which can be set to "low", "medium", and "high" to control the switch to full timing updates. It is unlikely that the user would need to change the default setting of the variable. See the manual page for this variable for more information.

What Next

Use 'set timing_update_effort low' if timing_update_effort is medium. Use 'set timing_update_effort medium' if timing_update_effort is high.

PTE-019

(error) report_delay_calculation is not enabled for library '%s'.

Description

The delay calculation report shows detailed performance information about library cells. By default, cell delay reporting is disabled. The technology library vendor can enable delay calculation for a library by specifying the following in the *.lib* source:

library_features(report_delay_calculation);

What Next

Contact your library vendor to request a library with this feature enabled.

PTE-020

(Error) The master clock %s has %d edges in a period. Cannot do frequency multiplication.

Description

If the master clock of a generated clock has more than 3 edges in a period, you cannot generate a frequency multiplied clock from that master clock.

What Next

You can use -edges option to generate the clock.

PTE-021

(error) The generated clock '%s' is in the fanout of clock source %s.

Description

A generated clock can only be in the fanout of a clock source from which it is generated. Here the generated clock is found to be in the fanout of some other clock source.

Feedback

What Next

Generate this clock from a clock in whose fanout it is in.

PTE-022

(error) Generated clock '%s' is not in the fanout of its master clock.

Description

The generated clock is not in the fanout of the master clock with respect to which it has been defined. A generated clock must be in the fanout of its master clock.

What Next

Please check the design and redefine the generated clock to be in the fanout of its master clock.

PTE-023

(warning) The generated clock '%s' has not been expanded, please create or activate its master clock.

Description

A generated clock will not expand if the master clock from which it is generated has not been created or activated. Also if the master clock was given with a -master_clock but does not reach the pin given with -source, this message will be given.

What Next

Please create or activate the master of the generated clock or change the -source pin given. Use the *report_clock* command to see if the master clock is created or inactive.

See Also

- create_clock
- set_active_clocks
- report_clock

PTE-024

(error) The following generated clocks '%s' form a loop.

Feedback

Description

The generated clock listed are defined in a loop. A loop of generated clocks is formed in that there is a circular dependency of generated clock to master clock.

For example, if A and B are generated clocks, and A is generated from B, and B is generated from A, there is a circular dependency.

What Next

Remove cirular dependency in the generated clock sources.

PTE-025

(error) The master of the generated clock '%s' is not connected to any clock source.

Description

The master clock of a generated clock must be either a clock source, or must be connected to a clock source. If it is neither, it is an error.

What Next

Make sure that the master source from which the clock is generated is a clock source or is connected to a clock source.

PTE-026

(information) Found %d generated clock master pins that are not connected to clock sources.

Description

It gives a summary of the number of generated clock master pins that are not connected to clock sources.

What Next

For a more detailed description of which generated clock master pins are not connected to any source, do check_timing -with -verbose option.

PTE-027

(information) Found %d loops in the generated clock network.

Feedback

Description

This message gives a summary of the number of loops in the generated clock network. If there is a circular dependency of generated clock sources and its master, there will be a loop in the generated clock network.

What Next

To get a more detailed description of where the generated clock loops are, use check_timing -verbose.

PTE-028

(warning) The variables timing_disable_bus_contention_check and timing_disable_floating_bus_check are both set to true. Reverting the setting of these variables to the default (false) value.

Description

It is a contradiction to set the variables timing_disable_bus_contention_check and timing_disable_floating_bus_check both to true. This is because setting the variable timing_disable_bus_contention_check implies that the user guarantees that on all multi-driven tri-state busses, disabling of the old drivers in the previous clock cycle is done before the enabling of the new drivers in the current clock cycle. This contradicts what is implied by setting the variable timing_disable_floating_bus_check that enabling of the new drivers occurs before disabling of the old drivers. PrimeTime detects this contradiction and resets the value of the two variables to the default (false) value. In most cases, the user need not adjust these default values.

What Next

Change your script to set both variables timing_disable_bus_contention_check and timing_disable_floating_bus_check to false, or to set only one of them to true.

PTE-030

(warning) No annotated %ss from '%s' to '%s'

Description

You attempted to remove an annotated delay or check between two pins and there was no annotation to remove.

What Next

Verify that the -from and/or -to arguments in the command are correct.

Feedback

PTE-031

(Warning) No annotated timing checks were removed

Description

The *remove_annotated_check* command did not find any checks to remove. If you did not limit the scope of the objects searched, then there are no checks in the design. If you did limit the search to a set of pins, cells, etc., then there are no checks on the objects which you specified.

PTE-032

(Error) Cannot %s annotated check from '%s' to '%s':%s

Description

An attempt to set or remove an annotated check failed because the from and to pins specified are on different cells.

What Next

Specify pins which are on the same cell.

PTE-033

(warning) Some related clocks cannot be expanded to a common clock period within the expansion limit of 100 times per pair of related clock. The subject clocks are: %s, %s, ...

Description

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set) and expands the clock waveforms to the base period.

The timing analysis when this warning is present can potentially miss some paths from being analyzed since some clock pulse relations would not be known.

If the large base period is due to the fact that clock periods do not divide evenly then PrimeTime tries to tweak the periods so that they divide evenly. Use *report_clock* to find out the exact clock period used. In any case, the PrimeTime restricts clock waveform expansion to no more than 100 times per pair clocks.

Feedback

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large base period. You can disable clock-gating checks by setting the environment variable timing_disable_clock_gating_checks to "true".

What Next

Use *set_false_path* to declare that timing paths between unrelated clocks are false.

PTE-035

(Warning) Dynamic loop breaking causes report_timing to track a large number of paths; PrimeTime may run out of memory. Please consider manually breaking some loop paths before issuing report_timing.

Description

You receive this message if the *timing_dynamic_loop_breaking* variable is set to *true* and your design contains a large number of loops, long paths in the loops, and many non-unate arcs in the path. In this case, the *report_timing* command could consume a large amount of memory, eventually causing PrimeTime to run out of memory.

What Next

There are two potential solutions, as follows:

1. Manually break some long loops, then reexecute *report_timing*.
2. Reset the *timing_dynamic_loop_breaking* variable to *false* to return to static loop breaking mode, then reexecute *report_timing*. While in dynamic loop breaking mode, use *report_constraint -all_violators* to verify if there are more constraining paths than static loop breaking mode reports. *report_constraint -all_violators* consumes less memory and always works in dynamic loop breaking mode.

PTE-036

(warning) User specified '%s' in set_clock_gating_check command overwrites what the logic function of the cell or pin implies that clock gating check at pin '%s' should be against the '%s' of the clock.

Description

You receive this message if you execute *set_clock_gating_check* with the *-high* or *-low* option, and this specification is different from the PrimeTime inference based on the logic function of the cell. This message warns you that your current specification takes precedence over the PrimeTime inference.

Feedback

What Next

Verify that your specification of *-high* or *-low* is correct; the PrimeTime inference is usually accurate. If you are satisfied that your specification is correct, no action is required on your part. Otherwise, reexecute the *set_clock_gating_check* command and do not specify *-high* or *-low* so that the PrimeTime inference remains.

PTE-037

(information) Issuing set_operating_conditions for setting analysis mode on_chip_variation.

Description

You receive this message when PrimeTime puts the design in on_chip_variation analysis mode during linking a design. PrimeTime issues a *set_operating_conditions* command with *-analysis_type on_chip_variation*, using best-case and worst-case operating conditions that are the same as the default operating condition in the main library.

What Next

This is an informational message only; no action is required on your part.

PTE-038

(warning) Net "%s" has many driver/load combinations (%d); expect performance degradation.

Description

You receive this message if the *update_timing* command finds a net with a large number of driver/load combinations. This message warns you that PrimeTime could run out of memory, because creating net arcs for each driver/load pair is very memory-intensive. You should expect a performance degradation.

What Next

PrimeTime can, under certain conditions, reduce the timing arcs in the net's fanin to alleviate the problem. This can be achieved by setting timing_reduce_multi_drive_net_arcs to true. Please refer to the man page for timing_reduce_multi_drive_net_arcs(3) for more details.

PTE-039

(information) Issuing set_operating_conditions corresponding to timing_slew_propagation_mode setting.

Feedback

Description

You receive this message when you set the *timing_slew_propagation_mode* variable to *worst_arrival* and have specified a single operating condition using *set_operating_conditions -analysis_type single*. PrimeTime cannot compute accurate transition time for hold timing paths if the analysis type is *single*. In this case, PrimeTime issues this message and executes a *set_operating_conditions* command with *-analysis_type on_chip_variation*, using best-case and worst-case operating conditions that are the same as the single operating condition under which you set the variable.

Conversely, if you set the *timing_slew_propagation_mode* variable back to its default value of *worst_slew*, PrimeTime again issues this message and executes a *set_operating_conditions* command with *-analysis_type single*.

In both cases, PrimeTime echoes the exact command that was issued.

What Next

This is an informational message only; no action is required on your part. However, you can avoid receiving this message by changing your script to use a *set_operating_conditions -analysis_type on_chip_variation* command with an appropriate operating condition.

PTE-040

(Warning) Source Latency defined on pin/port '%s' will overwrite the clock source latency for clock '%s' .

Description

You receive this message if clock source latency is defined for both a clock and its port (source pin). In this case, the source latency for the port takes precedence, because it is more specific.

What Next

If it is acceptable to you for the source latency on the specified pin/port to overwrite the clock source latency, no action is required on your part. Otherwise, reexecute the *set_clock_latency* command with the required specifications.

PTE-041

(warning) Unable to find specified driving cell for port '%s': expected %s/%s %s -> %s.

Description

The driving cell information for the specified port indicates that the port should inherit its drive capability from a certain library cell. This error indicates that the application was

Feedback

unable to locate a matching library cell, a pin on that library cell, or an arc between the pins. This might happen if the *link_path* variable does not contain the library for that cell, or if the cell name or pin name is incorrect. The driving cell information, set by the *set_driving_cell* command, is specified in the text of the message, and you can see it by using the *report_port* command with the *-drive* option.

What Next

If the driving cell requires a library that has not been identified in the link path, the *link_path* variable should be changed to include that library. Otherwise, check the information for errors in the library name, library cell name, or library cell pin name.

See Also

- report_port
- set_driving_cell
- link_path

PTE-042

(warning) Conflicted logic driving pin %s, setting resolved logic value %s on pin %s.

Description

You receive this message because, during the propagation of case analysis or logic constants, update_timing detects two conflicting logic values propagated to a pin. (The update_timing may occur as a result of executing the *update_timing* command or other commands, such as *report_timing*.)

For example, if two strong drivers drive a net with one carrying case analysis *0* and the other carrying case analysis *1*, then a logic conflict would arise.

In these situations, *update_timing* resolves the logic conflict to *0* and continues propagating this forward in the design. The message warns you that a logic conflict has occurred at the specified pin and that it has been resolved to the specified logic value.

Feedback

What Next

The case analysis values that propagated to the pin in question should be changed to prevent the logic conflict from arising, if the resolved value propagated forward is unsuitable. To identify the case values causing the problem, perform the following steps:

1. Enable the generation of a case analysis propagation log file by setting the *case_analysis_log_file* variable to a filename of your choice.
2. Reexecute update_timing, and review the log file to determine the reason for the conflicting values.
3. Correct the problem and reexecute *update_timing*.

See Also

- set_case_analysis
- report_timing
- update_timing
- case_analysis_log_file

PTE-044

(Warning) In the data check from reference pin '%s' to constraint pin '%s', multiple clocked signals arrive at the reference pin. The signal driven by clock '%s' is selected by default. You can use set_data_check -clock to select a specific clock.

Description

You receive this message during data checks performed by *update_timing*, if your design contains multiple clocks per register, the *timing_enable_multiple_clocks_per_reg* variable is set to false, and you did not specify a clock using *set_data_check -clock*. For these conditions, PrimeTime selects a random clock among all clocks that arrive at the reference pin, and issues this message.

PrimeTime supports multiple clocks when the *timing_enable_multiple_clocks_per_reg* variable is at its default setting of true. Normally, if your circuit contains more than one clocked signal that arrives at a reference pin, you should leave this variable at its default setting of true to analyze all clocks, or specify which clock you want to use with *set_data_check -clock*. You can use the *-clock* option even if you are using a library cell for the data check.

If only one clock arrives at the reference pin, you do not need to specify the clock.

Feedback

What Next

If it is acceptable to you for the specified clock to be used by default, no action is required on your part. Otherwise, verify that you intended for multiple clocked signals to arrive at the reference pin of the specified data check. If not, adjust your design accordingly.

If so, do one of the following:

- If you want all clocks to be analyzed simultaneously, set the *timing_enable_multiple_clocks_per_reg* variable to true.
- If you want to select one clock to be analyzed, use *set_data_check -clock* to select the clock to be used.

Finally, reexecute *update_timing*.

See Also

- set_data_check
- update_timing

PTE-045

(warning) The generated clock '%s' does not have a valid master clock because its master clock has been removed.

Description

When a generated clock is created using -add option , it's master clock must be specified using -master_clock option. But if at a later time, the master clock is deleted then the dependent generated clocks would not have a valid master.

What Next

Please make sure if the deletion of master clock is really intended. If it was intended, define a master clock for the generated clock, otherwise the generated clock would not be expanded.

See Also

- create_generated_clock

PTE-046

(information) Reducing %d parallel drivers: Reduction at net: '%s' Reduced to timing arcs from cell: '%s'

Feedback

Description

The parallel timing arcs through the specified net will be reduced to a single driver cell for timing analysis purposes. This optimization is triggered when the variable timing_reduce_multi_drive_net_arcs is set to true.

What Next

Refer to the man pages of timing_reduce_multi_drive_net_arcs(3) and timing_reduce_multi_drive_net_arcs_threshold(3) for more details.

PTE-047

(Information) Cannot reduce parallel timing arcs at net '%s' which has %d drivers x loads Reason: %s

Description

Even though the net drivers-loads product exceeds the threshold value set in *timing_reduce_multi_drive_net_arcs_threshold*, the cells driving this net will not be reduced for the reason specified.

What Next

For more details regarding the restrictions on clock network parallel buffers collapse, check the man pages for *timing_reduce_multi_drive_net_arcs*.

PTE-048

(information) No net arcs %s pin '%s' due to multi-drive timing arcs reduction

Description

The necessary timing arc to annotate does not exist because it was subject to parallel drivers reduction instigated by setting *timing_reduce_multi_drive_net_arcs* to true. Annotations specified as such will be ignored.

What Next

For more details regarding reducing multi-drivers in the clock network, check the man pages for *timing_reduce_multi_drive_net_arcs*. These messages may be suppressed using the following command: "suppress_message PTE-048".

PTE-049

(warning) power rails of operating condition on port '%s' are incompatible with power rails of driving cell '%s'. Driving cell ignored.

Feedback

Description

The power rails specified in the library of a driving cell must be a subset of those specified in the operating condition. Rails are matched by name, and the order of rails much also be identical.

What Next

Consider another operating condition or driving cell.

See Also

- report_port
- set_driving_cell

PTE-051

(warning) Using minimum CRP value due to mismatch in the launching and %s clock edges at the common point.

Description

You receive this message when you execute the *report_crpr* command. This message will occur for one of two reasons. One, the transition sense of the launching and capturing clocks at the common point differ. For example, a rising clock edge through the common point triggers the launching register and a falling clock edge through the common point triggers the capturing register. Two, the capturing register is a level-sensitive latch. In this case two CRP values will be calculated, one corresponding to the opening edge and one corresponding to the closing edge. This means that there will be a mismatch in one of these CRP values and the minimum CRP value will be used.

What Next

For the case when the capturing device is a level-sensitive device the report should clearly indicate what edge is using the minimum CRP.

See Also

- timing_remove_clock_reconvergence_pessimism
- report_crpr

PTE-052

(Warning) For computing a common base period for a number of clocks PrimeTime limits the waveform expansion of the smallest period to be no more than %d times and the waveform expansion of the largest period to be no more than %d times. Since the largest

period is too large compared to the smallest period, no common base period is possible satisfying these limits, and PrimeTime has taken the largest period as the common base period but still has not expanded the smallest period beyond its limit. In certain situations, this can cause paths between these clocks to be unconstrained.

Description

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set).

PrimeTime must ensure that the common base period of a set of related clocks is evenly divisible by every clock in the set. Since clock periods can be arbitrary floating-point numbers, this may require some adjustments to the clock periods. Moreover, to prevent the common base period from becoming too large, PrimeTime must restrict clock waveform expansions by the limits mentioned in the warning message.

Therefore, three cases can occur while computing the common base period:

1. Largest clock period is so large compared to the smallest clock period that no common base period can be computed satisfying the limits. In this case, PrimeTime takes the largest clock period as the common base period but still does not expand the smallest period beyond its limit. 2. A common base period is computed but it has to be decreased to satisfy the limits. 3. A common base period is computed and it already satisfies the limits. This warning message handles the first case.

One potential problem with the first scenario occurs if the maximum expansion of the smallest clock period is still lesser than the largest clock period. In this case, for a path between the two corresponding clocks, PrimeTime does not have enough resolution to apply the single cycle rule and thus the path constraints cannot be computed.

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large common base period. You can disable clock-gating checks by setting the environment variable *timing_disable_clock_gating_checks* to "true".

What Next

Use *set_false_path* to declare that timing paths between unrelated clocks are false.

PTE-053

(Warning) For computing a common base period for a number of clocks PrimeTime limits the waveform expansion of the smallest period to be no more than %d times and the waveform expansion of the largest period to be no more than %d times. PrimeTime has computed a common base period bounded by these limits.

Feedback

Description

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime computes a base period (over all the clocks in the set).

PrimeTime must ensure that the common base period of a set of related clocks is evenly divisible by every clock in the set. Since clock periods can be arbitrary floating-point numbers, this may require some adjustments to the clock periods. Moreover, to prevent the common base period from becoming too large, PrimeTime must restrict clock waveform expansions by the limits mentioned in the warning message.

Therefore, three cases can occur while computing the common base period:

1. The largest clock period is so large compared to the smallest clock period that no common base period can be computed satisfying the limits. In this case, PrimeTime takes the largest clock period as the common base period but still does not expand the smallest period beyond its limit 2. A common base period is computed but it has to be decreased to satisfy the limits 3. A common base period is computed and it already satisfies the limits. This warning message handles the second case.

Sometimes unexpected clock relationships due to automatically inferred clock-gating checks may cause a very large common base period. You can disable clock-gating checks by setting the environment variable *timing_disable_clock_gating_checks* to "true".

What Next

Use *set_false_path* to declare that timing paths between unrelated clocks are false.

PTE-054

(Information) Zero transition time used at to pin of annotated arcs. Delays on not annotated delay arcs will be estimated using best available slew.

Description

This message is issued when more than 95 percent of delay arcs on a design have annotated values and *timing_use_zero_slew_for_annotated_arcs* is set to *auto*, or when *timing_use_zero_slew_for_annotated_arcs* has been set to *always. This functionality is intended for use only on a design that is completely (or almost completely) SDF annotated, and in a flow which does not require transition times.*

Feedback

What Next

See man page of *timing_use_zero_slew_for_annotated_arcs* for more details on this functionality.

PTE-055

(warning) Variable "%s" must be set before link

Description

The PrimeTime variable indicated can only be consumed before the design is linked. That is, the current change in value will only be honored the next time the link_design command is invoked.

What Next

Please verify that the current setting is correct. If so, either invoke the link_design command or move the variable setting to a position prior to invoking the link_design command and rerun your script.

PTE-056

(Warning) Due to the value set by timing_crpr_threshold_ps, the CRP displayed in the timing_report will lie in the range: %g < CRP < %g.

Description

You receive this message when you execute the *report_crpr* command. In order to reduce the computational complexity of deriving a CRP value during *update_timing*, different compute mechanisme are utilized in the production of the CRP values for *report_timing* and *report_crpr*. This may result in a difference between the CRP values produced by *report_timing* and *report_crpr*. The difference will not be greater than the value of the variable, *timing_crpr_threshold* and will lie in the range: CRP(report_crpr)-threshold < CRP < CRP(report_crpr). Hence, the value of CRP used in *report_timing*, if different to *report_crpr*, will always be more pessimistic.

What Next

If more accuracy is required in the CRP value issued by *report_timing* set the variable *timing_crpr_threshold_ps* to a lower value and execute a full *update_timing*. Setting the variable *timing_crpr_threshold_ps* to a low value will result in significantly increased runtime and memory usage.

Feedback

See Also

- report_crpr
- timing_remove_clock_reconvergence_pessimism
- timing_crpr_threshold_ps

PTE-057

(Warning) Transition times on not annotated delay arcs have been set to zero. Cannot perform max_transition checking.

Description

This message issues if a zero value is used for transition time on the load pins of fully delay annotated arcs. For this reason, *report_constraint -max_transition* is disabled.

Fully annotated arcs are those with values for both rise and fall either read from an SDF file, or set with the command *set_annotated_delay*.

Zero transition times are used when more than 95 percent of delay arcs on a design have annotated values and the varibale *timing_use_zero_slew_for_annotated_arcs* is set to *auto*, or when *timing_use_zero_slew_for_annotated_arcs* is set to *always* (irrespective of the percentage of annotated delay arcs).

What Next

See man page of *timing_use_zero_slew_for_annotated_arcs* for more details on this functionality. Setting this this variable to *never will re-enable calculation of slews, and max_transition constraint checking.*

PTE-058

(Warning) timing_use_zero_slew_for_annotated_arcs will be disabled when slew propagation mode is not *worst_slew*.

Description

The functionality enabled by *timing_use_zero_slew_for_annotated_arcs* is compatible only with *worst_slew* slew propagation and will not be invoked when *timing_slew_propagation_mode* is set to anything other than *worst_slew.*

What Next

See man page of *timing_use_zero_slew_for_annotated_arcs* for more details on this functionality.

Feedback

PTE-059

(Error) timing_use_zero_slew_for_annotated_arcs cannot be enabled unless timing_slew_propagation_mode is worst_slew.

Description

The functionality enabled by *timing_use_zero_slew_for_annotated_arcs* is compatible only with *worst_slew\pB slew propagation mode.*

What Next

Setting *timing_slew_propagation_mode to worst_slew will allow timing_use_zero_slew_for_anntoated_arcs to be enabled. See man page of timing_use_zero_slew_for_annotated_arcs for more details on this functionality.*

PTE-060

(warning) No clock-gating check is inferred for clock %s at pins %s and %s of cell %s.

Description

Unless the variable *timing_disable_clock_gating_checks* is set to true, PrimeTime automatically infers clock-gating checks. For this cell, PrimeTime cannot infer a clock-gating check. This happens because the logic of this cell does not provide enough information to determine whether to perform a gating check on the high level or low level of the input clock signal.

What Next

Use *set_clock_gating_check* with either the *-high* or *-low* option to specify the level of the clock.

PTE-061

(Warning) Since the launching device is a level-sensitive latch and the variable timing_early_launch_at_borrowing_latches is set to TRUE, the CRP for any paths launched from the latch data pin will be zero.

Description

You receive this message when you execute the *report_crpr* command. Since the same (early) clock arrival time is used to both launch and capture data at a level-sensitive latch with borrow, normal application of CRPR may be optimistic. For this reason the CRP is set to zero for such paths. For more details see the man page for the variable *timing_early_launch_at_borrowing_latches*.

Feedback

What Next

In order to apply CRPR to paths launched from a borrowing data pin set the variable *timing_early_launch_at_borrowing_latches* to FALSE. This is recommended for PrimeTime to minimize the overall pessimism throughout a latch-based design.

See Also

- report_crpr
- timing_remove_clock_reconvergence_pessimism
- timing_early_launch_at_borrowing_latches

PTE-062

(Information) Accepted db or HyperScale inherited disable timing arcs to break loops.

Description

Accepted db inherited disable timing arcs to break loops due to a true value of the variable *timing_keep_loop_breaking_disabled_arcs*. Variable *timing_keep_loop_breaking_disabled_arcs* is false by default.

Alternatively, accepted HyperScale inherited disable timing arcs to model loop breaking. The variable *timing_keep_loop_breaking_disabled_arcs* has no effect in these cases.

There may still be loops in the design that the db inherited disabled timing arcs did not break, they are broken using the default loop breaking technique.

There is a difference between DC and PT where additional set_case_analysis and set_disable_timing commands will not remove db inheritied disabled timing arcs.

A boolean attribute *is_db_inherited_disabled* has been added to the class timing_arcs, where true indicates an arc is a db inherited disabled arc.

The command *remove_disable_timing* may be used to remove db inherited disabled timing arcs, since these arcs are considered to be under user control.

To remove all db inherited disable timing arcs for loop breaking, issue command *remove_disable_timing* [get_timing_arcs -of [get_cell *] \ -filter "is_db_inherited_disabled == true"]

See Also

- report_disable_timing
- timing_keep_loop_breaking_disabled_arcs

Feedback

PTE-063

(Warning) Resetting value of variable timing_keep_loop_breaking_disabled_arcs will have no effect.

Description

Resetting value of variable *timing_keep_loop_breaking_disabled_arcs* will have no effect after accepting db inherited disable timing arcs to break loops. This value of this variable is only checked during linking.

If the user wishes to remove the db inherited disable timing arcs, issue command *remove_disable_timing* [get_timing_arcs -of [get_cell *] \ -filter "is_db_inherited_disabled == true"]

See Also

- report_disable_timing
- timing_keep_loop_breaking_disabled_arcs

PTE-064

(information) Related clock set %d includes clock '%s' with period %.3f.

Description

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime assigns an integer identification number and computes a base period (over all the clocks in the set). This message says that this clock is a member of this clock set.

What Next

It is recommened that you mark paths between unrelated clocks as false.

See Also

- set_clock_groups
- set_false_path

Feedback

PTE-065

(information) Related clock set %d has base period %.3f.

Description

Two clocks are related if there exists a true path between them. They can also be related if they are respectively related to a third clock. For example, if CLK1 is related to CLK2 and CLK2 is related to CLK3, then CLK1 is related to CLK3. That is, CLK1 is related to CLK3 even though there may not be a true path between them. Using the relatedness relation, PrimeTime partitions the clocks in the design into mutually exclusive (related) clock sets. For each clock set, PrimeTime assigns an integer identification number and computes a base period (over all the clocks in the set). This message shows the base period of this clock set.

What Next

It is recommened that you mark paths between unrelated clocks as false.

See Also

- set_clock_groups
- set_false_path

PTE-066

(Warning) Zero transition time will be used at to pins of annotated arcs. Delays on not annotated delay arcs will be estimated using best available slew.

Description

If more than 95 percent of delay arcs on a design have annotated values, the SDF flow is automatically switched on during the timing update or during the execution of *report_annotated_delay*. Note that issuing *read_sdf* with the *-verbose* option will implicitly call *report_annotated_delay*. Switching on of the SDF flow will result in faster performance of update_timing, at the expense of no longer calculating the slews on the load pins of annotated arcs.

This functionality is intended for use on a design that is completely (or almost completely) SDF annotated, and in a flow which does not require transition times.

You can switch on the SDF flow explicitly by setting the variable *timing_use_zero_slew_for_annotated_arcs* to always.

Feedback

What Next

See man page of *timing_use_zero_slew_for_annotated_arcs* for more details on this functionality.

To avoid the SDF flow being automatically switched on when the value of *timing_use_zero_slew_for_annotated_arcs* is *auto* and more than 95% of arcs in the design are annotated, set *timing_use_zero_slew_for_annotated_arcs* to *never*.

PTE-067

(warning) Setting this variable to a lower value can cause a significant performance degradation during a timing update.

Description

You receive this message when setting the variable *timing_crpr_threshold_ps*. Turning CRPR on can cause a noticable performance degradation both in terms of CPU and capacity. Further to this, setting the variable to values lower than the default (20ps) can further degrade performance with little corresponding increase in the accuracy of the CRP calculation. See the man page for *timing_crpr_threshold_ps* for more details.

What Next

The recommended setting for the variable *timing_crpr_threshold_ps* is about one half of the stage (gate plus net) delay of a typical stage in the clock network.

PTE-068

(information) Using CRPR on a pre-layout clock network can cause performance degradation during a timing update.

Description

You receive this message during a timing update. The CRPR algorithm is optimized for post layout clock networks. Because of this fact it is not recommended to use this algorithm on a pre-layout (pre-clock tree synthesis) clock network as it can lead to degradation in both CPU performance and in capacity.

What Next

In order to alleviate performance concerns turn CRPR off by setting the variable *timing_remove_clock_reconvergence_pessimism* to false.

See Also

- timing_remove_clock_reconvergence_pessimism

Feedback

PTE-069

(error) The requested clock sense at pin '%s' for clock '%s' does not exist. Propagating the '%s' sense of the clock through this pin.

Description

There is a 'set_clock_sense' directive at the pin given and the requested clock sense does not exist at the pin for the given clock. This may be due to a conflicting 'set_clock_sense' directive on a previous pin or it may be because the only clock paths to that pin are not of the sense requested.

What Next

Remove the conflicting 'set_clock_sense' directives.

PTE-070

(information) A non-unate path in clock network detected. Propagating both inverting and noninverting senses of clock '%s' from pin '%s'.

Description

The clock tree for the specified clock contains non-unate paths. Clock networks normally do not contain cells such as exclusive-OR gates which have non-unate behavior. This implies that both inverting and noninverting clock waveforms reach the specified pin. This is an informational message that such a pin has been detected and that PrimeTime is propagating both senses of clock.

What Next

If you want to control the sense of the clock used through this pin, use the command 'set_clock_sense'.

PTE-071

(warning) The '%s' edge of clock '%s' through pin '%s' causes the clock to both rise and fall. A generated clock is needed at this pin.

Description

The clock tree for the specified clock contains two half unate paths such that the clock edge given causes both a rising and falling clock edges and the other edge of clock causes no change. This type of edge relationship requires that a generated clock be added to properly model the edge relationships. To model a pulse generator, use the 'create_generated_clock' command with a non-monotonic edge specification such as (1 1 3) or (2 2 4).

Feedback

What Next

Place a generated clock at the given pin.

PTE-072

(Warning) SI analysis is not enabled, therefore the adaptive CRPR engine will not be used.

Description

You receive this message during a timing update if the variable *timing_crpr_enable_adaptive_engine* is set to TRUE and SI analysis is turned off (*si_enable_analysis*). The adaptive CRPR engine applicable only when SI is turned on therefore will have no effect on the non-SI timing update.

See the man page for *timing_crpr_enable_adaptive_engine* for more details.

What Next

If the users intention is to perform an SI analysis then set the variable *si_enable_analysis* to TRUE. Otherwise turn off the adaptive CRPR engine by setting *timing_crpr_enable_adaptive_engine* to FALSE.

See Also

- timing_remove_clock_reconvergence_pessimism

PTE-073

(Warning) Turning off Adaptive CRPR.

Description

You receive this message during a timing update if the variable *timing_crpr_enable_adaptive_engine* is set to TRUE and either the max SI iteration count (set by *si_xtalk_exit_on_max_iteration_count*) or the max SI incremental iteration count (set by *si_xtalk_exit_on_max_iteration_count_incr*) is set to 1.

The adaptive CRPR engine requires at least two SI iterations to perform its analysis. Because of this the adaptive engine is turned off and standard CRPR analysis is performed.

See the man page for *timing_crpr_enable_adaptive_engine* for more details.

What Next

Set the variable *si_xtalk_exit_on_max_iteration_count* to at least 2 and repeat the timing update.

Feedback

See Also

- si_xtalk_exit_on_max_iteration_count
- timing_remove_clock_reconvergence_pessimism

PTE-074

(warning) At pin '%s' clock '%s' does not have the needed %s edge.

Description

The clock tree contains half unate timing arcs or disable timing commands that have disabled the needed rise or fall edge. The register clock pin given will not have the clock assigned to it and will not be timed.

What Next

Alter clock network to propagate the needed clock edge to this register.

PTE-075

(error) Generated clock '%s' has no path to its master clock.

Description

The generated clock has no path to the master clock on which it has been defined. This may be because there is no physical path, or because the generated clock has been defined using "-combinational" and the generated clock is not in the direct combinational fanout of the master clock. A propagated source latency of zero will be used from the master clock to the generated clock.

What Next

Please check the design and redefine the generated clock to be in the fanout of its master clock.

PTE-076

(Information) Setting %s to TRUE and updating timing.

Description

To conserve memory, PrimeTime retains arrival, required and slack information only where necessary to service the timing update and standard reporting requirements. This warning was issued to indicate that the command the user issued does not work under the current analysis settings.

Feedback

What Next

No explicit action is required on your part. Under these circumstances, PrimeTime adjusts the analysis settings as needed, updates timing and proceeds with the execution of the command.

See Also

- timing_save_pin_arrival_and_required
- timing_save_pin_arrival_and_slack

PTE-077

(Information) It is recommended that the variable %s be set before the initial timing update for optimal performance of this command.

Description

This command requires that additional slack-related info be available throughout the design for execution. To produce this information, an additional timing update will be incurred. In order to avoid the extra CPU cost of this additional update the variable should be set to TRUE before the initial timing update in this flow.

What Next

The optimal flow for any commands requiring pin arrivals and slacks is to set the associated variable to TRUE before the initial timing update. This prevents the need for additional work before and command requiring arrivals and slacks is executed.

PTE-079

(Warning) The %s attribute does not exist on the given pin, or one of the pins of the given net, because %s is set to FALSE.

Description

To conserve memory, PrimeTime retains arrival, required and slack information only where necessary to service the timing update and standard reporting requirements. This warning was issued to indicate that the attribute the user queried does not exist for the given pin, or one of the pins of the given net, under the current analysis settings.

What Next

Set the variable appearing in the warning message to TRUE.

Feedback

See Also

- timing_save_pin_arrival_and_slack
- timing_save_pin_arrival_and_required

PTE-080

(Error) pulse clock sense merging at pin: '%s' for clock: '%s' The clock will not propagate forward from this pin.

Description

A pulse clock is combinationally combining with another sense of the same clock. PrimeTime does not resolve this conflict. Any registers down stream from this point will be have this clock assigned to them.

What Next

Resolve the conflict by specifying the sense of the clock used through this pin by using the command 'set_clock_sense'.

PTE-081

(error) Can not honor set_clock_sense -pulse option at pin '%s'. Clock '%s' is missing needed rise and/or fall, or has conflicting high or low pulse types at this pin

Description

The user has specified a set_clock_sense -pulse option at the given pin. The needed clock senses were not available at this pin. For example, a 'rise_triggered_high_pulse' expects to find a clock source rise to this pin rise path and a clock source rise to this pin fall path. If both paths can not be found this message will be issued. There can be conflict between the pulse type propagating and that set by set_clock_sense -pulse. For example, if the propagating pulse is high and user sets a low pulse type at a pin, then this message will be issued. The pulse clock assignment for registers down stream from this pin will not be correct.

What Next

Change the options to the command 'set_clock_sense'.

PTE-082

(warning) Connected pin groups were detected that may generate a very large number of loops. Please check the validity of this feedback logic by inspecting the connected pin groups above. Dynamic loop breaking is being disabled.

Feedback

Description

The design contains one or more regions of logic which have combinational feedback. PrimeTime has identified these regions of connected pin groups which have the potential to generate a large number of combinational loops. Because the number of loops increases exponentially with the number of pins, these regions have the potential to exceed the limits of the machine during dynamic loop breaking. Dynamic loop breaking is being disabled.

What Next

Check the listed pin groups to ensure that the combinational feedback loops are expected and correct in the design. If they are unavoidable, manually disable dynamic loop breaking by setting the variable timing_dynamic_loop_breaking to false.

PTE-083

(warning) Connected pin groups were detected that generate a large number of loops. Here is the connected pin group that has generated the largest number of loops so far. Dynamic loop breaking will continue, which may exceed the machine's capabilities.

Description

The design contains one or more regions of logic which have combinational feedback. PrimeTime has identified a region of logic which has a very large number of combinational loops. The pins in this group will be reported, and PrimeTime will continue to attempt dynamic loop breaking. This may result in exceeding the limits of the machine. The system may become unstable and an "out of memory" error may occur.

What Next

Check the listed pin groups to ensure that the combinational feedback loops are expected and correct in the design. If they are unavoidable and dynamic loop breaking proves to be too costly, manually disable dynamic loop breaking by setting the variable timing_dynamic_loop_breaking to false.

PTE-084

(warning) Parasitics on the net "%s" have been overridden, because the net is part of an ideal network.

Description

This message is displayed during a timing update for ideal nets that have parasitics annotated. The effect of leaving ideal networks in the design is that the parasitics are ignored and the net delay is ideal. This may obscure timing violations.

Feedback

What Next

To display the ideal networks is the design use the *report_ideal_network* command. To remove ideal networks that are not intended use the *remove_ideal_network* command.

See Also

- remove_ideal_network
- report_ideal_network

PTE-085

(Warning) the calculated SHPR curve is not monotonic.

Description

The calculated interdependent setup/hold curve is not monotonic. The results of setup_hold_pessimisim_reduction (SHPR) may be inaccurate.

What Next

Check SHPR library data of setup/hold value and make sure they are characterized properly.

PTE-086

(Warning) Target constraint value is beyond the boundary of characterized SHPR library. Using nearest boundary value instead.

Description

The target constraint value, wich is required by SHPR optimization parameter, is beyond the boundary of characterized SHPR library. To avoid optimism, PrimeTime use the nearest boundary value as the updated target constraint value.

What Next

Check SHPR library data of setup/hold value and make sure they are characterized properly and the characterization scale covers the target constraint value.

PTE-087

(Warning) %s constraint set on %s '%s' will be ignored.

Feedback

Description

Pulse clock constraint set on the design, lib cell, instance or clock will be ignored. This can due to the fact that the design may not have any pulse generator cells, the constrained lib cell may not be a pulse generator or is not instantiated in the design, the constrained instance is not a pulse generator or the clock may not driving any pulse generators.

PTE-088

(Information) report_analysis_coverage was reported with timing_enable_pulse_clock_constraints variable set to FALSE.

Description

timing_enable_pulse_clock_constraints was set to FALSE during *report_analysis_coverage* for *-check_type min_pulse_width* and then set to its preset value i.e. TRUE after reporting.

PTE-090

(Error) No output clock defined on the output '%s' of the PLL.

Description

You receive this message if the design has a PLL and there is no clock defined on the output that is connected to the feedback pin of the PLL.

What Next

You should define a generated clock at the output of every PLL using the *create_generated_clock* command with the required specifications.

PTE-091

(Error) The feedback pin '%s' has no path to its PLL output clock.

Description

You receive this message if the design has a PLL and the feedback path is not connected correctly. Ideally, the feedback pin of a PLL should be connected to an output pin of the PLL. In addition, a generated clock should be defined on the output that is connected to the feedback pin.

Feedback

What Next

You should check that there is a path from the output of the PLL to the feedback pin. In addition, define a generated clock at the output of every PLL using the *create_generated_clock* command with the required specifications.

PTE-092

(Warning) The timing arc from the reference pin to the output pin of the PLL '%s' is not positive unate. Not performing the PLL adjustment for the arc.

Description

You receive this message if some of the arcs in the library model of the PLL do not have positive unate arcs from the reference clock pin to the output clock pin.

PTE-093

(Warning) the -delay_calculation_only_mode flag is ignored because of the current variable settings.

Description

You may receive this message in the following case(s):

"*timing_use_zero_slew_for_annotated_arcs* == always"

"*timing_use_zero_slew_for_annotated_arcs* == auto and more than 95 percent of delay arcs on a design have annotated values"

What Next

See man page of *timing_use_zero_slew_for_annotated_arcs* for more details.

PTE-094

(Warning) the si_xtalk_exit_on_max_iteration_count variable is ignored; only one iteration is performed

Description

You receive this warning because the *-delay_calculation_only_mode* option of the *write_sdf* command is exclusive with:

si_enable_analysis==true and *si_xtalk_exit_on_max_iteration_count*>1

Feedback

Since only one iteration is performed, the results may be less accurate (but always pessimistic.)

What Next

Do nothing if this behavior is acceptable to you or remove the *-delay_calculation_only_mode* option if you insist in running multiple SI iterations. Note the general issue that using SDF generated after several SI iterations can lead to optimistic results if not done properly.

PTE-095

(Error) Generated clock is not defined on the output pin of the PLL connected to the feedback pin; not performing the PLL correction.

Description

You receive this error because PLL cell output defined using *-pll_output* connected to the feedback pin defined using *-pll_feedback* does not have a generated clock defined on it.

Since the generated clock is not defined, no PLL correction would be performed.

What Next

If you want to perform PLL correction, define a generated clock at the PLL output connected to the feedback pin of the PLL.

PTE-097

(fatal) An exceptionally long combinational path with greater than 276,000 pins through '%s' is encountered. PrimeTime will exit its current session.

Description

PrimeTime does not time paths that have exceptionally large combinational depth for reasons of memory efficiency.

What Next

Consider breaking combinational paths that span across more than 276,000 pins. Note that there can be multiple paths which have such exceptionally large combinational depths and all such paths need to be broken to correctly time the design.

PTE-098

(Warning) Avoid setting timing_use_zero_slew_for_annotated_arcs to 'always' when SI analysis is enabled.

Feedback

Description

Setting *timing_use_zero_slew_for_annotated_arcs* to *always* foregoes slew propagation altogether. If SI analysis is enabled, then aggressor data with valid propagated slews are needed to accurately compute the SI impact on stage delay.

What Next

Use the *never* setting to make sure that the requisite slew propagation is performed. The *auto* setting could be used with the understanding that any non-annotated delays being calculated would still be SI inaccurate.

PTE-099

(Warning) Setting timing_use_zero_slew_for_annotated_arcs to never may slow down timing analysis.

Description

Setting *timing_use_zero_slew_for_annotated_arcs* to *never* forces slew propagation over arcs which have user-annotated. This mode is not recommended as the performance impact on timing update may be severe.

What Next

See man page of *timing_use_zero_slew_for_annotated_arcs* for more details.

To avoid performance degradation, set *timing_use_zero_slew_for_annotated_arcs* to *auto*.

PTE-100

(Warning) The transparent latch transitive slack feature cannot be used when the variable timing_slack_calculation_mode is set to slow. Transitive slack analysis will not be run.

Description

Setting *timing_enable_transitive_latch_slack_analysis* to *true* enables the transparent latch transitive slack feature. However, when the variable *timing_slack_calculation_mode* is set to *slow*, the feature cannot be used.

What Next

Try setting *timing_slack_calculation_mode* to *fast*.

PTE-101

(Warning) No clock-gating check was inferred for clock %s at pins %s and %s of cell %s because no clock pins could be found in the fanout for the propagating clock.

Feedback

Description

Unless the variable *timing_disable_clock_gating_checks* is set to true, PrimeTime automatically infers clock-gating checks. For this cell, PrimeTime cannot infer a clock-gating check because no clock pins of latches or registers were found in the fanout of the cell using this clock. The warning is not issued when the output of the cell is not part of the clock tree.

See Also

- set_clock_gating_check

PTE-102

(Information) The value for the variable timing_crpr_threshold_ps has been reset to the minimum allowable value of %g

Description

The variable *timing_crpr_threshold_ps* cannot be set to a value lower than a minimum limit. PrimeTime will automatically adjust a lower setting to the minimum allowable value.

See Also

- timing_crpr_threshold_ps

PTE-103

(Warning) Loop(s) were detected in the generated source latency network of clock %s. PrimeTime is prevented from computing the source latency of this clock with complete accuracy.

Description

The source latency network of a generated clock refers to the set of paths between the source pin of its master clock and the source pin of the generated clock. Unless the generated clock has been declared with *-combinational*, these paths might traverse through sequential elements as well as combinational cells.

This warning means that this network contains at least one loop where a path feeds back into itself. PrimeTime considers paths traversing the entire loop as invalid for determining the generated clock's latency, but this handling might not correspond to your design intent or that the generated clock has not been correctly specified. In rare cases, the latency shown by *report_timing* might not match the latency printed by *report_timing -path_type full_clock_expanded* when this warning occurs.

Feedback

What Next

Use *check_timing -override_defaults generated_clocks -verbose* to see the set of pins forming the loop. It is strongly advised that you alter your clock network specification to eliminate the loop. Perhaps the *-combinational* switch has been omitted in error or the *timing_gclock_source_network_num_master_registers* variable needs to be set. Equally, the clock network topology itself might need to be reconfigured to break the cycle using *set_disable_timing* or *set_clock_sense -stop_propagation* within the generated source network.

See Also

- check_timing
- create_generated_clock
- report_timing
- set_clock_sense
- set_disable_timing
- timing_gclock_source_network_num_master_registers

PTE-108

(Information) SDF delays annotated on multiple arc path from '%s' to '%s'.

Description

No direct timing arc could be found between the pins specified in the IOPATH statement in the SDF file. Because a path between the two cell pins exists and delays for all arcs in the path can be determined, the annotation is applied to this path.

For example, if a cell with the input pin 'A', the inout pin 'IO', and the output pin 'Y' has two arcs: one 'A -> IO' and the other 'IO -> Y', then the SDF file can specify delays between 'A' and 'Y', and between 'IO' and 'Y':

(IOPATH IO Y (2.691::2.691) (2.418::2.418)) (IOPATH A Y (5.060::5.060) (5.074::5.074))

In this case, arc delays 'A -> IO' will be calculated by substracting the delays for the arc 'IO->Y' from the total path delay.

See Also

- read_sdf

Feedback

PTE-109

(warning) At pin '%s' clock '%s' does not have the %s edge, so clock gating %s check will not be performed.

Description

The clock tree contains half unate timing arcs or disable timing commands that have disabled the rise or fall edge. The clock gating check will only support a check against the available edge.

What Next

If the behavior is not desired, alter clock network to propagate the needed clock edge to the clock gating pin.

PTE-110

(fatal) Internal error, too many timing contexts %s to analyze successfully. PrimeTime will exit its current session.

Description

The analysis is too complicated for PrimeTime and anaysis will not proceed with the present design, constraints, and variable settings. Certain variables contribute heavily to the analysis complexity.

What Next

It may be that analysis complexity can be reduced by one or more of the following:

Try running update_timing -full instead of repeatedly using incremental timing updates. Try disabling the variable timing_enable_through_paths. Try increasing the value of the timing_crpr_threshold_ps variable. Try reducing the number of modes or clocks analyzed simultaneously. Please check if there are PTE-160 warnings in the log, then this issue is likely due to borrowing related problem especially if PTE-053 is also encountered.

If these methods do not work, please file a STAR to let Synopsys know your design is hitting the analysis capacity limit.

PTE-111

(Warning) The stack size allocated for PrimeTime to run might be too small. It is recommended that you run PrimeTime with a stack size of %d MB to avoid problems in designs with exceptionally long combinational paths.

Feedback

Description

The allocated stack size is either unknown or possibly too small for running PrimeTime. This can lead to analysis failure in designs with exceptionally long combinational paths.

What Next

At the UNIX prompt, use the 'limit' command to set the stack size to the recommended value. For more information, see the PrimeTime Suite Installation Notes.

PTE-112

(information) Variable 'timing_reduce_parallel_cell_arcs' has been changed from true to false because advanced waveform propagation is enabled.

Description

Because advanced waveform propagation mode has been enabled, merging of parallel cell arcs has been disabled to improve accuracy.

What Next

This is an informational message. No action is required on your part. For more information, see the PrimeTime user guides.

PTE-113

(Error) There is a clock path that goes through pin '%s' and pin '%s', which are defined as exclusive.

Description

This error occurs when there is a mux-clock exclusivity relationship defined between a pin and one of its fanout pins.

What Next

Make sure no pin and its fanout pins are defined in a mux-clock exclusivity relationship, using 'set_clock_exclusivity' command.

PTE-114

(warning) The frequency at pin %s is outside the bounds of the lookup table defined at pin %s of the library cell %s. Extrapolation will be applied to compute the frequency-based max_capacitance. The frequency value is %.6f, and the table bounds are %.6f, %.6f.

Feedback

Description

Frequency-indexed lookup tables for max_capacitance are defined on the output or inout pins of a library cell.If the frequency at the pin is not within the bounds of the indexing frequencies specified in the library, extrapolation will be applied.

What Next

Either the library pin should be characterized with enough frequency indices to cover the design, or the design should be changed to stay within the library frequency characterization ranges.

PTE-115

(Error) There is a clock path that goes through pin '%s' more than once, which is defined as exclusive.

Description

This error occurs when there is a mux-clock exclusivity relationship defined on a pin, and there is a clock path that goes through the pin more than once.

What Next

Make sure no pin and its fanout pins are defined in a mux-clock exclusivity relationship, using 'set_clock_exclusivity' command. Also, make sure that the exclusive pin is not on any combination loops.

PTE-116

(Warning) The exclusivity set with '%s' option on the output pin '%s' is ignored, due to the violation of condition %d.

Description

The clock exclusivity relationship defined by the *set_clock_exclusivity* command for a cell output was not applied, due to one or more of the following conditions:

1. No clock reaches the output pin of the exclusivity cell from its inputs.
2. There is a clock reaching the select lines of the MUX exclusivity cell.
3. All the select lines of the MUX exclusivity cell are defined as constants.
4. Only one input pin (of the specified inputs) of the MUX exclusivity cell has clock(s) reaching it.

Feedback

5. The output pin of the MUX exclusivity cell is a clock source.
6. There are non-unate clock traces reaching the input pin of the MUX exclusivity cell.

What Next

It is not possible to set an exclusivity relationship when any of these conditions exists. Adjust the the clock definitions, the exclusivity definition, or the netlist logic to resolve the condition.

PTE-117

(warning) PT-SI license is required to read the frequency-based max_capacitance constraint tables from the library. PrimeTime will ignore these library tables.

Description

Frequency-based max_capacitance is only enabled in the presence of a PT-SI license.

What Next

Frequency based lookup tables will be ignored for the application of max_capacitance constraints

---

PTE-118

(Information) An internal max_time_borrow was set at pin '%s' with value %g for %s paths in a particular timing context, in order to limit the borrow of critical timing loops

Description

When the variable *timing_limit_borrow_for_critical_latch_loops* is true, internal max_time_borrow values may be set on transparent latches. The max_time_borrow becomes the constraint for the timing context, and limits the time given to startpoint for the borrow path. Only paths of a particular timing context are affected, and this max_time_borrow is rise/fall specific.

What Next

If this behavior is undesired, the variable *timing_limit_borrow_for_critical_latch_loops* can be set to false. Alternately, setting a max_time_borrow with the command *set_max_time_borrow* at the particular pin can prevent an internal max time borrow from being set.

Feedback

PTE-119

(Warning) Computation of internal max_time_borrow took too long at pin '%s' for %s paths in a particular timing context. The computation will be aborted and an internal max_time_borrow that is smaller than optimal may be used.

Description

When the variable *timing_limit_borrow_for_critical_latch_loops* is true, internal max_time_borrow values may be set on transparent latches. The internal max_time_borrow value is computed by tracing the design to find out the latest nonloop arrival value for the timing context. If the trace takes a long time, it will be aborted and potentially a lower than optimal value will be used for the internal max_time_borrow. This can cause nonloop paths incoming to the latch to appear to be violating even when there is able time available for borrowing at the latch.

Even if this message is issued during update timing, it may be that later computations remove the need for an internal max_time_borrow at the pin, so an internal max_time_borrow may not be set for the pin at the end of update_timing.

What Next

If this behavior is undesired, the variable *timing_limit_borrow_for_critical_latch_loops* can be set to false.

A more specific solution is to set a max_time_borrow value with the command *set_max_time_borrow* at the particular pin. This will prevent an internal max time borrow from being computed for the pin.

PTE-120

(Information) An internal max_time_borrow for required times was set at pin '%s' with value %g for %s paths in a particular timing context, in order to avoid overconstraining the fanin of critical loops.

Description

When the variable *timing_limit_borrow_for_critical_latch_loops* is true, Required times passing through loop breaker latches may be limited to be no earlier than the earliest nonloop required time. This increases the slack in the fanin of critical loops.

What Next

If this behavior is undesired, the variable *timing_limit_borrow_for_critical_latch_loops* can be set to false.

Feedback

PTE-121

(Warning) Computation of nonloop required times took too long at pin '%s' for %s paths in a particular timing context. The computation will be aborted and no internal limit for required times will be used.

Description

When the variable *timing_limit_borrow_for_critical_latch_loops* is true, required times at loop breaker latches are limited to the earliest nonloop required time. When PTE-121 is issued, the computation of the earliest nonloop required time was aborted, and the nonloop required time will not be used to limit the required time at the loop breaker latch.

What Next

If this behavior is undesired, the variable *timing_limit_borrow_for_critical_latch_loops* can be set to false.

PTE-122

(Information) When the variable timing_early_launch_at_borrowing_latches is set to false, negative slack is not passed upstream of loop breaker latches.

Description

When the variable *timing_early_launch_at_borrowing_latches* is true (the default), and the variable *timing_enable_through_paths* is set to true, Negative slack from violating paths in the fanout of loop breaker latches is propagated to the fanin of the loop breakers.

When the variable *timing_early_launch_at_borrowing_latches* is set to false (not the default), Negative slack from violating paths in the fanout of loop breaker latches is not propagated to the fanin of the loop breakers. As a result, paths ending and borrowing at loop breaker latches may see zero slack even if the downstream paths from the loop breaker are violating.

What Next

Try setting *timing_early_launch_at_borrowing_latches* to the default value (true).

PTE-123

(Information) When the variable timing_early_launch_at_borrowing_latches is set to false, the variable timing_limit_borrow_for_critical_latch_loops is ignored.

Feedback

Description

When the variable *timing_early_launch_at_borrowing_latches* is *true* (the default), and the variable *timing_limit_borrow_for_critical_latch_loops* is set to *true*, the tool attempts to limit the borrow amount in critical latch loops.

The borrow limiting feature is disabled if the variable *timing_early_launch_at_borrowing_latches* is set to the non-default value of *false*.

What Next

Try setting *timing_early_launch_at_borrowing_latches* to the default value (*true*).

PTE-124

(Information) Annotation on %s check arc from pin '%s' to pin '%s' will override annotated incremental value.

Description

Incremental annotated values on check arcs are combined with the calculated values only. Annotated values will not interact with incremental values.

What Next

The incremental value should should be included in the the annotated value.

PTE-125

(warning) New technology license NTA6 is not available.

Description

To apply constraint sigma multipliers to hold constraint arcs for non-POCV analysis, you need an available New Technology license NTA6. If you do not have this license, the tool ignores the constraint sigma multipliers during the calculation of hold constraints.

What Next

Check for the presence of a New Technology license NTA6. If you do not have this license, contact the Synopsys Technical Support Center or your applications consultant.

PTE-126

(error) %s. Two clocks should be specified as arguments to get_clock_relationship.

Feedback

Description

The command *get_clock_relationship* expects two clocks to be specified as its required arguments. The error will be printed if less or more than two clocks are specified, as well if the same clock is specified twice.

What Next

Specify a list of two clock names or a collection of two clocks as an argument for *get_clock_relationship*.

See Also

- set_clock_groups
- get_clock_relationship

PTE-127

(information) Message '%s' %s limit (%d) exceeded. Remainder will be suppressed.

Description

You receive this message if the total number of warning messages of a particular message id exceeds a default (or user set) limit.

What Next

This is an informational message only. To avoid receiving this message, you can increase the default limit using the variable *sh_message_limit* or the command *set_message_info*.

See Also

- PTE-127

PTE-130

(warning) Invalid sequential case propagation setting on %s '%s'.

Description

You receive this message if a set_case_sequential_propagation failed on the specified cell instance or library cell.

What Next

To avoid receving this message, check if the specified cell instance or library cell is sequential.

Feedback

See Also

- set_case_sequential_propagation
- remove_case_sequential_propagation
- set_case_analysis
- remove_case_analysis
- report_case_analysis
- PTE-130

PTE-131

(warning) Long depth detected during case analysis or logic constant propagation on pin %s, restarting depth to 1.

Description

You received this message because the propagation logic depth limit was exceeded during the propagation of case analysis or logic constants. This is triggered when case or logic constants are propagated through deep combinational paths and/or long sequential chains, if sequential propagation is enabled.

What Next

Check that the case analysis logic constant propagation is intended for long logic depths.

Pins that trigger this message are restarted at depth 1. Therefore, the new depth will be reflected in the case or logic constant propagation logging, if case_analysis_log_file is set.

See Also

- set_case_analysis
- set_case_sequential_propagation
- case_analysis_log_file

PTE-132

(Warning) No exclusivity will be inferred for clock %s at pins %s because the number of cascaded MUXes in the exclusive clock traces has exceeded the limit.

Feedback

Description

The variable *timing_auto_mux_cascaded_mux_limit* set the maximum number of cascaded MUXes to be considered for exclusivity. PrimeTime will not infer exclusivity on the MUXes on a clock trace if the number of visited exclusive MUXes in the clock trace has reached the limit. cell.

PTE-133

(Warning) Source pin '%s' of generated clock '%s' has no path to its master clock.

Description

There is no path from the master clock to the source pin of the generated clock. This may be because there is no physical path, or because the generated clock has been defined using "-combinational" and the generated clock is not in the direct combinational fanout of the master clock. Because no path can be found, the tool will use a propagated source latency of zero from the master clock to the generated clock.

What Next

Check the path from the master clock to the source of the generated clock. To properly calculate the propagated source latency, redefine the generated clock so that its source is in the fanout of its master clock.

PTE-134

(Warning) Complex clock topology encountered while calculating clock pessimism removal. The CRP may be pessimistic.

Description

The source latency network of a generated clock refers to the set of paths between the source pin of its master clock and the source pin of the generated clock. Unless the generated clock has been declared with *-combinational*, these paths might traverse through sequential elements as well as combinational cells.

This warning means the CRP calculation may have encountered a loop that prevented a pessimism to be removed, resulting in potentially pessimistic results. PrimeTime considers paths traversing the entire loop as invalid for determining the generated clock's latency, but this handling might not correspond to your design intent or that the generated clock has not been correctly specified. In rare cases, the latency shown by *report_timing* might not match the latency printed by *report_timing -path_type full_clock_expanded* when this warning occurs.

Feedback

What Next

Use *check_timing -override_defaults generated_clocks -verbose* to see the set of pins forming the loop. It is strongly advised that you alter your clock network specification to eliminate the loop. Perhaps the *-combinational* switch has been omitted in error or the *timing_gclock_source_network_num_master_registers* variable needs to be set. Equally, the clock network topology itself might need to be reconfigured to break the cycle using *set_disable_timing* or *set_clock_sense -stop_propagation* within the generated source network.

See Also

- check_timing
- create_generated_clock
- report_timing
- set_sense
- set_disable_timing
- timing_gclock_source_network_num_master_registers

PTE-135

(Information) The requested clock sense at clock source pin '%s' for clock '%s' will be applied.

Description

The user has specified a 'set_sense' at the given pin. The requested clock sense will be applied to the pin for the source clock.

See Also

- set_sense
- report_sense

PTE-136

(Warning) The clock source pin '%s' of clock '%s' is on the fanout of another source pin '%s' of the same clock.

Feedback

Description

This warning is issued when a clock source pin is reached from another clock source pin of the same clock. Please make sure that the clock source pins of multi-source clocks are not defined in such manner.

Clock latency propagation starts over at the later clock source. It is not propagated through a second source.

If you need sources in the fanout of other sources, it is recommended that you use set_sense -stop_propagation to prevent one clock from reaching another source of the same clock.

See Also

- create_clock
- create_generated_clock

PTE-137

(Information) Invalidating the graph-based refinement analysis.

Description

When *timing_enable_graph_based_refinement* is set to true, graph-based refinement is triggered prior to the first invocation of exhaustive PBA reporting in order to improve the performance of exhaustive PBA. Subsequent to this, when certain changes are made to the design - for instance, changes that invalidate the timing of the design or changes to the variables *timing_refinement_max_slack_threshold* or *timing_refinement_min_slack_threshold*, the refinement is invalidated.

See Also

- timing_enable_graph_based_refinement
- timing_refinement_max_slack_threshold
- timing_refinement_min_slack_threshold

PTE-138

(error) This variable pba_aocvm_only_mode is obsolete and superseded by the pba_derate_only_mode variable.

Description

PrimeTime no longer supports the setting of *pba_aocvm_only_mode* variable and will exit.

Feedback

This variable applies to the path-based analysis performed during the get_timing_paths and report_timing commands when the -pba_mode option is specified. This option controls whether or not regular path-based analysis (path-specific slew propagation) effects are performed during a path-based analysis in addition to advanced OCV path-based analysis.

See the *pba_derate_only_mode* variable for additional information.

What Next

The variable *pba_derate_only_mode* can be used.

PTE-139

(Information) Invalidating %s update.

Description

PrimeTime has the ability to perform a partial or logical update in response to certain attribute queries and arc traversal functions (for example, all_fanin/all_fanout).

When the user makes a change that invalidates the design such as set_case_analysis, create_clock, path exceptions, etc., PrimeTime automatically performs a partial or logical update whenever a new attribute query or arc traversal function is called.

This message is printed after the first command that invalidated the partial and/or logical update state of PrimeTime.

What Next

Using this information the user may be able to make their script more efficient by not interleaving certain query and timing constraint commands.

PTE-140

(error) The list of objects provided in a through_list to the reporting command forms a loop consisting of hierarchical nets and pins.

Description

PrimeTime has detected a loop consisting of hierarchical nets and pins among some of the objects provided in through_lists to one of reporting commands. Hierarchical pins that do not have constraints specified on them are normally not analyzed by PrimeTime graph ordering and automatic loop breaking algorithms. Therefore, such loops may not be automatically broken.

This error message is typically followed up by the list of pins that constitute the detected loop.

Feedback

What Next

The user should review the hierarchical objects passed in through_lists and modify the lists appropriately so as to remove all but one of the pins that constitute the detected loop.

PTE-141

(Warning) Clock '%s' goes through pin '%s' of a correlated exclusive mux, even though it had previously visited another pin of another mux that is correlated to this mux. This error occurs when there are two exclusive muxes connected in series that are correlated (e.g. the select lines are driven from the same net). A clock path can not visit an input of the first mux and then visit the second input of the second mux. As this path is illegal, since the first input of the first mux and the second input of the second mux cannot be active at the same time.

What Next

Make sure the exclusive muxes that are correlated are not connected in series, otherwise, some illegal clock paths might come up.

PTE-142

(Warning) set_clock_uncertainty on pin %s will be ignored because the pin is not in the direct clock network of any clock.

Description

When a pin has uncertainty set with *set_clock_uncertainty*, but the pin is not in the direct clock network of any clock, the uncertainty will not be propagated to any clock pins, and the setting will be ignored by the tool.

What Next

Either remove the setting on the pin, or find out why the pin is not in the direct clock network of a clock.

See Also

- set_clock_uncertainty

PTE-143

(warning) The slew at pin %s is outside the bounds of the lookup table defined at pin %s of the library cell %s. Extrapolation will be applied to compute the frequency and slew lookup table-based max_capacitance. The slew value is %.2f, and the table bounds are %.2f, %.2f.

Feedback

Description

Frequency and slew-indexed lookup tables for max_capacitance are defined on the output or inout pins of a library cell. If the slew at the pin is not within the bounds of the indexing slews specified in the library, extrapolation will be applied.

What Next

Either the library pin should be characterized with enough slew indices to cover the design, or the design should be changed to stay within the library characterization ranges.

PTE-144

(error) TCL variable '%s' is specified with unsupported value (format) '%s'.

Description

This error message occurs when you specified unsupported value for the TCL variable.

What Next

You need to check what is the legal format the TCL variable (upf_name_map/ sdc_name_map) supports.

PTE-145

(error) The application '%s' has '%d' columns while defining name map, '%d' column/ columns is/are specified

Description

This error message occurs when you specified wrong number of columns in define_name_maps for the application.

What Next

You need to check what is the legal columns for the application

---

PTE-146

(error) For the application '%s', the expected column name '%s' is not matching with column name '%s' specified in define_name_map command.

Description

This error message occurs when you specified wrong column in define_name_maps for the application.

Feedback

What Next

You need to check what is the legal columns for the application

---

PTE-147

(error) The class '%s' is not supported in '%s' application

Description

This error message occurs when you specified unsupported class in define_name_maps for the application.

What Next

You need to check what is the supported class for the application

---

PTE-148

(error) Existing entry in the map. None of the entries will be inserted in the map.

Description

This error message occurs when you specified already existing entry in define_name_maps.

What Next

You need to remove existing entry and re-issue the command.

PTE-149

(Information) Filename read from set_app_var %s '%s' overriding verilog pragma.

Description

The file name was read from set_app_var upf_name_map/sdc_name_map based on higher precedence.

What Next

Tcl global variable upf_name_map/sdc_name_map has a higher precedence than upf_name_map/sdc_name_map pragma in Verilog netlist.

PTE-150

(Warning) Duplicate entry in the map. Ignoring ...

Feedback

Description

This error message occurs when the given map has duplicate entries.

What Next

Please verify the correctness of the name map.

PTE-151

(warning) The max_transition limit for pin %s was set with the option -force, so the variable timing_max_transition_limit_from_library_only will be ignored.

Description

With the variable *timing_max_transition_limit_from_library_only* set to *true*, the limit applied should come from the library only. However, setting the limit with *-force* overrides the variable setting.

What Next

Either set the variable *timing_max_transition_limit_from_library_only* to *false*, or remove the limit from the pin with *remove_max_transition*.

See Also

- timing_max_transition_limit_from_library_only
- set_max_transition
- remove_max_transition

PTE-152

(warning) Incompatible variables timing_max_transition_limit_from_library_only and timing_enable_max_slew_precedence are set to true. Only timing_max_transition_limit_from_library_only will be respected.

Description

The effect of setting *timing_max_transition_limit_from_library_only* to *true* is that the limit applied by report_constraint should come from the library only. The effect of setting the variable *timing_enable_max_slew_precedence* variable to true is that the pin- or port-level max_transition value takes precedence over the library-derived max_transition value, which in turn take precedence over design-level max_transition value. The variables are incompatible. Only *timing_max_transition_limit_from_library_only* will be respected.

Feedback

What Next

Set one of the variables to false.

See Also

- timing_max_transition_limit_from_library_only
- timing_enable_max_slew_precedence

PTE-153

(warning) The max_capacitance limit for pin %s was set with the option -force, so the variable timing_max_capacitance_limit_from_library_only will be ignored.

Description

With the variable *timing_max_capacitance_limit_from_library_only* set to *true*, the limit applied should come from the library only. However, setting the limit with *-force* overrides the variable setting.

What Next

Either set the variable *timing_max_capacitance_limit_from_library_only* to *false*, or remove the limit from the pin with *remove_max_capacitance*.

See Also

- timing_max_capacitance_limit_from_library_only
- set_max_capacitance
- remove_max_capacitance

PTE-154

(warning) Incompatible variables timing_max_capacitance_limit_from_library_only and timing_enable_max_cap_precedence are set to true. Only timing_max_capacitance_limit_from_library_only will be respected.

Description

The effect of setting *timing_max_capacitance_limit_from_library_only* to *true* is that the limit applied by report_constraint should come from the library only. The effect of setting the variable *timing_enable_max_cap_precedence* variable to true is that the pin- or port-level max_capacitance value takes precedence over the library-derived max_capacitance value, which in turn take precedence over design-level max_capacitance value. The

Feedback

variables are incompatible. Only *timing_max_capacitance_limit_from_library_only* will be respected.

What Next

Set one of the variables to false.

See Also

- timing_max_capacitance_limit_from_library_only
- timing_enable_max_cap_precedence

PTE-155

(Warning) Maximum number of exclusive traces of clock %s has reached pin %s, some exclusivity points in the fan-in of the pin will be ignored.

Description

This warning message occurs when there is a pin in the clock network for which the maximum number of exclusive traces of a clock is reached. Please note that some exclusive points in the fan-in of the pin will be ignored.

What Next

Please verify that there clock network topology does not have complex re-convergent paths

---

PTE-156

(warning) The max_capacitance limit for pin %s was set with the option -force, so the variable report_use_out_of_table_range will be ignored for this pin.

Description

With the variable *report_use_out_of_table_range* set to *true*, the limit applied should come from the library only. However, setting the limit with *-force* overrides the variable setting.

What Next

Either set the variable *report_use_out_of_table_range* to *false*, or remove the limit from the pin with *remove_max_capacitance*.

Feedback

See Also

- report_use_out_of_table_range
- set_max_capacitance
- remove_max_capacitance

PTE-157

(warning) The max_transition limit for pin %s was set with the option -force, so the variable report_use_out_of_table_range will be ignored for this pin.

Description

With the variable *report_use_out_of_table_range* set to *true*, the limit applied should come from the library only. However, setting the limit with *-force* overrides the variable setting.

What Next

Either set the variable *report_use_out_of_table_range* to *false*, or remove the limit from the pin with *remove_max_transition*.

See Also

- report_use_out_of_table_range
- set_max_transition
- remove_max_transition

PTE-158

(warning) Due to derating, PBA delay value does not bound GBA delay value. Using the GBA delay value at %s.

Description

Some GBA/PBA ounding issues that arise due to derating are avoided by using the GBA value in this report. This can only occur if POCV is enabled.

For instance, on a min path, PBA computed delays usually have larger delay value. In POCV, This can mean having larger mean and a larger sensit. Certain derate settings, such as -pocvm_coefficient_scale_factor, can multiply the sensit sufficiently that the corner value of the PBA delay becomes less than the GBA delay corner. This can cause GBA/PBA bounding problems.

Feedback

When this warning occurs, it does not mean that the computed PBA delay values have a problem, merely that after applying pocvm derates, the PBA values become worse than GBA and are not reasonable.

These issues can be avoided by using smaller pocv derates.

What Next

Reduce pocvm derates

See Also

- set_timing_derate
- reset_timing_derate

PTE-159

(warning) Borrowing between clocks with unrelated periods exists in the design. Clock %s (period %20.20f) is borrowing into clock %s (%20.20f). Paths involving this borrowing may have pessimistic timing analysis, and paths may be shown using impossible clock edges.

Description

This warning is only issued when a hidden tool setting is enabled (may be enabled by TBC).

The tool normally tries to keep track of many transparent latch borrow situations between clocks of different periods. When the analysis is complex, and the hidden setting is enabled, the tool simplifies the analysis by not keeping track of many borrow situations. This can result in pessimistic analysis for paths involved in this borrowing. It can also result in showing timing reports where some clock edges have impossible values (i.e. not multiples of the clock period). When these timing reports are shown, the tool has not kept track of all the borrow situations, but is combining segments together that are impossible. Timing analysis in these situations is safe, but pessimistic.

What Next

Avoid borrowing between clocks of unrelated periods. If clocks have unrelated periods, but need to communicate, consider using set_max_delay to specify a single relation between the clocks. If the clocks do not need to communicate, consider specifying asynchronous or exclusive clock groups between the clocks.

See Also

- set_max_delay
- set_clock_groups

Feedback

PTE-160

(warning) Borrowing between clocks with unrelated periods exists in the design. Clock %s (period %20.20f) is borrowing into clock %s (%20.20f). Excessive runtime can result from tracing these paths.

Description

The tool tries to keep track of many transparent latch borrow situations between clocks of different periods. When the analysis is complex, runtime and memory required by the analysis can be degraded.

What Next

Avoid borrowing between clocks of unrelated periods. If clocks have unrelated periods, but need to communicate, consider using set_max_delay to specify a single relation between the clocks. If the clocks do not need to communicate, consider specifying asynchronous or exclusive clock groups between the clocks.

See Also

- set_max_delay
- set_clock_groups

PTE-161

(Information) Lower bound frequency is taken for pin %s from max_cap_table since the frequency is not specified.

Description

The frequency is not specified for the said pin in the max cap table. Hency lower bound frequecy from max cap table is taken for this pin.

What Next

Please specify the frequecy in the max cap table for the said pin.

PTE-162

(Warning) External delay specified on pin '%s' is not recognized. The timing path remains broken.

Description

This message is issued when there is no clock reaching the reference pin of the external delay. Please note that the timing path is broken due to this external delay.

Feedback

What Next

Please fix/remove the external delays specified on the pin.

PTE-163

(information) Master clock '%s' and its generated clock(s) '%s' are defined on the same source pin/port '%s'.

Description

You receive this message because you have defined multiple clocks on the same source pin.

What Next

Exercise care to make sure that all clocks that were defined on a single source pin are correctly defined.

PTE-164

(information) Retain value is larger than delay for the arc %s->%s:\n\t%s

Description

The retain value should be less than the corresponding delay value so that they can be considered for hold violations. Otherwise the retain values might be considered for setup violation.

See Also

- check_timing

PTE-166

(Warning) Non-unate clock paths of clock '%s' has reached pin '%s', some exclusivity points in the fan-in of the pin will be ignored.

Description

This warning message occurs when there is a pin in the clock network to which non-unate clock paths reach. Please note that some exclusive points in the fan-in of the pin will be ignored.

What Next

Please verify that there clock network topology does not have non-unate path traces

Feedback

PTE-167

(warning) Conflicted scenario logic driving pin %s, setting resolved logic value %s for scenario %s.

Description

You receive this message because, during the propagation of scenario case analysis or logic constants, update_timing detects two conflicting logic values propagated to a pin. The conflicting settings affect the same scenario

For example, if two strong drivers drive a net with one carrying case analysis *0* and the other carrying case analysis *1*, then a logic conflict would arise.

In these situations, *update_timing* resolves the logic conflict to *0* and continues propagating this forward in the design. The message warns you that a logic conflict has occurred at the specified pin and that it has been resolved to the specified logic value.

What Next

Correct the problem by changing set_scenario_case_analysis and reexecute *update_timing*.

See Also

- set_scenario_case_analysis
- remove_scenario_case_analysis
- report_timing
- update_timing

PTE-168

(warning) Scenario case analysis settings conflict with regular case analysis at pin %s, setting resolved logic value %s (instead of scenario value of %s) for scenario %s.

Description

You receive this message because, during the propagation of scenario case analysis or logic constants, update_timing detects a conflict between the settings for the scenario, and the settings from regular case analysis or logical constants.

In these situations, *update_timing* resolves the logic conflict by keeping the value from regular case analysis or logical constants. The scenario case analysis propagation is ignored starting at the specified pin.

Feedback

What Next

Correct the problem by changing set_scenario_case_analysis to avoid conflicts with regular case analysis.

See Also

- set_scenario_case_analysis
- remove_scenario_case_analysis
- set_case_analysis
- remove_case_analysis
- report_timing
- update_timing

PTE-169

(Warning) source latency time on pin %s inside a clock network loop failed to converge. old value: %.6e, new value: %.6e, from clock: %s, source latency for: %s.

Description

The source latency network of a generated clock refers to the set of paths between the source pin of its master clock and the source pin of the generated clock. Unless the generated clock has been declared with *-combinational*, these paths might traverse through sequential elements as well as combinational cells.

When loop is found in the source latency network, PrimeTime considers paths traversing the entire loop as invalid for determining the generated clock's latency, and thus expects all possible latency times inside a loop to converge. This warning indicates that the latency time has not converged after reaching maximum loop iteration.

What Next

Use *check_timing -override_defaults generated_clocks -verbose* to see the set of pins forming the loop. It is strongly advised that you alter your clock network specification to eliminate the loop. Perhaps the *-combinational* switch has been omitted in error or the *timing_gclock_source_network_num_master_registers* variable needs to be set. Equally, the clock network topology itself might need to be reconfigured to break the cycle using *set_disable_timing* or *set_clock_sense -stop_propagation* within the generated source network.

Feedback

See Also

- check_timing
- create_generated_clock
- report_timing
- set_clock_sense
- set_disable_timing
- timing_gclock_source_network_num_master_registers

PTE-170

(warning) Variable pba_exhaustive_any_slack_lesser_than must take either a float value, the string "disabled" or the string "slack_lesser_than"

Description

The PrimeTime variable pba_exhaustive_any_slack_lesser_than must take either a float value, the string "disabled" or the string "slack_lesser_than"

What Next

Set the variable to either a float value, the string "disabled" or the string "slack_lesser_than".

PTE-171

(Warning) A mux instance has clock signal propagated to both its input pin '%s' and select pin '%s'.

Description

Clock signal is propagated to the select pin and at least one input pin of a mux instance. It is unlikely that the clock signal is intended to propagate through both the input AND select pins of the same mux instance.

What Next

It is possible to stop clock signals from propagating through the mux select pin by using the following command:

set_sense -stop_propagation [get_pin $select_pin]

Feedback

PTECO

PTECO-001

(error) Cannot change the state of ECO mode because %s.

Description

This error message is issued when the attemp to change the state of ECO mode fails due to the reason indicated. Most often, it happens when you are trying to either enable or disable ECO mode after designs and/or libraries have already been loaded into PrimeTime.

What Next

Please verify the reason indicated by the error message, make sure you issue the command 'set_program_options' earlier, e.g. before any library/design is loaded.

PTECO-002

(information) ECO mode is %s, and the behaviors of the following ECO commands are changed: "read_parasitics -eco".

Description

This information message is issued when the state of ECO mode is changed.

What Next

Please verify if the commands listed in the message are really needed or not needed in the script.

PTECO-003

(error) %s.

Description

This is a generic error message.

What Next

Please note and confirm the specific reason indicated by the error message, modify your setting(s) accordingly, re-issue the command(s).

Feedback

PTECO-004

(error) Only one object is allowed for estimate_eco.

Description

Multiple objects are not allowed for *estimate_eco*.

What Next

Please specifiy only one object.

PTECO-005

(error) No library cell exists.

Description

No library cell exists for the specified library cell names.

What Next

Please check whether the speicified library cell name is correct or not.

PTECO-006

(error) ECO type size_cell requires a cell object.

Description

Only a cell object is allowed for ECO type size_cell.

What Next

Please specify a cell object for size_cell ECO type.

PTECO-007

(error) ECO type insert_buffers requires a pin object.

Description

Only a pin object is allowed for ECO type insert_buffer.

What Next

Please specify a pin object for insert_buffer ECO type.

Feedback

PTECO-008

(error) Options -libraries and -current_library cannot be specified together.

Description

Options -libraries and -current_library are mutually exculsive.

What Next

Please specify only one of the two options.

PTECO-009

(error) ECO type buffer_insertion requires -lib_cells option specified.

Description

For buffer insertion, it is required to specify new buffer library cells.

What Next

Please specify one or more than one buffer librarys.

PTECO-011

(error) No net exists for the current stage, and there are pins floating without any connection.

Description

The command requires that the current stage should have a net to estimate cell and net delays.

What Next

Please check whether the netlist is correct.

PTECO-012

(error) Cannot estimate buffer insertion at a hierarchical pin.

Description

The command requires that the specified pin object must not be a hiearchical pin.

What Next

Please check whether the pin is hierarchical or not.

Feedback

PTECO-013

(error) By default, option -methods includes insert_buffer, but no library cell is specified for option -buffer_list.

Description

The command requires that buffer library cells should be specified if the -methods option includes insert_buffer.

What Next

Please add buffer library cells or remove insert_buffer from the -methods option.

PTECO-014

(Error) '%s' is not a valid method.

Description

To fix hold timing and design rule checking (DRC) violations, use the *-method* option with the *size_cell* and/or *insert_buffer* method. You cannot use the method *size_cell_side_load*.

To fix setup timing violations, use the *-method* option with either the *size_cell*, *size_cell_side_load* or *insert_buffer* method; you cannot use all of them together in the same command.

To perform area/power recovery, use the *-method* option with either the *size_cell* or *remove_buffer* method; you cannot use both methods in the same command.

What Next

Verify that you used the *-method* option correctly for the ECO command.

See Also

- fix_eco_drc
- fix_eco_timing
- fix_eco_power

PTECO-015

(error) The number of hosts is different from the number of scenarios

Feedback

Description

The number of hosts should match the number of scenarios. Alternatively, set *eco_enable_more_scenarios_than_hosts* to true, if more scenarios than hosts should be allowed.

What Next

Please verify the number of hosts, and make sure that it is as same as the number of scenarios.

PTECO-016

(error) %s is not a valid type

Description

Valid types are setup and hold.

What Next

Please verify the type option specified, and make sure that only valid type is specified.

PTECO-017

(error) The buffer list specified by -buffer_list is empty or doesn't have any valid buffer.

Description

You have specified invalid buffer names, or the buffer list does not contain any valid buffer name.

What Next

Please verify the buffer names in the buffer list. They should be library cell base names.

PTECO-018

(information) Resource-limited fixing is enabled as there are %d scenarios, but only %d hosts are available.

Description

The number of available hosts is less than the number of scenarios. PrimeTime SI enables resource-limited fixing to fix violations with fewer hosts. The quality of results (QoR), such as fixing rate, buffer count, and the number of changes, might be different when compared to the results produced with the same number of hosts as the scenarios.

Feedback

What Next

Check the quality of results. If they are degraded, you may consider to increase the number of available hosts.

PTECO-019

(warning) The number of hosts is less than the recommended minimum host %d.

Description

The number of available hosts is less than the recommended minimum. PrimeTime SI recommends the mininum number of hosts should be at least 8 and one fourth of the number of scenarios, whichever is larger. If there are fewer available hosts than the minimum recommendation, quality of results (QoR), such as fixing rate, buffer count, and the number of changes, might be impacted.

What Next

Check the quality of results. If they have degraded, you might consider increasing the number of available hosts.

PTECO-020

(warning) Quality of results (QoR) might be impacted.

Description

PrimeTime SI has detected cases that might impact the quality of results. These situations include fixing rate, buffer count, area increase, and the number of changes. It is possible that QoR might degrade when it is compared to the run with the same number of scenarios and hosts.

The previous warning message shows what caused this warning message. For example, the previous warning message might have stated that the number of available hosts does not meet the minimum host recommendation.

What Next

Check the previous warning message, and resolve the issue if possible.

PTECO-021

(information) Enabling timing fixing with path-based analysis in the %s mode.

Feedback

Description

The *fix_eco_timing* command fixes the violations that are detected during path-based analysis. The path-based analysis shows less violations than the graph-based analsyis, thus it is expected to create a smaller number of ECO changes.

The *fix_eco_timing* command runs the path-based analysis internally to detect violations, thus runtime might take longer with this option.

What Next

After fixing violations, run the path-based analsyis again to report the final remaining violations.

PTECO-022

(information) %d violating endpoints located...

Description

This information message shows how many violating endpoints have been detected in each iteration. One violating endpoint can have more than one violation such as max_rise and max_fall violations that occur at the same time.

What Next

Check that the number of violations decreases in the next iterations.

PTECO-023

(information) %d %s located in the %s scenario...

Description

This information message shows the scenario with the largest number of violations in the given fixing type. With the *fix_eco_timing* command, this message shows the number of violating endpoints. With the *fix_eco_drc* command, it shows the number of specific type of timing design rule checking (DRC) violations such as maximum transition, maximum capacitance or maximum fanout violations.

What Next

Check that the number of violations decreases in the next iterations.

PTECO-024

(information) %d %s located in all scenarios...

Feedback

Description

This information message shows the total number of violations in all scenarios. With the *fix_eco_timing* command, this message shows the number of violating endpoints. With the *fix_eco_drc* command, this message shows the number of specific type of timing design rule checking (DRC) violations such as maximum transition, maximum capacitance or maximum fanout violations.

What Next

Check that the number of violations decreases in the next iterations.

PTECO-025

(information) %d %s estimated in all scenarios...

Description

This information message appears when resource-limited fixing is activated in which the number of available hosts is less than the number of scenarios. In this mode, the *fix_eco_timing* command does not show the exact number of violations. Instead, it estimates the total number of violations in all scenarios due to the lack of available hosts.

What Next

Check the number of availale hosts. If there are too few hosts available, use the *set_host_options* command to specify the host options.

PTECO-026

(warning) One or more than one worker failed, and only limited information is shown.

Description

Because one or more than one worker failed, some of information cannot be shown.

What Next

Find what caused the failure and fix it if possible. Also make sure that final results are fine.

PTECO-027

(information) %d endpoints are being considered for fixing...

Description

This information message shows how many endpoints will be considered for fixing. The number can be smaller than the number of located violating endpoints because PrimeTime

SI does not fix some specific violations. For example, a timing violation in clock networks is not fixed because changing clock network might cause wide impact on overall design timing statistics.

What Next

If this information message shows the number that is less than the number of violating endpoints, you minght want to use timing reports to find the cause.

PTECO-028

(error) The number of hosts is less than the minimum host requirement.

Description

The number of available hosts is less than the minimum requirement. PrimeTime SI requires the mininum number of hosts should be at least 4 if the number of scenarios and the number of hosts are not equal.

What Next

Increase the number of available hosts.

PTECO-029

(error) A PrimeTime SI license is required to run %s.

Description

A PrimeTime SI license is required for this technology, but the command failed to acquire it.

What Next

Check the availability of a PrimeTime SI license.

PTECO-030

(error) %s is not a valid cell_type.

Description

combinational and *sequential* are valid for option -cell_type to fix_eco_timing command.

What Next

Please verify the cell_type option specified, and make sure that only valid option is specified.

Feedback

PTECO-031

(information) The library cell '%s' in the buffer list has '%s' attribute set to true.

Description

This information message shows that a library cell specified for *-buffer_list* option to *fix_eco_timing* or *fix_eco_drc* command has specified attribute set to true. Note that PrimeTime uses all the specified library cells in the buffer list for fixing regardless of their *dont_use*, *dont_touch* or *pt_dont_use* attribute.

What Next

Check if the library cell should be avoided, in which case, provide a different usable library cell in the buffer list.

PTECO-032

(information) Writing intermediate change file to %s.

Description

This information message shows that a intermediate change list file for *fix_eco_timing* or *fix_eco_drc* command is generated. Note that the intemediate change list is not final, and using the intermediate change list may not result in a converged solution.

What Next

Check if the QoR of intermediate change list is acceptable. If not, use the final change list.

PTECO-033

(error) Physical database is invalid.

Description

This error message occurs when the ECO configuration is incorrect, or the LEF/DEF file is invalid.

What Next

Please verify that ECO configuration in the *set_eco_options* command is correct. Also ensure that the given LEF/DEF file is valid by examining the log file specified by the *set_eco_options* command.

PTECO-034

(warning) Port/pin %s does not exist.

Feedback

Description

The port/pin specified cannot be found in the design.

What Next

Check the port/pin name specified in the command.

PTECO-035

(error) Same attribute value is set on different library cells.

Description

This error message occurs when you set the same user-defined attribute value on different library cells for leakage fixing.

What Next

Ensure that each library cell has a unique user-defined attribute setting. To report library cells with duplicate attribute settings, use the *report_cell_usage* command.

In the following example, there are six library cells: BUF_A, B_BUF, BF1X, BUF2X_A, B_BUF2X, BF2X. The following user-defined attribute settings are incorrect:

```
# Incorrect settings for eco_pattern attribute
#
define_user_attribute eco_pattern -type string -class lib_cell
set_user_attribute -class lib_cell [get_lib_cell BUF_A] eco_pattern
 "buf_good"
set_user_attribute -class lib_cell [get_lib_cell B_BUF] eco_pattern
 "buf_ok"
set_user_attribute -class lib_cell [get_lib_cell BF1X ] eco_pattern
 "buf_bad"
set_user_attribute -class lib_cell [get_lib_cell BUF2X_A] eco_pattern
 "buf_good"
set_user_attribute -class lib_cell [get_lib_cell B_BUF2X] eco_pattern
 "buf_ok"
set_user_attribute -class lib_cell [get_lib_cell BF2X ] eco_pattern
 "buf_bad"
```

In the preceding example, buf_good is set on the BUF_A and BUF2X_A library cells. buf_ok is set on the B_BUF and B_BUF2X library cells. buf_bad is set on the BF1X and BF2X library cells. These attribute settings are incorrect because different library cells need different attribute values for leakage fixing. To see a table of all library cells with duplicate attribute settings, use the following command:

```
pt_shell> report_cell_usage -p {good ok bad} -pattern eco_pattern

 ...
```

```
Attr value     Lib cells
------------------------
buf_good       BUF_A BUF2X_A
buf_ok         B_BUF B_BUF2X
buf_bad        BF1X  BF2X
```

The following example shows correct attribute settings, with a unique value for each library cell:

```
# Correct settings for eco_pattern attribute
# Assign different value to each library cell with "good ok bad"
#
define_user_attribute eco_pattern -type string -class lib_cell
set_user_attribute -class lib_cell [get_lib_cell BUF_A] eco_pattern
 "buf_good"
set_user_attribute -class lib_cell [get_lib_cell B_BUF] eco_pattern
 "buf_ok"
set_user_attribute -class lib_cell [get_lib_cell BF1X ] eco_pattern
 "buf_bad"
set_user_attribute -class lib_cell [get_lib_cell BUF2X_A] eco_pattern
 "buf2x_good"
set_user_attribute -class lib_cell [get_lib_cell B_BUF2X] eco_pattern
 "buf2x_ok"
set_user_attribute -class lib_cell [get_lib_cell BUF2X ] eco_pattern
 "buf2x_bad"
```

See Also

- fix_eco_leakage
- report_cell_usage
- set_user_attribute

PTECO-036

(error) %s is not a valid physical mode.

Description

none,*open_site* and *occupied_site* are valid for option -physical_mode.

What Next

Please verify the -physical_mode option specified, and make sure that only valid option is specified.

PTECO-037

(error) Cannot change the ECO configuration after loading a valid physical database.

Feedback

Description

This error occurs when you try to change the ECO configuration after loading a valid physical database.

What Next

Use the previously specified ECO configuration.

PTECO-038

(error) Atleast one Design Exchange Format (DEF) file must be provided to the -physical_design_path option of the set_eco_options command for physically aware ECO commands to proceed.

Description

This error message occurs when no Design Exchange Format (DEF) file is provided to set_eco_options. Physically aware ECO commands cannot proceed without DEF files.

What Next

Check the -physical_design_path option to *set_eco_options* for correctness.

PTECO-039

(information) Starting to load physical information at [%s]...

Description

This information message shows the starting point of loading physical database.

What Next

Check the timestamps.

PTECO-040

(information) Loading physical data and creating output log in %s...

Description

This message shows that the log of reading physical data is redirected to the specified file.

What Next

Check the log file for any error or warning messages.

Feedback

PTECO-041

(error) Cannot open the log file: %s.

Description

This error occurs when the log file cannot be opened to write.

What Next

Verify that the path and access permission to the specified log file are correct.

PTECO-042

(warning) The %s is deprecated and will be obsolete in a future release. This feature is superseded by the %s.

Description

This is a warning message indicating the specified command, option or variable is in the process of being obsoleted and will not be supported in future releases of PrimeTime.

What Next

Please use the suggested replacement for this feature being obsoleted.

PTECO-043

(information) %d paths located...

Description

This information message shows the number of paths detected in each iteration. The paths are the timing paths that satisfy the criteria specified by the *-path_selection_options* option.

What Next

Check that the number of paths decreases in the next iterations.

PTECO-045

(information) Identifying MIM...

Feedback

Description

This information message shows PrimeTime will identify Multiply Instantiated Modules (MIM) for fixing if they are present in the design. This message also indicates the *eco_enable_mim* variable is set to true.

What Next

Check if identified MIM blocks are consistent with your design.

PTECO-046

(information) Reconfiguring MIM with user specification...

Description

This information message shows that user specified MIM is being applied to the design.

What Next

Check if new MIM blocks are consistent with your specification.

PTECO-047

(information) Reconfiguring MIM with physical data...

Description

This information message shows the MIM relation derived from parasitic files is different from physical data, and the MIM relation defined by Design Exchange Format (DEF) files is being applied to the design.

What Next

Check if MIM relation between parasitics files and DEF files are consistent.

PTECO-048

(information) Physical data and parasitics have the same MIM configurations.

Description

This information message shows the MIM relation derived from parasitic files matches the MIM relation defined by Design Exchange Format (DEF) files.

What Next

Check if MIM relation between parasitics files and DEF files are consistent.

Feedback

PTECO-049

(error) MIM configuration is fixed and cannot be changed.

Description

This error message indicates current MIM configuration cannot be changed by users. One possible reason would be one of *fix_eco_timing, fix_eco_drc* or *fix_eco_power* has already run and the user specification has been applied. Once the user specification is applied, MIM configuration cannot be changed.

What Next

Check if the user specification is applied before the first fixing command.

PTECO-050

(error) You cannot use the -path_selection_options option with other path search options.

Description

You cannot use the *-path_selection_options* option with the following path search options: *-from*, *-to*, *-group*, *-pba_mode*, *-slack_lesser_than*, and *-slack_greater_than*.

What Next

Use either the *-path_selection_options* option or the other path search options.

See Also

- fix_eco_timing

PTECO-051

(error) You cannot use the -path_selection_options and -delay_type %s options together with the -type %s option.

Description

This error message occurs when you specify an invalid value for the *-delay_type* option of the *-path_selection_options* option. When you use the *-type hold* option, you can specify the following values for the *-delay_type* option: *min*, *min_rise*, or *min_fall*. When you use the *-type setup* option, you can specify the following values for the *-delay_type* option: *max*, *max_rise*, or *max_fall*.

What Next

Use the valid values for the *-delay_type* option of the *-path_selection_options* option.

Feedback

See Also

- fix_eco_timing

PTECO-052

(error) The -path_selection_options option does not support the %s option.

Description

This error message occurs when the value in the *-path_selection_options* option specifies any of the following unsupported options: *-path_type*, *-ignore_register_feedback*, *-include_hierarchical_pins*, *-trace_latch_borrow*, *-trace_latch_forward*, *-normalized_slack*, *-dont_merge_duplicates*, *-pre_commands*, *-post_commands*, *-attributes*, and path collection options.

What Next

Remove unsupported options from the *-path_selection_options* option.

See Also

- fix_eco_timing

PTECO-053

(information) %d paths located in the %s scenario...

Description

This information message shows the scenario with the largest number of paths in each iteration. The paths are the timing paths that satisfy the criteria specified by the *-path_selection_options* option in the specified scenario.

What Next

Check that the number of paths decreases in the next iteration.

See Also

- fix_eco_timing

PTECO-054

(information) %d paths located in all scenarios...

Feedback

Description

This information message shows the total number of paths detected in all scenarios. The paths are the timing paths that satisfy the criteria specified by the *-path_selection_options* option.

What Next

Check that the number of paths decreases in the next iteration.

See Also

- fix_eco_timing

PTECO-055

(error) You must specify -max_paths and -nworst options in the -path_selection_options option.

Description

When you use the *-path_selection_options* option, you need to explicitly specify the *-max_paths* and *-nworst* options with values that are suitable for ECO, unless you specify the *-start_end_pair* or *-cover_design* option.

For the *-max_paths* and *-nworst* options, specify values that are large enough to cover all violating paths that you want to fix, which should be at least larger than the number of violations in a design. If the values are too small, each ECO fixing iteration targets to fix only a subset of violating paths; this can increase runtime by increasing the number of ECO fixing iterations and can result in less efficient fixing by not considering other paths that have a common path segment. If the values are too large, the runtime of the *get_timing_paths* command invoked internally might increase.

What Next

Specify the *-max_paths* and *-nworst* options in the *-path_selection_options* option.

See Also

- fix_eco_timing
- get_timing_paths

PTECO-056

(error) You must use curly braces to enclose the value of -path_selection_options option.

Feedback

Description

Use curly braces { } to enclose the value of *-path_selection_options* option when it contains any collection. If you use double quotation marks (" ") to enclose the value of *-path_selection_options* option, any specified collection (such as [get_cells u*]) is substituted to a pointer to the collection before it gets processed by the *fix_eco_timing* command. This is not safe when the lifetime of the collection can be shorter than the *fix_eco_timing* command invoked.

What Next

Enclose the value of the *-path_selection_options* option with curly braces.

See Also

- fix_eco_timing

PTECO-057

(error) Cannot find a scenario with valid setup timing constraints.

Description

This error message shows that the tool failed to find any scenario with valid setup timing constraints.

What Next

Verify that you have at least one scenario with valid setup timing constraints.

See Also

- fix_eco_power

PTECO-058

(error) Instance %s (%s) and %s (%s) have different references and cannot be in the same MIM group.

Description

This error occurs when the specified instances do not share the same reference. The instances in the same MIM group must have the same reference.

What Next

Verify that the instance names have the same reference or not.

Feedback

PTECO-059

(error) Atleast one Library Exchange Format (LEF) file must be provided to the set_eco_options command for physically aware ECO to proceed. The Technology LEF file must be provided to the -tech_lef_file option. The Physical Cell LEF files must be provided to the -physical_lib_path option.

Description

This error message occurs when no Library Exchange Format (LEF) file is provided to set_eco_options commands. Physically aware ECO commands cannot proceed without LEF files.

What Next

Check the -tech_lef_file and the -physical_lib_path options to *set_eco_options* for correctness.

PTECO-060

(error) Scenarios have different multiply instantiated modules.

Description

This error message indicates at least one scenario has different MIM configuration than the rest of the scenarios. When scenarios have different MIM configurations, timing or DRC fixing cannot be performed.

What Next

Check if MIM configuration is same across all scenarios.

PTECO-061

(Error) There is no %s library cell with power attribute '%s'.

Description

This error message occurs if none of combinational and/or sequential library cells have a valid power attribute when the user used the *-power_attribute* option of *fix_eco_power* or *fix_eco_timing* command. A valid power attribute value is a positive floating point number.

What Next

Ensure that each library cell has a valid power attribute. To report power attribute values set on library cells, use the *report_eco_library_cells* command with the *-power_attribute* option.

Feedback

See Also

- fix_eco_power
- fix_eco_timing
- report_eco_library_cells

PTECO-062

(error) Invalid spacing rules have been provided to the -physical_lib_constraint_file option of set_eco_options.

Description

This error message occurs when there are invalid spacing rules provided. Inspect the manpages of set_lib_cell_spacing_label and set_spacing_label_rule for syntax and guidelines to provide spacing rules.

What Next

Check the spacing rules file provided to the -physical_lib_constraint_file for correctness.

PTECO-063

(information) Enabling cell %s with path-based analysis in the %s mode.

Description

The *fix_eco_power* command downsizes or swaps cells with positive setup slack based on path-based analysis (PBA). The PBA setup slack is greater than or equal to the graph-based analsyis (GBA) slack, thus it is expected to perform more aggressive optimization.

The *fix_eco_power* command runs the PBA internally multiple times to maintain the PBA timing, thus runtime might take longer with this option.

What Next

After cell downsizing or swapping, run the PBA again to check that the worst PBA slack at each endpoint is maintained. Note that the GBA timing might not be maintained, and GBA violations can increase significantly when there is a large gap between GBA and PBA slack.

See Also

- fix_eco_power

Feedback

PTECO-064

(error) Path-based analysis failed.

Description

Path-based analysis (PBA) failed while performing the *fix_eco_power* command based on PBA slack.

In the distributed multi-scenario analysis (DMSA), this message is printed if PBA failed in one or more DMSA workers.

What Next

Find what caused the PBA failure and fix it.

PTECO-065

(error) You must use -pba_path_selection_options option together with the -pba_mode path option.

Description

You cannot use the *-pba_path_selection_options* option if either graph-based or exhaustive path-based analysis is used for the *fix_eco_power* command.

What Next

Specify the *-pba_mode path* option when using the *-pba_path_selection_options* option.

See Also

- fix_eco_power

PTECO-066

(error) The -pba_path_selection_options option does not support the '%s' option.

Description

This error message occurs when the value in the *-pba_path_selection_options* option does not match any of the following supported options: *-nworst*, *-max_paths*, and *-cover_design* options.

What Next

Remove unsupported options from the *-pba_path_selection_options* option.

Feedback

See Also

- fix_eco_power

PTECO-067

(warning) Cell %s with exhaustive path-based analysis can cause a long runtime. Consider using derate-only mode or the -pba_mode path to reduce the runtime.

Description

This message is issued when you run the *fix_eco_power* command with the *-pba_mode exhaustive* option. The *fix_eco_power* command runs the path-based analysis internally multiple times; therefore, this option might cause longer runtimes.

What Next

To avoid long runtimes, consider running the *fix_eco_power* command with the *-pba_mode path* option, which gives the best power savings with the fastest path-based analysis runtime without creating new violations detected by path-based analysis. If exhaustive path-based analysis detects any new violations after running the *fix_eco_power* command with the *-pba_mode path* option, fix the violations by using the *fix_eco_timing* command with the *-pba_mode exhaustive* option.

If you want to use the *-pba_mode exhaustive* option, consider setting the *pba_derate_only_mode* variable to *true*. This improves the runtime of exhaustive path-based analysis by only adjusting the derating according to the path-based conditions.

To further improve the runtime of exhaustive path-based analysis, please revisit following variables.

- **pba_exhaustive_endpoint_path_limit**
- **pba_recalculate_full_path**
- **timing_report_use_worst_parallel_cell_arc**

See Also

- fix_eco_power
- get_timing_paths
- pba_derate_only_mode
- pba_exhaustive_endpoint_path_limit
- pba_recalculate_full_path
- timing_report_use_worst_parallel_cell_arc

Feedback

PTECO-068

(error) Invalid viloation type '%s'.

Description

This error message shows that the specified violation type is invalid. It can be a typo or unsupported violation type.

What Next

Check if you have specified correct violation type.

PTECO-069

(information) ECO information not found in saved sessions. Analyzing violations...

Description

This information message shows that PrimeTime was not able to find ECO information from saved sessions. Instead, PrimeTime analyzes violation endpoints to create an ECO design.

What Next

Check if the *eco_save_session_data_type* was set before saving sessions.

PTECO-070

(error) Cannot find ECO information in the saved sessions. Use '%s' option to continue.

Description

This error message shows that ECO information to write an ECO design has not been found in saved sessions. Use the specified option to continue and create an ECO design.

What Next

Rerun the *write_eco_design* command with the specified option.

PTECO-071

(warning) No ECO design has been written.

Description

This error message shows that PrimeTime was not able to write an ECO design due to one or more than one errors or warnings.

Feedback

What Next

Check the warning or error messages generated by the *write_eco_design* command to identify issues.

PTECO-072

(error) No ECO design found in '%s'.

Description

This error message shows that PrimeTime is not able to find any ECO design in the specified directory.

What Next

Check if prior *write_eco_design* command was successful and an ECO design has been created.

PTECO-073

(error) Cannot write a new ECO design after reading an ECO design.

Description

This error message shows that you have attempted to run the *write_eco_design* command after reading an ECO design. Once an ECO design is read using the *read_eco_design* command, it is not allowed to write a new ECO design.

What Next

If your intention is to reduce the design further, it would be better to do so with the first *write_eco_design* command with reduced number of violations or endpoints.

PTECO-074

(error) %s is not a valid method for fix_eco_timing -physical_mode freeze_silicon.

Description

When fix_eco_timing is invoked with the -physical_mode freeze_silicon option, *insert_buffer* is the only valid method that can be provided to option -methods.

In the freeze_silicon physical ECO mode, by default, option -methods includes insert_buffer. A list of library cells must be specified to the -buffer_list option.

Feedback

What Next

Please verify the method option specified, and make sure that only valid options are specified.

PTECO-075

(error) %s is not a valid method for fix_eco_drc -physical_mode freeze_silicon.

Description

When fix_eco_drc is invoked with the -physical_mode freeze_silicon option, *insert_buffer* is the only valid method that can be provided to option -methods.

In the freeze_silicon physical ECO mode, by default, option -methods includes insert_buffer. A list of library cells must be specified to the -buffer_list option.

What Next

Please verify the method option specified, and make sure that only valid options are specified.

PTECO-076

(error) set_eco_options must specify a list of programmable spare cells to invoke fix_eco_drc with -physical_mode freeze_silicon option.

Description

To invoke fix_eco_drc with -physical_mode freeze_silicon option, the user must provide a list of programmable spare cells names to the -programmable_spare_cells option of the set_eco_options command. These programmable spare cells must be defined in the PrimeTime .libs, as LEF macros in the LEF files provided to the set_eco_options and instantiated in the DEF files provided to the set_eco_options command.

What Next

Please verify the options specified to the set_eco_options command.

PTECO-077

(error) set_eco_options cannot specify a list of programmable spare cells to invoke fix_eco_timing with -physical_mode open_site or occupied_site option.

Description

To invoke fix_eco_timing with -physical_mode open_site or occupied_site option, the user cannot provide a list of programmable spare cells names to

Feedback

the -programmable_spare_cells option of the set_eco_options command. The -programmable_spare_cells option is meant exclusively for use with -physical_mode freeze_silicon.

What Next

Please verify the options specified to the set_eco_options command.

PTECO-078

(error) set_eco_options cannot specify a list of programmable spare cells to invoke fix_eco_drc with -physical_mode open_site or occupied_site option.

Description

To invoke fix_eco_drc with -physical_mode open_site or occupied_site option, the user cannot provide a list of programmable spare cells names to the -programmable_spare_cells option of the set_eco_options command. The -programmable_spare_cells option is meant exclusively for use with -physical_mode freeze_silicon.

What Next

Please verify the options specified to the set_eco_options command.

PTECO-079

(error) set_eco_options cannot specify a list of programmable spare cells to invoke the fix_eco_power or fix_eco_leakage commands.

Description

To invoke fix_eco_power or fix_eco_leakage the user cannot provide a list of programmable spare cells names to the -programmable_spare_cells option of the set_eco_options command.

The -programmable_spare_cells option is meant exclusively for fix_eco_timing and fix_eco_drc for use with -physical_mode freeze_silicon.

What Next

Please verify the options specified to the set_eco_options command.

PTECO-080

(error) set_eco_options cannot specify a list of programmable spare cells to invoke the fix_eco_leakage command.

Feedback

Description

To invoke fix_eco_leakge the user cannot provide a list of programmable spare cells names to the -programmable_spare_cells option of the set_eco_options command.

The -programmable_spare_cells option is meant exclusively for fix_eco_timing and fix_eco_drc for use with -physical_mode freeze_silicon.

What Next

Please verify the options specified to the set_eco_options command.

PTECO-081

(error) set_eco_options must specify a list of programmable spare cells to invoke fix_eco_timing with -physical_mode freeze_silicon option.

Description

To invoke fix_eco_timing with -physical_mode freeze_silicon option, the user must provide a list of programmable spare cells names to the -programmable_spare_cells option of the set_eco_options command. These programmable spare cells must be defined in the PrimeTime .libs, as LEF macros in the LEF files provided to the set_eco_options and instantiated in the DEF files provided to the set_eco_options.

What Next

Please verify the options specified to the set_eco_options command.

PTECO-082

(information) Using the %s margin of %s...

Description

This information message shows the value of setup or hold margin used by *fix_eco_timing*, *fix_eco_drc*, or *fix_eco_power* command. The value of setup (or hold) margin can be set by either the *set_eco_options* command or the *-setup_margin* (or *-hold_margin*) option of *fix_eco_timing*, *fix_eco_drc*, or *fix_eco_power* command. The latter has higher precedence than the former.

What Next

Check the value is correct.

Feedback

See Also

- fix_eco_drc
- fix_eco_timing
- fix_eco_power
- set_eco_options

PTECO-083

(information) Using the %s margin of %s in all scenarios...

Description

This information message shows the value of setup or hold margin used by *fix_eco_timing*, *fix_eco_drc*, or *fix_eco_power* command in all scenarios. This message is printed only when the value of setup (or hold) margin is specified for the *-setup_margin* (or *-hold_margin*) option of *fix_eco_timing*, *fix_eco_drc*, or *fix_eco_power* command.

What Next

Check the value is correct.

See Also

- fix_eco_drc
- fix_eco_timing
- fix_eco_power

PTECO-084

(error) User specified MIM group must be subset of existing MIM groups.

Description

This error occurs when the specified MIM group is not the subset of existing MIM group.

What Next

Check the input group with existing MIM groups.

PTECO-085

(information) Library cell '%s' %s and is dropped from the estimation.

Feedback

Description

This error occurs when a library cell is supplied to the *estimate_eco* which is incompatible with the estimation type. For *size_cell* estimation this means that the library cell does not match the given cell instance and the reason for the mismatch (e.g. arcs or pins) is stated. For *insert_buffer* it means that the given library cell is logically not a buffer.

What Next

Use the *get_alternative_lib_cells* command to determine what library cells can be used to size your cell. For *size_cell* estimation, the user can also use the *size_cellfP command for more detailed information on the specific reason the cell types are incompatible.*

PTECO-086

(information) %d (%5.2f%%) %s library cells have power attribute '%s'.

Description

This message informs how many library cells (either combinational or sequential) have a valid power attribute when the user used the *-power_attribute* option of *fix_eco_power* or *fix_eco_timing* command. A valid power attribute value is a positive floating point number.

What Next

Use this information to verify that library cells have power attributes as expected. To report power attribute values set on library cells, use the *report_eco_library_cells* command with the *-power_attribute* option.

See Also

- fix_eco_power
- fix_eco_timing
- report_eco_library_cells

PTECO-087

(error) The -buffer_list option is specified, but insert_buffer is not included in the -methods option.

Description

The command requires to specify insert_buffer for the -methods option if a buffer list is specified in the -buffer_list option.

Feedback

What Next

Please add insert_buffer to the -methods option.

PTECO-088

(warning) There is more than one library cell with the name %s.

Description

There are multiple library cells with the same base name and voltage. This can potentially cause QoR issues when the PrimeTime *fix_eco_power* command is used because it expects each library cell's base name to be unique for the same voltage across all linked libraries.

What Next

Check and clean up the linked libraries to ensure that there are no duplicate library cell names with the same voltage.

See Also

- report_eco_library_cells
- fix_eco_power

PTECO-089

(information) Found %s power data...

Description

This information message shows that leakage or dynamic power is available and is up-to-date. The power data is used for driving activity-based power recovery when the *fix_eco_power* command is used with the *-power_mode* option.

What Next

After power recovery is done, check that the specified power type is recovered by running the *report_power* command.

See Also

- fix_eco_power
- report_power
- update_power

Feedback

PTECO-090

(information) Found %s power data in the %s scenario...

Description

This information message shows that leakage or dynamic power is available and is up-to-date in the scenario. The power data is used for driving activity-based power recovery when the *fix_eco_power* command is used with the *-power_mode* option.

What Next

After power recovery is done, check that the specified power type is recovered at the specified scenario by running the *report_power* command.

See Also

- fix_eco_power
- report_power
- update_power

PTECO-091

(error) Failed to find %s power data. Power is not available or is not up-to-date...

Description

This message occurs when leakage or dynamic power is not available or is not up-to-date. When *fix_eco_power* command is used with the *-power_mode* option, it requires valid power data to be available to drive activity-based power recovery.

What Next

Check that power analysis is performed by either the *update_power* command or the *report_power* command prior to running *fix_eco_power* command.

See Also

- fix_eco_power
- report_power
- update_power

Feedback

PTECO-092

(error) Failed to find %s power data in the %s scenario. Power is not available or is not up-to-date...

Description

This message occurs when leakage or dynamic power is not available or is not up-to-date in the scenario. When *fix_eco_power* command is used with the *-power_mode* option, it requires valid power data to be available at the scenarios specified by the *-leakage_scenario* or *-dynamic_scenario* options to drive activity-based power recovery.

What Next

Check that power analysis is performed in the scenario by either the *update_power* command or the *report_power* command prior to running *fix_eco_power* command.

See Also

- fix_eco_power
- report_power
- update_power

PTECO-093

(Warning) ECO fixing command disabling graph-based refinement.

Description

You receive this message when you have attempted an ECO fixing command (*fix_eco_**) and HyperTrace reporting is enabled:

```
set_app_var timing_enable_graph_based_refinement true
fix_eco_timing ...
fix_eco_power ...
```

To avoid unnecessary refinement updates during fixing timing updates, the fixing command temporarily disables HyperTrace reporting until the command completes.

However, the *fix_eco_timing* and *fix_eco_power* commands do provide a HyperTrace ECO fixing feature, enabled using a separate variable:

```
set_app_var eco_enable_graph_based_refinement true
fix_eco_timing ...
fix_eco_power ...
```

When the HyperTrace ECO fixing variable is enabled, the value of the HyperTrace reporting variable becomes irrelevant and this message does not occur.

Feedback

HyperTrace ECO fixing requires a PrimeECO license.

See Also

- eco_enable_graph_based_refinement
- timing_enable_graph_based_refinement

PTECO-094

(error) The option %s must be specified.

Description

This message occurs when either the *-leakage_scenario* or *-dynamic_scenario* option is not specified for activity-based power recovery in distributed multi-scenario analysis (DMSA) flow.

In DMSA flow, the tool gets its dynamic power data from exactly one scenario, which you must specify with the *-dynamic_scenario* option. Similarly, it gets its leakage power data from exactly one scenario, which you specify with the *-leakage_scenario* option. These options are used only in DMSA flow.

In general, you should specify the scenario showing the worst dynamic power and worst leakage power, respectively, for these two options. They could be the same scenario or two different scenarios. If you specify the *-power_mode total* option, both the *-leakage_scenario* and *-dynamic_scenario* options must be specified.

What Next

Specify the name of power scenario to either the *-leakage_scenario* or *-dynamic_scenario* options, or both depending on the type of power recovery.

See Also

- fix_eco_power
- report_power
- update_power

PTECO-095

(error) The %s option must be '%s' if the %s option is specified

Description

The specified option is not valid unless a correct value is specifed for the other option.

Feedback

What Next

Specify a valid opton as indicated by the error message

See Also

- fix_eco_timing

PTECO-096

(warning) Quality of results (QoR) might be impacted due to user interruption.

Description

fix_eco_timing/fix_eco_drc iteration has been interrupted by user. QOR might be impacted due to iteration abort.

Please double-check QOR result before you continue.

PTECO-097

(error) Could not find the block-level design to be replayed %s in the current design.

Description

The design name provided by the user to be replayed (read_eco_changes -design_name <design name>) is not present in the current design. The user should specify a valid block-level design name.

What Next

Provide a valid block (design) name as input to the read_eco_changes command.

PTECO-098

(error) Design name %s does not match with the design name %s in the changelist file.

Description

The block-level design name provided by the user (-design_name) to be replayed does not match the design in the replay file provided. Please provide the correct ECO changelist file or enter the matching block (design) name in read_eco_changes -design_name <design_name>.

PTECO-099

(warning) Ignoring lib cell %s as corresponding library cell definition does not exist.

Feedback

Description

This message occurs when either the *-buffer_list* or *-load_cell_list* options contain library cells whose corresponding definition is missing from loaded libraries.

What Next

Specify the name of library cells to either the *-buffer_list* or *-load_cell_list* options, or both, only if their corresponding libraries are loaded.

See Also

- fix_eco_timing
- read_db

PTECO-100

(warning) Cell instance %s found in %s, but not in %s.

Description

This message occurs when enabling option *-enable_consistence* and *-verbose* in command *check_eco*, and cell instance found in netlist file or physical database, but not found in the other one.

What Next

Please verify netlist file and physical database are consistent.

See Also

- check_eco

PTECO-101

(error) insert_buffer command is ignored because the specified buffer location is outside the physical boundary of the block.

Description

The coordinates provided in the insert_buffer command are not within the boundary of the block in which the buffer is being inserted.

PTECO-102

(warning) Ignoring '%s' as it %s %s.

Feedback

Description

The tool filters invalid cells from the buffer list. Specific filtering criteria are as follows.

- Invalid buffer

  A valid buffer should have a single input pin, a single output pin and a correct buffer logic function.

  Solution: Please specify a valid buffer to *fix_eco_timing -buffer_list* or *fix_eco_drc -buffer_list* command.

- Invalid inverter

  A valid inverter should have a single input pin, a single output pin and a correct inverter logic function.

  Solution: Please specify a valid inverter to *fix_eco_timing -buffer_list* or *fix_eco_drc -buffer_list* command.

- Invalid site definition

  A cell is valid when its LEF site definition matches DEF row site definition. If *-convert_sites* option is present in *set_eco_options* command, note that the DEF row site definition is converted and stored in the physical database. In addition, if *-keep_site_names* option is present in *set_eco_options* command, the cell is valid when its LEF site definition is included in the list of kept sites.

  Solution: Please check whether cell LEF site definition is consistent with DEF row site definition. In case of using *set_eco_options -keep_site_names*, please check whether cell LEF site definition is consistent with kept site names.

- Invalid power attribute

  The power attribute value of a cell is valid if it is a non-positive floating point number.

  Solution: Please use a positive float number for the power attribute value of the cell.

- Invalid dummy load cell

  A valid dummy load cell should have one input pin, no logic function and should be marked as a black box (is_black_box cell attribute should be set to true) and not a three-state cell (is_three_state cell attribute should be set to false).

  Solution: Please specify a valid dummy load cell to *fix_eco_timing -load_cell_list* command.

- Always_on cell

By default, always_on cells are filtered from the buffer list unless the following command is applied: *set_app_var eco_allow_sizing_with_lib_cell_attributes "always_on"*

Solution: Please remove always_on cells from the buffer list or enable their usage with *set_app_var eco_allow_sizing_with_lib_cell_attributes "always_on"*

- Level shifter cell

  Level shifter cells are filtered from the buffer list.

  Solution: Please remove a cell from the buffer list if its is_level_shifter attribute is set to true in the library.

What Next

Check the previously-described reasons, and follow the suggested solutions.

PTECO-103

(warning) Block '%s' has an invalid DEF row site '%s'.

Description

Site-aware ECO fixing requires a valid DEF row site definition of a block. Invalid DEF row sites prevent the tool from finding open sites, and cause unfixable reason 'O'.

What Next

If the *-convert_sites* option is used in the *set_eco_options* command, note that the DEF row site definition is converted and stored in the physical database. If the *-keep_site_names* option is used in the *set_eco_options* command, the provided site list must include DEF row site definitions.

PTECO-104

(error) '%s' is not a valid site definition.

Description

The site definition provided by the user is not present in the LEF files.

The *set_eco_options -keep_site_names* command requires a list of valid site names to enable site-aware physical ECO fixing.

What Next

Please provide a valid site to set_eco_options -keep_site_names command.

Feedback

PTECO-105

(warning) Ignoring custom training data '%s' as the '-power_mode' option is not specified

Description

The custom trainind data is ignored as the *-power_mode* option of the *fix_eco_power* command is not specified.

Custom training data written by the *write_training_data* command contain leakage, dynamic and total power information generated after the *update_power* command is executed. In order to use the power information in the training data, it is required to specify the *-power_mode* option for the *fix_eco_power* command. Otherwise, the trainind data will be ignored.

What Next

Specify *'-power_mode total'* for the *fix_eco_power* command.

PTECO-106

(error) The estimate_eco command failed because fast estimation is enabled.

Description

Estimate_eco could hit failure when fast estimation has been enabled while without corresponding timing-paths.

What Next

Please turn off fast estimation before run estimate_eco command.

PTECO-107

(warning) Cannot identify design name for DEF file %s

Description

This error message occurs when a file provided to *set_eco_options -physical_design_path* option does not contain the DESIGN statement, which is mandatory in Design Exchange Format (DEF) syntax.

What Next

Check that the specified file is a valid DEF file.

Feedback

See Also

- set_eco_options
- eco_enable_overwrite_physical_design_path

PTECO-108

(warning) The variable 'timing_update_effort' is set as high.

Description

This warning message alerts the user that the variable *timing_update_effort* is set as high. This would make the runtime of every timing update within PrimeTime ECO command (e.g. *fix_eco_timing*, *fix_eco_drc*, and *fix_eco_power*) slower.

What Next

If this is not expected, the variable *timing_update_effort* could be changed as per the requirements.

See Also

- fix_eco_timing
- fix_eco_drc
- fix_eco_power

PTECO-109

(error) No physical blocks found.

Description

No physical blocks found at the *current_instance* hierarchy level.

What Next

Please use *-hierarchical* option to see if there are physical blocks present in the lower-level hierarchies. Alternatively, try setting the *current_instance* at the top-level of the design to find out physical blocks in the entire design.

PTECO-110

(error) Load cap cell insertion is ignored because the specified buffer location is outside the physical boundary of the block.

Feedback

Description

The coordinates provided for the load cap cell are not within the boundary of the block in which it is being inserted.

PTECO-111

(error) No valid libraries found in the linked design.

Description

Either of link_path or search_path is incorrect. Please set it correctly and try again.

PTECO-112

(warning) Net '%s' does not have internal parasitic location.

Description

Missing internal parasitic locations for the net causes suboptimal solution for *insert_buffer* method in physical mode, and results in unfixable reason "R".

What Next

The physically aware ECO flow uses the parasitic node locations to accurately determine the effects of placing an ECO cell on a net. For *insert_buffer* method in physical mode, it suggests to include internal parasitic locations for violation nets in parasitic files. Set this option in StarRC command file to make internal parasitic node locations available: NETLIST_NODE_SECTION: YES Set read_parasitics_load_locations as true before reading parasitics.

See Also

- fix_eco_drc

PTECO-113

(information) Enabling %s with HyperTrace.

Description

The *fix_eco_power* or *fix_eco_timing* command will use HyperTrace technology to enhance ECO fixing based on path-based analysis (PBA). This mode is activated when *eco_enable_graph_based_refinement* is set to true.

Feedback

See Also

- fix_eco_power
- fix_eco_timing
- eco_enable_graph_based_refinement

PTECO-114

(warning) HyperTrace-based ECO fixing is not enabled as it cannot be used with %s option.

Description

Based on the current setting of *eco_enable_graph_based_refinement*, the *fix_eco_power* or *fix_eco_timing* command attempted to enable HyperTrace technology to enhance fixing. However, user-provided option described in the message prevented it from doing so.

What Next

Consider changing the option of the relevant command.

See Also

- fix_eco_power
- fix_eco_timing
- eco_enable_graph_based_refinement

PTECO-115

(information) Running HyperTrace-based ECO fixing.

Description

This message indicates that the current ECO fixing command is using HyperTrace-based ECO fixing algorithms. This mode is activated when the *eco_enable_graph_based_refinement* variable is set to *true* and the *fix_eco_timing* or *fix_eco_power* command is used.

Feedback

When this message is issued,

- HyperTrace technology is fully integrated into the ECO fixing algorithms. The *timing_enable_graph_based_refinement* variable is not used or needed.
- The graph refinement variables used by HyperTrace reporting are also not used or needed:

```
timing_refinement_min_slack_threshold
timing_refinement_max_slack_threshold
timing_refinement_maximum_critical_pin_percentage
```

Note that if any of the following unsupported options are used:

```
fix_eco_timing -path_selection_options
fix_eco_power -start_end_type reg_to_reg
fix_eco_power -pba_path_selection_options
```

then the fixing command reverts to partially integrating HyperTrace into the ECO fixing algorithms, a PTECO-116 message is issued instead of this message, and the graph refinement variables are used. For details, see the PTECO-116 man page.

See Also

- fix_eco_power
- fix_eco_timing
- eco_enable_graph_based_refinement
- PTECO-116

PTECO-116

(information) Enabling HyperTrace exhaustive path-based analysis reporting to accelerate exhaustive PBA-based ECO fixing.

Description

This message indicates that the current ECO fixing command is using HyperTrace reporting technology to accelerate the fixing process. This mode is activated when the *eco_enable_graph_based_refinement* variable is set to *true*, but the current ECO fixing command does not support full HyperTrace-based ECO fixing (as described in the PTECO-115 man page).

Feedback

When this message is issued,

- HyperTrace exhaustive PBA reporting is enabled by implicitly setting the *timing_enable_graph_based_refinement* variable to *true* for the duration of the ECO fixing command.
- The graph refinement variables used by HyperTrace reporting are also used during ECO fixing:

```
timing_refinement_min_slack_threshold
timing_refinement_max_slack_threshold
timing_refinement_maximum_critical_pin_percentage
```

Whether or not HyperTrace is used to accelerate the exhaustive PBA analysis depends on the refinement slack thresholds being set to appropriate values. To utilize HyperTrace acceleration, you must ensure that the refinement slack thresholds used by HyperTrace reporting bound the implicit or explicit *-slack_lesser_than value* of the ECO fixing command. See the *eco_enable_graph_based_refinement* man page for more details.

Normally, the *fix_eco_timing* and *fix_eco_power* commands fully integrate HyperTrace into the ECO fixing algorithms, as indicated by a PTECO-115 message. However, if any of the following unsupported options are used:

```
fix_eco_timing -path_selection_options
fix_eco_power -start_end_type reg_to_reg
fix_eco_power -pba_path_selection_options
```

then the fixing command partially integrates HyperTrace into the ECO fixing algorithms, as indicated by this message.

Distributed Multi-Scenario Analysis (DMSA)

In a Distributed Multi-Scenario Analysis (DMSA) fixing flow, the refinement slack thresholds can be set independently at each scenario, allowing per-scenario usage of HyperTrace technology to accelerate path-based analysis invoked during fixing. Consult the per-scenario logs to determine if HyperTrace has been used at individual scenarios.

See Also

- fix_eco_power
- fix_eco_timing
- eco_enable_graph_based_refinement
- timing_enable_graph_based_refinement
- timing_refinement_max_slack_threshold

- timing_refinement_min_slack_threshold
- PTECO-115

PTECO-117

(information) HyperTrace will not be used to accelerate PBA-based ECO fixing for delay_type %s, as the refinement slack threshold is set to 'disabled'.

Description

This message is received when a PBA-based ECO fixing command attempts to enable HyperTrace accelerated PBA, but the relevant refinement threshold is set to a value of *disabled*.

Graph refinement (and thus HyperTrace acceleration) is restricted to the *slack-critical* region of the design, which is the set of pins whose slack is the same or less than the following min/max slack threshold variables:

```
timing_refinement_max_slack_threshold  (default: 0)
timing_refinement_min_slack_threshold  (default: 'disabled')
```

Because HyperTrace acceleration is disabled for that delay type, it will not be used to accelerate this PBA-based ECO fixing command.

What Next

To use HyperTrace accelerated PBA for the ECO command, set the corresponding refinement min/max slack threshold variable to a numeric value that bounds the highest slack value you want to analyze.

See Also

- fix_eco_power
- fix_eco_timing
- eco_enable_graph_based_refinement
- timing_refinement_max_slack_threshold
- timing_refinement_min_slack_threshold

PTECO-118

(warning) Overwriting previously defined physical data specification for block %s.

Feedback

Description

The named block has previously defined physical data which is being overwritten. This may be because duplicate DEF files are being provided for a given design.

What Next

Check the specification of the blocks in set_eco_options.

See Also

- set_eco_options

PTECO-119

(warning) Block '%s' does not have any %s.

Description

The block with the given name does not have any objects of the specified type. This may be because there are no objects of that type in the DEF file, or because any existing objects of that type were ignored.

What Next

Check the validity of the corresponding DEF file.

PTECO-120

(Warning) Physical attribute disabled.

Description

The application tries to query a physical database attribute, but the feature physical_attributes_query is not enabled.

What Next

If the feauture physical_attributes_query is enabled, ECO-ELT license will be checked out while querying physical database attributes.

PTECO-121

(Error) Failed to write '%s' to session file.

Feedback

Description

The write_eco_session command failed to write the specified information to the session file.

What Next

Please check the permission and disk space of the specified session directory.

PTECO-122

(warning) Net '%s' does not have a valid driver.

Description

This warning message is issued when the net is not defined in the DEF file or the driving cell of the net is a black-box.

What Next

Check if the DEF file does not define the net or the driving cell of the net is a black-box. Missing .db loading can cause black-box cells.

PTECO-123

(error) No physical data is found for the cell '%s'.

Description

This message is issued when local layout effect (LLE) analysis is enabled and the cell does not have physical data.

What Next

Check if the cell has a corresponding macro definition in the LEF files.

PTECO-124

(warning) '%s' layer is missing in the LEF macro '%s'.

Description

This message is issued when local layout effect (LLE) analysis is enabled and the LEF macro does not have the layer that is necessary for LLE physical parameter computations.

What Next

Check if the layer information is described in the corresponding LEF file.

Feedback

PTECO-125

(error) A cycle has been detected during context-aware parameter scan to the %s, which starts from '%s' and visits '%s' twice. Failed to compute the context-aware parameter values.

Description

This message is issued when local layout effect (LLE) analysis is enabled and an unexpected loop is detected in the internal data structure.

What Next

Send the test case to Synopsys to debug this problem.

PTECO-126

(error) The corresponding library of the cell bounding box '(%d, %d), (%d, %d)' cannot be found. If it is a physical only cell, a dummy library is required.

Description

This message is issued when local layout effect (LLE) analysis is enabled and a cell without a corresponding library is found during the context-aware scan.

What Next

Specify the corresponding library. If it is a physical only cell, you must create a dummy library for the cell.

PTECO-127

(information) Stored necessary parameters from LEF macro '%s' for local layout effect (LLE) computation.

Description

This message is issued when local layout effect (LLE) analysis is enabled, a macro in the library exchange format (LEF) file is read, and the necessary parameters are cached successfully from the LEF macro for LLE physical parameter computation.

PTECO-128

(error) The physical shape information of the poly layer is missing from the LEF macro '%s' %s and the poly width assumption is invalid (%.6f um).

Description

This message is issued when local layout effect (LLE) analysis is enabled, poly layer shape information of the macro is missing in the library exchange format (LEF) file, and the variable for the assumed poly width has not been set or is set to an invalid value.

What Next

Provide the poly shape information of the macro in the LEF file or set a correct value to the *timing_lle_assume_poly_width_in_micron* variable.

PTECO-200

(information) Dump '%s' collateral from HyperGrid worker '%s' to file '%s'.

Description

This message indicates the corresponding step has been executed in write_eco_session command to write out timing collateral in binary format.

What Next

For information purpose only.

PTGUI

PTGUI-100

(warning) A timing update is required before timing data in the current design can be displayed in the GUI.

Description

The variable timing_save_pin_arrival_and_slack was found set to FALSE. To display data in the GUI, the slack and arrival window attribute data must be present for pins that are not endpoints. For this reason, a timing update will be required before data can be displayed on the current design.

To make such updates unnecessary in the future, please set timing_save_pin_arrival_and_slack to TRUE before running the last timing analysis prior to starting the GUI. Runtime for PrimeTime timing analysis may increase when this variable is set to TRUE, but it will save the time when you start the GUI.

What Next

For more information please refer to PrimeTime User Guide and the man page for timing_save_pin_arrival_and_slack.

Feedback

PTGUI-101

(Warning) Disabling GUI due to an invalid value for shell environment variable DISPLAY.

Description

The shell environment variable DISPLAY is used to identify a X server to use for GUI display. This variable was either blank or set to an invalid X server name. All GUI features will be disabled.

To enable GUI features, please set the DISPLAY variable to a valid value before starting PrimeTime.

PTGUI-102

(Warning) Disabling GUI due to missing symbol library in the installation.

Description

The symbol library used to display logical schematic views in PrimeTime GUI could not be opened for reading. All GUI features will be disabled.

To enable GUI features, please ensure that the the Synopsys root in use has been properly installed before starting PrimeTime.

PTGUI-801

(error) cannot create category rule '%s' since the previously created rule is not built-in.

Description

This error message occurs when an attempt is made to create a category rule with the -builtin option even though the previously created rule is not built-in.

What Next

Rerun gui_create_category_rule without the -builtin option.

See Also

- gui_create_category_rule

PTGUI-802

(error) cannot create category rule '%s' since it has an error in the category specification string at position %d.

Feedback

Description

This error message occurs when gui_create_category_rule is run with a -category option value which has a syntax error.

What Next

Fix the syntax error in the -category option string value and rerun gui_create_category_rule.

See Also

- gui_create_category_rule

PTGUI-803

(error) cannot create category rule with name '%s' since a rule with that name already exists.

Description

This error message occurs when an attempt is made to create a category rule with a rule name that is already in use.

What Next

Rerun gui_create_category_rule with a -name option value which is not a rule name that is already in use.

See Also

- gui_create_category_rule

PTGUI-804

(error) for category rule '%s' cannot add subrule '%s' since no such rule exists.

Description

This error message occurs when gui_create_category_rule -subrules references a rule which does not already exist.

What Next

One possibility is that the subrule name was mis-spelled when passed to -subrules. In that case rerun gui_create_category_rule but passing the correctly spelled rule name to -subrules. Another possibility is that the rule name passed to -subrules was correctly spelled but does not yet exist. In that case, create a new rule with that name (using

Feedback

gui_create_category_rule -name) and then rerun the gui_create_category_rule -subrules command that failed.

See Also

- gui_create_category_rule

PTGUI-805

(error) cannot add subrule '%s' since that subrule has already been added to the category rule '%s'.

Description

This error message occurs when gui_create_category_rule -subrules references the same subrule (using the same rule name) more than once in the subrules list.

What Next

Rerun gui_create_category_rule -subrule but removing duplicate references to the rule name that was listed in the subrules more than once.

See Also

- gui_create_category_rule

PTGUI-806

(error) -rule_names or -names contains invalid category rule name '%s'.

Description

This error message occurs when a command is run which accepts a list of category rule names via -rule_names or -names and that list includes a category rule name which does not exist.

What Next

Rerun the command with corrected spelling for the rule name (passed to -rule_names or -names) which was mis-spelled.

See Also

- gui_list_category_rules

Feedback

PTGUI-807

(error) cannot evaluate category specification since no attribute '%s' exists for '%s'.

Description

This error message occurs when -category references an attribute which does not exist for an object that the category rule is executed for.

What Next

Revise the -category spec to use an attribute which exists for the object in question.

See Also

- gui_create_category_rule

PTGUI-808

(error) cannot evaluate category specification since attribute '%s' is a collection.

Description

This error message occurs when -category references an attribute whose value is a collection containing multiple objects.

What Next

Referencing a collection containing multiple objects is currently not supported in -category. Use a different attribute instead.

See Also

- gui_create_category_rule

PTGUI-809

(error) cannot evaluate category specification since attribute '%s' of type '%s' has sub-attributes.

Description

This error message occurs when -category references an attribute whose value is a collection containing a single object.

Feedback

What Next

Consider using "dot notation" in -category to access an attribute of the object in the collection. For example, instead of -category <startpoint> try -category <startpoint.full_name>. Use list_attributes to discover the attributes supported for the type mentioned in the error message.

See Also

- gui_create_category_rule

PTGUI-810

(error) cannot create category rule '%s' since it has an error in the filter specification string.

Description

This error message occurs when gui_create_category_rule is run with a -filter option value which has a syntax error.

What Next

Fix the syntax error in the -filter option string value and rerun gui_create_category_rule.

See Also

- gui_create_category_rule

PTHC

PTHC-001

(information) %s.

Description

This is just a generic informational message.

What Next

No action needed.

PTHC-002

(waring) %s.

Feedback

Description

THis is a generic warning message.

What Next

Please note and confirm the specific reason indicated by the warning message, modify setting(s) accordingly, re-issue the command(s) if necessary.

PTHC-003

(error) %s.

Description

This is a generic error message.

What Next

Please note and confirm the specific reason indicated by the error message, modify your setting(s) accordingly, re-issue the command(s).

PTHC-004

(error) Cannot change the state of high capacity mode because %s.

Description

This error message is issued when the attemp to change the state of high-capacity mode fails due to the reason indicated. Most often, it happens when you are trying to either enable or disable high capacity mode after designs and/or libraries have already been loaded into PrimeTime.

What Next

Please verify the reason indicated by the error message, make sure you issue the command 'set_program_options' earlier, e.g. before any library/design is loaded.

PTHST

PTHST-100

(warning) %d errors were detected during the Tcl command evaluation.

Feedback

Description

While evaluating the Tcl command string given as the *-tcl_cmd* option with each object in the collection, a number of errors were encountered.

What Next

For more information see the *create_histogram* command man page.

See Also

- create_histogram

PTIO

PTIO-1

(error) Cannot open file '%s' for %s.

Description

The specified file could not be opened for reading or writing. If reading, the file may not exist, or might have incorrect permissions. If writing, you may not have access to the directory.

What Next

Verify the file name, directory name, and permissions.

PTIO-2

(error) %s for '%s' failed: %s

Description

A problem occured when reading or writing a file. For example, when writing an SDF file, you ran out of disk space. The message will indicate the command and problem.

What Next

Action based on the problem, indicated in the message.

PTIO-3

(error) Failed to create directory '%s'.

Feedback

Description

The specified directory could not be created by Primetime. You may not have access to the directory.

What Next

Verify the permissions and reissue the command

PTIO-4

(error) The remote process expected directory '%s' to '%s'

Description

While the worker process was performing an operation, it expected the directory specified to exist or non-exist as indicated. The manager process is responsible for manipulating the directories but failed to complete the operation.

What Next

Verify the permissions and reissue the command.

PTIO-5

(warning) Writing to pt_tmp_dir failed.

Description

The *pt_tmp_dir* is used to store data when high capacity mode is enabled. If there is not enough space available in this directory, or errors occur when writing to the directory, the performance and memory usage of the analysis may be negatively affected.

What Next

Please free up some space in the *pt_tmp_dir* if full, or specifiy another *pt_tmp_dir* before performing the analysis.

See Also

- set_program_options
- pt_tmp_dir

PTIO-6

(warning) The pt_tmp_dir variable is set to a nonlocal partition.

Feedback

Description

When you change the *pt_tmp_dir* variable to a nonlocal partition, expect performance to degrade if you enable the high capacity mode using the *set_program_options* command.

What Next

Set the *pt_tmp_dir* variable to a local partition if you want to achieve optimal performance when using the high capacity mode.

See Also

- set_program_options
- pt_tmp_dir

PTIO-7

(severe) The parasitics server was unable to write the parasitics file when terminating.

Description

When the parasitics server terminates, it transfers data back to the main PrimeTime application through several files located in *pt_tmp_dir*. When this directory is full, it is unable to transfer parasitics information and the correct execution of PrimeTime is compromised.

What Next

Several options exist, you can use one or several in combination to solve this problem: - Set the *pt_tmp_dir* variable to a partition with enough free space; - Disable multi-core by using *set_host_options -max_cores 1*; - Turn off disk caching by using *set_program_options -disable_high_capacity*.

See Also

- pt_tmp_dir
- set_host_options
- set_program_options

PTIO-8

(information) %s.

Description

An informational message for specified IO actions or events with Primetime.

Feedback

What Next

No action required.

PTIO-9

(warning) Failed to create the directory '%s' because '%s'

Description

Creation of the directory specified failed because of the explanation provided. The explanation is of the form "[<cmd>:<code>] <reason>" where

<cmd> : This is the operation being performed. <code> : This is the error code. <reason> : This is the explanation for the failure.

What Next

Ensure that the hierarchial path leading up to the leaf location exists and that the user has read/write permissions for that location.

PTIO-10

(warning) Failed to create a random directory in '%s' because '%s'

Description

Creation of a random directory inside the directory specified failed because of the explanation provided. The format for the explanation is of the form "[<cmd>:<code>] <reason>" where

<cmd> : This is the operation being performed. <code> : This is the error code. <reason> : This is the explanation for the failure.

What Next

Ensure that the directory specified exists and that the user has read/write permissions for that location.

PTIO-11

(warning) Failed to create a random file in '%s' because '%s'

Description

Creation of a random file inside the directory specified failed because of the explanation provided. The format for the explanation is of the form "[<cmd>:<code>] <reason>" where

Feedback

<cmd> : This is the operation being performed. <code> : This is the error code. <reason> : This is the explanation for the failure.

What Next

Ensure that the directory specified exists and that the user has read/write permissions for that location.

PTIO-12

(error) Program ran out of addressable memory.

Description

Storage infrastructure module ran out of addressable memory, the program must be aborted.

What Next

Seek advice on tuning the configuration of storage infrastructure.

PTIO-13

(information) The pt_tmp_dir variable is set to a directory that is on a Solid State Disk (SSD).

Description

When you change the *pt_tmp_dir* variable to a directory that is on an Solid State Disk (SSD), the disk caching infrastructure will operate more aggresively to take advantage of the performance of the disk.

What Next

No action required.

See Also

- set_program_options
- pt_tmp_dir

PTIO-14

(information) created unique pt_tmp_dir %s.

Feedback

Description

When *sh_pt_tmp_dir_unique_mode* is enabled, a randomized subdirectory will be created for *pt_tmp_dir*.

What Next

No action required.

See Also

- sh_pt_tmp_dir_unique_mode
- pt_tmp_dir

PTLIB

PTLIB-001

(error) The input of option -index_1 is invalid.

Description

The command *set_lib_max_cap_table* issues this error message when option -index_1 is specified with a invalid list of values.

What Next

Make sure the values in the list are monotonically increasing.

PTLIB-002

(error) The length of the input option -index_1 and -value should be the same.

Description

The command *set_lib_max_cap_table* issue this message when the input frequency indices and capacitance values are of two different length input lists.

What Next

Make sure the the input list of options -index_1 and -value have same length.

PTLIB-003

(error) No max cap table on the specified library pin '%s', failed to set max cap table.

Feedback

Description

The *set_lib_max_cap_table* command issues this message when there is no max cap table on the specified library pin.

What Next

Make sure the specified library pin contains max cap table or use -force option.

PTLIB-004

(error) The desired table on the specified library pin '%s' is not a 1-d frequency based max_cap table, failed to set max cap table.

Description

The *set_lib_max_cap_table* command issue this message when the desired table on the specified library pin is not a 1-d frequency based max_cap table. The *set_lib_max_cap_tablecommand supports only to override the 1-d frequency based max_cap table.*

What Next

Make sure the desired table on the specified library pin is a 1-d frequency based max_cap table.

PTLIB-005

(error) The input list of options -index or -value are empty.

Description

The command *set_lib_max_cap_table* issues this error message when the input list of options -index or -value are empty.

What Next

Make sure to provide values.

PTLIB-006

(error) Invalid frequency index value '%f', failed to override frequency index on the library pin '%s'.

Description

The *set_lib_max_cap_table* command issues this message when the specified -index_1 option is not in the table. Allowed only to override the existing table index

Feedback

What Next

Please provide the existing max cap table frequency index.

PTLIB-007

(error) Trying to set max cap table on library pin '%s' of directon '%s', failed to set max cap table.

Description

The *set_lib_max_cap_table* command issues this message when try to set max cap table on library pin which is not of direction Output or Inout.

What Next

Please provide a library pin of direction Output or Inout.

PTLIB-008

(error) Slew derate inconsistency found in library %s for %s.

Description

This message is issued when slew derate inconsistency is found for the specified library. The inconsistency happens when slew derate times the difference between upper and lower thresholds for pct rice/fall is greater than 1.

What Next

Please verify the values for slew_lower[upper]_threshold_pct_rise[fall] attributes in the library.

PTLIB-009

(Error) %s CCS noise model is invalidated because: %s

Description

This error message indicates that an issue was found with an arc or pin CCS noise model during library read. As a result, the model is invalidated and not used in delay calculation.

These checks are always performed, but they are reported only when the *rc_ccsn_enable_library_error_reporting* variable is set to *true*.

If library scaling groups are being used, invalidated CCS noise models can cause scaling group inconsistencies, resulting in SLG-403 errors.

Feedback

The limit value for the maximum current check can be set with the following variable:

```
pt_shell> set_app_var rc_ccsn_dc_current_limit_in_ma ...
```

What Next

Investigate and fix the CCS noise model issue in the library.

See Also

- rc_ccsn_dc_current_limit_in_ma
- rc_ccsn_enable_library_error_reporting
- RC-201
- SLG-403

PTLIB-010

(Warning) CCS receiver model of %s : %s

Description

You receive this warning because PrimeTime find a library CCS receiver model issue that may affect delay calculation accuracy. The message shows only when rc_receiver_enable_library_error_reporting is set to TRUE.

Types of warning

Negative capacitance value detected: PrimeTime does not support negative capacitance value in delay calculation.

Capacitance glitch detected: large fluctuation in C1Cn cap value may cause delay calculation inaccuracy.

The following example shows when negative value is detected:

Warning: CCS receiver model INV_4X: arc I->ZN : negative capacitance value detected. (PTLIB-010)

What Next

This is an informational message and no action required.

See Also

- rc_receiver_enable_library_error_reporting

Feedback

PTLIB-011

(Warning) Extrapolation is applied bounding to 10% of the limit.

Description

Extrapolation is applied to estimate the value of the capacitance for the respective frequency value and is bounded to 10% of the limit,if the freq lies in a range outside of the given data set.

This warning message will be thrown when user has overriden the freq-cap data from library i.e. when *set_lib_max_cap_table* is used to override the freq-cap data for the lpin.

What Next

This is an informational message and no action required.

PTNDM

PTNDM-001

(Error) NDM library '%s' not found.

Description

The PrimeTime tool could not find the library in specified directory.

What Next

Specify the correct path the IC Compiler II design library. You can specify either an absolute or relative path. For a relative path, the path must exist in the current working directory or a path specified by the *link_path* variable. Be sure to specify the library or library and block name in the proper form:

`[path/]library[:block[/label]][.view]`

For details, see the man page for the *read_ndm* command.

PTNDM-002

(Error) NDM library version prior to O-2018.06 not supported.

Description

The *read_ndm* command supports the reading of NDM block netlist data generated by IC Compiler II version O-2018.06 or later. The specified library did not meet this requirement.

Feedback

What Next

If you have data generated by an older IC Compiler II version, you can use a newer version of the tool to read in the data and save it in the current format. Start the newer IC Compiler II tool (O-2018.06 or later), open the library with the *open_lib* command, and save the library with the *save_lib* command.

PTNDM-003

(Information) Loading NDM design '%s'.

Description

The NDM design netlist is being loaded.

What Next

Wait for loading to be completed.

PTNDM-004

(Error) NDM design '%s' generated using older version. NDM design version prior to O-2018.06 not supported. Skipping design creation.

Description

The *read_ndm* command supports the reading of NDM block netlist data generated by IC Compiler II version O-2018.06 or later. The specified block did not meet this requirement.

What Next

If you have data generated by an older IC Compiler II version, you can use a newer version of the tool to read in the data and save it in the current format. Start the newer IC Compiler II tool (O-2018.06 or later), open the block with the *open_block* command, and save the block with the *save_block* command. Then you can read the netlist data from the newly saved block.

PTSML

PTSML-001

(information) disabled the Synopsys Monitoring Library.

Feedback

Description

The Synopsys Monitoring Library is disabled and will not monitor critical system throughout the lifetime of the PrimeTime process.

What Next

No action is needed from the user.

PTSML-002

(warning) failed to start the Synopsys Monitoring Library '%s'

Description

The Synopsys Monitoring Library failed to start due to the given reason.

What Next

If monitoring of the critical resources is needed, correct the problem reported and restart PrimeTime, otherwise this warning can be ignored.

PTSML-003

(warning) failed to stop the Synopsys Monitoring Library '%s'

Description

The Synopsys Monitoring Library failed to stop due to the given reason.

What Next

If monitoring of the critical resources is needed correct the problem reported and restart PrimeTime, otherwise this warning can be ignored.

PTSML-004

(Information) resource event resolved '%s (%.2f%%)'

Description

The Synopsys Monitoring Library has reported that the resource issue indicated is resolved.

PTSML-005

(Warning) resource event detected '%s (%.2f%%)'

Feedback

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which PrimeTime is running.

Low memory availability

```
----------------------
o This message indicates that the host is running low on
  available memory to service the processes its running.
o This event arises where the current process is running
  on a host with insufficient ram or is being starved of
  ram by other processes running on the host. It is
  detected where there sum of the free memory and cached
  memory is <5% of the total ram in the host.
o Run PrimeTime on a host with sufficient ram or on a host
  where it is not competing with other processes for ram.
```

High cpu utilization (current process <5%)

```
----------------------------------------
o This message indicates that the host is heavily loaded
  by all the processes running on it and that the current
  process is experiencing cpu starvation.
o This event arises where the current process is running
  on a host where it is only utilizing <5% of the total
  cpu capability, yet the host is running at >95% load.
o Run PrimeTime on a host with sufficient cores to satisfy
  the number of cores PrimeTime is specified to use.
  If the run is on a farm host, ensure the number of slots
  reserved on the host is sufficient to reserve the number
  of cores PrimeTime is specified to use.
```

High network packet loss

```
-----------------------
o This message indicates that the host is encountering
  poor network connectivity and that the percentage of
  packets shown, are being lost.
o This event arises where the current process is running
  on a host where >5% of the network packets it is sending
  are not being received by their intended recipient.
o Contact your IT department to investigate if there are
  any hardware issues with the host or problems with the
  network to which the host is connected.
```

High network packet retransmission

```
---------------------------------
o This message indicates that the host is encountering
  poor network connectivity and that the percentage of
  packets shown, had to be retransmitted.
o This event arises where the current process is running
```

Feedback

```
  on a host where >5% of all packets being transmitted
  had to be retransmitted due to loss or damage. It is
  an indicator that the network to which the host is
  connected is heavily congested.
o Contact your IT department to investigate if there are
  any hardware issues with the host or problems with the
  network to which the host is connected.
```

PTSML-006

(Information) resource event resolved '%s'

Description

The Synopsys Monitoring Library has reported that the resource issue indicated is resolved.

PTSML-007

(Warning) resource event detected '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which PrimeTime is running.

High network latency

```
--------------------
o This message indicates that the host is encountering
  poor network connectivity to the hosts indicated and
  the associated latency.
o This event arises where the current process is running
  on a host where it has TCP connections to another
  host and the network latency is >300ms. It is an
  indicator that the network to which the host is
  connected is heavily congested or there is a problem
  with networking hardware.
o Contact your IT department to investigate if there are
  any hardware issues with the host or problems with the
  network to which the host is connected.
```

PWR

PWR-001

(error) Power analysis is disabled.

Feedback

Description

You received this error message because the *power_enable_analysis* variable has been set to *false* while the command requires power analysis.

What Next

First, determine whether you want to perform power analysis. If you do, then set *power_enable_analysis* to *true*.

PWR-002

(error) Cannot proceed without power analysis feature.

Description

You received this error message because the command requires power analysis feature. The first power related command brings out the power analysis feature. This command cannot be the first command.

What Next

Make sure you set the variable power_enable_analysis to true at the beginning of your script. Make sure you have PrimePower license. Look at the man page of this command, and use it correctly.

PWR-003

(information) Setting timing_save_pin_arrival_and_slack to TRUE.

Description

You receive this informational message because sometimes in power extension mode, the timing_save_pin_arrival_and_slack variable must be set to TRUE for accurate power analysis.

What Next

This is an informational message. No action is required on your part.

See Also

- power_enable_analysis
- timing_save_pin_arrival_and_slack

Feedback

PWR-004

(error) Save and restore failed for user options.

Description

You received this error message because save and restore of user options did not behavior correctly.

What Next

Check whether same versions of PrimePower were used for save and restore.

PWR-005

(error) Run out of memory.

Description

You received this error message because the program runs out of memory.

What Next

Check whether the machine has the memory large enough to run the application.

PWR-006

(error) Event file (VCD or its equivalent) was not properly set for time based %s.

Description

You received this error message because time based power analysis did not find the corresponding event information specified by read_vcd command.

What Next

Check whether read_vcd command was specified or ran correctly. This command is required before update_power for time based power analysis.

PWR-007

(warning) VCD coverage on the design is too small. Power may be underestimated.

Description

You received this warning message because the annotated event coverage from VCD or its equivalent was too small. The activities of some parts of the design were not captured in the current VCD. This could be the name of the instance of the current design given by

Feedback

option -strip_path is incorrect, the time window specified by -time is out of range, the VCD file is EVCD, or VCD has syntax errors.

What Next

Check read_vcd command, especially the -strip_path and -path options to see whether VCD events were applied to the proper hierarchy of the design. Also check read_vcd command's log and see if it reports any syntax error about VCD. Be aware EVCD is not supported.

PWR-008

(error) The value of power_ui_backward_compatibility variable in the restore session is not the same as that in the save session.

Description

The power_ui_backward_compatibility variable determines whether PrimeTime uses the UI of 2008.06 or current release. You received this error message because the saving and restoring power related sessions used different values for this variable, which is not allowed in PrimePower.

What Next

Change the variable so that save and restore sessions use the same version of PrimeTime.

PWR-009

(warning) reset_power_derate on sequential cell

Description

By default, the clock pin power of sequential cell is included in the clock network power group. When there are different power derate value on the sequential cell and on clock network power group, the reset_power_derate command on the sequential cell only resets the sequential cell power derate. The power derate on clock network power group remains the same.

What Next

To reset the power derate of clock network power group, use reset_power_derate, reset_power_derate [current_design] or reset_power_derate -group clock_network

Feedback

PWR-010

(warning) Simulation end time '%f' ns is significantly later than the last effective event time %f ns.

Description

PrimePower uses the simulation time interval to calculate average power. The warning message is issued when there is a duration of time before the simulation end time in which there is no effective events for the design, and such a duration is at least 5% of the whole simulation time interval. Power may be underestimated if the simulation end time in event file is not correctly set for power purpose.

What Next

Check whether the simulation end time is correct. If not, either change event file or set a time duration for read_vcd command.

PWR-011

(Warning) Can't find design rail '%s' in current design.

Description

Can't find the design rail specified from user interface.

What Next

Check the -rails option of the related command and fix the design rail name.

PWR-012

(Warning) Can't find lib rail '%s' connected for lib_cell '%s'.

Description

Can't find the library rail connected to the library cell.

What Next

Check whether the library cell data in library is properly characterized.

PWR-013

(Error) The -rails option of report_power command can only be used when the power_enable_multi_rail_analysis variable is set true.

Feedback

Description

The -rails option of report_power command is designed to work when the power_enable_multi_rail_analysis variable is true.

What Next

Turn on the multirail power analysis feature by setting the power_enable_multi_rail_analysis variable to true.

See Also

- report_power
- power_enable_multi_rail_analysis

PWR-014

(Error) The key word 'all' is not supported by -rails option of set_annotated_power command.

Description

set_annotated_power -rails [rail_list] did not support the key word 'all'. If you would like to set annotated power on all rails, use the command without the -rails option.

What Next

Remove the -rails all option from set_annotated_power command and run the script again.

PWR-015

(error) Can't find any valid design rail specified in the set_annotated_power -rails option.

Description

set_annotated_power -rails [rail_list] accepts a list of valid design rail names. The error occurs when there is no valid rail found from the rail name list.

What Next

Check and fix the design rail names in the -rails option.

PWR-016

(error) Concurrent multi-rail power analysis does not support non-UPF power domain mode.

Feedback

Description

Concurrent multi-rail power analysis should be used for the designs under UPF specification or designs used legacy rail mapping mode. The non-UPF power domain mode is used supported.

What Next

Translate the script to UPF and run the concurrent multi-rail power analysis again.

PWR-017

(error) Lower power design environment is changed inside the script.

Description

The low power design environment for PrimePower is specified by the variable power_domains_compatibility and based on whether there is any power domain specification for the design. The environment should not be changed during one PrimePower run session.

What Next

Suggest to use the UPF to specify the low power design intention.

PWR-018

(warning) Toggle rate of root clock ('%f') is less than the toggle rate of '%s' ('%f').

Description

For a given clock network, the root clock toggle rate can not be less than the toggle rate on the cells through which it propagates. This warning indicates that the toggle rate of a pin connected to the clock network exceeds that of the root clock.

What Next

Check if root clock frequency is set correct or toggle annotation on cell is correct.

PWR-019

(warning) The gate object %s is already mapped to an RTL object.

Description

This warning denotes that there is already one mapping to RTL object is existing for the given gate level object. The existing mapping can be either from direct mapping or from a result of mapping an block instance.

Feedback

What Next

Check for duplication of mapping of same gate level object and keep one that is required for the analysis.

PWR-020

(warning) Assuming pin %s of cell %s represents Q functionality when performing annotation of the cell.

Description

This warning denotes that the unateness of the flop output pin can not be determined automatically from the library description.

What Next

If the pin is QB pin, modify the mapfile, and specify the pin name with the *-inverted* option to apply inverted annotation.

PWR-021

(error) Waveform interval of time-based power analysis is too large.

Description

In time-based power analysis, you set the waveform_interval and the time window with the *set_power_analysis_options -waveform_interval* and *read_vcd -time* commands, respectively. This error occurs when the waveform interval is larger than the time window.

What Next

Check the *set_power_analysis_options* and *read_vcd* commands to ensure that the waveform interval is smaller than the time window.

See Also

- read_vcd
- set_power_analysis_options

PWR-023

(warning) sdpd_tracked cell pin '%s' not annotated .

Feedback

Description

This warning denotes that the vcd has some of the pins missing for critical cells due to which sdpd tracking can not be perfomed on them.

What Next

Use a proper vcd file which has all the pins annotated for critical cells.

See Also

- read_vcd
- set_power_analysis_options

PWR-024

(Warning) option -separate_dyn_and_leak_power_waveform will no longer be supported in PrimePower starting future release.Use option -seperate_power_waveform instead.

Description

Future release, the tool will always use -seperate_power_waveform. If option -separate_dyn_and_leak_power_waveform used, it will be ignored.

What Next

Use option -seperate_power_waveform instead.

PWR-025

(Error) The -rails option of report_threshold_voltage_group command can only be used when the power_enable_multi_rail_analysis variable is set true.

Description

The -rails option of report_threshold_voltage_group command is designed to work when the power_enable_multi_rail_analysis variable is true.

What Next

Turn on the multirail power analysis feature by setting the power_enable_multi_rail_analysis variable to true.

See Also

- report_threshold_voltage_group
- power_enable_multi_rail_analysis

Feedback

PWR-026

(Information) Running cycle based power analysis with %d cores.

Description

PrimePower is running cycle based power analysis with the number of cores indicated in the message.

See Also

- power_enable_cycle_based_power_analysis
- set_host_options
- update_power

PWR-027

(Warning) Running scalar cycle based power analysis since there isn't enough number of available cores on the host.

Description

By default, cycle based power analysis in PrimePower is run with multiple cores on the host. When there is not enough number of available cores, cycle based power analysis will be run in scalar mode. Performance overhead is expected under such a mode.

What Next

Check the availabe resources on the host and run cycle based power analysis with expected number of cores for better performance.

See Also

- power_enable_cycle_based_power_analysis
- set_host_options
- update_power

PWR-028

(Information) Running cycle based power analysis with cycle time %g (ns).

Feedback

Description

PrimePower runs cycle based power analysis with the indicated cycle time. By default, the cycle time is derived from the input activity file (FSDB/VCD). User can also force cycle time by specifying *-waveform_interval* or *-cycle_accurate_clock* and *-cycle_accurate_cycle_count* options with the *set_power_analysis_options* command. Cycle based power analysis generates cycle power reports with specified cycle time.

See Also

- power_enable_cycle_based_power_analysis
- set_power_analysis_options
- update_power

PWR-029

(Warning) The cycle time derived from FSDB/VCD file (%g ns) is different from the cycle accurate clock period (%g ns) of the design.

Description

Cycle based power analysis in PrimePower expects that, by default, the cycle time in FSDB/VCD matches the cycle accurate clock period of the design. The message occurs when they do not match and cycle time derived from FSDB/VCD is used for the analysis.

What Next

Check whether the cycle time from FSDB/VCD is expected for cycle based power analysis or force the cycle time with *-waveform_interval* or *-cycle_accurate_clock* and *-cycle_accurate_cycle_count* options in the *set_power_analysis_options* command.

See Also

- power_enable_cycle_based_power_analysis
- set_power_analysis_options
- update_power

PWR-030

(Warning) Can't derive cycle time from the FSDB/VCD file. Please make sure using RTL or zero delay FSDB/VCD for cycle based power analysis.

Feedback

Description

Cycle based power analysis in PrimePower expects to be used only with RTL or zero delay FSDB/VCD as activity inputs. The message occurs when the FSDB/VCD file is not of such types.

What Next

Check the type of FSDB/VCD file and make sure it's either RTL or zero delay.

See Also

- power_enable_cycle_based_power_analysis
- read_fsdb
- update_power

PWR-031

(Information) Total simulation time = %f (ns).

Description

The message shows the total simulation time interval of cycle based power analysis.

See Also

- power_enable_cycle_based_power_analysis
- update_power

PWR-31

(error) %s is not valid special_function_type userdefined attribute. propagation through synchronizer cell is ignored.

Description

special_function_type userdefined attribute supports following values for, flop: posedge_synchronizer, negedge_synchronizer latch: active_high_sychronizer, active_low_synchronizer

Otherwise, propagation through synchronizer cell is not possible as functionality cannot be properly inferred from library view - marked as black boxes.

What Next

Provide a correct specification special_function_type attribute in .lib file.

Feedback

PWR-032

(Information) Analyze power with annotated timing information.

Description

Run PrimePower cycle based power analysis with annotated timing flow.

See Also

- power_enable_cycle_based_power_analysis
- update_power

PWR-32

(error) special_function_latency %d is not valid value. propagation through synchronizer cell is ignored.

Description

The number of trigger events required to update the output pin value X. (integer number X where generally 1 <= X <= 3)

Otherwise, propagation through synchronizer cell is not possible as functionality cannot be properly inferred from library view - marked as black boxes.

What Next

Provide a correct specification for the userdefined attribute special_function_latency in .lib file.

PWR-033

(Error) Can not open cycle power file "%s" for writing.

Description

There is no write permission for the cycle power file. The cycle power report is not generated for the design or related herarchy.

What Next

Check the write permission of the output file directory and the file. Fix the access permission issue and run PrimePower again.

Feedback

See Also

- power_enable_cycle_based_power_analysis
- set_power_analysis_options
- update_power

PWR-33

(error) The special_function_trigger_pin '%s' is not defined for library cell '%s'. propagation through synchronizer cell is ignored.

Description

special_function_trigger_pin, input pin which triggers logical update for output.

What Next

Provide a correct specification for the userdefined function attributes in the .lib for output pin.

PWR-034

(Error) Can't turn on cycle power with power_enable_advanced_cycle_power_analysis variable in RTL power analysis. Please use power_enable_rtl_advanced_cycle_power_analysis instead.

Description

In RTL power analysis flow, the variable to invoke advanced cycle power analysis is power_enable_rtl_advanced_cycle_power_analysis. When the variable is set to true, PP-RTL-Elite licese will be checked out and cycle power will be invoked in update_power.

What Next

Make sure PP-RTL-Elite license is available. Change power_enable_advanced_cycle_power_analysis to power_enable_rtl_advanced_cycle_power variable and re-run.

See Also

- power_enable_advanced_cycle_power_analysis
- set_power_analysis_options
- update_power

Feedback

PWR-34

(warning) Sampling resolution below 1ps is not supported in Delay shift mode. Resetting sampling interval from %g to %g.

Description

Sampling resolution below 1ps is not supported.

PWR-035

(Information) Taking the period of reference clock

Description

The message indicates that cycle power analysis uses the clock as the reference clock, and its period as the cycle time interval in the analysis. The clock can be specified by user from *set_power_analysis_options -cycle_accurate_clock <clock_name>* or derived from the list of clocks in the design. Usually the fastest clock is picked as default.

See Also

- power_enable_cycle_based_power_analysis
- set_power_analysis_options
- update_power

PWR-036

(Information) Can not derive cycle time from FSDB/VCD clock signals with the power_enable_use_simulation_clock feature.

Description

By *set power_enable_use_simulation_clock true*, cycle power analysis will derive the cycle time interval from the period of clock signals in FSDB/VCD file. This message indicated that the tool can not find valid information from FSDB/VCD in this way. Regular approach will be used to derive cycle time interval.

See Also

- power_enable_cycle_based_power_analysis
- set_power_analysis_options
- update_power

Feedback

PWR-037

(Information) Analysis start/end time adjusted to align with reference clock period.

Description

In time based distributed power analysis where vector partitioning is used, the resultant power waveform might not be smooth if start or end time of analysis is not aligned with reference clock period. Hence, start/end time has been automatically aligned with the reference clock period.

PWR-050

(Warning) No internal power arc found for event at %s pin %s and at time %f.

Description

Not able to find the internal power arc in the library cell for the instance, matching pin states and transitions. PrimePower will consider zero power for missing states/transition.

PWR-051

(Warning) No internal power arc found for %s pin %s, power from these transitions/states will be considered as zero.

Description

Not able to find the internal power arc in the library cell for the instance, matching pin states and transitions. PrimePower will consider zero power for missing states/transition.

PWR-101

(warning) Cannot open %s for write, write to stdout instead.

Description

Failed to open the file for writing. The results will be printed to screen.

What Next

Action based on the message.

PWR-103

(warning) No power will be reported for instance

Feedback

Description

The cell type of the instance at the leaf level is not defined in your HDL code. Power consumption for this particular instance will not be calculated.

What Next

Check your HDL code.

PWR-104

(error) Port %s is not found in cell %s!

Description

The port specified in the delay path is not found in the cell definition.

What Next

Check the Verilog model for the cell.

PWR-119

(error) Cannot open

Description

Not able to open the specified wire cap file for reading.

What Next

Check your read_wire_cap command for the correct file name.

PWR-120

(warning) Cannot read in net name and capacitance value from file %s line %ld. This line is skipped.

Description

Failed to read net name and capacitance value from the wire cap file.

What Next

Check your wire cap file for the correct syntax.

Example of specifying net capacitance in wire cap file: top.inst.u2.Z 0.01 top.inst.u1.u0.Z 0.01

Feedback

PWR-122

(warning) Capacitance of net '%s' is not set.

Description

The net capacitance is not set in the wire cap file. You can also use 'set_wire_load' to set the wire load model, or use 'set_load' to set the load on the net. The default net capacitance is 0.

What Next

Action based on the message.

PWR-123

(error) Cannot open

Description

Not able to open the specified file for reading.

What Next

Check the file name given in the command.

PWR-124

(warning) Capacitance unit '%s' is unrecognizable at line %ld. Use default 'pf'.

Description

The supported net capacitance units are 'pf', 'ff' and 'nf'.

What Next

Check your spf file for the correct capacitance unit.

PWR-134

(error) File "%s" is not in DSPF format which is not supported. Please use DSPF and try again.

Description

The read_spf command reads capacitances from a file only in Standard Parasitic Format form.

Feedback

What Next

Make sure the file is in DSPF format. Refer to read_spf man page.

PWR-135

(Error) Syntax error in DSPF file "%s".

What Next

Make sure the file is in DSPF format. Refer to *read_spf* man page.

PWR-136

(Warning) Name "%s" is too long.

Description

The matching pattern are too long to process. It exceeds the buffer limit - 2048 Bytes.

PWR-137

(error) Current design is not defined.

Description

The current design is not defined. Some commands require that the current design is set.

What Next

Use current_design command to set current design.

PWR-139

(Error) Cannot find %s '%s' in design '%s'

Description

The specified object cannot be found in the given design if the last %s is not given.

PWR-140

(Error) Cannot set current instance to leaf instance '%s'.

Description

The current instance must be a hierarchical instance.

Feedback

PWR-141

(Error) "%s" value must be positive.

PWR-142

(error) The pif design has already been loaded.

Description

The command read_pif has been used to read a pif design prior to the command that caused this error information. Currently, pp_shell can only accommodate one pif design at one time. That is, read_pif command can be used only once.

What Next

If another design is desired, quit and restart pp_shell.

PWR-143

(error) Design is not linked. Cannot continue.

Description

The command or the command with some specific options cannot proceed without linked design.

Note that when we say "Design is not linked", sometimes it is just the library is not read.

What Next

Use link or read_db to read libraries and link the design.

PWR-144

(warning) set_ideal_transition: Net "%s" is not an ideal net. The command on this net is ignored.

Description

set_ideal_transition command only works for ideal nets. If the specified nets are not ideal nets, the command is ignored.

What Next

Use set_ideal_net to specify the nets as ideal nets before using this command.

Feedback

PWR-145

(warning) set_ideal_load: Net "%s" is not an ideal net. The command on this net is ignored.

Description

set_ideal_load command only works for ideal nets. If the specified nets are not ideal nets, the command is ignored.

What Next

Use set_ideal_net to specify the nets as ideal nets before using this command.

PWR-147

(Error) Can't find %s '%s' in %s '%s'.

Description

(internal use)

PWR-148

(error) Can not find cell "%s" in the current design.

Description

There is inconsistency in the design data structure.

What Next

Make sure the pif files are read correctly. Verify the integrity of the pif files, regenerate pif if needed.

PWR-150

(error) There is no design. Check your design.

Description

There is inconsistency in the design data structure.

PWR-151

(warning) There is no port on design "%s".

Feedback

Description

There is inconsistency in the design data structure.

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-152

(error) There is unknown direction on pin "%s" in design "%s".

Description

There is inconsistency in the design data structure.

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-154

(error) Can find design which instantiate cell "%s".

Description

There is inconsistency in the design data structure.

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-155

(warning) There is no net connected to cell "%s".

Description

There is inconsistency in the design data structure.

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

Feedback

PWR-157

(warning) There is no cell connected to net "%s".

Description

There is inconsistency in the design data structure.

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-158

(error) There is mismatch of cell number connected to net "%s".

Description

There is inconsistency in the design data structure.

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-159

(error) Can not find net "%s" in the current design.

Description

There is inconsistency in the design data structure.

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-160

(error) There is no port in the design.

Description

There is inconsistency in the design data structure.

Feedback

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-163

(error) Can't use

Description

It is required that the design be read first in PrimePower.

What Next

Use command 'read_verilog', 'read_vhdl' or 'read_db' to read in the design first.

PWR-164

(error) lack design name in current_design

Description

It is required that a design name must be provided for the current_design command.

What Next

provide the design name with current_design

PWR-165

(error) design

Description

The specified design is not found.

What Next

make sure the design is already read and also check spelling.

PWR-166

(Warning) Please make sure SBPF file contains lumped cap information.

Description

PrimePower currently can only process lumped capacitance. SBPF file, unlike SPEF file, contains either lumped or decoupling capacitance, but not both. If the SBPF file was

Feedback

written by PrimeTime, it most probably does not contain lumped capacitance. PrimePower is able to read the file, but the power result could be inaccurate.

PWR-167

(Warning) No power information at the %s '%s'.

Description

(internal use)

PWR-168

(Warning) No timing window at the pin '%s'.

Description

(internal use)

PWR-169

(Error) Error when reading '%s' from %s.

Description

(internal use)

PWR-170

(Error) Cannot output average waveform because %s

Description

For the given reason, average power waveform cannot be output.

What Next

Make sure

1. the clock is correctly specified; 2. the specified clock is created; 3. the specified clocks are synchronous; 4. PrimeTime license is available; and then try again.

PWR-171

(Warning) No clock specified. %s

Feedback

Description

For the signals for which user has not specified switching activity values, PrimePower internally calculates their values. For switching activity calculation PrimePower uses clock period. Since clock is not specified, PrimePower will use default value.

What Next

Make sure

1. the clock is correctly specified; 2. the specified clock is created; 3. the specified clocks are synchronous; 4. PrimeTime license is available; and then try again.

PWR-172

(error) Failed to check out license for PrimePower.

Description

The application failed to check out the licenses required to enable this product. It may be that all the licenses are in use or the site is not licensed to use this product.

What Next

Make sure that the required feature is in the key file.

Contact your local Synopsys Support Center.

PWR-173

(Error) Synopsys root is not set.

Description

1. if ran through pp_shell: Synopsys root should be set during installation by environment variable $SYNOPSYS or the command path. This indicates a bad installation.
2. if ran through pp_shell_exec: $SYNOPSYS variable or -root_path command line option should be set in order to find installed files.

What Next

1. for case 1 above: Check your installation procedure, contact Synopsys support center if needed.
2. for case 2 above: Please set either $SYNOPSYS environment variable or -root_path command line option to the root of the installed Synopsys software.

Feedback

PWR-174

(error) Can't %s before reading pif files!

Description

It is required that the design be read first in PrimePower.

What Next

Use command 'read_pif' to read in the design first.

PWR-175

(warning) Effort level '%s' is not supported! Command 'set_ana_effort' is ignored.

Description

The valid option for 'set_ana_effort' command is medium or high.

What Next

Use the valid option for 'set_ana_effort'. Type "man set_ana_effort" for more information.

PWR-176

(warning) Effort level '%s' is not supported!

Description

The valid option for 'analyze_power -effort' is 'medium' or 'high'.

What Next

Type "man analyze_power" for more information.

PWR-177

(error) Only a single character among 01*xX can be used for 'set_match_xstate'.

Description

The valid option for 'set_match_xstate' command is '0', '1', 'X', or 'x'.

What Next

Use the valid option for 'set_match_xstate'.

Feedback

PWR-178

(error) Only one single character can be used for hier_sep.

Description

The symbol for hierarchical separator should be one single character.

What Next

Type "man set_hier_sep" for more information.

PWR-179

(error) link_path or link_library variable is not set.

Description

Variable link_path or link_library needs to be set when reading library.

What Next

Type "man link" for more information.

PWR-180

(error) Incorrect time values in -time

Description

The time values specified for 'analyze_power' command cannot be negative.

What Next

Provide the time window period for 'analyze_power' command.

PWR-181

(warning) Net %s does not exist!

Description

The net specified cannot be found in the design.

What Next

Check the port names specified in command 'set_load' and 'set_input_transition'.

Feedback

PWR-182

(warning) Invalid load capacitance unit '%s', use the default 'pf'.

Description

The unit used in the wire cap file is not supported by PrimePower.

What Next

Check your wire cap file.

PWR-183

(warning) Invalid option specified for 'analyze_power -sortby'.

Description

The option specified for '-sortby' is invalid. The valid options are 'power', 'toggle', 'name'.

What Next

Use the valid option for '-sortby' Type "man analyze_power" for more information.

PWR-184

(warning) histogram sampling interval cannot be negative. The -histogram option is ignored.

Description

Histogram sampling interval should be a positive number.

What Next

Provide the correct sampling interval for the -histogram option.

PWR-185

(warning) The digits after the second decimal point of histogram sampling interval will be ignored. Waveform displaying tool may give incorrect results.

Description

The minimum time precision for displaying power histogram is 0.1ns. Using smaller sampling interval than 0.1ns will result in incorrect waveform displayed by waveform tool. Since power histogram is an average power consumption over the period of sampling

Feedback

interval, use sampling interval smaller than 0.1ns can also cause PrimePower to give incorrect histogram power numbers.

What Next

Use sampling interval larger than 0.1ns. If you do think that you need finer resolution for histogram sampling interval, call Synopsys Service Center.

PWR-186

(error) Design label unspecified!

Description

Design needs to be specified for PrimePower run.

What Next

Use command 'read_pif' to specify the design label.

PWR-188

(warning) '%s' is not supported in %s mode. It is ignored.

Description

Each command has its own availability, like read_pif only works for gate mode and read_saif only works for RTL mode. This warning indicates a command used in an inappropriate mode.

Warning: 'read_saif' is not supported in gate mode. It is ignored. (PrimePower-017)

What Next

Look at the AVAILABILITY section in the command's man page.

PWR-189

(warning) '%s' of '%s' is not supported in %s mode. It is ignored.

Description

Each command's option has its own availability, like the "-gate_clock" option in update_power only works in the RTL mode. This warning indicates a command's option used in an inappropriate mode.

Warning: '-gate_clock' of 'update_power' is not supported in gate mode. It is ignored. (PrimePower-018)

Feedback

What Next

Look at the AVAILABILITY section in the command's man page.

PWR-190

(error) Can not find library file "%s".

Description

The library file name given are incorrect or the search path for this library file are not given or the path is not correct.

What Next

Give correct library file name or path name and run again.

PWR-191

(error) The interactive mode is not supported in RTL analysis.

Description

The interactive mode is only supported in gate level analysis.

What Next

Write a shell script for RTL analysis.

PWR-192

(Warning) set_load in the wire_cap file is no longer supported. Instead, make use of the set_load command.

What Next

Use built-in shell command 'source' to read the file.

PWR-193

(Error) Options '%s' and '%s' of command '%s' are mutually exclusive.

Description

The options cannot be specified at the same time.

Feedback

PWR-194

(Error) The %s given for option '%s' is incorrect!

Description

The option has a range of value or some specific values to specify.

What Next

Check the man page of the command for legal values.

PWR-195

(Warning) The given strip_path %s cannot match net name '%s'. Ignored!

Description

PrimePower cannot find the the strip_path specified by the user from the net name given in the parasitics file. It will give up striping off anything from the net name and use the net name as it is to search the net in the design.

What Next

Make sure you give the right strip_path.

PWR-196

(Error) Wire Load Model name must be specified.

Description

When you want to use wire load model for back annotation, make sure you read in the library and give the name of the wire load model.

PWR-197

(Error) Option '%s' must be specified in combination with option '%s'.

PWR-198

(error) Can not find net "%s" in the current design.

Description

There is inconsistency in the design data structure.

Feedback

What Next

Make sure the pif files and the library files are read correctly. Verify the integrity of the pif files, regenerate pif if needed. Verify the integrity of the library files.

PWR-199

(error) Can not find current design.

Description

No designs has been read in the memory.

What Next

Make sure the designs are read correctly. Verify the integrity of the designs.

PWR-200

(error) Command '%s' is obsolete. Use '%s' instead.

Description

Some old commands are obsolete. This message tells you what command to use instead.

What Next

Use the alternative command instead.

PWR-201

(error) There is no interrupted power calculation thread pending.

Description

The resume_power_calculation command can be used only after update_power is interrupted.

What Next

Use the update_power command instead.

PWR-202

(warning) After interruption, something in the environment has changed that may affect the way of power calculation. Use -force option if you still want to resume.

Feedback

Description

If, after power calculation is interrupted, the timing information, parasitics, vcd file, and/or waveform options have changed, and then you type resume_power_calculation, power will not be calculated in the same way as before. Therefore, resuming power calculation is not recommended.

What Next

Use -force option if you still want to resume. Otherwise, do update_power from start.

PWR-203

(Warning) The option 'set_waveform_options -effort high' is ignored because this is not a VCD flow.

Description

The option *-effort* of command *set_waveform_options only works for VCD flow. So for non-VCD flows, the value for this option is ignored.*

PWR-204

(error) The %s command can only be used after power calculation.

Description

Some commands can only be used after the update_power command has been successfully run through.

What Next

Run update_power command first.

PWR-205

(error) Can't annotate power on cell %s.

Description

Power can only be annotated on leaf cell or unresolved cell. The cell you specified is a hierarchical cell and is not an unresolved cell.

What Next

Give the correct cell name.

Feedback

PWR-206

(error) Cannot find current design when running update_power command or analyze_power command.

Description

Failed to get current design netlist from the memory. It is required that the design be read first in PrimePower.

What Next

Use command 'read_pif' to read in the design first.

PWR-207

(error) Negative start time or time interval (start_time >= end_time) in option "-time {%g, %g}" of update_power or analyze_power commands.

Description

Incorrect time window. It is required that the start time be no less than 0 and the end time no less than the start time.

What Next

Give correct time window and try again.

PWR-208

(warning) Invalid option "-sortby %s" in update_power or analyze_power command, option ignored.

Description

Currently, the option "-sortby" is not supported by PrimePower. The option is ignored.

What Next

None.

PWR-209

(warning) Invalid option "-histogram %g" in update_power command or analyze_power command, option ignored.

Feedback

Description

Currently, the option "-histogram" is not supported by PrimePower. The option is ignored.

What Next

None.

PWR-210

(error) Invalid option "-mode %s" in update_power command; option ignored.

Description

The Boolean expression specified by the *-mode* option of the *update_power* command is incorrect.

What Next

Check the Boolean expression for the *-mode* option of the *update_power* command.

See Also

- update_power

PWR-211

(error) Boolean function is too long in -mode option of update_power or analyze_power command.

Description

The string is too long and exceeds the buffer limit - 2048 Bytes.

What Next

Try to make the Boolean function short and run again.

PWR-212

(error) Unknown function operator "%c" in -mode option of update_power command.

Description

The Boolean expression specified by the *-mode* option of the *update_power* command is incorrect.

What Next

Check the Boolean expression for the *-mode* option of the *update_power* command.

See Also

- update_power

PWR-213

(error) Invalid -time option in the update_power command.

Description

Incorrect time window given.

What Next

Check the *-time* option of the *update_power* command.

See Also

- update_power

PWR-214

(error) Lack the VCD file name

Description

The VCD file name in report_vcd_hierarchy is missed.

What Next

Add the VCD file name or issue read_vcd before report_vcd_hierarchy.

PWR-215

(error) No rail name is specified for command set_current_rail. Please refer to command usage for more information.

Description

Design power rail name must be specified for command set_current_rail.

What Next

Type 'man set_current_rail' for more information

Feedback

PWR-216

(error) Power rail Verify the design rail name.

Description

Power rails in the design are defined by command create_power_rail_mapping. Then the defined design rail can be used in set_current_rail command to select the rail of interest. To list all the defined power rails, use command report_power_rail_mapping.

What Next

Check the power rail defined in the design and make sure that the name is spelled correctly.

See Also

- create_power_rail_mapping
- report_power_rail_mapping

PWR-217

(error) Design power rail name must be specified for command create_power_rail_mapping. Please refer to command usage for more information.

Description

Design power rail name must be specified for command create_power_rail_mapping.

What Next

Type 'man create_power_rail_mapping' for more information

PWR-218

(warning) Power rail Please verify the library rail name.

Description

The specific library rail name is not defined in the technology libraries which are linked with the design.

What Next

Check the rail names defined in the technology libraries and make sure that the name is spelled correctly.

Feedback

PWR-219

(error) There is no design power rail defined in this design. This command is ignored. Use command create_power_rail_mapping to define design power rails.

Description

Power rails in the design are defined by command create_power_rail_mapping. Then the defined design rail can be used in set_current_rail command to select the rail of interest. To list all the defined power rails, use command report_power_rail_mapping.

What Next

Type 'man create_power_rail_mapping' for more information

PWR-220

(error) There is only one design power rail defined in this design. Command set_current_rail has no effect on single rail design. This command is ignored. Use command create_power_rail_mapping to define design power rails.

Description

Power rails in the design are defined by command create_power_rail_mapping. Then the defined design rail can be used in set_current_rail command to select the rail of interest. To list all the defined power rails, use command report_power_rail_mapping.

What Next

Type 'man create_power_rail_mapping' for more information

PWR-221

(error) Internal error: library power rail for cell %s (%s). Please contact Synopsys Customer Support Center.

Description

An internal rare error has occurred. This cell is supplied by multi-voltages, but the specific power rail is not found in its definition from the technology library.

What Next

Contact Synopsys Customer Support Center.

PWR-222

(Information) Different library rails are mapped to the same design rail for cell

Feedback

Description

Different library power rails can be mapped to different design power rails at instance basis in PrimePower. Command *create_power_rail_mapping* can be used to define the design power rails and create such rail mapping.

PWR-223

(error) Can not find net

Description

The net name used in the Boolean expression for -off_condition option is not defined in the current design.

What Next

Check the Boolean expression for -off_condition option in command create_power_rail_mapping.

PWR-224

(error) Invalid specification in the -off_condition %s option of the create_power_rail_mapping command.

Description

The the -off_condition option does not specify a valid Boolean expression.

What Next

Check the Boolean expression for the -off_condition option of the create_power_rail_mapping command.

See Also

- create_power_rail_mapping

PWR-225

(error) Boolean function is too long in -off_condition option of command create_power_rail_mapping. The maximum acceptable number of characters is %d.

Description

The length limit for the Boolean expression is currently set to be 2048 characters.

Feedback

What Next

Check the Boolean expression for -off_condition option in command create_power_rail_mapping. Please contact Synopsys Customer Support Center if needed.

PWR-226

(error) Unknown function operator create_power_rail_mapping.

Description

The operator used in the Boolean expression for -off_condition option is not support. The supported operators list is: (,), !, +, *, &, |, ^, '.

What Next

Check the Boolean expression for -off_condition option in command create_power_rail_mapping.

PWR-227

(warning) The state probability of net is not set. Set to be 0.5.

Description

An internal error has occurred. The state probability of nets should have been set before power calculation starts in the PrimePower SAIF-based flow.

What Next

Contact the Synopsys Customer Support Center.

PWR-228

(warning) The state probability of net is %.3f, which is not allowed. Set to be 1.0.

Description

An internal rare error has occurred. The state probability of a net cannot exceed 1.0.

What Next

Contact Synopsys Customer Support Center.

PWR-229

(warning) No rail specific power table is defined for library cell

Feedback

Description

"related_pg_pin" or "power_level" (old syntax name) attribute can be specified in internal and leakage power tables to indicate power consumptions associated with different power rails in a cell. This enables PrimePower to report power consumption at rail basis.

What Next

Provide more accurate power characterization data in the library.

PWR-230

(warning) Rail specific power tables are not fully defined for library cell

Description

"related_pg_pin or "power_level" (old syntax name) attribute can be used in internal and leakage power tables to indicate power consumptions associated with different power rails in a cell. This enables PrimePower to report power consumption at rail basis. The number of rail specific power tables should match the number of power rails defined for the cell in the library.

What Next

Check power tables in the library

PWR-231

(warning) Rail specific power tables are over specified for library cell

Description

"related_pg_pin or "power_level" (old syntax name) attribute can be used in internal and leakage power tables to indicate power consumptions associated with different power rails in a cell. This enables PrimePower to report power consumption at rail basis. The number of rail specific power tables should match the number of power rails defined for the cell in the library.

What Next

Check power tables in the library

PWR-232

(error) Can not open file "%s" for reading.

Feedback

Description

The file can not be open for reading.

What Next

Check if the correct name mapping file is provided.

PWR-233

(error) Gate level object Therefore, will not be able to set mapping between RTL and gate level objects.

Description

Gate level object can not be found in the netlist. Without gate level object the command will not know one of the mapping parameter between RTL object and gate level object.

What Next

Please check if correct gate level object name is provided.

PWR-234

(Warning) %s time of the analysis window {%g %g} is %s than the %s event time (%g). Discarding this analysis window

---

PWR-235

(Warning) %s time of the analysis window {%g %g} is %s than the %s event time (%g). Resetting the %s time of the analysis window to (%g)

PWR-237

(error) Can't find user specified block in the design; check your $gen_pif task.

Description

Not able to find the instances specified by $gen_pif task in the design.

What Next

Verify that the instances specified by $gen_pif task exist.

Feedback

PWR-238

(Error) Analyze window (%g, %g) mismatches with the simulation activity window (%g, %g).

Description

The analyze window specified by '*analyze_power -time*' option mismatches with the simulation window captured by $gen_pif task. Mismatched window will cause incorrect power simulation results.

What Next

1. Check your $gen_pif task for pif generation 2. Choose the time window within the simulation time window.

PWR-239

(warning) Analyze window (%g, %g) starts earlier than the simulation activity window (%g, %g).

Description

The analyze window specified by 'analyze_power -time' option mismatches with the simulation window captured by $gen_pif task. Mismatched window will cause incorrect power simulation results.

What Next

1. Check your $gen_pif task for pif generation.
2. Choose the time window within the simulation time window.

PWR-240

(Warning) Analyze window (%g, %g) finishes later than the simulation activity window (%g, %g).

Description

The analyze window specified by '*analyze_power -time*' option mismatches with the simulation window captured by $gen_pif task. Mismatched window will cause incorrect power simulation results.

What Next

1. Check your $gen_pif task for pif generation 2. Choose the time window within the simulation time window.

Feedback

PWR-241

(error) Unknown port direction!

Description

The port direction in the cell is unknown. The supported port direction types are: input, output and inout.

What Next

Report this error to Synopsys Customer Service Center.

PWR-242

(Warning) Power simulation has been interrupted!

Description

If a user presses Ctrl-C in the middle of PrimePower run, power simulation will be interrupted. pp_shell will do a wrap-up and report the simulation results up to this point.

PWR-243

(warning) Window [%g, %g] negative or too narrow to be simulated!

Description

The analyze window specified by 'analyze_power -time' option gives too little the room to run simulation.

What Next

Choose a more reasonable time window in 'analyze_power' command..

PWR-244

(Warning) Analyze window has been adjusted to be (%g, %g).

Description

The analyze window specified by '*analyze_power -time*' option mismatches with the simulation window captured by $gen_pif task. This analyze window has been adjusted according to the simulation window to give more accurate power results.

Feedback

What Next

1. Check your $gen_pif task for pif generation 2. Choose the analyze time window within the simulation time window.

PWR-245

(warning) User specified switching activity information present on the design. However, using event based flow for power estimation as -saif switch is not used with the command.

Description

Both event file and user specified switching activity information is present on the design. However, since -saif switch is not used with the command, by default the command will use event based flow for power estimation.

What Next

Check if you are using wright flow for power estimation.

PWR-246

(Warning) Neither event file or switching activity data present for power estimation. The command will propagate switching activity values for power calculation.

Description

Since, neither event file or switching activity data is present on the design, the command will propagate switching activity values for power calculation.

PWR-247

(warning) Event end time %g is less than analysis start time %g

Description

event end time in VCD is less than the analysis start time. The VCD file doesn't your analysis window.

What Next

your test bench to make sure your simulation is run long enough.

your PrimePower run script to make sure you specify the correct "-time" values update_power.

Feedback

PWR-248

(error) Can not find any event in the event file.

Description

An event happens when the value at any net or pin changes. From the VCD file given, no event can be found.

What Next

Check -strip_path and -path in read_vcd to make sure correct paths are specified.

Check testbench and make sure to dump every leaf cell's events. For example, use $dumpvar(0).

PWR-249

(Warning) End time of the analysis window {%g %g} is earlier than the first event time (%g)

PWR-250

(Warning) Start time of the analysis window {%g %g} is earlier than the first event time (%g).

PWR-251

(error) No design has been specified for power analysis.

Description

Failed to get current design netlist from the memory. It is required that the design be read first in PrimePower.

What Next

Use command 'read_pif' to read in the design first.

PWR-252

(Warning) Power simulation has been interrupted.

PWR-253

(Warning) End time of the analysis window {%g, %g} is later than the last event time (%g).

Feedback

PWR-254

(error) Invalid direction on lib_pin "%s" in lib_cell "%s".

Description

Normally the direction attribute of a lib_pin has one of three values: in, out, inout. This error happens when the real value is none of these.

What Next

Check the library file.

PWR-255

(error) No activity is available in the VCD file for the given time interval for power calculation.

Description

Incorrect time window. The times specified must include VCD activity.

What Next

Check the VCD file to make sure that activity is dumped during the time window specified. Give the correct time window and try again.

PWR-256

(warning) There is no waveform options specified for update_power -waveform command. Use the default waveform options.

Description

When using update_power -waveform, set_waveform_options should be used before to specify the waveform options. Otherwise, use the default waveform options.

What Next

Refer to set_waveform_options and update_power man pages.

PWR-258

(error) (read_vcd) Cannot open file

Description

Not able to open the specified VCD file for reading.

Feedback

What Next

Check your read_vcd command for the correct file_name.

PWR-259

(error) (read_vcd) Unknown time unit.

Description

The time unit given is not recognizable.

What Next

Check your VCD file.

PWR-260

(error) (read_vcd) Can not find cell

Description

The cell read from vcd file cannot be found in the specified design.

What Next

Make sure the VCD file is created correctly, and the path and strip_path option are given appropriately.

PWR-261

(error) (read_vcd) Can not find the top cell in design

Description

The top cell read from vcd file cannot be found in the specified design.

What Next

Make sure the VCD file is created correctly, and the path and strip_path option are given appropriately.

PWR-262

(Error) (read_vcd) Syntax error. $scope and $upscope are not in pair. Ignoring the extra $upscope.

Feedback

What Next

Check the VCD file.

PWR-263

(warning) (read_vcd) Can not find net or port in cell

Description

The net or port of a certain cell read from the VCD file can not be found in the same cell of the design loaded in pp_shell.

What Next

Make sure the VCD file is created correctly, and the path and strip_path option are given appropriately.

PWR-264

(warning) (read_vcd) Variable length %d of identifier %s does not match the length of the vector %d.

Description

The variable length of the identifier does not match the length of the vector.

What Next

Check the VCD file.

PWR-265

(error) (read_vcd) Strip path matched in the VCD file.

Description

PrimePower cannot find the the strip_path specified by the user from the net name given in the VCD file. It will give up reading anything from the VCD file for this net.

What Next

Make sure you give the right strip_path.

PWR-266

(error) read_vcd command is not used in the PrimePower VCD flow.

Feedback

Description

PrimePower has VCD flow. In the VCD flow, PrimePower reads in the HDL netlist and VCD files. This error occurs when VCD file is not read in the VCD flow.

What Next

Please read in VCD file using read_vcd command before update_power.

PWR-267

(warning) The net

Description

The signal changes for the reported net is not recorded in the VCD file. This will lead power calculation inaccurate. Most likely the power number is less than it should be.

What Next

Please check $dumpvars in Verilog testbench to make sure all nets are dumped.

PWR-268

(error) Wrong input Valid inputs are "low" or "high".

Description

The option -effort accepts two variables of values "low" and "high". The "high" value is given if the user wants to use the new algorithm, which is cpu and memory intensive, for waveform generation. The "low" value is given if the user wants to use the old algorithm for waveform generation.

What Next

Please choose the correct variable value to the option and run the command again.

PWR-269

(error) Cannot turn on power analysis when variation analysis is on

Description

Power analysis and variation analysis are currently mutually exclusive. Power analysis cannot be enabled while variation analysis is on.

What Next

Turn off variation analysis first then turn on power analysis.

Feedback

PWR-270

(error) Power analysis license is not available.

Description

You received this error message because you do not have an available PrimePower or PrimePower license.

What Next

Make sure that you have an available PrimePower or PrimePower license.

PWR-271

(error) Can't create power group '%s' because of name conflict.

Description

Power group cannot be created because the name of the power group to be created is conflicting to an existing power group.

What Next

Try another group name.

PWR-272

(error) There is no predefined power group called '%s'.

Description

Only predefined power groups have default list of cells. The specified power group is not a predefined power group.

What Next

Use correct predefined power group name or create your own power group.

PWR-273

(error) Power group '%s' does not exist.

Description

There is no power group with the specified name. If the name is a predefined power group, it must have been removed.

Feedback

What Next

Make sure to give the correct name.

PWR-274

(Information) Average waveform period is %f ns.

Description

The average waveform period is the common base period of all clocks specified to generate the average waveform.

PWR-275

(error) Cannot generate average waveform because its period is too large.

Description

The average waveform period is the common base period of all clocks specified to generate the average waveform. You are receiving this message because the common base period of the specified clocks is too large. Most probably the clocks are not synced with one another very well. Generating a waveform for such a large period could be a waste of run time and memory.

To solve the problem, you should split the specified clocks into different groups, with clocks in each group syncing up very well with each other, and then generate waveforms for each group.

If you really want to generate average waveforms for such a large period, change the value of the *power_average_waveform_limit* variable.

What Next

Specify clocks again or change the value of power_average_waveform_limit.

PWR-276

(error) Clock network power has not been estimated.

Description

You are trying to include estimated clock network power in the power report, but the clock network power has not been estimated yet.

What Next

Try estimate_clock_network_power before report_power.

Feedback

PWR-277

(error) Missing the closing bracket in power off expression

Description

Missing the closing bracket in the Boolean expression for the -off_condition option of the create_power_rail_mapping command.

What Next

Check the Boolean expression specified by the -off_condition option of the create_power_rail_mapping command.

See Also

- create_power_rail_mapping

PWR-278

(warning) The hierarchical cell '%s' is an empty cell

Description

The reported cell is a hierarchical cell but without any instances in its manager reference design. It will be considered as a black box during power calculation.

What Next

Check the netlist to make sure that's correct. Make sure VCD, SAIF or set_switching_activity cover the output pins of the reported cell, otherwise the tool will set the default switching activity for them.

PWR-279

(error) Can't find reference clock for cycle accurate peak power analysis in current design.

Description

This message indicates that PrimePower can not find the reference clock for cycle accurate peak power analysis. Cycle accurate peak power analysis needs a reference clock to determine the cycle period or multiples of the cycle period over which the power values are averaged. The reference clock name can be specified by the *-cycle_accurate_clock* option in *set_power_analysis_options* command. If the option is not used, the tool will try to find a reference clock automatically. If no clock can be found, the *update_power* command will stop with this error message.

Feedback

What Next

Check whether the current design has any related clocks.

PWR-280

(information) Clock %s is selected as the reference clock for cycle accurate peak power analysis of the current design.

Description

This message indicates that PrimePower will use this clock as the reference clock for cycle accurate peak power analysis.

What Next

None.

PWR-281

(error) Can't use -interval option for cycle accurate peak power analysis.

Description

This message indicates that *-interval* option is used with *-cycle_accurate* option in the *create_power_waveforms* command. Please use *-cycle_accurate_clock* and *-cycle_accurate_cycle_count* to determine the sampling interval for cycle accurate peak power instead.

What Next

Use *-cycle_accurate_clock* and *-cycle_accurate_cycle_count* to specify the sampling interval.

PWR-282

(error) Can't use -clocks option for cycle accurate peak power analysis.

Description

This message indicates that *-clocks* option is used with the *-cycle_accurate* option in the *create_power_waveforms* command. Please use *-cycle_accurate_clock* to specify the reference clock instead.

What Next

Use *-cycle_accurate_clock* to specify the reference clock.

Feedback

PWR-283

(error) Can't use -cycle_accurate_cycle_count option without -cycle_accurate option in create_power_waveform command.

Description

This message indicates that *-cycle_accurate_cycle_count* option is used in the *create_power_waveforms* command, but *-cycle_accurate* option is not specified. The *-cycle_accurate_cycle_count* option is only allowed for cycle accurate peak power analysis. Please use the *-cycle_accurate* option in the *create_power_waveforms* command to turn on the cycle accurate peak power analysis.

What Next

Use *-cycle_accurate* option along with *-cycle_accurate_cycle_count* option in the *create_power_waveforms* command.

PWR-284

(error) Can't use -cycle_accurate_clock option without -cycle_accurate option in the create_power_waveform command.

Description

This message indicates that the *-cycle_accurate_clock* option is used in the *create_power_waveforms* command, but the *-cycle_accurate* option is not specified. The *-cycle_accurate_clock* option is only allowed for cycle accurate peak power analysis. Please use the *-cycle_accurate* option in *create_power_waveforms* to turn on the cycle accurate peak power analysis.

What Next

Use *-cycle_accurate* option along with *-cycle_accurate_clock* option in *create_power_waveforms*.

PWR-285

(warning) The value of -interval in create_power_waveforms is not correct.

Description

This message indicates that the value of -interval option in create_power_waveforms is not correct. This can happen when you use a zero delay VCD (read_vcd -zero_delay) and you either don't set -interval or set the value of -interval is too small. For a zero delay VCD, you need to set the interval value greater than a fast clock period since the power analysis for the zero delay VCD can only give a cycle accurate result.

Feedback

What Next

Set a correct interval value. Otherwise, the tool will set/reset the interval value. You can check power report to make sure the value set by the tool is what you expect.

PWR-286

(error) The cycle accurate power analysis cannot be used in vector free or SAIF based flow.

Description

The cycle accurate power analysis can only be used in VCD based flow. It cannot be used in vector free or SAIF based flow.

What Next

Remove -cycle_accurate option from create_power_waveforms command.

PWR-287

(error) Can't find any cell in the transient fanout of the specified sources.

Description

This message indicates *report_power -from* failed to find any cell in the transient fanout cone of the specified sources. The sources specified with *-from* option of *report_power* command need to be valid cell, net, pin or port objects. If the *-groups* option is also specified, the source object should be in the power groups.

What Next

Check whether the specified sources are valid. If not, fix it and run the command again.

PWR-288

(error) The _FANOUT_TREE_ power group exists.

Description

_FANOUT_TREE_ power group is reserved for the feature of *report_power -from*. If the power group was already created by user, there will be conflicts.

What Next

Remove or rename the user defined _FANOUT_TREE_ power group and run the command again.

Feedback

PWR-289

(error) Can't find main library for the design.

Description

The error happens when there is no cell in the design which can find the corresponding library cell. This is usually caused by incorrect link_library paths or invalid technology libraries.

What Next

Check whether link_path is correct and technology libraries are correctly loaded and re-run the case.

PWR-290

(error) Power value is required for 'set_annotated_clock_network_power' command.

Description

The error happens when *set_annotated_clock_network_power* command did not specify any power value, neither the default power value nor the power values specified by *-switching*, *-internal* or *-leakage* options. The command needs to accept at least one power value.

What Next

Add power value(s) to the command and re-run the case.

PWR-291

(error) Can't find clock '%s' in current design.

Description

The error happens when *set/remove_annotated_clock_network_power* command specified the clock with the *-clock* option. But the clock with this name cannot be found in the current design.

What Next

Check the clock name in SDC, correct it and re-run the case.

PWR-292

(warning) Power has already been annotated on the whole clock network. Ignore clock based power annotation.

Feedback

Description

The warning happens when *set_annotated_clock_network_power* command has already annotated the power on the whole clock network. Clock based annotation with *-clock* will be ignored under such a circumstance.

What Next

If you would like to do clock based power annotation, use *remove_annotated_clock_network_power* on the design first.

PWR-293

(error) No power has been annotated on the clock network.

Description

The error happens when *remove_annotated_clock_network_power* command can not find any annotated clock network power on the design.

What Next

Remove the command from in the context of the script.

PWR-294

(error) No power has been annotated on the clock network for clock '%s'.

Description

The error happens when *remove_annotated_clock_network_power* command can not find any annotated clock network power for the clock specified by the *-clock* option.

What Next

If you would like to remove all the annotated clock power, use *remove_annotated_clock_network_power* without *-clock* option.

PWR-295

(warning) Annotated clock network power exists. Ignore estimated clock network power.

Description

Annotated clock network power has higher priority than the estimated clock network power. If both are activated in the *report_power* command. The estimated clock network power will be ignored.

Feedback

What Next

Use either annotated or estimated clock network power, not both.

PWR-296

(error) Group based power reports must contain 'clock_network' group when annotated clock network power is used.

Description

When power is annotated for the clock network, *report_power -group groups* command must contain the 'clock_network' group.

What Next

If you don't want to report power with annotated clock network power, use *remove_annotated_clock_network_power* command before the *report power* command.

PWR-297

(warning) '%s' has already been annotated on the clock network. Override it.

Description

If the power has already been annotated on the clock network, the succeeding commands will override it. The overriding behavior only happens on switching, internal and leakage power separately. Default power is treated as internal power.

What Next

Check whether the command overriding is intended and fix them if it's not.

PWR-298

(error) Clock based power reports are not allowed when there is annotated power on the whole clock network.

Description

The error happens when there is annotated power on the whole clock network but *report_power* has the *-clocks* option. In this situation, there is no power information for each clock domain of the clock network. So PrimePower cannot generate a valid report.

What Next

Use *remove_annotated_clock_network_power* to remove the annotated clock network power. Then, use *set_annotated_clock_network_power -clock clk_name* to annotate clock

Feedback

based power on clock network, or remove *-clocks* option from *report_power* and re-run the case.

PWR-299

(error) Only one clock object is allowed for the '-clock' option.

Description

set/remove_annotated_clock_network_power command only allows to specify one clock domain. The error happens when more than one clock objects are specified with *-clock* option for the command.

What Next

If annotated clock network power is needed for more than one clock domains, use multiple *set/remove_annotated_clock_network_power* commands.

PWR-300

(warning) Cell '%s(%s)' drives %d loads.

Description

The warning occurs when the cell drives a large fanout. An example is, a clock gating cell drives a large number of sequential cells before the clock network is implemented. The large fanout can affect the power calculation. Event based power analysis will do some special handling for the large fanout drivers and their loads.

What Next

Set the high fanout nets as ideal nets, or let PrimePower handle them.

PWR-301

(warning) %d high fanout drivers are detected. Power analysis may be affected by high fanout drivers.

Description

The warning gives the number of high fanout drivers in the design. Event based power analysis in PrimePower will do some special handling for large fanout drivers and their loads.

What Next

Set the high fanout nets as ideal nets, or let PrimePower handle them.

Feedback

PWR-302

(warning) Inout port %s of library cell %s has neither functionality nor state and path dependent power table. Assume that it is an input.

Description

PrimePower relies on the three-state enable function of the cell or the when state of power tables to decide whether an inout pin works as an input or output. This warning indicates that both functionality and when state of power tables are missing. In this case, PrimePower assumes that the inout pin works as an input.

What Next

To model the behavior and power more accurately, specify the functionality, or generate state and path dependent power tables for the cell, and run PrimePower again.

PWR-303

(warning) switching activity at %s is reset due to multi driver net consolidation

Description

The specified pin or net is a multi driver net. You may specify switching activity on some pins or the net. During update_power, the tool will consolidate all of them and reset them properly. This warning gives you a hint that the switching activity you specify at the specified pin or net is ignored and the tool is reset it according to its consolidation rules.

What Next

Use get_switching_activity command to check if the switching activity is correct.

PWR-304

(error) -relative_toggle_rate option can only be use when -net_power option used.

Description

The error message indicated that the option -relative_toggle_rate of *report_power* was not supposed.

What Next

Use *-net_power* and *-relative_toggle_rate* option.

Feedback

PWR-309

(Error) Leakage probability data is not provided by user, default probability 0 will be used for power calculation.

Description

Leakage probability data should be provided by user.

What Next

Please provide leakage probability data.

PWR-310

(warning) No edge information found for cell %s in edge property side files.

Description

No edge information found for a cell in edge property side files during context leakage calculation.

What Next

Provide edge information to each cell in edge property side files.

PWR-311

(warning) Unable to find context leakage for operating condition %s.

Description

Unable to find context leakage for operating condition.

What Next

Provide context leakage for operating condition.

PWR-312

(Error) Edge side file %s is empty. Please provide non-empty file in command 'read_context_leakage_data'.

Description

Edge side file should be non empty.

Feedback

What Next

Please provide non-empty Edge side file in command 'read_context_leakage_data'.

PWR-313

(Error) Boundary leakage file %s is empty. Please provide non-empty file in command 'read_context_leakage_data'.

Description

Boundary leakage file should be non empty.

What Next

Please provide non-empty file in command 'read_context_leakage_data'.

PWR-314

(warning) Empty spaces detected in cell rows. Please refer to %s for more details.

Description

Empty spaces detected in cell rows, this could impact boundary leakage power calculation.

What Next

Please remove empty spaces from cell rows to minimize impact to boundary leakage power calculation.

PWR-315

(warning) The design is not fully legalized. Please refer to %s for more details.

Description

Design is not fully legalized and has cell(s) which doesn't fit vertically in cell row(s), this could impact boundary leakage power calculation.

What Next

Please make the design fully legalized to minimize impact to boundary leakage power calculation.

Feedback

PWR-316

(information) Legality check for design is complete and the design is ready for boundary leakage analysis.

Description

The design has no cell which does not fit vertically in the cell row(s) and also there are no empty spaces present in the design.

What Next

The design is fully legalized with respect to empty spaces and perfect vertical alignment of cells in the cell rows. Nothing to be done.

PWR-317

(warning) The design is not fully legalized. Please refer to %s for more details.

Description

Design is not fully legalized and has cell(s) overlap, this could impact boundary leakage power calculation.

What Next

Please make the design fully legalized to minimize impact to boundary leakage power calculation.

PWR-318

(warning) Could not find netlist instance for libcell %s at coordinates (xl: %s, yb: %s).

Description

Could not find netlist instance for library cell during CNOD leakage power calculation.

What Next

Check if linking of design was properly done.

PWR-319

(warning) No leakage derate data present for library '%s'.

Description

Leakage derate data not present for the specified library.

Feedback

What Next

Provide necessary leakage derate data for the library.

PWR-320

(warning) No leakage derate data present for cell '%s' with libcell '%s'.

Description

Leakage derate data not present for the specified cell.

What Next

Provide the necessary leakage derate data for the cell.

PWR-321

(Error) %s is invalid for %s in the Thermal Profile because of %s.

Description

The shell encounters an error when loading the Thermal Profile.

What Next

Please check the data of the Thermal Profile.

PWR-322

(Error) Thermal Profile already exists.

Description

There is already a Thermal Profile in the memory.

What Next

Please use remove_thermal_profile before loading another Thermal Profile.

PWR-330

(Error) Maximum number of discrete intervals allowed for concurrent power analysis is %d. Please trigger scalar run.

Feedback

Description

This error is shown when the number of discrete intervals specified with -time option in read_fsdb exceeds the maximum supported discrete intervals for concurrent power analysis.

What Next

Reduce the number of discrete intervals specified with -time option in read_fsdb or trigger a scalar run.

PWR-331

(Error) Set max_process greater than or equal to %d to run concurrent power analysis for discrete intervals or trigger scalar run.

Description

This error is shown when the number of max_process specified is lesser than the number of discrete intervals specified with -time option in read_fsdb.

What Next

Set max_process greater than or equal to number of discrete intevals mentioned; or reduce the number of discrete intervals specified to less than or equal to max_process; or trigger a scalar run.

PWR-340

(Warning) Negative value of %s is found at line no. %d.

Description

Negative values of TC, GC, TG, IG, T1, T0, TX are not expected in SAIF.

What Next

Please check if SAIF has been generated correctly.

PWR-402

(error) Clock is not defined

Description

extract_model -power will attach power tables to clock pins. So at least one clock must be defined.

Feedback

What Next

Use create_clock or create_generated_clock to define clock(s).

PWR-403

(error) Should set either period or ratio in set_simulation_clock.

Description

You should set either period or ratio in set_simulation_clock to a value greater than or equal to 0.

What Next

Ensure that you specify -period or -ratio for set_simulation_clock.

PWR-404

(error) Cannot set both period or ratio in set_simulation_clock

Description

In set_simulation_clock, you can either specify -period or -ratio. You cannot specify both.

What Next

Check your set_simulation_clock and make sure you only specify either -period or -ratio.

PWR-405

(error) Cannot specify period without clock in set_simulation_clock

Description

In set_simulation_clock command, you cannot specify -period without clock. Without clock you can only specify -ratio which is a global scaling ratio for all clocks.

What Next

Check your set_simulation_clock command.

PWR-406

(warning) The net %s has no base clock for power calculation.

Feedback

Description

For vector free power analysis and clock scaling, PrimePower uses the base clock to set and/or scale switching activity. This message indicates the reported net has no base clock. So the tool will use the fastest clock in the design.

What Next

Use check_power's no_base_clock to check your design. You can also use set_switching_activity to directly set the switching activity.

PWR-407

(error) (read_vcd) Syntax error: unprintable ASCII char in identifier code at line %d

Description

In VCD, the $var statement syntax is

$var var_type size identifier_code reference $end

This error indicates there is an unprintable ASCII character in identifier_code.

What Next

Check the VCD file.

PWR-408

(warning) toggle rate '%f' is larger than the fastest clock toggle rate '%f' on net (or pin) '%s'.

Description

The message occurs when the user set toggle rate from set_switching_activity command is larger than the fastest clock toggle rate. Such a toggle rate can not be properly propagated by the switching activity propagation.

What Next

By default, the toggle rate (or count) value from set_switching_activity command is per 1ns. When a clock or period is specified, the value will be per each clock period.

Check toggle rate (or count) value from set_switching_activity command and make sure the value is correct.

PWR-409

(warning) value provided to option %s is invalid, Ignoring check for this option.

Feedback

Description

Non-zero positive value need to be provided to above option.

What Next

Please provide non-zero positive value to above option.

PWR-410

(warning) -max_fanout/-max_slew/-max_cap/-max_delay can not be specified with object list, ignoring object list for these options.

Description

Checks for above options are performed only on the design.

What Next

Please use above options only for design.

PWR-501

(error) Power rail mapping commands and options can not be combined with power domain commands.

Description

Power domains can define the power intention for a multivoltage design. The power rail mapping commands and options can be replaced by power domain Tcl commands. Combining power rail mapping commands and options with power domain commands is not allowed.

What Next

For more information about power domain commands, see the man page for create_power_domain.

See Also

- create_power_domain

PWR-502

(Warning) The library cell '%s' does not have 'primary_power' or 'primary_ground' defined in the library.

Feedback

Description

It is required to have 'primary_power' and 'primary_ground' defined in the PG pin library.

PWR-503

(error) The legacy power rail mapping commands and options cannot be launched by default. Set the

Description

UPF is an industrial standard for specifying power design intent as an extension to logic specification. The legacy power rail mapping commands and options will continue to be supported. However, combining power rail mapping commands and options with UPF commands is not allowed.

What Next

For more information about UPF commands, see the man page for create_power_domain.

See Also

- create_power_domain

PWR-504

(error) The domain based power reporting cannot be launched in non-UPF mode. To enable UPF mode, apply UPF commands to the design, and set the power_domains_compatibility variable to false.

Description

UPF is an industrial standard for specifying power design intent as an extension to logic specification. The domain based power reporting is designed to be used in UPF mode.

What Next

For more information about UPF commands, see the man page for create_power_domain.

See Also

- create_power_domain

PWR-505

(warning) There are invalid value changes in the activity (VCD/VPD/FSDB) file.

Feedback

Description

The warning message indicates that PrimePower detects abnormal value change data in the VCD/VPD/FSDB file used for time based power analysis. PrimeTime PX stops after it detects more than 100 invalid value changes.

What Next

Check the activity (VCD/VPD/FSDB) data to make sure there is no error.

PWR-506

(error) Can't run power replay flow in PrimePower. Environment variable %s is not set.

Description

When the variable power_enable_power_relay is set to true, PrimePower enters the power replay mode. This mode requires the products of powrep, vcs and verdi to be installed and available.

What Next

Please install the correponding products or disable the power replay flow.

PWR-507

(error) Can't find %s executable, or %s executable does not have x permission.

Description

When the variable power_enable_power_relay is set to true, PrimePower enters the power replay mode. This mode requires the products of powrep, vcs and verdi to be installed and available.

What Next

Please check whether the executable of the product is available.

PWR-508

(information) Running

Description

In power replay mode, PrimePower wraps around "powrep" to perform expected activities. This message prints out the powrep command line in debug mode.

Feedback

What Next

Please check the powrep command line to make sure all options are intended.

PWR-509

(error) Internal command

Description

In power replay mode, PrimePower wraps around "powrep" to perform expected activities. The message indicated the execution of underline powrep command failed due to improper settings or configuation.

What Next

Please fix the related relay options from set_power_replay_options command and rerun.

PWR-510

(error) Can't find %s. Command %s failed.

Description

The message indicated that the required information was not available in power replay mode and the correponding command failed.

What Next

Please check and fix the configuation of power replay and rerun.

PWR-511

(information) %s %s to replay activities.

Description

The message indicates that the major process is started/ended in the replay_activity command.

What Next

Information only.

PWR-512

(error) Can't run command

Feedback

Description

PrimePower power replay flow checks out PP-Elite license when variable *power_enable_power_replay* is set to true. This command is to be used in the PrimePower power replay mode. It can not be run without PP-Elite license.

What Next

Turn on the power replay mode with *set power_enable_power_replay true* at the start of the script and run the case again.

PWR-513

(error) Power replay analysis is not enabled. Please set power_enable_power_replay true to invoke power replay flow.

Description

This command can only be run in PrimePower power replay mode. PrimePower power replay mode is enabled when variable *power_enable_power_replay* is set to true.

What Next

Turn on the power replay mode with *set power_enable_power_replay true* at the start of the script and run the case again.

PWR-514

(error) Can't create %s directory

Description

This message indicates that the tool is not able to create the directory for power replay processing.

What Next

Check and grant proper access permission for the corresponding directories, remove the existing old directories if needed, and rerun.

PWR-515

(error)

Description

This message indicates that the tool expects the given name is a directory in the file system, but it's not a regular directory.

Feedback

What Next

If there is a file with the same name, remove it. If the directory does not exist, create it and rerun.

PWR-516

(warning) Override existing %s directory or file

Description

This message indicates that the directory or file exists. Since the directory of the same name needs to be created for power replay processing, current directory or file will be overridden.

What Next

If the contents of the corresponding directory or file needs to be kept, rename it, otherwise the tool will override it by default.

PWR-517

(error) Can't remove backup %s directory. Directory

Description

This message indicates that the backup directory can't be removed due to access permission. The existing directory for power replay will be replaced and not backed up.

What Next

Change the access permission of the backup directory for proper backup of the current directory.

PWR-518

(error) Can't rename directory

Description

This message indicates that the existing directory can't be renamed to the new directory name.

What Next

Check and grant proper access permission to the directories and rerun.

Feedback

PWR-519

(error) The %s directory

Description

This message indicates that power replay need to write to the directory, but it has no writing permission.

What Next

Check and grant proper access permission to the directory and rerun.

PWR-520

(error) Command replay_activity has failed. Power replay options are reset.

Description

This message indicates that the replay_activity command failed due to error. The power options set by set_power_replay_options command are reset to their defult values.

What Next

Check previous detailed messages for the reason. set correct options with set_power_set_power_replay_options command and launch replay_activity command again.

PWR-521

(error) Failed to get RTL FSDB/VCD file information since %s.

Description

power replay requires RTL FSDB/VCD file as input, either from command option or derive from read_fsdb/read_vcd command. This message indicates that the tool can't find the information of RTL FSDb/VCD.

What Next

Check whether RTL FSDB/VCD file is proper set in the replay flow, fix the error and rerun.

PWR-522

(error) Can't open file

Feedback

Description

This message indicates that the tool can't open the file for reading/writing during power replay processing.

What Next

Check and grant the proper access permission to files/directories and rerun.

PWR-523

(error) Can't change file

Description

This message indicates that the tool can't change the file to the proper access mode.

What Next

Check and grant the proper access permission to files/directories and rerun.

PWR-524

(error) Can't find any RTL to gate naming mapping information.

Description

Power replay needs to map RTL names to netlist. This message indicates that the tool can't find any name mapping information. The default RTL to get name mapping is only available after readgin RTL FSDB with read_fsdb command.

What Next

Check whehter read_fsdb has already been called, and whether proper name mapping information has set for power replay. Fix the issue and rerun.

PWR-525

(error) Can't create %s file under %s directory.

Description

This message indicates that the tool can't create a file under the directory for power replay.

What Next

Check and grant the proper access permission to files/directories and rerun.

Feedback

PWR-526

(error) The %s process in replay_activity command has failed.

Description

This message indicates that the corresponding major process has failed in power the report_activity command.

What Next

To debug the issue, use set_power_replay_options -debug to output more information. Fix the issue and rerun.

PWR-527

(error) Can't find %s file

Description

This message indicates that the corresponding file was not found and power replay process has failed.

What Next

To debug the issue, use set_power_replay_options -debug to output more information. Fix the issue and rerun.

PWR-528

(information) Set power_disable_exact_built_in_name_mapping variable to false for generated activtiy.

Description

To match the names in gate level generated activity (FSDB) file to netlist, the power_disable_exact_built_in_name_mapping variable must to be set false. replay_activity command checks whether the variable is set to true. If that's the case, set it back to false.

What Next

Information only.

PWR-529

(error) Option type

Feedback

Description

The message indicates that the option in power replay config file is unknown or has not been supported.

What Next

Correct the power replay config file and rerun.

PWR-530

(error) Syntax error near line

Description

The message indicates that there is syntax erro near the line in the power replay config file.

What Next

Correct the power replay config file and rerun.

PWR-531

(error) Can't find any name mapping information for power replay.

Description

The message indicates that power replay can't find any mapping information. The information can be from generate_replay_man command, or set_rtl_to_gate_name commands.

What Next

Make sure name mapping information is generated before running replay_activity command.

PWR-532

(error) Failed to generate gate KDB with Verilog files in vlist file

Description

The message indicates that the tool tries to generate gate level KDB with the Verilog files in vlist provided by user, but failed.

What Next

Check whether the Verilog file list is complete, fix it and rerun.

Feedback

PWR-533

(error) Failed to generate target design. Please check the related option in set_power_replay_options command.

Description

The message indicates that the tool failed to generate the target design option for power replay. The target design can be generated with -target_design, -vtop with -lib, -dbdir or -vlist option in set_power_replay_options command.

What Next

Check the correctness of related option, fix the issue and rerun.

PWR-534

(information) Replay FSDB file is located at %s.

Description

The message shows the location of the output replay FSDB file. The file will be read back into PrimePower for accurate power analysis.

What Next

Information only.

PWR-535

(error) User specified RTL FSDB/VCD file %s does not exist.

Description

RTL FSDB file is specfied through config or set_power_replay_options command, but the file does not exist.

What Next

Check and correct the RTL FSDB/VCD file path and rerun.

PWR-536

(warning) %s file

Feedback

Description

The specified file from the command does not exist. The option of the command is ignored.

What Next

Check and correct the file path and rerun.

PWR-537

(warning) RTL FSDB file has already been read from read_fsdb command. File

Description

The message indicates that RTL FSDB file has already been read through read_fsdb command. The RTL FSDB file name specified from set_power_reply_options command or power replay config is ignored.

What Next

Ignore the warning if that's the intended behavior, or change the option to fix it.

PWR-538

(error) Can't generate default %s file

Description

The message indicates that the tool tries to generate the file as input to replay activities, but failed.

What Next

Check the access permission of corresponding file and directory. Fix the issue and rerun.

PWR-539

(error) Failed to generate map file from PowerReplay executable.

Description

The message indicates that the tool tries to generate replay map file by using powrep executable, but failed.

What Next

Check the related config setting, fix any issue and rerun.

Feedback

PWR-540

(warning) RTL FSDB from read_fsdb needs to be up to date to generate default replay mapping file.

Description

read_fsdb command for RTL FSDB generates built-in name mapping in addition to the user inputs. The message indicates that RTL FSDB information from read_fsdb is not up to date. Only user specified set_rtl_to_gate_name mapping info is used to generate default replay mapping file.

What Next

To generate replay mapping data with more coverage, Read RTL FSDB with read_fsdb command before replay_activity command.

PWR-541

(warning) Net %s is annotated from RTL FSDB. The constant from replay map file is ignored.

Description

In PrimePower replay flow, constant logic value of a net can be specified from the replay map file. If the net has activity annotation from RTL FSDB, the constant value from the replay map file will be ignored.

What Next

Check whether the logic and activity on the net is expected.

PWR-542

(warning) Constant

Description

In PrimePower replay flow, constant logic value of a net can be specified from the replay map file. This message indicates the constant value does not match the existing logic constant in the design from other sources.

What Next

Check whether the logic and activity on the net is expected.

Feedback

PWR-543

(information) Force signal logic to

Description

In PrimePower replay flow, constant logic value of a net can be specified from the replay map file. This information message indicates that the corresponding net has been forced to the constant.

What Next

Information only

PWR-544

(error) Can't make symbolic link %s to %s. Please use the original relayed FSDB file.

Description

When option -replayed_fsdb is specified for the replay_activity command, PrimePower makes a symbolic link of the name to the replayed FSDB file under replay log. The replayed FSDB will not be implicitly read in this case. The message occurs if it's failed to make such a symbolic link.

What Next

Check the access permission of the name or use the original replayed FSDB file.

PWR-545

(warning) Failed to derive strip_path for the replayed FSDB file %s.

Description

When option -replayed_fsdb is specified for the replay_activity command, the replayed FSDB will not be implicitly read in this case. The message occurs when the tool tries to automatically derive the strip_path for the replayed FSDB file.

What Next

Find out the strip_path from the design or check whether there is any issue in the related setting.

PWR-546

(information) Replay output file %s is successfully generated. Please run

Feedback

Description

When option -replayed_fsdb is specified for the replay_activity command, the replayed FSDB will not be implicitly read in this case. The message indicates that read_fsdb command needs to be run before update_power to read in replay FSDB file for accurate power analysis.

What Next

Information message.

PWR-547

(error) Can't derive target scope to replay activity. Please use set_power_replay_options -scope <scope_name> to specify the target scope.

Description

The target scope of power replay can be either specified from the *set_power_replay_options* command or derived from *read_fsdb* command. The message indicates the tool failed to derive the scope, or the scope is empty.

What Next

Check the setting of the power replay flow, fix the issue and rerun.

PWR-548

(information) Please check the target design options

Description

The message indicates that replay_activity command failed during extracting process of power replay. Possible reason can be incorrect options to generate the target design.

What Next

Check the options of the target design, fix and rerun.

PWR-601

(Information) Running %s analysis...

Description

PrimePower is running power analysis in the specified mode.

Feedback

See Also

- power_analysis_mode

PWR-602

(Information) Running power calculation with %d threads.

Description

PrimePower is running average power analysis in multiple threads.

See Also

- power_analysis_mode

PWR-603

(Warning) CCS power library data will no longer be supported in PrimePower starting 2018.06 release.

Description

Starting 2018.06 release, the tool will always use NLPM library data for power calculation. If CCS power data is presented, it will be ignored.

What Next

Characterize library using NLPM models for power.

PWR-604

(Warning) Legacy rail_connection library specifications will no longer be supported in PrimePower starting 2018.06 release.

Description

The tool supports Liberty PG pin syntaxes. Starting 2018.06 release, the tool will ignore legacy rail_connection related specifications.

What Next

Characterize library using Liberty PG pin sytnaxes.

PWR-610

(error) Can't find any clock in the design. Vector free analysis can not be run.

Feedback

Description

Clock needs to be defined for the vector free analysis feature.

What Next

Use create_clock to create a clock in the design. If the design doesn't have a real clock, create a virtual clock.

PWR-611

(error) Can't find any clock toggles in the design. Vector free analysis can not be run.

Description

Clock should toggle in the sdc for the vector free analysis feature.

What Next

Create a clock that has toggles.

PWR-612

(warning) The frequency of clock its source pin toggle rate. The toggle rate to clock frequency ratio is %g.

Description

This message occurs when there is mismatch between clock frequency and toggle rate at the source pin of the clock. Vector free rail analysis will scale the clock based on the toggle rate to match the switching activity profile of the design.

What Next

Check the consistency between SDC and user switching activities (VCD/SAIF/ set_switching_activity).

PWR-613

(information) The dominant clock of vector free analysis is

Description

Vector free analysis identifies a dominant clock controlling most part of the the design. The dominant clock will determine the simulation time and other behavior of vector free rail analysis.

Feedback

What Next

Confirm the dominant clock with SDC and user switching activities.

PWR-630

(Information) Running %s activity propagation...

Description

PrimePower is running activity propagation in the specified mode.

See Also

- power_analysis_mode

PWR-701

(Error) VCD filtering is not yet enabled.

Description

The feature requires VCD filtering to be enabled. Please set the corresponding variable to TRUE in order to use this feature.

PWR-702

(Error) The %s cost function is not enabled for VCD filtering.

Description

The specific cost filtering is not enabled. Use command *set_vcd_filtering_options* to enable this specific cost filtering.

PWR-703

(Error) %s can only be used in time-based power analysis

Description

The VCD filtering feature works only for time-based power anlsysis. This error indicates the specified VCD filtering command is not used in time-based power analysis.

PWR-704

(Error) The %s VCD filtering can't be performed as the filtering interval is not defined.

Feedback

Description

The specific VCD filtering requires the filtering interval to be defined. This error is encountered if neither filteirng interval nor clock is defined for the design. As default, the filtering interval is one clock cycle.

What Next

- use set_vcd_filtering_options to define the sampling interval for filtering Or - use create_clock to define the clock for the design.

See Also

- create_clock

PWR-706

(Information) Performed %s VCD filtering.

Description

The specific cost filtering has been performed.

PWR-801

(Error) UPF PST constructs are not enabled.

Description

This error message occurs when -pst option is specified in command report_power but UPF PST constructs are not enabled. Set variable 'upf_enable_pst' to TRUE before load_upf to enable UPF PST constructs in the tool.

What Next

Set variable 'upf_enable_pst' to TRUE and reload UPF.

See Also

- upf_enable_pst

PWR-802

(Error) Cann't find UPF power state group or PST defined at the current scope.

Feedback

Description

This error message occurs when option -pst is specified in command report_power but UPF power state group or PST has not yet been defined at the current scope.

What Next

Please check UPF PST specifications.

See Also

- report_power

PWR-803

(Warning) Option %s cann't be specified for PST based power reporting. It is ignored.

Description

This error message occurs when the specific option is specified along with option -pst in report_power. This report option is ignored for PST based power reporting.

See Also

- report_power

PWR-901

(error) Number of annotated nets from VCD is too low (< 95%) to calculate peak power.

Description

The number of annotated nets from VCD is too low (less then 95%) to calculate peak power.

The VCD file might come from RTL simulation in which case peak power calculation (create_power_waveforms) is allowed only if you use -cycle_accurate which enables cycle-accurate peak power analysis. See create_power_waveforms man page.

If you don't want the peak power, you can use update_power for average power calculation for RTL VCD. To generate average cycle waveform and its peak power, set the variable power_force_saif_flow to TRUE.

What Next

Use report_switching_activity to check the annotated activity and also check the VCD file. If it's a RTL VCD, make sure to add -cycle_accurate option to create_power_waveforms.

Feedback

PWR-902

(error) Average activity report not compatible with other options.

Description

The -average_activity flag allows for averaging toggle rates and glitch rates. The -state_cond, -source_pins, -rise, -fall flags cannot be used in conjunction with the -average_activity_flag.

What Next

Remove incompatible flags

PWR-903

(error) Filter options not allowed together with other specified options.

Description

The filter options -exclude, -exclude_source, -include_only, -include_only_source cannot be used together with any of the -state_cond, -source_pin, -rise, -fall options.

What Next

Remove the incompatible options.

PWR-904

(error) Cannot run get_switching_activity on pins with given options

Description

The command *get_switching_activity* cannot operate on pins of the design if the -average_activity, -exclude, -exclude_source, -include_only, -include_only_source, or -sort options have been used.

What Next

Remove the options, or try get_switching_activity on nets, or on hierarchical cells (for -average_activity).

PWR-905

(error) Only one of -average_activity, -coverage, -list_not_annotated, -list_annotated, -list_zero_activity, -list_low_activity, -list_by_source may be used in a single call to report_switching_activity.

Feedback

Description

Only one of -average_activity, -coverage, -list_not_annotated, -list_zero_activity, -list_low_activity, -list_by_source may be used in a single call to report_switching_activity.

What Next

Instead of requesting multiple reports with report_switching_activity, simply run the command multiple times, and request a different report with each command.

PWR-906

(error) report_switching_activity list options do not support -hierarchical

Description

The list options for report_switching_activity provide lists of nets. Reporting hierarchically is not supported.

What Next

Remove the -hier flag from the command.

PWR-907

(error) The primary_clock option is only supported with the -average_activity report.

Description

The primary_clock option only has meaning with the -average_activity report. It is an error to use the -primary_clock option with a different report request.

What Next

Remove the -primary_clock option.

PWR-908

(error) Option toggle_limit has no effect with other options chosen

Description

The option -toggle_limit only has an effect when the -coverage option or the -list_low_activity option are used with the command report_switching_activity.

What Next

Remove the -toggle_limit option from the report_switching_activity command.

Feedback

PWR-909

(error) The option -sort has no effect with other options chosen.

Description

For the command report_switching_activity, the -sort option only has an effect when the option -average_activity is chosen.

What Next

Remove the -sort option.

PWR-910

(error) Clock '%s' not found.

Description

A proper clock name must be specified with the -primary_clock option.

What Next

Make sure that the clock you intend to use as the primary clock exists in the design.

PWR-911

(error) Unknown source in '%s'

Description

An unrecognized source was specified with the -list_by_source option for the report_switching_activity command.

What Next

Specify the *report_switching_activity -list_by_source* command with one of the following sources: saif, vcd, default, propagated, set_switching_activity, set_case_analysis, annotated.

See Also

- report_switching_activity

PWR-912

(Error) Unknown source in '%s'

Feedback

Description

An unrecognized source was specified with the *-list_by_source* option for the *report_switching_activity* command.

What Next

Specify the *report_switching_activity -list_by_source* command with one of the following sources: saif, vcd, default, propagated, set_switching_activity, set_case_analysis, annotated.

See Also

- report_switching_activity

PWR-913

(error) Unknown source or group '%s'

Description

An unrecognized source or group was specified with the report_switching_activity command in relation to one of the filter options -exclude, -exclude_source, -include_only, -include_only_source

Possible sources are the following:

file, default, propagated, set_switching_activity, set_case_analysis, annotated, no_switching_activity.

Possible groups are the following:

sequential, combinational, black_box, tri_state, primary_input, rtl

---

PWR-914

(Error) Source string too long.

Description

The source list string for the *report_switching_activity* command was unexpectedly long.

See Also

- report_switching_activity

Feedback

PWR-915

(Error) The exclude options 'extended_clock' and 'buffer_tree' are not yet implemented for the Beta version of PrimePower

What Next

Wait until the release version to use these features.

PWR-916

(Error) Unknown source specification or exclusion group specified.

PWR-917

(error) The option -sort has no effect with other options chosen.

Description

For the command report_switching_activity, the -sort option only has an effect when the option -average_activity is chosen.

What Next

Remove the -sort option.

PWR-918

(error) Unknown sort method

Description

For the command report_switching_activity, the -sort option sorts net lists or hierarchical block lists.

For net lists, -sort net_toggle_rate or -sort name can be used

For hierarchical block lists, -sort net_toggle_rate sorts over the average toggle rate in the cell. -sort name and -sort hierarchy can also be used.

What Next

Remove the -sort option or change the -sort argument.

PWR-919

(error) No such clock found for -only_related_clock option

Feedback

Description

For the command report_switching_activity or get_switching_activity, the clock specified by the -only_related_clock option could not be found in the design.

What Next

Verify that the given clock exists in the design, or remove the -only_related_clock option.

PWR-920

(Error) cannot use -leakage_only flag with peak power analysis or when waveforms are requested.

Description

The *-leakage_only* flag for *report_power* can only be used with average power analysis.

PWR-921

(warning) Timing will not be updated prior to power analysis, and timing is not up-to-date.

Description

Timing will not be updated prior to power analysis. This can happen when either the -no_propagation flag was used, or leakage variation analysis is being used.

If the -no_propagation flag has been used, but timing is not up-to-date, then changes in clocks or case_analysis will not be reflected in the switching activity for power analysis. Changes in switching activity will not be propagated. Default power groups may not be correct.

Power groups may not be correct. In particular, without timing information, the tool will not properly distinguish between objects in the sequential and register groups.

What Next

Either avoid using the -no_propagation flag with report_power, or make sure that changes made to the design and the constraints will not affect switching activities. Avoid relying on power breakdowns into power groups.

See Also

- report_power

Feedback

PWR-922

(warning) There were %d nets without switching activities. No activity will be propagated. Default activity will be used on these nets.

Description

When the -no_propagation flag is used, propagation is skipped. Nets without activities will be treated as if they had default activity.

What Next

To take advantage of more accurate state-dependent power analysis, either apply activities to the design with a SAIF file, or avoid use of the -no_propagation flag.

PWR-923

(error) Only static probability can be reported for a cell when the -state_condition argument is used.

Description

The get_switching_activity command does not support the use of -state_condition and either -toggle_rate or -glitch_rate when applied to a cell. This is because only leakage power is associated with the state of a cell.

What Next

Remove the -toggle_rate or -glitch_rate flag

PWR-924

(error) This command can only be used in upf mode.

Description

The command set_supply_net_probability can only be used when upf compatibility mode is on.

What Next

Set the variable power_domains_compatibility to FALSE and avoid use of commands incompatible with upf mode.

PWR-925

(error) Options

Feedback

Description

The command report_power cannot be used with the specified features while the variable power_enable_leakage_variation_analysis is set to true.

What Next

Set the variable power_enable_leakage_variation_analysis to FALSE or remove the options from report power and try again.

PWR-926

(error) Leakage variation analysis failed. No report can be generated

Description

The report_power command tried to access the results of leakage variation analysis. But no results were found, indicating that the analysis failed.

What Next

Determine the cause of why leakage variation analysis failed, and rerun the analysis. If the leakage variation report is not wanted, set the variable power_enable_leakage_variation_analysis to FALSE and rerun report_power.

PWR-927

(error) Unknown interpolation method

Description

The variable *power_leakage_variation_interpolation_methods* should only be set to one of the values "exp", "linear_add", "linear_factor", "quadratic".

What Next

Changes the value of the variable *power_leakage_variation_interpolation_methods*.

PWR-928

(error) Option %s is not permitted when leakage variation is disabled.

Description

Certain options to the *report_power* command are available only if the leakage variation feature is enabled.

Feedback

What Next

To enable the leakage variation feature, set the *power_enable_leakage_variation_analysis* variable to i*true*.

See Also

- report_power

PWR-930

(error) Inconsistent or overlapping time windows

Description

The time windows used for activity analysis using the -time option of the command *create_activity_waveforms* must be nonoverlapping. They must be list in order from earliest to latest.

Bad example : *-time {0 100 50 200}* Good example : *-time {0 100 110 200}*

What Next

Reorganize the time windows so that they are nonoverlapping and listed from earliest to latest. Alternatively, remove the time option and run the analysis on the whole VCD.

PWR-931

(error) Inappropriate -interval option

Description

The *-interval* option for the *create_activity_waveforms* command indicates the time, in nanoseconds, over which the activity is aggregated. If the value is two small (less than 10 vcd timesteps) or two large (more than a trillion timesteps), this error is generated.

What Next

Choose an appropriate value for the interval.

PWR-932

(error) VCD file contains wire/reg at line %d not included in the VCD header

Feedback

Description

The VCD header should include all wires and reg identifiers. This erro is produced when the VCD includes a value change for a wire or reg not previously identified in the header. This indicates that the VCD is malformed.

What Next

Probably the simulator which produced the VCD has an issue.

PWR-933

(Warning) VCD file has reg/wire id '%s' defined multiple times with inconsistent size at VCD line number %d, for wire named '%s'.

Description

The indicated reg/wire was defined several different times in the VCD header, and had different sizes indicated in the VCD header. This can happen if the reg/wire is listed under several different hierarchical blocks in the VCD, and it is listed as having different sizes in different places.

In this case, any extra bits in the reg/wire may end up having zero toggles. This can affect the average toggle rate for a module.

In the VCD file, the following line defines s reg/wire:

```
$var reg 6 id wire_name [5:0] $end
```

Where *id* is a unique id for a signal, and *wire_name* is a (possibly non-unique) name for the signal.

Multiple definitions can have the same *id*. In this case, PrimePower treats them as the same signal. In this way, reg/wires can be defined multiple times.

Note that if a vpd or fsdb file was used as input, the VCD line number will not be meaningful for the input file.

PWR-934

(warning) large number of events necessitates some time shifting for event energy in the waveform

Description

This warning can happen during *update_power* with large designs in some cases.

This warning is only issued once per session. If this happens multiple times, the user will be warned only at the first time it occurs in a session.

Feedback

Internally, PrimePower keeps track of a time window of switching events. In some large cases, when the window is large (maybe due to large maximum cell delay), or when there are a lot of events in a short period of time, the internal buffers can get too large. To prevent overflows, PrimePower will immediately print out it's stored buffers to the power waveforms. It is possible that in doing this, PrimePower may have to print out part of the waveform before all data for the time window is known. In this case, any switching energy discovered later will be shifted later in time.

Average power calculations will not be affected, since all switching energy is accounted for. However, it is possible that if this happens at a peak, the peak may be lost due to shifting the energy to a later time.

What Next

Inspect the waveform after is is created. Re-run power analysis using the -time option with a small time window near the peaks.

PWR-935

(error) write_activity_waveforms must be run before report_activity_waveforms

Description

Analysis on a VCD file must be run before the report on the activity can be generated

What Next

Run write_activity_waveforms.

PWR-936

(error) vector length in activity file is not consistent for object %s at VCD line number %d.

Description

The VCD file has a vector with inconsistent length.

Example:

```
$var reg 4 a a [5:0] $end
```

This should be:

```
$var reg 6 a a [5:0] $end
```

Note that the VCD line number may not be the same as the fsdb line number if you used fsdb as input.

Feedback

What Next

Regenerate VCD file.

PWR-937

(Warning) The option -exclude_cells was used, but no corresponding modules were found in the VCD.

Description

The -exclude_cells option is used to exclude some modules from the VCD during time-based activity analysis. If the -exclude_cells option is used, but none of the specified modules were found in the VCD, then this warning is generated. However, activity analysis is not prevented by this warning.

What Next

Check to see that the correct VCD is being used. Check to make sure the spelling of module names in the -exclude_cells list is correct.

PWR-940

(error) Leakage variation analysis cannot be run with create_power_waveforms or the event based power flow.

Description

The variable power_enable_leakage_variation_analysis has been set, but the event-based flows in PrimePower cannot be used for leakage variation analysis.

What Next

Try report_power instead to run leakage variation analysis.

PWR-941

(error) Clock gate reporting failed.

Description

Clock gate savings reporting failed.

What Next

Nothing.

Feedback

PWR-942

(Warning) Could not find a %s pin on cell %s.

Description

During clock gate savings analysis, a cell was found, and a particular pin on the cell was searched for but could not be found.

If the cell is an ICG cell, but it is not used as a clock gate, this error will be generated because the clock pins on the cell could not be determined using timing information. Even if the cell is part of the clock tree, if (for instance) the enable on the cell is tied high, then the cell is not be used as a clock gate, and this warning will be reported.

If this warning is reported, the given cell will be excluded from the report and from any averaged reported by the command.

What Next

No suggestion.

PWR-943

(error) Could not find a clk_in pin on cell %s involved in clock gating.

Description

During clock gate savings analysis, a cell was found to be involved with clock gating, but no clk_in pin could be found.

What Next

No suggestion.

PWR-944

(error) Could not run command because power is not up-to-date

Description

Something went wrong when running power analysis.

What Next

Investigate and successfully run update_power. Then try again the command that issued the error.

Feedback

PWR-945

(Warning) Identified cell %s is not a hierarchical instance and will be skipped.

Description

A leaf cell passed to report_clock_gate_savings was expected to be a hierarchical instance in the design, but was not.

What Next

Remove the cell from the cell list and try again, or, alternately, just ignore the warning.

PWR-946

(Warning) Identified cell %s is not used as a clock gate and will be skipped.

Description

A leaf cell passed to report_clock_gate_savings was expected to be a clock gate in the design, but was not.

What Next

Remove the cell from the cell list and try again, or, alternately, just ignore the warning.

PWR-947

(Warning) Identified cell %s is not used as a register and will be skipped.

Description

A leaf cell passed to report_clock_gate_savings was expected to be a register in the design, but was not.

What Next

Remove the cell from the cell list and try again, or, alternately, just ignore the warning.

PWR-948

(error) Sorting option %s is not valid unless used with option %s

Description

A -sort_by option was given that is not valid in combination with the other options used.

Feedback

What Next

Change the requested sorting option, or remove the -sort_by option entirely.

PWR-949

(error) No design objects were found for analysis.

Description

During report_clock_gate_savings, no design objects of the type required (either registers or clock gates) were found for analysis.

What Next

Check the options used. It may be that the cell_list used was too restrictive. Also check the current_instance to make sure the instance being analyzed is the desired instance.

PWR-950

(error) The value for the -peak_window option should be a multiple of the interval.

Description

The *-peak_window* option of the *write_activity_waveforms* command or the *set_vcd_filtering_options* command causes the tool to identify a high activity in a larger window than the interval. The window size indicated should be a multiple of the interval size.

What Next

Adjust the requested peak window size to be a multiple of the interval size.

PWR-951

(error) The value for -peak_window option is unreasonable.

Description

The *-peak_window* option for the *write_activity_waveforms* command causes the tool to identify a high activity in a larger window than the interval. The window size indicated should be larger than the interval size, but limited to no more than a few thousand times the size of the interval. If a larger peak window is desired, the interval size should be increased as well. If a smaller peak window is desired, the interval should be smaller.

What Next

Adjust the requested peak window size or the interval size.

Feedback

See Also

- write_activity_waveforms

PWR-952

(error) Hierarchical cell %s cannot be processed by get_switching_activity unless the -average_activity flag is used.

Description

The activity of hierarchical cells can only be reported if the command is instructed to average the activity over the nets in the cell.

If the activity of each net in the hierarchical cell is desired, the following command can be used:

```
pt_shell> current_instance my_hier_cell
my_hier_cell
pt_shell> get_switching_activity [get_net -hier *]
```

What Next

Use leaf cells only, or apply the -average_activity flag

PWR-953

(Warning) For clock %s, the toggle rate %g is inconsistent with the toggle rate implied by the clock period, %g. There may be inconsistency between annotated activity and the sdc. Using %g.

Description

During report_clock_gate_savings default report, the toggle savings for registers is computed from the toggle rate on the primary clock as compared to the toggle rate on the clk pin of the register. In finding the toggle rate of the clock, there was an inconsistency between the clock period, and the toggle rate on the clock net, which may have been annotated.

This situation can arise if the sdc clock was different than that used by simulation to generate the vectors.

When these toggle rates are inconsistent, the annotated value is used.

What Next

Check to see if the sdc and simulation used different clock periods.

Feedback

PWR-954

(Warning) For clock %s, the toggle rate is either zero or is uninitialized. Clock gate savings with respect to this clock cannot be computed.

Description

During report_clock_gate_savings default report, the toggle savings for registers is computed from the toggle rate on the primary clock as compared to the toggle rate on the clk pin of the register. However, when the toggle rate of the clock is zero, toggle savings will be computed as zero.

What Next

Check the activity annotation on the clock source.

See Also

- report_clock_gate_savings
- get_switching_activity

PWR-955

(Warning) Identified cell %s is neither register nor clock gate and will be skipped.

Description

A leaf cell passed to report_clock_gate_savings was expected to be either a register or a clock gate in the design, but was not.

What Next

Remove the cell from the cell list and try again, or, alternately, just ignore the warning.

PWR-961

(error) Set the power_analysis_mode variable instead of using the set_power_analysis_mode command.

Description

The power analysis mode is controlled by setting the *power_analysis_mode* variable. Using the *set_power_analysis_mode* command is not permitted.

What Next

Set the *power_analysis_mode* variable instead.

Feedback

See Also

- power_analysis_mode

PWR-968

(Error) -exclude_rail and -rails options in set_power_budget command are mutually exclusive.

Description

-exclude_rail and -rails options in set_power_budget command are mutually exclusive.

What Next

Please specify any one of these two options with set_power_budget command.

PWR-969

(Error) -propagate should only be specified with -rail option in set_power_budget command.

Description

-propagate should only be specified with -rail option in set_power_budget command.

What Next

Please specify -rail option along with -propagate in set_power_budget command.

PWR-970

(Error) Attribute not available while leakage variation analysis is enabled.

Description

The requested attribute is not available while leakage variation analysis is enabled.

What Next

Turn off leakage variation analysis by setting power_enable_leakage_variation_analysis to false. Alternately, you can request the leakage_power attribute for the object, which will contain a quantile value.

PWR-971

(Warning) Could not map activity file signal '%s' on VCD line %d.

Feedback

Description

The signal from the activity file (VCD or SAIF) could not be found in the design. If the activity file is from RTL simulation, it could be that the signal was removed during synthesis.

See Also

- update_power

PWR-972

(Error) Could not map '%s' to a design object in Boolean expression '%s'.

Description

The *-when* option takes a Boolean expression as an argument. The identifiers in the expression must correspond to design nets or pins.

See Also

- read_vcd

PWR-973

(Error) The -when option specifies a Boolean expression string that could not be parsed: '%s' at token '%s'

Description

The *-when* option takes a Boolean expression as an argument. There was a problem when parsing the expression.

What Next

Check the expression to make sure you are using Boolean operators, and that there are no extra parentheses, or look for other problems.

See Also

- read_vcd

PWR-974

(Information) There were %d periods when the -when expression was true, for a total time of %g.

Feedback

Description

The *-when* option takes a Boolean expression as an argument. The expression was true for some distinct periods during the VCD. when the expression is not true, power is not calculated, and the time is subtracted from the total simulation time when computing average power.

See Also

- read_vcd
- update_power

PWR-975

(Error) Could not determine the activity file type from the file name.

Description

The tool was unable to determine the file format from the file name.

What Next

If you do not use the *report_activity_file_check* command with the *-format* option, the tool attempts to determine the file format from the file name.

Run the *report_activity_file_check* command with the *-format* option.

See Also

- read_saif
- read_vcd
- report_activity_file_check

PWR-976

(Error) Option '%s' cannot be used if the %s is '%s'.

Description

For the command report_activity_file_check, some options are not available for some activity file formats or power analysis modes. In general, options are only available for SAIF formats if a similar option is available for the read_saif command.

What Next

Run the command again without the incorrect option, or change the activity file format.

Feedback

See Also

- read_saif
- read_vcd

PWR-977

(Error) The design object %s was used in the Boolean expression of the -when argument, but was not annotated from the VCD.

Description

The *-when* option takes a Boolean expression as an argument. The variables of the expression are design objects or VCD signal names. All variables of the expression must map to a design object and must be annotated from the VCD.

See Also

- read_vcd
- update_power

PWR-978

(Error) The glob pattern %s could not be parsed

Description

Glob patterns use * to represent multiple characters. Multiple glob patterns can be included in one string by using commas (,). Commas and braces ({}) should be escaped if they need to be used literally.

See Also

- report_activity_file_check

PWR-979

(Error) Unknown type '%s' for power_cell_type attribute.

Description

The power_cell_type attribute only allows the following types: clock_network, register, combinational, sequential, memory, black_box, io_pad. The error occurs when a string different from the above type is set for the power_cell_type attribute.

Feedback

What Next

Make sure the string value is correct and run the command again.

See Also

- report_power

PWR-980

(Warning) PG pin %s is inferred as power pin for %s pin on cell %s. %s looks like a ground pin by name.

Description

Power pin with positive supply voltage reported for the pin of the cell looks like a ground pin by name.

What Next

No suggestion.

PWR-981

(Warning) Partial mapping of VCD vector %s encountered, which may cause incorrect annotation.

Description

You received this warning message because the VCD file contains vectors which are only partially mapped. When name-mapping is applied to bits of a vector bus, PrimePower assumes that all the bits are mapped, which can lead to annotation of incorrect values.

What Next

First, run the VCS utility: vcdpost [+scalar] *original_VCD_file bit_blasted_VCD_file*. Read the bit-blasted VCD file into PrimePower with the *-read_vcd* command to ensure accurate annotation.

See Also

- read_vcd

PWR-982

(error) Power is not calculated. Please run update_power before get_power_per_pgpin.

Feedback

Description

It is required that update_power be run before get_power_per_pgpin.

What Next

Refer to man pages of update_power.

PWR-983

(Warning) Could not find mode name %s, skipping the mode.

Description

Given mode name in the sequence list is not present in the macro model.

What Next

Please review the list of valid modes in the macro model.

PWR-984

(Warning) Can't find user defined clock %s, using derived clock for the macro modes.

Description

The user defined clock is not found. Tool will continue with the derrived clocks for the macro.

What Next

Please check the validity of the clock names defined in the command line for setting macro mode sequence.

PWR-985

(Warning) Can't find related clock macro model %s.

Description

Tool could neither find macro model's own clock nor any user defined clock.

What Next

Please check the macro model connection for the related clock.

PWR-986

(Warning) Can't find trigger pin of macro model %s for mode %s.

Feedback

Description

Tool could not find trigger pin for the reported macro cell model for the reported mode.

What Next

Please check the macro model for the trigger pin of the mode.

PWR-987

(Warning) Can't find design pin for trigger pin %s of macro model %s for mode %s.

Description

Tool could not find design pin for the trigger pin for the reported macro cell model for the reported mode.

What Next

Please check the macro model for the design pin.

PWR-988

(Warning) PG pin %s of cell %s is not connected to any supply nets.

Description

Tool could not find any connection to supply net for the reported PG pin of the reported macro cell.

What Next

Please check the design for the PG pin connection.

PWR-989

(error) get_power_per_rail is not supported, when multi_rail analysis is disabled.

Description

It is required to enable multi_rail analysis to support get_power_per_rail. Please set "power_enable_multi_rail_analysis" true.

What Next

Refer to man pages of get_power_per_rail.

Feedback

PWR-990

(Warning) Power budget set on %s cell is less than the cell's leakage power. Ignoring the given power budget.

Description

Power budget set on the cell is less than the cell's leakage power. Ignoring the given power budget.

What Next

Please assign valid power budget on the given cell.

PWR-991

(Warning) The sum of power budget being set on %s cell, power budget of its siblings, excluded power and original leakage powers of the rest of the block are greater than the parent %s cell's power budget. Ignoring the given power budget.

Description

The sum of power budget being set on the cell, power budget of its siblings, excluded power and original leakage powers of the rest of the block are greater than the parent cell's power budget. Ignoring the given power budget.

What Next

Please assign valid power budget on the given cell.

PWR-992

(Warning) Power budget set on %s rail of the cell %s is less than the cell's leakage power for the same rail. Ignoring the given power budget.

Description

Power budget set on rail of the cell is less than the cell's leakage power for the same rail. Ignoring the given power budget.

What Next

Please assign valid power budget on this rail of the given cell.

PWR-993

(Warning) The sum of power budget being set on %s rail of the cell %s, power budget of the cell's siblings for the same rail, excluded power for the same rail and original leakage

powers of the rest of the block for the same rail are greater than power budget of cell's parent cell %s for the same rail. Ignoring the given power budget.

Description

The sum of power budget set on the rail of the cell, power budget of the cell's siblings for the same rail, excluded power for the same rail, and original leakage powers of the rest of the block for the same rail are greater than power budget of cell's parent cell for the same rail. Ignoring the given power budget.

What Next

Please assign valid power budget on this rail of the given cell.

PWR-994

(Warning) Power budget set on %s hierarchical cell is less than the sum of power budgets applied on cells under its hierarchy, excluded power under its hierarchy and leakage powers of the rest of the block. Ignoring the given power budget.

Description

Power budget set on the hierarchical cell is less than the sum of power budgets applied on cells under its hierarchy, excluded power under its hierarchy and original leakage powers of the rest of the block. Ignoring the given power budget.

What Next

Please assign valid power budget on the given cell.

PWR-995

(Warning) Power budget set on %s hierarchical cell is less than the sum of power budgets applied on cell's rails, excluded rails's powers and original leakage powers of the rest of cell's rails. Ignoring the given power budget.

Description

Power budget set on the hierarchical cell is less than the sum of power budgets applied cell's rails, excluded rails's powers and original leakage powers of the rest of cell's rails. Ignoring the given power budget.

What Next

Please assign valid power budget on the given cell.

Feedback

PWR-996

(Warning) Power budget set on %s rail of the cell %s is less than the sum of power budgets of this rail under the cell's hierarchy, excluded power of this rail under the same hierarchy and original leakage powers for this rail of the rest of block. Ignoring the given power budget.

Description

Power budget set on the rail of the cell is less than the sum of power budgets of this rail under the cell's hierarchy, excluded power of this rail under the same hierarchy and original leakage powers for this rail of the rest of block. Ignoring the given power budget.

What Next

Please assign valid power budget on this rail of the given cell.

PWR-997

(Warning) The sum of power budget being set on %s rail of the cell %s, other rail's power budget, excluded rails's powers and original leakage powers of the rest of rails are greater than the cell's power budget. Ignoring the given power budget.

Description

The sum of power budget set on rail of the cell, other rail's power budget, excluded rails's powers and original leakage powers of the rest of rails are greater than the cell's power budget. Ignoring the given power budget.

What Next

Please assign valid power budget on this rail of the given cell.

PWR-998

(Error) This command/option(s)

Description

This is not supported in legacy power domain mode.

What Next

Set the variable power_domains_compatibility to FALSE and avoid use of commands incompatible with upf mode.

Feedback

PWR-999

(error) Mode based analysis not supported in time based power analysis.

Description

power_enable_mode_support cannot be set to true when in time based analysis mode. Mode based analysis need to be disabled.

PWR-1000

(warning) 'power_order_clock_events' can only be set to true with '-rtl' or '-zero_delay' in command read_vcd .

Description

You received this error message because command 'power_order_clock_events' can only used with '-rtl' or '-zero_delay' options in command read_vcd.

What Next

command read_vcd

PWR-1001

(error) Can't create work directory '%s' as write permission not granted.

Description

Kindly provide write permission to create work directory.

What Next

Please refer to man page of the command for more information on options.

PWR-1002

(Warning) Overwriting existing entry for opcond %s vt %s fin %s depth %s edge_type %s with latest value.

Description

Warning for overwriting existing values with the latest provided values.

Feedback

See Also

- read_vcd
- update_power

PWR-1003

(error) static probability can not be fraction in Time-based power analysis mode.

Description

Time-Based power analysis does not allow fraction value of supply net probability to determine what fraction of the time the cells connected to the supply net are powered. It is used to determined whether cells connected to supply net powered on/off.

What Next

Please refer to man page of the command for more information on options.

PWR-1004

(Error) The attribute can only be queried after update_timing.

Description

Some command can only be used after the update_timing command has been successfully run through.

What Next

Run update_timing command first.

PWR-1005

(error) Couldn't find any clock in FSDB, using SDC clock.

Description

This message indicates that PrimePower will use SDC clock, since it could not find any clock in FSDB.

What Next

None.

Feedback

PWR-1006

(error) Output waveform file:

Description

This message indicates that the existing waveform output file cannot be opened for writing. Hence, setting the waveform format to "none".

What Next

Check and grant proper access permission to the directories and rerun.

PWR-1007

(Warning) %s not present in fsdb. strip_path + RTL name should be present in fsdb.

Description

The rule is that strip_path + RTL name should be present in fsdb.

PWR-1008

(Error) report_sensitivity_power_lib_mapping command should be invoked before update_power

Description

report_sensitivity_power_lib_mapping should be invoked before update_power as the sensitivity library related checks should happen right after library loading. Once power is calculated, it is of no help to do the sensitivity checks.

What Next

Invoke the command before update_power command

PWR-1009

(Warning) initialization start time (%g) time of the analysis window greater than the event time (%g). Resetting and ignoring initialization start time.

PWR-1010

(Warning) no Physical DB or LLE DLL file loaded for cell %s

Feedback

PWR-1011

(error) Can't find any valid pg_pins in specified design for command set_annotated_power -pg_pin.

Description

set_annotated_power -pg_pin [pg_pin_list] accepts a list of valid design pg_pin names. The error occurs when there is no valid pg_pin found from the pg_pin name list.

What Next

Check and fix the design pg_pin names in the -pg_pin option.

PWR-1012

(Error) report_sensitivity_power_lib_mapping command should be invoked before update_power

Description

report_sensitivity_power_lib_mapping should be invoked before update_power as the sensitivity library related checks should happen right after library loading. Once power is calculated, it is of no help to do the sensitivity checks.

What Next

Invoke the command before update_power command

PYPR

PYPR-001

(warning) Voltage slack analysis is not performed because no define_scaling_lib_group for interpolation.

Description

Voltage slack analysis requires cells in a link library to be also present in scaling library group for interpolation. This error message reports library scaling groups are not defined.

What Next

Make sure that all library scaling groups are defined by *define_scaling_lib_group* command before performing Voltage slack analysis. Furthermore, make sure that *-exact_match_only* and *-best_match* options are not specified with *define_scaling_lib_group* command.

See Also

- define_scaling_lib_group

PYPR-002

(warning) Voltage slack analysis is skipped due to insufficient library scaling groups coverage %s. %s

Description

Voltage slack analysis (VSA) requires every library cell in a link library to also be present in every scaling library. This warning message reports insufficient scaling library groups for VSA.

This warning message is generated in the following two cases: missing DSLG or no overlapped scaling range.

- Missing DSLG:

In this case, "because the number of cells without DSLG exceeds the non-DSLG cell threshold" is appended to the warning message. This means that the number of cells without DSLG exceeds the non-DSLG cell threshold specified by the *vsa_non_dslg_cell_threshold* variable. Check for any PYPR-010 message for cell warning and add more scaling library groups. Adjust the non-DSLG cell threshold by changing the *vsa_non_dslg_cell_threshold* variable value.

- No overlapped scaling range:

In this case, "because there is no overlapped range for voltage scaling" is appended to the warning message. This means that there is no overlapped range for voltage scaling up or down. The tool is unable to perform voltage scaling in VSA.

What Next

- Verify that all scaling library groups are defined using the define_scaling_lib_group command and the exact_match_only option is not specified. • If VSA is skipped because the non-DSLG cell threshold is exceeded, adjust the vsa_non_dslg_cell_threshold variable value.

See Also

- define_scaling_lib_group
- vsa_non_dslg_cell_threshold
- PYPR-010

Feedback

PYPR-003

(warning) An extrapolation exceeding voltage scaling range has been detected. The accuracy of Voltage slack analysis may be affected. %s

Description

Voltage slack analysis performs voltage extrapolation in voltage slack calculation and the result is potentially lesser accurate due to insufficient library scaling group coverage.

What Next

Make sure that all library scaling groups are defined by *define_scaling_lib_group* command before performing Voltage slack analysis. Furthermore, make sure that *-exact_match_only* and *-best_match* options are not specified with *define_scaling_lib_group* command.

See Also

- define_scaling_lib_group

PYPR-004

(warning) Voltage slack analysis is not performed on unconstrained path. %s

Description

Voltage slack analysis only recomputes constrained paths and ignores unconstrained paths.

What Next

Only perform Voltage slack analysis on constrained paths.

PYPR-005

(warning) Voltage slack analysis is not performed on hold path. %s

Description

Voltage slack analysis only recomputes setup paths and ignores hold paths.

What Next

Only perform Voltage slack analysis on setup paths.

Feedback

PYPR-006

(warning) Voltage slack analysis is not performed when -path_type full_clock_expanded is not specified.

Description

Voltage slack analysis is only available for *-path_type full_clock_expanded* report.

What Next

To enable Voltage slack analysis, specify the *-path_type full_clock_expanded* option on *get_timing_paths* or *report_timing*.

See Also

- get_timing_paths
- report_timing

PYPR-007

(warning) Voltage slack analysis is not performed because -pba_mode is not specified.

Description

Voltage slack analysis is only available for *PBA mode*.

What Next

To enable Voltage slack analysis, specify the *-pba_mode path*|*exhuastive* option on *get_timing_paths* or *report_timing*.

See Also

- get_timing_paths
- report_timing

PYPR-008

(error) Voltage slack analysis -voltage_sweep should be specified with 1 voltage shift or a voltage sweep series [start,end,step].

Description

Error out for illegal Voltage slack analysis -voltage_sweep format.

What Next

Specify Voltage slack analysis -voltage_sweep command with a single voltage shift (relative to nominal voltage) or a voltage sweep series with start and end voltage shift and a voltage step in three numbers.

See Also

- get_timing_paths

PYPR-009

(warning) Voltage slack analysis voltage_sweep step size should be set to %.3f or greater instead of %.3f.

Description

Automatically correction to run with mininum step size for Voltage slack analysis voltage_sweep option.

What Next

Voltage slack analysis voltage_sweep should be run with reasonalbe step size to avoid excessive data size and runtime consumption.

See Also

- get_timing_paths

PYPR-010

(warning) No enough scaling library group (%s) for cell '%s'. The accuracy of voltage slack analysis may be affected. %s

Description

Voltage slack analysis (VSA) requires every library cell in a link library to also be present in every scaling library. This warning message reports the cell that has no scaling library and that the VSA result is potentially less accurate because of insufficient scaling library groups for some cells.

This warning message is generated in the following cases:

- “missing DSLG” in the warning message indicates that there is no scaling library for the cell. • “exact_match_only” in the warning message indicates that the cell has scaling library group but in exact_match_only mode and is unable to scale during the vdd_slack search.

Feedback

What Next

Verify that all scaling library groups are defined using the define_scaling_lib_group command and the exact_match_only option is not specified, before performing VSA.

See Also

- define_scaling_lib_group

PYPR-011

(warning) Voltage slack is clipped for path that %s. %s

Description

Voltage slack is clipped because of one of the following two reasons.

- The calculated voltage slack is above the upper vdd_slack_lesser_than threshold. • The calculated voltage slack is below the lower vdd_slack_greater_than threshold.

What Next

- Case 1: Increase the vdd_slack_lesser_than threshold to print the voltage slack. • Case 2: Decrease the vdd_slack_greater_than threshold to print the voltage slack.

Note: Runtime may increase with increase in the vdd_slack_lesser_than threshold or decrease in the vdd_slack_greater_than threshold.

See Also

- get_timing_paths
- report_timing

PYPR-012

(warning) Voltage slack analysis skipped for zero cycle path. %s

Description

Voltage slack analysis only recomputes constrained paths and ignores zero-cycle paths.

What Next

Only perform Voltage slack analysis on non-zero cycle paths.

Feedback

See Also

- get_timing_paths
- report_timing

PYPR-013

(warning) Voltage slack analysis skipped due to non-monotonic slack found at %.3f drop. %s

Description

This message is issued because a non-monotonic slack is found during Voltage slack search so that Voltage slack analysis is skipped.

What Next

Make sure that all library scaling groups are defined by *define_scaling_lib_group* command before performing Voltage slack analysis. Furthermore, make sure that *-exact_match_only* and *-best_match* options are not specified with *define_scaling_lib_group* command.

See Also

- define_scaling_lib_group

PYPR-014

(warning) Voltage slack set to voltage slack boundary because voltage slack is larger than default voltage slack boundary. %s

Description

Voltage slack is set to voltage slack boundary because voltage slack is larger than default voltage slack boundary.

What Next

Enlarge default voltage slack boundary before performing Voltage slack analysis.

See Also

- get_timing_paths
- report_timing

Feedback

PYPR-015

(warning) Voltage slack analysis voltage sweep range is reduced to [%.3f, %.3f] because of limited scaling library range [%.3f, %.3f].

Description

This error message reports voltage sweep range is reduced due to insufficient scaling library groups for sweep analysis.

What Next

Make sure that all library scaling groups are defined by *define_scaling_lib_group* command before performing Voltage slack analysis. Furthermore, make sure that *-exact_match_only* and *-best_match* options are not specified with *define_scaling_lib_group* command.

See Also

- define_scaling_lib_group

PYPR-016

(warning) Voltage slack analysis skipped because pba_derate_only_mode is set as true.

Description

Voltage slack analysis requires full recalculation instead of adjusting derating only.

What Next

Make sure *pba_derate_only_mode* is set to false before performing Voltage slack analysis.

See Also

- get_timing_paths
- report_timing
- pba_derate_only_mode

PYPR-017

(warning) Voltage slack analysis is not supported in Distributed Analysis.

Feedback

Description

You receive this message to inform you *hierarchical distributed analysis* is not fully supported Voltage slack analysis.

What Next

Do not use *-vdd_slack_lesser_than* after enabling hierarchical distributed analysis.

PYPR-018

(warning) In voltage slack analysis, DSLG range is extended by %.2f%%. The accuracy may be affected.

Description

This message is issued because DSLG range is extended. The result is potentially lesser accurate due to voltage extrapolation.

What Next

Verify that all scaling library groups are defined using the define_scaling_lib_group command and the exact_match_only option is not specified, before performing VSA.

See Also

- define_scaling_lib_group

PYPR-019

(warning) The delay of %s is annotated. The voltage sensitivity will be replaced by zero.

Description

This message is issued because a cell delay is annotated. The voltage sensitivity will be accuracy loss.

What Next

Do not apply annontated delay or remove it by remove_annotated_delay to get more accurate voltage sensitivity.

See Also

- set_annotated_delay
- remove_annotated_delay

Feedback

PYSIM

PYSIM-001

(warning) Recommended minimum sample size is %d to have at least %d tail samples for %.2f sigma.

Description

In *sim_analyze_path* command, user can specify Monte Carlo sample size by "-sample_size" option. If the specified sample_size is not large enough to get enough tail samples, the message will be issued that more samples are recommanded.

What Next

Increase sample_size or remove -sample_size option to let *sim_analyze_path* pick default sample size.

See Also

- sim_analyze_path

PYSIM-002

(error) PrimeShield is disabled.

Description

It's required to enable PrimeShield before *sim_analyze_path* command.

What Next

Set *ps_enable_analysis* to true before running *sim_analyze_path* command.

See Also

- sim_analyze_path
- ps_enable_analysis

PYSIM-003

(error) Only %.2f to %.2f sigma supported.

Feedback

Description

In *sim_analyze_path* command, user can specify focused sigma by "-num_sigma" option. Without the option, focued sigma is based on *timing_pocvm_report_sigma*. It has to be in the range of supported number of sigma.

What Next

Update *timing_pocvm_report_sigma* to be in the range or use "-num_sigma" option in *sim_analyze_path*.

See Also

- sim_analyze_path

PYSIM-004

(information) Default sample size %d used in sigma amplification mode.

Description

In *sim_analyze_path* command, when number of sigma is larger than 5.2, *sim_analyze_path* automatically uses 100M samples and enable sigma amplification mode. You don't have to specify sample_size. If sample_size is specified, this message will show up.

What Next

No need to specify "-sample_size" option with larger than 5.2 sigma.

See Also

- sim_analyze_path

PYSIM-005

(error) Full Monte Carlo for sigma level > 5.2 is not supported due to extremely slow runtime.

Description

In *sim_analyze_path* command, full Monte Carlo mode errors out due to extremely slow simulation time when sigma level is too high.

What Next

Enable fast Monte Carlo by *simlink_enable_fast_monte_carlo* for high sigma simulation to avoid extremely slow runtime.

Feedback

See Also

- sim_analyze_path
- simlink_enable_fast_monte_carlo

PYSIM-006

(information) Default sample size %d used for %.2f sigma, please increase sample_size if targeting higher accuracy.

Description

In *sim_analyze_path* command, the default sample size is picked based on focused number of sigma. If accuracy target is higher, you can increase the sample size by specify "-sample_size" option with larger number of sample size.

What Next

Consider using more samples if targeting on higher accuracy.

See Also

- sim_analyze_path

PYSIM-007

(error) Path %d report skipped due to failed simulation.

Description

In *sim_analyze_path* command, sometimes certain paths failed simulation. Common reason can be missing subckt for on path cells, hspice license issue, or spice model settings is wrong. Report on the path is skipped.

What Next

Check for reason of simulation failure. Fix the simulation failure or skip the path in *sim_analyze_path*.

See Also

- sim_analyze_path
- sim_setup_library
- sim_setup_simulator

Feedback

PYSIM-008

(information) Cell %s is replaced by pin cap %s in SPICE deck.

Description

In *sim_analyze_path* command, if an off-path cell does not have subckt, it will be replaced by pin cap in SPICE deck to avoid simulation failure.

What Next

If more accurate simulation is needed, please update subckt file to include missing subckt.

See Also

- sim_analyze_path
- sim_setup_library

PYSIM-009

(error) %s sigma reported based on qqt0.csv is %f, please increase sample size.

Description

In *sim_analyze_path* and *sim_validate_path* full Monte Carlo simulation, there is a limit of sigma range reported due to sample size. If the focused sigma level is not available in SPICE output qqt0.csv file, more samples are needed.

What Next

Using larger sample size for Monte Carlo simulation.

See Also

- sim_analyze_path
- sim_validate_path

PYSIM-010

(information) Only %d PrimeShield licenses are available, update max farm job count to %d.

Description

In *sim_analyze_path* and *sim_validate_path* fast Monte Carlo simulation, when simulation jobs are running on the farm and there are only limited number of PrimeShield licenses

available, max farm job count is reduced to meet license requirement. Other jobs will wait until some farm jobs are finished and *PYSIM-010 message is issued.*

If there is not enough PrimeShield license for 1 farm job at a time, *PYSIM-011* error message is issued.

What Next

Obtain more licenses if faster turnaround time is needed.

See Also

- sim_analyze_path
- sim_validate_path
- PYSIM-011

PYSIM-011

(error) No PrimeShield license is available to run simulation.

Description

In *sim_analyze_path* and *sim_validate_path* fast Monte Carlo simulation, when simulation jobs are running on the farm and there are only limited number of PrimeShield licenses available, max farm job count is reduced to meet license requirement. Other jobs will wait until some farm jobs are finished and *PYSIM-010 message is issued.*

If there is not enough PrimeShield license for 1 farm job at a time, *PYSIM-011* error message is issued.

What Next

Obtain more PrimeShield licenses.

See Also

- sim_analyze_path
- sim_validate_path
- PYSIM-010

PYSIM-012

(error) Required minimum sample size is %d to have at least %d tail sample for %.2f sigma.

Feedback

Description

In *sim_analyze_path* command, user can specify Monte Carlo sample size by "-sample_size" option. If the specified sample_size is too small, the message will be issued that more samples are needed.

What Next

Increase sample_size or remove -sample_size option to let *sim_analyze_path* pick default sample size.

See Also

- sim_analyze_path

PYSIM-013

(error) Required settings are not present for full Monte Carlo analysis.

Description

Purpose of the Error message is to avoid unintentional full Monte Carlo analysis, that can take a long time. In order to run full Monte Carlo analysis, two settings must be present: pt_shell> *set simlink_full_monte_carlo_error_out false* pt_shell> *set simlink_enable_fast_monte_carlo false* Otherwise, the default tool behavior is meant to safeguard against unintentional full Monte Carlo analysis.

What Next

To enable full Monte Carlo analysis, add the following settings pt_shell> *set simlink_full_monte_carlo_error_out false* pt_shell> *set simlink_enable_fast_monte_carlo false*

See Also

- simlink_enable_fast_monte_carlo

PYSR

PYSR-001

(warning) Voltage robustness analysis is not performed because no define_scaling_lib_group for interpolation.

Feedback

Description

Voltage robustness analysis requires cells in a link library to be also present in scaling library group for interpolation. This error message reports library scaling group are not defined.

What Next

Make sure that all scaling library groups are defined by *define_scaling_lib_group* command before performing voltage robustness analysis. Furthermore, make sure that *-exact_match_only* and *-best_match* options are not specified with *define_scaling_lib_group* command.

See Also

- define_scaling_lib_group

PYSR-002

(error) Voltage robustness analysis is not performed because -pba is not specified with -reg_to_reg.

Description

Voltage robustness analysis only support analyzing reg-to-reg path in PBA mode. This error message reports PBA mode is not enable while analyzing reg-to-reg paths.

What Next

Make sure that *-pba* option is specified with *-reg_to_reg* option.

See Also

- define_scaling_lib_group

PYSR-003

(error) report_voltage_robustness -voltage_shift and -voltage_shift_ratio can not be set together.

Description

Voltage robustness analysis -voltage_shift and -voltage_shift_ratio options are mutually exclusive settings.

What Next

Choose to use either absolute shift amount in report_voltage_robustness *-voltage_shift* option or relative amount in *-voltage_shift_ratio*.

See Also

- report_voltage_robustness

PYSR-004

(error) report_voltage_robustness -voltage_shift and -voltage_shift_ratio can not be set with negative or zero values.

Description

Negative or zero values in report_voltage_robustness -voltage_shift or -voltage_shift_ratio options are invalid.

What Next

Make sure that *-voltage_shift* or *-voltage_shift_ratio* option are specified with positive values.

See Also

- report_voltage_robustness

PYSR-005

(warning) An '%f' extrapolation exceeding voltage scaling range [%f, %f] has been detected. The accuracy of voltage robustness may be affected. [Cell: '%s']

Description

Voltage robustness analysis performs voltage extrapolation in robustness slack calculation and the result is potentially less accurate due to insufficient scaling library group coverage.

What Next

Make sure that all library scaling groups are defined by *define_scaling_lib_group* command before performing Voltage robustness analysis. Make sure that *-voltage_shift* or *-voltage_shift_ratio* is small enough so that the post-shift VDD is still within DSLG range.

See Also

- report_voltage_robustness

Feedback

PYSR-006

(error) Can not perform -dvd without DvD data. Please apply read_dvd beforehand.

Description

DvD-aware voltage robustness is not performed because design has not been annotated with DvD.

What Next

Use command 'read_dvd' to read in the DvD file first.

See Also

- read_dvd

PYSR-007

(error) Can not use -dvd with -voltage_shift or -voltage_shift_ratio.

Description

DvD-aware voltage robustness is not available for options -voltage_shift and -voltage_shift_ratio.

What Next

Remove one of the options -dvd, -voltage_shift, and -voltage_shift_ratio.

QTCL

QTCL-001

(error) Cannot find widget '%s'.

Description

The widget with the specified hierarchical name cannot bre found. The listed command options are exclusive. Only one of them can be specified.

What Next

Check whether the hierarchical path of the widget name is correct or whether the widget is already created.

Feedback

QTCL-002

(error) At least one of the following options need to be specified: '%s'.

Description

Not all required arguments are specified.

What Next

Check the correct syntax of the command and add all required arguments.

QTCL-003

(error) No widget name specified (option: %s).

Description

The new name of the widget is not specified.

What Next

Add the widget name with the described option.

QTCL-004

(error) Sender widget '%s' not found.

Description

The sender widget is not found with the specified hierarchical name.

What Next

Check whether the hierarchical path of the widget name is correct or whether the widget is already created.

QTCL-005

(error) Receiver widget '%s' not found.

Description

The receiver widget is not found with the specified hierarchical name.

What Next

Check whether the hierarchical path of the widget name is correct or whether the widget is already created.

Feedback

QTCL-006

(error) Parent Widget '%s' not of class type %s.

Description

The parent of the new widget is not of the required class type.

What Next

Check which parent class types are allowed for the new widget and correct the appropriate option.

QTCL-007

(error) Widget with name '%s' already exists.

Description

A widget with the specified hierarchical name already exists. You cannot create widgets with identical hirarchical names.

What Next

Choose a unique hirarchical name for the new widget.

QTCL-008

(error) Property '%s' of widget '%s' is not valid or not readable.

Description

A widget property with the specified name does not exist or is not readable.

What Next

Check the existence or readability of the property or correct the name.

QTCL-009

(error) Property '%s' of widget '%s' not found.

Description

The specified widget property does not exist.

What Next

Check whether the specified widget property exists or correct the property name.

Feedback

QTCL-010

(error) Widget '%s' of class type '%s' does not support list of items.

Description

The class type of the specified widget does not support list of items. The current tcl function cannot be apllied on this widget.

What Next

Correct the class type or widget name.

QTCL-011

(error) Setting value '%s' for property '%s' of widget '%s' failed.

Description

Cannot set the property value of specified name.

What Next

Check in the widget documentation whether the property is not writable. Check the correctness of the hierarchical widget name and property name.

QTCL-012

(error) Cast of value '%s' for property '%s' of widget '%s' to type '%s' failed.

Description

Cannot convert the value of the specified widget value to the data type of the property.

What Next

Check whether this data type is supported. Check the correctness of the hierarchical widget name and the property name.

QTCL-013

(error) Cannot cast value '%s' for property '%s' of widget '%s' to type '%s'.

Description

Cannot convert the value of the specified widget value to the data type of the property.

Feedback

What Next

Check whether this data type is supported. Check the correctness of the hierarchical widget name and the property name.

QTCL-014

(error) Widget of class '%s' not supported.

Description

The specified class type is not yet supported.

What Next

Choose one of the supported widget class types.

QTCL-015

(error) Value '%d' of option '%s' is out of range (%d <= index <= %d).

Description

The specified option value is out of the allowed range.

What Next

Correct the value according to the described option value range.

QTCL-016

(error) Indices list '%s' is not correct. Syntax: {i1 i2 ... in}.

Description

The syntax of the index list is not correct.

What Next

Correct the syntax according to the described syntax.

QTCL-017

(error) Specified ui file '%s' does not exist.

Description

The specified ui file does not exist.

Feedback

What Next

Correct the path name and filename and check the existence of the file.

QTCL-018

(error) Value '%d' of option '%s' is out of range (must be %s).

Description

The option value os out the the allowed described range.

What Next

Correct the option value according to the described range rules.

QTCL-019

(error) Cannot connect signal '%s' of sender '%s'\nto slot '%s' of receiver '%s'.

Description

Cannot setup a connection between sender and reciever widget.

What Next

CHeck for the correct hierarchical names of the sender and receiver widgets. Check the correct names and arguments for signal and slot functions.

QTCL-020

(error) Cannot connect signal '%s' of sender '%s'\nto tcl command '%s'.

Description

Cannot setup a connection between sender widget and a tcl clallback function.

What Next

CHeck for the correct hierarchical name of the sender widget. Check the correct name and arguments for signal and tcl function.

QTCL-021

(error) The star '*' is not allowed as last name in hierarchical widget name %s'.

Feedback

Description

The charecter '*' cannot be used as the last name in the specifier of a hierarchical widget name.

What Next

Use this character only for levels in between.

QTCL-022

(error) Widget '%s' has already specified %sproperty '%s'.

Description

The widget has already a property or extra property of the specified name.

What Next

Check for the correct hierarchical name of the sender widget. Check the correct name of the extra widget property and make sure that no other extra property is already attached to the widget.

QTCL-023

(error) Incorrect value '%s' for enum property '%s' of widget '%s'.

Description

The property with a enum datatype cannot be initialized with the specified value.

What Next

Make sure that you only use supported values for the enum datatype.

QTCL-024

(error) Object '%s' is not of type 'widget'.

Description

The specified object is not derived from QWidget. In order to work properly is needs to be derived from QWidget or from a class derived frm QWidget.

What Next

Derive the object from QWidget or from a class derived from QWidget.

Feedback

QTCL-025

(error) Parent object '%s' is not derived from QWidget

Description

The specified parent object is not derived from QWidget.

What Next

Derive the parent object from QWidget or from a class derived from QWidget.

QTCL-026

(error) The specified file '%' does not exist or is not readable

Description

The specified file does not exist or is not readable.

What Next

Check the existence and the read permissions of the specified file.

QTCL-027

(error) Cannot find parent '%s'.

Description

The object with the specified hierarchical name specified as parent cannot be found.

What Next

Check whether the hierarchical path of the widget name is correct.

QTCL-028

(error) Widget '%s' is not inherited from QDialog.

Description

The specified widget needs to be inherited from QDialog in order to provide the correct functionality.

What Next

Derive specified widget from QDialog or widget derived from QDialog.

Feedback

QTCL-029

(error) Cannot find extension widget '%s'.

Description

The specified dialog extension widget does not exist.

What Next

Check correct name and creation of dialog extension widget.

QTCL-030

(error) Dialog extension object '%s'is not a widget.

Description

The specified dialog extension widget is not a widget.

What Next

Derive the dialog extension object from QWidget or an object derived from QWidget.

QTCL-031

(error) Syntax of string list argument value '%s' incorrect.

Description

The syntax of the value of a string list argument is incorrect.

What Next

Correct the value of the string list argument.

QTCL-032

(error) Cannot find menu item '%s'.

Description

The specified menu item does not esist.

What Next

Check the existence and specification of the menu item.

Feedback

QTCL-033

(error) Object alias '%s' already in use.

Description

The object specified object alais is already in use by another object.

What Next

Choose another object alias name.

QTCL-034

(error) Cannot disconnect signal '%s' of sender '%s'\nto slot '%s' of receiver '%s'.

Description

Cannot disconnect the specified signal from specified sender to receiver.

What Next

Check correct names of signal, sender, receiver and slot.

QTCL-035

(error) Cannot disconnect signal '%s' of sender '%s'\nto tcl command '%s'.

Description

Cannot disconnect the specified signal from specified sender to tcl command.

What Next

Check correct names of signal, sender and tcl command name.

QTCL-036

(error) Property '%s' of object '%s' is ReadOnly

Description

Cannot set the value of specified property since it is a 'ReadOnly' property.

QTCL-037

(error) Value list has more items than signal or slot argument definition

Feedback

Description

The number of values passed to a signal or slot function does not match the number of arguments of the signal or slot function.

What Next

Check the number of arguments of signal or slot function and the number of values.

QTCL-038

(error) Cannot activate slot '%s' of receiver object '%s'

Description

Cannot find the name of the slot function for the specified receiver object

What Next

Check correct names of the slot function and the receiver object.

QTCL-099

(error) '%s'

Description

Generic error

What Next

Fix issue or request specific error

QTM

QTM-1

(error) Cannot create the QTM model '%s' before saving the existing one.

Description

You have tried to create a new QTM model before saving the current QTM model.

What Next

Save the current QTM model using *save_qtm_model* and then create a a new QTM model.

Feedback

QTM-2

(error) There is no QTM model that is currently being defined.

Description

You are using a QTM command without actually creating a QTM model.

What Next

Use *create_qtm_model* to create a new QTM model. All QTM commands have to be between a *create_qtm_model* and *save_qtm_model* command.

QTM-3

(error) Unable to load the library '%s'

Description

QTM is unable to load the library you have specified. Perhaps you have not read in the library.

What Next

Please make sure that the library is read in using the *read_db* command. QTM will not be able to auto load the library even if the library is in the search path.

QTM-4

(warning) Technology library '%s' has been already been loaded

Description

You have already defined the technology library. The existing technology library will be replaced with the new one.

What Next

If you do not intend to overwrite the existing technology library please reload the existing technology library

QTM-5

(warning) The parameter '%s' has already been set to '%f', overriding with the new value.

Feedback

Description

The global parameter has already been set, the existing value will be overridden with the new value.

What Next

If you do not want to override the existing value of the global parameter, please set it back to the old value.

QTM-6

(warning) The parameter '%s' has already been set to '%s'; overriding with the new value.

Description

The global parameter has already been set, the existing one is overridden with the new value.

What Next

If you do not want the overridden value, please replace it with the existing value.

QTM-7

(error) The option '%s' cannot be used in conjunction with '%s'

Description

The two options cannot be used together. Please use either one of them.

What Next

Please use either one of the two options.

QTM-8

(error) To use option '%s', you must also use the option '%s'.

Description

The two options have to be used together, you cannot use one of them alone.

What Next

Use the two options together.

Feedback

QTM-9

(error) To use option '%s', a library should have been specified, but no library has been specified for this model

Description

You are attempting to use a lib_cell, but you have not set the technology library.

What Next

Please set the technology library with *set_qtm_technology* with the -library option to set the technology library.

QTM-10

(warning) The path type '%s' has already been defined, redefining the path type with the new one.

Description

The path type has already been defined. The existing path type definition will be replaced by the new path type definition.

What Next

If you do not want the existing path type definition to be replaced by the new one, give unique names to the two different path types.

QTM-11

(error) The library cell '%s' is not present in the technology library you have specified.

Description

The specified lib_cell is not present in the technology library.

What Next

Please provide the correct lib_cell name.

QTM-12

(error) The '%s' pin '%s' you have specified, is not present in the cell '%s'.

Description

The input/output pin name specified is not present in the lib_cell.

Feedback

What Next

Please provide the correct input/output pin name for the lib_cell you are using.

QTM-13

(warning) Fanout count not specified for the path type '%s'; using the default fanout of %d.

Description

You have not specified the fanout count for the path type definition. The tool uses a default count of 1.

What Next

If you do not want to use the default fanout count (of 1), please provide the fanout count using the -fanout option.

QTM-14

(warning) The drive type '%s' has already been defined; redefining the drive type with the new one.

Description

The drive type has already been defined. The existing drive type definition will be replaced by the new drive type definition.

What Next

If you do not want the existing drive type definition to be replaced by the new one, give unique names to the two different drive types.

QTM-15

(warning) The load type '%s' has already been defined; redefining the load type with the new one.

Description

The load type has already been defined. The existing load type definition will be replaced by the new load type definition.

What Next

If you do not want the existing load type definition to be replaced by the new one, give unique names to the two different load types.

Feedback

QTM-16

(warning) The port '%s' has already been created in the model. Replacing the original port with the new port.

Description

A QTM port with the same name already exists; the original port will be replaced with the new port.

What Next

If you want the original port direction, recreate the port.

QTM-17

(error) Must specify one of '%s', or '%s' options

Description

Must use either one of the two options in the command.

What Next

Please use one of the two options in the command.

QTM-18

(error) The '%s' QTM parameter '%s' used has not been defined

Description

The QTM parameter you are using has not been defined. Please define the QTM parameters before using them. For e.g., if you are using a path type A in defining a timing arc, please define the path type A before using it in the timing arc.

What Next

Please define the QTM parameters (path type, drive type, load type) before using them.

QTM-19

(error) The port '%s' used in the arc is not defined

Description

The port referred in the arc has not been defined.

Feedback

What Next

Please define the ports before using them in the timing arcs.

QTM-20

(error) The '%s' port for a '%s' arc must be a '%s' port, but port '%s' is of type '%s'.

Description

The port type for the type of arc you are defining is not of the correct type.

For a setup arc, the from port must be of type clock and the to port must be of type input/inout.

For an edge delay arc, the from port must be of type clock and the to port must be of type output/inout.

For a combinational delay arc, the from port must be of type input/inout and the to port must be of type output/inout.

What Next

Create the arc between valid type of ports as explained above.

QTM-21

(error) The port '%s' is not a bus, but you have implied a bus structure.

Description

You have implied a bus structure for the port, but the port is not a bus.

What Next

If the port is intended to be a bus, define the port to be of bus type, else use the port in a non bussed fashion.

QTM-22

(error) The bus index specified %d:%d for the bus '%s', is out of the bus array bounds %d:%d.

Description

The indicies used for the bus is not within the array bounds of the bus.

Feedback

What Next

Please check the array bounds of the bus and use the indicies with the array bounds.

QTM-23

(error) The arc that is an edge arc (launch) has more than one port (%d) as the from port.

Description

An edge delay arc can originate from a single port. In the edge delay arc you have defined, there is more than one 'from' port.

What Next

If you want to define more than one edge delay arc to the same port, define different timing arcs, do not combine them in one.

QTM-24

(error) The global '%s' parameter has not been defined, you cannot define a '%s' arc

Description

Before defining setup/hold/edge delay timing arcs, the corresponding global parameter have to be defined.

Before defining setup arcs, define the global parameter, global setup time using *set_qtm_global_parameter* with -setup option.

Before defining hold arcs, define the global parameter, global hold time using *set_qtm_global_parameter* with -hold option.

Before defining edge delay arcs, define the global parameter, global clock to output time using *set_qtm_global_parameter* with -clk_to_output option.

What Next

Define the corresponding global parameter before defining the setup/hold/edge delay arcs.

QTM-25

(error) Cannot get clock pin for the cell '%s'.

Description

The cell does not have a clock pin. If you are defining global setup/hold/clk_to_output time using a lib_cell, the lib_cell should have the corresponding arc types, which means that the cell must have a clock pin too.

Feedback

What Next

Please use a lib_cell that has an arc corresponding to the global parameter you are defining.

QTM-26

(error) Cannot find a '%s' arc in the cell '%s' from the clock pin '%s'.

Description

If you are defining global parameter (setup/hold/clk_to_output) using lib_cell, the lib_cell must have corresponding arc. Further, if you specify the clock pin, there must be a corresponing arc from the clock pin.

What Next

Please provide a lib_cell and a clock pin which has a timing arc corresponding to the global parameter you are defining. For example, If you are defining global setup time, the lib_cell must have a setup arc whith regard to the clock pin. If you are defining global hold time, the lib_cell must have a hold arc with regard to the clock pin. If you are defining global clk_to_output time, the lib_cell must have a clk_to_output arc originating from the clock pin.

QTM-27

(error) Cannot find the pin '%s' in the cell '%s'

Description

Cannot find the pin specifed in the lib_cell.

What Next

Please check the pin name and give a valid pin name in present in the lib_cell.

QTM-28

(error) Pin '%s' is not of type '%s'

Description

The pin is not of the type desired.

What Next

Provide a pin in the lib_cell which is of the type desired.

Feedback

QTM-29

(error) Could not find arc of type '%s' coming %s the pin %s.

Description

QTM expects a timing arc to come into/go out of the specified pin. It did not find an arc of the corresponding type at the pin.

What Next

Please specify a pin in the lib_cell to satisfy the above requirement.

QTM-30

(error) Could not find arc from clock '%s' to the output pin '%s'.

Description

The lib_cell does not have an edge delay arc from the clock pin to the output pin.

What Next

Choose the clock pin and output pin such that there is an edge delay arc from the clock pin to the output pin.

QTM-31

(error) The port '%s' is not defined in the QTM model.

Description

The port you are referring to has not been defined in the QTM model.

What Next

Please define the port before referring to the port.

QTM-32

(error) The port '%s' for which the drive is defined is neither an output port nor an inout port.

Description

Drive can be defined only on the output/inout ports.

Feedback

What Next

Please define drives only for output ports.

QTM-33

(error) The drive type '%s' used is not defined

Description

The drive type you have referenced has not been defined.

What Next

Please define the drive type before refering to the drive type.

QTM-34

(error) The port '%s' for which the load is defined is not an input port, a clock port, or an inout port.

Description

A load can be defined only on input/clock/inout ports, and not on output ports.

What Next

Define the loads only on input/clock/inout ports.

QTM-35

(error) The load type '%s' used is not defined.

Description

The load type referenced has not been defined.

What Next

Please define the load type first before referring to it.

QTM-36

(error) There is no pin '%s' of type %s in the cell '%s'.

Description

The input or output pin specified is not present.

Feedback

What Next

THe pin you specified is not present or the direction of the pin might not be right.

QTM-37

(error) No arc exists from '%s' to '%s' in the lib_cell %s.

Description

Could not find a combinational arc between the two specified pins.

What Next

Please specify the pins between which there is a combinational arc.

QTM-38

(information) Path Type: %s, Cell: %s, Input Pin: %s, Output Pin: %s Delay : %f.

Description

This is an informational message that provides the details of the path type defined.

What Next

This is not an error message.

QTM-39

(information) Load Type: %s, Cell: %s, Pin: %s.

Description

This is an informational message which provides the details of the load type defined.

What Next

This is an information message.

QTM-40

(information) Drive Type: %s, Cell: %s, Input Pin: %s, Output Pin: %s .

Description

This is an informational message which prints the details of the drive type defined.

Feedback

What Next

This is an informational message.

QTM-41

(information) Parameter: %s, Cell: %s, Clock Pin: %s, Input Pin: %s, Constraint Value : %f.

Description

This informational message prints out the details of the global parameter defined.

What Next

This is an informational message.

QTM-42

(information) Parameter: clk_to_output, Cell: %s, Clock Pin: %s, Output Pin: %s Delay Value : %f

Description

This informational message prints the details of the clk_to_output parameter defined.

What Next

This is an informational message.

QTM-43

(error) Parameter '%s' cannot be a negative number

Description

The parameter cannot have a negative value

What Next

You have entered a negative for a parameter which is invalid. Please enter a value greater than 0 for the parameter

---

QTM-44

(error) Port '%s' not defined to be a clock

Description

For a constraint or clk_to_output arc, the from port must be a clock.

Feedback

What Next

Create the constraint or clk_to_output arc starting from a clock port.

QTM-45

(error) Port '%s' not of the type input/inout.

Description

The 'to' port of a constraint arc must be of the type input/inout. Any other port direction is illegal.

What Next

Create the constraint arc ending in an input/inout port.

QTM-46

(error) Port '%s' not of the type output/inout.

Description

The 'to' port of a delay arc must be of the type output/inout.

What Next

Create the delay arc ending in an output/inout port.

QTM-47

(error) Port '%s' not of the type input/inout.

Description

The 'from' port of a delay arc must be of the type input/inout.

What Next

Create the delay arc starting from an input/inout port.

QTM-48

(warning) The port '%s' has invalid name.

Description

A QTM port with an invalid name is being created. Examples, are " ", "/".

Feedback

What Next

Check the name of the port that you are creating. If the ports are defined in a list, check the list.

QTM-49

(warning) Wire Load Model '%s' does not exist in the library. Using 0 capacitance.

Description

The Wire Load Model specified must exist in the technology library.

What Next

Specify a valid Wire Load Model name.

QTM-50

(error) Input transitions have already been defined for drive type '%s'.

Description

The drive type you have referenced has been defined with rise and/or fall input transitions. You cannot specify the transition again for the port.

What Next

Please define another drive type without transition specification before refering to it for this port.

QTM-51

(error) %s.

Description

This is a general error message due to some unexpected command options, and/or settings in creating the QTM.

What Next

Please correct the indicated error and try again.

QTM-52

(error) Attribute '%s' for object class '%s' %s type '%s'.

Feedback

Description

This is an error message indicating the specified attribute for the indicated QTM object class has already been defined to the given type, or it is an application reserved attribute of the specified type.

What Next

Please correct the indicated error and try again.

QTM-53

(information) Defining new attribute '%s' of type '%s' for object class '%s'.

Description

This is an informational message indicating the specified attribute for the QTM object class has been successfully defined.

What Next

No user action necessary.

QTM-54

(error) %s '%s' has not been defined.

Description

This is a general error message indicating the specified object has not been defined in the QTM, therefore it cannot be refered to in other commands.

What Next

Please correct the indicated error and try again.

QTM-55

(error) No attribute named '%s' is defined for object class '%s'.

Description

This is an error message indicated the named attribute for the specifed object class has not been defined yet.

What Next

Please define the attribute for the QTM object class before set it on objects.

Feedback

QTM-56

(error) Attribute named '%s' for object class '%s' is not defined as type '%s'.

Description

This is an error message indicated the named attribute for the specifed object class has not been defined yet.

What Next

Please define the attribute for the QTM object class before set it on objects.

QTM-57

(warning) Attribute '%s' is not defined for %s%s.

Description

This is a warning message indicating that the named attribute for the specifed object/class has not been defined yet.

What Next

Please define the attribute for the QTM object class before set or remove it on objects.

QTM-58

(information) Attribute '%s' has already been set on%s'%s' and is now replaced with the new value.

Description

This is an informational message indicating that the named attribute for the specifed object/class has not been re-defined, so the value is updated.

What Next

No user action is necessary.

QTM-59

(error) The specified value '%s' does not match the defined data type '%s'.

Description

This is an error message indicating the given attribute value does not match the type defined for the attribtue.

Feedback

What Next

Please correct the indicated error and try again.

QTM-60

(information) Attribute '%s' successfully removed for '%s'.

Description

This is an informational message indicating the specified attribute for the QTM object has been successfully removed.

What Next

No user action necessary.

QTM-61

(error) Cannot find a proper timing arc in the specified lib cell to define the drive.

Description

This is an error message indicating that PrimeTime cannot find a proper delay arc in the specified cell to be used in defining the drive. There are 2 possible reasons for this: 1. the absense of a proper delay arc to be used as a driving arc. 2. there are ambiguities in deciding a specific arc that can be used to define the drive.

What Next

If the error is caused by absense of proper timing arcs in the lib cell, please choose another lib cell with arcs providing the intended driving characteristics. If the error is caused by ambiguity, please use options such as -input_pin and -output_pin to tell PrimeTime exactly which timing arc should be used to define the drive.

QTM-62

(warning) Defining '%s' attribute on %s disables %s, %s.

Description

This is a general warning message. It may not be an error requiring corrective action, but it provides important information for your reference.

For example, the 'function' attribute for lib_pin, even thought QTM allows 'function' attribute be defined for ports, but it treats the boolean logic expressions as string literals, does not perform any syntax check, and only writes QTM with such attributes to .lib format, the correctness of the attributes therefore only enforeced when compiled by LibraryCompiler.

What Next

Please note and confirm the indicated reason/action and make any changes if necessary.

QTM-63

(error) Attribute '%s' for object class '%s' can not be defined for %s '%s', %s.

Description

This is an error message indicated the named attribute for the specifed object class is not applicable to the named object.

What Next

Please correct the definition of the attribute for the indicated QTM object and try again.

QTM-64

(warning) The bus port '%s' does not match the existing bus port in QTM.

Description

Bus ports must be removed together by giving the start and end index (A[0:5]). A single bus port can not be removed.

QTM-65

(warning) No QTM '%s' object is removed.

Description

When no object is removed, it could be that no object in the current QTM satisfied the given conditions in the command. Please check the given options and rerun the command.

RC

RC-001

(error) The parasitics of the net '%s' could not be completed.

Description

There are some dangling nodes in the partially annotated parasitics of the net.

Feedback

What Next

You must correct the parasitics file and try to complete the net again.

RC-002

(warning) The net '%s' controls only a subset of the drivers of the multidriven net '%s', so detailed RC delay calculation cannot be used.

Description

A net is controlling the switching activity of only a subset of the drivers of a multidriven net. The switching activity of the remaining drivers is uncertain, so detailed RC delay calculation cannot be used. Instead, the load is assumed to be the total capacitance of the multidriven net divided by the number of drivers.

What Next

Ensure that all drivers are switched by each from_net (that is, they are wired in parallel), or annotate delays and transition times if you want greater accuracy than the lumped fallback analysis can provide.

See Also

- set_annotated_delay
- set_annotated_transition
- DES-023
- RC-003

RC-003

(warning) The net '%s' connects to more than one pin or arc on a driver of the multidriven net '%s', so detailed RC delay calculation cannot be used.

Description

A net is ambiguously controlling the switching activity of the drivers of a multidriven net, so detailed RC delay calculation cannot be performed. Instead, the load will be assumed to be the total capacitance of the multidriven net divided by the number of drivers.

What Next

Ensure that all drivers are switched by each from_net in a unique way, or annotate delays and transition times if you seek greater accuracy than the lumped fallback analysis can provide.

Feedback

See Also

- DES-023
- RC-002
- set_annotated_delay
- set_annotated_transition

RC-004

(Warning) Failed to compute C-effective for the timing arc %s (%s%s) %s %s

Description

This message warns you that the cell delay calculation failed to compute the effective capacitance of the detailed RC network driven by a specific timing arc, so a lumped capacitance is being used to compute the cell delay. If the library data for the total or zero capacitance is unphysical, the RC-008 warning message is issued at the end of a timing update to inform you that the min or max bounds on correct results cannot be guaranteed. When the RC-004 message is issued, delta delay on the stage is not guaranteed to be conservative.

Reasons for this failure fall into three classes: library-related, parasitics-related, and design-related. The following sections describe each type of problem and possible solutions.

Library-Related Problems

One of the following messages is appended to this warning to explain the library-related reason for the C_effective failure:

- "because the library data indicates a non-positive drive resistance"

  This message is appended if the cell delay does not increase with increasing output load capacitance. This condition can be caused by extrapolating too far outside the library table, or by problems in the table itself.

  Solution: Check the timing arc on a lumped load using the *set_load* and *report_delay_calculation* commands; you might have to annotate delays and transition times until the library data can be fixed by the library vendor. Typically, extrapolations disappear when buffer trees are applied to large fanout networks.

- "because the library data is inconsistent with a linear-driver model"

  This message is appended if the parameters of the linear-driver model cannot be determined for this timing arc and/or RC network. Usually the trip-point variables have

not been set correctly, or the library data is artificial. If generic_cmos library models are being used, ensure that the later slew trip-point is the same as the delay trip-point.

Solution: Double-check the settings of the RC delay-calculation thresholds using attributes or the *report_driver_model* command. If the thresholds are correct, then there is a problem with the library data. If you have access to the library source, ensure that any generic_cmos library models present are used correctly (the later slew trip-point must be the same as the delay trip-point). If nonlinear delay models (a.k.a. tables) are used, confirm that the data was derived from transistor simulation with sufficient accuracy; sometimes libraries are characterized with insufficient accuracy or the data has been manually manipulated in some way.

Parasitics-Related Problems

One of the following messages is appended to this warning to explain the parasitics-related reason for the C_effective failure:

- "because C_total is less than or equal to zero"

  This message is appended if the total capacitance of the RC network is not positive, so that there is no way to determine an effective capacitance.

  Solution: Check the network using *report_net -connections -verbose* and correct the parasitics file if necessary.

- "because the RC network has an invalid reduced-order model"

  This message is appended usually if the annotated connectivity does not match the logical connectivity; for example, if there is an unconnected pin in the design.

  Solution: Look for earlier *link_design* (LNK) warnings pertaining to the problematic net. In rarer situations, there might be a non-positive resistive or capacitive path to ground. Check the network with *report_net -connections -verbose* and correct the parasitics file if necessary.

- "because the RC network has an invalid pole-residue model"

  This message is appended if the network has poles and residues that do not generate a converging waveform. Usually this is caused by problems in the network definition has problems.

  Solution: Check the network with *report_net -connections -verbose* and correct the parasitics file if necessary. This reason applies only to pi-models (for example, RSPF and RNETs in SPEF).

Feedback

Design-Related Problems

The following message is appended to this warning to explain the design-related reason for the C_effective failure:

- "because the from_pin is unconnected"

  This message is appended if a driving arc on a multi-driven network has an unconnected from_pin. In this case, there is no way of knowing the behavior of that arc relative to the other driving arcs of the network; this will prevent RC cell delay calculation from being performed. In this case, you should receive a LNK-022 link warning message for the unconnected pin, this RC-004 warning message, and a RC-007 multidrive warning message.

  Solution: Connect the from_pin or use commands *set_case_analysis* or *set_disable_timing* to fully qualify the unconnected arc.

Timing Arc Notation

The warning message describes the timing arc in the following format:

```
library_cell cell_instance_name/from_pin --> to_pin (sense_direction
 sense_type_unateness)
```

If the timing arc goes through a port with a driving cell, then the message shows the name of the port and the direction (min/max rising/falling). To see more information about the driving cells set on the port, use the *report_port -drive* command.

See Also

- report_delay_calculation
- report_driver_model
- report_net
- set_annotated_delay
- set_annotated_transition
- set_load
- RC-008

RC-005

(warning) Failed to compute the %s RC network delay from the pin '%s' to the pin '%s' in the network '%s'.

Feedback

Description

The RC network delay for the specified timing arc could not be computed. Common reasons for this are as follows:

- Unsupported multidrive scenarios

  Support for RC networks with multiple strong drivers is currently limited to the case where all drivers are wired in parallel. Thus, if a from_pin on a driver connected to a network does not connect to a from_pin on all other drivers, PrimeTime cannot perform RC delay calculation.

  Solution: Directly annotate the delays and slews.

- Networks without timing arcs

  You can define networks that have only driver pins or only load pins. If no pins are bidirectional, PrimeTime cannot perform RC delay calculation. You receive this warning message if you attempt to report from or to one of these pins.

- Extremely under-driven networks

  Networks that are extremely large for their drivers might not converge to one or more RC delay calculation thresholds. This sometimes occurs before layout for nets (for example, clock trees) when buffer insertion has not yet been performed.

  Solution: Either adjust the RC threshold variables or directly annotate the delays and slews.

- Incompatible voltage swings

  If the driver and load assume different voltage-swings, it is possible that the load waveform trip-point voltages are not sufficiently covered by the driver voltage-swing.

  Solution: Verify whether the voltage-swing differences are valid. If so, different library trip-points must be used to ensure sufficient coverage. If the voltage-swing differences are invalid, then the design must be fixed. Another common cause of this problem is using a library without a default operating condition; when this occurs one can either fix the library or use the *set_operating_conditions* command on the affected cells. You can see what trip-points are provided by libraries for the delay calculation by using the *report_delay_calculation -thresholds* command, or you can examine the threshold information for a specific library by using the *report_lib* command.

What Next

Check the network for the previously-described conditions, and follow the suggested solutions.

Feedback

See Also

- report_delay_calculation
- report_lib
- set_annotated_transition
- set_annotated_delay
- set_operating_conditions

RC-006

(warning) The current wire load mode is %s; 'enclosed' mode is used instead to complete parasitics.

Description

You receive this message if you execute *complete_net_parasitics* or *read_parasitics -complete_with* and the wire load mode is not set or is set to *segmented*. The only allowed wire load modes for completion of parasitics are *top* or *enclosed*. This message warns you that the *enclosed* mode is being used.

What Next

If it is acceptable to you for the *enclosed* wire load mode to be used to complete net parasitics, no action is required on your part. Otherwise, perform the following steps:

1. Set the mode to *top* by using the *set_wire_load_mode* command.
2. Remove the parasitics by using the *remove_annotated_parasitics* command.
3. Read all the parasitics that were read before the first completion by using the *read_parasitics* command.
4. Complete the parasitics by using the *complete_net_parasitics* or *read_parasitics -complete_with* command.

See Also

- complete_net_parasitics
- read_parasitics
- remove_annotated_parasitics
- set_wire_load_mode

Feedback

RC-007

(warning) Failed to compute C-effective for the %s multidriven net \'%s\' driven by cell arcs controlled by the from_net \'%s\'

Description

This message warns you that the cell delay calculation failed to compute the effective capacitance of the detailed RC network driven by a specific set of timing arcs, so the total capacitance is being used. Reasons for this failure fall into two classes, library-related and parasitics-related. For information about these, see the man page for the RC-004 warning message.

Another multidrive-specific reason for failure could be that the collective action of multiple drivers causes the output waveform to switch faster than the library delay returned for zero output capacitance. This is a fundamental limitation of using gate-level models in multidrive analysis. When this situation occurs, PrimeTime uses driver models with zero load to preserve the max bound on timing results. Note that there is no adequate fallback for preserving the min bound. For more information, see the man page for the RC-008 warning message.

What Next

Validate the driver arcs in question with lumped output capacitances; use a value equal to the total capacitance of the multidriven net divided by the number of strong drivers. Also, detect any multidriven networks that have large input skew, such that a driver output pin transitions before its input pin does. If the output switches faster than the library delay with zero load, use annotated delays and slews from simulation when high accuracy is needed.

See Also

- RC-004
- RC-005
- RC-008

RC-008

(warning) The type of RC delay calculation problems that have occurred prevents the %s results from bounding the correct values.

Description

When RC delay calculation fails, PrimeTime performs an analysis to determine whether the choice of fallback value will continue to preserve the reported min and max bounds

on the correct value. This message is displayed when the specified bounds cannot be guaranteed.

The most common cause of this situation is a library table extrapolation that returns a negative slew; in that case, a zero delay and zero slew are propagated and the min-max bounds cannot be guaranteed.

Another cause of this situation is a multidriven network that switches faster than the library delay returned for zero output capacitance. If this occurs during min analysis, there is no way to guarantee that propagating a zero delay and zero slew preserves the min bound.

What Next

Fix the library or change the design to avoid library extrapolations. If you have a multidriven network that is failing delay calculation with drivers that can have negative delay, use annotated delays and slews from simulation to obtain a valid min bound.

See Also

- RC-004
- RC-005
- RC-007

RC-009

(Warning) The drive-resistance for the timing arc %s (%s%s) is much less than the network impedance to ground; PrimeTime has adjusted the drive-resistance to improve accuracy.

Description

PrimeTime builds a driver model from library data in order to perform RC delay calculation. The driver model consists of a voltage ramp in series with a resistor; the resistor helps smooth out the voltage ramp so that the resulting driver waveform has similar curvature to that of an actual transistor driver. When the drive resistor is much less than the impedance of the network to ground, the smoothing effect is reduced, causing RC delay calculation to be potentially inaccurate. This condition can occur when a very strong driver is connected to a very resistive network. This condition does not arise out of a problem with library data.

When this condition occurs, PrimeTime adjusts the drive resistance to improve accuracy; however, note that even with this adjustment the resulting accuracy might be insufficient. By default, extra pessimism is sought in min analysis mode by not using slew-degradation.

If you wish to turn on slew degradation in min analysis mode, set the *rc_degrade_min_slew_when_rd_less_than_rnet* shell variable to *true*.

Feedback

Also by default, PrimeTime issues the RC-009 message only for the subset of these conditions where net-delays are greater than driver transition times. This is because these net delays have depended upon the portion of the driver waveform most affected by drive resistance, namely that near and beyond the later slew trip point.

If you wish to see the RC-009 message whenever PrimeTime overrides the drive resistance (i.e. without the just-mentioned filtering), set the *rc_filter_rd_less_than_rnet* shell variable to *false*.

With some designs you may get flooded with RC-009 messages. This can occur for two reasons.

The first is that PrimeTime uses a threshold parameter to determine when to override the drive-resistance, and the default value assumes well-distributed RC extraction (i.e. that very resistive nets are extracted with many RC segments). As a rule of thumb, there should not be more than 100 ohms per segment. If you are using too few RC segments, and you do not wish to increase the extraction resolution, then you can either (a) qualify the tool accuracy in RC-009 mode and suppress the messages with the *suppress_message* command, or (b) change the value of the shell variable *rc_rd_less_than_rnet_threshold* to optimize accuracy for your desired extraction methodology.

The second reason for getting flooded with RC-009 messages is that there may just be a lot of very strong drivers connected to very resistive nets in the design. If this is so, then you can either (a) qualify PrimeTime's accuracy in RC-009 mode and suppress the messages, or (b) annotate delays and slews on the arcs of concern. Another, albeit rarely possible solution is to use weaker or smaller drivers.

To completely shut-off the RC-009 feature, set the *rc_adjust_rd_when_less_than_rnet* shell variable to *false*.

What Next

Simulate the indicated timing arc with the network load to determine whether the accuracy of the PrimeTime result is sufficient. Typically, the number of these conditions in a design is very small, and the resulting delay calculations are overly pessimistic. You can back-annotate the simulator results with SDF, or use a weaker driver and/or less resistive network in the design.

Timing Arc Notation

The warning message describes the timing arc in the following format:

```
library_cell cell_instance_name/from_pin --> to_pin (sense_direction
 sense_type_unateness)
```

If the timing arc goes through a port with a driving cell, then the message shows the name of the port and the direction (min/max rising/falling). To get more information about the driving cells set on the port, use the *report_port -drive* command.

Feedback

See Also

- read_sdf
- report_delay_calculation
- report_driver_model
- set_annotated_delay
- set_annotated_transition
- suppress_message
- rc_adjust_rd_when_less_than_rnet
- rc_degrade_min_slew_when_rd_less_than_rnet
- rc_filter_rd_less_than_rnet
- rc_rd_less_than_rnet_threshold

RC-010

(Warning) Fast multi-drive analysis is being used for the multi-driven net \'%s\' driven by cell arcs controlled with the from_net \'%s\' [#drivers=%d, #loads=%d, arcs%smatch, opconds%smatch; r/f spreads: slew=%g/%g, skew=%g/%g]

Description

This message warns you that an approximate analysis technique is being applied to the specified multidrive scenario. This fast multidrive analysis can reduce runtime by many orders of magnitude for massively multidriven networks. However, the analysis assumes that all driver timing arcs, operating conditions, input slews, and input skews are identical. The analysis also assumes the effective capacitance is the same for all drivers.

This analysis mode is activated when the number of strong (non-tristate) drivers on a net exceeds 9.

Multidriven networks act as strong aggressors and weak victims, due to their high drive strength and distributed network characteristics.

Fast multidrive analysis considers signal integrity effects as follows:

- Delta-delay victim analysis on the multidriven net is skipped.
- Noise victim analysis on the multidriven net is performed.
- Aggressor effects of the multidriven net on neighboring nets are computed.

Feedback

What Next

To yield reasonably accurate results, ensure that the disparity in driver characteristics is sufficiently small. The spreads in operating conditions and input slews should cause small spreads in output delay and output slew. The spread in input skews should be small as compared to the delays through the network.

If the accuracy of this analysis is insufficient, you can either shut this feature off or annotate delays and slews onto the network. Note that full-accuracy analysis of multidriven nets scales as the product of #drivers x #loads.

MESSAGE NOTATION

This warning message includes some useful information about the multidrive scenario to help you decide whether fast multidrive analysis is appropriate. This information includes the number of drivers, the number of loads, whether the driver library timing arcs all match, whether the driver operating conditions all match, and the rise/fall spreads in input slew and input skew (in library units).

RC-011

(Warning) An extrapolation exceeding %s of the library characterization range has been detected. The delay calculation accuracy may be affected. %s (%s%s) %s

Description

This message occurs when RC delay-calculation is attempted using slew or load that is much larger than the maximum library slew or load indices of a cell or a pin, or much smaller than the minimum library slew or load indices of a cell or a pin. Extrapolations can cause inaccurate and even unphysical data;

Presently this message is only issued when Composite Current-Source (CCS) driver modeling is used.

For driver slews, driver loads and receiver loads that exceed the maximum library index by more than 10%, delay calculation uses the last library index incremented by 10%, and the RC-011 message is issued.

For receiver slews that exceed the maximum library index by more than 10%, delay calculation uses the last library index incremented by 10%. For these cases, the RC-011 messages are not issued since they have minimum or no impact on timing results, if the related driver slew RC-011 messages are addressed.

For slews or loads that are below the minimum library index by more than 80%, delay calculation uses the first library index decremented by 80%, and RC-011 messages are issued.

Feedback

What Next

The timing arc and pin should be characterized with enough capacitance and slew indices to cover the design, or the design should be changed to stay within the library slew and capacitance characterization ranges.

The following guidelines can be used to address RC-011 messages:

- Characterizing Design Rule Constraints

  The max_transition pin attributes are normally present on the input and output pins of library cells. For input pins, the max_transition attribute value should not exceed the maximum slew index in the nonlinear delay model (NLDM) and Composite Current Source (CCS) driver and CCS receiver_capacitance2 tables. The lowest value of the maximum slew index between the NLDM and CCS tables should be used as a reference. The tables used as reference are for the rising and falling timing arcs from the relevant input pin for which the max_transition attribute is being characterized. You should take both the arc-based and pin-based tables into account.

  The max_capacitance pin attributes are normally present on the output pins of library cells. For output pins, the max_capacitance attribute value should not exceed the maximum load index in the NLDM and CCS driver as well as CCS receiver_capacitance1 and receiver_capacitance2 tables. You should use the lowest value of the maximum load index between the NLDM and CCS tables as a reference. The tables used as reference are for the rising and falling timing arcs to the relevant output pin for which the max_capacitance attribute is being characterized. You should take both the arc-based and pin-based tables into account.

- Fixing RC-011 Warning Messages

  If the libraries used in the design follow the guidelines outlined in the Guidelines for Characterizing Design Rule Constraints section, all RC-011 messages are addressed by fixing the max_transition and max_capacitance violations reported by the report_constraint command. If the libraries are not compliant with these guidelines, you should consider RC-011 warning messages to be important. You need to address the DRCs in the design to fix these warnings.

Timing Arc Notation

The warning message describes the timing arc or pin in the following format:

```
lib_cell_pin cell_pin_instance_name/from_pin -->
to_pin (sense_direction sense_type_unateness)
```

If the timing arc goes through a port with a driving cell, then the message shows the name of the port and the direction (min/max rising/falling). To see more information about the driving cells set on the port, use the *report_port -drive* command.

Feedback

See Also

- report_delay_calculation
- report_net

RC-012

(Warning) %s extrapolation exceeding %s outside the library characterization range has been detected. Accuracy may be affected %s (%s%s) %s

Description

This message occurs when nonlinear delay model (NLDM) based delay calculation is attempted using slew or load that is larger than the maximum library slew or load indices of a cell or a pin, or smaller than the minimum library slew or load indices of a cell or a pin. Extrapolations can cause inaccurate and even unphysical result;

For cell input slews or output loads that exceed the maximum library slew or load indices, delay calculation extrapolates the output delay based on output delay values at two closest slew or load indices and RC-012 message is issued.

What Next

The timing arc and pin should be characterized with enough capacitance and slew indices to cover the design, or the design should be changed to stay within the library slew and capacitance characterization ranges.

The following guidelines can be used to address RC-012 messages:

- Characterizing Design Rule Constraints

  The max_transition pin attributes are normally present on the input and output pins of library cells. For input pins, the max_transition attribute value should not exceed the maximum slew index in the nonlinear delay model (NLDM) tables. The lowest value of the maximum slew index between the NLDM tables should be used as a reference. The tables used as reference are for the rising and falling timing arcs from the relevant input pin for which the max_transition attribute is being characterized. You should take both the arc-based and pin-based tables into account.

  The max_capacitance pin attributes are normally present on the output pins of library cells. For output pins, the max_capacitance attribute value should not exceed the maximum load index in the NLDM tables. You should use the lowest value of the maximum load index between the NLDM tables as a reference. The tables used as reference are for the rising and falling timing arcs to the relevant output pin for which the max_capacitance attribute is being characterized. You should take both the arc-based and pin-based tables into account.

- Fixing RC-012 Warning Messages

Feedback

If the libraries used in the design follow the guidelines outlined in the Guidelines for Characterizing Design Rule Constraints section, all RC-012 messages are addressed by fixing the max_transition and max_capacitance violations reported by the report_constraint command. If the libraries are not compliant with these guidelines, you should consider RC-011 warning messages to be important. You need to address the DRCs in the design to fix these warnings.

Timing Arc Notation

The warning message describes the timing arc or pin in the following format:

```
lib_cell_pin cell_pin_instance_name/from_pin -->
to_pin (sense_direction sense_type_unateness)
```

See Also

- report_delay_calculation
- report_net
- RC-011

RC-013

(warning) Detected abnormal LVF values. LVF values will be ignored for this arc. (%s)

Description

In the process of LVF lookup, abnormal values have been observed. The LVF data will be ignored for this arc.

What Next

Check the LVF tables.

See Also

- timing_pocvm_enable_analysis

RC-104

(Warning) Failed to compute the cell timing arc %s (%s%s) %s %s

Description

This message warns you that the RC delay calculation based on composite current source (CCS) data failed to compute for a specific timing arc, so a lumped capacitance is being used to compute the cell delay. To be conservative, the total capacitance of the RC

network is used in max analysis mode, and zero capacitance in min analysis mode. If the delay and/or slew library data for the total or zero capacitance is unphysical, the warning message RC-008 is issued at the end of a timing update to inform you that the min and/or max bounds on correct results cannot be guaranteed. When the RC-104 message is issued, delta delay on the stage is not guaranteed to be conservative.

This is the CCS version of the RC-004 warning message.

Reasons for this failure fall into three classes: library-related, parasitics-related, and design-related. The following sections describe each type of issue and possible solutions.

Library-Related Problems

One of the following messages is appended to this warning to explain the library-related reason for the delay-calculation failure:

- "because there is a problem with the driver's CCS data"

  This message is appended if the delay-calculation does not produce a full-swing transition on all the netlist pins, or if the threshold voltages for such pins are not all reached. This condition can be caused by the final voltage level that is obtained from integrating the library CCS current data does not get close to the voltage set on the pins, or the final voltage does not drive the net to the second slew trip point of a load pin, or data extrapolating too far outside the library table, or by problems in the table itself.

  Solution: Check the timing arc on a lumped load using the *set_load* and *report_delay_calculation* commands; you might have to annotate delays and transition times until the library data can be fixed by the library vendor. Typically, extrapolations disappear when buffer trees are applied to large fanout networks.

  Solution: Double-check the settings of the RC delay-calculation thresholds using attributes or the *report_delay_calculation -thresholds* command; If the thresholds are correct, then there is a problem with the library data.

Parasitics-Related Problems

One of the following messages is appended to this warning to explain the parasitics-related reason for the delay-calculation failure:

- "because C_total is less than or equal to zero"

  This message is appended if the total capacitance of the RC network is not positive, so that there is no way to perform a valid delay calculation.

  Solution: Check the network using *report_net -connections -verbose* and correct the parasitics file if necessary.

- "because the RC network has an invalid reduced-order model"

This message is appended usually if the annotated connectivity does not match the logical connectivity; for example, if there is an unconnected pin in the design.

Solution: Look for earlier *link_design* (LNK) warnings pertaining to the problematic net. In rarer situations, there might be a non-positive resistive and/or capacitive path to ground. Check the network with *report_net -connections -verbose* and correct the parasitics file if necessary.

Design-Related Problems

One of the following messages is appended to this warning to explain the design-related reason for the delay-calculation failure:

- "because some load-pin thresholds are not covered"

  This message is appended if load pin delay or slew threshold is outside the range of the driver output voltage.

  Solution: Double-check the load pin thresholds. For example, you can run *report_delay_calculation -thresholds* command.

Timing Arc Notation

The warning message describes the timing arc in the following format:

```
library_cell cell_instance_name/from_pin --> to_pin (sense_direction
 sense_type_unateness)
```

If the timing arc goes through a port with a driving cell, then the message shows the name of the port and the direction (min/max rising/falling). To see more information about the driving cells set on the port, use the *report_port -drive* command.

See Also

- report_delay_calculation
- report_net
- set_annotated_delay
- set_annotated_transition
- set_load
- RC-004
- RC-008

Feedback

RC-201

(warning) Timing arc %s->%s does not have CCS noise model for accurate waveform analysis.

Description

When waveform propagation analysis is enabled, it is required that the stage driver cell has CCS noise model(s) for its timing arcs in terms of either arc-based or pin-based CCS noise model(s). When such CCS noise model(s) are not present in the library, analysis with desired accuracy cannot be performed.

What Next

Fix the library to ensure that all library cell timing arcs have either arc-based or pin-based CCS noise models.

See Also

- RC-202

RC-202

(Warning) CCS noise model on timing arc %s->%s does not have full rail output swing.

Description

When waveform propagation analysis is enabled, it is required that the stage driver cell has valid CCS noise model(s). This warning message will be issued if the output voltage swing of the CCS noise model(s) related to the affected timing arc does not reach 95% of VDD. This oftentimes is due to CCS noise library characterization issue. You may ignore this message if your cell indeed cannot reach 95% VDD voltage swing.

See Also

- RC-201

RC-203

(warning) Timing arc %s->%s (%s) does not have CCS timing model for accurate waveform analysis.

Description

When waveform propagation analysis is enabled, it is required that the stage driver cell has CCS timing model(s) for its timing arcs. When such CCS timing model(s) are not present in the library, analysis with desired accuracy cannot be performed.

Feedback

What Next

Fix the library to ensure that all library cell timing arcs have CCS timing models.

See Also

- RC-201

RC-204

(warning) Constraint arc %s->%s for %s does not have CCS noise model at pins for constraint evaluation with waveform distortion.

Description

When constraint evaluation with waveform is enabled, it is required that the pins for constraint arc have CCS noise model(s) to consider the impact from the waveform distortion. When such CCS noise model(s) are not present in the library, analysis with desired accuracy cannot be performed.

What Next

Fix the library to ensure that all library cell constraint arcs have CCS noise models.

RC-205

(Warning) CCS noise model on timing arc %s->%s %s

Description

When waveform propagation analysis is enabled, it is required that the stage driver cell has valid CCS noise model(s). This warning message will be issued if the model does not pass certain requirement for accuracy, such as NLDM, CCST correlation check, and signal level check.

Reasons for this failure fall into three classes: library-related, and design-related. The following sections describe each type of problem and possible solutions.

Library-Related Problems

does not correlate with timing model

This warning message will be issued if the CCS noise model(s) does not correlate with timing model such as CCST and NLDM. CCSN noise modeling uses equivalent circuit model which sometimes may not correlate with measured model well.

Feedback

is not supported

This warning message will be issued if CCS noise model(s) has features not supported yet, such as pass-gate and model with different input and output voltage signal level.

Design-Related Problems

input waveform has a very low voltage

This indicates the previous driver has a low voltage that is unable to trigger high trip voltage of the input pin. PrimeTime will automatically correct the voltage and proceed waveform propagating. Please check if the previous stage has an RC-104 message and and correct the cell power supply.

See Also

- RC-104
- RC-201
- RC-202

RC-206

(Warning) Unable to derive advanced receiver modeling for pin %s. Accuracy may be affected.

Description

This warning reports there's an issue of advanced receiver modeling of the pin. Advanced receiver is enabeld when delay_calc_enhanced_ccsn_waveform_analysis set to true. When this happens PrimeTime will fallback to basic single pin capacitance receiver model .

Reason for this issue is incorrect scaling library group formation.

See Also

- rc_receiver_enable_error_reporting

RULE

RULE-002

(error) Rule '%s' is already defined.

Feedback

Description

The rule name is in use by an existing rule.

What Next

Specify a valid rule name that is not already in use.

RULE-004

(error) Rule '%s' is not defined.

Description

The specified rule cannot be found.

What Next

Specify a valid rule name.

RULE-006

(error) User-defined rule name '%s' does not begin with 'UDEF_'.

Description

User-defined rules must have names beginning with 'UDEF_'. For example, 'UDEF_0345'.

What Next

Specify a valid name for the user-defined rule.

RULE-007

(error) Parameter name '%s' was specified more than once.

Description

The list of parameter names for a rule must not contain any duplicates.

What Next

Specify unique parameter names within a rule.

RULE-008

(error) Parameter name '%s' contains invalid characters.

Feedback

Description

Parameter names should contain only alphanumeric characters plus '_'.

What Next

Specify parameter names that contain valid characters.

RULE-012

(error) Checker procedure '%s' does not exist.

Description

The checker procedure associated with a user-defined rule must be a valid Tcl procedure.

What Next

Specify the correct checker procedure.

SCL

SCL-200

(information) License server is unreachable (Network connectivity issue or Server down). Lost licenses. Your job is suspended during reconnect.

Description

This message is printed when the application has lost connection to the license server. This could be due to a server restart or a network interruption between application and the license server.

At this point the application processing is suspended until the original set of licenses are all re-acquired.

See Also

- get_license
- SCL-203

SCL-203

(information) Reacquired license after server disconnect.

Feedback

Description

This message is printed when the connection between application and the license server is reestablished after an *SCL-200* message and the tool has re-acquired the licenses that it lost due to disconnection.

See Also

- get_license
- SCL-200

SCOPE

SCOPE-002

(error) File '%s' is not the expected format of binary scope data file.

Description

You receive this message to inform you that the file specified to provide block-level scope data is not recoganized by PrimeTime as the expected binary format.

What Next

Please make sure the file is the right format and contains the scope data.

SCOPE-003

(information) Loading scope data from file '%s'.

Description

You receive this message to inform you that the scope constraint data used to do scope check for the specified blocks are loaded from the given file.

What Next

No user action is needed if the file contains the intended scope data.

SCOPE-004

(information) Checking the hierarchical scope of block '%s' as an %s.

Feedback

Description

You receive this message to inform you that the scope checks will be performed for the cell by treating the cell as the indicated model type.

What Next

No user action is needed.

SCOPE-005

(information) Overwriting existing file '%s'...

Description

You receive this message to inform you that the scope data captured for the specified block is being written into the indicated file. Since the file already exists, so the original data in the file will be overwritten.

What Next

No user action is needed.

SCOPE-006

(wanring) Scope data for block '%s' as %s model and scenario '%s' already exists in the output file '%s', replace the existing data.

Description

You receive this message to inform you that the scope data captured for the specified block as the indicated model type and scenario name already present in the indicated file, and the existind data will be overwritten and replaced with the newly captured scope data.

What Next

No user action is needed.

SCOPE-007

(error) No valid cell instances to perform the scope check.

Description

You received this message because there are no valid cell instance to perform the scope check.

Feedback

What Next

Please make sure the cell instances are specified correctly.

SCOPE-008

(error) No scope data found in file '%s'.

Description

You received this message because there are no valid scope data found in the given file.

What Next

Please make sure the file contains proper scope data to perform check.

SCOPE-009

(error) No scope data defined in file '%s' to check for block/cell '%s' as %s model in scenario '%s'.

Description

You received this message because there are no valid scope data found in the specified file for the given block and scenario.

What Next

Please make sure the file contains proper scope data to perform check.

SCOPE-010

(error) Cannot find cell instance named '%s' in the design.

Description

You received this message because there are no cells found in the current design with the specified name to do scope check.

What Next

Please make sure the cell names are correct.

SCOPE-011

(error) Cannot determine the model type for cell instance '%s'.

Feedback

Description

You received this message because PrimeTime cannot determine the exact timing model type for the specified cell/block instance and therefore cannot perform correct scope check for it.

What Next

Please make sure the cell names are correct.

SCOPE-012

(warning) Cannot find any pin named '%s' within the cell/block '%s' at top-level.

Description

You received this message because PrimeTime cannot find a pin as named within the hierarchy of the cell/block instance to do scope check for it. This can happen when the cell name is wrong, or the indicated pin is not contained in the model for the original block.

What Next

Please make sure the cell names are correct, and the pin present in the model for the original block.

SCOPE-013

(information) No scope constraints defined for the input data signals of cell or block '%s'.

Description

You received this message because PrimeTime cannot find any scope information on the data signals of the indicated cell/block and therefore will not perform and scope checks for them. This can happen when there is no input data signals on the cell, or the input data signals are ignored when capturing the scope for the block.

What Next

Please check that proper information is captured in the scope file for the block when the model for the block is generated.

SCOPE-014

(wrning) No top-level clocks propagate to pin '%s'.

Feedback

Description

You received this message because PrimeTime cannot find any clocks defined at the top-level propagate to the pin as indicated. This can happen when there are missed clock definitions at top-level or redundant clock definitions at block-level when the model and scope data was generated.

What Next

Please check that clocks are properly defined at both the block and top level.

SCOPE-015

(information) %s.

Description

This is a general informational message to indicate the progress and/or status of the command execution

What Next

No user action is needed.

SCOPE-016

(warning) Ignoring a duplicated instance name for cell/block '%s', scope check for the block is done only once.

Description

This is a warning message because the indicated cell/block instance have been specified multiple times, only one will be checked.

What Next

Please specify a cell instance only once in the -instance option to avoid the the warning message.

SCOPE-017

(warning) %s.

Description

This is a general warning message for some potential siginificant issues found when performing scope checks.

Feedback

What Next

Please check for any problems indicated by the message and verify the design settings and command options to avoid the warning message.

SCOPE-018

(warning) Unexpected %s range %8.4f(min)->%8.4f(max) %s %s, min value is greater than max.

Description

This is a warning message for a situation in which the min bound of a scope range is greater than the max bound, it may be caused by some inproper settings for timing analysis.

What Next

Please check for any setup related issues that may cause the indicated problem and verify/correct the design settings.

SCOPE-019

(error) Cannot check the scope for cell/block instance '%s', it is a black-box and not properly linked.

Description

You received this message because the specified cell/block instance is found to be a black-box in the current design. It is not properly resolved during the design link time.

What Next

Please make sure the library or design source for the named cell is provided and properly linked.

SCOPE-020

(error) %s.

Description

This is to inform the user that the tool has encountered a general error as indicated

What Next

Please make sure the error is fixed and try issue the command again.

Feedback

SCOPE-021

(error) Scope file '%s' is created by %s version of PrimeTime and can no longer be read in for analysis.

Description

You receive this message to inform you that the file specified for PrimeTime to load scope data from is a binary scope file, but created by a certain version of PrimeTime as specified which is no longer being supported by the current version of PrimeTime.

For example, a scope file created by the first beta version of the hierarchical block scope analysis feature for PrimeTime, i.e. 2004.06-Beta3, is not supported by the 2004.06 production and later releases.

However, this is only a special case. In general, scope files will be kept backward compatible. This means a later release of PrimeTime will understand and make use of the scope files created by previous releases of PrimeTime. Therefore, the scope files do not need to be re-generated with each releases of PrimeTime in general.

What Next

Please re-create the scope file with the new version of PrimeTime, so it can be read in for scope checking and analysis.

SDC

SDC-1

(information) Setting sdc_version outside of an SDC file has no effect

Description

You set the *sdc_version* variable outside of the context of an SDC file. In that context, changing the variable has no effect.

What Next

No action necessary.

SDC-2

(warning) SDC version in file (%s) does not match the version you requested\n \tfrom read_sdc (%s). Some constraints and options may not function.

Feedback

Description

The version indicated by the setting of the *sdc_version* variable in your SDC file does not match the version requested by the *read_sdc* command.

What Next

Ensure that you select the correct version when issuing the *read_sdc* command.

SDC-3

(warning) Constraint '%s' is not supported by %s.

Description

Not all Synopsys Design Constraints are supported by all applications. The specified constraint is not supported by the current application, and it is ignored. For example, test constraints are not recognized by PrimeTime. One SDC-3 message is issued per instance of the constraint which is ignored. Then, after *read_sdc* completes, an SDC-4 summary message will tell you how many of each constraint was ignored.

SDC-4

(information) Ignored %d unsupported '%s' constraint%s.

Description

This is a summary message indicating how many instances of a particular constraint were ignored by *read_sdc* because the constraint is unsupported.

SDC-5

(error) Errors reading SDC file:\n \t%s.\n \tUse error_info for more info.

Description

This message is generated by *read_sdc* when an syntax error occurs during the read. The specific error is shown in the text of the message.

What Next

You can use *error_info* to help trace the cause of the error. For example, it might show the file and line number of the syntax error.

Feedback

SDF

SDF-001

(error) SDF version '%s' is not supported. The following SDF versions are supported: '%s'.

Description

The SDF version is not supported.

What Next

Use an SDF version which is supported.

SDF-002

(error) Error in SDF file '%s' near line %d : wrong divider '%s'.

Description

Only dividers '.' and '/' are allowed by SDF.

What Next

Use a supported DIVIDER symbol in SDF.

SDF-003

(warning) No library was found on the search path; time unit '%s' is assumed.

Description

There was no library found on the search path.

What Next

Verify the search path with *list search_path* and verify the link library is under the search path. The link library is specified with *link_library*. Use *link* to verify the design has necessary libraries on the search path. Read the timing file once again after fixing the link errors.

SDF-004

(warning) The library '%s' has no time unit specified, '%s' is assumed.

Feedback

Description

The library has no time unit specified. By default the time unit is nanosecond and time scale is 1. The only valid library time unit for the sdf format are 0.001, 0.01, 0.1, 1, 10, and 100. The time unit is specified in the library with the attributes *time_scale* and *time_unit_name*. For example, a library with timing values in 10 picosecond units is specified with the attributes: *time_scale = 10* and *time_unit_name = ps*. *read_timing* assumes the technology library time unit is 1ns. The time unit in the sdf file is specified with 'timescale' construct.

What Next

If this assumption is incorrect, modify the scale and time unit of the sdf timing file before reading it in the Design Compiler product.

SDF-005

(warning) No library was found on the search path; time unit '%s' is assumed.

Description

There was no library found on the search path.

What Next

Verify the search path with *list search_path* and verify the link library is under the search path. The link library is specified with *link_library*. Use *link* to verify the design has necessary libraries on the search path. Read the timing file once again after fixing the link errors.

SDF-006

(warning) The SDF file contains delays for the design '%s', which is different from the current design '%s'.

Description

The current design and the design that the sdf file was written for are not the same. The 'design' construct in the sdf file contains the name of the design for which the timing file was written. This name should be the same as the *current_design*.

What Next

Verify the sdf file was created for the current design, the 'design' construct in the sdf file must contain the name of the current design. Check the usage of the *read_timing* command, you might need to use the *-path* option.

Feedback

SDF-007

(error) There is '%s'.

Description

There is no current design. SDF file cannot be read if the design is not previously read.

What Next

Prior to reading the SDF file, you must read the netlist.

SDF-008

(error) Error in SDF file %s Line %d: %s at or near token '%s'.

Description

A syntax error has been found when reading the SDF file.

What Next

Fix the SDF file at the given line and reload the SDF.

SDF-009

(error) Cannot find hierarchical path '%s'.

Description

Cannot find the specify hierarchical path to which SDF delays must be annotated.

What Next

Find the correct hierarchical path.

SDF-010

(error) Hierarchical path '%s' corresponds to design '%s', and not to design '%s' as you specified with option -design.

Description

The specified hierarchical path, to which SDF delays should be annotated, corresponds to a design whose name is different from the -design option you specified.

Feedback

What Next

Find the correct design corresponding to the given hierarchical path, or do not specify the design name and the tool will derive it.

SDF-011

(error) Cannot find instance '%s'. All delays related to that instance are ignored.

Description

This instance specified in the SDF file cannot be found in the current design.

What Next

Check that the SDF file is correct and corresponds to the current design.

SDF-012

(warning) Library cell '%s' is not used in the current design.

Description

This library cell specified in the SDF file cannot be found in the current library.

What Next

Check that the SDF file is correct and corresponds to the current design.

SDF-013

(warning) SDF variables '%s' are obsolete. Please use option 'read_sdf %s'.

Description

The Design Compiler sdfin_* variables are obsolete in PrimeTime. Use the equivalent command line options of command 'read_sdf':

sdfin_top_instance_name <path_name> : read_sdf -strip_path <path_name>

sdfin_fall_net_delay_type <minimum|typical|maximum> : read_sdf -type <sdf_type>
sdfin_rise_net_delay_type <minimum|typical|maximum> : read_sdf -type <sdf_type>
sdfin_fall_cell_delay_type <minimum|typical|maximum> : read_sdf -type <sdf_type>
sdfin_rise_cell_delay_type <minimum|typical|maximum> : read_sdf -type <sdf_type>

The folowing sdfin_* variables are obsolete:

sdfin_min_rise_net_delay sdfin_min_fall_net_delay sdfin_min_rise_cell_delay sdfin_min_fall_cell_delay

Feedback

What Next

Remove the use of sdfin_* variable and add the equivalent command line option to the read_sdf command.

SDF-014

(warning) SDF variables '%s' are obsolete.

Description

The Design Compiler sdfin_* variables are obsolete in PrimeTime. Use the equivalent command line options of command 'read_sdf':

sdfin_top_instance_name <path_name> : read_sdf -strip_path <path_name>

sdfin_fall_net_delay_type <minimum|typical|maximum> : read_sdf -sdf_type <type>
sdfin_rise_net_delay_type <minimum|typical|maximum> : read_sdf -sdf_type <type>
sdfin_fall_cell_delay_type <minimum|typical|maximum> : read_sdf -sdf_type <type>
sdfin_rise_cell_delay_type <minimum|typical|maximum> : read_sdf -sdf_type <type>

The folowing sdfin_* variables are obsolete:

sdfin_min_rise_net_delay sdfin_min_fall_net_delay sdfin_min_rise_cell_delay sdfin_min_fall_cell_delay

What Next

Remove the use of sdfin_* variable and add the equivalent command line option to the read_sdf command.

SDF-015

(error) Cannot open file '%s'.

Description

The file name provided to *read_sdf* or *write_sdf* cannot be opened.

What Next

Validate that the file name is correct. Or, for writing SDF, check that the directory where you want to write the SDF is opened for writing.

SDF-016

(warning) Timing check arc to internal pin '%s' of libcell '%s' is not compressed in SDF file.

Feedback

Description

The timing check arc is not compressed when both from pin and to pin are internal pins. Also, timing check arc from or to internal pin for NOCHANGE is not compressed.

What Next

This is the limitation of current implementation of SDF export.

SDF-017

(error) write_constraints option '%s' not supported in PrimeTime.

Description

The given option used for write_constraints is not supported in PrimeTime.

What Next

Check in the PrimeTime User Guide the options supported for write_sdf_constraints.

SDF-018

(warning) There is no delay to write in SDF.

Description

Because there are no delays to write in the SDF, the SDF file is not created.

What Next

The most common reason for not having any delay written in SDF is because the design was not linked correctly and have only black boxes.

SDF-019

(warning) The %s of cell `%s` from `%s` to `%s` could not be annotated.

Description

There are more delay arcs or timing check information in SDF than what can be annotated based on the library timing arcs and timing checks. For example, if both rise and fall values exist in SDF for a timing arc which only has a rise value, then the SDF reader will warn that the fall value from SDF cannot be annotated. Another example is when the timing check in the library has data edge and SDF does not, then only the appropriate edge will be annotated.

Note: The timing check portion of this warning is suppressed when reading SDF version one.

Feedback

What Next

Your SDF file can be incorrect, or your library is missing some timing arcs or has incorrect timing checks to match the transition delays specified in SDF.

SDF-020

(error) Unable to open SDF mapping file %s.

Description

PrimeTime was unable to open the SDF mapping file for reading.

What Next

Check whether the SDF mapping file exists and has read permissions.

SDF-021

(error) Error reading SDF mapping file %s. Mapping info for only %d cells read.

Description

The SDF mapping file has improper syntax. Mapping information for cells which was specified before the cell at which error occured will be stored and used while mapping their instances, rest of the file is not read.

What Next

Check whether the SDF mapping file has correct syntax.

SDF-022

(error) Unsupported operator used in an expression in SDF mapping file.

Description

SDF mapping file contains an unsupported operator.

What Next

See the list of supported operators in the SDF mapping file syntax, and re-write the expression using only supported operators.

SDF-023

(warning) Arc corresponding to label %s on library cell %s not found. Functions that access delays with this label will return 0.0.

Feedback

Description

No arc corresponding to the label exists.

What Next

Check the SDF mapping file.

SDF-024

(warning) No library cell named %s found.

Description

SDF mapping file had mapping information for a cell, which was not found in any of the loaded libraries.

What Next

Check the SDF mapping file and correct the library cell name. If the library cell name is correct, ensure that you have loaded the library prior to using the "write_sdf -map" command.

SDF-025

(error) Value '%d' of level is not greater or equal to 1.

Description

The level of hierarchy must be greater than or equal to 1. Level 1 means to include arcs that start or end at the level of the top design or the instance specified by *-instance*. Level *N* means to include arcs that start or end at the level of the top design or the instance specified with *-instance* and at all levels of hierarchy up to *N*.

What Next

If you want to include arcs at all levels of the circuit, do not use *-level* option. If you want only arcs immediately inside a hierarchical cell, use *-level* 1 *-instance* <cell>.

SDF-026

(warning) The SDF file is version 3.0. Current SDF-3.0 supported constructs are: %s.

Description

Currently read_sdf has a limited support for SDF 3.0. Only the specified subset of SDF 3.0 constructs are supported.

Feedback

What Next

Remove the unsupported SDF 3.0 constructs to avoid any syntax error.

SDF-027

(warning) '%s' is not supported with the -include option for SDF version '%s'

Description

You received this message because you executed the *write_sdf* command and specified the SDF constructs *SETUPHOLD* and/or *RECREM* with the -include option. In addition you specified a version using the -version option or alternatively you specified no version and the default of version 2.1 was specified for you. The SDF version you specified does not support *SETUPHOLD* and/or *RECREM*.

What Next

Reexecute *write_sdf* and specify a valid version for the constructs as follows *SETUPHOLD*, version 2.1 , version 3.0 *RECREM*, version 3.0

SDF-028

(warning) No delays were found for either ABSOLUTE or INCREMENT

Description

You received this message because no delays were found after either ABSOLUTE or INCREMENT in the SDF file read in by *read_sdf*. This is non spec compliant SDF but the error is ignored and the remainder of the file is read in as normal.

What Next

Check that your SDF writer has not ommitted any delays which should have appeared in the empty space after either ABSOULTE or INCREMENT .

SDF-029

(warning) Primetime may not be able to fully annotate SDF generated with the -no_internal_pins option

Description

You received this message because you wrote SDF using write_sdf with the -no_internal_pins option. Primetime does not support the reading of SDF generated with the -no_internal_pins option.

Feedback

What Next

To generate SDF which can be read back in to primetime, use write_sdf without the -no_internal_pin option. If you wish to exclude just internal pins which are checkpins from the SDF, use the -exclude checkpins option, Primetime will be able to fully annotate this SDF.

SDF-030

(Warning) Port construct being used.

Description

The port construct is being used instead of the interconnect construct at the reported locations.

SDF-031

(Information) Using one port statement for %d net arcs at pin %s.

Description

The port construct is being used instead of the interconnect construct at the reported locations.

SDF-032

(Information) Cell delay values of cells %s are being aligned.

Description

The cell delay values of the reported cells are being aligned.

SDF-033

(warning) Both port and interconnect statements have been used at pin %s.

Description

The net arcs to the specified pin have been written out using both port and interconnect statements. It was not possible to just use a port construct as the net arc delay spread was too great. If cell alignment has been enabled, it will not succeed at this cell pin due to combined port and interconnect usage.

Feedback

What Next

To use only port statements, the *sdf_enable_port_threshold* value will have to be raised. For more details regarding port construct usage and the restrictions on clock network parallel buffers collapse, check the man pages for *sdf_enable_port_construct* and *sdf_align_multi_drive_cell_arcs*.

SDF-034

(warning) The %s construct is not supported for %s sdf delay reading mode.

Description

Only net arc delays can be specified in the sdf file in this mode. All delays referring to other constructs will be ignored. The *port* and *interconnect* are the only supported constructs in this mode.

What Next

Read in non-net arc delays using regular read_sdf.

SDF-035

(error) The ABSOLUTE construct is not supported in %s sdf delay reading mode.

Description

Only net arc delays with INCREMENT construct can be specified in the sdf file in this mode. All delays referring to other constructs will be ignored.

What Next

Use INCREMENT construct in this mode.

SDF-036

(warning) The sum of the %s values in the cell '%s' for the arc between pins '%s' and '%s' is negative, which is not allowed. To make it positive, the %s value has been adjusted from %f to %f.

Description

This warning message occurs when the sum of the setup and hold values is negative for a given arc. Note that negative values for either the setup time or hold time are allowed; however, their sum must always be greater than 0.

Feedback

What Next

This is a warning message only. No action is required because the %s time has been automatically adjusted to give a positive sum for the setup and hold times.

SDF-037

(warning) Circular timing arcs were detected in the cell '%s' while writing SDF. The pin '%s' is in the loop. SDF information for the cell may contain errors.

Description

The cell pin has circular timing arcs. A circular timing arc occurs when an inout or output pin is related to itself though other inout or output pins. A change in one pin belonging to a circular timing arc continually loops around. Circular timing arcs do not make sense and are probably mistakes.

When writing SDF, timing information for the pin in a circular timing arc might be incorrectly determined.

What Next

Check the cell library file and verify the questionable circular timing arcs.

SDF-038

(error) The delta_net_delays_only option can only be used when coupling capacitances are read along with parasitics and SI analysis is enabled in PrimeTime.

Description

The delta_net delay option of write_sdf writes the delta delays on the interconnects and therefore coupling capaacitances should be read from the parasitics file and, to annotate delta delays on the nets, SI analysis mode should be enabled.

What Next

Use -keep_capacitive_coupling with read_parasitics and set si_enable_analysis variable to TRUE

SDF-039

(warning) Merged delay values will be used when writing delays of parallel cell arcs.

Description

Multiple parallel cell arcs of the same sense can exist between the same pair of pins. If the variable timing_reduce_parallel_cell_arcs is set to true, delays on these parallel cell arcs

are merged in a bounding manner. write_sdf will write merged delay values for parallel cell arcs.

What Next

To disable merging of parallel cell arcs delays, set timing_reduce_parallel_cell_arcs to false.

See Also

- write_sdf

SDF-041

(error) Setting the value of %s to %s is not allowed.

Description

The passed command argument cannot be used. For example, the delay value between two pins cannot be set to NaN (not a number).

What Next

Check the arguments of the command.

SDF-042

(warning) Timing condition '%s' for libcell '%s' not found in library.

Description

A timing condition in the SDF file cannot be found in the library for the libcell.

What Next

Check that all timing conditions in the SDF file correspond to sdf conditions in the library file.

SDF-043

(error) File '%s' is compressed %d times. The read_sdf cannot read SDF files that are compressed more than once.

Description

The file provided to *read_sdf* is compressed multiple times

Feedback

What Next

Uncompress the file appropriate times

SDF-044

(warning) Overwriting previous delay set on arcs in a parallel set.

Description

The selected arcs belongs to a group of parallel arcs and the value of variable timing_reduce_parallel_cell_arcs is set to true. Despite that the provided delay value will overwrite all previous delays on those arcs and no delay merging in a bounding manner is going to take place. This is happening because the options -from/-to targets the entire group of the parallel arcs.

What Next

To enforce merging with the existing delays on those parallel arcs use option -of_objects instead of the -from/to to specify the arcs. For example "set_annotated_delay -from A -to B" should change to "set_annotated_delay -of_objects [get_timing_arcs -from A -to B]"

See Also

- set_annotated_delay

SDF-045

(warning) Supplied arc is part of a parallel set. Merging with existing delays.

Description

The selected arcs belongs to a group of parallel arcs and the value of variable timing_reduce_parallel_cell_arcs is set to true. The provided delay will be merged with the existing delays in a bounding manner.

What Next

To enforce overwriting the delays use the options -from/to instead of the -of_objects to target the entire set of the parallel arcs. For example "set_annotated_delay -of_objects [get_timing_arcs -from A -to B]" should change to "set_annotated_delay -from A -to B"

See Also

- set_annotated_delay

Feedback

SDF-046

(warning) The SDF file contains multiple instances of INTERCONNECT statements (i.e. net arcs) between pins '%s' and '%s'. This may lead to unexpected behavior during read_sdf command.

Description

This warning message occurs when multiple instances of INTERCONNECT statements between the same set of pins (from and to pins of the net arcs) are detected. The read_sdf command is optimized for maximum efficiency for the case of SDF file without any duplicate or repeat instances of net arcs.

What Next

The occurence of multiple instances of INTERCONNECT statements between the same set of pins may lead to unexpected behavior during read_sdf command. To avoid this possibility, it is recommended to beforehand remove duplicates and uniquify the SDF files.

SDF-047

(error) Option '-objects' requires attribute 'is_write_sdf_object' to be defined by user on cells or nets.

Description

Option *-objects* will only include in the SDF the cell/net instances that have attribute *is_write_sdf_object* set to *true*. This attribute must be defined by the user and set to *true* on the instances he wants to be included in the sdf.

What Next

Create a user defined atrribute with name *is_write_sdf_object* on cell or net and set it to true on the instances you want to be included in the SDF.

Example:

```
define_user_attribute -type boolean -class cell is_write_sdf_object
set_user_attribute [get_cells block1/*] is_write_sdf_object true
write_sdf -objects out.sdf
```

SEC

SEC-0

(error) Software is not licensed for this machine.

Feedback

Description

Could not find a valid matching key in the key file for this feature

What Next

Check to see that the machine hostid, using the machine_id utility provided by Synopsys, matches the hostid in the key file for the feature.

SEC-1

(error) %s

Description

The key file with all of the license information cannot be opened.

What Next

Check directory and file read permissions.

SEC-2

(error) Cannot open key file '%s' or a licensing environment parameter has not been set correctly.

Description

The keyfile cannot be read.

What Next

Check the location of the keyfile to see if a keyfile is present and it is readable.

SEC-3

(error) Encryption file header is corrupt.

SEC-4

(error) Unknown encryption method.

Description

The application is trying to match the encryption with that in the keyfile. The encryption being used is not correct.

Feedback

What Next

Make sure that the executable is not corrupt or has not been changed.

SEC-5

(warning) License for '%s' expires within %2d days.

Description

The license for the listed feature is going to expire within 2 days.

What Next

Contact your Synopsys support representative.

SEC-6

(warning) License for '%s' has expired.

Description

The license for the listed feature has expired.

What Next

Please contact your Synopsys support representative.

SEC-10

(error) Software is not licensed for this machine.

Description

There was a problem matching the key file information to the machine you are trying to run the software on.

Possible causes are bad encryption code and the hostid specified in the license file does not match the node on which the software is running.

What Next

Check to see if the hostid in the key file matches the machine hostid.

Check to make sure that the key certificate encryption code exactly matches the key file encryption code.

Contact your Synopsys support representative.

Feedback

SEC-11

(error) Software is not yet enabled or has expired.

Description

The feature trying to be used does not have a valid license. Either the date may be wrong or the encryption may be wrong.

What Next

Check the start date of the feature. It may not have been reached. Contact your Synopsys support representative.

SEC-12

(error) Can't communicate with the license server.

Description

The machine you are running the software on is having trouble communicating with the license server.

The attempt to the connect to the vendor daemon on all SERVER nodes was unsuccessful.

What Next

Check to make sure that the daemon name in the license file FEATURE line matches the vendor daemon name.

Check to see that the ethernet device can be located.

Check network connections from node running software to server node(s).

Contact local System Adminitrator.

SEC-13

(error) The date/time difference between your host and the license\n \tserver host is too great.

Description

The date/time difference between your host and the license server host cannot be greater than 4 hours.

Feedback

What Next

Contact local System Administrator to synch client/host times.

SEC-14

(error) Key file syntax error: %s.

Description

The start or expiration date is invalid.

What Next

Check the dates in the license file.

Contact your Synopsys support representative.

SEC-15

(error) Key file '%s' has an unrecognized format.

Description

The keyfile is unreadable.

What Next

Check the permissions on the file. It may also not be a text file.

SEC-16

(error) Can't read the '%s' file.

Description

The file /dev/kmem or /vmunix is not readable on this system.

What Next

Contact you local System Administrator.

SEC-17

(error) Internal licensing error number %d: %s.

Feedback

Description

A possible reason is a bad encryption handshake with the server. The client performs an encryption handshake operation with the daemon prior to any licensing operations. This handshake operation failed.

A possible reason is the feature database got corrupted in the daemon. The daemon's run-time feature data-structures have somehow become corrupted. This is an internal daemon error.

A possible reason is that there is no TCP/IP service "license." This happens if a SERVER line does no specify a TCP/IP port number, and the TCP service does not exist. There is no socket to talk to the server on.

What Next

Make sure that there is a socket number in the SERVER line of the key file. Also check with your system administrator.

SEC-18

(error) Unknown internal licensing error number: %d.

Description

Unknown error has occurred.

What Next

Check the status of the license server and the vendor daemon. Try bringing down the license server and bringing it back up again.

SEC-20

(error) This site is not authorized for license(s):\n %s

Description

This site is not licensed to use this product.

What Next

Make sure that the required features are in the key file.

Use lmstat to make sure that the server has enabled the required features.

Contact your local Synopsys Support Center.

Feedback

SEC-21

(error) Failed to checkout license for feature(s):\n %s

Description

The application failed to check out the licenses required to enable this product. It may be that all the licenses are in use or the site is not licensed to use this product.

What Next

Make sure that the required features are in the key file.

Use lmstat to make sure that the server has enabled the required features and to find the current users of the features.

Contact your local Synopsys Support Center.

SEC-22

(information) %s feature '%s'.

Description

This is an informational message indicating the feature that has been queued, checked-out, or checked-in.

What Next

If the feature has been queued for sometime, then you can find out the current users of this feature (by using the lmstat -A command) and request them to release it.

SEC-23

(information) Waiting for required feature(s). (%s)

Description

This is an informational message that is displayed periodically when the process is queued for required set of features. You can find out the current users of all the required features by using the lmstat -A command.

What Next

Request the current users to release the licenses, if possible.

Let the process wait in queue for indicated period of time to acquire the license.

Feedback

SEC-24

(error) Timed out while queuing for required feature(s). (%s)

Description

This is an error message that is displayed when the process has timed out after queuing for required set of features. You can find out the current users of all the required features by using the lmstat -A command.

What Next

Request the current users to release the licenses, if possible.

SEC-50

(error) All '%s' licenses are in use.

Description

The maximum number of licenses has been reached.

What Next

Contact your Synopsys support representative to order more licenses.

SEC-51

(error) This site is not licensed for '%s'.

Description

A possible cause is that no such feature exists. The feature could not be found in the license file.

A possible problem is that the version is not supported at the server end. The version specified in the checkout request is greater than the highest version number the daemon supports.

A possible problem is that the server does not support this feature or the feature has expired or has not yet started (on the server node).

What Next

Check to make sure that the license file supports this version.

Feedback

SEC-52

(error) Requested more licenses for '%s' than supported in the key file.

Description

A checkout request was made for more licenses than are supported in the license key file.

What Next

Make sure that you have enough licenses in the keyfile.

SEC-53

(error) The end-user license options EXCLUDE you from using '%s'.

Description

The user/host/display has been excluded from this feature by an end-user's daemon option file.

What Next

Contact your local System Administrator to have your name removed from the EXCLUDE list in the options file.

SEC-54

(error) The end-user license options don't INCLUDE you for using '%s'.

Description

The user/host/display has NOT been included in this feature by an end-user's daemon option file.

What Next

Contact your local System Administrator to include you in the options file.

SEC-55

(error) Can't remove your '%s' license. You must always have one or\n more of the following license(s): %s.

Description

A request was received to remove a license that is necessary for the application to be run. At least one of these licenses is required for the application to be running.

Feedback

What Next

Make sure that you are removing the right license.

SEC-56

(error) MAX limit reached for required feature(s). (%s)

Description

This is an error message that is displayed if the user has MAX limit set in the options file and tries to checkout more number of quantities than the MAX limit.

What Next

Please check the options file to find the MAX limit allowed for this feature.

SEC-57

(error) License daemon version is older than application's FLEXlm version.

Description

This is an error message that is displayed if the FLEXlm version of the application is higher than than the license daemon version.

What Next

Please upgrade the license server to latest version.

SEC-80

(information) Attempting to reacquire license for '%s'; wait %d minutes.

Description

The node has lost communication with the license server and is attempting to reacquire a license. It will try to reestablish connection every minute for the first X minutes (default is 10, but it will use the number supplied with the *-timeout* option). It will retry for four days.

What Next

Contact your local system administrator to check to see whether the license server or network is hung.

SEC-81

(information) Reacquired license for '%s' after %d minutes.

Feedback

Description

The application lost the license due to some reason. It could be that the vendor daemon died or the license daemon died and it was brought back up again. The application tries to reconnect to the daemon a few times.

What Next

Make sure that the license and vendor daemons are running.

SEC-82

(warning) License server is busy, retrying.

Description

The application server is "busy" trying to connect. The license server is busy establishing a quorum of server nodes so that licensing can start.

What Next

Wait a few minutes. If the license daemon does not start up, bring it down and back up again. It could also be that one of the servers in the redundant server configuration is down.

SEC-83

(warning) Timeout value must be between %d and %d; using default of %d.

Description

The timeout value used is not correct.

What Next

Use the correct timeout value.

SEC-84

(warning) Unable to obtain a license for '%s'.\n \t Obtained a license for '%s' instead.\n \t '%s' contains these features:%s.

Description

The tool could not check out all licenses for the application.

What Next

Check the key file to ensure that you have the licenses for all the features in the product.

Feedback

SEC-85

(error) Communication with the license server failed; error number %d.

Description

Bad return from server. The port number returned from lmgrd is invalid. An attempted connection to a vendor daemon did not result in a correct acknowledgement from the daemon. The daemon did not send back a message within the timeout interval. A message from the daemon had an invalid checksum.

Cannot read from server. The process cannot read data from the daemon within the timeout interval. The connection was reset by the daemon (usually because the daemon exited) before the process attempted to read data.

Cannot write to server The process could not write data to the daemon after the connection was established.

Feature checkin failed at daemon end The checkin request did not receive proper reply from the vendor daemon (the license might still be considered in use).

What Next

Make sure that the port number and the path to the daemon in the keyfile are correct. Either the daemon is down or the machine is not alive. Try checkin again or try removing the license for that feature.

SEC-86

(error) This site is not licensed for third party software; error number %d.

Description

A possible cause is that no such feature exists. The feature could not be found in the license file.

A possible problem is that the server does not support this feature or the feature has expired or has not yet started (on the server node).

What Next

Check to make sure that the license file supports this version.

SEC-87

(error) Unable to obtain license for '%s'. Feature is suppressed.

Feedback

Description

The functionality cannot be invoked for this product package. Possible cause is the functionality is not supposed to be supported for this product package, eventhough the license key is available.

What Next

If the functionality should be within the product package, contact your Synopsys support representative.

SEC-88

(warning) Unable to set precedence for key '%s'. Cyclic dependency detected.

Description

Cyclic dependency on the prerequisite licenses detected. Some features may not execute because of inability to obtain license. If you encounter this warning, please report it to your Synopsys sypport representative.

What Next

Contact your Synopsys support representative.

SEC-89

(information) Unable to set precedence for key '%s'. Precedence already exists.

Description

Order of prerequisite licenses has already existed. Re-setting the precedence is redundant, and does not cause any harm.

What Next

Contact your Synopsys support representative to ensure that the redundant order setting is removed in the next product release.

SEC-100

(error) This can only be used with software that is network licensed.

Description

The application is licensed to run only with network licensing. You may be running the application by using a node locked license.

Feedback

What Next

Check the keyfile being used.

SEC-101

(information) No one is using any feature from the license server.

Description

No features from the keyfile are being used.

What Next

Nothing needs to be done.

SEC-102

(error) Unable to get an optimize license.

Description

The license cannot be obtained.

What Next

Check the keyfile for this feature. Check the location of the keyfile, default or SYNOPSYS_KEY_FILE.

SEC-103

(error) You must have a Design-Analyzer or one of the optimize licenses to use this feature.

Description

The keyfile must have a Design-Analyzer or an optimize license to use this application.

What Next

Check to see if the keyfile has these features. Check whether the correct keyfile is being used.

SEC-104

(information) Checking out the license '%s'.

Feedback

Description

This is a message from the daemon that the license for this feature is being checked out.

What Next

Check whether you are using this feature. If so, nothing needs to be done.

SEC-105

(information) Checking in the license '%s'.

Description

This is a message from the daemon that the license for this feature is being released.

What Next

Nothing need to be done.

SEC-106

(information) Checking out '%s' implies that '%s' is also available. Checking '%s' back in to avoid duplicate license checkout.

Description

The new license key, "DesignWare", is issued to replace the following old license keys: "DesignWare-Foundation", "SynLib-ALU", "SynLib-AdvMath", "SynLib-Control", "SynLib-FltTol", "SynLib-Seq". When the new key is checked out, no old key will be checked out. If any of the old keys are already checked out, they are checked back in to avoid having duplicate licenses checked out.

This is a message from the daemon that the license for the specified feature is being released, because it is not needed.

What Next

This is an informational message only. No action is required on your part.

SEDF

SEDF-1

(error) Unable to open file '%s'.

Feedback

Description

The EDIF file you tried to open does not exist or has incorrect permissions.

What Next

Verify the file name and permissions.

SEDF-2

(information) Ignoring unrecognized construct '%s'\n \tat line %d in '%s'\n \t(and all future occurrences).

SEDF-3

(error) Unmatched right parenthesis\n \tat line %d in %s.

SEDF-4

(error) Missing %s parenthesis\n \tat line %d in %s.

SEDF-5

(error) Net connection failed\n \tat line %d in %s.

SEDF-6

(error) Misplaced percent sign\n \tat line %d in %s.

SEDF-7

(error) Unrecognized token '%s'\n \tat line %d in %s.

SEDF-9

(error) Expected %s\n \tat line %d in %s.

SEDF-10

(error) Incorrect number of elements in %s construct\n \tat line %d in %s.

Feedback

SEDF-11

(error) Argument %d for %s construct is invalid\n \tat line %d in %s.

SEDF-12

(error) array name '%s' does not match bus_extraction_style '%s'\n \tat line %d in %s.

SEDF-13

(error) Unexpected %s\n \tat line %d in %s.

SEDF-14

(error) In rename, '%s' inconsistent with bus extraction style\n \tat line %d in %s.

SEDF-15

(error) ASCII character is not between 0 and 127\n \tat line %d in %s.

SEDF-16

(error) Invalid %s token\n \tat line %d in %s.

SEDF-17

(warning) Duplicate base name '%s' for port bus. Using '%s' instead\n \tat line %d in %s.

Description

The EDIF file contains two port bus (array) definitions which are trying to use the same base name. For example, in[3:2] and in[1:0] both want to use in as the base name. This might be an error, but for compatibility with Design Compiler, this reader will use the full name of one of the port busses as the base name. In this case, it might pick in[3:2] as the base name for one of the port busses.

What Next

Verify that this is not a typo in the file.

SEDF-18

(error) Duplicate port name '%s'\n \tat line %d in %s.

Feedback

Description

The EDIF file contains two scalar ports with the same name. This is an error.

What Next

Correct the port name and re-read the file.

SEL

SEL-001

(error) No such collection '%s'

Description

The collection which you specified does not exist.

What Next

Verify that the collection is the one you want. It is possible that it existed, but was transient. Transient collections are automatically garbage-collected and cannot be relied upon across command boundaries. In order to make a collection persistent, set it to a variable, and then use it. For example:

```
set uPorts [get_ports U*]
    command_for_ports $uPorts
```

SEL-002

(warning) Collection '%s' has inappropriate type (%s).

Description

The collection which you specified contains objects which are not acceptable for this command. Either the data type of the objects is incorrect, or the objects are out of context (for example, they are not in the current design).

What Next

Check the command to determine the allowable object types for it, or specify objects that are in the correct context.

SEL-003

(warning) Nothing implicitly matched '%s'

Feedback

Description

The pattern which you specified did not match any objects of the classes acceptable for this command.

What Next

Check the pattern to see if it is what you expected.

SEL-004

(warning) No %s objects matched '%s'

Description

The pattern which you specified did not match any objects of the class acceptable for this command.

What Next

Check the pattern to see if it is what you expected.

SEL-005

(error) Nothing matched for %s

Description

The pattern(s) which you specified did not match any objects.

What Next

Check the values which you entered.

SEL-006

(error) More than one object matched for '%s'.

Description

The pattern(s) which you specified matched more than one object. This command option accepts only a single object.

What Next

Check the values which you entered.

Feedback

SEL-007

(error) Invalid index %d for collection %s

Description

During an iteration over a collection (with foreach_in_collection), an invalid index was generated.

What Next

Contact your application consultant.

SEL-008

(warning) Collection/attribute class '%s' has not been defined

Description

The collection class which you specified does not exist. Classes of objects include designs, cells, etc.

What Next

Verify that the class name is spelled correctly, or that the class of objects is applicable for this product.

SEL-009

(warning) Collection class '%s' cannot be %s

Description

The collection class which you specified cannot be used for the operation you attempted. Some collection classes cannot be queried, indexed, or copied, so they cannnot be used as an argument to query_objects, index_collection, or copy_collection.

What Next

Only use collections of this class as arguments to appropriate commands.

SEL-010

(warning) %s objects from '%s' were of the %scorrect class.

Feedback

Description

A heterogeneous collection was passed to another command. This collection contained some objects that were of a class which is not accepted by the command. The message will indicate whether some objects or no objects were accepted by the command.

What Next

Some commands continue to operate when only a subset of the patterns match. Other commands only perform their action when all patterns match something. So, verify that the command was applied to the objects which were expected.

SEL-011

(warning) Some objects (%s) could not be queried.

Description

A heterogeneous collection was passed into query_objects. This collection contained some objects that were of a class which cannot be the target of a query.

What Next

There is no adverse affect of this situation.

SEL-012

(information) Iteration for collection %s was terminated\n \tbecause the collection was modified or deleted.

Description

Commands in the body of a *foreach_in_collection* can affect the collection which is currently in iteration. Some commands can cause objects to be removed from the collection, and others can cause the collection to be deleted. When such events occur, the iterator is modified and in some cases will terminate. This message advises you of that event.

For example:

foreach_in_collection itr [get_cells *] { remove_design [current_design] }

would cause the collection of cells to be deleted, and the iteration would be terminated.

What Next

No action is required.

Feedback

SEL-013

(error) Regular expression error: %s.

Description

While using a regular expression with a collection command, you entered an invalid regular expression. For example, use of the * (zero or more) or + (one or more) operators alone always yields the empty set; therefore, ".*" or ".+" would be appropriate. Other errors such as unmatched parens or invalid characters within square braces will also cause this error.

What Next

Take action based on the error that occurred.

SEL-014

(error) At least one %scollection required for argument '%s'%s

Description

Some commands do not allow heterogeneous collections as arguments, whereas others allow them only in some contexts. Other commands require at least one collection as an argument. You entered a variation of a command which requires at least one collection (either homogeneous, or of either type) for the named argument.

What Next

Consult the man page from the command which failed for further information.

SEL-015

(warning) Ignored all implicit elements in argument '%s'%s

Description

Many commands allow implicit searches for objects - an argument can be a list of collections or patterns which are searched for in a documented set of object classes. However, in some cases, it is not possible to determine any object classes in which to search for an implicit pattern. For example, attempting to add an implicit pattern to a heterogeneous collection with *add_to_collection* would cause this warning.

What Next

Consult the man page from the command which failed for further information.

Feedback

SEL-016

(error) Name patterns are not allowed in this argument context - the pattern %s will be skipped/ignored; use only collections in this argument context.

Description

Many commands allow implicit searches for objects - an argument can be a list of collections or name patterns which are searched for in a documented set of object classes. However, in some cases, when there is more than one object class to be searched, it is not allowed to include name patterns, and only collections should be included in such an argument.

What Next

In the argument context in which this error happened, remove all name patterns from the offending argument, and make sure that only collections are included in the argument. You can typically use a "get" command to convert a name pattern to a collection.

SEL-017

(error) %s index %s for collection %s

Description

An invalid or out of range index was supplied to a command.

What Next

Contact your application consultant.

SIM

SIM-001

(error) Number of reference paths %d does not match the number of measured paths %d.

Description

Path comparison is done one path at a time. For example, the first reference path is compared to the first measured path, and the second reference path is compared to the second measure path. Therefore, the number of reference and measured paths must be same.

Feedback

What Next

Ensure that you compare collections of the same physical paths. If one collection is a superset of the other, use the *foreach_in_collection* and *append_to_collection* commands to create a new collection with a subset of path objects to compare. Use *sim_validate_path* to do path correlation with SPICE.

See Also

- append_to_collection
- foreach_in_collection
- sim_validate_path

SIM-002

(warning) Paths cannot be compared because %s

Description

Path comparison is done pin by pin. Only pins of the same name and rise/fall sense can be compared.

What Next

Ensure that you compare collections of the same physical paths. If one collection is a superset of the other, use the *foreach_in_collection* and *append_to_collection* commands to create a new collection with a subset of path objects to compare. Use *sim_validate_path* to do path correlation with SPICE.

See Also

- sim_validate_path

SIM-003

(information) The reference path has no simulation data

Description

Only segments of the reference path annotated with Spice-simulated delays are reported during the comparison. This is to avoid both long reports as well as misleading accuracy percentage of overall path delay. To force comparison on all pins of the datapath use *sim_validate_path* without *-from* and *-to* options.

Feedback

What Next

Use the *sim_validate_path* command on a valid path segment for correlation.

See Also

- report_timing
- sim_validate_path

SIM-004

(error) Simulation failed %s.

Description

The simulation of the spice deck has failed. This could be because of multiple reasons. Most common are incorrect spice simulator path, missing transistor model files, or failed measure statements.

What Next

Use the *-verbose* option to show detailed message of simulation log directory indicated by "The generated SPICE deck is ...". Investigate sim.log in simulation log directory for reasons of simulation failure.

To keep the simulation directory after simulation terminates, use the *sim_setup_simulator* command with the *-preserve failed* or *-preserve all* option.

See Also

- sim_analyze_clock_network
- sim_setup_library
- sim_setup_simulator
- sim_validate_noise
- sim_validate_path
- sim_validate_setup
- sim_validate_stage

SIM-005

(error) Simulation failed because there are designs in memory

Feedback

Description

Validation of simulation setup and predriver characterization create their own design based on a library cell that you want to simulate.

What Next

Either remove all designs by *remove_design -all* and rerun this command or in case of setup validation you can validate an existing timing path by *sim_validate_path*.

See Also

- sim_setup_simulator
- sim_validate_path
- remove_design

SIM-006

(error) Validation of simulation setup does not support sequential cells

Description

Validation of simulation setup supports only combinational cells.

What Next

Use an arc of a combinational cell in *sim_validate_setup*.

See Also

- sim_validate_path

SIM-007

(information) Using default %s of %g library units

Description

Validation of simulation setup determines default load capacitance and input transition from library data as follows: For CCS libraries middle Indexes of output_current table of the first library arc selected by *sim_validate_setup* are used. For NLD libraries default capacitance is 10 times pin capacitance of the from pin of the first library arc selected by *sim_validate_setup*. Transition time is 100ps.

What Next

To use a specific value use *sim_validate_setup -transition_time <slew_value> -capacitance <cap_value>*.

See Also

- sim_validate_setup

SIM-008

(information) Simulator executable %s does not exit or is incorrect

Description

Simulator executable has to exist, be a regular file, readable and executable.

What Next

Make sure that you can execute simulator standalone (paste the above path to your current shell). Correct the path or adjust file access permissions.

See Also

- sim_setup_simulator

SIM-009

(Error) Clock model generation failed %s.

Description

Generation of clock model has failed because an unsupported feature as noted above has been enabled. If need to generate clock model that captures the interaction of unsupported feature on the clock network, please contact Synopsys support center

What Next

Disable the unsupported feature and re-run the command.

See Also

- sim_analyze_clock_network

Feedback

SIM-010

(Warning) The clock model generation may not be accurate due to the loaded parasitics in design.

Description

The clock model generation flow needs to be enabled before loading any parasitics in the design. If the parasitics of the clock network are loaded before enabling the clock model generation flow, there is a possiblity of some clock nets (especially mesh nets) being treated as ideal nets. In order to avoid this, please load the parasitics of the clock network after enabling the clock model generation flow.

What Next

Remove the annotated parasitics and re-load them again after enabling clock model generation flow.

See Also

- sim_setup_spice_deck
- sim_analyze_clock_network
- remove_annotated_parasitics

SIM-012

(Error) Multiple clocks have been defined inside the clock network specified by the -from and -to options.

Description

The clock network model generation failed while tracing the clock network with the given -from and -to options, because PrimeTime encountered another clock definition inside the clock network.

What Next

Please ensure that the -from and -to options are used to specify a clock network with a single clock passing through it.

See Also

- sim_analyze_clock_network

Feedback

SIM-014

(Error) The number of nets can be enabled for SI correlation exceeds limit. This command has no effect.

Description

The *sim_enable_si_correlation* command only accepts a maximum of 1000 nets. This command has no effect if the limit is exceeded.

What Next

Reduce the size of nets and rerun the *sim_enable_si_correlation* command.

See Also

- sim_enable_si_correlation
- sim_validate_stage

SIM-015

(Warning) Correlation cannot be done on this stage with net arc %s.

Description

The *sim_validate_stage* command or *sim_validate_noise* command ignore this net arc for correlation purpose. Typical reasons include the net arc does not have a driving arc, no effective coupling on the net, no physical driver, or no *sim_enable_si_correlation* on the net before *update_timing*.

What Next

Ensure that the net has effective coupling and physical driver. If not, remove the net arc from the *sim_validate_stage net_arc_objects* list. Also, use the *sim_enable_si_correlation* command on specified nets before using the *update_timing* command.

See Also

- sim_enable_si_correlation
- sim_validate_noise
- sim_validate_stage

Feedback

SIM-016

(warning) The start pin of the specified path segment is an output pin of a cell. This might cause an inaccurate correlation.

Description

The *-from* option specifies the start pin of the specified path segment for SPICE simulation and correlation. Simulation from an input pin of a cell is recommended.

What Next

Specify an input pin of a cell as the start pin for the *-from* option of the *sim_validate_path* command.

See Also

- sim_validate_path

SIM-017

(warning) No path exists through the net arc. Simulation is skipped.

Description

The net arc does not have any paths through it. The *sim_validate_stage* skips SPICE correlation on this stage.

This issue commly occurs when all driving timing arcs of the net arc are disabled.

What Next

Check whether any path goes through the specified net arc. If not specify a different arc for correlation purpose.

See Also

- sim_validate_stage

SIM-018

(warning) Double switching found on %s.

Description

Simulation found double switching at interested pin related to SI correlation. The *sim_validate_stage* may still report SPICE correlation on this stage, but this net arc should be excluded for correlation purpose.

Feedback

What Next

Exclude the stage for correlation purpose.

See Also

- sim_validate_stage

SIM-019

(Warning) -measure_type option %s is not matching with si_ccs_aggressor_alignment_mode value.

Description

The *sim_validate_stage* command -measure_type option must match with *si_ccs_aggressor_alignment_mode* value. Otherwise, correlation accuracy can be affected due to inconsistent alignment mode in PrimeTimeSI and SPICE.

What Next

Ensure that *si_ccs_aggressor_alignment_mode* value is consistent with *sim_validate_stage -measure_type option.*

See Also

- sim_validate_stage

SIM-020

(Warning) %s value in sweeping is worst case; may need additional sweeping.

Description

The *sim_validate_stage* command does auto-sweeping around PrimeTime worst case alignment to find SPICE worst case alignment.

What Next

Increase sweeping range until the worst case SPICE delay is not from the first or last index of sweeping.

See Also

- sim_enable_si_correlation
- sim_validate_stage

Feedback

SIM-021

(warning) Simulation has been skipped for path %d due to %s.

Description

The simulation of the path has been skipped. Because it would fail when sub_circuit is missing. Please check for *SPICE-211* message for further information.

What Next

Update *sim_setup_library* -sub_circuit setting to include needed sub_circuit.

See Also

- sim_setup_library
- SPICE-211

SIM-022

(warning) %s. CCB output correlation report will be skipped.

Description

CCB output correlation report is skipped. Some of the common reasons are the following: 1) No valid CCSN model is available from the input pin. This could be because the library does not have CCSN model from the input pin or CCSN model is disabled by case analysis, etc. 2) CCB output calculation failed because of bad CCSN model.

What Next

Check if a valid CCSN model exists from the given pin or the CCSN model is good.

See Also

- sim_validate_noise

SIM-023

(warning) The -from '%s' is an output '%s' that may result in an inaccurate simulation.

Description

The from port/pin of the sim_analyze_clock_network command is an output port/pin which may result in inaccurate simulation.

Feedback

What Next

Verify that the from port/pin is correct.

See Also

- sim_analyze_clock_network

SIM-024

(warning) Clock network simulation is enabled in hyperscale analysis, accuracy is not guaranteed.

Description

In hyperscale analysis flow, if some part of the clock network that needs simulation is not physically exist in Verilog, the simulation accuracy will be impacted.

What Next

Pleaes check if the simulated clock network is physically represented in the design completely.

See Also

- sim_analyze_clock_network

SIM-025

(information) supporting generated clock defined on internal pin which may cause large simulation files

Description

When the feature of supporting generated clock defined on internal pin is on, all internal nodes of subcircuit could be accessed for measurement. This may cause large simulation result files if many subcircuits are included or complex subcircuits are included in the SPICE deck.

What Next

Pleaes check if the feature is needed to be on.

See Also

- sim_analyze_clock_network

Feedback

SIM-026

(warning) SPICE noise area measurement failed, reported as zero.

Description

When the noise height is too small in SPICE simulation, the SPICE noise area will be reported as zero and the noise area difference percentage will be reported as 100.

What Next

Please check the noise height correlation.

See Also

- sim_validate_noise

SIM-027

(warning) The %s option is obsolete as of the %s release. Do not use this option as it is no longer supported.

Description

You received this message because you have used the indicated option of the command you are running.

As of the indicated release of PrimeTime, this option is obsolete and will no longer be supported in this or subsequent releases. In the indicated release, PrimeTime will honor the usage of this option and issue this warning message. In subsequent releases, the option will be removed from the command that you are running and you will receive an error message when you use the option.

What Next

Please do not use this obsolete option of the command that you are running.

SIM-028

(Error) The specified from pin '%s' is not in the given clock network '%s'.

Description

The clock network model generation failed while tracing the clock network with the given -from option. The specified from pin must either be the source of the given clock or be in the given clock network.

Feedback

What Next

Please ensure that the -from and -clock_source options are consistent.

See Also

- sim_analyze_clock_network

SIM-029

(Error) The specified to pin is not in the clock network '%s'.

Description

The clock network model generation failed while tracing the clock network with the given -from and -to options. The specified to pin must be in the given clock network or the clock network associated with -from option. Please use option -include_generated_clock if the generated clock is involved in the tracing clock network with -from and -to options.

What Next

Please ensure that the -from, -to and -clock_source options are consistent.

See Also

- sim_analyze_clock_network

SIM-030

(Error) There is no connection with given -from and -to in clock network.

Description

The clock network model generation failed while tracing the clock network with the given -from and -to options.

What Next

Please ensure that there is path between -from and -to within clock network.

See Also

- sim_analyze_clock_network

SIM-200

(error) Report cannot be generated due to %s.

Feedback

Description

The correlation or analysis report cannot be generated. This could be because of missing necessary statistics output files from Hspice simulation.

Even if the simulation is successful (i.e. mt0 file is generated without failed measurement), SIM-200 may still be issued because of missing mpp0/qqt0.csv files. This may happen if simulation skips generating the statistics files due to the Hspice mcbrief option setting (e.g. mcbrief=1).

Please check the mcbrief setting in the header file. If the purpose is just to avoid generating the mc0 file, mcbrief=5 can generate statistics files like mpp0/qqt0.csv file without mc0 file.

What Next

Please check mcbrief setting in header file. If the purpose is just to avoid generation mc0 file, mcbrief=5 can generate statistics files like mpp0/qqt0.csv file without mc0 file.

To keep the simulation directory after simulation terminates, use the *sim_setup_simulator* command with the *-preserve failed* or *-preserve all* option.

See Also

- sim_setup_library
- sim_validate_path

SIM-312

(information) Path has time given or borrowed to startpoint, simulation from start point.

Description

In *sim_analyze_path* or *sim_validate_path* command, when startpoint is transparent latch with time given or borrowed. Simulation cannot cover clock path and data path at the same time. Simulation is done from start point.

What Next

If clock path needs to be simulated, please apply *sim_analyze_path* or *sim_validate_path* on clock path.

See Also

- sim_analyze_path
- sim_validate_path

Feedback

SIM-313

(warning) path %d is not full_clock_expanded in sim_analyze_path.

Description

To make sure *sim_analzye_path* does simulation from CRP point to endpoint, it's required to use full_clock_expanded path. Otherwise clock information is not completed, capture clock simulation is skipped, and only data path is simulated by SPICE.

What Next

Update path collection used in *sim_analyze_path* by using *get_timing_path -path_type full_clock_expanded*.

See Also

- sim_analyze_path
- SPICE-211

SLG

SLG-001

(fatal) This is NOT a code crash but an intentional bailout to get your attention. There are scaling-related setting errors or library data issues that are considered fatal to your analysis, and need to be resolved as soon as possible. See the SLG-001 man page.

Description

The *define_scaling_lib_group* command specifies a group of libraries for scaling and exact-match usages. These features have these major requirements:

- Library data consistency requirements.
- Scaling formation requirements which are needed by scaling only.
- Cell instance operating condition setting cannot go beyond the acceptable range defined by the scaling group.

If these requirements are not met, PrimeTime issues SLG and DEL errors and warnings. You got the SLG-001 message and bailout because the script has one or more of these major errors that seriously affect QoR or even cause calculation failure and fatal errors. PrimeTime stops before *update_timing* so you can get a list of related errors.

If you choose to accept the error and want timing analysis to continue, you can set the *timing_continue_on_scaling_error* variable to true to bypass SLG-001 errors. In that case, you will still see SLG-418 warnings with a list of offending error IDs. However, by bypassing SLG-001 errors, calculation failure or QoR effects can occur.

What Next

Use the *check_timing -include operating_conditions* command and fix the following check failures:

```
SLG-202(n)
SLG-209(n)
SLG-211(n)
SLG-217(n)
SLG-303(n)
SLG-310(n)
SLG-311(n)
SLG-316(n)
SLG-317(n)
SLG-320(n)
SLG-321(n)
SLG-330(n)
```

See Also

- define_scaling_lib_group
- timing_continue_on_scaling_error

SLG-201

(error) A library can be in only one scaling library group.

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the *link_design* commands occur (either explicitly or implicitly).

If you try to use a library in more than one group, the SLG-201 error message occurs.

After design linking occurs, the remaining libraries in scaling library groups will be loaded to "complete" the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other; if this association fails, the scaling library groups cannot be completed, and the SLG-202 error message is issued.

What Next

Ensure that the set of arcs and pins is identical across the members of the scaling library groups. The positions of the arcs and pins within the libraries must be the same as well.

Feedback

See Also

- define_scaling_lib_group
- SLG-201
- SLG-202
- SLG-203
- SLG-205

SLG-202

(error) Completion of scaling library groups failed %s.

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is read.

If you try to use a library in more than one group, the SLG-201 error message occurs.

After design linking occurs, the remaining libraries in scaling library groups will be loaded to "complete" the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other; if this association fails, the scaling library groups cannot be completed and the SLG-202 error message is issued.

What Next

Ensure that the set of arcs and pins is present across the members of the scaling library groups. This message is issued when some of the arcs or cells are missing across the members of the scaling library groups.

If you are using Base-curve Technology CCS Timing libraries, also verify if the base curve information in the libraries have been discretized and normalized in identical manner; that is, check if curve_x has identical values across the scaling libraries in a library group.

See Also

- define_scaling_lib_group
- SLG-201
- SLG-202
- SLG-203

Feedback

SLG-203

(information) The members of a scaling library group have significantly different output-capacitance indexes; this can adversely affect scaling accuracy.

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the *read_db* and *link_design* commands occur (either explicitly or implicitly).

If you try to use a library in more than one group, the SLG-201 message occurs.

After design linking occurs, the remaining libraries in scaling library groups are loaded to complete the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other. If this association fails, the scaling library groups cannot be completed, and the SLG-202 error message is issued.

What Next

Ensure that the set of arcs and pins is identical across the members of the scaling library groups. The positions of the arcs and pins within the libraries must be the same as well.

The output-capacitance indexes used for Composite Current Source (CCS) driver data is better to have identical values across the libraries. If this is not satisfied, the SLG-203 message is issued.

See Also

- define_scaling_lib_group
- SLG-201
- SLG-202
- SLG-203

SLG-204

(warning) The timing arcs %s cannot be uniquely determined across the scaling libraries, it is assumed that the timing arcs are defined in the same order across all the libraries.

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is linked.

If you try to use a library in more than one group, the SLG-201 message occurs.

Feedback

After design linking occurs, the remaining libraries in scaling library groups are loaded to complete the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other. If the timing arcs cannot be associated across the scaling libraries because the timing arcs cannot be identified uniquely within a library, the SLG-204 warning message is issued. Since the timing arcs cannot be uniquely identified, the arcs are assumed to be in the same order across the libraries in a library group.

Note that this is only an informational warning; the scaling relationship for the scaling library group is still created.

What Next

Ensure that the set of arcs that cannot be uniquely identified are present in the same order across the members of the scaling library groups. Run LC scaling check to detect and correct all major violations.

See Also

- define_scaling_lib_group
- SLG-201
- SLG-202
- SLG-203

SLG-205

(warning) CCS Noise information is inconsistent for %s across the libraries in the scaling library group. Scaling for CCS noise will not be supported.

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is read.

If you try to use a library in more than one group, the SLG-201 message occurs.

After design linking, the remaining libraries in scaling library groups are loaded to complete the groups. During the completion step, data for the same arcs and pins across libraries are associated with each other. If this association fails, the scaling library groups cannot be completed, and SLG-202 error message is issued. If the association fails only due to missing or inconsistent CCS noise data, the SLG-205 warning message is issued and the inconsistent CCS noise data is not used in calculation.

Feedback

What Next

Ensure that the CCS noise data for the set of arcs and pins is present across the members of the scaling library groups. This message is issued when some of the arcs or pins have at least one of the following conditions:

- Missing CCS noise model information across the members of the scaling library groups
- CCS noise model information with the input voltage and output voltage indexes not in the same percent vdd in all libraries of a scaling group
- Inconsistent or missing conditions for CCS noise models across the members of a scaling library group
- Inconsistent ordering of conditional CCS noise models across the members of a scaling library group

See Also

- define_scaling_lib_group
- SLG-201
- SLG-202
- SLG-203

SLG-206

(warning) Completion of scaling library group failed for power analysis: %s.

Description

This message is issued when some of the power arcs are missing across the members of the scaling library group.

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is read.

After design linking, the remaining libraries in scaling library group are loaded to complete the group. During the completion step, data for the same arcs and pins across libraries are associated with each other. If this association fails for associating power arcs across the libraries, the SLG-206 warning message is issued, and scaling is not enabled for power analysis.

Note that this warning is for power analysis, the scaling relationship for the scaling library group is still created. The scaling for timing analysis is not affected. The SLG-202

Feedback

message is issued when some of the timing arcs or cells are missing across the members of the scaling library group.

What Next

Ensure that the set of power arcs is present across the members of the scaling library group.

See Also

- define_scaling_lib_group
- SLG-202

SLG-207

(warning) Some of the power arcs cannot be uniquely determined across the scaling libraries, it is assumed that the power arcs are defined in the same order across all the libraries.

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is linked.

After design linking, the remaining libraries in scaling library group are loaded to complete the group. During the completion step, data for the same arcs and pins across libraries are associated with each other. If the power arcs cannot be associated across the scaling libraries because the power arcs cannot be identified uniquely within a library, the SLG-207 warning message is issued. Since the power arcs cannot be uniquely identified, the arcs are assumed to be in the same order across the libraries in a library group.

Note that this is only an informational warning, the scaling relationship for the scaling library group is still created.

What Next

Ensure that the set of arcs that cannot be uniquely identified are present in the same order across the members of the scaling library group.

See Also

- define_scaling_lib_group
- SLG-204
- SLG-206

Feedback

SLG-208

(error) The command define_scaling_lib_group needs to be defined before the command set_variation_library.

Description

You must use the *define_scaling_lib_group* command before using the *set_variation_library* command.

What Next

Use the *define_scaling_lib_group* command before using the *set_variation_library* command.

See Also

- define_scaling_lib_group
- SLG-201
- SLG-202
- SLG-203

SLG-209

(error) Invalid set of libraries passed to define_scaling_lib_group.

Description

A valid set of libraries should be passed to *define_scaling_lib_group*. Check the characterization operating conditions of the libraries in the group.

For example, if you want to use operating conditions between 0.8 and 0.9 V and temperatures between -40 and 125 degrees, libraries characterized at all four voltage and temperature combinations should be specified:

```
pt_shell> define_scaling_lib_group { \\
          lib_max_125_0.8V_cccs.db \\
          lib_max_125_0.9V_cccs.db \\
          lib_max_-40_0.8V_cccs_v2.db\\
          lib_max_-40_0.9V_cccs_v2.db }
```

If any of the four libraries are missing, the scaling library group is rejected. When specifying multiple temperatures or voltages, all libraries on the resulting voltage-temperature grid must be provided.

Feedback

What Next

Check the characterization operating conditions of the libraries provided to *define_scaling_lib_group*, and ensure that the grid is fully populated.

See Also

- define_scaling_lib_group
- report_lib

SLG-210

(error) Zero or more than one scaling library is in the link_path or link_path_per_instance. Creation of scaling group failed.

Description

Only one library in each scaling library group should be in the link_path, or be the min library of a library in the linked path. If there is none or more than one scaling library in the link_path, the tool does not create this library group.

What Next

Fix the scaling library group, and rerun your script.

See Also

- define_scaling_lib_group

SLG-211

(warning) Loading of CCS data for multi-rail scaling support has failed , the reason is: %s.

Description

The reasons that might cause the loading to fail include: if the libraries are non-PG-pin libraries; if the libraries do not have any CCS data; if more than one or none of the specified libraries is a link library or a min library of a link library, and finally a series of data inconsistencies such as if a specific arc has driver data but no receiver data.

When this warning is issued, multirail scaling is not possible for that scaling group, and the scaling calculations using the scaling library group revert to regular single-rail scaling.

Feedback

What Next

Ensure that libraries specified are CCS PG-pin libraries, and exactly one of them is a link library or min library of a linked library. Also, ensure that corresponding receiver and driver data is available for every arc in each of the libraries.

See Also

- define_scaling_lib_group

SLG-212

(information) The variable %s cannot be turned on because %s.

Description

If you set the *variation_enable_analysis* variable after you use the *define_scaling_lib_group* command, the variable setting change does not take effect.

What Next

Set the *variation_enable_analysis* variable before using the *define_scaling_lib_group* command.

SLG-213

(information) The number of dimensions in dimension_names and dimension_values list are not consistent.

Description

The size of the list in *dimension_names* and *dimension_values* should match.

When this information is issued, the command does not take effect.

What Next

Reissue the command with correct set of *dimension_names* and *dimension_values*.

See Also

- define_scaling_lib_group

SLG-214

(error) Scaling will not be done for cell %s, since it does not have consistent scaling information across the scaling libraries.

Feedback

Description

Scaling cannot be done for specific arcs or pins of the specified cell because of inconsistent or missing scaling data.

What Next

Check the scaling libraries using the Library Compiler utility to correct the inconsistencies. This might be due to missing arc or pin data in one of the libraries. Reissue the command with a correct set of scaling libraries.

See Also

- define_scaling_lib_group
- SLG-209

SLG-215

(warning) Scaling creation for the %s has failed due to missing or mismatching data.

Description

If there is an arc or pin with missing or mismatching data, the scaling relation for that arc or pin is not created. The other arcs or pins in the scaling library group are not affected. The calculation of that arc or pin uses linked library data instead.

See Also

- define_scaling_lib_group
- SLG-202

SLG-216

(error) An unexpected exact-match has been detected for the cell timing %s in %s calculation

Description

If you use the *define_scaling_lib_groups* command with the *-exact_match_only* option, only exact matches are considered acceptable. If the cell operating condition requires scaling, or none of the library operating condition matches the desired one, it is considered an exact-match failure, and this message is issued. Then the linked library is used.

Feedback

What Next

In the case or *-exact_match_only*, change the operating condition of the cell instance, or add a library in the scaling group with the specified operating condition. Operating conidtions include voltage, rail voltage, temperature, and process. Alternatively, consider using scaling.

You can use "check_timing -override_default operating_conditions -verbose" to determine detail information about the PVT mismatch between design and library. And use "report_lib_group -scaling -show { process voltage temperature} " can determine each library PVT, "report_power_pin_info" can display the cell instance voltage setting. Compare both reports, you can see the PVT difference.

Please do not ignore this message. This error must be fixed or it will impact QoR.

SLG-217

(error) Scaling will not be done for cell %s, since the associated scaling library group does not meet the scaling formation requirement.

Description

Scaling cannot be mathematically performed if the data is insufficient for performing scaling, such as trying to do two-dimensional scaling with only two libraries. Scaling formation is done by the points representing the operating conditions of the libraries in a multidimensional space.

PrimeTime supports on-the-grid, n+1, and 2n+1 scaling formations. This message is issued when the scaling operating condition formation of an arc or pin data of a cell does not meet any of the three formations.

What Next

Check the operating conditions of the libraries, including voltage, rail voltages, temperature, and so on. Provide libraries that meet the scaling formation requirements, and reissue the command.

See Also

- define_scaling_lib_group
- SLG-209

SLG-218

(information) Find %s, check your scaling libraries.

Feedback

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. This requires data consistency otherwise scaling might encounter issues. This message detects inconsistency issues, such as missing voltage_maps or mismatch voltage_map sequence across the scaling libs.

What Next

This informational message indicates an issue that the tool attempts to fix internally. However, you should fix the library to avoid any potential issues and run the Library Compiler scaling check. All libraries used in scaling should pass the Library Compiler scaling check.

See Also

- define_scaling_lib_group

SLG-220

(warning) Completion of scaling library group failed for rail analysis: %s.

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is read.

After design linking, the remaining libraries in scaling library group are loaded to complete the group. During the completion step, data for the same arcs and pins across libraries are associated with each other. If this association fails for associating power arcs across the libraries, the SLG-220 warning message is issued, and scaling is not enabled for analysis.

What Next

Ensure that the set of power arcs is present across the members of the scaling library group. This message is issued when some of the power arcs are missing across the members of the scaling library group.

See Also

- define_scaling_lib_group

Feedback

SLG-221

(warning) Some of the power arcs cannot be uniquely determined across the scaling libraries for rail analysis, it is assumed that the power arcs are defined in the same order across all the libraries.

Description

The *define_scaling_lib_group* command specifies a group of libraries to interpolate between for voltage and temperature scaling. The command must be issued after the design is linked.

After design linking, the remaining libraries in scaling library group are loaded to complete the group. During the completion step, data for the same arcs and pins across libraries are associated with each other. If the power arcs cannot be associated across the scaling libraries because the power arcs cannot be identified uniquely within a library, the SLG-221 warning message is issued. Since the power arcs cannot be uniquely identified, the arcs are assumed to be in the same order across the libraries in a library group.

Note that this is only an informational warning; the scaling relationship for the scaling library group is still created.

What Next

Ensure that the set of arcs that cannot be uniquely identified are present in the same order across the members of the scaling library group.

See Also

- define_scaling_lib_group

SLG-222

(warning) Library scaling group: Mismatch detected in the number of POCV tables for %s in library %s.

Description

This warning occurs when defining a library scaling group, if a discrepancy is detected in the number of POCV tables across the different libraries.

See Also

- define_scaling_lib_group

Feedback

SLG-223

(warning) Library scaling group: Mismatch detected in the index sizes of POCV tables for %s in library %s.

Description

This warning occurs when defining a library scaling group, if a discrepancy is detected in the index sizes of POCV tables across the different libraries.

See Also

- define_scaling_lib_group

SLG-224

(warning) Replacing library for '%s' with '%s'

Description

This message warns you that you have the same cell instance listed multiple times in the setting for the *define_cell_alternative_lib_mapping* variable. In the following example, the *uls/utlb_ctl/U112* instance is listed twice.

```
define_cell_alternative_lib_mapping liberty_ss_0p600v_m25c_mis.db -cell
 "uls/utlb_ctl/U112 uls/utlb_ctl/U112"
```

What Next

Examine the setting for the *define_cell_alternative_lib_mapping* variable, and ensure that only one valid library exists per cell-instance.

See Also

- define_cell_alternative_lib_mapping

SLG-225

(error) The *define_cell_alternative_lib_mapping* command failed due to missing library group information for library '%s'

Description

You need to create a scaling group for the library used in the *define_cell_alternative_lib_mapping* command.

Feedback

What Next

Specify the library group using the *define_scaling_lib_group* command as shown in the following example.

```
set link_path "* my_linked_lib.db"
read_verilog my_design.v
link_design my_design
define_scaling_lib_group -exact_match_only {my_linked_lib.db
 my_alt_lib.db}
define_cell_alternative_lib_mapping my_alt_lib.db -cells {U1 U2}
update_timing
```

See Also

- define_cell_alternative_lib_mapping
- define_scaling_lib_group
- link_path

SLG-226

(warning) Scaling creation for the %s has failed due to unsupported 3-D NLDM data.

Description

If there is an arc using 3-D NLDM data, the scaling relation for that arc will not be created. The other arcs or pins in the scaling library group are not affected. The calculation of that arc or pin uses linked library data instead.

See Also

- define_scaling_lib_group
- SLG-202

SLG-227

(error) An unexpected exact-match failure due to missing arc/pin has been detected for the cell timing %s in %s calculation

Description

If you use the *define_scaling_lib_groups* command with the *-exact_match_only* option, only exact matches are considered acceptable. You get this message when the exact_match library does not have the matching arc/pin as the linked library.

Feedback

What Next

Please run Library Compiler scaling check to find the mismatching arc/pin and fix accordingly.

SLG-228

(error) An unexpected scaling failure due to extrapolation has been detected for the cell timing %s in %s calculation

Description

This is a special error on extrapolation. You receive this error because your operating conditon of the cell is too close to a missing scaling library cell or a missing scaling library. Therefore accuracy is impacted and it is considered extrapolation.

What Next

Please change cell operating condition to stay away from the missing library or the missing library cell. Check report_power_pin_info/report_design and report_lib_group -scaling -show {process voltage temperature} to check why the cell PVT is not in the range of the scaling group. Also check whether there is any lib cell/pin/arc is missing message SLG-305, SLG-307 and SLG-308 in the previous define_scaling_lib_group processing log file.

SLG-229

(error) An unexpected scaling calculation failure has been detected for the cell timing %s in %s calculation

Description

This is an error to let you know that CCS or NLDM data scaling has failed. This is a very rare failure, often due to bad library data causing scaling to go wrong, that triggers internal detection to issue this error.

What Next

Please check for bad library data, in particular if any data that is way too large or too small than it should be. Also, whether multiple libraries with same operating conditons are used. This could happen when most of the rails of the libraries are excluded from scaling calculation, then scaling uses the left over rails to decide scaling connection. Scaling choose to use the first library among the libraries with same set of remaining rails. If the first library happends to have dramatically different data than other libraries used in scaling, you may get this error on bad data triggering scaling failure.

Feedback

SLG-231

(error) Detected a scaling failure because specified operating conditions is not on proper grid of the scaling group for the cell timing %s calculation.

Description

You receive this error because your operating conditon of the cell is far to the desired range of the scaling library group. This error message is to attention customer that it may have bad scaling calculation results due to the inproper operating condition setting or scaling lib definition.

What Next

Please change the cell operating condidtion or add more full grid library corner and make sure the specified cell operating condition is within desired scaling range.

If it is voltage-only scaling, use 'report_power_pin_info' to get the related cell voltage setting, and use 'report_lib_group -scaling -show {voltage}' to find out the scaling range of the group.

See Also

- report_power_pin_info

SLG-232

(warning) The specified operating conditions for the cell timing %s is not inside nearby local grid of the scaling group, and scaling chooses the biggest grid for calculation.

Description

You receive this warning because your operating conditon of the cell isn't within any nearby local grid, but the operating condition is within range of the biggest of grid of the group. Scaling is using the biggest grid to do calculation. This might cause scaling accuracy lost because of using lib corner that is far to operating condition.

What Next

Please add extra new lib corner to cover the specified operating condition.

If it is voltage-only scaling, use 'report_power_pin_info' to get the related cell voltage setting, and use 'report_lib_group -scaling -show {voltage}' to find out the scaling range of the group.

See Also

- report_power_pin_info

Feedback

SLG-301

(warning) Scaling libraries are defined after timing analysis.

Description

define_scaling_lib_group command is recommended to be used before any timing update.

What Next

To modify your running script and make all *define_scaling_lib_group* commands are used before any timing update. If user doesn't change the script and wants to skip this warning message, user needs to run update_timing -full to honor the newly added scaling libraries.

See Also

- define_scaling_lib_group

SLG-302

(error) Scaling libraries can be defined only after the design is linked.

Description

You tried to use the *define_scaling_lib_group* command before the *link_design* command.

What Next

Read in and link the design with the *link_design* command. Then use the *define_scaling_lib_group* command. Do this before the first timing update.

See Also

- define_scaling_lib_group

SLG-303

(error) Multiple scaling libraries '%s' are in the link path specfied by the link_path and link_path_per_instance variables. Creation of the scaling group failed.

Description

The *define_scaling_lib_group* command requires exactly one library of a scaling library group to be in the link path specified by the *link_path* and *link_path_per_instance* variables. The remaining scaling libraries are automatically read in to create the group. This error message indicates that more than one scaling library was found in the link path.

Feedback

What Next

Change either the link path or the *define_scaling_lib_group* command so that exactly one library in the scaling library group exists in the link path.

See Also

- define_scaling_lib_group
- link_path
- link_path_per_instance

SLG-305

(error) Cell '%s' is not present in scaling library '%s'. Scaling will not be performed for this cell.

Description

The *define_scaling_lib_group* command requires every library cell in a link library to be also present in every scaling library. This error message reports a library cell in a link library that does not exist in a scaling library.

What Next

Make sure that all the libraries listed in *define_scaling_lib_group* command contain all of the library cells in the linked libraries.

See Also

- define_scaling_lib_group
- link_path
- link_path_per_instance

SLG-306

(error) define_scaling_lib_group '%s', cannot find scaling Library '%s', scaling will not be performed.

Description

define_scaling_lib_groups command requires all libraries in the scaling lib group are present. This message will be issued if there is one scaling library cannot be found.

Feedback

What Next

Correct the library in the define_scaling_lib_group and make sure all scaling libraries are present.

SLG-307

(error) Pin '%s' of cell '%s' is present in link library '%s' but not in scaling library '%s'.

Description

The *define_scaling_lib_group* command requires every pin of every library cell in a link library to be also present in every scaling library. This error message reports a pin of a library cell in a link library that does not exist in a scaling library. define_scaling_lib_group command will error out when detect this error.

What Next

Make sure that all the libraries listed in *define_scaling_lib_group* command contain all of the library pins in the linked libraries. Please modify script remove or change the library that contain different pin.

See Also

- define_scaling_lib_group
- link_path
- link_path_per_instance

SLG-308

(error) Arc '%s' of cell '%s' is present in link library '%s' but not in scaling library '%s'. Scaling might not be performed for this arc.

Description

The *define_scaling_lib_group* command requires every timing arc of every library cell in a link library to be also present in every scaling library. This error message reports an arc of a library cell in a link library that does not exist in a scaling library. If the related scaling lib group is exact_match_only, calculation will fallback to link library arc lib data.

What Next

Make sure that all the libraries listed in *define_scaling_lib_group* command contain all of the library arcs in the linked libraries.

Feedback

SLG-309

(error) The voltage rail of scaling library '%s' does not match that of the link library '%s'. The scaling group cannot be formed.

Description

define_scaling_lib_groups command requires each scaling library voltage rail is same with the link library among the library group. If any scaling library voltage rail is different with the link library, define_scaling_lib_group command will error out, and output this message.

What Next

Replace the offending scaling library with library that has same library voltage rail as link library.

SLG-310

(error) The pin thresholds of scaling library '%s' do not match those of the link library '%s'.

Description

The *define_scaling_lib_group* command requires each scaling library threshold to be the same as that of the the link library in the library group. This message indicates that the *define_scaling_lib_group* command found a threshold difference.

What Next

Replace the offending scaling library with a library that has the same library threshold definitions as the link library.

See Also

- define_scaling_lib_group

SLG-311

(error) The CCS driver data of scaling library '%s' does not match that of link library '%s'. The scaling group cannot be formed.

Description

The *define_scaling_lib_group* command requires library CCS data to be consistent between each scaling library and the link library. This error message indicates that the command found inconsistent CCS library data.

Feedback

What Next

Make sure that the *define_scaling_lib_group* command specifies a list of libraries with CCS driver data consistent with the link library.

See Also

- define_scaling_lib_group

SLG-312

(error) The user data of scaling library '%s' does not match that of the link library '%s'. The scaling group cannot be formed.

Description

The *define_scaling_lib_group* command requires library user data to be consistent between each scaling library and the link library. This error message indicates that the command found inconsistent user data.

What Next

Make sure that the *define_scaling_lib_group* command specifies a list of libraries with user data consistent with the link library.

See Also

- define_scaling_lib_group

SLG-313

(error) Arc %s in library %s arc group index is different from the index of the library group. The scaling group cannot be formed.

Description

The *define_scaling_lib_group* command requires each library arc index in the arc group to match its library index in the library group. This error message indicates that the command found inconsistent arc group index data.

What Next

Make sure that each library arc is present in all libraries in the scaling library group defined by the *define_scaling_lib_group* command.

See Also

- define_scaling_lib_group

Feedback

SLG-314

(error) Pin '%s' in library '%s' pin group index is different from the index of the library group. The scaling group cannot be formed.

Description

The *define_scaling_lib_group* command requires each library pin index in the pin group to match its library index in the library group. This error message indicates that the command found inconsistent pin group index data.

What Next

Make sure that each library pin is present in all libraries in the scaling library group defined by the *define_scaling_lib_group* command.

See Also

- define_scaling_lib_group

SLG-315

(error) Invalid set of libraries '%s' passed to define_scaling_lib_group. Multi-dimension scaling requires the number of libraries to be at least the number of dimensions plus one.

Description

The *define_scaling_lib_group* command requires the number of libraries in a group to be at least the number of scaling dimensions plus one. This error message indicates that too few libraries were listed.

What Next

Check numbers of process, temperature, and voltage rail values. Make sure that the number of scaling libraries is at least the number of scaling dimensions plus one.

See Also

- define_scaling_lib_group

SLG-316

(error) Library '%s' already belongs to a scaling library group.

Description

A library listed in the *define_scaling_lib_group* command already belongs to a scaling library group. Each library can belong to no more than one scaling library group.

Feedback

What Next

Report the existing library groups using the *report_lib_groups* command. You can create multiple scaling library groups to cover different parts of the design, but each library can belong to no more than one group.

See Also

- define_scaling_lib_group
- report_lib_groups
- SLG-201
- SLG-202
- SLG-203
- SLG-205

SLG-317

(error) No library in the scaling library group was found in the link path specified by the link_path and link_path_per_instance variables. Creation of the scaling group failed.

Description

The *define_scaling_lib_group* command requires exactly one library of a scaling library group to be in the link path specified by the *link_path* and *link_path_per_instance* variables. The remaining scaling libraries are automatically read in to create the group. This error message indicates that no scaling library was found in the link path.

What Next

Change either the link path or the *define_scaling_lib_group* command so that exactly one library in the scaling library group exists in the link path.

See Also

- define_scaling_lib_group
- link_path
- link_path_per_instance

SLG-318

(error) Parallel lib arc '%s' of cell '%s' is present in link library '%s' but not in scaling library '%s'. Scaling might not be performed for this arc.

Feedback

Description

The *define_scaling_lib_group* command requires every timing arc of every library cell in a link library to be also present in every scaling library. This error message reports a parallel arc of a library cell in a link library that does not exist in a scaling library. If the related scaling lib group is exact_match_only, calculation will fallback to link library arc lib data.

What Next

Make sure that all the libraries listed in *define_scaling_lib_group* command contain all of the library arcs in the linked libraries. Please check whether the same from lib pin and to lib pin contain different number of parallel arcs between link library and scaling library.

SLG-319

(error) define_scaling_lib_group cannot read library file %s, and creation of the scaling group failed.

Description

The *define_scaling_lib_group* command requires all lib file name must be valid library format. If user put non-library file, this command will fail.

What Next

Correct the wrong lib file.

See Also

- define_scaling_lib_group

SLG-320

(error) Cell '%s' hits scaling extrapolation problem, '%s' value '%f' is less than scaling range low value '%f'. Scaling calculation cannot be performed on this cell.

Description

Scaling calculation can only be done if one cell pvt is within the range of the scaling lib group.

What Next

Check problem cell operating condition and voltage setting, correct the design setting problem.

Feedback

See Also

- define_scaling_lib_group

SLG-321

(error) Cell '%s' hits scaling extrapolation problem, '%s' value '%f' is larger than scaling range high value '%f'. Scaling calculation cannot be performed on this cell.

Description

Scaling calculation can only be done if one cell pvt is within the range of the scaling lib group.

What Next

Check problem cell operating condition and voltage setting, correct the design setting problem.

See Also

- define_scaling_lib_group

SLG-325

(error) '%s' in define_scaling_lib_group command.

Description

The library number in *define_scaling_lib_group* command must be equal or greater than two.

What Next

Specify two or more than two libraries in the define_scaling_lib_group command.

See Also

- define_scaling_lib_group

SLG-328

(warning) Arc '%s' of cell '%s' is tagged as invalid in scaling library '%s'. This may affect scaling of this arc.

Feedback

Description

The *define_scaling_lib_group* command expects that every timing arc of every library cell in a link library will also be present in every scaling library. This warning message reports an arc of a library cell in a scaling library that has been explicitly tagged as invalid. Scaling calculations will be done for the arc as if it did not exist in that scaling library. One-dimensional scaling may have degraded accuracy or may result in an exprapolation error and multi-dimensional scaling may fail completely, with calculation falling back to link library arc data. If the related scaling lib group is exact_match_only and the invalid arc is an exact match, calculation will fall back to link library arc lib data.

What Next

Confirm that this is the expected behavior, and that the scaling group structure and design operating conditions are compatible with the presence of the invalid arc data.

SLG-330

(error) in the define_scaling_lib_group command, there are at least two libraries share the same name '%s', and they have same process, temperature and voltage definition. Creation of scaling group failed.

Description

The libraries in one define_scaling_lib_group command should not have exactly same process, temperature and voltage definition, when detect their names are also same, define_scaling_lib_group command disallows such duplicate library usage.

What Next

Fix the scaling library group, and rerun your script.

See Also

- define_scaling_lib_group

SLG-331

(warning) In the define_scaling_lib_group command, library '%s' and '%s' have same process, temperature and voltage definition.

Description

In order to do scaling calculation, any two libraries in one define_scaling_lib_group command should not have exactly same process, temperature and voltage.

Feedback

What Next

User should check and correct the wrong library in the define_scaling_lib_group command.

See Also

- define_scaling_lib_group

SLG-332

(warning) Detect best-match failure for the cell timing %s in %s calculation, using best-match library.

Description

If you use the *define_scaling_lib_groups* command with the *-best_match* option, when one cell PVT exceeds best-match threshold, and if timing_use_link_library_on_best_match_failure is false, calculation will still choose the library with closest PVT.

What Next

This warning message means reported cell pvt exceeds best-match threshold. User needs to check whether the PVT and define_scaling_lib_group threshold settings are correct or not. User can modify define_scaling_lib_group -p_abstol, -v_abstol or -t_abstol to loose the threshold if both cell PVT and used library are expected.

See Also

- timing_use_link_library_on_best_match_failure

SLG-333

(warning) Detect best-match failure for the cell timing %s in %s calculation, using link library.

Description

If you use the *define_scaling_lib_groups* command with the *-best_match* option, when one cell PVT exceeds best-match threshold, and if timing_use_link_library_on_best_match_failure is true, calculation will still choose the link library.

What Next

This warning message means reported cell pvt exceeds best-match threshold. User needs to check whether the PVT and define_scaling_lib_group threshold settings are correct or

Feedback

not. User can modify define_scaling_lib_group -p_abstol, -v_abstol or -t_abstol to adjust the threshold.

If user want to choose library with closest PVT instead of link library in this case, user can disable variable timing_use_link_library_on_best_match_failure.

See Also

- timing_use_link_library_on_best_match_failure

SLG-350

(warning) Detect 3 or higher dimension scaling.

Description

Accurate scaling can only be performed on 1 or 2 dimension scaling, when detect 3 or higher dimension, scaling will fallback less accurate mode.

What Next

Use report_lib_group -scaling -show {process voltage temperature} to see whether the high dimension scaling is desired or not. Use define_scaling_lib_group -excluded_rail_names or set_disable_pg_pins to reduce scaling dimension if need.

See Also

- define_scaling_lib_group
- set_disable_pg_pins

SLG-401

(error) Pin '%s' of cell '%s' library '%s' data is present in link library '%s', but it is not present in scaling library '%s'. This type library data scaling will not be performed for this pin.

Description

Scaling requires library data is consistent across all libraires in the group. If one pin lib data exists in link library but doesn't exist in scaling library, this message will be displayed.

What Next

Check and correct the missing library data in the scaling library.

Feedback

See Also

- define_scaling_lib_group

SLG-402

(error) Arc '%s' of cell '%s' library '%s' data is present in link library '%s', but it is not present in scaling library '%s'. This type library data scaling will not be performed for this arc.

Description

Scaling requires library data is consistent across all libraires in the group. If one arc lib data exists in link library but doesn't exist in scaling library, this message will be displayed.

What Next

Check and correct the missing library data in the scaling library.

See Also

- define_scaling_lib_group

SLG-403

(error) Pin '%s' of cell '%s' library '%s' data isn't consistent between link library '%s' and scaling library '%s', this type library data scaling will not be performed for this pin.

Description

Scaling requires library data is consistent across all libraires in the group. If one pin lib data are not consistent between link library and scaling library, this message will be displayed.

What Next

Check and correct the missing library data in the scaling library. If the error is related to CCS Noise model consistency but library group has corresponding CCSN models, please enable rc_ccsn_enable_library_error_reporting to check if any CCSN model is invalidated by CCS Noise model checking.

See Also

- define_scaling_lib_group
- rc_ccsn_enable_library_error_reporting

Feedback

SLG-404

(error) Arc '%s' of cell '%s' library '%s' data isn't consistent between link library '%s' and scaling library '%s', this type library data scaling will not be performed for this arc.

Description

Scaling requires library data is consistent across all libraires in the group. If one arc lib data are not consistent between link library and scaling library, this message will be displayed.

What Next

Check and correct the missing library data in the scaling library.

See Also

- define_scaling_lib_group

SLG-405

(warning) Pin '%s' of cell '%s' library '%s' data isn't consistent between link library '%s' and scaling library '%s', partial scaling will be performed on those consistent data.

Description

Scaling requires library data is consistent across all libraries in the group. If there are some partial lib data are consistent across the lib group, scaling will only be performed on those consistent lib data and this message will be displayed.

What Next

Check and correct the missing library data in the scaling library.

See Also

- define_scaling_lib_group

SLG-417

(information) The arc '%s' in lib cell '%s' in scaling library '%s' has significantly different output-capacitance indexes with link library '%s'; this can adversely affect scaling accuracy.

Description

The *define_scaling_lib_group* requires ccs receiver cap indexes are closed between scaling library and link library, big difference could result in accuracy problem.

What Next

Ensure that the set of arcs and pins is identical across the members of the scaling library groups. The positions of the arcs and pins within the libraries must be the same as well.

The output-capacitance indexes used for Composite Current Source (CCS) driver data is better to have identical values across the libraries. If this is not satisfied, the SLG-417 message is issued.

See Also

- define_scaling_lib_group

SLG-418

(warning) Timing analysis accuracy will be degraded because of problems with scaling group or library data.

Description

The *define_scaling_lib_group* requires library data is consistent across all scaling libraries in the scaling group. If there is severe library data missing or inconsistency, it will bail out with SLG-001. If user enable variable timing_continue_on_slg001 to ignore the problem, this message will be displayed with a list of offending scaling check errors.

What Next

Correct all the library data issues for the offending check errors.

See Also

- define_scaling_lib_group

SLG-419

(error) DCALM failed on cell %s as its libcell %s is not found in the specified dcalm library.

Description

The *define_cell_alternative_lib_mapping* command requires the libcell of the specified cell to exist in the dcalm library specified. If not dcalm will not be applied on the cell.

What Next

Please use the library which has the libcell for the cell used in the DCALM.

Feedback

SLG-420

(warning) Certain cells or pins are excluded from check_timing operating conditions or signal level, the results should not considered for signoff.

Description

The message warns that a few cells or pins are excluded from timing checks of operating conditions or signal level using set_check_operating_condition_exclude command. The results of the check_timing command ignores the said checks and PrimeTime does not recommend considering the results for signoff.

What Next

Please resolve all the errors without excluding cells or pins.

See Also

- check_timing

SLOC

SLOC-001

(error) can no longer enable source file information capture.

Description

This message is issued if you attempt to enable source file location capture after the first target SDC command is input.

What Next

Control the setting of the variable before reading and inputting SDC commands.

See Also

- reset_design
- sdc_save_source_file_information

SLOC-002

(warning) comment string is truncated, not to exceed %d Bytes.

Feedback

Description

The comment string specified by the previous SDC command *-comment* option is too long, exceeding a discretionary length specified in the message. The comment string is still stored; however, only the initial number of characters specified in the message are kept, and the remainder is ignored.

What Next

Ensure that the process creates command comments limited to the length indicated in the message.

See Also

- read_sdc

SLOC-003

(warning) comment string storage exceeded; comment will be ignored.

Description

The total budgeted storage area for SDC command comment strings has been exhausted such that the string associated with the previous command cannot be saved and is therefore ignored. This discretionary limit bounds the capacity impact of storing SDC comment strings.

What Next

Control and reduce command comment lengths to reduce the overall memory footprint.

See Also

- read_sdc

SML

SML-001

(warning) '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which Synopsys tool is running.

Low memory availability

Feedback

```
----------------------
o This message indicates that the host is running low on
  available memory to service the processes its running.
o This event arises where the current process is running
  on a host with insufficient ram or is being starved of
  ram by other processes running on the host. It is
  detected where there sum of the free memory and cached
  memory is <5% of the total ram in the host.
o Run Synopsys tool on a host with sufficient ram or on a host
  where it is not competing with other processes for ram.
```

SML-002

(warning) '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which Synopsys tool is running.

High cpu utilization (current process <5%)

```
----------------------------------------
o This message indicates that the host is heavily loaded
  by all the processes running on it and that the current
  process is experiencing cpu starvation.
o This event arises where the current process is running
  on a host where it is only utilizing <5% of the total
  cpu capability, yet the host is running at >95% load.
o Run Synopsys tool on a host with sufficient cores to satisfy
  the number of cores Synopsys tool is specified to use.
  If the run is on a farm host, ensure the number of slots
  reserved on the host is sufficient to reserve the number
  of cores Synopsys tool is specified to use.
```

SML-003

(warning) '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which Synopsys tool is running.

High network packet retransmission

```
--------------------------------
o This message indicates that the host is encountering
  poor network connectivity and that the percentage of
  packets shown, hast to be retransmitted.
o This event arises where the current process is running
```

Feedback

```
  on a host where >5% of all packets being transmitted
  had to be retransmitted due to loss or damage. It is
  an indicator that the network to which the host is
  connected is heavily congested.
o Contact your IT department to check with the host/network
  connectivity problem.
```

SML-004

(warning) '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which Synopsys tool is running.

High network packet loss

```
------------------------
o This message indicates that the host is encountering
  poor network connectivity and that the percentage of
  packets shown, are being lost.
o This event arises where the current process is running
  on a host where >5% of the network packets it is sending
  are not being received by their intended recipient.
o Contact your IT department to check with the host/network
  connectivity problem.
```

SML-005

(warning) '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which Synopsys tool is running.

High network latency to hosts

```
----------------------------
o This message indicates that the host is encountering
  poor network connectivity to the hosts indicated and
  the associated latency.
o This event arises where the current process is running
  on a host where it has TCP connections to another
  host and the network latency is >300ms. It is an
  indicator that the network to which the host is
  connected is heavily congested or there is a problem
  with networking hardware.
o Contact your IT department to check with the host/network
  connectivity problem.
```

Feedback

SML-007

(warning) '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which Synopsys tool is running.

Low memory and pagecache availability

```
-----------------------
o This message indicates that the host is running low on
  available memory and the available pagecache space to
  service the processes its running.
o This event arises where the current process is running
  on a host with insufficient ram or is being starved of
  ram by other processes running on the host. It is
  detected when free memory is <5% of the total ram in the
  host and the system's pagecache size drops below 15% of
  the total virtual memory of the process.
o Run Synopsys tool on a host with sufficient ram or on a host
  where it is not competing with other processes for ram
  and pagecache.
```

SML-008

(warning) '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which Synopsys tool is running.

Low core availability

```
----------------------------------------
o This message indicates that the host is loaded by other
  processes running on it and as a result the current process
  does not have the expected number of cores available to it.
  For example, if Synopsys tool is specified to use 16 cores,
  the process is expected to have 16 cores available to it.
o This event arises when the number of cores available to the
  current process falls below 75% of the expected amount.
o Terminate other processes running on the same host, or
  run Synopsys tool on a host with sufficient cores to satisfy
  the number of cores Synopsys tool is specified to use and the
  other processes.
```

Feedback

SML-100

(information) '%s'

Description

The Synopsys Monitoring Library has detected the resource issue indicated with the host on which Synopsys tool is running is resolved.

SML-500

(information) disabled the Synopsys Monitoring Library.

Description

The Synopsys Monitoring Library is disabled and will not monitor critical system throughout the runtime.

What Next

No action is needed from the user.

SML-501

(warning) failed to start the Synopsys Monitoring Library: '%s'

Description

The Synopsys Monitoring Library failed to start due to the given reason.

What Next

If monitoring of the critical resources is needed, correct the problem reported and restart the Synopsys tool, otherwise this warning can be ignored.

SML-502

(warning) failed to stop the Synopsys Monitoring Library: '%s'

Description

The Synopsys Monitoring Library failed to stop due to the given reason.

What Next

If monitoring of the critical resources is needed correct the problem reported and restart the Synopsys tool, otherwise this warning can be ignored.

Feedback

SPFP

SPFP-001

(error) Cannot open file '%s'.

Description

The named parasitics file cannot be opened.

What Next

Validate that the file name is correct.

SPFP-002

(error) Could not determine the format of parasitics file:\n \t'%s'

Description

The named parasitics file was opened, but the format of the file (DSPF, RSPF, SPEF) could not be determined.

What Next

Validate that the file is a properly formatted parasitics file in one of the supported formats.

SPFP-010

(error) %s syntax error: %s\n \tat line %d near '%s' in file '%s'

Description

A syntax error was found while reading the indicated type of parasitics file. A nearby line is given to help you isolate the problem.

What Next

This message covers a wide variety of syntax errors. Review the line number reported in the message and determine if the writer of the parasitics file has introduced a syntax error.

SPFP-011

(error) Unknown %s construct '%s'\n \tat line %d in file '%s'

Feedback

Description

An unexpected or unknown construct was found while reading a parasitics file of the indicated format, This will often be followed by a general syntax error, *PARA-010*.

What Next

Review the line number reported in the message and determine if the writer of the parasitics file has introduced an unknown construct.

SPFP-012

(warning) Missing '*|GROUND_NET' statement in SPF file '%s'\n \tUsing 'vss', 'VSS', 'gnd' and 'GND'

Description

The GROUND_NET statement is missing from the named DSPF or RSPF file.

What Next

This is just a warning to indicate that default values will be used.

SPFP-013

(warning) name DELIMITER and hierarchy DIVIDER are the same!\n \tSome objects may not be found, and performance may be affected.

Description

The hierarchy divider and pin delimiter in the named parasitics (SPEF, DSPF, RSPF) file are the same. This may not be completely supported. Some net or pin objects may not be found, and performance may be adversely affected.

What Next

Modify your use of the application which generated the parasitics file and regenerate it using different (or default) DELIMITER and DIVIDER. Synopsys strongly recommends that for the best performance, you should use different characters for the hierarchy delimiter and name delimiter.

SPFP-014

(warning) %s value %g exceeds user-defined threshold\n \tat line %d in file '%s'.

Feedback

Description

You receive this message if the parasitics file contains a capacitance value (in picofarads) or a resistance value (in ohms) that exceeds user-defined thresholds, as specified by the *parasitics_cap_warning_threshold* and *parasitics_res_warning_threshold* variables. This warning is intended to assist you in detecting large, unexpected values generated by other applications. The specified value is still used by the application.

What Next

This is a warning message only; no action on your part is required. However, you can change the thresholds by setting the *parasitics_cap_warning_threshold* and *parasitics_res_warning_threshold* variables to different values, or to 0.0 (the default) to suppress the generation of this message. For more information, see the manual pages of these variables.

See Also

- parasitics_cap_warning_threshold
- parasitics_res_warning_threshold

SPFP-015

(warning) value %g exceeds maximum. Using %g instead,\n \tat line %d in file '%s'.

Description

You receive this message if the parasitics file contains a value which, after unit conversion, exceeds the maximum value allowed.

What Next

You can try to correct the syntax error manually. However, since SPF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-100

(error) Expected %skeyword %s but found '%s'\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has a syntax error where a specific keyword was expected (for example, *D_NET), but something else was found. The file name and line number are given so you can isolate the problem.

Feedback

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-101

(error) Invalid %s '%s'%s\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has a syntax or semantic error in a number of different constructs. The message will indicate the type of construct and what part of it is invalid. Some examples include:

- You specified a DIVIDER, DELIMITER, or BUS_DELIMITER which is outside of the allowed set of values for the construct
- Any of the header unit constructs has an invalid number or multiplier string.
- A port or D_NET connectivity entry has an invalid direction.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-102

(error) NAME_MAP syntax error at '%s'\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has a syntax or semantic error in an entry in the NAME_MAP section of the file.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-103

(error) %s requires %d or more %s's\n \tat line %d in file '%s'.

Feedback

Description

Many sections of the SPEF file require one or more sub sections of a specific type. You receive this message if the SPEF file violates that semantic. Some examples include:

- The *CAP section of a D_NET, if specified, requires one or more capacitor elements.
- The *RES section of a D_NET, if specified, requires one or more resistor elements.
- The connectivity section of a D_NET requires one or more *P or *I sub sections.
- The *POWER_NETS and *GROUND_NETS sections, if specified, require one or more net names.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-104

(error) %s requires %s\n \tat line %d in file '%s'.

Description

Some sections of the SPEF file require a specific sequence of sub sections. You receive this message if the SPEF file violates that semantic. Generally, this message is reserved for some rarely used sections of the file, like *DEFINE.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-105

(error) Invalid node name '%s'\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has a syntax or semantic error in a node name, which is used in several places in the *RES and *CAP sections. The specific node name which is in error is shown in the message. A node name is either a port name, an instance pin name (an instance name or name map id, followed by the pin delimiter, followed by a pin name or name map id), or an internal node name (a net name, followed by the pin delimiter, followed by a positive integer).

Feedback

The SPEF specification details the various possible forms for a node name.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-106

(error) Strict SPEF syntax error: invalid %s %s\n \tat line %d in file '%s'.

Description

Historically, there are a number of SPEF writers which write illegal SPEF. For backward compatibility with existing questionable SPEF files, the parser allows a number of forms which are strictly illegal. If the parser is in *strict* mode, you will receive this error when one of these strict-SPEF rules is violated.

What Next

The first thing to try is to turn off strict mode. Or, you can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-107

(error) Expected %s but found '%s'\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has a construct in the wrong place or out of order. Some examples include:

- The *D_NET section expects a certain series of optional sub sections. A SPEF keyword which is not a valid *D_NET sub section was found where a *D_NET sub section was expected.
- The *S connectivity attribute has some optional thresholds which must be positive fractions (between 0 and 1). The value found is not a positive fraction.
- Several sections of the SPEF file require a positive integer, and that was not found.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine-generated and extremely large, you will most likely need to work with the vendor of the application that wrote the file to correct the syntax.

Feedback

SPFP-108

(error) Invalid value '%s'\n \tat line %d in file '%s'.

Description

Many sections of the SPEF file use values, or triplets of values. You receive this message if the SPEF file has a syntax error in a value. Values are used in the *L and *S connectivity attributes, total capacitance of a D_NET or R_NET, capacitances, resistances, poles and residues, and so on.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-109

(error) Syntax error in complex number: '%s %s%s%s%s%s'\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has a syntax error in a complex number. Complex numbers are used in the specification of poles and residues. They can be specified as (r i), or as a triplet such as (r i):(r2 i2):(r3 i3). The message will indicate the specific problem number.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-110

(error) Syntax error near '%s'\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has a syntax error not covered by any of the other syntax error messages. The token in question, as well as the file name and line number, will be given in the message.

Feedback

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-111

(error) Undefined name map index *%d referenced\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file finds a syntactically correct name map reference, such as *2379, but no such entry was ever defined in the NAME_MAP section.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-112

(error) Non-terminated comment starting at line %d\n \tof '%s'

Description

You receive this message if the SPEF file contains a multi-line comment, which begins with /*, but does not end. This message is intended to help you find the line where the non-terminated comment starts.

What Next

You can try to correct this error manually by terminating or removing the comment. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-113

(error) Premature end-of-file reading '%s'.

Description

You receive this message if the SPEF file ends unexpectedly, for example, in the middle of parsing required header sections, or before any D_NET or R_NET sections were found. A missing double quote in the header section can cause this error.

Feedback

What Next

You might be able to correct this error manually if this is caused by missing header sub-sections, or by a missing closing quote in one of the header sub sections. But, generally, it will be difficult to isolate the problem in a large file.

SPFP-114

(information) Ignored unsupported %s section starting at line %d\n \tof '%s'

Description

You receive this informational message if the SPEF file contains a construct which is being ignored, such as D_PNET and R_PNET.

What Next

No action is necessary.

SPFP-115

(error) BUS_DELIMITER cannot be the same as %s\n \tat line %d in '%s'.

Description

You receive this message if the BUS_DELIMITER is found to be the same as either the DIVIDER or the DELIMITER. SPEF does not allow this combination.

What Next

The SPEF file will almost certainly need to be regenerated.

SPFP-116

(error) Semantic error near '%s': %s\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file reader has found a semantic error. The token in question, the specific problem, and the file name and line number will be given in the message.

What Next

You can try to correct the error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the problem corrected.

Feedback

SPFP-117

(error) SENSITIVITY syntax error at '%s'\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has a syntax or semantic error in an entry in the SENSITIVITY section of the file.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-118

(error) Sensitivity factor syntax error at '%s'\n \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has an invalid value for a sensitivity factor. A sensitivity factor is supposed to be a floating point number.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-119

(error) Invalid parameter ID '%d' value in sensitivity \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has an invalid value for a variation parameter ID in the sensitivity section. The variation parameters are defined in the *VARIATION_PARAMETERS section and are supposed to be within the values defined in this section. This error indicates that the current parameter ID is outside the valid range.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

Feedback

SPFP-120

(error) Invalid parameter types for process parameter '%s' \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has an invalid type of process variation parameter. The variation parameters are defined in the *VARIATION_PARAMETERS section and allowed values are 'D', 'N' or 'X' type of process variation parameters. This indication implies whether the parameter affects capacitance, resistance and inductance in numerator (for 'N'), denominator (for 'D') or does not affect resistance (for 'X').

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-121

(error) Syntax error at line %d in file '%s'. Cannot \tdefine process variations after temperature variations.

Description

You receive this message if the SPEF file has temperature variations followed by process variations. It is expected that the file contains process variation parameters followed by temperature variations. The variation parameters are defined in the *VARIATION_PARAMETERS section.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-122

(warning) Invalid sensitivity for capacitance \tat line %d in file '%s'.

Description

You receive this message if the SPEF file has sensitivities for ground or coupling capacitances with respect to temperature variations or 'N' parameters to inform you that these sensitivities are illegal.

Feedback

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-123

(error) Syntax error at line %d in file '%s'. Expected \tto see keyword CRT2.

Description

You receive this message if the SPEF file has syntax errors in the definition of temperature variations. The variation parameters are defined in the *VARIATION_PARAMETERS section.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPFP-124

(error) Illegal name map index *%d referenced at line '%d' in file '%s'.

Description

You receive this message if the SPEF file finds a syntactically illegal name map reference, such as *-1. Such lines will be ignored.

What Next

You can try to correct the syntax error manually. However, since SPEF files are usually machine generated and extremely large, you will most likely need to work with the vendor of the application which wrote the file to get the syntax corrected.

SPICE

SPICE-001

(error) The aggressor cell driver pin '%s' is not connected.

Feedback

Description

The *write_spice_deck* command has found that the specified aggressor cell driver pin is not connected in the netlist.

What Next

Examine the netlist file, and determine if this is the case. Send the test case to Synopsys to debug this problem.

See Also

- write_spice_deck

SPICE-002

(error) The aggressor cell clock pin '%s' is not connected.

Description

The *write_spice_deck* command has found that the specified aggressor cell clock pin is not connected in the netlist.

What Next

Examine the netlist file, and determine if this is the case. Send the test case to Synopsys to debug this problem.

See Also

- write_spice_deck

SPICE-003

(warning) Unable to find the clock for pin '%s'.

Description

The *write_spice_deck* command cannot find the clock information related to the clock pin.

What Next

Examine the netlist file, and determine whether the specified pin is connected. Check the script to determine whether clocks are defined for the design. Check the design to determine whether it is properly constrained. When this warning is issued, a default clock period of 10 is assumed.

Feedback

See Also

- write_spice_deck

SPICE-004

(error) A conflict occurred in setting voltage level of pin '%s'. It is set to logic '%s'.

Description

The *write_spice_deck* command has tried to set the voltage level of the specified pin, whose level has been previously set.

What Next

Examine the netlist file, and determine that the voltage source is correct for the timing path generated. Change it if necessary.

See Also

- write_spice_deck

SPICE-005

(warning) Unable to find the arrival window for pin '%s'.

Description

The *write_spice_deck* command is not able to find the arrival window to write the correct piecewise linear waveform (PWL) for the pin.

What Next

Examine the netlist file, and verify that there is a timing path through the pin. If this is the case, send the test case to Synopsys for debugging.

See Also

- write_spice_deck

SPICE-006

(warning) Forced initialization of the output of the cell '%s' might be necessary because the timing path's data input pin '%s' is connected to timing path nets '%s'.

Feedback

Description

The *write_spice_deck* command has found that the data input pin is connected to a net in the timing path so no piecewise linear waveform (PWL) is generated for this pin.

What Next

You might have to add the initialization option in the spice deck that is generated to ensure the correctness of the timing path's initial state.

See Also

- write_spice_deck

SPICE-007

(warning) Forced initialization of the output of the cell '%s' might be necessary because the timing path's data input pin '%s' is connected to a feedback net '%s' driven by the same cell.

Description

The *write_spice_deck* command has found that the data input pin is connected to a net driven by the same cell so no piecewise linear waveform (PWL) is generated for this pin.

What Next

You might have to add the initialization option in spice deck that is generated to ensure the correctness of the timing path's initial state.

See Also

- write_spice_deck

SPICE-008

(warning) The timing path data input pin '%s' is driven by a %s clock net '%s'.

Description

The *write_spice_deck* command has found that the data input pin is driven by a timing path clock net so no piecewise linear waveform (PWL) is generated for this pin.

What Next

You might have to increase all PWLs by a few clock periods.

Feedback

See Also

- write_spice_deck

SPICE-009

(warning) The timing path data input pin '%s' is driven by a %s clock cell '%s'.

Description

The *write_spice_deck* command has found that the data input pin is driven by a timing path clock cell so no piecewise linear waveform (PWL) is generated for this pin.

What Next

You might have to increase all PWLs by a few clock periods.

See Also

- write_spice_deck

SPICE-010

(warning) The timing path data pin '%s' is connected to an aggressor '%s'. Please check the PWL and voltage source of the aggressor's driver.

Description

The *write_spice_deck* command has found that the data input pin is driven by an aggressor so no piecewise linear waveform (PWL) is generated for this pin.

What Next

You might have to inspect the aggressor's driver PWL and voltage source or increase all PWLs for a few clock periods.

See Also

- write_spice_deck

SPICE-011

(warning) The timing path data pin '%s' is connected to an aggressor cell '%s'. Please check the PWL and voltage source of the aggressor's driver.

Feedback

Description

The *write_spice_deck* command has found that the data input pin is driven by an aggressor cell so no piecewise linear waveform (PWL) is generated for this pin.

What Next

You might have to inspect the aggressor's driver PWL and voltage source or increase all PWLs for a few clock periods.

See Also

- write_spice_deck

SPICE-012

(error) The timing path sequential data input pin '%s' is not connected.

Description

The *write_spice_deck* command has found that the timing path sequential data input pin is not connected in the netlist.

What Next

Examine the netlist file and determine if this is the case. You might have to inspect or generate it's piecewise linear waveform (PWL) or voltage source. If timing path sequential data input pin is is connected, send the test case to Synopsys to debug this problem.

See Also

- write_spice_deck

SPICE-013

(warning) A conflict occurred in setting the switching direction of pin '%s'. It is set to '%s'.

Description

The *write_spice_deck* command has tried to set the switching direction of the specified pin on which the direction was previously set. It usually indicates that the aggressor is coupled with at least two nets in the timing path that are switching in the opposite directions. There are conflicting requirements of the switching direction (sense) of the aggressor input pin. In this case, *write_spice_deck* choose the rising direction.

Feedback

What Next

Examine the netlist file, and verify that the switching is correct for the timing path generated. Change the switching direction if it is better for the delay analysis of the path.

See Also

- write_spice_deck

SPICE-014

(warning) The timing path cell side pin '%s' is driven by an aggressor '%s' that is set to %s.

Description

The *write_spice_deck* command has found that the side pin of a timing path cell is driven by the specified aggressor.

What Next

Examine the netlist file, and verify the connection and switching direction of the aggressor. Change them if necessary.

See Also

- write_spice_deck

SPICE-015

(warning) A conflict occurred in setting the voltage level of the aggressor '%s'. It is set to '%s'.

Description

The *write_spice_deck* command has tried to set the voltage level of the specified aggressor on which the voltage level was previously set.

What Next

Examine the netlist file, and verify that the voltage level is correct for the timing path generated. Change it if necessary.

See Also

- write_spice_deck

Feedback

SPICE-016

(information) The aggressor-driven latch '%s' is in transparent mode. The data pin is '%s'.

Description

The *write_spice_deck* command has found that the specified aggressor-driven latch in the spice deck is in transparent mode.

What Next

This is an informational message only. No action is required on your part. However, you can examine the netlist file and verify that the piecewise linear waveform (PWL) and voltage sources of the date pin and gate pin are correct for the timing path generated. Change them if necessary.

See Also

- write_spice_deck

SPICE-017

(information) The side pin '%s' is set to '%s'.

Description

The *write_spice_deck* command has set the specified side pin to the specified logic level.

What Next

This is an informational message only. No action is required on your part. However, you can examine the netlist file and verify that the voltage source of the side pin is correct for the timing path generated. Change it if necessary.

See Also

- write_spice_deck

SPICE-018

(information) The cell '%s' has potential multi-input switching on pin(s) %s.

Description

The *write_spice_deck* command has found that the pin on the cell is connected to switching net along the path. The specified side pins could be switching at the same time as primary pin on the path due to tie-off or upstream logic. *write_spice_deck* attempts to duplicate this cell to resolve this issue.

Feedback

What Next

You can examine the netlist file and verify that the logic connected to side pins will allow the signal to propagate through the cell. Disconnect and change the voltage on conflicting side pins if necessary.

See Also

- write_spice_deck

SPICE-019

(information) The setting of aggressor '%s' is changed from '%s' to '%s'.

Description

The *write_spice_deck* command has found that the aggressor logic needs to be changed as specified to satisfy the sensitization of a side pin.

What Next

This is an informational message only. No action is required on your part. However, you can examine the netlist file and verify that the voltage of the aggressor has the correct effect on the side pin for the timing path generated. Change it if necessary.

See Also

- write_spice_deck

SPICE-020

(information) The spice deck that is generated has PWLs for you to verify.

Description

The *write_spice_deck* command has generated piecewise linear waveforms (PWLs) to stimulate the timing path.

What Next

This is an informational message only. No action is required on your part. However, you can examine the netlist file and verify the correctness of the PWLs for the timing path generated. Change them if necessary.

See Also

- write_spice_deck

Feedback

SPICE-021

(warning) Unable to propagate the side pin value '%s' backward through the aggressor arc %s -> %s due to a side pins sensitization problem.

Description

The *write_spice_deck* command is unable to sensitize the specified aggressor cell arc to generate the specified logic value.

What Next

Examine the spice deck generated, and manually sensitize the arc to the specified logic value.

See Also

- write_spice_deck

SPICE-022

(error) Unable to trace the clock tree from pin '%s' of cell '%s'.

Description

The *write_spice_deck* command is unable to trace the clock tree path from the specified pin due to a missing clock tree in PrimeTime's internal data structure.

What Next

Examine the spice deck generated, and determine if the error will affect the spice run. Change the spice deck manually if necessary.

See Also

- write_spice_deck

SPICE-023

(warning) A subckt declaration has no name in the file specified by the -sub_circuit_file option.

Description

The *write_spice_deck* command used with the *-sub_circuit_file* option has found a subcircuit declaration without a name in the SPICE pin order file.

What Next

Examine the spice pin order file, and remove the subcircuit declaration. Correct the file if necessary.

See Also

- write_spice_deck

SPICE-024

(warning) The subckt '%s' declaration occurs without a pin in the file specified by the -sub_circuit_file option.

Description

The *write_spice_deck* command used with the *-sub_circuit_file* option has found a subcircuit declaration without a pin in the SPICE pin order file.

What Next

Examine the spice pin order file, and remove the subcircuit declaration or add a subcircuit pin definition.

See Also

- write_spice_deck

SPICE-025

(warning) Unable to find the delay of port '%s'.

Description

The *write_spice_deck* command cannot find the delay of the specified input port.

What Next

Use the *set_input_delay* command to define the delay for the port.

See Also

- set_input_delay
- write_spice_deck

Feedback

SPICE-026

(warning) Negative start time '%g' for PWL is generated. The initial_delay, %s delay and slew time are %g, %g and %g, respectively.

Description

The *write_spice_deck* command generated a negative start time for a PWL.

What Next

Use the *-initial_delay* option to define a larger initial delay to make the start time non-negative.

See Also

- write_spice_deck

SPICE-027

(warning) SPICE deck generation for non-delay timing arc (%s -> %s) is not supported.

Description

The *write_spice_deck* command can't generate the deck for non-delay arc.

What Next

Check the arc specification for the get_timing_arcs is correct or not.

See Also

- write_spice_deck

SPICE-028

(error) -analysis_type cannot be specified for timing path.

Description

The option -analysis_type of *write_spice_deck* command is applicable only for crosstalk delay and noise analysis on a timing arc.

What Next

Don't use this option when writing the spice deck for the timing path.

Feedback

See Also

- write_spice_deck

SPICE-029

(information) -analysis_type is not set for timing arc. max_rise assumed.

Description

The *write_spice_deck* command didn't find the option -analysis_type for timing arc.

What Next

Specify the option when writing the spice deck of a timing arc.

See Also

- write_spice_deck

SPICE-030

(Error) Unable to find clock for the pin '%s' of the driving cell of the port '%s'.

Description

The *write_spice_deck* can't find the clock to the sequential driving cell of a port.

What Next

Specify a valid clock or replace it with a combinatorial driving cell in the *set_driving_cell* command.

See Also

- write_spice_deck
- set_driving_cell

SPICE-031

(Error) Erroneous %s arrival window(min %g max %g)of the pin '%s'.

Description

The *write_spice_deck* found problem with the arrival window of the pin

Feedback

What Next

Check for related messages from update_timing about delay calculation and try to remove them.

See Also

- write_spice_deck

SPICE-032

(warning) Unable to find library cell '%s'.

Description

The *write_spice_deck* can't find the library cell in the library specified in the set_driving_cell command or the libraries used by the current design.

What Next

Check the library name and library cell name of the set_driving_cell command.

See Also

- write_spice_deck
- set_driving_cell

SPICE-033

(error) The cell arc in '%s' and the %s is not in one stage.

Description

The *write_spice_deck* find that the cell arc and the net arc specified don't for a single stage.

What Next

Specified the correct cell arc that drives the net arc with this option.

See Also

- write_spice_deck

Feedback

SPICE-034

(information) There are %d simulation sweeps from %d sweep points for %d active aggressors.

Description

The *write_spice_deck* generated the number of SPICE sweep described above.

What Next

The SPICE run time may be large if the sweep is large.

See Also

- write_spice_deck

SPICE-035

(information) The plateau time (%g) of the clock pin '%s' is %s to %g%% of the period (%g) due to the skew of rise and fall delay.

Description

The *write_spice_deck* find that the delay skew between different edges of the clock pin might cause clock waveform problem.

What Next

Examinate the clock network.

See Also

- write_spice_deck

SPICE-036

(error) The clock period on pin '%s' is too small for the rise and fall transitions to happen.

Description

The *write_spice_deck* found that the transition times of the clock pin are too large that the clock pulse will not reach logic one or logic zero state.

For example: The rise and fall slews are 0.1ns with 30-70 trip points and clock period is 0.3ns. When the slew values are converted to 0-100 points, the clock period is not large enough to hold the rising and falling edges completely inside the period.

Feedback

What Next

Increase the clock period or speed up the transition times of the pin.

See Also

- write_spice_deck

SPICE-037

(error) Can't specify both '%s' and '%s' options.

Description

The *write_spice_deck* find the two incompatible options.

What Next

Specified the correct the options.

See Also

- write_spice_deck

SPICE-038

(warning) Can't align the aggressor '%s' (input pin '%s'.)

Description

The *write_spice_deck* wasn't able to align the aggressor.

What Next

Sweep the input pin to find the worst case aggressor switching time.

See Also

- write_spice_deck

SPICE-039

(warning) The aggressor alignment for pin '%s' may not be the worst case because '%s'.

Feedback

Description

write_spice_deck or *sim_validate_stage* command wasn't able to align the aggressors of the victim net for its worst case. Sweeping the aggresssors over a small window might be needed.

What Next

Make sure you are using the above mentioned feature on this pin. If you cannot, and *write_spice_deck* command is used, use sweep option or manually sweep the generated spice deck for input pins of all aggressors to find the wost case alignment.

See Also

- write_spice_deck
- sim_validate_stage

SPICE-040

(Error) The non-positive value (%g) specified by the option '%s'.

Description

The option value of the *write_spice_deck* must be a positive floating point number.

What Next

Set a positive floating point number.

See Also

- write_spice_deck

SPICE-041

(information) The option '%s' is ignored for the %s.

Description

The option of the *write_spice_deck* is ignore. number.

What Next

Remove the option from the write_spice_deck command.

See Also

- write_spice_deck

Feedback

SPICE-042

(Error) Unable to write spice deck for the %s '%s' without appropiate annotated RC parasitic.

Description

The *write_spice_deck* cannot write out the spice deck. This may be because there is no annotated RC or no coupling in the noise analysis.

What Next

Use another cell or net arc with the appropiate RC parasitics.

See Also

- write_spice_deck

SPICE-043

(Error) Unable to find the %s %s library pin '%s' of the set_driving_cell '%s' in the library '%s'.

Description

The *write_spice_deck* can't found the library pin specified in the set_driving_cell command.

What Next

Specify the correct pin name on the set_driving_cell command.

See Also

- write_spice_deck

SPICE-044

(Error) Unable to find the library '%s' for the set_driving_cell '%s'.

Description

The *write_spice_deck* can't found the library specified in the set_driving_cell command.

What Next

Specify the correct library name on the set_driving_cell command.

Feedback

See Also

- write_spice_deck

SPICE-045

(Error) Unable to find any cell arc.

Description

You used a net timing_arc object to *write_spice_deck* which had no proper driver cell. The *write_spice_deck* cannot be performed on a stage that has no driver cell arc.

What Next

Either use the correct net timing_arc object to *write_spice_deck*, or enable at least one of the cell timing arcs that drives the net.

See Also

- write_spice_deck

SPICE-046

(Error) Sequential driving cell '%s' of the clock port '%s' is not supported.

Description

You used a sequential library cell to drive a clock port. The *write_spice_deck* cannot write out correct voltage sources to generate the clock pulse required.

What Next

Please use combinatorial library cells to drive clock port.

See Also

- write_spice_deck

SPICE-047

(Error) Unable to find the clock for clock pin '%s'.

Description

The *write_spice_deck* cannot find the (generated) clock for the clock pin. It can't write out the SPICE pulse statement related to the clock pin.

Feedback

What Next

Please properly define the clock related to the clock pin in PrimeTime.

See Also

- write_spice_deck

SPICE-048

(Warning) Unsupport timing path type.

Description

The *write_spice_deck* doesn't support the path type generated by the get_timing_paths.

What Next

Please generate only the full path.

See Also

- write_spice_deck

SPICE-049

(Error) Spice deck cannot be written because %s

Description

The *write_spice_deck* command cannot write the spice deck for one of the following reasons.

The spice deck needs input stimulus to be applied on an internal pin of cell, which is not possible with spice models.

Find that multiple inputs of cell connected to same net on correlated path/stage.

Library scaling flow is not supported for Spice correlation purpose.

What Next

Reconsider the inputs given to spice deck or try to eliminate the possibility of having cells with internal pins in spice deck, or use non-scaling flow.

Feedback

See Also

- set_si_delay_analysis
- write_spice_deck

SPICE-050

(warning) Net '%s' has no RC parasitics.

Description

The net referenced above does have parasitics annotated on it. The spice deck written out will use wire load capacitance, if available and models the net as ideal net.

What Next

Check for the parasitics annotated on the net and try to annotate detailed parasitics on the net.

See Also

- write_spice_deck
- report_annotated_parasitics
- read_parasitics

SPICE-051

(warning) Failed to sensitize cell '%s'.

Description

Automatic sensitization of *write_spice_deck* command has failed to sensitize the above referenced cell. In this case, a default voltage (zero voltage) will be used for all the side input pins.

Sensitization can fail for many reasons. Common reasons are insufficient information in the Liberty library, which was used during its characterization, or user set disable timing on all cell arcs from/to related pin. SPICE-051 is more common to see on sequential cells for two reasons: 1) sequential cell is complicated and when condition is not enough, sensitization vector is needed. 2) sequential cell data pin is connected to on-path net, and there is no pin-based CCST receiver model with when condition on data pin. This means there is no when condition available in library for cell sensitization.

Feedback

What Next

Provide the information of how the cell was sensitized during its characterization, as part of Liberty sensitization language. Check disable timing settings on the cell.

See Also

- sim_validate_path
- sim_validate_stage
- write_spice_deck

SPICE-052

(warning) Write spice deck does not support scaling of multi-rail cells %s.

Description

The *write_spice_deck* Multi-rail cell scaling or exact-match is not fully supported in write spice deck yet, result may be inaccurate.

What Next

Do not trust the QoR that may be inaccurate. Or use non-scaling flow for now.

See Also

- write_spice_deck

SPICE-053

(Error) All loads of net '%s' are connected to black box.

Description

The reported net have all loads conneting to black box. The *write_spice_deck* cannot be performed with such net.

What Next

Please check the load connection and resolve unexpected black box issue if spice deck needs to be written out.

See Also

- write_spice_deck

Feedback

SPICE-054

(warning) : No clock is defined on pin '%s'.

Description

No clock is defined on the given pin.

What Next

Please check if the pins of option -from and -to are provided correctly.

See Also

- sim_analyze_clock_network

SPICE-055

(warning) Failed to compute driver model for cell '%s'.

Description

The driver model of the cell could not be computed, maybe all timing arcs are disabled. The default model for the cell is used.

What Next

Check disable timing settings on the cell.

See Also

- sim_validate_path
- sim_validate_stage
- write_spice_deck

SPICE-056

(error) The user measure failed as it couldn't find the pin/port with the name '%s' in the spice circuit.

Description

SPICE was unable to apply the user measure as it could not find a pin or port with the specified name in the spice circuit. One possible reason could be that the specified measure is on a pin or port is before the -from pin in the write_spice_deck command.

Feedback

What Next

Check that the measure has been applied on a relevent pin that is part of the spice circuit to be written out

See Also

- write_spice_deck

SPICE-057

(warning) : The master clock of the generated clock defined on pin '%s' does not exist.

Description

The master clock of the generated clock defined on the given pin doesn't exist.

What Next

Please check if the clocks in the design are defined correctly. Please check if the pins of option -from and -to are provided correctly.

See Also

- sim_analyze_clock_network

SPICE-058

(warning) The port '%s' is skipped in SPICE deck because there's waveform annotated on pin %s from HyperScale.

Description

In HyperScale block run, PrimeTime will honor the annotated waveform from HyperScale context on pins. If there's hyperscale annotated waveform on the interface pin which is connected to the starting port, the starting port will not be included in the SPICE deck. The SPICE simulation starts from the interface pin.

What Next

You may check the port and the pin attributes to confirm.

See Also

- sim_validate_path

Feedback

SPICE-059

(error) Waveform is annotated on pin '%s' in the path from HyperScale, SPICE simulation cannot match.

Description

In HyperScale block run, PrimeTime will honor the annotated waveform from HyperScale context on pins. If there's hyperscale annotated waveform on the pin in the path, SPICE simulation cannot match this behavior. The SPICE deck will be empty and simulation will not be done.

What Next

Please check the path.

See Also

- sim_validate_path

SPICE-060

(error) Duplicated pin names are not allowed in option -pins.

Description

The sensitization sequence are defined for the given pin list. The pin name should be unique in the pin list.

What Next

Please check the option -pins value.

SPICE-061

(warning) The cell or lib cell '%s' doesn't have pin '%s', the sensitization sequence cannot be set.

Description

There is mismatch between the pin list and the cell or lib cell, so the sensitization data will not be set.

What Next

Please check the cell or lib cell and pins.

Feedback

SPICE-062

(error) No valid cell or lib cell specified for the pin list.

Description

There is mismatch between given cell or lib cell and pin list. The sensitization sequence cannot be set.

What Next

Please check the option -cells, -lib_cells and -pins value.

SPICE-063

(error) The sensitization sequence data are missing.

Description

Both option -rise_vectors and -fall_vectors are not specified. No data to be set.

What Next

Need to set at least one option of -rise_vectors and -fall_vectors.

SPICE-064

(error) The sequence count in '%s' vectors does not match the pins count.

Description

The rise and fall vectors are a list of vectors. Each vector specifies 0 or 1 for the pins. The 0 and 1 count of each vector should be equal to the pins count.

What Next

Please check the vectors and specify consistent data.

SPICE-065

(warning) The clock period %gns is too small for pin '%s' to have complete rise and fall transitions.

Description

The transition times of the clock pin are too large compared with clock period. The clock pulse may not be able to reach logic one or logic zero state on this pin in simulation. This may cause simulation failure.

Feedback

For example: The rise and fall slews are 0.1ns with 30-70 trip points and clock period is 0.3ns. When the slew values are converted to 0-100 points, the clock period is not large enough to hold the rising and falling edges completely inside the period.

What Next

Increase the clock period or speed up the transition times of the pin.

See Also

- write_spice_deck
- sim_validate_path

SPICE-066

(information) Suggest to increase clock period larger than %gns.

Description

The transition times of clock pins along clock path are too large compared with clock period. The clock pulse may not be able to reach logic one or logic zero state on the pins in simulation.

The suggested clock period is based on the maximum transition time of pins along the clock path with certain margin.

What Next

Increase the clock period or speed up the transition times of the pins.

See Also

- write_spice_deck
- sim_validate_path

SPICE-067

(information) The adaptive clock period %gns is used in simulation with considering the transition times of pins along the clock path.

Description

The transition times of the pins along the clock path are too large compared with clock period. The clock pulse may not be able to reach logic one or logic zero state on the pins in simulation.

Feedback

In sep_init flow, the default clock period is replaced by the adaptive clock period which is calculated based on the maximum transition time of pins along the clock path with certain margin.

What Next

Please check clock period in SPICE simulation to make sure clock signal is propagated as expected.

See Also

- write_spice_deck
- sim_validate_path

SPICE-068

(information) Load capacitance for cell '%s' is being used in SPICE deck.

Description

Usually, cell is referenced to sub-circuit in SPICE simulation. In some situations, the load capacitance will be used to represent the cell in SPICE deck.

For example:

```
- when basic receiver modle is used in PrimeTime delay calculation.
- when user specifies to use pin load capacitance.
- when the cell is macro or blackbox.
```

What Next

Please check related settings.

See Also

- sim_validate_path

SPICE-119

(Error) Must specify output directory name when using -sample_size.

Description

The *write_spice_deck* command is used with *-sample_size* option but without the *-output* option. The *-output* option is mandatory when you use *-sample_size* option.

Feedback

What Next

Specify a directory name via -output option and re-issue the command.

See Also

- write_spice_deck

SPICE-122

(warning) The timing path has duplicate occurrences of cell '%s'.

Description

The timing path given to *write_spice_deck* has multiple references to the listed cell instance.

This typically occurs when a timing path launches from and is captured by the same sequential cell, sometimes called 'loopback' paths. In these cases, there is a conflict between trying to capture a preload value in the cell (acting as the path startpoint) and trying to capture the value (acting as the path endpoint). These paths cannot be simulated reliably.

What Next

The sensitization will be chosen for one instance of the cell. This sensitization may not be correct for all instances of the cell, or may not appear in the sensitization list at all.

See Also

- write_spice_deck

SPICE-123

(information) Detailed parasitics of the net '%s' are ignored due to '%s'.

Description

Detailed parasitics and lumped resistances of the net are ignored due to user set *set_load -wire_load* on the port connecting the net, *set_load* on the net or *set_resistance* on the net. SPICE results does not match with PT calculations.

What Next

Please avoid using lumped parasitics on the nets. These lumped parasitics does not have a equivalent representation at transistor level.

Feedback

See Also

- write_spice_deck
- set_load
- set_resistance

SPICE-124

(warning) Resistance set due to set_resistance on net '%s' is ignored due to '%s'.

Description

set_load and *set_resistance* cannot be used together on a net. Use only one of them. Also, if the net has multiple fanouts then resistance due to *set_resistance* will be ignored.

What Next

Use only *set_load* or *set_resistance* on the net, but not both. Also, please avoid using *set_resistance* on a net with multiple fanouts.

See Also

- write_spice_deck
- set_load
- set_resistance

SPICE-126

(warning) No spice equivalence for composite aggressor. Turn off the composite aggressor for %s analysis

Description

Coupled analysis is performed by turning on the composite aggressor feature. There is no spice equivalence for composite aggressor. Hence the spice deck does not represent how the analysis is performed in PTSI engine.

What Next

If you are doing correlation, please turn off the composite aggressor and run *update_timing*, *write_spice_deck* to regenerate the spice deck.

See Also

- write_spice_deck

Feedback

SPICE-127

(Warning) The cell '%s' could not be sensitized correctly because %s.

Description

The sensitization used for the above indicated cell does not match the worst case scenario it was characterized.

This is mainly due to missing information in the library except for noise correlation. *Write_spice_deck* tries to handle these situations by sensitizing the cell to behave closer to the condition it was characterized. Please verify this sensitization.

For noise correlation purpose, this message may indicate that worst case scenario is from default condition, where characterization scenario is missing. Please don't use the stage for correlation purpose.

What Next

Populate the library with the missing information and run write_spice_deck for correlation purposes, or skip the stage for noise correlation purpose.

See Also

- sim_validate_noise
- sim_validate_path
- sim_validate_stage
- write_spice_deck

SPICE-130

(information) The cell '%s' is duplicated due to conflict in sensitization.

Description

The sensitization involves the input pin(net) or the output pin(net) of the cell to switch in specific direction at specific time. And for some cells there is conflict due to multiple of these requirements. *write_spice_deck* handles it by duplicating the cell and sensitizing them according to the requirement.

Sensitization conflict can happen due to many reasons some of them are,

o Crosstalk stage shares a common cell between the victim and aggressors. The above cell needs to be rising for victim and falling for aggressor at specific time. This conflict is resolved by dupliating the common cell and sensitizating one as victim and another one as aggressor. This could also happen between two aggressors.

Feedback

o Timing false path or reconverging timing path, sometimes the timing path may not sensitizable or the reconverging paths is faster or conflicting with timing path of interest.

What Next

Generally this is conservative and safe.

See Also

- write_spice_deck
- si_enable_analysis

SPICE-200

(Warning) There is no library waveform set for the %s pin(%s). The default waveform (type : %s) is used.

Description

write_spice_deck needs the shape of the waveform that is used for the characterization of the timing library. Previously it was assumed to be ramp. Most of the current library characterization waveforms are type of smooth waveform called Synopsys pre-driver waveform. So to consider that the default waveform is changes to Synopsys pre-driver.

set_library_driver_waveform is the command used to set the library characterization wavefrom per library. This command allows to set multiple type of wavforms per libraray and library cell. The most appropriate approach is to find the waveform shape used for the library and apply it when the library is read to PrimeTime. However, to get the pre-2007.06 behaviour of ramp waveform as default waveform, apply "set_library_driver_waveform -type ramp" before update_timing.

What Next

Apply appropriate waveform shape using *set_library_driver_waveform*.

See Also

- write_spice_deck
- set_library_driver_waveform

SPICE-201

(error) Keeping waveform on timing points is disabled in the advanced waveform propagation mode.

Feedback

Description

The *timing_keep_waveform_on_points* variable is set to *false*. Therefore, there is no waveform information on the timing point to write to the SPICE deck for simulation. This causes inconsistent analysis between PrimeTime and SPICE.

What Next

Set the *timing_keep_waveform_on_points* variable to *true*, and generate the timing paths again. However, you do not need to update timing again.

See Also

- timing_keep_waveform_on_points

SPICE-202

(Warning) Internal pin %s is ignored. Please manually change the SPICE deck before simulation.

Description

Internal pin is not physical. The *write_spice_deck* command still writes out the spice deck without internal pin, and user needs to manually change the SPICE deck before simulation.

What Next

Manually change the SPICE deck before simulation. Or try to eliminate the possibility of having cells with internal pins in spice deck.

See Also

- write_spice_deck

SPICE-203

(warning) Clock period used for stimuli on pin '%s' is longer than 1000 ns.

Description

If there is a clock defined on the pin, SPICE simulation uses the clock period based on it.

If there is no clock defined on the pin, but there are clocks through it, SPICE simulation uses the longest clock period through the source pin.

If there is no clock defined on or through the pin, SPICE simulation uses the longest clock cycle in the design.

Feedback

Extremely long clock periods can cause long simulation times or failed simulations.

What Next

Find the clock with the extemely long clock period, and verify that the clock period is correct. If the long clock period is used in another part of the design, define a shorter clock period on the portion of the clock network of interest.

See Also

- sim_analyze_clock_network
- write_spice_deck

SPICE-204

(warning) The clock period or pulse width on pin '%s' is small and chopping the %s waveform.

Description

SPICE simulation uses chopped waveform on clock pin because the waveform of the clock pin is chopped due to small clock period or pulse width. The partial swing waveform may cause wrong simulation results or simulation failure.

What Next

Increase the clock period of the pin or adjust clock pulse width setting.

See Also

- sim_analyze_clock_network
- sim_validate_path
- sim_validate_stage
- write_spice_deck

SPICE-205

(warning) sim_enable_si_correlation is not set on net %s, alignment of aggressors may not be accurate.

Description

SPICE simulation for singal integrity correlation needs aggressor alignment information. If alignment information is not available correlation accuracy cannot be guaranteed.

Feedback

What Next

Set sim_enable_si_correlation on the net.

See Also

- sim_enable_si_correlation
- sim_validate_stage
- write_spice_deck

SPICE-206

(warning) All cell arcs %s pin %s are disabled in cell '%s'.

Description

Spice correlation related commands need cell arcs to do proper sensitization for cells on interested path or stage. *set_disable_timing may break the path or cause sensitization failure in SPICE.*

What Next

If simulation failure happens, check disable timing settings on the cell.

See Also

- sim_validate_path
- write_spice_deck

SPICE-207

(warning) TD for delay from %s to %s is too early compared to %s switch time. The spice deck measurement might be incorrect.

Description

For complicated sequential cell without sensization language, TD of sequential cell arc delay measurement may be off by one or more clock cycles.

What Next

If simulation measurement fails or miscorrelation happens, try *sim_validate_path -sep_init to decouple initialization Spice simulation from measurement Spice simulation.*

Feedback

See Also

- sim_validate_path

SPICE-208

(warning) pin %s does not have a valid sense for simulation.

Description

Commands related to SPICE correlation require a pin to have a valid sense (rise/fall/low/high) to do proper sensitization or measurement. An invalid sense can be caused by a SPICE-051 condition on the previous stage, by the cell not having any timing arc, or by disabled timing set with the *set_disable_timing command.*

What Next

If simulation failure happens, check for disabled timing settings, see if any cells need to be removed from the simulation, and check for SPICE-051 error conditions that need to be fixed.

See Also

- report_disable_timing
- set_disable_timing
- sim_validate_path
- write_spice_deck
- sim_analyze_clock_network
- SPICE-051

SPICE-209

(Warning) The cell '%s' uses fallback solution to sensitize.

Description

Common case can be case analysis or tied pin conflicting with library sensitization, or library misses binary state table and sensitization language. *Write_spice_deck* tries to handle these situations by sensitizing the cell to behave closer to the condition for which it was characterized. Please verify this sensitization.

What Next

If simulation failed or correlation looks bad, please verify sensitization. If the library cannot be updated with sensitization information, the path or stage needs to be skipped for correlation purpose.

See Also

- sim_validate_noise
- sim_validate_path
- sim_validate_stage
- write_spice_deck

SPICE-210

(warning) The cell '%s' is level-shifter.

Description

Level shifter cell is involved in simulation. Voltage definition can be complicated especially when scaling is enabled.

What Next

Generally this is conservative and safe.

See Also

- write_spice_deck
- sim_validate_noise
- sim_validate_path
- sim_validate_stage

SPICE-211

(error) Cannot find sub_circuit for cell '%s' (%s) for simulation.

Description

There is no sub_circuit for the lib_cell. This will cause simulation failure. Simulation will be skipped.

Feedback

What Next

Update *sim_setup_library* -sub_circuit setting to include needed sub_circuit.

See Also

- sim_setup_library
- sim_validate_noise
- sim_validate_path
- sim_validate_stage

SPICE-212

(warning) SPICE simulation result in the CCB output correlation report may not be correct when the load cell is a sequential cell.

Description

For the SPICE simulation result at the CCB output to be meaningful, the CCB output node needs to be initialized to the correct value. When the load cell is a sequential cell, a sensitization vector may be needed to do this initialization properly. But CCSN library syntax does not currently support sensitization vector. If the input CCB of the sequential cell is of combinational nature, the SPICE result will be correct, else, accuracy of the result cannot be guaranteed. In either case, PrimeTime result should be correct.

What Next

Identify a sensitization vector by looking at the subcircuit and manually modify the generated SPICE file to ensure that the CCB output node is initialized to the correct value and do the simulation. This result should match PrimeTime value.

See Also

- sim_validate_noise

SPICE-213

(warning) '%s' (%s) on-path missing sensitivity data, it may cause spice mis-correlation.

Description

Project Sicily requires library sensitivity data in side-file (defined by *define_sensitivity_lib_mapping*). Missing library sensitivity data will cause accuracy loss; and those paths shouldn't be used for correlation purpose v.s. golden SPICE model.

Feedback

What Next

Make sure *define_sensitivity_lib_mapping* is done properly on the library and all its scaling libraries. May sure there is no PSLIB-XXX warning indicating sensitivity for the focused lib_timing_arc/lib_pin/lib_cell is missing. If the missing data is not intented, please follow-up with library characterization team to fix the side-file library.

See Also

- SPICE-214
- PSLIB-001
- PSLIB-003
- PSLIB-004
- PSLIB-005
- PSLIB-006

SPICE-214

(warning) '%s' (%s) side-load missing sensitivity data, it may cause spice mis-correlation.

Description

Project Sicily requires library sensitivity data in side-file (defined by *define_sensitivity_lib_mapping*). Missing library sensitivity data will cause accuracy loss; and those paths shouldn't be used for correlation purpose v.s. golden SPICE model. The side-load cells usually has less impact v.s. on-path cells for path level correlation, but still could be source of inaccuracy.

What Next

Make sure *define_sensitivity_lib_mapping* is done properly on the library and all its scaling libraries. May sure there is no PSLIB-XXX warning indicating sensitivity for the focused lib_timing_arc/lib_pin/lib_cell is missing. If the missing data is not intented, please follow-up with library characterization team to fix the side-file library.

See Also

- SPICE-213
- PSLIB-001
- PSLIB-003
- PSLIB-004

Feedback

- PSLIB-005
- PSLIB-006

SR

SR-001

(error) The directory '%s' already exists.

Description

The specified directory to save the application session data already exist. If you want to overwrite the data in the directory, use -replace option.

What Next

Verify the directory name.

SR-002

(information) Cleaning and overwriting all data in the existing directory '%s'.

Description

The specified directory to save the PrimeTime session data already exists and -replace option is specified to overwrite the data in the directory.

Please use -replace with great caution, because it will try to remove all the existing data, including all files and sub-directories, already present in the target directory. If the target directory is logically the parent directory of current working directory or the directory from which the current session has been launched, the behavior is undefined.

What Next

Please confirm that it is safe for the application to delete the specified directory before issue the commond with -replace option.

SR-003

(error) %s.

Description

As indicated by the content of the message, save or restore operation has encountered some unexpected error condition and cannot proceed. The most common error is mis-aligned or missing data files in the image directory.

Feedback

What Next

Please confirm the reason(s) as indicated by the message, fix the specified problem and try again.

SR-004

(information) %s.

Description

As indicated by the message, some potentially risky operations have been performed during the save/restore.

What Next

Please confirm the indicated operation.

SR-005

(error) Mismatch of technology library. The library '%s' does not match between saved image and the one being currently loaded. Restore will be aborted.

Description

As indicated by the message, technology libraries are either recompiled or a different version of the library is being read.

What Next

Check your technology libraries (look in lib_map file) and redo restore_session.

SR-006

(error) Required library '%s' not found. Restore will be aborted.

Description

The given technology library was not found. This is required to perform restore.

What Next

Check your technology libraries (look in lib_map file) and redo restore_session.

SR-007

(error) The library file '%s' could not be restored.

Feedback

Description

The given technology library could not be restored. This is required to perform restore.

What Next

Check your technology libraries (look in lib_map file) and redo restore_session.

SR-008

(error) Cannot save design data to directory '%s'.

Description

As indicated by the message, the application is unable to save the design data in the specified directory. Usually, the target directory should not be the current directory, or a directory which is parent of the current working directory, or a directory which is a subdir of some unexisting directory.

What Next

Please confirm the indicated reason, fix the prolem and try again.

SR-009

(warning) Can not save variable '%s': unsupported %s

Description

As indicated by the message, the application is unable to save the specified variable. The type of data listed is not supported by the save_session command.

What Next

If the variable is needed in the restored session issue the needed commands to re-create the variable.

SR-010

(error) The session was not saved with the current version of application.

Description

The directory given to the restore_session command was not written by the current version of application. To see what version it was written with look at the file <directory>/README.

Feedback

What Next

Use the same version of PrimeTime/PrimePower to restore a session as was used to save the session.

SR-011

(error) The session directory is corrupted

Description

The directory given to the restore_session command is not complete. One or more files do not contain the expected data.

What Next

The session directory can not be used. Please re-run the original script.

SR-012

(error) Expected to find '%s' but found '%s' in the lib_map file.

Description

The directory given to the restore_session command has corrupted lib_map file. One or more technology library files are missing/changed in position.

What Next

Please re-run the restore_session after fixing the ascii lib_map file.

SR-013

(error) Cannot read the saved session files because they were not generated by the same product.

Description

The directory given to the restore_session command was not generated by the same product. To see what product generated this session, please refer to file <directory>/README.

What Next

Use the same version and the same product to restore a session as was used to save the session.

Feedback

SR-014

(information) The library location '%s' is changed to '%s' in the lib_map file.

Description

This is an information message that the lib_map file was edited to change the location of the technology libraries.

What Next

No action is required, this is just information.

SR-015

(error) Cannot restore the session saved with version '%s', which is different from the current version '%s'.

Description

The directory given to the restore_session command was not written by the current version of application. To see what version it was written with look at the file <directory>/README.

What Next

Use the same version of PrimeTime/PrimePower to restore a session as was used to save the session.

SR-016

(error) Clean up partially restored design data...

Description

As indicated by the message, some potentially risky operations have been performed during the save/restore and resulted in the restore failing.

What Next

Please confirm the indicated operation.

SR-017

(information) Could not remove previously added hosts as they are either still on line or are currently being launched.

Feedback

Description

As indicated by the message, prevously added hosts could not be removed. Therefore, the number of hosts added for the restored session will exceed the number of hosts required.

What Next

No action is required.

SR-018

(warning) The -only_used_libraries option is not supported in distributed multicore analysis and will be ignored.

Description

As indicated by the message, the -only_used_libraries option is not supported in distributed multicore analysis. This option will be ignored when saving the session. As a result, all libraries loaded will be required when the session is restored.

What Next

No action is required.

See Also

- save_session

SR-019

(warning) The number of online hosts is less than the number required for the session being restored. Sourcing the multicore_compute_resources.tcl file.

Description

If the number of currently online hosts is less than the number used by the saved session then the multicore_compute_resources.tcl file is sourced in order to bring the correct number of hosts online for the restored session. Additionally, any hosts currently online will be shutdown.

What Next

No action is required.

See Also

- restore_session

Feedback

SR-020

(warning) Cannot open file '%s' for writing - setting pt_tmp_dir to default value.

Description

The pt_tmp_dir could not be set to the directory used in the saved session. As a result, the pt_tmp_dir will be set to the default value.

To determine the current value of the pt_tmp_dir, type printvar pt_tmp_dir or echo $pt_tmp_dir.

What Next

No action is required. However, you may want to verify the directory name and permissions for the pt_tmp_dir.

SR-021

(information) The pt_tmp_dir has not changed from '%s' to '%s'.

Description

If the pt_tmp_dir has been set to a specific directory before the *restore_session command is issued then this value overrides the value saved by the save_session command. This essentially results in the user-specified pt_tmp_dir setting to be of higher precedence than the saved session's value.*

What Next

No action is required.

SR-022

(error) Path collection has not been restored because a design is instantiated.

Description

Loading a session containing only timing paths using *restore_session is only possible if no design is instantiated in PrimeTime shell.*

What Next

Remove the design using *remove_design command prior to restoring a path collection session.*

Feedback

SR-023

(error) Path collection cannot be restored because its name '%s' is already in use.

Description

Loading a session containing only timing paths using *restore_session creates a collection of timing paths. If the collection name is not unique to the PrimeTime session, restoring the collection is not possible.*

What Next

Specify a unique name for the path collection by using *-name option of restore_session.*

SR-024

(error) Option *-name can only be used when restoring a path session.*

Description

Loading a session containing only timing paths using *restore_session creates a collection of timing paths. Option -name allows specifying a unique collection name. The option is only valied when restoring a path session.*

SR-025

(information) %s Interactive Multi-Scenario Analysis.

Description

Loading a saved session containing only timing paths using *restore_session puts PrimeTime shell in the Interactive Multi-Scenario Analysis Mode. In this mode, you may load multiple timing path sessions to compare and manipulate timing paths saved by different PrimeTime sessions. Only a limited number of PrimeTime commands is available in this mode.*

What Next

No action is required. However, if you want to exit IMSA mode, use *remove_design command.*

SR-026

(error) Only path sessions can be restored in Interactive Multi-Scenario Analysis.

Feedback

Description

Loading a saved session containing only timing paths using *restore_session puts PrimeTime shell in the Interactive Multi-Scenario Analysis Mode. In this mode, you may load multiple timing path sessions to compare and manipulate timing paths saved by different PrimeTime sessions. Restoring saved sessions that are not timing path sessions is disabled in IMSA mode.*

What Next

If you want to exit IMSA mode, use *remove_design command.*

SR-027

(error) The specified save_session directory '%s' is currently in use by another process.

Description

Another process is currently either saving its session to the specified directory or restoring a session from that directory which is preventing the current process from overwriting the directory. You can see the process id of the job using the directory by looking at the .lock_save_$pid or .lock_restore_$pid file in the save_session directory.

What Next

Either wait for the other process to finish saving or restoring its session or specify another save_session directory.

SR-028

(error) The specified save_session directory '%s' is currently in use by another process.

Description

Another process is currently saving data to the specified directory and has not completed its save_session action. You can see the process id of the job writing to the directory by looking at the .lock_save_$pid file in the save_session directory.

What Next

Please wait for the other process to finish saving its session before issuing the restore_session command again.

SR-029

(error) restore_session requires at least %ld MB of free space in the pt_tmp_dir '%s' but available space is only %ld MB.

Feedback

Description

The *pt_tmp_dir* is used to store data when high capacity mode is enabled. For *restore_session* to complete successfully enough space is required in the *pt_tmp_dir* to store this data. If enough space is not available then *restore_session* will fail.

What Next

Please free up some space in the *pt_tmp_dir* or specifiy another *pt_tmp_dir* before issuing the *restore_session* command again.

See Also

- set_program_options
- pt_tmp_dir

SR-030

(information) Clock %s restored as clock %s.

Description

During loading of a saved timing path collection session using *restore_session, it was detected that a clock which is being restored has the same name as a clock already in memory. The restored clock was renamed.*

What Next

No action is required.

SR-031

(error) You can use the -libs_dir option only if the current session was restored from a directory including libraries.

Description

After *restore_session* the session libraries are loaded either from the saved image or from an external location. If restored from the saved image, you can use the *save_session* command with the *-libs_dir* option to create an image that does not contain its own libraries but refers to an external directory. However, if the restored session libraries do not come from the saved image, you cannot use the *-libs_dir* option because libraries are already set as coming from an external path, in which case this error is issued.

What Next

Run the command without the *-libs_dir* option.

Feedback

SR-033

(error) Cannot save to %s: it contains the current session libraries in use.

Description

The current session has been restored from an image that included the libraries. It is not permitted to overwrite this directory as it would compromise the current session stability.

What Next

Run the command with a different save directory.

SR-034

(error) There is more than one loaded library named %s.

Description

The save_session -include libraries or save_session -libs_dir commands require that there are no two libraries with the same filename.

What Next

Remove the unused repeated library and run the command again.

SR-035

(error) Failed to create %s when saving.

Description

The save_session command stopped because a file copy or directory create failed.

What Next

Verify write permissions and that there is enough disk space and that no other process is operating in the save session directory.

SR-036

(information) Saved session uses shared data located in %s

Description

Some data in the current saved image can potentially be shared across multiple scenario saved images. This data is stored in a common data location. This feature can be disabled using the -disable_common_data_sharing option to save_session.

Feedback

What Next

No action is required.

See Also

- save_session

SR-037

(error) The session directory is corrupted due to missing data.

Description

The session directory has missing data files. Typically, disk related issues during save_session could result in this corruption.

What Next

Ensure that the disk on which the session is saved is not full and has appropriate write permissions.

See Also

- save_session

SR-038

(error) Cannot overwrite a session with ICC2 signature.

Description

The session directory %s stores a session with ICC2 signature.

What Next

To overwrite the session, run command with *-force* option.

See Also

- save_session

SR-039

(warning) Can not save variable '%s': It could potentially exceed memory limit

Feedback

Description

As indicated by the message, the application is unable to save the specified variable due to possibility of exceeding memory limit.

What Next

If the variable is needed in the restored session issue the needed commands to re-create the variable.

SR-040

(error) The -only_timing_paths option is not supported in %s.

Description

As indicated by the message, the -only_timing_paths option is not supported in the given analysis mode of PrimeTime. The command will exit without saving a timing path collection session.

What Next

Use a compatible analysis mode for saving a timing path collection session.

See Also

- save_session

SR-041

(Error) Cannot change this variable in IMSA mode.

Description

When the Interactive Multi Scenario Analysis (IMSA) mode is enabled, eco_enable_physical_gui cannot be changed.

What Next

Exit IMSA mode using *remove_design -all*

SR-042

(error) Cannot incrementally add path collections to directory '%s'.

Description

The directory does not exist, could not be expanded or the session files do not exist.

Feedback

What Next

Ensure the directory has been correctly specified and that the session files are present and have previously been saved with a call to *save_session -only_timing_paths ...*.

See Also

- save_session

SR-043

(warning) Cannot restore user-defined attribute '%s' of type %s. The attribute was previously defined to be of type %s.

Description

The type of the user attribute has previously been defined and cannot be redefined. Incompatible user attribute values will be ignored.

What Next

Ensure that the session you are restoring from does not have incompatible user attribute definitions with the session you are restoring into.

See Also

- restore_session
- restore_timing_paths

SR-044

(information) At least %s of free disk space in pt_tmp_dir will be required to restore this session. %s

Description

The *pt_tmp_dir* is used to store data when high capacity mode is enabled. In order to restore this data, there must be sufficient free disk space available.

What Next

Make sure there is sufficient free disk space in the *pt_tmp_dir* before restoring this session.

Feedback

See Also

- set_program_options
- pt_tmp_dir

SR-046

(error) Cannot restore the session. At least %.2f %s free disk space is required in pt_tmp_dir; only %.2f %s is available.

Description

The *pt_tmp_dir* is used to store data when high capacity mode is enabled. In order to restore this data, there must be sufficient free disk space available.

What Next

Make sure there is sufficient free disk space in the *pt_tmp_dir* before restoring this session.

See Also

- set_program_options
- pt_tmp_dir

SR-047

(error) Cannot restore the version compatible session saved with version '%s' in '%s'. Please save with latest SP version and try to restore.

Description

The directory given to the restore_session command was saved with older version which is not supported for restore. Please try saving with latest SP version and restore. To see what version it was written with look at the file <directory>/README.

What Next

Use the latest version of PrimeTime/PrimePower to save a session and restore.

SR-048

(information) Restoring the version compatible session saved with version '%s'.

Feedback

Description

To see what version it was written then look at the file <directory>/README.

What Next

Use the latest version of PrimeTime to save a session and restore.

SR-049

(information) ICC-II reference library information in the session is not saved, instead corresponding directory path is saved which needs to be accessible during restore_session.

Description

In version compatible mode when session generated using -include physical_data, if the eco physical information is supplied in the form of IC Compiler II reference library, then it is not captured in the session, instead only corresponding path is saved, hence, the path needs to be accessible during restore_session and when this information is read using eco flow either with check_eco or fix_eco_xx, typically IC Compiler II reference library library directory path is specifyed, using command "set_eco_option -physical_icc2_lib"

What Next

During restore_session, when eco physical information is read either using check_eco or fix_eco_xx, ICC-II reference library path must be accessible. Check <saved_session_dir>/eco_config for paths included in the session.

See Also

- save_session
- set_eco_options
- check_eco

SR-051

(warning) Restoring DEF file specification '%s' even though the file can not be found.

Description

This warning is issued when *restore_session* command restores a Design Exchange Format (DEF) file specification from saved session, but the file can not be found. The file must exist for physically aware ECO commands to proceed.

Feedback

What Next

Please use *report_eco_options* command to review physical data specification, and re-define them using *reset_eco_options* and *set_eco_options* commands.

See Also

- report_eco_options
- reset_eco_options
- set_eco_options
- check_eco
- restore_session

STAT

STAT-001

(error) Invalid attribute %s.

Description

An element in the attribute name list does not match one of the valid names.

What Next

Correct the command so that all attribute names are valid. See the command man page for a list of the valid commands.

STAT-002

(error) The "all" attribute was found but was not alone.

Description

If the "all" attribute is used it must be the only attribute name in the list.

What Next

Remove all attribute names except the "all" name.

STAT-003

(error) Size of value list does not match name list.

Feedback

Description

If the *-values* option is used then the number of elements in the list must match the number of elements in the name list.

What Next

Fix the values or names list so that the number of elements match.

STAT-004

(error) Unrecognized variation names are given.

Description

Reference variation name list is given with the *reference_value* option of the *set_variation_library* command. Any other settings cannot provide names outside of this list.

What Next

Remove extraneous names from the variation name list.

STAT-005

(error) Found reference value and value list options.

Description

The reference value option precludes the use of the value list option. They cannot be used together.

What Next

Remove either the reference value or the value list from the command.

STAT-006

(error) More than one non-reference value is given.

Description

Reference variation value list is given with the *reference_value* option of the *set_variation_library* command. Any other settings can provide only one non-reference value.

What Next

Ensure only one non-reference value.

Feedback

STAT-007

(warning) Library %s, variation %s, value %f already exists.

Description

The library, variation, and value already exists as a triplet. Only the first setting is used; subsequent settings are ignored.

What Next

Only set the library, variation, and value once.

STAT-008

(error) More than one distribution in distribution list.

Description

The *-distribution* option must reference exactly one distribution.

What Next

Check that the variable used with the *-distribution* argument references exactly one distribution.

STAT-009

(error) Missing a distribution in the distribution list.

Description

The *-distribution* option must reference exactly one distribution.

What Next

Check that the variable used with the *-distribution* argument references a distribution.

STAT-010

(warning) Cannot find variation.

Description

PrimeTime could not find the specified variable to delete it.

Feedback

What Next

Ensure that the variation has been created. Ensure that the variable has not already been deleted.

STAT-011

(error) Variation library %s does not exist.

Description

The given library does not exist in the search path.

What Next

Ensure that the search path exists, and that the library exists in the search path.

STAT-012

(error) Cell %s may not have a timing arc or may not match across libraries.

Description

A cell in the library may not have a timing arc, or does not match across libraries. There could be cells in one library not in another, a different number of pins between cells of the same name, or pins having different directions.

What Next

If the cell has no timing arc, check that it is not used. Check that the libraries all have the same cells, and that their pins match in name, number, and direction.

STAT-013

(error) %s quantile with value %lf is out of range.

Description

A quantile value falls outside the open interval zero to one. It must be strictly greater than zero and strictly smaller than one.

What Next

Change the quantile to be a floating point number between zero and one.

STAT-014

(error) Cannot turn on variation analysis when power analysis is on.

Feedback

Description

Power analysis and variation analysis are currently mutually exclusive. Variation analysis cannot be enabled while power analysis is on.

What Next

Turn off power analysis first then turn on variation analysis.

STAT-015

(error) Size of variation_name_list does not match size of variation_value_list.

Description

When the *-reference_value* option is used, the number of names in the *variation_name_list* must match the number of values in the *variation_value_list*.

What Next

Either remove the *-reference_value* option from the command, or make the number of names equal the number of values.

STAT-016

(error) The %s distribution cannot be specified with %d values.

Description

The type of the distribution determines the number of elements needed in the value list. See the *create_distribution* man page for a description of the types, the number of values they need, and what the arguments mean.

What Next

Make sure that the type on the command and the number of values match.

STAT-017

(error) The first and last function value of a pwl distribution must be 0.0.

Description

The first and last function value in the value list of a pwl distribution must always be 0.0.

What Next

Change the distribution type to something other than pwl, or change the second value and last value in the value list to 0.0.

Feedback

STAT-018

(error) The -reference_value option is required on first call.

Description

The first time set_variation_library command is called it must have the *-reference_value* option.

What Next

Set a reference value the first time that set_variation_library is called. See the *set_variation_library* command for more information.

STAT-019

(error) Variation library %s does not exist.

Description

The given library does not exist in the search path.

What Next

Ensure that the search path exists, and that the library exists in the search path.

STAT-020

(error) Cannot have a variation called nom.

Description

The word 'nom' is a reserved variation name internal to PrimeTime.

What Next

Select a different name for the variation.

STAT-021

(warning) %s %s is not supported yet.

Description

This feature is not supported in the current version of PrimeTime.

What Next

Contact your PrimeTime representative if this feature is absolutely needed now.

Feedback

STAT-022

(error) Library data for variation %s is needed in advance.

Description

PrimeTime requires that library data for each variation be entered before these variations are defined using the *set_variation* command.

What Next

Ensure that in your scripts, any *set_variation_library* commands occur before any *set_variation* commands.

STAT-023

(error) Parameter names %s and %s do not match.

Description

The parameter name associated with a variation must match the name of the corresponding variation parameter. PrimeTime has found a mismatch during the execution of the command and produces this error.

What Next

Ensure that the parameter name provided with the command matches the correct variation parmater.

STAT-024

(error) Value %s is unknown to class %s.

Description

The value is expected to be a valid value or a member of the class. This error shows that this expectation has failed.

What Next

Check the allowed values for the class and ensure that the value belongs to this class.

STAT-025

(error) Cannot remove the variation from the arc.

Feedback

Description

PrimeTime cannot remove a variation from an arc that does not have that variation.

What Next

Provide those arcs that do have the given variation.

STAT-026

(error) The variation %s of the %s parameter is assigned to both the design and an arc.

Description

The same variation must not be used for both the design and any timing arcs.

What Next

Uniquify the varition names or remove the shared variation from the design or the arcs.

STAT-027

(error) The number of variations to sub in the collection is %d.

Description

One can sub two and only two variations. The collection must contain two variations. any timing arcs.

What Next

Make the collection contain two variations and run again.

STAT-028

(error) A library is given for a second time.

Description

Variation libraries can only be given once.

What Next

Remove from the script the redundant library and rerun.

STAT-029

(error) The lower bound %lf for the distribution is larger than the upper bound %lf.

Feedback

Description

A distribution lower bound must be smaller than its upper bound.

What Next

Fix the bounds and rerun.

STAT-030

(error) The area under the curve of this pwl distribution is %lf and not 1.0.

Description

The area under the curve of a probability density function must be 1.0.

What Next

Choose numbers such that the area under the curve of the pdf is 1.0, and rerun.

STAT-031

(warning) The variation %s of the %s parameter has a non-zero mean of %f.

Description

The variations are expected to have zero mean.

What Next

Adjust the variation parameters to ensure zero mean.

STAT-032

(error) For a pwl probability distribution, the first and last weight values must be 0.0.

Description

Weight values at the ends of the distribution support must be 0.0.

What Next

Fix the weight value(s) and run again.

STAT-033

(error) For a pwl probability distribution, the x-values must be increasing. Value %lf was smaller than its predecessor.

Feedback

Description

x-values of a pwl distribution must be strictly increasing.

What Next

Fix the x value(s) and run again.

STAT-034

(error) For a pwl probability distribution, the weight values must be non-negative. Value %lf was found.

Description

Weight values of a pwl distribution must be nonnegative.

What Next

Fix the w value(s) and run again.

STAT-035

(error) The lower or upper bound %lf must be smaller or larger than %lf.

Description

The lower or upper bound must be correct relative to the lowest or largest x-value.

What Next

Fix the bounds or fix the x-values, and run again.

STAT-036

(error) This %s distribution must have its %s bound %s than %lf.

Description

The bounds or the parameters of this distribution are incorrect.

What Next

Fix the bounds or the parameters of this distribution.

STAT-037

(error) The distribution attribute %s has parameter value %d.

Feedback

Description

The parameter value for the distribution attribute of cdf_values (or pdf_values) must be two or larger.

What Next

Increase the number of data points or use the distribution attribute cdf (or pdf).

STAT-038

(error) Invalid variable name %s.

Description

An element in the variable name list does not match one of the existing names. Each variable name in the variable name list must match one of the variable names defined with the *-reference_point* option.

What Next

Either correct the command so that the variable name matches one of the reference point variable names, or correct the reference point definition to have the needed variable name.

STAT-039

(warning) Library %s contains a special cell %s with no timing arc. Variation-aware PrimeTime may not be able to handle this cell.

Description

A special cell in the library does not have timing arcs. If a design contains such a cell, Variation-aware PrimeTime may not be able to handle it.

What Next

Check that these cells are not in the design.

STAT-040

(error) %s %s when variation-aware analysis is not enabled.

Description

Variable variation_enable_analysis must be TRUE to enable this feature.

Feedback

What Next

Set variable variation_enable_analysis to TRUE.

STAT-041

(error) For command %s, %s must be %s than %g.

Description

For certain commands, there are restrictions on the range of possible option values.

What Next

Make sure that the values of the option are within the allowed range.

STAT-042

(error) Library specified in define_scaling_lib_group cannot be specified as a variation library.

Description

Any library specified as a scaling library using the command define_scaling_lib_group cannot be specified as a variation library.

What Next

If you want to specify the library as a variation library, re-define the define_scaling_lib_group and re-link the design.

STAT-043

(error) For the %s distribution, the %s parameter must be %s than %lf.

Description

The value entered for this parameter is incorrect.

What Next

Fix the value of the parameter.

STAT-044

(error) For the %s distribution, the %s must be %s than %lf.

Feedback

Description

The bound entered is incorrect.

What Next

Fix the value or the bound of the distribution parameters.

STAT-045

(error) Command %s cannot be executed before linking the design.

Description

The design needs to be linked before using this command.

What Next

Link the design and issue the command again.

STAT-046

(error) The support of this %s distribution has weight %lf. We require that the support of a truncated distribution be at least %lf.

Description

Either the lower and upper bounds are too close, the lower bound is too large, or the upper bound is too small.

What Next

Fix the bound(s) so the truncated distribution has heavier support or try another distribution.

STAT-047

(error) This %s probability distribution has a %s equal to %lf. This is invalid for this probability distribution.

Description

An invalid value(s) was entered for the relevant parameter(s) of this distribution.

What Next

Fix the value of this parameter(s) for this distribution.

Feedback

STAT-048

(error) Path-based analysis works with variation-aware analysis only when design is in on_chip_variation mode.

Description

Variation-aware analysis requires the *on_chip_variation* analysis type. Path-based analysis recomputes the paths only when analysis type is set to on_chip_variation. When analysis_type is set to *bc_wc* or *single*, no recomputed path will be returned.

What Next

Use *set_operating_conditions* to set the design in *on_chip_variation* for variation-aware analysis; or disable variation-aware analysis when the design is in *bc_wc* or *single* analysis type.

See Also

- set_operating_conditions

STAT-050

(Error) Creation of variation library group failed %s.

Description

While creating a variation library, data for the same arcs and pins across the libraries for a variation library group are associated with each other; if this association fails, the variation library group cannot be completed and the STAT-050 error message is issued.

What Next

Be sure that the set of arcs and pins is present across the members of the variation library groups and the linked libraries. This message is issued when some of the arcs or cells are missing across the members of the scaling library groups.

Note that it removes all the previous variation libraries that were set. So after making sure that the set of arcs and pins are present within all the libraries, set all the variation libraries again.

STAT-051

(warning) Cannot report library sensitivity. '%s'

Feedback

Description

Sensitivity values cannot be computed due to different formats of delay and slew tables in variation libraries.

What Next

Make sure all variation libraries have the same dimensions, sizes and breakpoints of delay and slew tables.

STAT-052

(Warning) Some of the timing arcs cannot be uniquely determined across the variation library group, it is assumed that the timing arcs are defined in the same order across all the libraries.

Description

While creating a variation library, data for the same arcs and pins across libraries are associated with each other; if the timing arcs cannot be associated across the scaling libraries because the timing arcs cannot be identified uniquely within a library, the STAT-052 warning message is issued. Since the timing arcs cannot be uniquely identified, the arcs are assumed to be in the same order across the libraries in a library group.

Note that this is only an informational warning, the association of pins and arcs for the variation library group will still be created.

What Next

Be sure that the set of arcs that cannot be uniquely identified are present in the same order across the members of the scaling library groups.

STAT-053

(error) For command %s, the list for option %s contains an invalid number (%d) of elements.

Description

The number of elements in the list is invalid.

What Next

Correct and rerun.

STAT-054

(error) For command %s, the list for option %s must contain %d or more elements.

Feedback

Description

The number of elements in the list is invalid.

What Next

Correct and rerun.

STAT-055

(error) For command set_variation_correlation %s, the number %d of variations in the list does not match the expected number %d derived from the size of the list of correlation values of correlation %s.

Description

For a set_variation_correlation command associated with a correlation that is cross, the number of variations listed must equal the number of variations derived from the size of the list of correlation values (listed in the corresponding create_correlation command).

What Next

Correct and rerun.

STAT-056

(error) For command set_variation_correlation %s, the corresponding covariance matrix is not positive definite.

Description

For a set_variation_correlation command associated with a correlation that is cross, the covariance matrix formed by the correlation values listed in the corresponding create_variation command along with the variances of the variations, must be positive definite. Either there is a linear relationship between the variations, in which case one should eliminate the redundant variation(s), or the correlation values were not estimated precisely enough.

What Next

Correct the correlation numbers or the standard deviations of the distributions.

STAT-057

(warning) The distribution of variation %s is %s. Variations with %s are assumed to have a %s normal distribution. This implies that the marginal distributions must be normal.

Feedback

Description

This type of correlation is supported under the condition that the variations have a multidimensional normal distribution.

What Next

Check whether the univariate distribution is modeled well enough by a normal. If not, the results will not necessarily be mathematically correct.

STAT-058

(error) Variation %s has cross-correlation with another set of variations (associated with set_variation_correlation %s).

Description

A variation can have cross-correlation with one set of variations. Otherwise, it should have a cross-correlation with the union of the sets.

What Next

If there is no error, one should take a larger set of cross-correlated variations, estimate the correlations for this larger set, and set a new create_correlation and set_variation_correlation commands.

STAT-059

(error) %s cannot be set with option %s.

Description

Cross-correlations must be set on a specific set of variations. Further, the number of variations in the set must be consistent with with the number of correlation values entered in the corresponding create_correlation statement.

What Next

Enter the list of variations this command applies to.

STAT-060

(error) Value %f of option %s of command create_correlation is invalid.

Description

The value for this option is invalid or not yet supported.

Feedback

What Next

Fix the value for this option and rerun.

STAT-061

(warning) Command %s with option -name %s has been reissued with possibly a different value(s). The current command will overwrite the previous one.

Description

The command has been reissued with possibly a different value(s).

What Next

Make sure this was intended.

STAT-062

(error) For command %s, one and only one of the two options %s or %s must be given.

Description

Exactly one of the two options is required.

What Next

Correct and rerun.

STAT-063

(error) For option %s of command %s, the collection of %s's is of size %d. It must be of size 1.

Description

The collection for the option must be exactly of size 1.

What Next

Correct and rerun.

STAT-064

(error) Cannot find a correlation with name '%s'.

Feedback

Description

Each correlation object is identified with a unique string name. No correlation object can be found with the given name.

What Next

Make sure the correlation with the given name exists.

STAT-065

(error) %s quantile undefined.

Description

High and low quantiles must be defined together.

What Next

Define both high and low quantiles with proper values.

STAT-066

(error) Parameter name required to set a variation on timing objects

Description

The create_variation command has a list of timing objects but is missing the parameter name. It requires a parameter name when setting the variation on timing objects.

What Next

Re-issue the command and add a parameter name.

STAT-067

(error) More than one design found in the timing object list

Description

The create_variation command only allows one design in the timing object list.

What Next

Re-issue the command with only one design specified.

STAT-068

(error) If a design is specified it must be the current design

Feedback

Description

The create_variation command requires that if a design is specified as a timing object then it must be the current design. If you leave out the timing object list and specify a parameter_name, create_variation defaults to using the current design.

What Next

Re-issue the command with either the current design or an empty timing object list.

STAT-069

(error) The timing object list must be of a single object type

Description

The create_variation command requires that all objects in the timing object list be the same time. The timing object list can be either timing arcs or a design.

What Next

To put a variation on both timing arcs and a design, issue the command twice: once with timing arcs and once with the design.

STAT-070

(error) The name %s for command %s conflicts with another %s name

Description

This error message is generated if the command has already created an object with the same name.

What Next

Re-issue the command with a different name for the -name option.

STAT-071

(error) Command %s cannot be executed with option %s before linking the design.

Description

The design needs to be linked before using this command with the given option.

What Next

Link the design and issue the command again.

Feedback

STAT-072

(error) Command %s requires at least two variations in the object_list

Description

The command requires two or more variations in its object list in order to perform the operation. The object list is a collection of variations, and in this case there was less than two elements in the list.

What Next

Include more variations in the collection. Either use *add_to_collection* to insert variations from other collections, or use pattern in *get_variations* to create a collection with more than one variation in it.

STAT-073

(error) Missing *-all* and *variation_list* arguments

Description

The command requires either the *-all* or the *variation_list* options on the command line, and it could not find either.

What Next

Re-issue the command with either the *-all* or the *variation_list* option.

STAT-074

(error) Both *-all* and *varaition_list* specified

Description

The command requires one of either *-all* or *variation_list*, but it found both.

What Next

Re-issue the command with only one of *-all* or *variation_list*.

STAT-075

(error) For spatial correlation %s, the list of pairs of values (distance, correlation) of option -physical_distance must contain a positive even number of elements. It is %d.

Feedback

Description

Elements must be missing from the list.

What Next

Correct and rerun.

STAT-076

(error) For spatial correlation %s, a %s has value %f. It is %s, and, so, is illegal.

Description

Elements of the list are out-of-order or are incorrect.

What Next

Correct and rerun.

STAT-077

(error) For spatial correlation, PrimeTime could not obtain a bounding box from the parasitics SBPF file(s). The physical locations of pins may not be available. Spatial correlation will be ignored. Full autocorrelation (i.e., correlation with constant 1.0) for the relevant variation(s) will be assumed.

Description

Physical location of pins must be available in the SBPF file(s).

What Next

Verify that the SBPF file(s) contain(s) the pins physical locations.

STAT-080

(error) %s cannot be used when variation-aware analysis in the default mode is disabled.

Description

Variable variation_enable_analysis must be TRUE in the default mode to use this option.

What Next

Ensure that the variation_enable_analysis variable is set to TRUE and that the variation_analysis_mode variable is set to default.

Feedback

STAT-081

(warning) The %s physical distance %f is %s compared to the %s %f. Please verify that the units of distance of the correlation function are in nanometers.

Description

The warning is simply a recommendation to the user to double-check the units of distance (which must be in nanometers). PrimeTime checks whether the physical distances are very small or very large relative to the size of the bounding box (that is read in from the spef file).

What Next

Verify that the values of the physical distance of this correlation were those intended. If they are indeed correct, please ignore this warning.

STAT-082

(warning) PrimeTime could not handle the spatial correlation %s. It will be assumed that the variations are not spatially dependent, and have a constant correlation with value 1.

Description

If the correlation function does not decay fast enough or varies wildly (i.e., it is not monotone at all), PrimeTime may have a problem handling this spatial correlation. Such correlation functions are atypical.

What Next

Try a correlation function that decays to zero faster (with distance) or is more monotone.

STAT-083

(error) set_variation is applied here on a non-variation.

Description

The command set_variation must be applied on a genuine variation, i.e., on a construct declared via create_variation.

What Next

Fix typo(s) if any, or precede the command by a create_variation if it is missing.

STAT-085

(error) %s is missing from command set_variation_library.

Feedback

Description

The command set_variation_library is missing a list of variations, a list of values, or a library name.

What Next

See the *set_variation_library* command for more information.

STAT-086

(error) For command %s, options %s and %s are invalid together.

Description

The command does not take in these two options together.

What Next

Correct and rerun. For more information, see the user guide.

STAT-087

(error) For command set_variation_library with multi-libraries linked, library %s is out of order, or contains an incorrect variation name or value.

Description

When linking multi-libraries, the sets of set_variation_library commands must be in step-lock.

What Next

For more information, see the user guide.

STAT-088

(error) For command set_variation_library with multi-libraries linked, more than one library were linked.

Description

When linking multi-libraries in this context, there should be a single library linked.

What Next

For more information, see the user guide.

Feedback

STAT-089

(error) For command %s, options %s and %s are incompatible without option %s.

Description

The command has either an incompatible option or is missing an option.

What Next

See the man page for more information about this command.

STAT-090

(error) The command variation_correlation cannot process the %s object.

Description

The command applies generally to variations queried from path-based analysis, such as path variation_arrival and variation_slack.

What Next

Apply this command to a variation queried via get_attribute on a timing path or timing point obtained from a path-based analysis.

STAT-091

(error) %s variation report is not available %s.

Description

The cell and net variation report is only available when variation-aware analysis is turned on in the default mode.

What Next

Set variation_enable_analysis to TRUE and variation_analysis_mode to default.

STAT-092

(error) For command set_variation_correlation %s with discrete parameter distributions, all the weights of each discrete parameter distribution must be identical.

Description

For a set_variation_correlation command with discrete parameter distributions, associated with a correlation that is cross, all the weights of each discrete parameter distribution

Feedback

should be identical. For a k-valued discrete parameter, the corresponding weights (k in number) should each be equal to 1/k.

What Next

Correct and rerun.

STAT-093

(error) For command set_variation_correlation %s with discrete parameter distributions, all the weights of each discrete parameter distribution must be identical.

Description

For a set_variation_correlation command with discrete parameter distributions, associated with a correlation that is cross, all the weights of each discrete parameter distribution should be identical. For a k-valued discrete parameter, the corresponding weights (k in number) should each be equal to 1/k.

What Next

Correct and rerun.

STAT-094

(error) For command set_variation_correlation %s with discrete parameter distributions, all the weights of each discrete parameter distribution must be identical.

Description

For a set_variation_correlation command with discrete parameter distributions, associated with a correlation that is cross, all the weights of each discrete parameter distribution should be identical. For a k-valued discrete parameter, the corresponding weights (k in number) should each be equal to 1/k.

What Next

Correct and rerun.

STAT-095

(error) A user-defined variation %s.

Description

A user-defined variation requires a name and cannot have a parameter name.

Feedback

What Next

Create a user-defined variation with a unique name, without a parameter name.

STAT-096

(error) Cross-correlation '%s' specified between '%s' with spatial auto correlation and '%s' with constant auto correlation. Ignoring specified cross-correlation.

Description

Cross-correlation can only be specified between variables with identical auto correlation.

What Next

Investigate and see if you can make the cross-correlated variables have identical auto-correlation

---

STAT-097

(error) Cross-correlation '%s' specified between spatial variables '%s' and '%s' with different correlograms. Ignoring specified cross-correlation.

Description

Cross-correlation can only be specified between spatial variables with identical correlograms.

What Next

Investigate and see if you can make the spatial variables have the same correlograms.

STML

STML-1

(error) File %s: Error at line %d, token %s, %s

Description

Syntax error in the 'stamp' file.

What Next

Correct the syntax error.

Feedback

STML-2

(error) File %s: Line %d, lu_table_template '%s' already defined.

Description

The lu_table_template is already defined. You cannot define the same lu_table_template more than once.

What Next

Change the name of the lu_table_template so that it does not clash with the previous one.

STML-3

(error) File %s: Line %d, in the lu_table_template %s definition, h variable 1 redefined.

Description

In the lu_table_template definition, the variable corresponding to variable_1 is declared more than once.

What Next

Perhaps variable_1 was mistakenly choosen instead of variable_2. Change it to variable_2 or remove one of the lines which define variable_1.

STML-4

(error) File %s: Line %d, lu_table_template %s variable 2 redefined.

Description

In the lu_table_template definition, the variable corresponding to variable_2 is declared more than once.

What Next

Perhaps you mistakenly chose variable_2 instead of variable_1. Change it to variable_1 or remove one of the lines which define variable_2.

STML-5

(error) File %s: Line %d, lu_table_template %s index 1 redefined.

Description

In the lu_table_template definition index_1 is redefined.

Feedback

What Next

Perhaps you mistakenly choose index_1 instead of index_2. Change it to index_2 or remove one of the lines which define index_1.

STML-6

(error) File %s: Line %d, lu_table_template %s index_2 redefined.

Description

In the lu_table_template definition index_2 is redefined.

What Next

Perhaps you mistakenly choose index_2 instead of index_1. Change it to index_1 or remove one of the lines which define index_2.

STML-7

(error) File %s: Line %d, INTERNAL ERROR detected.

Description

Internal error detected.

What Next

Check if the error was caused because of cumulative effect of previous errors. If you cannot solve the error, contact Synopsys support.

STML-8

(error) File %s: In LU_TABLE_TEMPLATE %s variable_1 is not defined.

Description

For a lu_table_template, at least variable_1 must be defined. If variable_1 is not defined, it is an error.

What Next

Define variable_1.

STML-9

(error) File %s: In LU_TABLE_TEMPLATE %s variable_2 is defined but variable_1 is not defined.

Feedback

Description

Variable_2 can be defined only if variable_1 is defined.

What Next

Make the variable_2 definition to be the variable_1 definition and remember to change index_2 to index_1.

STML-10

(error) File %s: In LU_TABLE_TEMPLATE of '%s' index_2 is defined but variable_2 is not defined.

Description

Index_2 can be defined only if variable_2 is defined.

What Next

Define variable_2, to which index_2 refers.

STML-11

(error) File %s: arc label '%s' at or before line %d redefined.

Description

The arc label has already been defined, so the same arc label cannot be defined again.

What Next

Perhaps the arc label is being redefined by mistake. If not, change the arc label and proceed.

STML-12

(error) File %s: The values defined at or before line %d are not same for different rows.

Description

Each row of the value table must have the same size. This size must be equal to the size of the index_2 table.

What Next

Make sure that each row of the 'values' is same as each row of the index_2.

Feedback

STML-13

(error) File %s: For the arc '%s' the LU_TABLE_TEMPLATE name '%s' used at or before line %d is not defined.

Description

The LU_TABLE_TEMPLATE used in the arc definition is not present. The LU_TABLE_TEMPLATE must be defined before using the LU_TABLE_TEMPLATE name.

What Next

Check that the LU_TABLE_TEMPLATE, which is referred to, is present. If the lu_table_templateis not present, define it before use.

STML-14

(error) File %s: index_1 is not defined for the arc '%s' defined at or before line %d, which refers to LU_TABLE_TEMPLATE %s.

Description

In the arc label definition, the index_1 is not defined. Define it.

What Next

index_1 is not defined, please give it a list of points. The index_1 definition is not required for scalar tables.

STML-15

(error) File %s: index_2 is not defined, but var2 is defined for the arc '%s' defined at or before line %d, which refers to LU_TABLE_TEMPLATE %s.

Description

For the arc defined at or before the line specified, index_2 is not defined, but variable_2 is defined.

What Next

Define index_2 or remove the variable_2 definition.

STML-16

(error) File %s: In the arc '%s' defined at or before line %d, variable_1 and variable_2 defined refer to the same variable.

Feedback

Description

variable_1 and variable_2 cannot refer to the same variable for a LU_TABLE_TEMPLATE or an arc.

What Next

Change the variable_1 or variable_2 to a different variable, or have a one dimensional table.

STML-17

(error) File %s: In the arc '%s' defined at or before line %d, %d elements are expected in the one dimensional table but %d were found.

Description

In one dimensional table the number of elements expected in the value table is equal to the number of elements in the index_1 list.

What Next

Make the number of elements in the 'values' table equivalent to the number of elements in the index_1 list.

STML-18

(error) File %s: For the arc '%s' before line %d, expected to find %d groups of values, but found %d groups of values.

Description

The number of rows in a 'values' table is equal to the number of values in index_1. If this is not the case, an error occurs.

What Next

Check the index_1 values and the number of groups of values in the 'values' table and make them equal.

STML-19

(error) File %s: For the arc '%s' defined before the line %d, expected to find %d group of values in a group, but found %d.

Feedback

Description

The number of values in a group must be equal to the number of values in the defined index_2 table.

What Next

Verify that the number of values in a group (row) is equal to the number of elements in the index_2 table.

STML-20

(error) File %s: %s table specified twice for the arc '%s' defined at or before line %d.

Description

For an arc the same type of table (for example, RISE_TRANSITION) cannot be defined more than once. If the table is defined more than once, it is an error.

What Next

Delete one or more occurences of the repeated table types.

STML-21

(error) File %s: %s specified with one of %s/%s/%s for the arc '%s' defined at or before line %d.

Description

If propagation is specified for an arc, rise or fall propagation cannot be defined for the same arc. The same holds true for transition and constraint.

What Next

Have either propagation or fall/rise propgation, transition or fall/rise transition, and constraint or rise/fall constraint.

STML-22

(error) File %s: Specifed constraint tables and cell_delay transition tables for the arc '%s' defined at or before line %d.

Description

An arc can be a constraint arc or a delay arc; it cannot be both. Describe either constraint or delay behavior for an arc.

Feedback

What Next

Do not mix constraint and delay behaviors for the same arc; separate them.

STML-23

(error) File %s: For the arc '%s' defined at or before line %d, transition table specified but corresponding cell delay table not specified.

Description

For an arc, if transition table is specified, corresponding cell delay table must be specified. For example, if rise_transition is specified, cell_rise must also be specified.

What Next

Specify cell delay table if transition table is specified.

STML-24

(error) File %s: For the arc %s' defined at or before line %d, the %s values are not monotonically increasing.

Description

The values defined in index_1 and index_2 are expected to be monotonically increasing. If they are not monotonically increasing, it is an error.

What Next

Change the specified table so that the values are monotonically increasing.

STML-25

(error) File %s: The arc_label %s referred to in line %d as a drive table is not defined.

Description

The arc_label, as an argument to the DRIVE, is not defined.

What Next

Define the arc referred in 'drive' and try again.

STML-26

(error) File %s: In the arc label (%s) referred by drive at or before line %d, expected variable_1 to be OUTPUT_NET_CAPACITANCE, but found it to be %s.

Feedback

Description

The only variable (variable_1) that can be defined for the arc label referred to by 'drive' is output_net_capacitance. If the variable is anything else or is undefined, it is an error.

What Next

Make the variable_1 of the arc label definition to be output_net_capacitance.

STML-27

(warning) File %s: In the scalar table refered to by the arc '%s' at or before line %d, %s defined, ignoring...

Description

For scalar tables, index_1, index_2, variable_1, and variable_2 cannot be specified. If they are, they are ignored.

What Next

If you have defined the table to be scalar by mistake, change it.

STML-28

(error) File %s: In the SCALAR table refered by the arc '%s' at or before line %d, expected to see only one value but found %d.

Description

Scalar tables must have only one value. If more than one value is found, it is an error.

What Next

Change the scalar table in question to have only one value.

STML-29

(warning) File %s: at or before line %d, the value of attribute '%s' is redefined for %s. Replacing previous defined value...

Description

One of the attribute for the specified object is defined more then once. The new redefined value will always replace the existing value, so the last defined value is actually finally written in to the library.

Feedback

What Next

If you do not want to keep the new value, delete the redefined values.

STML-30

(warning) File %s: Parameter defined for port %s in data file but no such port is defined in the model file.

Description

The port parameter is defined for some port that is not defined in the model file.

What Next

Define the port in the model file. If the port name in the port parameter definition is not correct, correct or delete it.

STML-31

(error) Timing arc '%s' is defined in file %s, but thers is no data defined for it in file %s.

Description

The arc that is used in the model file is not defined in the data file.

What Next

Arcs used in the model file must be defined in the data file. Define this arc in the data file and use it in the model file.

STML-32

(error) File %s: Line %d, the arc %s is already instanced in the model file.

Description

An arc can be instanced in a model file only once.

What Next

Change the name of the arc label and define it in the data file, or remove the arc label instance in the model file.

STML-33

(error) File %s: Line %d, The qualifier is already set to %s, but again it is being set to %s.

Feedback

Description

The qualifiers for the delay arcs cannot be set to conflicting types. Check the manual to see what qualifers conflict and cannot be used together.

What Next

Change the qualifiers to remove the conflict.

STML-34

(error) File %s: Line %d, The tlatch edge arc '%s' has not been defined.

Description

The edge arc, which the 'tlatch' arc refers to (in the construct TLATCH = arc_name), is not defined. The corressponding arc must be instantiated first in the model file and then that arc can be referred by the tlatch arc.

What Next

Instantiate the tlatch edge arc before using it in the 'tlatch' construct.

STML-35

(error) File %s: Line %d, The edge arc %s used along with the tlatch arc should be either POSEDGE or NEGEDGE arc, but arc %s is not.

Description

The arc refered by 'tlatch'arc ('tlatch'= edge_arc) has to be a 'posedge' or 'negedge' type. If the arc is not, it is an error.

What Next

Make the edge arc refered by the 'tlatch'arc to be 'posedge' or 'negedge'.

STML-36

(error) File %s: Line %d, Cannot use %s in conjuction with %s.

Description

Some types of arcs cannot be used in conjuction with others. Bitwise is used only in conjuction with 'nonunate', 'inverting', or 'noninverting'; it cannot be used with any other type of arc. Logic can be only in conjuction with 'enable_high' or 'enable_low.

Feedback

What Next

Remove the incompatible arc types from occuring together.

STML-37

(error) File %s: Line %d, The number of ports in start port list is > 1.

Description

The number of ports in the start port list that can be greater than 1 are only for 'inverting', 'noninverting', or 'nonunate' arcs. For any other type of arc the start port can only be a single port.

What Next

If you have more than 1 port as start port, split the port up into different arcs and instantiate it separately.

STML-38

(error) File %s: Line %d, The number of ports in the start port (%d) does not equal the number of end ports (%d) for the BITWISE qualifier.

Description

If the 'bitwise' qualifier is used, the number of ports in the start port must be the same as the number of ports in the end port list.

What Next

You might have missed out some ports; please check for missed ports and correct them.

STML-39

(error) File %s: Line %d, Arc %s: %s can be only one of constrained_pin_transition or related_pin_transition.

Description

In the data file where the arcs are defined, the constraint arc label can have variable_1 or variable_2 to be one of constrained_pin_transition or related_pin_transition.

What Next

Make sure that the constraint arcs have variables defined only as constraint_pin_transition or related_pin_transition.

Feedback

STML-40

(error) File %s: Line %d, Arc %s: found arc tables other than '%s', for this %s arc.

Description

For constraint arc the only tables allowed are 'constraint', 'rise_constraint' or 'fall_contstraint'. If any other table is specified, it is an error. For delay arc the only tables allowed are 'cell', 'cell_rise' or 'cell_fall' and 'transition', 'fall_transition' or 'rise_transition'. If any other table is specified, it is an error.

What Next

Make sure that the tables used to describe the arc are correct.

STML-41

(error) File %s: Line %d, Arc %s: Found tables other than CONSTRAINT.

Description

For width, period, recovery, or removal, only the constraint table can be specified.

What Next

Change the table type to constraint for the previous type arcs.

STML-42

(error) File %s: Line %d, Arc %s: %s can be only one of input_net_transition or output_net_capacitance.

Description

In the data file where the arcs are defined, the delay arc label can have either variable_1 or variable_2 to be as input_net_transition or output_net_capacitance.

What Next

Make sure that the constraint arcs have variables defined as either input_net_transition or output_net_capacitance.

STML-43

(error) File %s: Line %d, Arc %s, Both RISE_TRANSITION/CELL_RISE and FALL_TRANSITION/CELL_FALL must be specified for the arc.

Feedback

Description

For 'inverting', 'noninverting', or 'nonunate' arcs, both rise and fall tables must be specified.

What Next

For 'inverting', 'noninverting', or 'nonunate' arcs specify both rise_transition and fall_transition or cell_rise and cell_fall.

STML-44

(error) File %s: Line %d, Arc %s, Expected to find RISE_TRANSITION/CELL_RISE, but it was not found.

Description

For enable_high, set_high, clear_high, posedge, or disable_high arcs, cell_rise or rise_transition must be present.

What Next

Please specify the rise_transition or the cell_rise table.

STML-45

(warning) File %s: Line %d, Arc %s, Expected to see only the RISE tables but found FALL tables too; ignoring the fall tables...

Description

For enable_high, disable_high, set_high, clear_high, or posedge arcs, only rise tables (rise_transition or cell_rise) are expected, but found fall tables too. The compiler ignores fall tables

What Next

This is just an information message. If you want to remove the warning message, remove the fall table.

STML-46

(error) File %s: Line %d, Arc %s, Expected to find FALL_TRANSITION/CELL_FALL, but it was not found.

Description

For enable_low, set_low, clear_low, posedge, or disable_low arcs, fall_transition or cell_fall must be present.

Feedback

What Next

Specify fall tables.

STML-47

(warning) File %s: Line %d, Arc %s, Expected to see only the FALL tables but found RISE tables too; ignoring the RISE tables.

Description

For enable_low, disable_low, set_low, clear_low, or posedge arcs, only fall tables (cell_fall or fall_transition) were expected, but found rise tables too. The compiler ignores rise tables.

What Next

This is just an information message. If you want to remove the warning message, remove the fall table.

STML-48

(error) File %s: Line %d, Arc %s, Transition table not accompanied by corresponding cell delay tables.

Description

Transition tables must be accompanied by corresponding cell delay tables. For example, if RISE_TRANSITION is specified it must be accompnied by CELL_RISE table.

What Next

Check to see that the transition table is accompanied by corresponding cell delay table.

STML-49

(error) File %s: Line %d, The mode %s is already defined.

Description

The mode you are trying to define is already defined.

What Next

Change the mode name.

Feedback

STML-50

(error) File %s: Line %d, The mode value %s is repeated for the mode %s.

Description

The value is repeated for the given mode.

What Next

Remove the repetitive name. Either delete it or replace it with some other name.

STML-51

(error) File %s: Line %d, The mode used %s is not defined.

Description

The mode used in the arc definition is not defined.

What Next

Define that mode (before the arc definition) and use it in the arc definition.

STML-52

(error) File %s: Line %d, Could not find mode_value %s in the mode_definition of %s.

Description

The mode_value used in the arc_defintion is not found in the mode definition.

What Next

Either add the mode_value in the mode_definition or use one of the defined mode_values.

STML-53

(error) File %s: Line %d, %s already defined as a %s.

Description

The name given for the port, pin, or bus declaration is already used for declaring either a port, a pin, or a bus. You cannot have more than 1 port, pin, or bus with the same name.

What Next

Change the name of the port being declared so that there is no conflict.

Feedback

STML-54

(error) File %s: Line %d, %d ports are declared to make the bus %s of width %d.

Description

The number of ports declared is different from the bus_width of the bus that contains the ports. They must be equal.

What Next

Make the bus width equal to the the number of ports that make up the bus.

STML-55

(error) File %s: Line %d, %s is not defined as a PORT/PIN/BUS.

Description

The port, pin, or bus used is not defined in the port_definitions. The ports must be defined before they are used in the arcs.

What Next

Define the port you are using in the arcs before using them.

STML-56

(error) File %s: Line %d, %s is a bussed pin, and cannot be used as a start port for this arc.

Description

Bused pins or ports can be used as a start_port only for 'inverting', 'noninverting', or 'nonunate' arcs. No other arc can have start ports > 1.

What Next

If the arc is not 'inverting', 'noninverting', or 'nonunate', do not have start_port >1.

STML-57

(error) File %s: Line %d, ENABLE arc not of LOGIC type; must end in a TRIOUT port. However, %s is not a TRIOUT port.

Feedback

Description

enable_high or enable_low arcs without the 'logic' qualifier must end in a 'triout' port. If the arc does not end with this, it is an error.

What Next

Either make the 'enable' arc end in a 'triout' port or add the 'logic' qualifer if there is a logic after the 'tristate' buffer.

STML-58

(error) File %s: Line %d, Port %s expected to be of INPUT/INOUT/OUTPUT but found to be %s.

Description

The start for delay_arcs is expected to be of input, inout, or output type. If the start is anything other than this, it is an error.

What Next

Make the start port of the delay arcs either input, output, or inout type.

STML-59

(error) File %s: Line %d, Port %s expected to be of INOUT/OUTPUT/TRIOUT but found to be %s.

Description

The end_port for delay_arcs are expected to be either triout, inout, or output type. If the end_port is anything other than one of these, it is an error.

What Next

Make the end port of the delay arcs either triout, output, or inout type.

STML-60

(error) File %s: Line %d, %s port indicated to be of BUSSED type but was found to be of NON BUSSED type.

Description

The port is infered to be a bus type because it is of port[start:end] type of usage. However, 'port' is not of bused type.

Feedback

What Next

If it was mistakenly declared to be a nonbused type, modify the port definition to be a bused type. If the usage in the arc definition was wrong, modify the usage.

STML-61

(error) File %s: Line %d, The bus limits %d:%d used for the bus '%s' is not within the limits %d:%d of the port declaration.

Description

The bus limits used in the arc definition are not within the bus limits of the port declaration.

What Next

Either change the bus limits of the port declaration or change the bus limits in the usage so that the bus limit usage is within the port declaration bus limits.

STML-62

(error) File %s: Line %d, The port name %s specified in the TLATCH arc output port does not exist in the corresponding edge delay arc.

Description

The output port specified in the 'tlatch' arc must be present as an output port in the correponding edge delay arc. If the arc is not, it is an error.

What Next

Make the output port of the 'tlatch' arc and the corresponding edge delay arc the same

---

STML-63

(warning) File %s: Line %d, %s specified for %s, which is not an output port.

Description

'drive' cannot be specified for output ports only.

What Next

Remove the 'drive' specification from the port parameter definitions in the data file.

Feedback

STML-64

(error) File %s: Line %d, the arc %s referred to by TLATCH qualifier has not been instanced.

Description

The arc referred to by 'tlatch' = <arc_name> construct must be instanced before referring to it.

What Next

Instance the arc referred to by 'tlatch'before using it in 'tlatch' construct.

STML-65

(error) File %s: Line %d, The number of output ports in TLATCH arc and the corresponding edge arc %s do not match.

Description

The ports used as output port in the 'tlatch' arc and the corresponding edge delay arc must be the same.

What Next

Use the same output ports for the 'tlatch' arc and the corresponding edge delay arc.

STML-66

(error) File %s: Line %d, Cannot create SHORTED ports before defining the ports.

Description

The 'shorted' port section only comes after the ports used in the 'shorted' ports are defined.

What Next

Define the ports that you are 'shorting' before using them.

STML-67

(error) File %s: Line %d, The port %s used in the SHORTED ports is not defined.

Feedback

Description

Ports must be defined before using the 'shorted' port construct on the ports that you are shorting.

What Next

Create the ports you want to short before 'shorting' them.

STML-68

(error) File %s: Line %d, Buses of different lengths shorted.

Description

Buses of different lengths cannot be shorted.

What Next

Make sure that buses are of the same length while shorting.

STML-69

(error) File %s: Line %d, Port %s repeated twice in SHORTED ports construct.

Description

Repeating the same port name twice in shorted ports is not allowed.

What Next

Remove the repetition.

STML-70

(error) File %s: Line %d, The bus limits declaration (%d:%d) is not consistent with its use (%d:%d) for the bus %s.

Description

The bus was declared with limits whose order (start and end limits) are inconsistent with the use.

What Next

If the start and end index of a bus is in particular order, the usage of the bus must reflect the same order.

Feedback

STML-71

(error) File %s: Line %d, The %s clock source pin %s is not defined.

Description

You used a pin as a source for either a master or generated clock, but it was not defined as a port or internal pin.

What Next

Either define the generated or the master clock source as a port or internal pin; or if the pin name specified is an error, change the name to reflect the correct port or pin name.

STML-72

(error) File %s: Line %d, The master clock source pin %s is found to be of type %s.

Description

The master for a generated clock can only be an input or inout type. If it is of any other type it must be a generated clock.

What Next

Check the port or pin definition of the source pin of the master and change it to one of the allowed types.

STML-73

(error) File %s: Line %d, Generated Clock source pin %s is of input type.

Description

A direction of the generated clock source pin cannot be input. If it is, an error occurs.

What Next

Define generated clock only on output, inout, or internal pins.

STML-74

(error) File %s: Line %d, The %s factor used %d is not a power of two.

Description

The multiplication or division factor must be a power of two. If the factor is not, it is an error.

Feedback

What Next

If the multiplication or division factor is not a power of two, try to model the generated clock with 'edges' and 'edge_shift'.

STML-75

(error) File %s: Line %d, The duty_cycle specified (%f) is not within the limits (0 < duty_cycle <100).

Description

The duty cycle must be within 0 and 100.

What Next

Change the duty cycle to be within 0 and 100.

STML-76

(error) File %s: Line %d, The generated clock %s has already been defined.

Description

The generated_clock definition you are trying to define in the data file is already defined. There can be only one definition for a generated clock.

What Next

Either change the name of the redefined clock, or remove the definition if it is really a repetition.

STML-77

(error) File %s: Line %d, In the generated clock specification, the number of edges (%d) does not equal the number of edge_shifts (%d).

Description

If 'edge_shift' has been specified using edge_shift(), the number of edge_shifts must equal the number of edges specified.

What Next

If you want to use edge_shift, specify one edge shift for each edge specified.

Feedback

STML-78

(error) File %s: Line %d, Expected to find a float value for the %s, but found something else.

Description

The value for the attribute was expected to be a float, but something else is found (for example, strings).

What Next

Make sure the attribute is a float.

STML-79

(error) File %s: Line %d, non-positive values found for %s.

Description

The argument was expected to be positive, but it is not.

What Next

Make the necessary values positive.

STML-80

(error) File %s: Line %d, Expected to find an integer value for the %s, but found something else.

Description

The value for the attribute is expected to be an integer, but something else is found (for example, strings).

What Next

Make sure that attribute is an integer.

STML-81

(warning) File %s: Line %d, The data defined for generated clock '%s' has not been defined in the model file.

Feedback

Description

The generated clock defined in the data file should be defined in the model file first. Otherwise it is a potential error.

What Next

Please define the generated clock in the model file.

STML-82

(error) File %s: Line %d, The '%s' pin %s is not found in the design.

Description

The pin you are using has not been defined in the design.

What Next

Define the pin before using it.

STML-83

(error) File %s: Line %d, The generated clock '%s' is being redefined.

Description

The generated clock is redefined in this model file. The generated clock is defined elsewhere in the model file with the same name. There can be only one generated clock defintion per generated clock name, per model file.

What Next

Have only one generated clock definition per generated clock name, per model file.

STML-84

(error) Unable to open '%s' file - %s.

Description

Unable to open either the data file or model file.

What Next

Check the path name of the data or model file in question and look at the search path if the file is present in the search path. If the file is not present in the search path, update the search path. If the file is present in the search path, perhaps the access permission is not there.

Feedback

STML-85

(error) File %s: Line %d Arc %s: expected to find '%s' table but it was not found.

Description

You receive this message if the *compile_stamp_model* command does not find the arc RISE_CONSTRAINT or FALL_CONSTRAINT in the Stamp data file. For the following arcs, the following tables are expected:

```
RECOVERY_RISE_CLK_RISE - RISE_CONSTRAINT;
RECOVERY_RISE_CLK_FALL - RISE_CONSTRAINT;
RECOVERY_FALL_CLK_RISE - FALL_CONSTRAINT;
RECOVERY_FALL_CLK_FALL - FALL_CONSTRAINT;
REMOVAL_RISE_CLK_RISE - RISE_CONSTRAINT;
REMOVAL_RISE_CLK_FALL - RISE_CONSTRAINT;
REMOVAL_FALL_CLK_RISE - FALL_CONSTRAINT;
REMOVAL_FALL_CLK_FALL - FALL_CONSTRAINT.
```

What Next

Edit your Stamp file to add the required information, then reexecute *compile_stamp_model*. For information about creating Stamp files, see the *PrimeTime Modeling User's Guide*, Chapter 6.

STML-86

(warning) File %s, Line %d, Arc %s: expected to find only '%s' table, but also found '%s' table which will be ignored.

Description

For the type of arc that is being defined, found some other table types too.

What Next

Other than the expected delay tables found, some other delay tables also presented in the file.

STML-87

(warning) File: %s, Line: %d, Arc: %s Found two edge specifications where only one was expected. Ignoring the second edge specification.

Description

For SETUP, HOLD, DELAY, NOCHANGE, PERIOD, and WIDTH only one edge needs to be specified. If two edges are specified, only the first edge specified is considered.

Feedback

What Next

If the first edge being considered as the triggering edge is incorrect, please change the file.

STML-88

(warning) File: %s, Design name not specified in the MODEL DATA file.

Description

Design name has not been specified in the MODEL DATA file.

What Next

Please specify the design name in the MODEL DATA file.

STML-89

(warning) File %s, Line %d: Design name '%s' specified in the MODELDATA file (%s) does not match the one in MODEL file '%s'.

Description

There is a discrepancy in the design name between MODELDATA file and MODEL file.

What Next

Make sure that the design name in the MODELDATA file and MODEL file match.

STML-90

(warning) File: %s, Design name not specified in the MODEL file.

Description

Design name has not been specified in the model file.

What Next

Please specify the design name in the model file.

STML-91

(warning) Arc '%s' defined in the stamp data file '%s' has not been used in the model file '%s'.

Feedback

Description

Data for an arc has been defined in the model data file, but the same arc has not been defined in the model file.

What Next

If you need that arc, define the arc in the model file. If the arc is not needed, remove it from the modeldata file.

STML-92

(error) File %s, Line %d: Version %s for MODEL_VERSION illegal.

Description

For this release MODEL_VERSION can be only 1.0.

What Next

Change the MODEL_VERSION string to 1.0.

STML-93

(error) File %s, Line %d: Version %s for MODELDATA_VERSION illegal.

Description

For this release MODELDATA_VERSION can be only 1.0.

What Next

Change the MODELDATA_VERSION string to 1.0.

STML-94

(information) No timing arcs are defined from or to pin '%s'.

Description

The pin or port does not have any arcs coming in or going out.

What Next

If this is a real error please fix it.

STML-95

(Error) File %s, Line %d: The number of bits referred to by the two expressions %s, %s are different (%d, %d).

Description

The number of bits the operation performed for the binary operators (!, &, ^) must be equal.

What Next

Check if the effective bus widths are the same.

STML-96

(Error) File %s, Line %d: Cannot specify more than one port for clock in constraint arcs.

Description

The clock port in the constraint arc cannot consist of more than one port.

What Next

If you want to constrain a port for different clocks, create separate arcs from each clock port.

STML-97

(Error) File %s, Line %d: Different attribute types mixed in the list.

Description

Different attribute types cannot be mixed in a list attribute. In a list, all the attributes have to be of the same type.

What Next

Make the attributes the same type in the list.

STML-98

(error) File %s, Line %d: The STAMP language reserved %s attribute '%s' has been defined as type '%s', but is used with a value of type '%s'.

Feedback

Description

You receive this message because the data type of the attribute value that you are using in your STAMP model files is wrong. To use a reserved attribute in STAMP and compile it, you need to define its value to be the same type as the application-defined lib, lib_cell, or lib_pin attribute, or one of these attributes defined by STAMP language:

```
k_process_cell_rise
    k_temp_cell_rise
    k_volt_cell_rise
    k_process_cell_fall
    k_temp_cell_fall
    k_volt_cell_fall
    k_process_rise_transition
    k_temp_rise_transition
    k_volt_rise_transition
    k_process_fall_transition
    k_temp_fall_transition
    k_volt_fall_transition
    original_pin
```

What Next

Check and correct the attribute definitions in the STAMP files, then try compile the STAMP again.

STML-99

(error) File %s, Line %d: The user attribute '%s' for %s has already been defined as type '%s', but is used as '%s'.

Description

The data type for the attribute has already been defined to be of one type in the STAMP files, but is used as a different type. For example, the attribute is defined to be of type string, but is used as an integer.

What Next

Check and correct the attribute definitions in the STAMP files, then try compile the STAMP again.

STML-100

(warning) File %s, Line %d: The attribute '%s' is used as a list, but is not defined to be of list type.

Feedback

Description

The attribute was not defined to be a list but is used as a list.

What Next

Check the attribute definition and change the usage accordingly.

STML-101

(warning) File %s, Line %d: The attribute '%s' is defined to be of list type, but is not used as a list type.

Description

The atribute is defined to be of list type but is not used as a list type.

What Next

Check the attribute definition and change either one of definition/usage to make both of them consistent.

STML-102

(error) File %s: The gate_type %s referred to in line %d is not a valid type.

Description

Currently, supported gate types are DOMINO_N_FOOTED, DOMINO_N_FOOTLESS, DOMINO_P_FOOTED, DOMINO_P_FOOTLESS, DOMINO_LATCH, DOMINO_RETAIN, DOMINO_FLOP.

What Next

Correct the gate_type and try again.

STML-103

(error) File %s: Cannot use COND with SDF_COND for an arc, line %d.

Description

Conditions on a delay/constraint arc can be specified using either the COND construct or by using the SDF_COND with WHEN construct, but not both.

What Next

Choose one form of defining conditional arcs and delete the other.

Feedback

STML-104

(error) File %s: Line %d, Arc %s One of RISE_TRANSITION/FALL_TRANSITION/ TRANSITION has to be specified for this arc.

Description

For 'posedge' and 'negedge' arcs, one of rise and fall delay tables must be specified.

What Next

For 'posedge' and 'negedge' arcs specify at least one of cell_rise and cell_fall.

STML-105

(warning) File %s: Line %d, Arc %s One of RISE/FALL TRANSITION or RISE/FALL PROPAGATION not specified for this arc. The missing data will be replaced by the data from the opposite TRANSITION/PROPAGATION.

Description

For 'posedge' and 'negedge' arcs, if one of rise/fall data is missing then the missing data is copied from the existing data. For example, if a 'posedge' arc is defined with only CELL_RISE, then the CELL_FALL data will be taken from the CELL_RISE data. The same holds true in case of RISE/FALL_TRANSITION.

What Next

Currently the PrimeTime timing engine cannot handle 'posedge' and 'negedge' arcs that are single transition (rise only or fall only). Hence when compiling such arcs from STAMP, they are forced to have data for both polarities by replicating the values.

STML-106

(error) Option -remove_internal_arcs is no longer supported.

Description

Option -remove_internal_arcs is no longer supported for the compile_stamp command.

What Next

If the STAMP model is generated via the extract_model command and has internal arcs, then use extract_model -remove_internal_arcs to remove the internal arcs from STAMP model. Then compile with complie_stamp. If you are hand-creating STAMP model and you do not want the compiled stamp model to have internal arcs, please remove all internal arcs manually from the stamp model file.

Feedback

STML-107

(error) File %s: Incorrectly specified a delay arc for the arc label '%s' on or before line %d that uses constraint arc data.

Description

You receive this message if *compile_stamp_model*, while reading a Stamp file, detects an arc that is first defined as a delay arc and then used as a constraint arc. You must define and use an arc either as a delay arc or as a constraint arc; it cannot be both.

What Next

Edit your stamp file to correct the errors.

For information about creating stamp files, see the user guide.

STML-108

(error) File %s: Line %d, Arc %s the expected %s table is not found in the data file.

Description

For 'POSEDGE' and 'NEGEDGE' specified for constraint arcs, the first edge specification is for data and the second edge spec is for clock. For example, a SETUP(POSEDGE, NEGEDGE) arc means the rising data is checked against falling clock, so a RISE_CONSTRAIN table is required in the data file. However, if you only specify one edge in the arc definition, it only means for the clock edge and both transitions for the data will be checked. For example, a hold arc HOLD(POSEDGE) means both the rising and the falling edge of the data will be checked against the falling edge of the clock, so both RISE_CONSTRAINT and FALL_CONSTRAINT tables are expected, or you can simply use CONSTRAINT if the timing numbers are the same for both edges.

What Next

Please fix the problems identified for the arc and try compile again.

STML-109

(error) Generated clock '%s' is defined in file %s, but thers is no data defined for it in file %s.

Description

The generated clock that is defined in the model file is not defined in the data file.

Feedback

What Next

Generated clocks that are defined in the model file must be also be defined in the data file. Add the data definition for the generated clock in the data file before compile.

STML-110

(error) File %s:Line %d, the conditions defined for mode %s are either not mutually exclusive or not complete.

Description

The conditions you defined for the mode values of the mode group must be mutually exclusive and must be complete as a set. In another words, there should be exactly one mode in the mode group that can be enabled under the specified conditions, given any combinations of variable values in the condition expressions. In addition, you should not include modes that have conditions with modes that do not have conditions in one mode group.

What Next

Check the conditions defined for the modes.

STML-111

(error) File %s, Line %d: the table values are missing.

Description

A table must have values defined by VALUES.

What Next

Please define the table values for the arc before compile.

STML-112

(error) File %s, Line %d: syntax error at or before token %s, '%s' is expected.

Description

A syntax error has been found during compile.The syntax error must be fixed for successful compile.

What Next

Please fix the syntax error and try compile again.

Feedback

STML-113

(error) File %s, Line %d: syntax error at or before token %s, one of the port direction specifiers '%s' is expected.

Description

A syntax error has been found during compile.The syntax error must be fixed for successful compile.

What Next

Please fix the syntax error and try compile again.

STML-114

(warning) File %s, Line %d: skew check is not currently supported.

Description

The skew check is not supported.

What Next

Please remove the arc for skew check and try compile again.

STML-115

(warning) File: %s, Line: %d, found unexpected "CLKGAT" attribute defined for arc %s. Ignoring the attribute...

Description

The CLKGAT attribute is to flag the constraint arcs as clock_gating checks. It is valid only for SETUP, HOLD, and NOCHANGE arcs. It will be ignored if defined for any other types of arcs.

What Next

Please correct the arc in the STAMP file before using stamp compiler.

STML-116

(error) Found %s in the "when" expression '%s' defined for mode value '%s' in group '%s'.

Feedback

Description

The conditional expression defined for the mode is incorrect. It does not comply with the syntax definition for logical "when" expressions, or it refers to some undefined objects.

What Next

Please correct the specified error and try compile again.

STML-117

(error) File: %s, Line %d, found %s in the "when" expression '%s' defined for arc '%s'.

Description

There is either syntax error in the specified conditional expression, or the expression refers to some undefined port/pins in the design.

What Next

Please correct the specified error and try compile again.

STML-118

(error) Found mixed conditional expressions defined with both WHEN/SDF_COND and COND syntax for the modes of mode group '%s'.

Description

All the conditional expressions defined for a set of mode values within one mode group should be either the old COND syntax or the new WHEN/SDF_COND syntax. You cannot mix them in one mode group.

What Next

Please choose one syntax for all the mode values. The new WHEN/SDF_COND syntax is recommended.

STML-119

(warning) Found conditional expression in mode/arc defined by the old COND syntax. WHEN/SDF_COND syntax is recommended.

Description

To support the analysis of conditional modes/arcs more efficiently, it is recommended to use the WHEN/SDF_COND syntax when defining the conditional mode and timign arcs.

Feedback

What Next

Please use the WHEN/SDF_COND syntax if possible.

STML-120

(warning) Port '%s' appears to be unbussed.

Description

You receive this message to warn you that *compile_stamp_model* has detected a port in your Stamp file that appears to be part of a bus, but has not been declared as a bus.

For example, the following declaration creates three ports, but no bus.

```
INPUT A[2];
INPUT A[1];
INPUT A[0];
```

By contrast, the following declaration creates a port bus named A, and 3 ports, A[2], A[1], and A[0].

INPUT A[2:0];

This is a warning to help you identify places where you might have omitted bus declarations. Missing buses can cause problems later when you try to link the design.

What Next

This is a warning message only; no action is required on your part. However, if the ports should be bussed, edit your stamp file to add the correct syntax for a bus declaration, then reexecute *compile_stamp_model*.

For information about creating stamp files, see the user guide.

STML-121

(Error) File %s, line %d: %s.

Description

There are some problems with the RELATED_OUTPUT defined for the timing arc as indicated.

What Next

Make sure that the RELATED_OUTPUT port:

1. Is defined only once; 2. Does not refer to an INPUT port; 3. Is not the same as either of the 2 end ports of the arc; 4. Is not defined for a WIDTH, or PERIOD arc.

Feedback

STML-122

(warning) File %s, line %d: %s.

Description

A RELATED_OUTPUT port has been defined for the indicated timing arc in the STAMP model file, but no delay tables defined for the timing arc in the STAMP data file refers to the related output port, so it is not needed.

What Next

Please make sure that the RELATED_OUTPUT port is really not needed.

STML-123

(error) File %s, line %d: DRIVE %s refers to related_ouput_load.

Description

The tables defined for the DRIVE arc refers to related_output_load. This is not supported in timing analysis.

What Next

Please make sure that the DRIVE arc does not depend on any related_output load.

STML-124

(error) File %s, line %d: %s has already been defined for arc %s.

Description

The indicated table field has been defined more than once for the timing arc.

What Next

Please correct the error and compile again.

STML-125

(error) File %s, line %d: in the table for arc '%s', %s is defined without %s.

Description

You have to define the required table fields before defining the indicated one. For example, INDEX_2 and VARIABLE_2 have to be defined before you can define INDEX_3 and VARIABLE_3.

Feedback

What Next

Please correct the table definition and compile again.

STML-126

(error) File %s, Line %d: the VARIABLE_3 must be related_output_capacitance.

Description

The VARIABLE_3 can only be related_output_capacitance in a delay table.

What Next

Please correct the definition of the table in the STAMP data file and try compile again.

STML-127

(warning) File %s: Line %d, Port %s expected to be of direction INOUT/OUTPUT/TRIOUT but found to be %s.

Description

The end_port for delay arcs are expected to be either triout, inout, or output type. If the end_port is anything other than one of these, it is suspectable and please verify.

What Next

Make sure the end port of the delay arcs are of direction triout, output, or inout. If not, please verify that the directions and the arcs are really correct.

STML-200

(error) File %s: Line %d, the arc '%s' referred to by the DELAY qualifier is not defined.

Description

You receive this message if *compile_stamp_model*, while reading a Stamp file, detects an arc that is referred to by the DELAY = <arc_name> construct, but has not been defined. The arc must be defined before the definition of the RETAIN arc.

What Next

Edit your stamp file to correct the error. If the arc referred to by the DELAY qualifier is not defined, add the definition. If the definition of the missing arc DELAY arc is after the RETAIN arc, reverse the order of the two definitions.

For information about creating stamp files, see the user guide.

Feedback

STML-201

(error) Cannot compile multiple data files in LIB format.

Description

You receive this message from *compile_stamp_model* if *-data-files* has more than one data file in its list and the *-formats* option has *lib*. The *compile_stamp_model* command cannot compile multiple stamp data files to a single library file.

What Next

Either choose to output in DB format, or compile each data file separately.

STML-202

(error) Cannot expand busses for LIB format

Description

You receive this message from *compile_stamp_model* if you sepcify *-expand_buses* in conjunction with the *lib* output format. The *compile_stamp_model* command cannot expand busses when writing liberty format.

What Next

Either choose to output in DB format, or do not expand the busses by removing *-expand_buses* from the command line.

STML-203

(error) The LIB format requires the -library_cell option

Description

You receive this message from *compile_stamp_model* if you do not sepcify *-library_cell* in conjunction with the *lib* output format. The *compile_stamp_model* requires the *-library_cell* option whenever writing liberty format.

What Next

Either choose to output in DB format, or add the *-library_cell* option to the command line.

STML-204

(Error) The -update option cannot be used when writing\liberty format

Feedback

Description

You receive this message from *compile_stamp_model* if you specify the *-update* option in conjunction with writing liberty format. The *compile_stamp_model* cannot update a liberty format file.

What Next

Either choose to output in DB format, or remove the *-update* option from the command line.

STROKE

STROKE-001

(Error) Specified stroke sequence string, %s, is not valid.

Description

The specified stroke sequence string is not valid. The sequence is comprised of an optional sequence of key modifiers and separated from the path sequence which is a sequence of one or more grid numbers in the range 1-9. See the man page for the set_gui_stroke_binding command for detailed documentation on the format for stroke sequences.

STROKE-002

(Error) Failed to set the stroke binding because the built-in stroke command %s does not exist

Description

The specified built-in stroke command name is not valid. Use the report_gui_stroke_builtins command to get a report listing the available built-in commands.

STROKE-003

(Error) Failed to set the gui stroke preference %s because the value was not valid for that preference.

Description

The specified stroke preference value is not valid. Please refer to the man page for the set_gui_stroke_preferences command for more details on the preferences.

Feedback

STROKE-004

(Error) Failed to set the gui stroke preference %s because the preference key was not valid.

Description

The specified stroke preference key does not exist. Please refer to the man page for the set_gui_stroke_preferences command for more details on the preferences.

STROKE-005

(Error) Stroke dictionary %s does not exist.

Description

The specified stroke dictionary does not exist. Use the report_gui_stroke_bindings commands to view the dictionaries that are defined as well as the bindings that they specify.

SVR

SVR-1

(error) Unable to open file '%s'.

Description

The Verilog file you tried to open does not exist or has incorrect permissions.

What Next

Verify the file name and permissions.

SVR-2

(information) Verilog read failed.

Description

This is a summary informational message indicating that the Verilog file could not be read. Previous error messages will point you at the actual problem source. There are two types of syntax errors: a real violation of Verilog syntax, or reading a Verilog file that has non-structural or other unsupported constructs with this reader.

Feedback

What Next

Review previous error messages. Then, either correct the actual Verilog syntax errors in the file and reread the file, or use a Verilog reader that supports the constructs that are flagged as syntax errors.

SVR-3

(error) Unsupported construct '%s'\n \tat line %d in '%s'.

Description

The reader detected an unsupported construct. Not all unsupported constructs are trapped in this way. Many show up as more simple syntax errors.

What Next

Either correct the error by removing the construct or use a Verilog reader that supports the construct.

SVR-4

(error) Expected %s but found '%s'\n \tat line %d in '%s'.

Description

This message covers a wide variety of syntax errors. A token was expected, but something else was found. For example, after a module formal list, a close paren is expected, but if it is omitted and a semicolon is found, this message appears.

This can be an indication of a real syntax error. It is also possible for this message to be used when Verilog constructs, which are not supported by this reader, are encountered.

What Next

Review the line number reported in the message and determine if a real syntax error needs to be corrected or if the file contains unsupported constructs.

SVR-5

(error) Expected identifier after %s\n \tat line %d in '%s'.

Description

An identifier is expected after the token shown and something else was found.

Feedback

What Next

Review the line number reported in the message and determine if a real syntax error needs to be corrected or if the file contains unsupported constructs.

SVR-6

(error) Premature end-of-file reading '%s'.

Description

The reader detected end-of-file before it was expected. For example, an end-of-file within a module construct before the endmodule would cause this message to be raised.

What Next

Correct the error and reread the file.

SVR-8

(error) Port '%s' is not defined in module terminal list\n \tbut is defined in an %s statement \n \tat line %d in '%s'.

Description

While processing an input, output, or inout statement, a port was found which did not exist anywhere in the module terminal list.

What Next

Correct the module terminal list or remove the port wire from the appropriate input/output/inout declaration.

SVR-9

(error) Duplicate wire/tri/wand/wor declaration for '%s'\n \tat line %d in '%s'.

Description

The named wire was found in a wire, tri, wand, or wor statement. However, the wire was already declared in a similar statement.

What Next

Ensure that each wire is only declared once.

Feedback

SVR-10

(error) Illegal assignment %s\n \tat line %d in %s.

Description

An assign statement (or wire statement with inline assignment) has one of several errors:

- Nothing is on the left side of the '='. • The left side of the assignment contains an undeclared net or unexpected characters. • The right side of the assignment contains an undeclared net or unexpected characters.

Note that the following syntax for *assign* is not supported:

assign z = (a);

Use of parentheses is considered non-structural.

What Next

Correct the syntax error and reread the file.

SVR-11

(error) Cannot assign to constant%s\n \tat line %d in %s.

Description

There is a constant on the left side of an assignment, which is not allowed.

What Next

Correct the error, and reread the file.

SVR-13

(error) Number of ports of instance is inconsistent with other instances\n \tat line %d in %s.

Description

All ordered (non-name based) instances of a design must have the same number of ports. The first such instance sets the number. The following example would raise this error.

```
ND2 i1 (a, b, c);
ND2 i2 (d, e);
```

Feedback

The first instance has 3 ports, whereas the second has only 2. It's possible that the second instance is missing a comma. For example,

```
ND2 i1 (a, b, c);
ND2 i2 (d, , e);
```

What Next

Examine the instances to determine which is correct. One might be missing a comma.

SVR-14

(error) Indexing into non-array '%s' is not allowed\n \tat line %d in %s.

Description

A connection has a wire or port with bus notation, and the wire or port was not declared as a bus. For example, the following would raise this error.

```
input A;

ND2 i1 (A[0], b, c);
```

What Next

Determine if the wire or port declaration or usage is correct.

SVR-15

(error) Width of port %s (%d) is inconsistent with other instances (%d)\n \tat line %d in %s.

Description

The first instance of a design's port sets its width. The width is inferred from the connections to that port. This error indicates, and a subsequent instance has, a different width for a particular port. The following example would raise this error.

```
D1 i1 (A[15:0], b, c);
D1 i2 (A[17:16], e, f);
```

What Next

Examine the various instances of the design to see which one is correct.

SVR-16

(error) Constant width overflow\n \tat line %d in %s.

Feedback

Description

The constant is too large to be represented. Constants cannot exceed 32K bits.

What Next

Correct the error and reread the file.

SVR-17

(error) %s constant requires %d bits\n \twhich is too large for %s width %d\n \tat line %d in %s.

Description

The constant specified is too wide for the given width. The default width for a decimal constant is 32 bits. In all other cases, the width would be specified as in 64'b0. An example error would be specifying a decimal number 2535353678882999122 without a width.

What Next

Correct the error and reread the file.

SVR-18

(error) Slice direction [%d:%d] does not match array direction\n \tat line %d in %s.

Description

An array (bus) was declared either ascending (like A[0:3]) or descending (like A[3:0]). The reference to this array is inconsistent with the way it was declared. For example, if the declaration is A[3:0], a reference like A[0:1] would raise this error.

What Next

Correct the error and reread the file.

SVR-19

(error) Index range [%d:%d] is not within bounds [%d:%d]\n \tat line %d in %s.

Description

Some or all of the array (bus) indecies of the reference are out of range of the declaration. For example, if the bus was declared A[15:0], A[31:0] would raise this error, because indecies 31 down to 16 are out of bounds.

Feedback

What Next

Correct the error and reread the file.

SVR-20

(error) Non-terminated comment starting at line %d\n \tof '%s'

Description

The reader detected end-of-file in the middle of a C-style comment.

What Next

Go to the line number mentioned, and find where the comment should be terminated.

SVR-21

(information) %s converted to a wire with no special attributes\n \tat line %d in %s

Description

The verilog constructs wand, wor, and tri are converted to a simple wire with no special attributes. This is just an informational message.

What Next

No action.

SVR-22

(error) Duplicate instantiation of '%s' (first instance at line %d)\n \tat line %d in %s

Description

A duplicate instance name was found. The line number of both the duplicate and the original are shown.

What Next

Rename one of the duplicates.

SVR-23

(error) Duplicate module '%s' (first occurrence at line %d)\n \tat line %d in %s

Feedback

Description

A module is defined more than once in the file. The line number of both the duplicate and the original are shown.

What Next

Rename one of the duplicates.

SVR-24

(warning) Ignored '%s' construct\n \tat line %d in '%s'.

Description

This message covers a variety of constructs which are ignored by the native verilog reader, including *specify*, *parameter*, and so on.

This can be an indication of a real problem, especially in the case of *parameter*. The native verilog reader does not support parameters, so if the parameter is being used, other syntax errors will follow. If the parameter is just defined but not used, then ignoring it will be sufficient.

What Next

In almost all cases, no action is necessary. If you have real parameters in your netlist, you must use a different verilog reader which understands parameters.

SVR-25

(error) Global reference to '%s' not valid in this context\n \tat line %d in '%s'.

Description

Global references are inter-module references, for example, a connection to a wire in a different module like 'global.gnd'. Although this is part of the verilog language, the native verilog reader has very limited support for global references. They can only be used in connections - they cannot be used in assign statements, tran statements, and so on.

This error is generated when a global reference is used in an unsupported context.

What Next

For any usage of global references other than in a connection, you need to use a different verilog reader.

Feedback

SVR-26

(error) Port '%s' has no defined direction (input/output/inout)\n \tin module %s at line %d in file %s.

Description

You received this message because the named port was defined in the module terminal list, but did not appear in an input, output, or inout statement. The line number reported is the line number in the module statement where the port is referenced.

What Next

Add an appropriate input, output, or inout statement for the named port.

SVR-27

(error) Duplicate declaration of port '%s' in instance '%s'\n \tat line %d in '%s'.

Description

You received this message because the named port was defined twice in the terminal list of the given instance, as in the following example:

```
AN2 i0 (.A(a), .A(b), .Z(z));
```

What Next

Remove or replace the duplicate port.

SVR-28

(warning) Number %s is too big. It will be truncated to 32 bits\n \tat line %d in '%s'.

Description

When reading a bus (array) declaration or instance, the msb or lsb was bigger than 32 bits, and was truncated. For example:

```
BOX u1 (.A(a[36'hF00000001:0]), .Z(z));
```

The range of a will be truncated to 1:0.

What Next

Verify that the netlist is correct. This could be a typo.

Feedback

SVR-31

(error) Expected %s '%s' to be declared as a range\n \tat line %d in '%s'.

Description

A port has been declared in an input/output/inout statement as a scalar, but was referenced in the module terminal list using a range. In this example:

```
module test (a, b[0], z);
input b;
```

port 'b' is either declared incorrectly in the input statement, or it is referenced incorrectly in the module statement.

What Next

Correct one of the errors.

SVR-32

(error) Range of %s port '%s' (%d:%d) does not cover\n \tthe range required by the module statement (%d:%d)\n \tat line %d in '%s'.

Description

A port has been declared in an input/output/inout statement as a range, but the range was inadequate to cover the range required by references to it from the module statement. In this example:

```
module test ({a, b[2:1]}, b[0], z);
input [1:0] b;
```

the module statement requires a range of 2:0, but the input statement declares 1:0. Either the module statement or the input statement is incorrect.

What Next

Correct one of the errors.

SVR-33

(warning) Port '%s' (%s) has a different direction than\n \tother ports in module formal %d (declared line %d); %s statement\n \tat line %d in '%s'.

Feedback

Description

A port has been declared in an input/output/inout statement, but its usage in the module statement creates a bus with mixed directions. For example:

```
module test ({a, b}, z);
output b, z;
input [1:0] a;
```

Port number 1 of the module statement has both inputs and outputs. The first *output* statement sets the direction as output. When the input statement is processed, this warning will be issued, since 'a' and 'b' are concatenated in the first module port, and they are different directions. The first port in the concatenation defines the direction for the entire bus (in this case, an input).

What Next

Verify that the ports are declared correctly, and consider that the netlist created may not have the port directions that you expect.

SVR-34

(error) Slice direction for '%s' [%d:%d] in module port %d ('%s')\n \tdoes not match declared array direction\n \tat line %d in '%s'.

Description

A port has been declared in an input/output/inout statement as an array with a particular order, like n:0 or 0:n. Its usage in the given port in the module statement is inconsistent with that order. For example:

```
module test ({a[0:1], b}, z);
input [1:0] a;
input b;
output z;
```

Port number 1 of the module statement references a[0:1], but 'a' is declared 1:0. Either the module statement or the input statement is incorrect.

What Next

Correct one of the errors.

SVR-35

(error) Port wire '%s' was never declared in an input/output/inout\n \tstatement in module %s in file %s.

Feedback

Description

A port in the module statement references a wire which was never declared in an input/output/inout statement. For example:

```
module test ({a[0:1], b}, z);
input [1:0] a;
output z;
```

Port number 1 of the module statement references 'b', but 'b' was never declared. Either the module statement or the input statement is incorrect.

What Next

Correct one of the errors.

SVR-37

(warning) Port ‘%s’ at Port number %d of module '%s' was renamed to '%s'\n\tat line %d in '%s'.

Description

A port has been found in the module terminal list which needs to be renamed. Ports will be renamed if they are explictly repeated, or if they are a single bit of a bus. For example, in this module statement:

```
module test (a, b[0], a, {a,b});
```

The first port will be named 'a'. The second port will be renamed Port2. The third port will be renamed Port3 because 'a' is already in use. Similarly, the fourth port will be renamed Port4, again because 'a' is already in use. In case one of these generated names is already in use, the Verilog reader will continue to append the port number until a free port name is found.

What Next

No action necessary.

SVR-38

(error) You are declaring the direction of a port '%s'\n \twhose direction is already specified. (File: %s Line: %d)

Description

Formality reports this error if a port direction is declared more than once. It is an error if the port re-declared with direction whose direction is already specified.

Feedback

Example:

```
module test (a, b);
input a;
output b;
output a;  //Error
output b;  //Error
```

In above example port 'a' is declared as 'input' port and later re-declared with 'output' direction. Also port 'b' is declared as a 'output' port and re-declared again as 'output' port. Formality will issue an error in each of these cases.

What Next

Verify that the ports are declared correctly and correct the netlist.

SVR-40

(error) Could not open temp file in '%s'

Description

While reading Verilog, it was necessary to create a temporary file, and the file could not be opened. This could be due to file permissions on the directory, incorrect directory, and so on.

What Next

Verify that you have access to the given directory. If necessary, change the directory as directed by the application.

SVR-41

(error) while writing to temp directory '%s':\n \t%s

Description

An error occured while writing to a temporary file in the given directory. This could be due to insufficient space on the disk, or other disk errors.

What Next

Use a different temporary directory.

SVR-42

(warning) %s constant '%s' requires %d bits\n \twhich is too large for width %d. Truncated. \n \tAt line %d in %s.

Feedback

Description

The constant specified is too wide for the given width. A simple example would be specifying 2'h1e which is truncated from 00011110 to 10. Another example would be specifying a decimal number 2535353678882999122 without a width. The default width for decimal is 32 so this would be truncated from the MSB.

SVR-50

(error) %s

Description

A syntax error occurred while parsing the Verilog file during the preprocessor phase. The message specifies where the error appeared and why it was issued.

What Next

Action based on the text of the message.

SVR-51

(error) End of file seen before %s block begun at line %d was ended

Description

During preprocessing, a comment or directive was found which crossed the end of file boundry, indicating it wasn't terminated appropriately. This problem likely involves an unbalanced "/*", which will need a terminating "*/", or an ifdef without a terminating endif.

What Next

For run-on comments, examine the lines immediately after the one specified in the error. Mark the boundry between code and comment with a terminating "*/".

For (preprocessor) directives, its very likely an `ifdef or `else was not completed with an `endif. Determine what code should fit within the `ifdef, and end it with an `endif.

SVR-52

(error) 'include' directive requires a filename enclosed in double quotes\n \t%s

Description

The Verilog preprocessor found a missing or misformed include filename. Here is an example of the correct usage of `include:

`include "myfile.v"

Feedback

What Next

Provide the filename, if missing.

Preface the filename with a double-quote ("), and place another double-quote after the last character in the filename.

SVR-53

(error) Recursive file inclusion detected for file "%s"

Description

While preprocessing the Verilog file, a circular dependency was found in the use of an "`include" directive. This error is issued to prevent a file from including itself in an endless loop. Breaking the need for an include loop will avoid triggering this error.

A file that directly includes itself most likely meant to include another file with a similiar name.

What Next

Examine the need for the nested "`include". Most likely, several files all depend on each other. The dependencies should be split up so that one file does not depend on any of the others. This can be achieved by moving needed code or `defines to one central file. When one file no longer depends on the others, the corresponding `include(s) can be removed from that file. This should break the `include loop and avoid this error.

SVR-54

(error) Unable to open file '%s' included by the 'include'\n \tdirective %s

Description

The Verilog preprocessor was unable to open a file specified in an "`include" directive. This is most likely caused by the file being outside of the search path. This error is also triggered if the file permissions prohibit read access.

What Next

If the file exists in the current directory, ensure that "." is present in the search path.

For files in other directories, add the directory to your search path.

Permissions problems can be ruled out by trying to view the file in an editor. Errors of this variety are not specific to Verilog.

Feedback

SVR-55

(error) Mismatched directive %s

Description

The Verilog preprocessor found a compiler directive used with incorrect coupling. For example, an "`endif" is used without a corresponding "`ifdef" before it.

What Next

Delete the mismatched directive or add the missed one.

SVR-57

(warning) Macro %s is redefined %s

Description

The Verilog preprocess detected a macro redefinition. The same macro name is provided two different definitions, leading to a single macro name having different meanings in separate parts of the file. Although not an error, this is a potentially hard to find and confusing problem.

What Next

If the duplicate macro definition was accidental, provide a different name for one of the usages.

If the duplicate usage is intentional, this warning can be avoided by performing an `undef of the macro name before each duplicate definition.

SVR-58

(error) You are declaring a variable '%s' whose name is already found in the same scope\n \tat line %d in %s

Description

This fatal error occurs when the Verilog Netlist reader encounters a variable name that is already used in that scope. For example:

```
module top(clk, out);
  input clk;
  output out;
  wire a, b;
  GTECH_BUF aaa ( .A(clk), .Z(aaa) );
endmodule
```

Feedback

What Next

Correct the source so that the port, net, instance or variable is not redeclared.

SVR-59

(error) Instantiation '%s' has mixed ordered and named port connections\n \tat line %d in %s

Description

This fatal error occurs when the Verilog Netlist reader encounters a Instantiation with mixed ordered and named port connections. For example:

```
module top (a,b,c,out,out1,out2,out3);
input [1:0] a,b,c;
output out,out1,out2,out3;
and_gate and_instance2 ( {b[0],b[1]},.out(out2));
endmodule
```

What Next

Correct the source so that the Instantiation does not have mixed port connection.

SVR-60

(error) Token beginning with '%s'\n \texceeds maximum allowable length (%d)\n \tat line %d in '%s'.

Description

A token was found which exceeds the maximum allowable length.

What Next

Look for a syntax error, such as missing punctutation, near the line referenced.

SVR-61

(warning) Empty port at Port number %d of module '%s' was renamed to '%s'\n\tat line %d in '%s'.

Description

You receive this warning message when the port list for a module has empty port, with no local name by which to form connections between its body and the instantiation site.

Feedback

Examples

The following legal Verilog statement indicates a module with four ports, the last of which is unconnected. ... module m(a,b,c,); /* Legal, but perhaps not intended */ ...

What Next

This is a warning message only. No action is required on your part.

However, if the unconnected port is not your intention, remove a comma and then run the command again.

SVR-62

(error) Mixed Port declaration style in module '%s'

Description

Verilog module can have port declarations in 'ANSI' and 'non-ANSI' formats. It is illegal to mix both the formats.

Examples

Following example shows illegal use of non-ANSI style port declarations inside module 'myDesign'. ... module myDesign (input a,b, output c); /* ANSI style */ input a, b; /* non-ANSI style: illegal to have port declarations here*/ ... endmodule

What Next

Edit source code to follow one port declaration format.

SVR-63

(error) Type mismatch in assignment to supply net at line %d\n \tin %s.

Description

There is a type mismatch b/w supply net in LHS & RHS, which is not supported.

What Next

Correct the error, and re-read the file.

SVR-64

(warning) Size mismatch between port & wire declaration for the port \n \t '%s' at line %d in '%s'. \n

Feedback

Description

SVR throws this warning when a port is defined as a vector and its corresponding wire declaration is a scalar. For example :

```
module test(out);
output [15:0] out;
wire out = 16'b101;     //'out' was declared initially with range [15:0]
endmodule
```

What Next

This is a warning message only. No action is required on your part. However, if the range mismatch is not your intention, modify the RTL & re-read the file.

SVR-65

(warning) Continuous assignment statement present in netlist design '%s'\n \tat line %d in %s.

Description

It is a common situation where assign statements result in a technology-mapped netlist sometimes due to feedthrough paths or two outputs being generated from the same logic where a buffer has not been inserted. Continuous assign statements present in technology-mapped netlist can cause problems in downstream Place and Route tools.

For example :

```
module top(in1,in2,out1,out2,out3,out4);
    input in1, in2;
    output out1,out2,out3,out4;
    wire w1,w2,w3;
    low inst1 (in1,in2,w1,w2);
    assign out1 = w1;         //Warning
    assign out2 = w1;         //Warning
    low inst2 (in1,in2,out1,out2);
    low inst3 (in1,in2,out2,out3);
    low inst4 (in1,in2,out3,out4);
endmodule

module low (in1,in2,o1,o2);
    input in1, in2;
    output o1,o2;

    assign o1 = in1;          //Warning
    assign o2 = in2;          //Warning
endmodule
```

Feedback

What Next

Check if the assign statement is valid.

SVR-66

(warning) Statement at Line %d in '%s'\n \texceeds maximum allowable length (%d).\n \tIncomplete statement will be returned.

Description

A statement was found which exceeds the maximum allowable length.

SVR-67

(warning) The undeclared symbol '%s' is assumed to have default\n \tnet type 'wire' at line %d in %s.

Description

The RHS of an assignment contains an undeclared net. It will be implicitly declared as wire for Verilog 2001 onwards.

Ex: module x (a, z); input a; output z; assign z = q; //q will be implicitly declared as 'wire' endmodule

What Next

Check your design to make sure that you intended an implicit declara- tion for this symbol. If not, add an explicit declaration.

SW

SW-001

(Information) STOPWATCH has started. Output will be written to '%s'.

Description

Collection of data for the generation of runtime and memory usage log has started. Performance reports will be written to the given directory.

SW-002

(Error) Stopwatch is currently active in %s.

Feedback

Description

Stopwatch has already been activated.

What Next

To disable Stopwatch, the command pt_stopwatch -stop can be used.

SW-003

(Error) Stopwatch is not currently active.

Description

Stopwatch has not been activated.

What Next

To start Stopwatch, use the command pt_stopwatch -start.

THERM

THERM-400

(error) Temperature query at point {%g %g} outside the die %s boundary %s.

Description

This error indicates that the point for temperature query is outside die boundary.

What Next

Provide correct point which is inside the die boundary.

THERM-401

(error) Die %s does not exist in the current thermal result.

Description

This error indicates that the die does not exist in the currently opened thermal result. This could happen either there is no thermal result loaded into memory, or the opened thermal result does not contain the die. For the second case, thermal analysis may be done on a 3DIC system which consists of several dies. Once the thermal analysis finishes, the thermal result stores temperature for all dies in the analysis.

What Next

Use command open_thermal_result to open the thermal result which consists the relevant die.

THERM-402

(error) Layer %s of die %s does not exist in the current thermal result.

Description

This error indicates that the layer does not exist in the currently opened thermal result. This could happen either there is no thermal result loaded into memory, or the opened thermal result does not contain the layer, or the layer name is incorrect.

What Next

Use command open_thermal_result to open the thermal result which consists the relevant die.

THERM-403

(error) Thermal result %s does not exist in the thermal database.

Description

This error indicates that the thermal result to be loaded does not exist in the thermal database pointed by the option set_thermal_options -database.

What Next

Use command list_thermal_results to list all available results in the pointed thermal database, then provide correct thermal result name for command open_thermal_result.

THERM-404

(error) Thermal result is not ready for query due to %s.

Description

This error indicates that there is no thermal result ready for query.

What Next

Use command open_thermal_result to open the thermal result and load to memory so it is ready for query. Make sure the thermal map name specified in the option -thermal_map is consistent between open_thermal_result and query_thermal_result.

Feedback

THERM-405

(error) Fail to open thermal result %s due to %s.

Description

This error indicates that the thermal result may have a missing file or the file is corrupted which caused failure in loading the thermal result.

What Next

Use command list_thermal_results to list all relevant files under the thermal database. In order to successfully load the thermal result, the following files must exist and should not be corrupted: THERMAL_DATABASE/top_block_name/hier.xml, THERMAL_DATABASE/top_block_name/result_name/options.xml, THERMAL_DATABSE/die_block_name/die_inst_name/result_name/grid.result. THERMAL_DATABASE is the thermal database name from the command set_thermal_options -database. top_block_name is the top block name during thermal analysis (default is KELVIN_TOP). result_name is the thermal result name.

The relevant file could be missing because the provided thermal result name or top block name does not exist in the thermal database. If this is the case, providing a correct result name and/or top block will resolve the issue.

THERM-406

(error) Thermal result with map name %s does not exist in the current thermal result.

Description

This error indicates that the die does not exist in the currently opened thermal result. This could happen either there is no thermal result loaded into memory, or the opened thermal result does not contain the die. For the second case, thermal analysis may be done on a 3DIC system which consists of several dies. Once the thermal analysis finishes, the thermal result stores temperature for all dies in the analysis.

What Next

Use command open_thermal_result to open the thermal result which consists the relevant die.

TIM

TIM-001

(Error) There are no arcs from pin '%s' to pin '%s' on cell '%s'.

Feedback

Description

No timing arcs exist between these pins of the cell. Therefore, we cannot time between them. We will either report no paths or for unmapped logic, assume 0.

What Next

Fix the library to create the proper timing arcs.

TIM-002

(information) Timing loop detected.

Description

The design contains at least one timing loop. This message is followed by a list of pins on one loop, and then messages indicating which timing arcs are being automatically disabled to break the loop.

What Next

To view all timing loops in your design, use *report_timing -loops*. To manually break loops, use *set_disable_timing*.

TIM-003

(warning) Disabling timing arc between pins '%s' and '%s' on cell '%s'%s

Description

This message is displayed when timing arcs are disabled by tool to break combinational feedback loops. It is not displayed for arcs that are manually disabled with the *set_disable_timing* command.

What Next

If you want to manually break a timing loop, examine the design to see why there is combinational feedback and then choose a different point at which to break the loop. To do this, use the *set_disable_timing* command instead of letting the tool automatically break the loop.

Examples

Warning: Disabling timing arc between pins 'A' and 'Z' on cell 'u10'to break a timing loop (TIM-003)

Feedback

TIM-004

(error) The pin '%s' which is a derived clock pin is either in a loop or is in the fanout of two clock sources

Description

The derived clock pin is either in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network or can you have a derived clock in the fanout of two clock sources.

What Next

If it is a loop, break the loop. If the derived clock is in the fanout of two clock sources, try to isolate it or use internal clocks.

TIM-005

(information) Invalidating all auto-disabled timing arcs.

Description

Some arcs have been enabled, forcing the tool to do loop detection from scratch. Therefore, the tool enables all auto-disabled arcs.

What Next

To view all timing loops in your design, use *check_timing*. To manually break the loops, use *set_disable_timing*.

TIM-006

(error) report_delay_calculation is not enabled for library '%s'.

Description

The delay calculation report shows detailed performance information about library cells. By default, cell delay reporting is disabled. The technology library vendor can enable delay calculation for a library by specifying the following in the *.lib* source:

library_features(report_delay_calculation);

What Next

Contact your library vendor to request a library with this feature enabled.

Feedback

TIM-007

(error) The master clock %s has %d edges in a period. Cannot\n do frequency multiplication.

Description

If the master clock of a generated clock has more than 3 edges in a \n period, you cannot generate a frequency multiplied clock from that master\n clock.

What Next

You can use -edges option to generate the clock.

TIM-008

(error) The generated clock '%s' is in the fanout of clock\n source %s.

Description

A generated clock can only be in the fanout of a clock source from which it is generated. Here the generated clock is found to be in the fanout of some other clock source.

What Next

Generate this clock from a clock in whose fanout it is in.

TIM-009

(error) Generated clock '%s' is not in the fanout of its \n master clock.

Description

The generated clock is not in the fanout of the master clock with respect to which it has been defined. A generated clock must be in the fanout of its master clock.

What Next

Please check the design and redefine the generated clock to be in the fanout of its master clock.

TIM-010

(warning) The generated clock '%s' has not been expanded,\n \tplease create its master clock.

Feedback

Description

A generated clock will not expand if the master clock from which it is generated has not been created.

What Next

Please create the master of the generated clock.

TIM-011

(error) The following generated clocks '%s' form a loop.

Description

The generated clock listed are defined in a loop. A loop of generated clocks is formed in that there is a circular dependency of generated clock to master clock.

For example, if A and B are generated clocks, and A is generated from B, and B is generated from A, there is a circular dependency.

What Next

Remove cirular dependency in the generated clock sources.

TIM-012

(error) The master of the generated clock '%s' is not \n connected to any clock source.

Description

The master clock of a generated clock must be either a clock source, or must be connected to a clock source. If it is neither, it is an error.

What Next

Make sure that the master source from which the clock is generated is a clock source or is connected to a clock source.

TIM-013

(information) Found %d generated clock master pins that are not connected to clock sources.

Description

It gives a summary of the number of generated clock master pins that are not connected to clock sources.

Feedback

What Next

For a more detailed description of which generated clock master pins are not connected to any source, do check_timing -with -verbose option.

TIM-014

(information) Found %d loops in the generated clock network.

Description

This message gives a summary of the number of loops in the generated clock network. If there is a circular dependency of generated clock sources and its master, there will be a loop in the generated clock network.

What Next

To get a more detailed description of where the generated clock loops are, use check_timing -verbose.

TIM-015

(Error) The -edges spec of generated clock '%s' has edge number\n \tless than 1, the edge number should be from 1 up.

Description

The -edge specification in creat_generated_clock command should use edge number of the master clock which should be from 1 up. Zero or negative number are not allowed.

What Next

Change your -edge spec in create_generated_clock coommand.

TIM-016

(Error) In the -edge specification of create_generated_clock\n \t'%s', the edge numbers must be in increasing order.

Description

In the -edge specification of a create_generated_clock command, the edge numbers specified must be in increasing order.

What Next

Check the -edge spec in create_generated_clock command and edge numbers increasing.

Feedback

TIM-017

(warning) The master source of the generated clock '%s' is not known. Ignoring generated clock '%s'.

Description

You receive this warning because you did not specify the master clock source of the named generated clock. The master clock of a generated clock must be a specified clock source or be connected to a clock source. Otherwise, this error occurs.

What Next

Make sure that the master source from which the clock is generated is a clock source or is connected to a clock source. See the man page for the *create_generated_clock* command.

See Also

- create_generated_clock

TIM-018

(warning) The source of the generated clock '%s' is not known. Ignoring generated_clock '%s'.

Description

You receive this warning because you did not specify the source of a generated clock. The source of a generated clock can be a list of ports or pins.

What Next

Make sure that the generated clock has a source object. See the man page for the *create_generated_clock* command.

See Also

- create_generated_clock

TIM-019

(warning) Ignoring incorrectly specified library generated_clock '%s' in library cell '%s/%s'.

Description

You receive this warning because the library generated clock description does not have complete specification for creating the derived waveform. A generated_clock must have

Feedback

a 'master_pin', source 'clock_pin', and specification for 'divide_by' or 'multiply_by' or 'edge_spec'.

What Next

Fix the description in the library to completely specify the generated_clock.

See Also

- create_generated_clock

TIM-020

(Error) '%s' is not a legal value for '%s'. The value defaults to '%s'.

Description

You have specified an invalid value for the variable. Therefore, the default value described will be used.

What Next

If you do not want the default value, please specify a valid value for this variable.

TIM-021

(warning) The generated clock '%s' is being removed because the pin '%s' has been deleted and the clock no longer has a %s.

Description

Generated clocks require a master_pin and at least one clock source. If either of these is deleted, then the generated clock is deleted as well.

What Next

Create a new generated clock with the same name using remaining pins.

See Also

- create_generated_clock
- remove_cell

TIM-022

(warning) Since mcpr is off, we can only create the clock %s for either true or inverted sense.

Feedback

Description

During clock propagation, a non unate sense was seen, thereby resulting in both true and inverted senses reaching the sub-block clock port. However, since mcpr is off, clocks can be created for only one of these two senses. Hence timing analysis on the sub-block may not be consistent with the top block.

What Next

Enable mcpr in order to see clocks being created for both true and inverted senses in the sub-block.

TIM-023

(warning) Since timing_non_unate_clock_compatibility is on, we can only propagate either true or inverted sense for clock %s.

Description

During clock propagation, a non unate sense was seen from a clock source, thereby resulting in both true and inverted senses reaching its fanout. However, since timing_non_unate_clock_compatibility is on, clocks can be created for only one of these two senses. Hence timing analysis on the sub-block may not be consistent with the top block.

What Next

Set timing_non_unate_clock_compatibility to false to ensure that both clocks are propagated and also enable multiple clocks per register to ensure that both clocks are created on the sub-block.

See Also

- TIM-022

TIM-024

(information) Using CCS timing libraries.

Description

This message is produced if any libraries containing CCS timing information are used. It is only produced once per session when the first ccs timing library is read.

What Next

No action is needed. This information may be helpful when determings whether a library contains ccs timing data.

Feedback

TIM-025

(information) Using CCS timing info.

Description

This message is produced if any CCS delay information is used. It is only produced once per session when the first cell with CCS timing is loaded for delay calculation.

What Next

No action is needed. This information may be helpful when examining delay correlation issues.

TIM-026

(information) Using CCS timing information.

Description

This message occurs when the tool uses any Composite Current Source (CCS) delay information. It is issued only once per session, when the first cell with CCS timing is loaded for delay calculation.

What Next

No action is needed. This information might be helpful when examining delay correlation issues.

TIM-027

(Warning) Specifying large number of endpoints (%d) can cause long runtime and increased memory usage.

Description

This message occurs when the user tries to set a large value for the *-num_endpoints* option of the *set_fast_pba_analysis_options* command. Specifying a large number of endpoints would cause the tool to search, and generate margins, for a large number of paths. This can significantly increase the runtime and memory usage for both timing analysis and optimization.

What Next

Set the value to a smaller number to reduce runtime and memory usage.

Feedback

TIM-035

(information) Using CCS timing based waveform propagation.

Description

This message is produced if any CCS timing based waveform propagation is used. It is only produced once per session when the first cell is calculated using CCS timing based waveform propagation for delay calculation.

What Next

No action is needed. This information may be helpful when examining delay correlation issues.

TIM-036

(information) Using CCS noise based waveform propagation.

Description

This message is produced if any CCS noise based waveform propagation is used. It is only produced once per session when the first cell is calculated using CCS noise based waveform propagation for delay calculation.

What Next

No action is needed. This information may be helpful when examining delay correlation issues.

TIM-037

(warning) No CCS noise info found in the design. Waveform propagation will not be used.

Description

This message is produced if there is no CCS noise info found when CCS noise based waveform propagation is enabled. It is only produced once per session.

What Next

You may have to add the CCS noise libraries into the design.

TIM-052

(warning) A non-unate path in clock network for clock '%s'\n from pin '%s' is detected.

Feedback

Description

The clock tree for the specified clock contains non-unate paths, which means that the sense of the signal reaching the clock pin of a sequential device could be either the same or inverted with respect to the original clock source. This could be caused by the presence of an XOR gate in the clock path, for example. By default, timing analysis considers the worst possible arrival times of both positive and negative unate clock edges.

What Next

If you do not want both the inverted and non-inverted clock waveforms to reach the clock pin of a sequential device, use the *set_clock_sense* command to explicitly specify the sense of the signal reaching the clock pin, either positive or negative unate, with respect to the clock source.

TIM-97

(Warning) Overriding result from previous set_min_library command on library '%s'.

Description

The *set_min_library* command

What Next

Consider whether this is correct.

TIM-98

(Error) Minimum version must be a different library.

Description

The *set_min_library* command was used to set the minimum version of a library to be the same as the maximum version. This is not allowed.

What Next

Enter the correct name of the minimum library, or use the '-none' option to revert to using the same library for both minimum and maximum analysis.

TIM-099

(Information) There are %d clock pins driven by multiple clocks, and some of them are driven by up-to %d clocks.

Feedback

Description

timing_enable_multiple_clocks_per_reg is TRUE, and all clocks reaching the register are cost-ed simultaneously. Concurrent analysis of multiple clocks can result in significant runtime increase due to increased timing complexity. To improve runtime, the interactions between multiple clocks should be analyzed and *set_false_path* be used to remove invalid interactions between mutually exclusive clocks or use *set_clock_groups* to specify logically exclusive clocks.

What Next

Analyze interaction between clock domains due to multiple clocks per register and use *set_false_path* or *set_clock_groups* to improve runtime. If concurrent analysis of multiple clocks per register is not required then set *timing_enable_multiple_clocks_per_reg* to FALSE or use *set_case_analysis* or *set_disable_timing* to select the clocks for driving the register.

TIM-100

(error) Unable to obtain a DC-Expert license.

Description

Timing commands such as *report_timing* or *highlight_path* require that a DC-Expert key, other appropriate technology key, or both be checked out.

What Next

To determine who is using the DC-Expert, use the *license_users* command. Should problems occur with the license server, contact your system administrator.

TIM-101

(error) The '%s' command is not supported in dt_shell.

Description

This error occurs when a valid Design Compiler command is used, but the command is not supported in *dt_shell*, the timing analysis user interface. Commands such as *compile* are supported only in *dc_shell*, and are ignored in *dt_shell*.

What Next

If you need to use the command, use the *dc_shell* program instead of *dt_shell*.

Feedback

TIM-102

(Error) Ultra license is required for true path reporting.

Description

The *-justify* and *-true* options of *report_timing* require an Ultra license.

TIM-103

(Warning) Reference %s contains internal pins with clock attribute.

Description

The reference contains internal/generated clocks on some internal pins which are not accessible to user to create clocks.

What Next

In order to create a clock on internal pins, use *access_internal_pins*.

TIM-104

(Warning) Worst timing paths might not be returned.

Description

Design Compiler static timing verifier is optimized for finding the longest paths (max delay) and the shortest paths (min delay) in the design. The timing verifier cannot always efficiently compute the longest path in the design, which is shorter than a given amount or the shortest path in the design, which is longer than a given amount. This warning indicates that the current *report_timing* command has made such a request that cannot be satisifed efficiently.

In this case, *report_timing* uses the -nworst option to limit its search for paths meeting the -greater or -lesser criteria. There is no guarantee that the paths returned will be the worst ones in the design that meet the criteria specified in the *report_timing* command. In fact, it is possible that no paths will be returned even though a path meeting the report_timing criteria does exist in the design.

What Next

Increasing the number of paths to return using the -nworst option of *report_timing* increases the likelihood that the worst paths will be found. However, increasing this value also increases the memory and runtime needed by *report_timing*.

Feedback

TIM-105

(Information) Converting time units for library '%s' since those in library '%s' differ.

Description

The time units specified in the first library differ from those in the second library. The second library is Design Compiler's "main" library and determines DC's default time units. DC reports use these units and all time values annotated on the design (using *create_clock*, *set_input_delay*, and so on.) are assumed to be in these units.

The informational message notifies you that Design Compiler is handling conversion of units so that delay calculation using cells in the first library use time values in its native units.

Design Compiler's "main" library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

What Next

To see the units that are specified for a library, use the *report_lib* command.

TIM-106

(Information) Converting capacitance units for library '%s' since those in library '%s' differ.

Description

The capacitance units specified in the first library differ from those in the second library. The second library is Design Compiler's "main" library and determines DC's default capacitance units. DC reports will use these units and all capacitance values annotated on the design (using *set_load*) are assumed to be in these units.

The informational message notifies you that Design Compiler is handling conversion of units so that delay calculation using cells in the first library will use capacitance values in its native units.

Design Compiler's "main" library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

What Next

To see the units that are specified for a library, use the *report_lib* command.

Feedback

TIM-107

(Warning) Main library '%s' has no time units specified, but library '%s' does.

Description

Time units were not specified in the first (main) library, but time units were specified in the second library.

Design Compiler uses the main library to determine the default time units. The default time units are used in reports and all time values annotated on the design (using *create_clock*, *set_input_delay*, and so on.) are assumed to be in these units. However, this main library has no time units and as a result DC runs in a "unitless" mode. No time unit conversion is performed. This can result in incorrect analysis if different time units are actually required.

DC's main library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

What Next

To see the units that are specified for a library, use the *report_lib* command.

To change the main library to a different one with units specified, remove the local_link_library attribute on the current design if one is present and put the desired library first in the link_library or link_path variables.

To add units to a unitless library, the library source (.lib) must be modified and the library must be read in using *read_lib*.

TIM-108

(Warning) Main library '%s' has no capacitance units specified, but library '%s' does.

Description

Capacitance units were not specified in the first (main) library, but capacitance units were specified in the second library.

Design Compiler uses the main library to determine the default capacitance units. The default capacitance units are used in reports and all capacitance values annotated on the design (using *set_load*) are assumed to be in these units. However this main library has no capacitance units and as a result DC runs in a "unitless" mode. No capacitance unit conversion is performed. This can result in incorrect analysis if different capacitance units are actually required.

DC's main library is determined as follows: During reporting the main library is the first library in the link path that contains a cell that is used in the design. During optimization the main library is the first target library specified.

What Next

To see the units that are specified for a library, use the *report_lib* command.

To change the main library to a different one with units specified, remove the local_link_library attribute on the current design if one is present and put the desired library first in the link_library or link_path variables.

To add units to a unitless library, the library source (.lib) must be modified and the library must be read in using *read_lib*.

TIM-109

(Warning) Cell '%s' cannot be optimized because it has \ conflicting timing exceptions on pins '%s' and '%s'.

Description

The identified cell has multiple input pins with conflicting point-to-point timing exceptions on them. During optimization this cell is dont_touch'ed to prevent the point-to-point exceptions from being lost if the cell gets remapped to a configuration with fewer input pins. An example of such an optimization is pulling a multiplexer out of a mux'ed flip-flop. In this case, conflicts in timing exceptions could not be accurately resolved in the new, single input configuration.

Commands which create timing exceptions are *set_max_delay*, *set_min_delay*, *set_false_path*, *set_multicycle_path*, and *group_path*.

What Next

To allow optimization to be performed on this cell, set timing exceptions on the cell such that both of the indicated pins have matching timing constraints. To analyze the timing exceptions that currently exist on the design, use the commands *report_timing_requirements* and *report_path_group*.

TIM-110

(Warning) Cell '%s' is being dont_touch'ed because of \ timing constraints on pin '%s'.

Description

The identified cell has timing constraints which cannot always be transferred to another cell during optimization. As a result, the cell is dont_touched to prevent it from being replaced and to prevent the timing constraints from being lost.

Feedback

What Next

To view the timing constraints set on the pin, use *report_timing_requirements*. If the cell is sequential, verify that the library cell has the correct timing arcs.

TIM-111

(warning) Clock port '%s' is assigned input delay relative to clock '%s'.

Description

This issue will be issued when setting an input delay on clock port, and it is not specified relative to the same clock.

What Next

Remove the unneeded input delay value using the *remove_input_delay* command.

See Also

- remove_input_delay

TIM-112

(Information) Input delay ('%s') on clock port '%s' will be added to the clock's propagated skew.

Description

An input delay set on a clock port is interpreted as clock tree delay between the ideal clock source and the input port.

What Next

If you don't want to have the input delay on the clock added to the clock skew, unset the input delay using the *remove_input_delay* command.

TIM-113

(Information) set_input_delay values are added to the propagated clock skew.

Description

When setting input delay on a clock signal, this value is added to the clock network delay when calculating the skew at the clock pins.

Feedback

What Next

If you don't want to have the input delay on the clock added to the clock skew, unset the input delay using the *remove_input_delay* command.

TIM-114

(Warning) File '%s' could not be opened.

Description

You receive this warning message because the log file specified by the *case_analysis_log_file* variable could not be opened. The case analysis information will not be output to a log file.

What Next

Specify a valid file that can be opened by the *case_analysis_log_file* variable.

See Also

- report_timing
- set_case_analysis
- case_analysis_log_file

TIM-120

(Error) Cannot find library file named '%s'.

Description

The file specified cannot be found or is not readable.

What Next

Check to make sure that the filename exists, permissions are set correctly, and the search_path variable contains the directories that should be searched.

TIM-121

(warning) The -locations option of the report_timing command is now obsolete. Use the -physical option instead.

Feedback

Description

You receive this message if you have issued *report_timing -locations*. This message informs you that the *-locations* option is now obsolete and has been replaced by the *-physical* option. *-locations* continues to be supported for backward compatibility.

What Next

Unless you need to use the *-locations* option for backward compatibility, the next time you use *report_timing*, use *-physical* instead of *-locations*.

See Also

- report_timing

TIM-125

(error) The pin '%s', which is a generated clock pin, is either in a loop or is in the fanout of two clock sources.

Description

The generated clock pin is in a loop or is in the fanout of two clock sources. You cannot have loops in the clock network, or can you have a generated clock in the fanout of two clock sources.

What Next

If it is a loop, break the loop. If the generated clock is in the fanout of two clock sources, try to isolate it or use internal clocks instead.

TIM-128

(warning) No controlling value could be found for the clock gating cell '%s' for the clock pin '%s'.

Description

You receive this warning message because you executed the *set_clock_gating_check* command but did not specify a controlling value for the pin of the clock gating cell driven by the clock. Normally, clock gating checks are performed for the interval where the clock does not have the controlling value. If no controlling value can be determined, no clock gating check will be performed.

What Next

Use the *-high* or *-low* option with the *set_clock_gating_check* command to specify the noncontrolling interval for the clock pin.

Feedback

See Also

- set_clock_gating_check

TIM-129

(warning) User specified controlling value is different.

Description

User defined controlling value for the clock gating cell '%s' for the clock pin '%s' conflicts with the one calculated by the tool. But the user specified value takes precedence over the calculated value.

What Next

The clock gating check is performed for the interval of the clock pin depending on the controlling value. See the manual page for the command *set_clock_gating_check* for detailed instructions on using -high and -low options.

TIM-130

(warning) The attribute '%s' is not supported.

Description

You receive this message because the attribute specified in the iming_report_attributes variable is not supported by the *report_timing* command with the *-attributes* option. Currently, only the *dont_touch*, *dont_use*, *map_only*, *ideal_net* and *size_only* attributes are supported.

The *timing_report_attributes* variable is in the system .synopsys_dc.setup file.

What Next

Modify the *timing_report_attributes* variable.

See Also

- report_timing

TIM-131

(warning) There are no specified attributes to report.

Feedback

Description

You receive this message because you used the the *report_timing* command with the *-attributes* option; but, because there was no variable in the *timing_report_attributes* variable, no attributes are printed.

The *timing_report_attributes* variable specifies the attributes to be reported by the *report_timing* command with the *-attributes* option. Currently, only the *dont_touch*, *dont_use*, *map_only*, *ideal_net* and *size_only* attributes are supported.

The *timing_report_attributes* variable is in the system .synopsys_dc.setup file.

What Next

Modify the *timing_report_attributes* variable.

See Also

- report_timing

TIM-133

(warning) Setting clock gating check on multiplexer '%s'.

Description

You receive this warning message because you have executed the *set_clock_gating_check* command and specified a controlling value for a clock for a multiplexer. Generally, clock gating checks ensure that the enable signal does not change during the interval when the clock input has a noncontrolling value.

A multiplexer is a cell that has no controlling value. To perform a clock gating check on a multiplexer, you must specify the noncontrolling interval for the clock. Use the *-high* and *-low* options carefully, as the tool does not perform detailed analysis to determine if the selected signal changes only in the safe intervals.

What Next

Use the *-high* or *-low* option for performing clock gating checks carefully on cells like multiplexers after understanding when it is safe to change the selected signal. There can be situations when there is no interval when it is safe to change the selected signal. Carefully analyze the consequences before using these options on cells like multiplexers.

See Also

- set_clock_gating_check

Feedback

TIM-134

(warning) Design '%s' contains %d high-fanout nets. A fanout number of %d will be used for delay calculations involving these nets.

Description

The design contains high-fanout nets whose delays will be computed using a simplified delay model that assumes a fixed fanout number. The rationale behind this is that delays of high-fanout nets are expensive to compute, but such nets are often unconstrained (as in the case of global reset nets, scan enable nets, and so on). Those high-fanout nets that are constrained should eventually be replaced by buffer trees. In both cases, detailed delay calculations are expensive and unnecessary.

The simplified net delay model is used only when computing data delays. Propagated clock latencies are always computed using the full accuracy net delay model.

What Next

You can control the load pin threshold for high-fanout nets using the *high_fanout_net_threshold* variable. Setting the threshold to 0 (or to a very large number) ensures that no nets will be treated as high-fanout nets. However, you should be aware that forcing fully accurate delay calculations on all nets can significantly increase compilation runtime in some cases.

The pin capacitance for high-fanout nets is computed by multiplying the capacitance specified by the *high_fanout_net_pin_capacitance* variable times the high-fanout threshold.

Examples

Warning: Design 'reg_top' contains 3 high-fanout nets. A fanout number of 1000 will be used for delay calculations involving these nets. (TIM-134)

TIM-135

(Warning) Net '%s' exceeds the high-fanout threshold. Using \ a fanout number of %d to calculate net delay and load.

Description

The named net is classified as a high-fanout net because its fanout number exceeds the threshold specified by the *high_fanout_net_threshold* variable. Delays of high-fanout nets are computed using a simplified delay model that assumes a fixed fanout number. The rationale behind this is that delays of high-fanout nets are expensive to compute, but such nets are often unconstrained (as in the case of global reset nets, scan enable nets, and so on). Those high-fanout nets that are constrained should eventually be replaced by buffer trees. In both cases, detailed delay calculations are expensive and unnecessary.

Feedback

The simplified net delay model is used only when computing data delays. Propagated clock latencies are always computed using the full accuracy net delay model.

What Next

You can control the load pin threshold for high-fanout nets using the *high_fanout_net_threshold* variable. Setting the threshold to 0 (or to a very large number) ensures that no nets will be treated as high-fanout nets. However, you should be aware that forcing fully accurate delay calculations on all nets can significantly increase compilation runtime in some cases.

The pin capacitance for high-fanout nets is computed by multiplying the capacitance specified by the *high_fanout_net_pin_capacitance* variable times the high-fanout threshold.

TIM-140

(warning) Gated clock latch is not created for pin '%s' because pin has a connection to a clock.

Description

You receive this warning because the tool has detected that you set the *set_clock_gating_check* command on a pin that is driven by a clock. Clock-gating checks are normally performed on the enable pins of the clock-gating cell. Setting a clock-gating check on a pin driven by the clock in the clock-gating cell has no effect.

What Next

If you are not sure which pin to set the clock-gating check on, consider setting the check on the clock-gating cell. The clock-gating cell performs clock-gating checks on all the enable pins of the cell. See the man page for the *set_clock_gating_check* command for more detailed information on this command.

See Also

- set_clock_gating_check

TIM-141

(warning) Gated clock latch is not created for cell '%s' on pin '%s' in design '%s'.

Description

You receive this warning because the tool has detected that you set the *set_clock_gating_check* command on a pin that is either a non-input pin or is driven by a clock. Clock-gating checks should be performed on input enable pins of the clock-gating

cell. Setting clock-gating check on the pins driven by the clock in the clock-gating cell has no effect. Similarly, setting clock-gating check on an output pin has no effect.

What Next

If you are not sure which pin to set the clock gating check on, consider setting the check on the clock-gating cell, which will then perform clock-gating checks on all the enable pins of the cell. See the man page for the *set_clock_gating_check* command for detailed information on this command.

See Also

- set_clock_gating_check

TIM-142

(warning) No gated clock latch created for cell '%s'.

Description

You receive this warning because the tool has detected that you set the *set_clock_gating_check* command on a pin that is a non-input pin or is driven by a clock. Clock-gating checks should be performed on input enable pins of the clock-gating cell. Setting a clock-gating check on the pins driven by the clock in the clock-gating cell has no effect. Similarly, setting clock-gating check on an output pin has no effect.

What Next

If you are not sure which pin to set the clock-gating check on, consider setting the check on the clock-gating cell, which will then perform clock-gating checks on all the enable pins of the cell. See the man page for the *set_clock_gating_check* command for more detailed information.

See Also

- set_clock_gating_check

TIM-143

(warning) Converting propagated clock at '%s' to ideal clock.

Description

You receive this warning to let you know that because you set the *set_clock_latency* command on a propagated clock object, that clock object will be changed to ideal.

Feedback

What Next

If you want the clock to be propagated, do *not* specify *set_clock_latency* on the propagated clock object.

TIM-144

(warning) Ideal timing is specified on the non-ideal pin '%s'.

Description

Ideal latency and ideal transition are ignored if they are set on a non-ideal network.

What Next

If the user wants to use ideal latency or ideal transition on a pin object, it must marked as ideal.

TIM-149

(warning) Cannot preserve timing constraints on IO pin '%s' during ungroup.

Description

This warning message occurs when the *ungroup* command cannot move constraints from an IO pin that has more than one driver or more than one receiver. Timing constraints on that pin are not preserved after the ungrouping.

What Next

This is only a warning message. No action is required.

TIM-150

(warning) Cannot preserve timing constraints on pin '%s' during ungroup.

Description

You receive this warning to let you know that the *ungroup* command could not find the named pin and therefore cannot move constraints to that pin.

This warning message reports the situation. The pin might not be connected.

What Next

Verify that you set the constraint on the correct pin. Then invoke the *ungroup* command again.

Feedback

TIM-151

(warning) Cannot preserve the clock at source pin '%s' during ungroup.

Description

This warning lets you know that a clock with a hierarchical source pin cannot be preserved because the source cannot be moved to another pin on the same net. The clock source might not be connected. Or possibly you have defined another clock on the same net.

What Next

Check to see if the clock source is unconnected or if there is another clock defined on the same net. Make any necessary corrections, and invoke the command again.

TIM-152

(warning) Cannot preserve the generated clock source pin '%s' during ungroup.

Description

You receive this warning to let you know that the generated clock with a hierarchical source pin will not be preserved because it is not possible to move the source pin to another pin on the same net.

What Next

The *ungroup* command will automatically remove the generated clock.

TIM-154

(warning) Generated clock '%s' will be lost after ungroup.

Description

You receive this warning to let you know that the tool is not preserving a generated clock with a hierarchical master pin or hierarchical source pin, because it is not possible to move the source pin or the master pin to another pin on the same net.

What Next

The *ungroup* command will automatically remove the generated clock.

TIM-155

(warning) The disable_timing constraint on pin '%s' will be lost after ungroup.

Feedback

Description

You receive this warning to let you know that the disable_timing constraint that is set on a hierarchical pin cannot be preserved because the *ungroup* command cannot find another pin on the same net where the constraint can be set.

What Next

This is a warning only and requires no action on your part.

TIM-156

(warning) Case analysis on pin '%s' will be lost after ungroup.

Description

You receive this warning to let you know that the case-analysis value that you set on the named hierarchical pin cannot be preserved, because the *ungroup* command cannot find another pin in the same net on which to set the constraint.

What Next

This is a warning only and requires no action on your part.

TIM-157

(warning) Generated clock '%s' will be lost after ungroup.

Description

You receive this warning because the named generated clock that has a hierarchical master pin or hierarchical source pin will not be preserved, because it is not possible to move either the source pin or the master pin to another pin on the same net.

What Next

The *ungroup* command will automatically remove the generated clock.

TIM-158

(warning) Input/output delay on pin '%s' will be lost after ungroup.

Description

You receive this warning to let you know that the input delay or output delay that you set on a hierarchical pin will not be preserved because the *ungroup* command could not find another pin in the same net on which to set the constraint.

Feedback

What Next

This is a warning only and requires no action on your part.

TIM-159

(warning) Exception through pin '%s' is lost after ungroup.

Description

You receive this warning to let you know that timing exception through a hierarchical pin will not be preserved after the ungroup process because the *ungroup* command cannot find another pin in the same net on which to set the constraint.

What Next

This is a warning only and requires no action on your part.

TIM-160

(warning) The variable named %s is set to an illegal value (%g) and will be ignored.

Description

This warning message occurs when a variable is set to a value that is not within the range of acceptable values. The variable setting is ignored.

The following shows an example of the warning message.

Warning: The variable named rc_input_threshold_pct_rise is set to an illegal value (150) and will be ignored. (TIM-160)

What Next

This is only a warning message. No action is required.

However, if you do not want the variable value to be ignored, reset the variable to an acceptable value. Refer to the man page for the variable shown in the message to determine the acceptable values. After making your changes, run the command again.

TIM-161

(warning) The variable named %s is set to a very low value (%g).

Description

This warning message occurs when a variable is set to a legal value that is well below the range of values that are normally used. This message warns you to check the variable's value to make sure that it is correct.

The following shows an example of the warning message.

Warning: The variable named rc_input_threshold_pct_rise is set to a very low value (0.50). (TIM-161)

What Next

This is a only a warning message. No action is required.

However, if the value of the variable is not the value you want, reset the variable to the correct value. Refer to the man page for the variable shown in the message to determine the range of values. After making your changes, run the command again.

TIM-162

(warning) The value of variable '%s' (%g) overrides the original value (%g) in library '%s'.

Description

This warning message occurs when you set the named variable because you are overriding a library parameter that is specified by the creator of the library. This is not considered best practice because it can cause inaccurate or incorrect results.

Consult the creator of the library before attempting to override a library parameter.

The following shows an example of the warning message.

Warning: The value of variable 'rc_input_threshold_pct_rise' (80) overrides the original value (50) in library 'cmos_013_comb'. (TIM-162)

What Next

This is a warning message only. If you are sure you want to override the library parameter value, no action is required.

However, to use the value defined in the library, unassign the variable and remove the variable assignment from any scripts. After completing your changes, rerun the command.

TIM-163

(warning) The library named %s specifies a very small trip-point value (%g).

Description

This warning message occurs when the library contains a trip-point value that is legal, but is well below the range of values that are typically used.

The following shows an example of the warning message.

Feedback

Warning: The library named cmos_013_comb specifies a very small trip-point value (0.5). (TIM-163)

What Next

This is a warning message only. No action is required.

However, it is best practice to ask the library creator to check the trip-point values in the library. You can use the *report_lib* command to see the trip-point values in the library.

See Also

- report_lib

TIM-164

(warning) The trip points for the library named %s differ from those in the library named %s.

Description

This warning message occurs when two libraries with different trip-point values are being used. This may result in a loss of timing accuracy when cells from one library are connected to cells of the other library.

The following shows an example of the warning message.

Warning: The trip points for the library named cmos_013_comb differ from those in the library named cmos_013_fflop. (TIM-164)

What Next

This is a warning message only. No action is required.

However, you can check the trip points for a library using the *report_lib* command. It is best practice to use libraries that use the same trip-point values when cells from different libraries will be connected.

See Also

- report_lib

TIM-165

(warning) The library named %s contains an illegal trip-point value (%g) that will be ignored.

Feedback

Description

This warning message occurs when a a library contains an illegal trip-point specification that is ignored.

The following shows an example of the warning message.

Warning: The library named cmos_013_comb contains an illegal trip-point value (150) that will be ignored. (TIM-165)

What Next

This is only a warning message. No action is required.

However, you can check the trip points for a library using the *report_lib* command. Inform the library creator of the illegal trip-point value, because improper trip-point specifications may cause inaccurate timing results.

See Also

- report_lib

TIM-166

(error) For the library named %s, the lower %s slew trip point (%g) is larger than the upper trip point (%g). The trip points will be interchanged.

Description

This error message occurs when a lower slew trip point is set to a larger value than the corresponding upper trip point. This is not allowed. The upper trip point must always be larger than the lower trip point (even for falling transitions).

The following shows an example of the error message.

Error: For the library named cmos_013_comb, the lower fall slew trip point (75) is larger than the upper trip point (25). The trip points will be interchanged. (TIM-166)

What Next

Check the trip points for the library using the *report_lib* command.

- If the incorrect values are specified in the library, inform the library creator.
- If the trip-point values are not coming from the library, they were set using variables such as *rc_slew_lower_threshold_pct_rise*. In this case, reset the variables to the correct values.

Feedback

See Also

- report_lib

TIM-167

(error) For the library named %s, the lower %s slew trip point (%g) is the same as the upper trip point. The default values of %g and %g will be used.

Description

This error message occurs when a lower slew trip point is set to the corresponding upper trip point of the same value. This is not allowed because it makes all transition times zero.

The following shows an example of the error message.

Error: For the library named cmos_013_comb, the lower fall slew trip point (75) is the same as the upper trip point. The default values of 20 and 80 will be used. (TIM-167)

What Next

Check the trip points for the library using the *report_lib* command.

- If the incorrect values were specified in the library, inform the library creator.
- If the trip-point values are not coming from the library, they were set using variables such as *rc_slew_lower_threshold_pct_rise*. In this case reset the variables to the correct values.

See Also

- report_lib

TIM-168

(information) There are logic constants set for unused pins.

Description

This information message occurs when there are unused (hanging) pins in the design. The tool binds the unused pins to logic constants that may affect case analysis, arc disabling, and report_timing.

What Next

This is only an information message. No action is required.

However, the tool ignores this setting if you set the *dont_bind_unused_pins_to_logic_constant* variable to true.

Feedback

TIM-169

(warning) Clock '%s' does not have edge values monotonically increasing, so waveform is adjusted.

Description

You receive this warning to let you know that the edge values of the clock is not in a monotonically increasing sequence. The reason that this is a TIM message instead of an UID message suggests that the waveform inferred from input delays could be violating the condition. In order to proceed with the analysis, the waveform edge values of the clock are adjusted.

What Next

Clearly define the clock waveform to meet the conditions, or adjust external delays that could have led to this violation.

See Also

- create_clock

TIM-170

(warning) Restored the timing arcs disabled by loop breaking.

Description

When the timing graph is changed, the internally disabled timing arcs for loop breaking is restored.

What Next

Exam the timing arcs to be sure they are correct for loop breaking.

See Also

- set_disable_timing

TIM-171

(warning) The hierarchical cell named %s that is being ungrouped has derate. This derate will be set on the lower level leaf cells if the leaf cell does not have a derate itself. This may cause timing inconsistency before and after ungrouping.

Feedback

Description

This warning message occurs when ungrouping a cell that has derate. The cell's derate factors are set on the lower level cells if the lower level cells do not have their own derate factors. Because the derate factor of library cells has has higher priority than hierarchical cells, this setting may cause the derate factors used in delay calculation to change after ungrouping.

What Next

This is only a warning message. No action is required.

However, if this is not the result you intended, use the *set_timing_derate* command to change the derate factors.

See Also

- set_timing_derate

TIM-172

(error) For library pin %s, the lower %s slew trip point (%g) is larger than the upper trip point (%g). The trip points will be interchanged.

Description

This error message occurs when a lower slew trip point is set to a larger value than the corresponding upper trip point. This is not allowed. The upper trip point must be larger than the lower trip point (even for falling transitions).

The following shows an example error message:

error: For library pin clk, the lower fall slew trip point (75) is larger than the upper trip point (25). The trip points will be interchanged. (TIM-172)

What Next

Check the trip points for the library pin. If the incorrect values are specified in the library, inform the library creator.

TIM-173

(error) For library pin %s, the lower %s slew trip point (%g) is the same as the upper trip point. The default values of %g and %g will be used.

Feedback

Description

This error message occurs when a lower slew trip point is set to the same value corresponding upper trip point. This is not allowed, because it makes all transition times zero.

The following shows an example error message:

error: For library pin clk, the lower fall slew trip point (75) is the same as the upper trip point. The default values of 20 and 80 will be used. (TIM-173)

What Next

Check the trip points for the library pin. If the incorrect values are specified in the library, inform the library creator.

TIM-174

(warning) For library pin %s, the lower %s slew trip point or the upper trip point is not set. The default values of %g and %g will be used.

Description

This warning message occurs when a lower slew trip point or the corresponding upper trip point is not set to any value. The default values will be used in this situation.

What Next

This is only a warning message. No action is required.

TIM-175

(Warning) Breaking the timing path through pin '%s'\n \tdue to user timing constraints.

Description

Some timing constraint commands can cause timing paths to be broken when placed on pins which are not normal timing startpoints or endpoints. Examples include *set_max_delay*, *set_min_delay*, *set_multicycle_path*, *set_false_path*, and *group_path*. Paths are broken by making the pin an endpoint for all timing paths leading to the pin. In addition, the pin becomes a startpoint for all timing paths going out of the pin.

What Next

To avoid broken timing paths, try to set timing exceptions on ports and register clock or data input pins. For other types of pins, use -through pin exceptions rather than -from and -to pin exceptions. The major difference between the -from, -to, and -through options is that -from causes the path to be broken if the pin is not a normal timing startpoint, -to

Feedback

causes the path to be broken if the pin is not a normal timing endpoint, and -through does not break paths.

See Also

- set_max_delay
- set_min_delay
- set_false_path
- group_path

TIM-176

(information) Timer is not in zero interconnect delay mode.

Description

This information message advises you that the timer is no longer working in the zero interconnect delay mode. The timer is in normal mode so the net wire capacitance is restored from the back annotation or from the wire load model.

What Next

This is an informational message only. No action is required.

However, if the result is not what you intended, you can enable zero interconnect delay mode by setting *set_zero_interconnect_delay_mode* to *true*.

TIM-177

(warning) Timer is in zero interconnect delay mode.

Description

This warning message occurs when the timer is working in the zero interconnect delay mode. The net wire capacitance is 0 when calculating the delay, for example, Cw = 0.

When you run the *set_zero_interconnect_delay_mode* command without specifying *true* or *false*, zero interconnect delay mode is enabled by default.

After you set the interconnect delay mode to zero, the *report_timing*, *report_constraint*, and all commands that use the wire delay reflect the zero Cw. This also affects optimization.

What Next

This is only a warning message. No action is required.

Feedback

However, if the result is not what you intended, it is considered best practice to set *set_zero_interconnect_delay_mode* to *false* before the timing optimization. Otherwise, the optimization does not see the interconnect delay, even if the design has the wire load model specified, the design is back annotated, or the design is routed.

What Next

```
get_zero_interconnect_delay_mode(2)
set_zero_interconnect_delay_mode(2)
```

TIM-178

(warning) This '%s' constraint is no longer applicable to any path.

Description

This warning message occurs when pins or clocks have been removed from the timing path constraint to the extent that the constraint cannot be applied. For example, a false path from {A B} to {C D} is dropped if both C and D have been removed from the design.

This message is also issued when an ungroup is performed by first changing the current_design to a subdesign, and then back to top. The timing constraints set from the top level design might not apply after the ungroup and can be lost.

What Next

This is only a warning message. No action is required.

However, if the result is not what you expected, check the constraint file for any redundancies. If the message occurs because the ungroup was performed from a subdesign, run the *ungroup* command from the top level using the *-all_instances* option, if needed.

TIM-179

(warning) '%s' constraint made a reference '%s %s' which no longer exists.

Description

This warning message occurs when the pin or object specified in the timing constraint has been removed as the result of an optimization or constraint propagation. This can cause the constraint to no longer apply to the design.

This message is also issued when an ungroup is performed by first changing the current_design to a subdesign, and then back to top. The timing constraints set from the top level design might not apply after the ungroup and can be lost.

Feedback

What Next

This is only a warning message. No action is required.

However, if the result is not what you expected, check the constraint file for any redundancies. If the message occurs because the ungroup was performed from a subdesign, run the *ungroup* command from the top level using the *-all_instances* option, if needed.

TIM-180

(information) Total %d nets in the design, %d nets have timing window.

Description

This message gives a summary of the number of nets in the design and how many of them have timing windows. This message is issued during timing update when SI analysis is enabled and timing windows are considered in SI analysis.

What Next

This is an informational message only. No action is required.

TIM-181

(Error) Relationship between clocks %s and %s is already defined to be %s by group %s

Description

The clock pair already has a relationship defined by a set_clock_groups command prior to the current set_clock_groups command.

What Next

If you want to change the clock relationship, remove the exisiting relationship by using the *remove_clock_groups* command. You can use *report_clock* command with -groups *option to see more details.*

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

Feedback

TIM-182

(Warning) Clock group %s has all design clocks in one group.

Description

The current set_clock_groups command specifies all the clocks in the same group. This is a valid setting if you plan to add more clocks. This command serves no prupose otherwise.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

TIM-183

(Warning) False path got overridden by set_clock_groups.

Description

The current set_clock_groups command overrode an existing false path between the specified clocks. The clocks are from different groups of set_clock_groups command.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

TIM-184

(Error) Clock group settings for %s and %s conflict with previously set clock group settings.

Description

This error message occurs when a set_clock_groups command conflicts with a previous set_clock_groups command. For example, if a previous command has specified a false path between a pair of asynchronous clocks, then a new command tries to allow paths between the pair of clocks, you will see this error message. Use report_clock -groups to see all clock groups. Remove the existing clock group if you want to change the clock group settings for the clock pair.

Feedback

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

TIM-185

(Error) Clock group %s not found.

Description

The error occurs if the clock group of given name is not found by remove_clock_group command. Use report_clock with -groups option to list all clock groups.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

TIM-186

(Error) Clock group %s already exists.

Description

The error occurs if the clock group of given name and given type already exists. Use report_clock with -groups option to list all clock groups.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

TIM-187

(Error) Clock group setting clash with false path settings of group %s (%s).

Feedback

Description

The current set_clock_groups command conflicts with an earlier set_clock_groups setting issued for the group of clocks. This message usually occurs when all clocks in the design have been specified in the same group and their false path settings clash with another set_clock_groups command. For example, a previous set_clock_groups command specifies false path but the current command allows timing paths. Use report_clock -groups to see all clock groups. Remove the existing clock group if you want to change the clock group settings for the set of clocks.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

TIM-188

(Error) Clock group %s already defines the %s relationship for given clocks.

Description

This error message occurs when a set_clock_groups command tries to redefine a relationship for the set of clocks. Use remove_clock_groups remove the existing clock group if you want to change the clock group settings. Use report_clock -groups to report all clock groups.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

TIM-189

(warning) there are conflicting senses converging for clock '%s' from pin '%s' in the clock network.

Description

The clock tree for the specified clock contains paths that have conflicting senses merging. This clock will not be propagated forward starting from this pin.

Feedback

What Next

Since there is ambiguity on which sense to choose to propagate, user could use set_clock_sense to pick which sense to propagate for the clock.

TIM-190

(warning) sense defined on pin '%s' cannot be honored for clock '%s'.

Description

The sense defined on the pin is not available and cannot be honored. This happens when the clock senses propagated to this pin doesn't contain the sense user has chosen. The defined sense is ignored and the original senses are propagated forward.

What Next

A feasible clock sense has to be set by set_clock_sense, otherwise the defined sense is ignored.

TIM-191

(warning) Tool does not support AOCV analysis for clock as well as data derates.

Description

In AOCV analysis, we do not support derates on data (only clock analysis is supported). The supplied table only has derates for data path objects as well as clocks.

What Next

Perform analysis using derates on clock objects only.

TIM-192

(error) Tool does not support AOCV analysis for derates on data only.

Description

In AOCV analysis, we do not support derates on data (only clock analysis is supported). The supplied table only has derates for data path objects. Hence we will bail out.

What Next

Perform analysis using derates on clock objects.

Feedback

TIM-193

(info) Generated Clock (%s) has non_unate sense on master source pin.

Description

For a generated clock if the master source pin has a non-unate sense, then by default the tool will only propagate the positive sense waveform from the generated clock source pin to the clock pins. This information will help the user understand which generated clock has non-unate sense on their master source pin.

What Next

The user can create an additional generated clock with a -preinvert option to propagate the negative sense.

TIM-194

(error) Tool does not support AOCV analysis for different voltages.

Description

In AOCV analysis, we do not support analysis for different voltages.

What Next

Do not use tables which have a voltage field.

TIM-196

(warning) Clock group %s already defines the relationship for the given set of clocks.

Description

This warning message occurs when the clock group for the specified set of clocks and type already exists.

What Next

Use the *report_clock* command with the *-groups* option to list all clock groups. Rerun the command with either a new clock group, or a new set of clocks.

See Also

- remove_clock_groups
- report_clock
- set_clock_groups

Feedback

TIM-197

(error) Cannot find the definition of mode '%s'.

Description

This error message occurs when user tries to set an invalid mode value to cell, which is not defined in the reference library.

What Next

Use the *report_mode* command to list all modes to look for which mode is you wanted.

TIM-198

(warning) Only keeping depth data for distance: '%f' (row: '%d').

Description

In AOCV analysis, PrimeTime supports both depth and distance data, whereas this tool supports only depth data. *read_aocvm -distance_row* allows you use a 2-D advanced OCV table intended for PrimeTime and specify which row to use in the table. By default, the command uses the most pessimistic derate values found among the rows of the table.

What Next

To specify which row to use in the table, use *read_aocvm -distance_row*.

TIM-199

(warning) The AOCVM library file is used for '%s' operating condition only.

Description

The advanced OCV derate table read by *read_aocvm* applies to the minimum or maximum operating condition only.

What Next

To specify which operating condition is applied for the table, use *read_aocvm*.

TIM-200

(warning) Data Checks from-pin (%s) and to-pin (%s) are the same pin. Ignoring

Feedback

Description

Datacheck from pin and to pin cannot be the same pin. The tool will ingore the data-check constaint in that case.

What Next

Tool will issue a warning message and skip the constaint.

TIM-201

(Error) Generated clock (%s) (%s) is not satisfiable; zero source latency will be used.

Description

This is an error message whenever the clock network traverse can not find a path which satisfies the sense relationship defined by create_generated_clock command.

What Next

Check for the generated clock definition to see if the generated clock is correctly defined. One example is that a divided_by 2 generated clock is driven by a inverter only. In this case, generated clock should be redefined with -invert with -divided_by 1. Another example is a divided_by 2 generated clock with preinverting. If master clock source pin is used as generated clock source pin, the warning message will be issued. In this case, generated clock source pin should be redefined to clock pin of divider.

TIM-202

(Error) The master of the following generated clock is not connected to any clock source.

Description

This error message occurs when check_timing command finds generated clock in the design is not connect to any clock source.

See Also

- check_timing
- timing_check_defaults

TIM-203

(Error) The following generated clocks form a loop.

Feedback

Description

This error message occurs when check_timing command finds generated clocks in the design form a loop. For example, when the source pin of G_CLK1 is the definition point of G_CLK2, meanwhile the source pin of G_CLK2 is the definition point of G_CLK1, the tow generated clocks form a loop.

See Also

- check_timing
- timing_check_defaults

TIM-204

(Warning) The following generated clock has no path to its master clock.

Description

This warning message occurs when check_timing command finds the definition point of generated clock has no path to its master clock. For example, master clock CLK1 defines on point A, and its generated clock GCLK1 defines on B, if there's no path from A to B, the Warning message will be printed out.

What Next

Check the definition point of the generated clock to make sure there is a physical connection to its master clock. However, if the generated clock genuinely has no path to its master, then users can explicitly apply a source latency on the generated clock.

See Also

- check_timing
- timing_check_defaults

TIM-205

(Warning) cross clocks found.

Description

This Warning message occurs when check_timing command finds clock interactions. If a clock launches one or more paths, which are captured by other clocks, it will have an entry in clock crossing report. If all paths between two clocks are false paths or the are exclusive/asynchronous clocks, the path is marked by *. If only part of paths are set as false paths, the path is marked by #.

Feedback

See Also

- check_timing
- timing_check_defaults

TIM-206

(Warning) following data check register reference pins are not driven by clocked signal.

Description

This warning message occurs when check_timing command finds no clocked signal reaches a data check register reference pin.

See Also

- check_timing
- timing_check_defaults

TIM-207

(Warning) following data check register reference pins are driven by multiple clocked signals.

Description

This warning message occurs when check_timing command finds multiple clocked signals reach a data check register reference pin.

See Also

- check_timing
- timing_check_defaults

TIM-208

(Warning) The following input ports have no clock_relative delay specified, a default clock is assumed for these input ports.

Description

This warning message occurs when check_timing command finds no clock related delay specified on an input port, where it propagates to a clocked latch or output port. Note that

Feedback

with timing_input_port_default_clock set to 'true', a default clock will be assumed for the input port. Otherwise it will not be clocked, and the paths are unconstrained.

What Next

Please manually set the input delay for the listed ports by using the command set_input_delay with -clock option.

See Also

- check_timing
- timing_check_defaults
- set_input_delay

TIM-209

(Warning) timing loops detected.

Description

This warning message occurs when the *check_timing* command finds combinational feedback loops.

What Next

The preferred way to break loops is to explicitly use the *set_disable_timing* command to determine where to break the loop. Otherwise, the tool automatically breaks the loop, and this might not result in the intended functionality.

See Also

- check_timing
- set_disable_timing
- timing_check_defaults

TIM-210

(Warning) there are %d input ports without driving cell specified.

Description

This warning message occurs when check_timing command finds no driving cell specified on an input port. In such case, the accuracy of delay calculation could be impacted, as a default strong driver is assumed in absence of driving cell definition. Especially, in presence of crosstalk, a port with no driving cell could act as a strong aggressor which

Feedback

could lead to significant amount of pessimism in the analysis. Also, a port with no driving cell could act as a string victim, which could underestimate the crosstalk effect. Command set_driving_cell could be used to specify a library cell or pin to drive ports.

See Also

- check_timing
- timing_check_defaults

TIM-211

(Warning) there are %d ideal clocks.

Description

This warning message occurs when check_timing command finds ideal clocks. Generally, all clocks should be propagated so that the clock network timing is accurately calculated. Especially, in presence of crosstalk, the delay changes induced by other nets on the clock network will not be reflected in the calculated slacks in the design. Command set_propagated_clock could be used to define clock as propagated.

See Also

- check_timing
- timing_check_defaults

TIM-212

(Warning) there are %d input ports that only have partial input delay specified.

Description

This warning message occurs when check_timing command finds partial input delay specified on an input port. This happens when set_input_delay -min is appliedon a port to set the min input delay with respect to a clock, however no set_input_delay -max is applied to that port to specify the max delay, or vice versa. As a result, some paths starting from the port with partially defined input delay may become unconstrained and some potential violations could be missed. Command set_input_delay could be used to set both min and max delay on the port.

See Also

- check_timing
- timing_check_defaults

Feedback

TIM-213

(warning) the specific arc is in clock path, report_delay_calculation result may not match with timing report or clock skew report for this arc.

Description

This warning message occurs when both from pin and to pin are in clock network. In clock skew/latency calculation, tool use the slew from clock propagation path to calculate delay result. While in report_delay_calculation command, tool use the worst slew to calculate delay. This may cause different delay results.

See Also

- report_delay_calculation

TIM-214

(Warning) there are %d nets without driver pins.

Description

This warning message occurs when check_timing command finds nets without driver pins.

See Also

- check_timing
- timing_check_defaults

TIM-215

(Warning) there are %d nets without timing arcs on driver pins.

Description

This warning message occurs when check_timing command finds no timing arcs defined on the driver pins of the net.

See Also

- check_timing
- timing_check_defaults

Feedback

TIM-216

(Warning) The following input ports have no clock_relative delay specified, the command set_input_delay without -clock option will be ignored.

Description

This warning message occurs when check_timing command finds no clock related delay specified on an input port, where it propagates to a clocked latch or output port. Note that with timing_input_port_default_clock set to 'false', the command set_input_delay without -clock option will be ignored, and the paths are unconstrained. Otherwise a default clock will be assumed for the input port.

What Next

Please manually set the input delay for the listed ports by using the command set_input_delay with -clock option.

See Also

- check_timing
- timing_check_defaults
- set_input_delay

TIM-219

(information) Freezing clock timing with %f percentage of clock nets routed and extracted.

Description

In clock arnoldi flow, during psynopt, at this point, we will freeze the clock timing numbers. In order to unfreeze, clocks must be routed after psynopt, followed by an extraction, to regenerate the clock routes.

TIM-220

(Warning) Verbose reporting of clock network timing is not available in clock_arnoldi mode when clock-routing may be needed. The reporting will revert to non-verbose mode.

Description

This warning message occurs during clock_arnoldi mode, and the user is trying to execute a command that requires a recompute of the clock network. Such a recompute is not possible until when clock network is re-routed and extracted.

Feedback

What Next

Route all the clocks, and perform extraction in order to recompute and report detailed clock network timing.

TIM-221

(warning) Command %s being executed when the clock network needs re-routing.

Description

This warning message occurs when the user is trying to execute a command that requires a recompute of the clock network at a time when clocks still need re-routing.

What Next

Route all the clocks, and perform extraction first, and then reapply the command.

TIM-222

(information) Resetting clock timing frozen to FALSE since percentage of routed and extracted clock nets is %f and threshold expected is %f.

Description

Upon rerouting a very high percentage of the clock nets, we can reset "clock_timing_frozen" flag, thereby allowing recompute of the clock network delays. This ensures that the numbers computed using arnoldi delay method are accurate.

TIM-223

(warning) Cannot reset clock timing frozen to FALSE since percentage of routed and extracted clock nets is %f and threshold expected is %f.

Description

This warning message occurs when a high percentage of clock routes are not routed, as detected during extraction. Hence, during clock arnoldi flow, we cannot reset clock_timing_frozen flag. Clock skews will continue to remain frozen.

What Next

Reroute all the clocks, and perform extraction to clear the clock_timing_frozen flag.

TIM-224

(warning) Cannot freeze clock timing since none of the clock nets are routed/extracted.

Feedback

Description

This warning message occurs when a high percentage of clock routes are not routed, as detected during extraction. Hence, during clock arnoldi flow, we cannot set clock_timing_frozen flag. Clock network skews and source latencies will be estimated for the unrouted nets.

What Next

In order to guarantee better accuracy, route all the clocks, and perform extraction, before calling psynopt.

TIM-225

(information) Using frozen clock skews and source latencies.

Description

In clock arnoldi flow, during psynopt, at this point, we will freeze the clock timing numbers. In order to unfreeze, all clocks must be routed after psynopt, followed by an extraction, to regenerate the clock routes.

TIM-226

(information) Saving clock skews and source latencies on layer %s since clock timing is frozen.

Description

In clock arnoldi flow, if the clock timing is frozen, and the latches are being rebuilt, we will save the clock skews and source latencies for all endpoint registers on a per pin, clock, and clock sense basis. Subsequent latch timing will see these saved numbers.

TIM-227

(warning) Clock timing on layer %s will no longer be frozen due to potential changes on the clock network.

Description

In the clock Arnoldi flow, at this point, the tool unfreezes the clock timing numbers. Constraints were added to the clock network or operating conditions/TLUPlus were changed when the clock timing was frozen. Therefore, the clock timing should not be frozen beyond this point, and the tool resets the flag even though the clock network might not be fully routed and extracted.

Feedback

What Next

Route the broken nets in the clock network and perform extraction, before making any such changes.

See Also

- TIM-219
- TIM-222
- TIM-223

TIM-228

(error) Cannot find the table containing frozen latch skews and source latencies.

Description

This error occurs during clock arnoldi flow when clock_timing_frozen flag is true, and we cannot find the frozen clock skew value table for the design.

TIM-229

(error) Could not find entry for latch with %s %s on clock %s with clock sense %d.

Description

This error occurs during the clock Arnoldi flow when the *clock_timing_frozen* attribute is true and the tool cannot find the entry in the table for the <clock,sense> tuple for this pin. If additional constraints were added when the clock timing was frozen, this might cause the entry not to be stored in the table.

What Next

Add additional constraints only after clock timing has been unfrozen (after all clocks are routed and extraction has been performed).

See Also

- TIM-225
- TIM-226
- TIM-230

Feedback

TIM-230

(error) Could not find an entry in the hash for latch with %s %s.

Description

This error occurs during the clock Arnoldi flow when the *clock_timing_frozen* attribute is true and the tool cannot find an entry in the table for this pin. If additional constraints were added when the clock timing was frozen, this might prevent the entry from being stored in the table.

What Next

Add additional constraints only after the clock timing has been unfrozen after all clocks are routed and extraction has been performed.

See Also

- TIM-229
- TIM-230

TIM-231

(warning) Clock skews computed at this point may not be accurate since clock routes are not valid.

Description

This warning message occurs when the user is trying to execute a command that causes a recompute of the clock network phase delays, when clock routes are not valid. Clock skews computed using clock_arnoldi hence may not be accurate

What Next

Route all the clocks, and perform extraction first, and then run this command.

TIM-232

(info) Number of %s routed nets is %d while number of %s nets is %d.

Description

This message tells us the number of clock/all nets in the design and the number of such nets that have a valid route.

Feedback

TIM-233

(warning) Clock network timing may not be up-to-date since only %f percentage of clock nets are routed.

Description

This message is issued when the previous command caused some of the clock nets to be broken, and therefore delays can no longer be computed accurately using the clock Arnoldi flow.

What Next

Route all the clocks and fix the broken nets before performing extraction and timing reporting.

See Also

- TIM-223
- TIM-225

TIM-234

(information) Postroute Elmore delays will be computed using RC annotations.

Description

In elmore flow, if the design is in post route mode, we will remove extraction BA, and compute delays using RC annotations.

TIM-240

(Information) AOCV '%s' analysis is performed in scenario '%s'.

Description

AOCV analysis of given mode is performed.

What Next

To change AOCV analysis mode, use *timing_aocvm_analysis_mode*.

TIM-241

(information) Annotating OCVM table on lib cell %s from %s.

Feedback

Description

The OCVM derate table read by *read_aocvm* is annotated onto the lib cell of given name. If an ellipsis is given, the derate table is annotated onto multiple lib cells.

What Next

Use *report_ocvm* command to check whether OCV tables have been annotated onto the intended objects.

TIM-242

(Warning) No coordinate locations have been defined; AOCVM analysis may be inaccurate.

Description

You have received this message because you have attempted to perform an AOCVM analysis, but no coordinate locations have been defined.

Coordinates locations are used to calculate the systematic component of an AOCVM derate factor.

The tool will continue with the AOCVM analysis and assume the most pessimistic coordinate locations possible.

What Next

AOCVM analysis is intended for post-CTS designs with propagated clocks and CRPR enabled. If you enabled AOCVM distance analysis after the read_aocvm command, the tool does not have AOCVM tables with distance information available (only the worst case distance information was preserved). You need to use read_aocvm to read in your AOCVM tables again.

See Also

- report_timing
- report_aocvm

TIM-243

(Information) POCV Distance '%s' analysis is performed in scenario '%s'.

Description

POCV Distance analysis of given mode is performed.

Feedback

What Next

To change POCV Distance analysis mode, use *timing_aocvm_analysis_mode*.

TIM-244

(Warning) AOCV ideal_clock_depth mode is enabled with propagated clocks in the design.

Description

You have received this message because you have attempted to enable AOCV ideal_clock_depth mode with propagated clocks in the design. AOCV ideal_clock_depth mode is intended for pre-CTS designs with ideal clocks.

What Next

To change AOCV analysis mode, use *timing_aocvm_analysis_mode*.

TIM-250

(warning) At pin '%s' clock '%s' does not have the needed '%s' edge.

Description

The clock tree contains half unate timing arcs or disable timing commands that have disabled the needed rise or fall edge. The register clock pin given will not have the clock assigned to it and will not be timed.

What Next

Alter clock network to propagate the needed clock edge to this register.

TIM-255

(Warning) Sense relationship for generated clock (%s) (%s) is not satisfied.

Description

This is a warning message whenever the clock network traverse cannot find a path which satisfies the sense relationship defined by create_generated_clock command.

What Next

Check for the generated clock definition to see if the generated clock is correctly defined. One example is that a divided by 2 generated clock is driven by an inverter only. In this case, generated clock should be redefined with -invert with -divided by 1. Another example is a divided by 2 generated clock with pre-inverting. If master clock source pin is used as

generated clock source pin, the warning message will be issued. In this case, generated clock source pin should be redefined to clock pin of divider.

TIM-260

(Warning) Low CPU utilization was detected during timing update.

Description

This message indicates that more physical memory is needed for this design to run efficiently with the specified degree of parallelism, or possibly that too many other processes are running concurrently on the same machine so performance is degraded by memory swapping.

What Next

Allocate more memory resources for the job. You can also reduce the degree of parallelism by setting the application variable *timing_max_parallel_computations* to a smaller value or decreasing -max_cores specified in *set_host_options*.

See Also

- set_host_options

TIM-268

(Warning) Timer cannot run multicore despite available cores.

Description

This message is issued when multicore behavior is enabled after the timer or detail-route extractor have been invoked.

What Next

To get the benefit of multicore timing, please turn on multicore behavior by issuing *set_host_options -max_cores n*, before calling the Timer. The Timer is invoked as a result of issuing command such as report_timing, report_qor, update_timing or during optimization.

If you wish to use the multicore timer in the current session, please save and re-open the design.

See Also

- set_host_options

Feedback

TIM-269

(Information) Used %d cores for timing computations.

Description

This message indicates that multiprocessing has been used to speed up timing computations.

What Next

Multi-process timing updates require more physical memory (RAM) than is needed for single process updates and this can lead to exessive paging and low CPU utilization if your machine doesn't have enough memory. To disable multi-process timing updates, you can set the 'timing_single_core' variable to 'true'.

See Also

- set_host_options

TIM-270

(Information) Using %d cores for timing computations.

Description

This message indicates that multiple cores are being used to speed up timing computations.

What Next

No action is required.

See Also

- set_host_options

TIM-271

(Information) Multithreaded timing computations have been disabled because this is a post-CTS design.

Description

This message indicates that multithreaded timing updates have been disabled.

Feedback

What Next

No action is necessary.

See Also

- set_host_options

TIM-272

(Information) Multi-core timing computations have been %s.

Description

This message indicates that multi-core timing updates have been disabled or enabled.

What Next

No action is necessary.

See Also

- set_host_options

TIM-273

(Error) The command (%s) does not support the combination of (%s) and (%s).

Description

This message indicates that listed options are exclusive, only one can be specified. The command does not support the combination of -scenario and -clock_trees (report_clock_tree) or -clock (report_clock_timing). It supports -clock or -clock_tree for current scenario.

What Next

Users can loop through each of the scenario, make the scenario current by using current_scenario command, then call the command either report_clock_timing -clock {list of clock objects} or report_clock_tree -clock_tree {list of clock objects}.

e.g. # save the original scenario set scn [current_scenario]

current_scenario newScen report_clock_timing -clock {list of clock objects in newScen} report_clock_tree -clock_tree {list of clock objects in newScen}

restore the original scenario current_scenario $scn

Feedback

See Also

- current_scenario
- get_clocks

TIM-276

(warning) Paths from startpoints clocked by clock '%s' to endpoints clocked by clock '%s' may be unconstrained because the ratio of clock periods exceeds the expansion limit (%d).

Description

This warning message occurs when a path exists from a startpoint to an endpoint where the endpoint's clock period is larger than the startpoint's clock period multiplied by the expansion limit. Due to limits in the floating point variables used to store clock pulse times, timing for such paths cannot be accurately computed and the paths may become unconstrained.

What Next

Try to avoid using clocks with widely different periods in the same design. If this is not possible, you may be able to use the set_max_delay and set_min_delay commands (with -from_clock and -to_clock options) to constrain paths involving clocks with very different periods.

TIM-280

(warning) Both set_arc_delay_override and set_annotated_delay are specified from '%s' to '%s', set_annotated_delay constraint is ignored.

Description

This warning message occurs when you set both set_arc_delay_override and set_annotated_delay at the same arc, tool will only honor set_arc_delay_override and ignore the set_annotated_delay command.

The following shows an example of the warning message.

Warning: set_arc_delay_override and set_annotated_delay are specified at the same object from 'U1/A' to 'U1/Z', set_annotated_delay constraint is ignored (TIM-280).

What Next

This is a warning message only.

Feedback

TIM-281

(warning) Both set_pin_transition_override and set_annotated_transition are specified at '%s', set_annotated_transition constraint is ignored.

Description

This warning message occurs when you set both set_pin_transition_override and set_annotated_transition at the same pin, tool will only honor set_pin_transition_override and ignore the set_annotated_transition command.

The following shows an example of the warning message.

Warning: set_pin_transition_override and set_annotated_transition are specified at the same object 'U1/A', set_annotated_transition constraint is ignored (TIM-281).

What Next

This is a warning message only.

TIM-282

(warning) Both set_timing_check_override and set_annotated_check are specified from '%s' to '%s', set_annotated_check constraint is ignored.

Description

This warning message occurs when you set both set_timing_check_override and set_annotated_check at the same arc, tool will only honor set_timing_check_override and ignore the set_annotated_check command.

The following shows an example of the warning message.

Warning: set_timing_check_override and set_annotated_check are specified at the same object from 'ff1/CP' to 'ff1/D', set_annotated_check constraint is ignored (TIM-282).

What Next

This is a warning message only.

TIM-283

(warning) Both "set_annotated_check" and "set_annotated_check -increment" are specified from '%s' to '%s', "set_annotated_check -increment" constraint is ignored.

Feedback

Description

This warning message occurs when you set both set_annotated_check and set_annotated_check -increment at the same arc, tool will only honor set_annotated_check and ignore the set_annotated_check -increment command.

The following shows an example of the warning message.

Warning: Both "set_annotated_check" and "set_annotated_check -increment" are specified from 'ff1/CP' to 'ff1/D', set_annotated_check -increment constraint is ignored (TIM-283).

What Next

This is a warning message only.

TIM-284

(warning) Path exception applied to '%s' is ignored because '%s' is an invalid startpoit/endpoint.

Description

This warning message occurs when timing_reset_path_with_invalid_fromto is set to true and set_false_path/set_multicycle_path -from/-to is applied to the pin/cell which is not a valid startpoint/endpoint, in which case the exception will be ignored for the given object and the object will be removed from that path exception.

set_max_delay/set_min_delay will force given from/to object as startpoint/endpoint so will not be ignored.

group_path will also not be ignored.

What Next

This is only a warning message. No action is required.

However, if the result is not what you expected, check the constraint file for any errors.

TIM-300

(Error) Could not %s timing data %s %s:\n \t%s.\n \tFalling back to full update.

Description

The application sometimes saves timing data to a temporary file. Something went wrong either saving or restoring this data. For example, if the target disk was full, you would get this message. The program will continue as though the temporary directory was unavailable, possibly with some performance penalty.

Feedback

What Next

Files are saved either to /tmp or the value of the TMPDIR environment variable. If the message indicates that saving was in progress, most likely the temporary directory does not exist, you don't have permissions to write to it, or it is full. The message will indicate the cause. In most cases, the disk is full. Either delete some files, or find a different temporary directory and set the TMPDIR environment variable to point at it. A problem during restore is rare. It might be that someone accidently deleted the file or the file became corrupt.

TIM-301

(Warning) Could not launch a process to update timing for scenario (%s) due to insufficient memory, required: %lld kB, avaialbe (swap+RAM) %lld kB.\n \tContinue timing update in the main process.

Description

Failed to launch a process during timing update with multicore due to insufficient memory.

What Next

More memory resource could be allocated to this job. The degree of parallelism in multicore timing update can also be reduced by setting the application variable *timing_max_parallel_computations* to a number less than -max_cores value specified in *set_host_options*.

See Also

- set_host_options

TIM-302

(Warning) Insufficient memory for %d processes in multicore timing update, %lld Kbytes memory are needed to run with %d cores.\n \tContinue timing update in the main process.

Description

Currently, physical memory installed is insufficient for timing update using current setting, so we continue timing update in the main process to prevent performance degradation due to memory paging/swapping.

What Next

You can reduce the degree of parallelism by setting the application variable *timing_max_parallel_computations* to a number less than -max_cores specified in *set_host_options*, or allocate more memory resource for this job.

Feedback

See Also

- set_host_options

TIM-303

(Warning) Could not launch a process in multicore timing update for scenario (%s), reason is (%s).\n \tContinue timing update in the main process.

Description

Failed to launch a process during timing update with multicore due to a system limit or lack of critical system resources, like memory.

What Next

If launch failed due to insufficient memory, more memory resource should be allocated to this job. Alternatively the degree of parallelism in multicore timing update can be reduced by setting the application variable *timing_max_parallel_computations* to a number less than -max_cores specified in *set_host_options*.

See Also

- set_host_options

TIM-310

(Warning) Pin (%s) (%s) (%s) will be using annotated value of (%f) as clock (%s) transition.

Description

When there are *set_pin_transition_override* on one pin for some specified clocks, the other un-specified clocks computation will honor the worst user specified clock transition value.

What Next

User can specify their wanted pin transition value for all clocks by using *set_pin_transition_override -clocks*.

TIM-320

(warning)tag independent clocks at pin is different with the tag dependent clocks at (%s)

Description

the clocks at pin that derived from dc pin hash, this is tag independent, are different with the ones from accessing pin totals, this is tag dependent.

Feedback

What Next

you should use the tag dependent clocks, set timing_tag_independent_clocks_at_pin = FALSE this message is on when using the new flow, or the self test is on, to trun off the message, set timing_tag_independent_clocks_at_pin_self_test = FALSE

TIM-321

(warning)tag independent clocks at pin check is different with the tag dependent clocks check at (%s)

Description

the check whether any clock arrive this pin that is derived from dc pin hash, this is tag independent, is different with the check from accessing pin totals, this is tag dependent.

What Next

you should use the tag dependent clocks, set timing_tag_independent_clocks_at_pin = FALSE this message is on when using the new flow, or the self test is on, to trun off the message, set timing_tag_independent_clocks_at_pin_self_test = FALSE

TIM-401

(warning) Library (%s) contains zero CCS output_current table, skip auto CCS to NLDM conversion .

Description

This warning message occurs when values in one library arc CCS output_current table are all zero. This kind of CCS library is invalid. If it is mix NLDM and CCS library we will skip CCS to NLDM conversion and turn to use the original NLDM library. User can use check_library command to check output_current table_trend to verify the library problem.

What Next

To fix the library problem.

TIM-402

(warning) All existing lib_cell timing derate settings will be reset due to variable switching.

Description

This warning message occurs when the value of the application variable timing_library_derate_is_scenario_specific is modified. Once we change this value, all previous lib-cell timing derate values will be reset, no matter global or scenario-specific.

Feedback

What Next

This is only a warning message. No action is required.

See Also

- set_timing_derate

TIM-403

(warning) All existing set_disable_timing settings upon lib-cell will be reset due to variable switching.

Description

This warning message occurs when the value of the application variable timing_disable_lib_cell_is_scenario_specific is modified. Once we change this value, all previous set_disable_timing settings upon lib-cell will be reset, no matter global or scenario-specific.

What Next

This is only a warning message. No action is required.

See Also

- set_disable_timing

TIM-422

(warning) Ignore set_data_check constraint due to related_pin '%s' beyond charz-block.\n

Description

This warning message occurs we try doing characterize for set_data_check constraint while its related-pin is defined beyond charz-block.

What Next

This is only a warning message. No action is required.

See Also

- set_data_check

Feedback

TIM-423

(warning) CHARZ: Precedence lost detected,auto-adjusting path-exception...\n

Description

This warning message occurs we try doing some path-exception precedence adjustment for charactrize. ICC might have issue when characterize try to convert path-exception from top-level to sub-block. The top-most constraint which originally honored in top-level will be replaced by some other constraint.

What Next

This is only a warning message. No action is required.

See Also

- set_max_delay
- set_multicycle_path

TIM-424

(information) Mismatch max/min libraries defined in set_operating_condition. Pick up generated-clock derived from '%s'.\n

Description

In MV-multicorner mode, ICC will pick up the generated-clock definition derived from max_library which has been defined through set_operating_condition. You will see this information when different max/min libraries have been used in set_operating_condition.

TIM-425

(warning) Characterize: Generated clock (%s) with -multiply_by switch cannot be aligned when only the inverted clock is avaialable to the block.

Description

This warning message occurs the characterize command is processing a generated clock that was defined using the -multiply_by swtich, and only the inverted source clock is available in the block that is being characterized. Under these conditions, it is not always possible to created a generated clock within the that has rise and fall edges at the same times as the original clock had at the top level.

Feedback

What Next

If the exact phase relationship is imporant, it may be necessary to replace the generated clock with a non-generated clock.

See Also

- create_generated_clock

TIM-501

(warning) All timing-context settings will be reset due to variable switching.

Description

This warning message occurs when the value of the application variable 'hier_enable_analysis' is changed. Once we change this value, all previous timing-context setting file will be reset.

What Next

This is only a warning message. No action is required.

TIM-502

(warning) Error happens when resolve timing-context clock '%s'.

Description

This warning message occurs when failure happens during resolving timing-context clocks.

What Next

Needs changes to clock definition based upon 'report-clock -map'.

TIM-503

(warning) Inconsistency detected in timing context file.

Description

This warning message occurs when some inconsistency detected in timing context file.

What Next

You need to double-check the timing-context file correctness and see whether there is any change(netlist) after context file being generated.

Feedback

TIM-504

(Warning) Timing-context has been removed.

Description

This info message occurs when timing-context has been removed.

What Next

Please double-check whether you need reload timing-context file or not.

TIM-505

(Warning) lib-cell %s based timing derate constraint dropped.

Description

Could not locate library cell while reading lib-cell based timing derate constraint the saved design. Possible reason may be linked libraries were changed.

What Next

Please double-check the linked libraries.

TIM-506

(Warning) lib-cell %s based aocvm table constraint dropped.

Description

Could not locate library cell while reading lib-cell based aocvm tables from the saved design. Possible reason may be linked libraries were changed.

What Next

Please double-check the linked libraries.

TIM-510

(Warning) report_timing has satisfied the max_paths criteria. There are %d further endpoints which have paths of interest with slack less than %g that were not considered when generating this report.

Description

This message indicates that the *report_timing* algorithm has succeeded in finding max_paths number of paths and that there are further endpoints with paths of interest.

Feedback

What Next

To see all paths of interest, increase max_paths.

See Also

- report_timing

TIM-511

(warning) All the path_margin values specified by the set_path_margin command will also be removed.

Description

reset_fast_pba_analysis_options will remove all path margins generated by *apply_fast_pba_analysis* or those specified by the user through *set_path_margin* commands.

What Next

This is only a warning message. No action is required.

See Also

- set_path_margin

TIM-512

(Warning) Derate reporting is ignored when the net of driver pin has no detailed parasitics.

Description

This warning message occurs during *report_delay_calculation. When -derate is applied and the net of driver pin has no detailed parasitics, the -derate option will be ignored.*

See Also

- report_delay_calculation

TIM-513

(Warning) After J2014.09 release, the option -stop_propagation stops propagation of the specified clocks at the specified pins along the clock paths only.

Feedback

Description

This warning message occurs when *set_clock_sense -stop_propagation* is used. The option *-stop_propagation* stoped propagation of the specified clocks at the specified pins along both clock paths and data paths in previous versions. After J2014.09 release, it stops propagation along the clock paths only to be compatible with PrimeTime(PT).

See Also

- set_clock_sense

TIM-514

(error) Illegal -sort_by option of '%s'.

Description

Valid option strings for the -sort_by option are "group", "slack". Type help 'report_timing' to see a description of the options.

What Next

Re-type command with correct options.

TIM-530

(information) Using cell EM libraries.

Description

This message is produced if any library containing cell EM information is used. It is only produced once per session when the first cell EM information is queried.

What Next

No action is needed. This information may be helpful when determining whether a design contains cell EM library.

TIM-531

(information) Unable to set modes for cell instance %s in scenario %s.

Description

This message is produced if there are no mode information in the scenario for the specified cell instance.

Feedback

What Next

No action is needed. Please make sure that the current scenario has the correct mode information.

TIM-532

(information) Using cell EM libraries.

Description

This message is produced if any library containing cell EM information is used. It is only produced once per session when the first cell EM information is queried.

What Next

No action is needed. This information may be helpful when determining whether a design contains cell EM library.

TSV

TSV-001

(Error) No design loaded for TSV or TSV module is not enabled.

Description

This message is issued during TSV die level run, when the timing information of feedthrough paths is written into files using *write_tsv_timing*.

What Next

Make sure the current design is set correctly and TSV module is enabled in PrimeTime.

TSV-002

(Information) Wrote timing for %d feedthrough paths.

Description

This message is issued during TSV die level run, when the timing information of feedthrough paths is written into files using *write_tsv_timing*.

What Next

No action required.

Feedback

TSV-003

(Error) Instance named '%s' is not found!

Description

This message is issued during TSV stack level run, when the timing information of feedthrough paths is read into PrimeTime using *read_tsv_timing*.

What Next

Make sure the instance name is typed correctly.

TSV-004

(Information) Annotate timing for %d feedthrough paths.

Description

This message is issued during TSV stack level run, when the timing information of feedthrough paths is annotated using *read_tsv_timing*.

What Next

No action required.

TSV-005

(Error) Found error in reading '%s'. Please make sure the setting of each corner is the same when write tsv timing.

Description

This message is issued during TSV stack level run, when the timing information of feedthrough paths is read into PrimeTime using *read_tsv_timing*.

What Next

Make sure the setting of each corner is the same using *write_tsv_timing*.

TSV-006

(Information) No from pin or to pin specified, report all TSV timing by default.

Description

This message is issued during TSV stack level run, when the timing information of a user specific feedthrough path is reported using *report_tsv_timing*.

Feedback

What Next

No action required.

TSV-007

(Error) Cannot open '%s' for reading.

Description

This message is issued during TSV stack level run, when the timing information of feedthrough paths is read into PrimeTime using *read_tsv_timing*.

What Next

Get the permission to access the file when use *write_tsv_timing*.

TSV-008

(Warning) TSV path from %s to %s is unconnected.

Description

This message is issued during TSV stack level run, when this TSV path has been identified but not used after *read_tsv_timing*.

What Next

Check if the unconnected TSV path is expected.

TSV-009

(Error) At least 2 corners are required to compute skew adjustment!

Description

This message is issued during TSV stack level run, when the timing information of feedthrough paths is read into PrimeTime using *read_tsv_timing*. PrimeTime requires at least 2 corners to compute skew adjustment.

What Next

Make sure to provide at least 2 corners when *read_tsv_timing*.

TSV-011

(Error) No TSV timing information to remove.

Feedback

Description

This message is issued during TSV stack level run, when the timing information of feedthrough paths is removed using *remove_tsv_timing*.

What Next

Make sure there exists TSV timing information before trying to remove it.

TSV-013

(Error) '%s' is not a valid TSV timing data file!

Description

This message is issued during TSV stack level run, when the timing information of feedthrough paths is read into PrimeTime using *read_tsv_timing*.

What Next

Make sure the file read by PrimeTime TSV module is a valid TSV timing data file generated by *write_tsv_timing*.

TSV-015

(Error) No TSV timing data files have been read in.

Description

This message is issued during TSV stack level run, when the names of read-in timing data files are reported using *report_tsv_file*, or the timing information of a user specific feedthrough path is reported using *report_tsv_timing*, or the TSV skew calculation details of a user specific timing path are reported using *report_tsv_skew*.

What Next

Make sure to read some TSV data files using *read_tsv_timing*.

TSV-017

(Error) '%s' is not a valid pin!

Description

This message is issued during TSV stack level run, when the timing information of a user specific feedthrough path is reported using *report_tsv_timing*.

Feedback

What Next

Make sure the pin name represents a valid pin in the design.

TSV-019

(Error) No timing path has been specified.

Description

This message is issued during TSV stack level run, when the TSV skew calculation details of a user specific timing path are reported using *report_tsv_skew*.

What Next

Make sure to get a valid timing path using *get_timing_paths*.

TSV-021

(Error) No valid TSV path starts from '%s' !

Description

This message is issued during TSV stack level run, when the timing information of a user specific feedthrough path is reported using *report_tsv_timing*.

What Next

Make sure the pin name represents a valid start pin of the TSV path in the design.

TSV-023

(Error) No valid TSV path ends to '%s' !

Description

This message is issued during TSV stack level run, when the timing information of a user specific feedthrough path is reported using *report_tsv_timing*.

What Next

Make sure the pin name represents a valid end pin of the TSV path in the design.

TSV-025

(Error) '%s' and '%s' are not on the same die!

Feedback

Description

This message is issued during TSV stack level run, when the timing information of a user specific feedthrough path is reported using *report_tsv_timing*.

What Next

Make sure the pin names represent valid start and end pins of the TSV path on the same die.

TSV-027

(Error) From '%s' to '%s' is not a valid TSV path!

Description

This message is issued during TSV stack level run, when the timing information of a user specific feedthrough path is reported using *report_tsv_timing*.

What Next

Make sure the pin names represent valid start and end pins of the TSV path in the design.

TSV-029

(Error) '%s' is not on a middle die!

Description

This message is issued during TSV stack level run, when the timing information of a user specific feedthrough path is reported using *report_tsv_timing*.

What Next

Make sure the pin name represents a valid pin on a middle die in the stack level.

TSV-101

(Error) %s is enabled but not supported by TSV analysis.

Description

This message is issued during TSV stack level run, when the timing information of feedthrough paths is read into PrimeTime using *read_tsv_timing*.

What Next

Disable the corresponding incompatible features which is not supported by TSV analysis.

Feedback

UFO

UFO-001

(Warning) Unexpected fatal occurrence when calculating %s for driver %s. %s

Description

You receive this warning message because the tool encountered an unexpected error during calculation for the particular driver reported. For this stage the tool has performed a default action to avoid a crash.

What Next

Please report the issue so the testcase can be debugged. You can also workaround the issue by either excluding the particular stage for analysis if possible.

See Also

- set_si_delay_analysis
- set_si_noise_analysis
- set_multi_input_switching_analysis

UFO-002

(Warning) Unexpected fatal occurrence when calculating %s for arc from %s to %s.

Description

You receive this warning message because the tool encountered an unexpected error during delay calculation for the particular arc reported. For this stage the tool has performed a default action to avoid a crash.

What Next

Please report the issue so the testcase can be debugged.

See Also

- report_delay_calculation

Feedback

UIAT

UIAT-1

(error) Cannot specify %s for '%s' type.

Description

While defining a new user attribute, you specified (a) either or both of the options that define a range, but did not specify a data type that supports ranges, or (b) an option limiting a string type to a set of values without using a string data type.

What Next

Ranges only work with integer and double data types. Limiting an attribute to a set of strings only works with the string data type.

UIAT-2

(error) Min of range (%s) cannot be greater than max (%s).

Description

While defining a new user attribute, you specified a numeric range, and the minimum value was greater than the maximum value.

What Next

Complete ranges require that the max value is greater than min.

UIAT-4

(Warning) Attribute '%s' is already defined in class '%s'

Description

While defining a new user attribute, you specified an attribute name that is already defined. There is no mechanism to change an attribute definition.

UIAT-5

(warning) Cannot get attribute for more than one object.

Feedback

Description

While getting the value of an attribute, you specified more than one object. You can only get the attribute for a single object.

What Next

Specify a single object.

UIAT-7

(Warning) Cannot import user attributes for %s.

Description

While defining a new user attribute, you specified that the attribute should be imported from db files. However, the class of objects for which you are defining the attribute does not allow attributes to be imported.

UIAT-8

(warning) Attribute '%s' is already defined as %s for another class.

Description

While defining a new user attribute, you specified an attribute name which is in use for another object class, but the data type which you specified was not the same as for the other object class. An attribute must have the same data type for all object classes for which it is defined.

What Next

Determine which is the correct data type, and re-define the attribute for each affected class.

UIAT-9

(Warning) Size of %s created by %s exceeds Tcl limit of 2147483647 characters.

Description

PrimeTime tried to create a Tcl variable of size exceeding Tcl variable size limit of 2147483647 characters (2 GB - 1 byte). For example, this error may be issued if *get_object_name* is called with a large collection of pins to create a list of pin names and the size of the list exceeds the Tcl variable size limit.

If this warning is issued, the command which tried to create the list exits without creating a list.

Feedback

What Next

Modify the script to generate Tcl variables of sizes less than 2147483647 characters.

UIAT-10

(Warning) Length of Tcl list created by %s exceeds the limit of 536870909 elements.

Description

PrimeTime tried to create a Tcl list of length exceeding Tcl list limit of 536870909 elements. For example, this error may be issued if *get_object_name* is called with a pin collection with the collection size being greater than 536870909.

If this warning is issued, the command which tried to create the list exits without creating a list.

What Next

Modify the script to avoid creation of Tcl lists beyong the limit.

UID

UID-95

(warning) Can't find %s '%s' in design '%s'.

Description

This error message is generated when you try to find a non existing object of a given type in the specified design or the design is hidden and so the object cannot be shown.

What Next

Check the object by invoke report_<object>, then reinvoke the current command.

UID-1060

(error) There must be at least 3 elements in %s list.

Description

This error is generated when there are not enough elements for -regsub option for command 'set_query_rules'.

Feedback

What Next

Check out the man page for Tcl Built-In regsub then reset the options for this.

UIMS

UIMS-001

(Warning) -setup, -hold and -op_cond are not supported in PrimeTime

Description

These options are not supported in PrimeTime, and used only in Design Compiler.

UIMS-003

(error) Command option %s only works on PrimeTime multi-scenario manager.

Description

The specified command option can only be used in the manager session of the PrimeTime multi-scenario analysis.

What Next

Launch PrimeTime in multi-scenario mode to use the specified option.

UIMS-004

(error) Cannot open the following %s type files %s.

Description

The file name provided cannot be opened.

What Next

Validate that the file name is correct. Or, confirm that the file path is visible, by verifying that the search path with *list search_path*. Read the file once again after fixing.

UIMS-005

(error) Scenario '%s' already exists.

Description

The scenario has already been created. Each scenario must have a unique identifier.

Feedback

What Next

Use a different name for each scenario.

UIMS-007

(error) No configuration exists.

Description

No configuration has been created or exists.

What Next

Create a configuration using the *create_configuration* command.

UIMS-008

(error) There is no current session.

Description

The current session has not been specified and does not exist.

What Next

Use command *current_session to create a current session.*

See Also

- current_session

UIMS-009

(Error) The following scenario name '%s' does not exist.

Description

The specified scenario does not exist.

UIMS-010

(Error) A configuration already exists.

Description

A configuration has already being created. It is not possible to have more than one configuration at any given time.

Feedback

UIMS-011

(error) The command focus cannot be accessed before the session focus has been set.

Description

Until the session has been create with the *current_session* command, there is no command focus to get or alter using the *current_scenario* command.

What Next

Use the *current_session* command to create the current session and then apply the *current_scenario* command again to interact with the command focus.

See Also

- current_scenario
- current_session

UIMS-013

(error) The scenario '%s' is not defined in the current session.

Description

The specified scenario must be in the current session before using current_scenario.

What Next

To bring the specified scenario into exclusive focus, use current_session *first.*

UIMS-014

(error) Passing a sub-set of duplicate scenarios with common name '%s' to %s is not allowed.

Description

A list of scenarios passed to the command shown in the message contains duplicate scenarios. The command requires that the full set of duplicates of a particular scenario should be passed to the command together.

What Next

Add all duplicates of a particular scenario to the list of scenarios passed to the command.

Feedback

UIMS-015

(error) Could not set %s to be the error log .

Description

The multi scenario error log was set to an invalid file name. The file name given was either a directory or the filename resolved to a file which could not be opened or the file name contained a path which could not be resolved.

What Next

Choose a valid file name for the error log.

UIMS-016

(Error) The host type has not been specified.

Description

PrimeTime cannot add a distributed host without host type being specified.

What Next

Specify a host type when specifying a host.

UIMS-017

(Warning) The max number of hosts allowed to be added has been reached.

Description

The maximum number of hosts allowed to be added has been reached. The maximum allowable number of hosts is %d.

UIMS-018

(Warning) Unable to read host '%s' . This host has not been added.

Description

There has been a problem reading the host '%s'. The host has not been added.

What Next

Ensure that when adding a host, the format is correct, i.e. hostname.

Feedback

UIMS-019

(Error) Cannot add a distributed host with an unknown host type.

Description

The host type specified is unknown, so the host has not been added.

What Next

Ensure that when adding a host, the options are correct. Type help -v *add_distributed_processor*.

UIMS-020

(Error) Cannot set the current session.

Description

The resources required to be able to set the current session are not available.

What Next

See the *current_session* command for the resource requirements and how to query the available resources.

UIMS-021

(Information) Generating a Distributed Path-Based Analysis report.

Description

The *report_timing* command is generating a PBA report using multiple duplicated scenarios to parallelize PBA caculations.

UIMS-022

(Error) The command %s has exceeded the maximum number of allowable characters

Description

The remote execute command can not handle commands greater than 1000 characters long.

Feedback

What Next

Use ';' to seperate the remote_execute command_string into a set of individual commands. If a single command is greater than 1000 lines, place the command in a script and issue remote_execute {source script}

UIMS-023

(Error) No scenarios were found.

Description

While trying to create a multi-scenario session using all scenarios, no scenarios were found to add to the current session.

UIMS-024

(Error) The configuration must have at least one netlist file.

Description

When creating a configuration using the *create_configuration* command, at least one file must be specified with the *-common_data* option.

UIMS-025

(error) Scenario '%s' could not be created.

Description

Scenario with the given name could not be created due to an error.

What Next

Check options given to *create_scenario*.

UIMS-027

(Error) create_scenario does not support the usage of -common_variables or -common_data when the -image option is specified.

Description

The *create_scenario* command does not support the *-common_variables* and *-common_data* options when the *-image* option is passed to the command.

Feedback

What Next

Either use the *-common_variables* and *-common_data* options with the *create_scenario* command or use the *-image* option, but not both. If variables need to be set and/or data files sourced after loading the scenario image, the *-specific_variables* and *-specific_data* options can be used with the *-image* option.

See Also

- create_scenario

UIMS-028

(error) There are no scenarios in command focus.

Description

There are no scenarios in command focus on which the command can be run.

What Next

Use the *current_scenario* command to specify the command focus.

UIMS-029

(error) The session saved at '%s' is not usable.

Description

The session saved in the location specified either cannot be accessed or is not a valid saved session.

What Next

Ensure the directory specified is a network accessible directory so that both the manager and remote processes can access the directory.

Ensure the user account has premssions to access the directory.

Ensure the directory contains a valid PrimeTime saved session compatible with the version of PrimeTime being run.

UIMS-030

(error) The scenario name cannot contain '%s'

Feedback

Description

The scenario name cannot contain the string specified.

What Next

Create the scenario using a name that does not contain the string specified.

UIMS-031

(error) Mix and match of -mode/-corner style and -name style is prohibited.

Description

You have either created some scenarios with -mode/-corner and are now creating a scenario with -name OR vice versa. Please use one style exclusively. If you use -mode/-corner style, a scenario name of $mode_$corner is automatically created.

What Next

Use one style uniformly. The new style of specifying with -mode/-corner is recommended.

UIMS-032

(Information) Variable '%s' is assigned the value '%s' following merging of the scenario-specific value '%s' and the manager-side value '%s'

Description

In the distributed multi-scenario analysis, the indicated variable can be set both at the DMSA manager and a scenario. In this case, the value of the variable at the manager is added to the value of the variable at the scenario.

UIMS-033

(error) Command option %s is not supported in the DMSA manager session.

Description

The specified command option is not supported at the DMSA manager.

What Next

Execute the command using remote_execute

Feedback

UIMS-034

(warning) The name 'common_data' cannot be used as the name of a scenario. It is reserved for internal use by PrimeTime to effect disk usage savings by sharing common data among DMSA scenarios.

Description

The name 'common_data' cannot be used as the name of a scenario.

What Next

Choose another scenario name.

See Also

- create_scenario
- save_session

UIMS-035

(warning) empty affinity specification.

Description

The affinity specification is empty so it will be treated as if no affinity has been specified. The scenario is allowed execute on any worker process launched using any host options.

What Next

If you intended to specify an affinity, please remove the scenario using the *remove_scenario* command and re-create it specifying a valid affinity.

See Also

- create_scenario
- remove_scenario

UIMS-036

(error) invalid host options name '%s' in affinity specification.

Description

The host options name indicated is not a valid argument for the affinity specification. Either the host options named does not exist or is an auto-derived name.

Feedback

What Next

Use the *report_host_options* command to see if the host options exist.

If the host options do not exist, then create the host options using the *set_host_options* command and create the scenario as before.

If the host options do exist, then they were created without specifying the *-name* option to *set_host_options* command. Use the *remove_host_options* command to remove the host options, recreate the host options using the *set_host_options* command passing a suitable *-name* argument and create the scenario as before.

See Also

- create_scenario
- remove_scenario
- set_host_options
- remove_host_options

UIMS-037

(Error) This command is disabled on the DMSA manager and curly braces {} should be used around the command.

Description

This command is disabled on a Distributed Multi Scenario Analysis (DMSA) manager. Use the curly brace syntax to forward the command to a DMSA enabled command.

What Next

Please surround the command with curly braces (i.e {}) when passing this command to a DMSA-compatible command.

UIMS-038

(Error) The command %s can only be run on the DMSA manager.

Description

This command can only be run in the Distributed Multi Scenario Analysis (DMSA) manager shell.

What Next

Please check that you are running the command in the correct PrimeTime mode.

Feedback

UIMS-039

(Error) The command %s requires netlist to be loaded at DMSA manager.

Description

This command can only be run in the presence of netlist in a DMSA manager process.

What Next

Please load design information in a manager process before running this command.

UIMS-040

(error) The specified path '%s' does not exist.

Description

The directory or file name path specified by the option does not exist.

What Next

Ensure the directory specified is a network accessible directory so that both the manager and remote processes can access the directory.

Ensure the user account has premssions to access the directory.

UIPTC

UIC-067

(warning) Option '%s' contains implicit references to objects, use '[get_* %s]' instead.

Description

This option contains implicit references to objects. A standard format with explicit references to objects using [get_* *] is recommended.

What Next

Update your script to use the suggested new option.

Feedback

UIPWR

UIPWR-001

(error) Command '%s' is not enabled in UI backward compatibility mode. Set power_ui_backward_compatibility to FALSE to enable this command.

Description

You received this error message because variable *power_ui_backward_compatibility* has been set to *TRUE* while this command is not enabled in UI backward compatiblity mode.

What Next

Set *power_ui_backward_compatibility* to *FALSE*.

UIPWR-002

(error) Command '%s' is not enabled as default. Set power_ui_backward_compatibility to TRUE to enable this command.

Description

You received this error message because variable *power_ui_backward_compatibility* has been set to *FALSE* while this command is not enabled if backward compatiblity is not ON.

What Next

Set *power_ui_backward_compatibility* to *TRUE*.

UIPWR-003

(error) Command '%s' is not supported in '%s' power analysis mode. Set power_analysis_mode to '%s' in order to run this command.

Description

You received this error message because variable *power_analysis_mode* has been set to a mode which is not compatible with this command.

What Next

Set *power_analysis_mode* to the recommended mode.

See Also

- power_analysis_mode

Feedback

UIPWR-004

(Warning) Command '%s' is not fully supported in '%s' power analysis mode. The annotated power value is only reflected in average power result but not in peak power result.

Description

Command '*set_annotated_power*' is not fully supported in time_based power analysis mode yet. The annotated power value is only reflected in average power result but not in peak powers and power waveforms.

See Also

- power_analysis_mode
- set_annotated_power

UIPWR-005

(error) Command '%s' is not supported in '%s' power analysis mode. Set power_analysis_mode to '%s' in order to run this command.

Description

You received this error message because variable *power_analysis_mode* has been set to a mode which is not compatible with this command.

What Next

Set *power_analysis_mode* to the recommended mode.

See Also

- power_analysis_mode

UIPWR-006

(Error) Command '%s' can not be run when power is not updated in '%s' power analysis mode. Please check the current power analysis mode and run update_power if necessary.

Description

In time_based power analysis mode, command '*write_saif*' can only be issued after power analysis is done. Please make sure that the correct power analysis mode is set, and run *update_power* in case of time_based power analysis mode.

Feedback

See Also

- power_analysis_mode
- update_power

UIPWR-007

(Error) Option '%s' in command '%s' has been moved to command set_power_analysis_options.

Description

The specified option has been moved to a new PrimePower command *set_power_analysis_options*. Please use the new command for setting this specific option.

What Next

Please check out the man page for command *set_power_analysis_options* for more information. Set the option by using command *set_power_analysis_options* instead. As a temporary work around, you can also set *power_ui_backward_compatibility* to true.

See Also

- set_power_analysis_options

UIPWR-008

(error) Can not enable or disable UI backward compatibility after power analysis commands have been issued.

Description

Variable *power_ui_backward_compatibility* can only be set before the first power analysis command. It can not be changed after power analysis commands have been issued.

What Next

Set variable *power_ui_backward_compatibility* before the first power analysis command.

UIPWR-009

(error) Can't switch to power analysis mode '%s'.

Description

Variable *power_analysis_mode* can be changed during run. However, error was incurred during mode switching.

Feedback

What Next

Please check the analysis mode setting and run power analysis again.

See Also

- power_analysis_mode

UIPWR-010

(error) '%s' option can only be specified in '%s' power analysis.

Description

The error message indicated that the option of *set_power_analysis_options* was not supposed to be used in the current power analysis mode.

What Next

Check the value of *power_analysis_mode* and make sure the option can be used for the specified mode.

See Also

- power_analysis_mode

UIPWR-011

(error) Unknown power waveform format '%s'.

Description

You received this error message because the value specified by -waveform_format option in set_power_analysis_options was not supported. The supported values are 'fsdb', 'out' and 'none'.

What Next

Check the -waveform_format option, correct the value and run the command again.

UIPWR-012

(error) Unknown value '%s' for -include option.

Feedback

Description

You received this error message because the value specified by -include option in set_power_analysis_options was not supported. The supported values are 'top', 'all_without_leaf' and 'all_with_leaf'.

What Next

Check the -include option, correct the value and run the command again.

UIPWR-013

(error) Current waveform in FSDB format is not supported. Please use .out format instead.

Description

You received this error message because the tool did not support current waveform in FSDB format. the value specified by -waveform_format option in set_power_analysis_options needs to be set to 'out' if -current option is also set for the command.

What Next

Correct the setting and run command again.

UIPWR-014

(error) Event file (VCD or its equivalent) is not properly read for the time based power analysis mode.

Description

You received this error message because the event file (VCD or its equivalent) was not properly read before the time based power analysis.

What Next

Check whether read_vcd command was specified and worked correctly.

UIPWR-015

(error) Set the power_analysis_mode variable instead of using the set_power_analysis_mode command.

Description

The power analysis mode is controlled setting by the *power_analysis_mode* variable. Using the *set_power_analysis_mode* command is not permitted.

What Next

Set the *power_analysis_mode* variable instead.

See Also

- power_analysis_mode

UIPWR-016

(warning) Previous VCD (or its equivalent) file '%s' exist, will be overriden in time based power analysis mode.

Description

You received this error message because time based power analysis mode only allow one VCD file (or its equivalent). If more than one read_vcd command is issued, the later one will override the previous one.

What Next

Check to see whether the latest file from read_vcd command is the expected file for event based power analysis.

UIPWR-017

(error) Unknown VCD format '%s'.

Description

You received this error message because the option -format of read_vcd is specified with the format unknown to PrimePower. Only 'Verilog', 'VHDL' and 'SystemVerilog' are allowed for this option.

What Next

Correct the option and run the command again.

UIPWR-018

(error) Negative start time or time interval (start_time >= end_time) in option "-time {%g, %g}" of read_vcd/read_fsdb commands.

Description

Incorrect time window. It is required that the start time be no less than 0 and the end time no less than the start time.

Feedback

What Next

Give correct time window and try again.

UIPWR-019

(error) Invalid value of

Description

Incorrect time window given.

What Next

Refer to PrimePower Manual or manpage of read_vcd/read_fsdb for how to specify time window by -time option.

UIPWR-020

(error) Command '%s' is not supported in '%s' power analysis mode.

Description

You received this error message because variable *power_analysis_mode* has been set to a mode which is not compatible with this command.

What Next

Set *power_analysis_mode* to the mode which is compatible with this command.

See Also

- power_analysis_mode

UIPWR-021

(error) Only current design is allowed for command '%s'.

Description

You received this error message because the command can only accept current design as the design object.

What Next

If the command needs to be specified for a part of current design, use cell and library cell objects for the command.

UIPWR-022

(error) Cannot specify '-leakage' with '-subtrehsold_leakage' in command set_power_derate.

Description

You received this error message because set_power_derate command can't accept leakage and subthresold leakage options together.

What Next

Remove one of the options.

UIPWR-023

(warning) '%s' option is ignored with '%s' option.

Description

The warning message indicated that the option of *report_clock_gate_savings* is ignored with the specific option combination, since it has not effect on that option combination.

What Next

Remove the specified option from *report_clock_gate_savings*.

UIPWR-024

(warning) '%s' Vth group either is not used in the design or mispelled.

Description

The warning message indicated that the supplied threshold voltage group is either is not used in the design or mispelled at command line.

What Next

Please check the spelling for the threshold voltage group in command line.

UIPWR-025

(error) '%s' option can only be specified when sdpd tracking is turned on

Feedback

Description

The error message indicated that the option sdpd_tracking_cells of *set_power_analysis_options* was not supposed to be used when sdpd tracking is turned off.

What Next

Enable sdpd tracking mode to perform sdpd tracking of the list of cells specified by sdpd_tracking_cells option.

UIPWR-026

(warning) The list of state dependent path dependent tracking cells is empty.

Description

The warning message indicates that there are no cells in the design that needs to be tracked for state and path dependent analysis.

What Next

Provide the list of cells using set_power_analysis_options -sdpd_tracking_cells

---

UIPWR-027

(error) At least internal or leakage power needs to be specified for set_annotated_power command.

Description

You received this error message because you have specified neither internal nor leakage power in the set_annotated_power command.

What Next

Specify the internal or leakage power that needs to be annotated for the cell

---

UIPWR-028

(warning) The list of library cells is empty.

Description

The warning message indicates that library cells could not find in the design.

What Next

Provide the list of lib cells using set_power_analysis_options -exclude_arc_scaling_libcells

Feedback

UIPWR-029

(error) '%s' option can only be specified when power_scale_internal_arc is turned on

Description

The error message indicated that the option exclude_arc_scaling_libcells of *set_power_analysis_options* was not supposed to be used when power_scale_internal_arc is turned off.

What Next

Enable power_scale_internal_arc.

See Also

- power_scale_internal_arc

UIPWR-030

(error) Only positive value allowed for activity derating factor.

Description

You received this error message because the value specified by -derate_factor option in set_activity_derate was not supported. The supported values are positive float values only.

What Next

Check the -derate_factor option, correct the value and run the command again.

UIPWR-031

(error) Only TR=0 and SP=0 or SP=1 allowed with -force option.

Description

You received this error message because the value specified by -toggle_rate and -static_probability option in set_switching_activity was not correct. The supported values with -force option are TR=0, and SP=0 or SP=1 only.

What Next

Check the -toggle_rate and -static_probability options, correct the value and run command again.

Feedback

UIPWR-032

(error) Cannot specify '-x_transition' with '-rails' or '-pg_pins' in command set_power_derate.

Description

You received this error message because set_power_derate command can't accept x_transition and rails/pg_pins options together.

What Next

Remove one of the options.

UIPWR-033

(error) Unknown power waveform separation '%s'.

Description

You received this error message because the value specified by -separate_power_waveform option in set_power_analysis_options was not supported. The supported values are 'leakage' and 'all'.

What Next

Check the -separate_power_waveform option, correct the value and run the command again.

UIPWR-034

(Warning) Option -include_shutdown_cells can only be specified with Option -pst in PST based power reporting.

Description

This error message occurs when the specific option is not specified along with option -pst in report_power.

What Next

Give both the option -include_shutdown_cells and -pst together in report_power and run the command again.

UIPWR-035

(Warning) '%s' option is mandatory for using '%s' option.

Feedback

Description

The prerequisite to use the mentioned option is not fulfilled.

What Next

Please check out the man page for used command to find the prerequisite for the option used.

UIPWR-036

(error) '-vt' is missing when '-cnod' is specified in command set_power_derate.

Description

You received this error message because set_power_derate command require vt to be given with cnod option.

What Next

Specify vt with cnod option.

UIPWR-039

(error) report_nonmission_pgpin_condition/get_nonmission_default_pgpin_condition commanads only works when variable power_enable_non_mission_mode_leakage is set to true.

Description

You received this error message because report_nonmission_pgpin_condition/ get_nonmission_default_pgpin_condition commands only executes when new off state leakage library model support is enabled.

What Next

Set power_enable_non_mission_mode_leakage to true for the command execution.

UIPWR-040

(error) '-verbose' can only be specified with '-pg_condition' in command report_nonmission_pgpin_condition.

Description

You received this error message because report_nonmission_pgpin_condition command require pgpin condition to be given with -verbose option.

Feedback

What Next

Specify pg_condition with verbose option.

UIPWR-041

(error) Please specify valid pgpin condition in -pg_condition for the command report_nonmission_pgpin_condition.

Description

You received this error message because provided pgpin condition is not valid.

What Next

Specify valid pgpin condition.

UIPWR-042

(error) '-no_nonmission_leakage' cannot be specified with '-pg_condition' for report_nonmission_pgpin_condition command.

Description

You received this error message because -no_nonmission_leakage and -pg_condition have been specified together.

What Next

Specify -verbose with pgpin condition to get detailed report.

UIPWR-043

(Error) Command 'write_saif' can not be run in cycle based power analysis when 'power_keep_cycle_based_activity' variable is set to true before 'update_power'.

Description

In cycle based power analysis mode, command '*write_saif*' can only be issued after power analysis is done with 'power_keep_cycle_based_activity' variable set to true. Please make sure that the variable is set to true before 'update_power' and run *update_power* in case of cycle based power analysis

See Also

- power_analysis_mode
- update_power

Feedback

UIPWR-109

(Warning) reset_switching_activity is not fully supported for objects when VCD files have been identified but not applied. The command will proceed, but since VCD activity is not applied yet, results may not be as expected.

Description

In the *averaged* or *leakage_variation* power analysis modes, VCD annotation may be deferred until later during *update_power*. Running *reset_switching_activity* prior to *update_power* will not invalidate the switching activity from the VCD if specific cells are selected.

What Next

Either reset switching activity on the whole design, or run update_power first, then reset switching activity on specific instances.

UIPWR-110

(Error) Failed to properly annotate activity from activity file

Description

An unknown error resulted in the activity file not being properly read.

UIPWR-111

(warning) command '%s' is obsolete and will be removed in the upcoming release. Please use IEEE 1801 (UPF) command 'create_power_switch' instead.

Description

Command 'set_supply_net_probability' is obsolete as it is not a standard UPF command. UPF command 'create_power_switch' should be used. For more information about 'create_power_switch', please check out the man page.

What Next

Please update the script accordingly.

See Also

- create_power_switch

Feedback

UIPWR-201

(Warning) cycle accurate options in set_power_analysis_options are ignored

Description

The *-cycle_accurate_clock* and *-cycle_accurate_cycle_count* options in *set_power_analysis_options* command can only take effect when RTL VCD or zero delay VCD is used. Otherwise, they are ignored.

What Next

Check your VCD file. If it's RTL VCD, add -rtl to read_vcd. If it's zero-delay VCD, add -zero_delay to read_vcd. Otherwise, remove -cycle_accurate_clock and -cycle_accurate_cycle_count in set_power_analysis_options.

UIPWR-202

(Warning) name mappings are ignored in time_based mode

Description

The *set_rtl_to_gate_name* commands in the time_based power analysis mode are only for RTL VCD. It will be ignored for gate level VCD.

What Next

Check your VCD file. If it's RTL VCD, add -rtl to read_vcd. Otherwise, don't use set_rtl_to_gate_name.

UIPWR-203

(Error) reset_switching_activity does not support reseting activity on individual objects in the time_based power analysis mode

Description

The *reset_switching_activity* command can only be used to clear the activity file indicated with *read_vcd* when *power_analysis_mode* has been set to *time_based*

In other modes, *reset_switching_activity* can be used to reset activity on individual objects. The *time_based* mode does not use toggle rates for power computation, but instead computes power for individual events in the activity file.

What Next

Run *reset_switching_activity* without arguments to clear the VCD.

Feedback

Or, switch to another mode if power analysis is desired with modified activity on individual design objects.

UIPWR-204

(Warning) -waveform_interval in set_power_analysis_options is ignored for RTL VCD and zero delay VCD

Description

For RTL VCD (read_vcd -rtl ...) and zero delay VCD (read_vcd -zero_delay ...), the waveform interval is determined by -cycle_accurate_cycle_count and -cycle_accurate_clock in set_power_analysis_options. The -waveform_interval in set_power_analysis_options is ignored for RTL VCD and zero delay VCD.

What Next

Remove -waveform_interval in set_power_analysis_options.

See Also

- read_vcd
- set_power_analysis_options

UIPWR-205

(Warning) When using -pipe_exec in time_based power analysis_mode, switching activity reports will not be available until after update_power has been run.

Description

In time_based mode, with the -pipe_exec option, the VCD is read during update power. Switching activity reports from *report_switching_activity* or *get_switching_activity* rely on the VCD. Before the VCD is read during update_power, such reports cannot display meaningful information.

What Next

Run update_power

See Also

- read_vcd
- update_power

Feedback

UIPWR-206

(Error) In the *time_based* power analysis mode, activity reporting may not be available prior to *update_power*

Description

In *time_based mode*, activity annotation can be reported after *read_vcd* if the *-pipe_exec* option is used. If the *-pipe_exec* option is used, annotation cannot be reported until after *update_power*.

What Next

Run read_vcd

See Also

- read_vcd
- update_power
- power_analysis_mode

UIPWR-207

(Information) Rail based waveform generation is enabled.

Description

Waveform data will be generated for each of the rails/supply_nets specified by the user in '*set_power_analysis_options*'.

See Also

- read_vcd
- set_power_analysis_options
- power_enable_multi_rail_analysis

UIPWR-208

(Warning) Rail based waveform generation could not be enabled as no valid supply nets specified.

Description

Multi rail waveform cannot be written out due to missing or invalid supply nets specified.

What Next

Check if the design has valid supply nets defined through UPF. You can use 'get_supply_nets' to check for valid supply nets.

See Also

- read_vcd
- set_power_analysis_options
- power_enable_multi_rail_analysis

UIPWR-301

(Error) variable power_enable_leakage_variation_analysis must be set to true to run leakage variation analysis

Description

In the *leakage_variation* power analysis mode, the variable power_enable_leakage_variation_analysis must be set to true prior to reading the library containing leakage varation data.

What Next

Set the variable to true at the beginning of the script, and run the script again.

UIPWR-302

(Error) The variable *power_enable_leakage_variation_analysis* is turned on, but the power analysis mode is other than *leakage_variation*.

Description

Leakage variation analysis is performed when both the variable *power_enable_leakage_variation_analysis* is set to true, and the power analysis mode is set to *leakage_variation*. If leakage variation analysis is not desired, set the variable to false.

What Next

Either set *power_enable_leakage_variation_analysis* to false, or change the power analysis mode to *leakage_variation*.

Feedback

UIPWR-601

(Error) Variable 'power_enable_transit_power_analysis' cannot be set after library power data has been loaded.

Description

Variable *power_enable_transit_power_analysis* can be used to enable transit power analysis and reporting capability. This variable needs to be set before library power data is loaded.

What Next

Set variable *power_enable_transit_power_analysis* before library power data is loaded.

UIPWR-602

(Error) Command '%s' is not enabled in Transit power analysis mode. Set power_enable_transit_power_analysis to FALSE to enable this command.

Description

This command is not enabled in Transit power analysis mode.

What Next

Set *power_enable_transit_power_analysis* to *FALSE*.

UIPWR-603

(Error) Command '%s' is only enabled in Transit power analysis mode. Set power_enable_transit_power_analysis to TRUE to enable this command.

Description

This command is used for Transit power analysis. Variable *power_enable_transit_power_analysis* must be set to *TRUE* in order to use this command.

What Next

Set *power_enable_transit_power_analysis* to *TRUE*.

UIPWR-604

(error) Command 'set_current_ground' is only supported in UPF or pre-UPF rail mapping modes.

Description

This command is used for Transit power analysis. Transit power analysis is support in UPF or pre-UPF rail mapping modes.

What Next

Use UPF for pre-UPF rail mapping commands for this feature.

See Also

- create_power_domain
- create_supply_net
- create_power_rail_mapping

UIPWR-605

(error) Rail name is not specified for set_current_ground -rail.

Description

This command is used for Transit power analysis. Transit power analysis is support in UPF or pre-UPF rail mapping modes. In pre-UPF rail mapping mode, a valid design rail name must be specified for set_current_ground -rail.

What Next

Make sure if a valid design rail name is provided for the command.

See Also

- create_power_rail_mapping

UIPWR-606

(error) There is no design rail defined in this design. This command is ignored. Use command create_power_rail_mapping to define design rails.

Description

Power or ground rails in the design can be defined by command create_power_rail_mapping. Then the defined design rail can be used in set_current_ground command to select the rail of interest. To list all the defined rails, use command report_power_rail_mapping.

Feedback

What Next

Type 'man create_power_rail_mapping' for more information

UIPWR-607

(error) There is only one design rail defined in this design. Command set_current_ground has no effect on single rail design. This command is ignored. Use command create_power_rail_mapping to define design rails.

Description

Power or ground rails in the design can be defined by command create_power_rail_mapping. Then the defined design rail can be used in set_current_ground command to select the rail of interest. To list all the defined rails, use command report_power_rail_mapping.

What Next

Type 'man create_power_rail_mapping' for more information

UIPWR-608

(Error) Variable 'power_enable_transit_power_analysis' cannot be set to TRUE in -rail mode.

Description

Variable *power_enable_transit_power_analysis* can be used to enable transit power analysis and reporting capability. This feature is not supported in pt_shell -rail mode.

What Next

Set *power_enable_transit_power_analysis* to *FALSE*.

UIPWR-609

(error) Supply net is not specified for set_current_ground -supply_net.

Description

This command is used for Transit power analysis. Transit power analysis is support in UPF or pre-UPF rail mapping modes. In UPF mode, valid supply net(s) must be specified for set_current_ground -supply_net.

What Next

Make sure if a valid supply net object is provided for the command.

See Also

- create_supply_net

UIPWR-610

(Warning) Simultaneous use of -time and -when options may cause unexpected results. Conditions will be intersected.

Description

When reading the VCD, both the -time and -when options are used to limit the time periods in which power is to be anlyzed. When both -time and -when are used, the only periods in which power is analyzed is during the specified -time windows, AND when the -when condition is true.

What Next

Make sure you wanted the intersection of the conditions. If so, there is no issue. If not, review your use of the options, and refer to the man page.

See Also

- read_vcd

UIPWR-611

(Error) the command report_activity_file_check cannot be used in the backward compatibility mode, or in this power analysis mode

Description

The command report_activity_file_check can be used in the averaged, time_based, or leakage_variation power modes only.

What Next

Change modes, or debug the activity file matching with another method.

See Also

- read_saif
- read_vcd

UIPWR-612

(Error) the command read_vcd does not support file with extention '%s'.

Feedback

Description

The command read_vcd does not support VCD file in .tar, .tar.gz and .tgz format.

What Next

untar the VCD file and run it again.

UIPWR-701

(Error) the command report_clock_gate_savings in DMSA mode does not support this options.

Description

The command report_clock_gate_savings in DMSA mode only support "report_clock_gate_savings -by_clock_gate -sequential"

UIPWR-702

(Error) the command report_power in DMSA mode does not support options '%s'.

Description

The command report_power in DMSA mode following commands are available.

```
report_power
   report_power -include_boundary_nets
   report_power -include_boundary_nets -cell_power -leaf
   report_power -include_boundary_nets -cell_power -net_power -groups
 clock_network -leaf
```

UIPWR-703

(error) Cannot use command option %s under RTL Ananlysis mode.

Description

The listed command option is not allowed to be used in RTL Analysis mode.

What Next

Look at the manpage of this command for more information on command options and their combined usage.

UIPWR-704

(error) Cannot use command option %s since RTL Analysis mode is not enabled.

Feedback

Description

Enable RTL Analysis mode to use the mentioned command option.

What Next

Look at the manpage of this command for more information on command options and their usage.

UIPWR-705

(Error) %s '%s' is currently not supported with Simultaneous Multi Voltage Analysis.

Description

The specified %s '%s' is currently not supported with Simultaneous Multi Voltage Analysis flows.

What Next

Disable Simultaneous Multi Voltage Analysis by setting 'timing_enable_cross_voltage_domain_analysis' to 'false'

UIPWR-801

(error) -time option of report_activity_propagation command is not supported in '%s' power analysis mode. Set power_analysis_mode to '%s' in order to use this option.

Description

You received this error message because variable *power_analysis_mode* has been set to a mode which is not compatible with the use of -time option in report_activity_propagation command.

What Next

Set *power_analysis_mode* to the recommended mode.

See Also

- power_analysis_mode

UIPWR-802

(error) -through_switch option of report_power can only be used with option -rail.

Feedback

Description

You received this error message because option *-through_switch* has been used without option *-rail*.

What Next

Use option *-through_switch* along with -rail option.

UIPWR-803

(error) Provide both valid prefix and separator for multi-bit registers using -adv_mapping_mbit_prefix and -adv_mapping_mbit_separator options of set_power_name_mapping_options command.

Description

You received this error message because valid prefix and separator for multi-bit registers have not been specified.

What Next

Use option *-adv_mapping_mbit_prefix* and *-adv_mapping_mbit_separator* options to provide valid prefix and separator.

UIPWR-804

(Warning) Max no. of nets reported limit is set to 30.

Description

Limit number of nets reported max set to 30 for report_power_capacitance options - detailed and verbose

What Next

report_power_capacitance(2)

UIPWR-805

(warning) (read_saif) Can not find cell

Description

The cell read from saif file cannot be found in the specified design.

What Next

Make sure the SAIF file is created correctly, and the path and strip_path option are given appropriately.

UIPWR-806

(error) '-propagate_through_feedbackloop' can only be specified with '-cells' in command set_power_analysis_options.

Description

You received this error message because command set_power_analysis_options require cells condition to be given with -propagate_through_feedbackloop option.

What Next

Specify cell with propagate_through_feedbackloop option.

UIPWR-807

(error) %s option of read_fsdb can only be used with option %s.

Description

You received this error message because incorrect use of option.

UIPWR-808

(error) Provide both valid space separated string patterns for replacing the string pattern given using -from_pattern option with the string_pattern provided by -to_pattern option of set_power_name_mapping_options command.

Description

You received this error message because valid string arguments have not been provided to -from_pattern and/or -to_pattern option of the set_power_name_mapping_options_command.

What Next

Use option *-from_pattern* and *-to_pattern* options to provide valid string pattern that needs to be replaced and with the string pattern with which it will be replaced.

Feedback

UITE

UITE-100

(error) Design mode configuration '%s' is not defined.

Description

The given design mode configuration is not defined.

What Next

Design mode might be misspelled. Try report_design_modes to find out. To make a new design_mode_configuration, use create_design_mode.

UITE-101

(error) Design mode '%s' is not defined in mode configuration '%s'.

Description

The given design mode configuration does not contain the given mode. If no design modes configuration is specified, the first one is assumed.

What Next

The design mode might be misspelled. Try report_design_mode to find out. The wrong design mode configuration might be assumed.

UITE-102

(error) No design modes have been defined.

Description

No design modes have been defined for the current design.

What Next

To make a design_mode_configuration, use create_design_modes.

UITE-103

(error) Design mode group '%s' is already defined.

Feedback

Description

There is already a design mode group of the specified name.

What Next

To define a different design mode group, choose another name and enter the command again. Once a design mode group is defined, you cannot change it. You must reset all of the design modes and start again.

UITE-104

(error) Input port '%s' not found.

Description

Synchronize_inputs only works on top-level input or inout ports of the current design.

What Next

To find the names of the existing input ports, use report_port.

UITE-105

(error) Port '%s' must be an input or inout port.

Description

Synchronize_inputs only works on the top-level input or inout ports of the current design.

What Next

To find the names of the existing input and inout ports, use report_port.

UITE-106

(Warning) The %s command will be discontinued in future releases. This command has been replaced by %s

Description

A command has been renamed. The old command name is being supported temporarily but will cause syntax errors in future releases

What Next

Use the new command instead of the discontinued command.

Feedback

UITE-107

(error) Cannot set timing derates on a design that is not the current design.

Description

This message is issued if the user has called the set_timing_derate command with a design, which is not the current design, as an argument.

What Next

If the user has intended to operate on the specified design, then set the current design using the current_design command.

See Also

- set_timing_derate
- current_design

UITE-108

(error) the path collection passed to %s contains no path signatures.

Description

The *create_path_tag_set* command saves signatures created in gathering of timing paths into a tagged set. This message is issued when the timing path collection contains no path signatures.

Timing path signatures are created if the variable *enable_path_tagging* is set to *true*. Timing paths gathered when path tagging is disabled contain no signatures required by the *create_path_tag_set* command.

What Next

Redo the path gathering with *enable_path_tagging* set to *true*.

See Also

- create_path_tag_set
- enable_path_tagging

UITE-109

(warning) only %d out of %d paths in the path collection passed to %s contain path signatures.

Feedback

Description

The *create_path_tag_set* command saves signatures created in gathering of timing paths into a tagged set. This message is issued when some of the timing paths in the collection passed as an agrument to the command contains no path signatures.

Timing path signatures are created if the variable *enable_path_tagging* is set to *true*. Timing paths gathered when path tagging is disabled contain no signatures required by the *create_path_tag_set* command.

What Next

Redo the path gathering with *enable_path_tagging* set to *true*.

See Also

- create_path_tag_set
- enable_path_tagging

UITE-110

(Information) %d out of the total %d timing paths were excluded.

Description

You have specified the *-exclude* option with a collection of timing paths passed to *report_timing* or *get_timing_paths*. The *-exclude* option arguments contained path tag names associated with timing paths that should be excluded from the consideration by *report_timing* or *get_timing_paths* command. The informational message shows the number of paths that were excluded from the subsequent path-based analysis or reporting.

What Next

This is an informational message, no action is required.

See Also

- create_path_tag_set
- enable_path_tagging

UITE-111

(Warning) Cannot specify option '%s' with a collection of abstracted timing paths.

Feedback

Description

You have specified an incompatible option with a collection of abstracted timing paths passed to *report_timing*. In the Distributed Multi-Scenario Analysis (DMSA), the *get_timing_paths* command executed at the DMSA manager returns a collection of *slave_timing_path objects. These represent timing paths as printed sub-reports, that is all design and timing data is abstracted away. Each slave_timing_path can only be printed out in the format it was created by get_timing_paths.*

Thus any formatting option passed to *report_timing* has no effect on the report when printing out a collection of abstracted timing paths. In addition, no path based analysis can be performed on a collection of *slave_timing_path objects.*

What Next

Remove incompatible formatting or PBA options to *report_timing*.

See Also

- multi_scenario_enable_analysis

UITE-115

(Error) Reference '%s' '%s' must be a leaf pin or port.

Description

-reference_pin should specify a leaf pin or port on some clock network, i.e. direct or transistive fanout of some clock source given by -clock.

UITE-116

(Error) Edge value of clock '%s' is greater than its subsequent edge values.

Description

The value of each edge must be less or equal than its subsequent edge values. There must be an even number of edges and they are assumed to be alternating rise and fall.

What Next

Use *report_clock* to check for clock information.

UITE-119

(Warning) Clock does not have waveform values monotonically increasing, so waveform has been adjusted.

Feedback

Description

There must be an even number of edges, which are interpreted as alternating rising and falling edges. The edges must be monotonically increasing, except for a special case with two edges specified. When only two edge values are specified and the first value is greater than the second value, it is interpreted as a return-to-one waveform instead of the normal return-to-zero waveform if the falling edge adding one period is still larger than rising edge.

UITE-120

(Error) Invalid waveform. Edges must be an even number of monotonically increasing values less than one period in duration.

Description

The specified clock waveform is not valid.

UITE-121

(warning) Creating virtual clock named '%s' with no sources.

Description

This warning occurs when a virtual clock is created. A virtual clock has a name but no sources. This means it is not applied to any ports or pins in the design. A virtual clock can be used to specify input or output delay.

What Next

The command *create_clock -period 10 -name CLK* does not apply the clock to any sources. If you want to apply the clock to a pin or port, you must specify the pin or port as in *create_clock -period 10 CLK* or *create_clock -period 10 -name CLK ff1/CP*.

UITE-122

(error) The 'create_clock' command cannot be used on output port '%s'.

Description

Clock sources must be input ports or internal pins. Inout ports can be used, but they are not recommended because of bus contention issues.

What Next

Identify a valid set of sources and reapply the *create_clock* command.

Feedback

UITE-123

(warning) Creating a clock source on inout port '%s'.

Description

A circuit, where a clock signal drives an inout port, can be unpredictable. If the port is functioning as an output while the clock is driving, bus contention occurs. If the clock is three-stated, any registers in the fanout of the clock can lose state.

What Next

Verify that the circuit is safe according to your design rules. The PrimeTime product assumes that the clock is valid.

UITE-124

(error) Cannot remove internal path group '%s'.

Description

You cannot use *remove_path_group* to remove internal path groups (such as the default group).

What Next

Reenter the command without the internal path group name.

UITE-125

(warning) Invalid delay direction for port '%s'.

Description

The entered port direction does not match the specifier used. For example, an input port is used with a -to specifier.

What Next

Re-enter the command with valid port directions.

UITE-126

(Error) Unable to %s on path from '%s' to '%s'.

Description

A timing exception command failed to apply or remove information on the specified path.

Feedback

UITE-127

(Information) Found a design with sdf backannotation: (design '%s', file '%s'). Performance will be better by reading the db with -netlist_only and then reading the sdf file with read_sdf.

Description

A design with sdf backannotation was read in from a db file. The performance of PrimeTime will be improved if the design db is read in order to obtain only the netlist (*read_db -netlist_only*), and the sdf data is read from an sdf file using *read_sdf*.

UITE-128

(Error) Unable to set %s on '%s'.

Description

Failed to execute the given set operation on the specified clock.

UITE-129

(Error) Unable to remove %s on '%s'.

Description

Failed to execute the given remove operation on the specified clock.

UITE-130

(warning) Creating a clock on internal pin '%s'.

Description

Clock sources must be input ports. Internal pins can be used, but they are not recommended because they segment your path and prevent slew propagation. PrimeTime restarts slew propagation from the internal clock source pins and reset its value to zero as if the user issued a set_annotated_transition command with a value of zero on the internal clock source pin. You can use the set_annotated_transition command on the clock source pin to set a slew value different than zero.

What Next

Identify a valid set of sources and reapply the *create_clock* command.

Feedback

See Also

- create_clock
- set_annotated_transition

UITE-131

(error) Design mode '%s' is already defined.

Description

There is already a design mode of the specified name.

What Next

Choose a different design mode name and enter the command again, or remove the old design mode with the remove_design_mode command.

UITE-132

(warning) Mode '%s' does not exist on cell '%s'.

Description

There is no mode of the specified name on the cell.

What Next

Use report_mode to determine the valid modes for the cell.

UITE-133

(error) Pin '%s' is not a valid %s.

Description

The specified pin is not a valid timing startpoint or endpoint. Some commands such as set_mode require that the from objects be valid timing startpoints, and the to objects be valid endpoints.

What Next

Use input ports or register clock pins for the from objects, and output ports or register data pins for the to objects.

Feedback

UITE-134

(warning) Creating a %s on multi-driven net '%s', only driverpin '%s' is used as the source.

Description

It is recommended that you use only ports/pins as clock or generated clock sources. Net can be used as clock source, but the effective source used by PrimeTime is the driver pin of the net. If the net is multi-driven, only one of the driver pins is used as the source of the clock.

What Next

Identify a valid set of sources and reapply the *create_clock* or *create_generated_clock* command.

See Also

- create_clock
- create_generated_clock

UITE-135

(error) Creating a %s on net '%s' which does not have a driver pin as real source.

Description

It is recommended that you use only ports/pins as clock or generated clock sources. Net can be used as clock source, but the effective source used by PrimeTime is the driver pin of the net. If the net is multi-driven, only one of the driver pins is used as the source of the clock. If the net does not have a driver pin, the clock will not be correctly created.

What Next

Identify a valid set of sources and reapply the *create_clock* or *create_generated_clock* command.

See Also

- create_clock
- create_generated_clock

UITE-136

(warning) Creating a generated clock on hierarchical pin '%s'.

Feedback

Description

It is recommended that you do not specify a generated clock on a hierarchical design pin.

What Next

Move the generated clock to a leaf driver or load pin on the same net.

See Also

- create_clock
- create_generated_clock

UITE-137

(warning) Creating '%s' on a hierarchical pin '%s'.

Description

Defining a constraint at a hierarchical pin causes the timing arcs (net arcs) from leaf pins driving this pin to leaf pins driven by this pin to be broken. This gives rise to two distinct limitations. First, the hierarchical boundary is a virtual designation and, generally, does not map to a specific physical location. Hence, PrimeTime cannot make any assumptions as to distributing the interconnect delay to the left and right of the bidirectional boundary. Second, breaking the original timing arcs may introduce a loss of timing information. For example, if the hierarchical pin were driven by three leaf pins and drives three other leaf pins, then breaking at the hierarchical boundary would reduce nine timing arcs to six, or worse, three considering the first limitation.

What Next

Move the constraint to a leaf driver or load pin on the same net.

See Also

- create_clock
- set_clock_sense
- set_input_delay
- set_output_delay

UITE-138

(error) Creating '%s' on a hierarchical pin '%s'.

Feedback

Description

Defining a constraint at a hierarchical pin causes the timing arcs (net arcs) from leaf pins driving this pin to leaf pins driven by this pin to be broken. This gives rise to two distinct limitations. First, the hierarchical boundary is a virtual designation and, generally, does not map to a specific physical location. Hence, PrimeTime cannot make any assumptions as to distributing the interconnect delay to the left and right of the bidirectional boundary. Second, breaking the original timing arcs may introduce a loss of timing information. For example, if the hierarchical pin were driven by three leaf pins and drives three other leaf pins, then breaking at the hierarchical boundary would reduce nine timing arcs to six, or worse, three considering the first limitation.

What Next

Move the constraint to a leaf driver or load pin on the same net.

See Also

- create_clock
- set_clock_sense
- set_input_delay
- set_output_delay

UITE-147

(error) Reduced driver pins specified without the corresponding non-reduced driver.

Description

The object list specified contains a reduced driver of a reduced multi-driven net but does not contain the selected non-reduced driver. The implication is that the constraint being specified would not be consumed correctly by the subsequent timing analysis in the presence of the multi-drive reduction capability.

What Next

Please make sure to add the non-reduced driver to the object list. This can be simply achieved by including all drivers of reduced nets. Alternatively, the non-reduced driver can be gotten by accessing the 'non_reduced_driver' application attribute off the reduced net.

See Also

- timing_reduce_multi_drive_net_arcs

Feedback

UITE-150

(warning) Negative clock latency specified: %g

Description

You specified a negative value to *set_clock_latency*. Although this is legal, it is not typical.

What Next

Ensure that you really wanted a negative value.

UITE-200

(error) Must specify %s option along with %s option.

Description

The two options must be together; if one of them is not specified, it is an error.

What Next

Specify both the options together.

UITE-201

(warning) Option '%s' is valid only with option '%s'.

Description

The option specified is valid only if specified along with the other option.

What Next

This option will be ignored, so you can remove this option from the command.

UITE-202

(error) The factor for -MULTIPLY_BY/-DIVIDE_BY '%d' is not a power of two.

Description

The -MULTIPLY_BY or -DIVIDE_BY factor should be a power of two, if not, it is an error.

What Next

If the multiplication factor or division factor is not a power of two, model the clock derivation with -EDGES option.

Feedback

UITE-203

(error) The number of edges specified '%d' is not an odd number larger than or equal to 3.

Description

The number of edges to make one period of the generated clock waveform has to be an odd number larger than or equal to 3.

What Next

Carefully specify edges and ensure that you specify one full clock cycle using the edges.

UITE-204

(error) The number of edge_shifts specified '%d' using '-EDGE_SHIFT' option is not equal to the number of edges specifed '%d' using '-EDGES' option.

Description

The number of edge_shifts specified using the '-EDGE_SHIFTS' option must be equal to the number of edges specified using the '-EDGES' option.

What Next

Make the number of edge_shifts equal to the number of edges.

UITE-205

(error) Expected to find, at most, two numbers along with the option '%s', but found %d.

Description

The options '-MAX_EDGE_DELAY/-MIN_EDGE_DELAY' can have, at the most, two numbers along with each, one for rise and one for fall edge.

What Next

Specify only the rise and fall edge delays.

UITE-206

(error) The clock %s is a generated clock.

Description

A generated clock cannot be removed using 'remove_clock' command.

Feedback

What Next

To remove the generated clocks, use the *remove_generated_clock* command.

UITE-207

(error) A generated clock has already been defined with the name %s.

Description

A generated clock has already been defined with the name you specified.

What Next

Either delete the generated clock and change the name, or change the name of the clock you are defining.

UITE-208

(error) You can specify only a single object for master clock source.

Description

The -source option takes only a single object as an argument.

What Next

You can have a generated clock derived from a single clock. You cannot generate a clock from more than one master clock.

UITE-209

(error) You cannot specify an output port '%s' to be a generated clock master source.

Description

Generated clock master can be an input or inout port or a pin.

What Next

An output port cannot be a generated clock master.

UITE-210

(warning) Creating a generated clock on input or inout port '%s'.

Feedback

Description

When creating a generated clock on an input or inout port, please note that the generated clock would only derive its waveform characteristics from the master clock. Delay, on the other hand, is derived from delay information at the port itself. Additionally, creating a generated clock to drive an inout port can cause unpredictable circuit behavior. If the port is functioning as an output while the clock is driving, bus contention occurs. If the clock is three-stated, any registers in the fanout of the clock can lose state.

What Next

Verify that the circuit is safe according to your design rules. The PrimeTime product assumes the generated clock is valid.

UITE-211

(Error) The -edges spec of generated clock '%s' has edge number less than 1, the edge number should be from 1 up.

Description

The -edge specification in creat_generated_clock command should use edge number of the master clock which should be from 1 up. Zero or negative number are not allowed.

What Next

Change your -edge spec in create_generated_clock coommand.

UITE-212

(Error) In the -edge specification of create_generated_clock '%s', the edge numbers must be in increasing order.

Description

In the -edge specification of a create_generated_clock command, the edge numbers specified must be in increasing order.

What Next

Check the -edge spec in create_generated_clock command and edge numbers increasing.

UITE-213

(Warning) clock port '%s' cannot be assigned input delay relative to clock '%s'. Ignoring the value.

Feedback

Description

When setting an input delay on clock port, it must be specified relative to the same clock. If a different clock is specified, this setting is ignored.

What Next

Remove the unneeded input delay value using the *remove_input_delay* command.

UITE-214

(Information) Updating %-35s

Description

Shows the progress of update timing. The update timing can happen explicitly by calling *update_timing* or implicitly by calling one of the commands that need update timing.

UITE-215

(Warning) Ignoring -significant_digits option with -connections.

Description

Since the output of *report_net* with the *-connections* option formats the output according to the number of significant digits necessary, the *-significant_digits* option is ignored.

UITE-216

(warning) Object '%s' is not a valid %s.

Description

The specified object is neither a valid timing startpoint nor endpoint. Commands such as *set_false_path*, *set_multicycle_path*, and *group_path* require the *-from* option *from_list* objects to be valid timing startpoints and the *-to* option *to_list* objects to be valid timing endpoints.

One important limitation to note is that the call to *update_timing* command may cause the creation of path endpoints at combinational pins. One major example is clock gating checks if the pin connects to the signal gating the clock signal. In that case, entering an exception before an *update_timing* would emit this message, whereas doing so after an *update_timing* would not.

What Next

Use input ports or register clock pins for the *from_list* objects. Use output ports or register data pins for the *to_list* objects.

Feedback

See Also

- group_path
- set_false_path
- set_multicycle_path
- update_timing

UITE-217

(warning) Forcing pin '%s' to be a timing %s.

Description

The specified pin is neither a valid timing startpoint nor endpoint. The *set_max_delay* and *set_min_delay* commands are point-to-point timing exception commands. In this case, these commands override the default single-cycle timing relationship for affected timing paths, so the matched component of each path has a new startpoint (if you specify the *-from* option) and a new endpoint (if you specify the *-to* option). The remaining portions of the path are left unconstrained at the specified pin.

What Next

PrimeTime assumes the behavior described above is intended. If not, use input ports or register clock pins for the *from from_list* objects, and output ports or register data pins for the *-to to_list* objects.

See Also

- set_max_delay
- set_min_delay

UITE-218

(Warning) set_clock_groups overwrote existing false paths.

Description

The *set_clock_groups* command won't analyze the paths between exclusive and asynchronous clocks. Previous manually defined false paths between these exclusive and asynchronous clocks will be removed by *set_clock_groups* command.

What Next

Use the *report_exceptions* command to see the existing false paths. To undo the *set_clock_groups*, use the *remove_clock_groups* command.

See Also

- set_false_path
- set_clock_groups
- remove_clock_groups
- report_exceptions

UITE-219

(warning) Exception overwrites a previous exception of the same type.

Description

The entered exception overwrites a previously entered exception that is of the same type: false path, multicycle path, min or max delay. The overwritten exception uses the same design objects in the specification. Part or all of the former exception will be discarded.

What Next

Make sure that the appropriate exceptions are set to the desired design paths. Note that discarded exceptions will not appear as ignored in report_exceptions.

See Also

- set_false_path
- set_multicycle_path
- set_max_delay
- set_min_delay
- report_exceptions

UITE-220

(information) Design exceptions have been modified.

Description

Some user-entered false paths, multi-cycle paths, min or max delays, were cleaned up by the *transform_exceptions* command. While this clean up removed ignored path specifiers from the original specifications, the design paths utilization of the exceptions is unchanged.

Feedback

What Next

Refer to the man page for *transform_exceptions(2)* for more details.

UITE-221

(error) Transformation options %s are mutually exclusive.

Description

The *transform_exceptions* command options *-remove_ignored*, *-flatten*, *-use_to_for_endpoints* cannot be specified for the same command invocation. Since these are different transformations with different requirements that can be order dependent, the user cannot intermix these transformations.

What Next

Separate the indicated transformation options into separate calls to the *transform_exceptions* command.

UITE-222

(error) The feedback pin '%s' , and the output pin '%s' do not belong to the same PLL.

Description

The feedback pin specified using the *-pll_feedback* and the output pin specified using the *-pll_output* option of *create_generated_clock* command do no belong to the same PLL. Since these pins belong to different cells, there is no valid feedback path for the PLL.

What Next

Define a valid configuration for the PLL, where the feedback pin is connected to an output clock pin on the PLL.

UITE-223

(error) The source pin '%s' does not belong to the PLL cell '%s'.

Description

The master pin specified using the *-source* does not belong to the same PLL to which the feedback pin specified by the *-pll_feedback* belongs. During the defining of a PLL and its feedback path, the master pin specified using the *-source* option should be the reference clock pin of the PLL.

Feedback

What Next

Define a valid configuration for the PLL, where the master pin is the reference clock pin of the PLL.

UITE-224

(error) The clock %s is a generated clock.

Description

A generated clock cannot be used in 'set_clock_jitter' and 'remove_clock_jitter' commands.

What Next

To execute the command, use a *master clock*.

UITE-225

(Information) The -through option for net '%s' is interpreted to imply its load pins.

Description

By default, the net specified by the *-through* option implies the driver pins of the net. If the previous *through_list* in the exception already includes the driver, the net implies its load pins. This is done in order to uniquely specify the exception.

What Next

PrimeTime assumes the behavior described above is intended. If not, replace the net specified by the *-through* option with the appropriate pins.

See Also

- reset_path
- set_false_path
- set_max_delay
- set_min_delay
- set_multicycle_path

UITE-300

(Error) %s '%s' in when expression: '%s' for libcell '%s'.

Description

There was an error while parsing the when expression for the specified library cell. Therefore, the when expression will be ignored.

What Next

The library DB file has not been properly generated.

UITE-301

(Warning) Conflict in specifying '%s' with '%s'. Option '%s' will be used.

Description

The listed command options cause a conflict. The more specific option will be chosen.

What Next

Look at the manpage for this command for more information on command options.

UITE-302

(Warning) Negative clock uncertainty specified: %g

Description

You specified a negative value to set_clock_uncertainty.

Typically, clock uncertainty should be positive. Negative uncertainty values are supported for constraining designs with complex clock relationships. Setting the uncertainty value to a negative number may lead to optimistic timing analysis and should be used with extreme care.

What Next

Ensure that you really wanted a negative value.

UITE-303

(warning) Setting input delay on clock port '%s'. This will not be supported in future releases.

Description

The setting of an input delay on a clock port that does not fanout to a latch D pin is interpreted as clock source latency. However, this feature will not be supported in future releases.

What Next

Use the *set_clock_latency* command with the *-source* option to specifically set clock source latency.

See Also

- remove_clock_latency
- set_clock_latency

UITE-304

(Warning) Setting input delay on clock port '%s', which also has a source latency. Input delay will be ignored.

Description

The setting of an input delay on a clock port that does not fanout to a latch D pin is interpreted as clock source latency. However, the clock also has a defined source latency, so the input delay is ignored.

See Also

- remove_clock_latency
- set_clock_latency

UITE-305

(warning) Converting a propagated clock '%s' to an ideal clock.

Description

The direct setting of a clock network latency on a propagated clock converts it to a ideal clock.

What Next

Verify that this is the intended behavior.

See Also

- remove_clock_latency
- set_clock_latency

Feedback

UITE-306

(Error) The %s command requires all clocks are active.

Description

You receive this error message because there is inactive clocks in the design. The *characterize_context* require all clocks in the design are active.

What Next

To active all clocks in the design, use the *set_active_clocks [all_clocks]* command. To report clock status, use the *report_clock* command.

See Also

- set_active_clocks
- report_clock

UITE-307

(error) Clock %s exists in more than one group.

Description

The *set_clock_groups* command allows each clock can be defined in only one clock group.

What Next

To define multiple groups related to the same clock, use multiple *set_clock_groups* commands.

See Also

- set_clock_groups

UITE-308

(Error) Clock group %s does not exist.

Description

All names must be predefined by the *set_clock_groups*.

Feedback

What Next

Use the *set_clock_groups* command to define clock groups. Use the *report_clock* command with -groups option to see existing clock groups.

See Also

- remove_clock_groups
- set_clock_groups
- report_clock

UITE-309

(warning) Exclusive or asynchronous clock groups specification supersedes set_false_path between clocks.

Description

A preceding *set_clock_groups* command already dictates that paths between some or all clocks specified by the current *set_false_path* exception will not be analyzed. Therefore, the exception will not be entered into PrimeTime and will not show in the output of the *report_exceptions* command.

Note: if the exception specifies more clocks than present in the asynchronous or exclusive groups, then a reduced exception is entered such that this reduced exception is a subset of the original that only specifies clock to clock pairs not in the asynchronous or exclusive groups.

What Next

Use *report_clock -groups* to view the current asynchronous or exclusive clock groups. Use the *remove_clock_groups* command to remove existing clock groups, if desired.

See Also

- remove_clock_groups
- report_clock
- set_clock_groups
- set_false_path

UITE-310

(Warning) CRPR command options will be discontinued in future releases.

Feedback

Description

The user interface to clock reconvergence pessimism removal (CRPR) has changed. The following discontinued options:

-remove_clock_reconvergent_pessimism
-report_clock_reconvergent_pessimism

of the *report_timing*, *report_constraint*, and *get_timing_paths* commands are replaced with the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

In future releases, use of the discontinued options will cause a syntax error.

What Next

Use the new *timing_remove_clock_reconvergence_pessimism* variable instead of the discontinued options. For details on backward compatibility, see the *timing_remove_clock_reconvergence_pessimism* man page.

See Also

- get_timing_paths
- report_constraint
- report_timing
- timing_remove_clock_reconvergence_pessimism

UITE-311

(Error) CRPR command options cannot be used if the design is up to date.

Description

Until the following discontinued options:

-remove_clock_reconvergent_pessimism and
-report_clock_reconvergent_pessimism

of the *report_timing*, *report_constraint*, and *get_timing_paths* commands are completely removed, limited backward-compatibility support is provided: If the design is not up to date, then the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

is automatically set to *TRUE*. If the design is up to date, then the command fails.

Feedback

What Next

Use the new *timing_remove_clock_reconvergence_pessimism* variable instead of the discontinued options. For more detail on backward compatibility, see the *timing_remove_clock_reconvergence_pessimism* variable man page.

See Also

- get_timing_paths
- report_constraint
- report_timing
- update_timing
- timing_remove_clock_reconvergence_pessimism

UITE-312

(Information) Variable timing_remove_clock_reconvergence_pessimism was set to TRUE.

Description

Until the following discontinued options:

```
-remove_clock_reconvergent_pessimism
-report_clock_reconvergent_pessimism
```

of the *report_timing*, *report_constraint*, and *get_timing_paths* commands are completely removed, limited backward-compatibility support is provided. If the design is not up to date, then the following Boolean variable:

timing_remove_clock_reconvergence_pessimism

is automatically set to *TRUE*. If the design is up to date, then the command fails.

What Next

Update your scripts to use the new *timing_remove_clock_reconvergence_pessimism* variable instead of the discontinued command options.

See Also

- get_timing_paths
- report_constraint
- report_timing
- timing_remove_clock_reconvergence_pessimism

Feedback

UITE-313

(Information) '%s' has been renamed to '%s'.

Description

You receive this message because the *-exclusive* option has been renamed to *-logically_exclusive* since *-physically_exclusive* is added.

What Next

Use the *report_clock* with -groups option to check what clock groups have been set.To remove the existing clock groups, use the *remove_clock_groups* command.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

UITE-314

(warning) Converting pin '%s' from propagated to ideal.

Description

Setting a clock network latency on a pin or port directly will convert all the latches in the transitive fanout to ideal if they were marked propagated before.

What Next

Please verify that this is the intended behaviour.

UITE-315

(warning) Converting %s object '%s' from ideal to propagated.

Description

The direct setting of a propagated_clock attribute on a clock, pin, or port can convert all latches in the transitive fanout to propagated. This occurs if they were already marked ideal and had some network latencies set. The user-specified network latencies are removed and can not be recovered. This message is generated if you use the *set_propagated_clock* command on the objects (pin, port or clock) after setting network latencies by using the *set_clock_latency* command on the same objects.

What Next

Verify that this is the intended behavior.

See Also

- remove_clock_latency
- set_clock_latency
- set_propagated_clock

UITE-316

(warning) Virtual clock '%s' cannot be made propagated.

Description

A virtual clock cannot be made propagated as it has no source and does not affect any register in the design.

What Next

Remove the virtual clock from the clock list.

See Also

- remove_clock

UITE-317

(error) Exception is not set because no through objects could be found.

Description

The object list of the exception path is empty at the from, to, or through position. This might happen if the specified object in the command line is a net that does not have any global driver or is a cell with no output pins.

What Next

Verify that this is the intended behavior.

UITE-318

(Warning) Clock groups with same clocks are already set.

Feedback

Description

You receive this warning message because the clock groups you specified are already set by previous command.

What Next

Use the *report_clock* with -groups option to check what clock groups have been set.To remove the existing clock groups, use the *remove_clock_groups* command.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

UITE-319

(warning) Setting clock latency on a non-clock pin or port.

Description

The direct setting of a clock network latency on a non-clock pin or a port converts all latches in the transitive fanout to an ideal clock.

What Next

Verify that this is the intended behavior.

See Also

- remove_clock_latency
- set_clock_latency

UITE-320

(information) Detected %d empty groups, setting up specified relationship among the remaining %d clock groups.

Description

The *set_clock_groups* command sets the specified relationship among the groups of clocks. when there are some groups become empty list due to undefined clocks or incorrect clock names specified for the selection commands, if there are two or more non-empty and valid clock groups remaining, PrimeTime proceeds to set the specified relationships among the remaining valid groups.

Feedback

In prior releases, all the relationships became undefined and ignored for all the clocks and groups in the command.

What Next

Please check to ensure that the clock name specified are correct and the clocks are properly defined before issuing this command. Otherwise, there is no further actions required for the remain valid clocks and groups.

See Also

- set_clock_groups

UITE-321

(error) Detected %d empty groups, failed to set the specified relationship for the remaining one clock group.

Description

The *set_clock_groups* command sets the specified relationship among the groups of clocks. when there are some groups become empty list due to undefined clocks or incorrect clock names specified for the selection commands, if there are less than two non-empty and valid clock groups remaining, PrimeTime discards the command and does not set the specified relationship.

PrimeTime cannot proceed to set the specified relationship because it implies the clocks in the remaining group will become false path against all the other clocks in the design.

What Next

Please check to ensure that the clock name specified are correct and the clocks are properly defined before issuing this command.

See Also

- set_clock_groups

UITE-323

(warning) Comment string ("%s") is ignored.

Description

The comment string argument of the causing constraint command cannot be stored and later output if write_sdc were invoked. In general, a more specific message would be additionally output describing some root cause.

What Next

Address the root cause by correcting the containing SDC file or re-entering the command interactively.

See Also

- write_sdc

UITE-400

(Error) No sequential clock pins in '%s' or its transitive fanout.

Description

You receive this message if you execute *report_clock_timing* with an input pin list (either *from_list* or *to_list*) that does not contain any sequential clock pins, nor any in the pins' transitive fanout. All pins in the *from_list* and *to_list* lists must be sequential clock pins, or must contain them in their transitive fanout.

What Next

Reexecute the *report_clock_timing* command and ensure that all pins in the *from_list* or *to_list* are sequential clock pins, or that they have sequential clock pins in their transitive fanout.

See Also

- report_clock_timing

UITE-401

(Warning) Pins that are not sequential clock pins and contain no sequential clock pins in their transitive fanout have been dropped from '%s'.

Description

You receive this message if the list of input pins submitted to *report_clock_timing* in the *to_list* or *from_list* contains pins that are not sequential clock pins, and do not have sequential clock pins in their transitive fanout. Such pins are not valid inputs to *report_clock_timing*. This message warns you that the offending pins are being omitted from the report.

What Next

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the *report_clock_timing* command, and

Feedback

ensure that all pins on the *from_list* and *to_list* are sequential clock pins, or that they have sequential clock pins in their transitive fanout.

See Also

- report_clock_timing

UITE-402

(Error) No pins specified by the given '%s' belong to the specified clock domains.

Description

You receive this message if you execute *report_clock_timing* and none of the pins on the input pin list (either *from_list* or *to_list*) belong to any of the clock domains specified by *clock_list*. All pins in the *from_list* and *to_list* must be clocked by one of the specified clocks.

What Next

Reexecute the *report_clock_timing* command and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *clock_list*.

See Also

- report_clock_timing

UITE-403

(Warning) Pins specified by the given '%s' that do not belong to the specified clock domains have been dropped from the current %s report.

Description

You receive this message if you execute *report_clock_timing* with an input pin list (either *from_list* or *to_list*), and some of the pins do not belong to any of the clock domains specified by *clock_list*. All pins in the *from_list* and *to_list* must be clocked by one of the specified clocks. This message warns you that the offending pins are being omitted from the report.

What Next

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the *report_clock_timing* command, and ensure that all pins on the *from_list* and *to_list* are clocked by at least one of the clocks in *clock_list*.

See Also

- report_clock_timing

UITE-404

(Error) 'from_list' and 'to_list' contain no pins that are clocked by the same clock; therefore, the skew cannot be reported.

Description

You receive this message if you execute *report_clock_timing* and specify a skew report, but the *from_list* and *to_list*) do not contain any pins clocked by the same clock. Skew reports are produced by *report_clock_timing* only on a per-clock-domain basis. If both *from_list* and *to_list* are specified and *clock_list* is not, the set of clock domains clocking any pin in the *from_list* is intersected with the set of clock domains clocking any pin in the *to_list*. If this intersection is null, the skew report cannot continue.

What Next

Reexecute the *report_clock_timing* command, and ensure that the *from_list* and *to_list* contain pins clocked by the same clock. If you do not specify the *clock_list*, ensure that pins on the *from_list* and *to_list* belong to the same clock domain or set of domains.

See Also

- report_clock_timing

UITE-405

(Warning) Pins have been dropped from '%s', because they are not contained in the clock intersection with '%s'.

Description

You receive this message if you execute *report_clock_timing* and specify a skew report, but the *from_list* and *to_list* contain some pins that are not clocked by the same clock. Skew reports are produced by *report_clock_timing* only on a per-clock-domain basis. If both *from_list* and *to_list* are specified and *clock_list* is not, the set of clock domains clocking any pin in *from_list* is intersected with the set of clock domains clocking any pin in *to_list*. This message warns you that pins in either input list that are not part of any of these derived domains are being removed from the list of pins to report.

What Next

This is a warning message only; no action is required on your part. In general, you can ignore this warning, because the *report_clock_network* command makes it easy to specify

Feedback

a superset of the clock pins of interest; the pruning referred to in this message is helpful to narrow down the superset of clock pins. However, if you have specified pins that you believe are part of a shared clock domain or set of domains, you should investigate why a sink pin in *to_list* is not included in ANY domain implied by *from_list*, or vice versa.

See Also

- report_clock_timing

UITE-406

(Error) No clock pins of '%s' sequential devices found.

Description

A skew report requires a set of clock pins capable of launching data and a set of clock pins capable of capturing data. The combination of *from_list*, *to_list*, and *clock_list* values specified in the *report_clock_timing* command failed to produce these two sets of pins.

What Next

If you specify the *from_list* value, ensure that it contains clock pins of launching sequential devices, either explicitly or in its transitive fanout. If you specify the *to_list* value, ensure that it contains clock pins of capturing sequential devices, either explicitly or in its transitive fanout. If you specify the *clock_list* value, ensure that the clocks have associated networks (that they are not virtual clocks).

See Also

- report_clock
- report_clock_timing

UITE-407

(Error) No clock pins of launching or capturing sequential devices are found.

Description

A latency or transition time report requires a set of clock pins capable of either launching or capturing data. The combination of *from_list*, *to_list*, and *clock_list* values specified in the *report_clock_timing* command failed to produce these pins.

What Next

If you specify the *from_list* or *to_list* value, ensure that they contain clock pins of launching or capturing sequential devices, either explicitly or in their transitive fanout. If you specify

Feedback

the *clock_list* value, ensure that the clocks have associated networks (that they are not virtual clocks).

See Also

- report_clock
- report_clock_timing

UITE-408

(Error) No sequential clock pins in '%s' or its transitive fanout are clocked.

Description

The specified list contains sequential device clock pins, but none of them are clocked.

What Next

The specified input pin list (either the *from_list* or *to_list* value) must be part of the clock network of a defined clock. Check the clock definitions and the scope of their networks and determine if this is true.

See Also

- all_clocks
- create_clock
- report_clock
- report_clock_timing

UITE-409

(Error) No pins specified by the given '%s' belong to the specified '%s'.

Description

You receive this message if you execute an inter-clock skew report using *report_clock_timing* and none of the pins on the input pin list, either *from_list* or *to_list*, belong to the clock domains specified by *from_clock_list* or *to_clock_list* respectively. At least one pin in both *from_list* and *to_list* must be clocked by one of the specified clocks.

What Next

Reexecute the *report_clock_timing* command and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *from_clock_list* and *to_clock_list* respectively.

Feedback

See Also

- report_clock_timing

UITE-410

(Warning) Pins specified by the given '%s' that do not belong to the specified '%s' have been dropped from the current inter-clock skew report.

Description

You receive this message if you execute an inter-clock skew report using *report_clock_timing* and some of the pins on the input pin list, either *from_list* or *to_list*, do not belong to any of the clock domains specified by *from_clock_list* or *to_clock_list* respectively. All pins in the *from_list* and *to_list* should be clocked by one of the specified clocks. This message warns you that the offending pins are being omitted from the report.

What Next

If it is acceptable to you for these pins to be excluded from the report, no action on your part is required. Otherwise, investigate why these were included in the lists of input pins, and make corrections accordingly. Then reexecute the *report_clock_timing* command, and ensure that all pins on the *from_list* and *to_list* are clocked by one of the clocks on the *from_clock_list* and *to_clock_list* respectively.

See Also

- report_clock_timing

UITE-411

(Error) No clock pins of '%s' sequential devices found.

Description

An intre-clock skew report requires a set of clock pins capable of launching data and a set of clock pins capable of capturing data. The combination of *from_list*, *to_list*, *from_clock_list* and *to_clock_list* values specified in the *report_clock_timing* command failed to produce these two sets of pins.

What Next

If you specify the *from_list* value, ensure that it contains clock pins of launching sequential devices, either explicitly or in its transitive fanout. If you specify the *to_list* value, ensure that it contains clock pins of capturing sequential devices, either explicitly or in its transitive fanout. If you specify *from_clock_list* or *to_clock_list*, ensure that the clocks have associated networks (that they are not virtual clocks).

See Also

- report_clock
- report_clock_timing

UITE-412

(Error) Pin '%s' is not the clock pin of a sequential device.

Description

You receive this message if you execute *report_crpr* with an input pin (either *from_pin* or *to_pin*) that is not a sequential clock pin. Both the *from_pin* and *to_pin* must be sequential clock pins.

What Next

Reexecute the *report_crpr* command and ensure that the *from_pin* and *to_pin* are sequential clock pins.

See Also

- report_crpr
- timing_remove_clock_reconvergence_pessimism

UITE-413

(Warning) Searching unconstrained paths will take longer run-time than expected.

Description

The tool will search for unconstrained paths when constrained paths can not be found, which will involve partial update timing, and takes longer time than searching constrained paths.

What Next

It is suggested that all paths in the design get constrained. The potential unconstrained paths may be caused by black boxes, no launching or capturing clocks, empty hierarchy, cells from IP instead of from library, etc. To check constraints in the design, please use the *check_timing* command. Specifing the to_pin_list can also reduce the number of endpoints to search and speed up the report timing process.

Feedback

See Also

- check_timing
- timing_report_status_level
- report_timing
- report_constraint

UITE-414

(Error) CRPR is currently switched off.

Description

This error message is being issued because the user has attempted to use some functionality related to Clock Reconvergence Pessimism Removal (CRPR) when it is not turned on (see the *report_crpr* man page).

What Next

Set the variable, *timing_remove_clock_reconvergence_pessimism* to TRUE and carry out a full update_timing in order to have CRPR included in the timing analysis.

See Also

- report_crpr
- timing_remove_clock_reconvergence_pessimism

UITE-416

(Warning) There %s %d invalid %s.

Description

When *report_timing* is specified with "*" or a cell name, there is possibility that many invalid startpoints or endpoints are gotten, such as *-from [get_pins FF/*]* includes input, output and asynchronous pins. The current behavior for PrimeTime will consider these invalid startpoints or endpoints as through points and continues the path searching. Even though it is convenient to use, it is not suggested since it usually takes longer run time.

What Next

You can use filter to filter redundant or invalid objects, such as *-from [get_pins "FF/* -filter "is_clock_pin == true"]*. You also can use variable *timing_report_always_use_valid_start_end_points* to report using valid startpoints and endpoints only.

Feedback

See Also

- report_timing
- timing_report_always_use_valid_start_end_points

UITE-418

(Error) Could not find latch for pin '%s'.

Description

You receive this error message because the input clock pin (either *from_pin* or *to_pin*) you specified with the *report_crpr* command does not correspond to a sequential device or constrained port. Both the *from_pin* and *to_pin* must be sequential clock pins or constrained ports.

What Next

Reexecute *report_crpr* and ensure that the *from_pin* and *to_pin* are sequential clock pins or constrained ports.

See Also

- report_crpr
- timing_remove_clock_reconvergence_pessimism

UITE-419

(error) Cannot report for start_end_pair, cover_through and cover_design on unconstrained paths.

Description

Reporting using *report_timing -cover_through*, *-start_end_pair* and *-cover_design* can only be performed where there is at least one constrained timing path in the search space implied by the topological specification (*-from*, *-through*, *-cover_through* etc).

What Next

Only perform this form of reporting where the design section searched as implied by the topology specification has at least one constrained path.

UITE-421

(warning) Using the %s option to specify both launching and capturing clocks has been discontinued and will not be supported in future releases.

Feedback

Description

The *report_crpr* command accounts for cases where multiple clocks fan out to the clock pins of sequential devices. To specify the clocks incident on both the launching and capturing devices, use options for the *report_crpr* command.

What Next

After examining the man page, repeat the *report_crpr* command with the relevant options.

See Also

- report_crpr

UITE-422

(warning) -leaf cannot be specified for pins/ports. Ignoring -leaf.

Description

The all_connected command allows -leaf option to be specified for net objects. You are seeing this message because you specified -leaf for pins/ports.

What Next

The command will proceed by ignoring the -leaf. So, you need not do anything.

UITE-423

(error) path_collection cannot be used with any other path search option.

Description

The path_collection is intended to be directly printed according to formatting options specified. No option that need path search, like -nworst, -from, -to etc. can be used with this option.

What Next

Try use only print formatting options with path_collection.

UITE-424

(error) Regular path-based analysis works only when design is in on_chip_variation mode and in worst_slew propagation mode

Feedback

Description

Regular path-based analysis only recomputes paths when the analysis type of the design is set to *on_chip_variation* and slew propagation mode is set to *worst_slew*. When the analysis type is set to *single*, or when the slew propagation mode is set to *worst_arrival*, no recomputed paths are returned.

What Next

Use *set_operating_conditions* to set the design to the *on_chip_variation* analysis mode and/or set the *timing_slew_propagation_mode* variable to *worst_slew*.

UITE-425

(error) Cannot activate modes %s and %s on cell %s as they are in the same mode group %s, no mode has been activated.

Description

It is not possible to activate more than one cell mode in a cell mode group at any one time.

What Next

Select only one cell mode per cell mode group

UITE-426

(error) Cannot perform PBA on unconstrained paths.

Description

Path-based analysis (PBA) only recomputes constrained paths and ignores unconstrained paths, regardless of the value of the variable *timing_report_unconstrained_paths*.

Also, the unconstrained paths will not be returned in the resulting collection.

What Next

Only perform path-based analysis on constrained paths.

UITE-427

(warning) Setting a %s derate on hierarchical net '%s', all other portions of this net will also use this derate factor.

Description

This message is issued if the user has set a net-specific derate factor on a hierarchical portion of a global net. A global net is a net that spans a number of hierarchies.

Feedback

Since PrimeTime will calculate only one delay for the entire global net the derate factor will be set for every net segment (hierarchical portion) in this global net.

What Next

No user action required.

See Also

- set_timing_derate
- report_timing_derate

UITE-429

(Warning) The timing path due to a data check constraint at pin '%s' has not been recalculated.

Description

PrimeTime does not support the path-based recalculation of paths due to data check constraints. These paths are returned directly without recalculation.

See Also

- get_timing_paths
- report_timing
- set_data_check

UITE-430

(warning) Variable timing_report_maxpaths_nworst_reached is suggested to use with timing_report_always_use_valid_start_end_points.

Description

Variable *timing_report_maxpaths_nworst_reached* message may count more endpoints and less max paths if invalid start/through/end points are specified.

UITE-431

(warning) Derate summary report is only shown for full_clock_expanded paths.

Feedback

Description

PrimeTime generates a derate summary report in addition to the timing report when the -derate option has been specified; however this report is only available for *full_clock_expanded* reports.

What Next

To display the derate summary report, specify the *-derate* and *-path_type full_clock_expanded* options on *get_timing_paths* or *report_timing*. If you're not interested in the derate summary report, then no action is needed.

See Also

- get_timing_paths
- report_timing
- set_timing_derate

UITE-432

(warning) The %s variable is obsolete as of the %s release. Do not use this variable as it is no longer supported.

Description

You received this message because you have set the indicated variable to a value other than the default value of the variable.

As of the indicated release of PrimeTime, this variable is obsolete and will no longer be supported in this or subsequent releases. In the indicated release, PrimeTime will honor the setting of this variable and issue this warning message. In subsequent releases, the behavior with default value of this variable will be supported only, and the variable will be removed from PrimeTime.

What Next

Please remove the settings of this variable.

UITE-433

(warning) The %s option is obsolete as of the %s release. Do not use this option as it is no longer supported.

Feedback

Description

You received this message because you have used the indicated option of the command you are running.

As of the indicated release of PrimeTime, this option is obsolete and will no longer be supported in this or subsequent releases. In the indicated release, PrimeTime will honor the usage of this option and issue this warning message. In subsequent releases, the option will be removed from the command that you are running and you will receive an error message when you use the option.

What Next

Please do not use this obsolete option of the command that you are running.

UITE-434

(warning) The %s option is obsolete as of the %s release. Do not use this option as it is no longer supported.

Description

You received this message because you have used the indicated option of the report_timing or get_timing_paths command.

As of the indicated release of PrimeTime, this option is obsolete and will no longer be supported in this or subsequent releases. In the indicated release, PrimeTime will honor the usage of this option and issue this warning message. In subsequent releases, the option will be removed from the command that you are running and you will receive an error message when you use the option.

This variable is obsolete and replaced with the usage of the variable timing_enable_preset_clear_arcs. By setting the value of this variable to the non-default value, you can obtain the same effect as with this obsoleted option. You will, however, incur the CPU cost of a full update when the value of the variable is changed. In order to minimize the CPU cost, please do not change the value of the variable frequently.

What Next

Please set timing_enable_preset_clear_arcs variable to true instead.

UITE-435

(Information) %s

Feedback

Description

Display messages when the *timing_report_maxpaths_nworst_reached* variable is set to *true*.

UITE-436

(warning) Resetting a %s derate on hierarchical net '%s', all other portions of this net will also use this derate factor.

Description

This message is issued if the user has reset a net-specific derate factor on a hierarchical portion of a global net. A global net is a net that spans a number of hierarchies.

Since PrimeTime will calculate only one delay for the entire global net the derate factor will be reset for every net segment (hierarchical portion) in this global net.

What Next

No user action required.

See Also

- reset_timing_derate

UITE-437

(warning) Implicitly setting the '%s' option for the set_timing_derate command.

Description

This message is issued if the user has called the set_timing_derate command with an object_list and has not explicitly set one of the net_delay, cell_delay or cell_check options.

What Next

Explicitly specify one of the net_delay, cell_delay or cell_check options. The net_delay and cell_delay options may be specified together.

See Also

- set_timing_derate

UITE-438

(error) The *set_timing_derate* command must use the *-net_delay*, *-cell_delay*, or *-cell_check* option when the *object_list* contains a hierarchical cell.

Feedback

Description

In general, by default, the *set_timing_derate* command derates cell delays and net delays, and not cell timing checks. However, when the command operates on a hierarchical cell, you must explicitly specify the derating type by using one or more of the options *-net_delay*, *-cell_delay*, or *-cell_check*.

What Next

Run the *set_timing_derate* command again and specify the types of derating to perform: *-net_delay*, *-cell_delay*, or *-cell_check*. To derate both net delays and cell delays in hierarchical cells, use both *-net_delay* and *-cell_delay*.

See Also

- report_timing_derate
- set_timing_derate

UITE-445

(Information) %s

Description

Display messages when the *timing_report_maxpaths_nworst_reached* variable is set to *true*.

UITE-446

(Warning) Enabling Clock Reconvergence Pessimism Removal (CRPR).

Description

This message is being issued because the user has enabled the adaptive CRPR engine (turned on by setting *timing_crpr_enable_adaptive_engine* to TRUE) when CRPR is turned off. The adaptive engine will only function when CRPR is turned on, hence CRPR has been enabled automatically.

See the man page for *timing_crpr_enable_adaptive_engine* for more details.

What Next

Update scripts to set the variable *timing_remove_clock_reconvergence_pessimism* to TRUE.

See Also

- timing_remove_clock_reconvergence_pessimism

UITE-447

(Warning) Derate summary report may not match the output of report_timing without timing derates applied.

Description

This warning message is issued when the *report_timing* command has been called with the '-derate' option when the design has derate and signal integrity data and signal integrity analysis is enabled.

The derate summary report may not match the output of report_timing when there are no timing derates applied. Application of derates to aggressor nets will widen arrival windows thus making crosstalk interaction more likely. These additional crosstalk effects appear in the output of report_timing with derates applied. A full analysis with no derating applied would be required to remove these additional crosstalk effects.

If CRPR is on, then the clock reconvergence pessimism (due to derating) in the derate summary report shows the amount of CRP removed due to the static effect of derating. It is not possible to remove the additional crosstalk effects arising from derating.

What Next

Reset the timing derates using the *reset_timing_derate* command and use report_timing to determine the effect of removing timing derates.

See Also

- report_timing
- reset_timing_derate
- timing_remove_clock_reconvergence_pessimism

UITE-448

(Warning) Unrealistically large derate value specified: %g

Description

This warning message is issued when the *set_timing_derate* command has been called with a derate value greater than 2. If *-increment* option is used then the ranage is from -1 to +1.

Feedback

A derate factor greater than a range of 2.0 is unrealistically large. As a consequence, the values shown in the Derate Summary Report in the *report_timing* output may not be accurate.

What Next

It is likely that the specified derate value is incorrect, because of a user input error. Please specify a more realistic derate factor within the range [0 to 2], or [-1 to +1] if *-increment* option is used.

See Also

- report_timing
- set_timing_derate

UITE-450

(Warning) Transferring ideal net attribute onto driver pin '%s' of net '%s'.

Description

This warning message occurs when the set_ideal_network command is called with nets specified in the object_list.

If a net is ideal then all it's driver pins must be ideal. The ideal network attribute is transferred from the specified net to the global driver pins of that net.

What Next

No action is required.

See Also

- set_ideal_network

UITE-451

(Warning) Ignoring hierarchical pin '%s'. Object must be a port, net or pin of a leaf cell.

Description

This warning message occurs when the set_ideal_network command is called with a hierarchical pin in the object_list. You cannot specify a hierarchical pin as an ideal network start point.

PrimeTime ignores the hierarchical pin specified in the warning message, but continues to set ideal networks on any remaining valid objects in the object_list.

What Next

Specify only ports, nets or pins of leaf cells in the object_list. A leaf cell is a cell that does not contain other cells.

See Also

- set_ideal_network

UITE-452

(Warning) Ignoring net '%s' because the 'no_propagate' option is not specified.

Description

This warning message occurs when the set_ideal_network command is called with nets specified in the object_list and the 'no_propagate' option has not been specified.

What Next

To set a net ideal use the 'no_propagate' option.

See Also

- set_ideal_network

UITE-453

(Warning) Overwritting previous ideal network that was set on pin '%s'.

Description

This warning message occurs when the user sets an ideal network on a pin, which already has an ideal network set on it. The previous ideal network that was set on the pin is overwritten with this ideal network set on the pin.

What Next

No action is required.

See Also

- set_ideal_network

UITE-454

(Warning) Ignoring hierarchical pin '%s'. Object must be a port or pin of a leaf cell.

Feedback

Description

This warning message occurs when the set_ideal_latency command or set_ideal_transition command is called with a hierarchical pin in the object_list. You cannot annotate ideal timing values on a hierarchical pin.

PrimeTime ignores the hierarchical pin specified in the warning message, but continues to set ideal values on any remaining valid objects in the object_list.

What Next

Specify only ports or pins of leaf cells in the object_list. A leaf cell is a cell that does not contain other cells.

See Also

- set_ideal_network
- set_ideal_latency
- set_ideal_transition

UITE-455

(Warning) Removing ideal attribute from driver pin '%s' of net '%s'.

Description

This warning message occurs when the remove_ideal_network command is called with nets specified in the object_list.

If a net is ideal then all it's driver pins must be ideal. The ideal network attribute is transferred from the specified net to the global driver pins of that net.

What Next

No action is required.

See Also

- remove_ideal_network

UITE-456

(Warning) Ideal timing is specified on the non-ideal %s.

Feedback

Description

This warning message occurs if the user has annotated ideal latency and/or ideal transition values on a pin or port that is not part of an ideal network. The annotated ideal timing values will only take effect if the object is part of an ideal network.

What Next

If you intend to apply the annotated ideal timing values, then set an an network on the pin or port using the set_ideal_network command.

If you do not intend to apply annotated ideal timing values on the object, then remove the annotated ideal timing values using the remove_ideal_latency command and/or the remove_ideal_transition command.

See Also

- set_ideal_network
- set_ideal_latency
- set_ideal_transition
- remove_ideal_latency
- remove_ideal_transition

UITE-457

(Error) '%s' and '%s' are already defined as '%s' not allowing paths.

Description

You receive this error message because the *-allow_paths* defined by asynchronous clock groups is conflict with false path set by either the asynchronous, physically exclusive or logically exclusive clock groups for the same clock pair.

What Next

Use the *report_clock* with -groups option to check what clock groups have been set.To remove the existing clock groups, use the *remove_clock_groups* command.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

Feedback

UITE-458

(Error) '%s' and '%s' are already defined as -allow_paths in asynchronous clock groups.

Description

You receive this error message because the clock pair is already defined as asynchronous clock relationships which allow paths between these two clocks.

What Next

Use the *report_clock* with -groups option to check what clock groups have been set.To remove the existing clock groups, use the *remove_clock_groups* command.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

UITE-459

(Error) Reference pin '%s' is not reached by any clock.

Description

You receive this error message because the input or output delay you defined on a pin or port with respect to a reference pin, which is not a fanout of any clock network. In case of no clock propagates to reference pin, the defined input/output delay will be ignored.

What Next

It is suggested that reference pin for input/output delay constraints should be in the fanout of clock network. Please verify the connection of reference pin and modified the reference pin if needed.

See Also

- set_input_delay
- remove_input_delay
- set_output_delay
- remove_output_delay

Feedback

UITE-461

(Error) Generated clock '%s' '%s' is not satisfiable%s

Description

This is an error message whenever the clock network traversal can not find a path which satisfies the sense relationship defined by create_generated_clock command.

What Next

Check for the generated clock definition to see if the generated clock is correctly defined. One example is that a divided_by 2 generated clock is driven by a inverter only. In this case, generated clock should be redefined with -invert with -divided_by 1. Another example is a divided_by 2 generated clock with preinverting. If master clock source pin is used as generated clock source pin, PrimeTime will issue the warning message. In this case, generated clock source pin should be redefined to clock pin of divider.

UITE-462

(Error) No constant bounding derates have been defined.

Description

You have received this message because you have attempted to perform a path-based AOCVM analysis using either the *report_timing* command or the *get_timing_paths* command, but no constant timing derates have been defined.

Constant derates are required to pessimistically bound derates calculated during a path-based AOCVM analysis. PrimeTime aborted the AOCVM analysis, because there are no constant derates and so there is no OCV pessimism for AOCVM to remove.

What Next

Define constant bounding derates using the *set_timing_derate* command. Alternatively, consider using the graph-based AOCVM analysis, which *automatically* determines tight non-optimistic bounding derates for the path-based AOCVM analysis.

See Also

- report_timing
- get_timing_paths
- set_timing_derate
- report_timing_derate
- timing_aocvm_enable_analysis

Feedback

UITE-463

(Error) No AOCVM derate factors have been defined. PrimeTime cannot continue with AOCVM analysis.

Description

You have received this message because you have attempted to perform an AOCVM analysis, but no AOCVM derate factors have been defined. An AOCVM analysis requires AOCVM derate factors.

AOCVM derate factors are specified using the *read_aocvm* command.

What Next

Either define AOCVM derate factors using the *read_aocvm* command.

See Also

- read_aocvm
- report_aocvm

UITE-464

(Warning) No coordinates locations have been defined; AOCVM analysis may be inaccurate.

Description

You have received this message because you have attempted to perform an AOCVM analysis, but no coordinates locations have been defined.

Coordinates locations are used to calculate the systematic component of an AOCVM derate factor. The coordinates of various nodes of nets, pins, and ports are imported into PrimeTime from parasitic files using the *read_parasitics* command.

PrimeTime will continue with the AOCVM analysis and assume the most pessimistic coordinates locations possible.

What Next

Set the *read_parasitics_load_locations* variable to *true* and read parasitics using the *read_parasitics* command.

Feedback

See Also

- report_timing
- get_timing_paths
- read_parasitics
- read_parasitics_load_locations

UITE-465

(Warning) No clock paths found. Advanced on-chip variation requires a 'full_clock_expanded' path for an accurate analysis.

Description

You have received this message because you have attempted to perform an advanced on-chip variation analysis on a path, but the clock path has not been included.

PrimeTime will continue with the advanced on-chip variation analysis; however, the analysis might be inaccurate due to the lack of information.

What Next

Use the *get_timing_paths* command with the *-path_type* option to obtain a path with its associated clock path.

See Also

- get_timing_paths
- report_timing

UITE-466

(Warning) Ignoring hierarchical cell '%s'. Object must be a leaf cell or a library cell.

Description

This warning message occurs when the set_aocvm_coefficient command is called with a hierarchical cell in the object_list. You cannot annotate AOCVM coefficients on a hierarchical cell.

PrimeTime ignores the hierarchical cell specified in the warning message, but continues to set AOCVM coefficient values on any remaining valid objects in the *object_list*.

What Next

Specify only leaf cells or library cells in the *object_list*. A leaf cell is a cell that does not contain other cells.

See Also

- set_aocvm_coefficient
- report_aocvm

UITE-467

(Error) AOCVM and Variation-Aware analyses are mutually exclusive; PrimeTime will disable the AOCVM analysis.

Description

You have received this message because you have attemtped to perform an AOCVM analysis and a Variation-Aware analysis together. The analyses cannot be performed together.

What Next

If you intend to perform a Variation-Aware analysis only, then no action is required.

If you intend to perform an AOCVM analysis, then you must disable Variation-Aware analysis, which is controlled using the PrimeTime variable *variation_enable_analysis*.

See Also

- get_timing_paths
- report_timing
- timing_aocvm_enable_analysis

UITE-468

(Information) The CRP value reported by report_timing and report_clock_timing will be %s.

Description

You are receiving this message because the *report_crpr* command has detected that its corresponding *report_timing* (or *report_clock_timing*) command is using a smaller CRP value. The *report_crpr* command reports the exact CRP value whereas *report_timing* (and *report_clock_timing*) use values calculated considering the CRPR threshold.

Feedback

This difference is a product of performance optimizations that are outlined in the next paragraph.

In order to prevent performance degradation during *update_timing*, CRPR groups sequential devices with similar CRP values (i.e. the difference between the CRP values is within the value of the crpr threshold). This can lead to some paths using a CRP value that will be smaller than the exact CRP. The difference between the two will be bounded by the value of the CRPR threshold.

What Next

In order to align the CRP values used by *report_timing*, *report_clock_timing* and *report_crpr* the crpr threshold may be set to a smaller value. It should be noted that this can cause significant performance degradation during subsequent timing updates.

See Also

- timing_crpr_threshold_ps

UITE-469

(Error) Unable to set %s on '%s'.

Description

Failed to execute the given set operation on the specified object.

UITE-472

(Error) You cannot specify the -aocvm_guardband option of set_timing_derate in the derate_list of the timing_aocvm_derate_list variable.

Description

You have received this message because you have attempted set guardband derate factors using the *-aocvm_guardband* option of the *set_timing_derate* command in the *derate_list* of the *timing_aocvm_derate_list* variable.

What Next

Remove the *-aocvm_guardband* option.

See Also

- set_timing_derate

Feedback

UITE-473

(Error) You cannot specify the -aocvm_guardband option of set_timing_derate in the pba_derate_list variable.

Description

You have received this message because you have attempted set AOCVM guardband derate factors using the *-aocvm_guardband* option of the *set_timing_derate* command in the *pba_derate_list* variable. This usage is not permitted.

What Next

Remove the *-aocvm_guardband* option.

See Also

- set_timing_derate

UITE-474

(Warning) The option '%s' is now the default and will be removed from the UI in a later release. You can use '%s' to get the old default behavior.

Description

You have received this message because you have issued an option that is now the default option on the command and will be removed from the UI in a later release.

What Next

Remove the option for future.

UITE-476

(Error) Graph-based AOCVM analysis must be performed in 'on_chip_variation' mode.

Description

You have received this message because you have attempted to perform graph-based AOCVM analysis in the 'single' or 'bc_wc' analysis mode, which is not supported.

What Next

Use the *set_operating_conditions* command to set the design into 'on_chip_variation' mode.

See Also

- report_design
- set_operating_conditions
- timing_aocvm_enable_analysis

UITE-477

(Error) Graph-based delay-weighted AOCVM analysis cannnot be performed in worst_arrival mode.

Description

You have received this message because you have attempted to perform graph-based AOCVM analysis in the delay-weighted analysis mode, but the design is in worst_arrival mode.

What Next

Set the *timing_slew_propagation_mode* variable to "worst_slew" and set the *si_xtalk_delay_analysis_mode* variable to "all_paths" if you want to perform graph-based AOCVM analysis in the delay-weighted analysis mode.

See Also

- si_xtalk_delay_analysis_mode
- timing_aocvm_analysis_mode
- timing_aocvm_enable_analysis

UITE-478

(Error) Graph-based delay-weighted AOCVM analysis cannnot be used when the si_use_driving_cell_derate_for_delta_delay variable is set to true.

Description

You have received this message because you have attempted to perform graph-based AOCVM analysis in the delay-weighted analysis mode, but the *si_use_driving_cell_derate_for_delta_delay* variable is set to *true*.

What Next

Set the *si_use_driving_cell_derate_for_delta_delay* variable to *false* if you want to perform graph-based AOCVM analysis in the delay-weighted analysis mode. Otherwise, if you

Feedback

need to use the *si_use_driving_cell_derate_for_delta_delay* variable, turn off graph-based AOCVM using the *timing_aocvm_enable_analysis* variable.

See Also

- si_use_driving_cell_derate_for_delta_delay
- timing_aocvm_analysis_mode
- timing_aocvm_enable_analysis

UITE-479

(Warning) Exhaustive path-based analysis may take a long time using the current PrimeTime settings. Try using the following settings, which may reduce the runtime of the analysis:%s

Description

You have received this message because you have attempted to perform an exhaustive path-based analysis using settings that may considerably degrade the runtime of the analysis.

What Next

The warning message suggests settings that should be changed to improve the runtime of the analysis.

See Also

- report_timing
- get_timing_paths
- pba_derate_only_mode
- timing_aocvm_analysis_mode
- timing_aocvm_enable_analysis
- timing_remove_clock_reconvergence_pessimism
- timing_report_use_worst_parallel_cell_arc

UITE-480

(Warning) The exhaustive path-based recalculation limit of %d has been exceeded at endpoint '%s' and group '%s'. The worst PBA slack found at this endpoint was %g. The

Feedback

worst GBA slack of the remaining paths not recalculated is %g. It is known that no PBA paths exist with worse slack than this worst GBA slack at this endpoint for this group.

Description

You have received this message because the user specified path-based endpoint recalculation limit has been met during an exhaustive search for worst paths at this endpoint. This message gives details on the endpoint that has not been exhaustively searched.

What Next

Exhaustive path recalculation is a last mile analysis technique and as a result it should only be used when the design is close to signoff. Try to recalculate the endpoint using conservative values for slack_lesser_than, nworst and max_paths.

Increasing the user specified path-based endpoint recalculation limit may allow the endpoint to be exhaustively searched, however this will increase the runtime of the analysis.

See Also

- report_timing
- get_timing_paths
- pba_exhaustive_endpoint_path_limit
- timing_aocvm_analysis_mode

UITE-482

(Error) Cannot specify a value for nworst (%d) greater than the path-based recalculation limit (%d) unless pba_path_recalculation_limit_compatibility is false. Setting nworst to %d.

Description

You have received this message during a path-based recalculation. A path-based limit applies during this analysis and the user specified nworst value cannot exceed this limit.

Unless gba paths are to be mixed with pba paths in the results, it is not permitted to set an nworst larget than the recalculation limit per endpoint.

What Next

Set a conservative value for nworst. If necessary increase the path-based endpoint recalculation limit, however this will increase the runtime of the analysis.

See Also

- report_timing
- get_timing_paths
- pba_exhaustive_endpoint_path_limit
- timing_aocvm_analysis_mode

UITE-485

(Warning) Cannot set %s delay on a clock port (%s) that does not fanout to any data sink.

Description

A *set_input_delay* or *set_output_delay* command was applied to this clock port. However, this port has no data sinks, so the input or output delay is not applied to this port. To specify clock latency instead of data input or output delays, use the *set_clock_latency* command instead.

What Next

Use the *set_clock_latency* command with the *-source* option to set clock source latency at a port. If a data sink is expected in the fanout of this port, check the design.

See Also

- remove_clock_latency
- set_clock_latency

UITE-486

(Error) Cannot specify a value for the pba_derate_list variable in an AOCVM context.

Description

You have received this message because you attempted to perform a path-based AOCVM analysis and you specified a value for the *pba_derate_list* variable.

What Next

To perform a path-based AOCVM analysis, set the *pba_derate_list* variable to "". Otherwise, to use the derates specified in the *pba_derate_list* variable, you must remove all AOCVM information using the *remove_aocvm* command.

Feedback

See Also

- get_timing_paths
- report_timing
- remove_aocvm

UITE-487

(Warning) AOCVM path-based analysis can take a long time if path-specific slew propagation is also performed.

Description

The *-pba_mode* option on *report_timing* (and *get_timing_paths*) instructs PrimeTime to perform both AOCVM PBA and regular PBA (path-specific slew propagation). The analysis runtime is significantly improved if only AOCVM path-based analysis is performed.

This message is only displayed once per session.

What Next

If you intended to perform AOCVM and regular path-based analyses, then no action is required.

If you intended to perform only AOCVM path-based analysis, then set the *pba_derate_only_mode* variable to true.

See Also

- report_timing
- get_timing_paths
- pba_derate_only_mode

UITE-488

(warning) Setting input delay on clock port ('%s') that has data sink(s). The behavior will change in future releases.

Description

The setting of an input delay on a clock port that has data sink(s) is also interpreted as clock source latency. However, this feature will not be supported in future releases.

What Next

Use the *set_clock_latency* command with the *-source* option to specifically set clock source latency.

See Also

- remove_clock_latency
- set_clock_latency

UITE-489

(Warning) Setting input delay on clock port (%s) relative to a clock (%s) defined at the same port. Command is ignored.

Description

The tool ignores the setting of an input delay on a clock port relative to a clock defined at the same port. The same signal at the port cannot be delayed relative to itself.

What Next

Review the constraints. You can set the input delay at the clock port if it is relative to a clock defined at another port.

See Also

- remove_clock_latency
- set_clock_latency
- set_input_delay

UITE-490

(Warning) The setting of variable '%s' will be ignored when the mode of operation is defined by setting variable '%s' to '%s'.

Description

You received this message because you have set the indicated variable to a value other than its default value when PrimeTime is in the indicated mode of operation.

PrimeTime will honor the setting of this variable and issue this warning message, but the analysis will assume the variable with its default setting under the above mode of operation. Changing the mode of operation will use the current setting of the variable.

What Next

Please remove the setting of this variable to its non-default value in the above mode of operation or perform the analysis with a different mode of operation.

See Also

- timing_ideal_clock_zero_default_transition
- si_xtalk_delay_analysis_mode

UITE-491

(Warning) Timing paths have not been obtained with -path_type full_clock_expanded.

Description

You have received this message because you have attempted to perform path-based analysis with the pba_recalculate_full_path variable set to true, but some or all of the paths passed into the command were not obtained with "-path_type full_clock_expanded".

PrimeTime will continue with recalculation, however timing information on any missing clock paths will come from GBA.

What Next

Use the *get_timing_paths* command with the "-path_type full_clock_expanded" option to obtain timing paths with their associated clock paths.

See Also

- get_timing_paths
- report_timing

UITE-493

(Warning) This design has derates set on both library cells and hierarchical cells, and the precedence rules of applying timing derates are changed.

Description

Starting from D1006 release, derate factors are applied in the following priority order (in decreasing order of precedence):

```
1) Leaf Cell
2) Library Cell
3) Hierarchical Cell
4) Design
```

Feedback

The change in D1006 release is the priority of library cell is no longer sandwiched between hierarchical cell and design. To use the old behavior, set variable *timing_derate_precedence_compatibility* to true.

See Also

- set_timing_derate

UITE-494

(warning) Setting %s derate factor to 0.0 on %s object %s as the calculated derate factor is negative (%s).

Description

This message is issued if the total calculated derate factor of an object, calculated by adding non-incremental and incremental derates is less than zero.

Since negative derates can result in negative delays, PrimeTime converts negative derate factors to 0.

What Next

Fix the script to avoid negative total derate factors.

See Also

- set_timing_derate
- report_timing_derate

UITE-495

(Error) The %s option to report_constraint requires that a %s hierarchical flow type analysis is being performed.

Description

This message is issued when *report_constraint* is issued with an option that is only compatible with certain hierarchical flow types.

UITE-496

(error) Ignoring the set_aocvm_parameters command.

Feedback

Description

This message is issued if the user has called the set_aocvm_parameters command with an object_list and has not explicitly specified one of depth or distance options.

What Next

Explicitly specify one of the depth or distance options. The depth and distance options may be specified together.

UITE-497

(error) Object '%s' is not a %s. Command being ignored on this port.

Description

The specified object is not a port. The command is currently supported only on input, output and inout ports.

What Next

Investigate why the command is being specified on objects that are not ports.

UITE-498

(error) Invalid set_aocvm_parameters specifier %s for %s port '%s'. Command being ignored for the specific port.

Description

The specified direction for the set_aocvm_parameters command does not match the port direction. For example, an input port is used with a -output specifier.

What Next

Re-enter the command with valid port directions.

UITE-499

(Information) Performing logical update.

Description

Shows the progress of logical update timing. This is a partial timing update that computes clock and constant propagation paths, but does not perform delay calculation. Logical

Feedback

updates are incurred by commands that need to know the logical state of the design, but do not need timing information. Some examples of such commands are:

- **all_registers -clock**
- **all_fanin**
- **all_fanout**
- **get_attribute** (for some non-timing attributes)

A logical update is performed by the commands (such as those given above) if the design has never been updated at all, or if a command that changes the state of the design has been applied since the last update, which causes another update to become pending. Some examples of commands that change the design state and cause a pending update are:

- **set_case_analysis**
- **remove_case_analysis**
- **create_clock**
- **set_disable_timing**
- **set_disable_clock_gating_check**
- **set_input_delay**
- **set_output_delay**
- **set_clock_latency**

See Also

- update_timing

UITE-500

(Information) The group %s does not reach -max_paths.

Description

This informational message is displayed during *report_timing* when insufficient paths are found for the group to satisfy the maximum number of paths specified.

The message is only displayed when the *timing_report_maxpaths_nworst_reached* variable is set to *true*.

UITE-501

(Warning) set_input_delay does not permit min_%s value %g to be greater than max_%s value %g at pin or port %s. Both values will be set to %g.

Feedback

Description

For external delays, the early arrival must occur before the late arrival. Attempting to set an early arrival after a late arrival, or attempting to set a late arrival before an early arrival, results in this warning.

This message is only a warning. The values are adjusted so that the early and late arrivals are the same, and analysis can continue.

See Also

- set_input_delay

UITE-502

(Warning) report_timing has satisfied the max_paths criteria. There are %d further endpoints which have paths of interest with slack less than %s that were not considered when generating this report.

Description

This message indicates that the *report_timing* algorithm has succeeded in finding max_paths number of paths and that there are further endpoints with paths of interest.

What Next

To see all paths of interest, increase max_paths.

See Also

- report_timing

UITE-503

(Warning) The max_paths value of %d passed to the %s command has exceeded the max_paths limit. The command will continue using the max_paths limit of %d.

Description

The max_paths limit has been exceeded.

What Next

Issue multiple reporting commands. Each reporting command should focus on a portion of the path search space. The path search space can be defined with the -from/-through/-to/-group options.

Feedback

See Also

- get_timing_paths
- report_timing

UITE-504

(Warning) Input delays set without the -clock option will not create constrained paths to clocked registers.

Description

There is no default clock associated with unclocked input delays created using *set_input_delay* without the *-clock* option. As a result, constrained paths are not created from the port to clocked registers in the fanout of the port.

What Next

Use the *set_input_delay* command with the *-clock* option to specify the clock related to the input delay.

Alternately, the *timing_input_port_default_clock* variable to create a default clock on these input delays, which was the behavior of PrimeTime before version F-2011.12.

See Also

- timing_input_port_default_clock

UITE-505

(Warning) The report_timing variable timing_report_maxpaths_nworst_reached is no longer supported.

Description

From the 2011.12 release onwards, *report_timing* has been enhanced to better report when *max_paths* has been satisfied so this variable is no longer needed.

What Next

Look for the UITE-502 message which will be issued when max_paths has been satisfied and will indicate how many further endpoints have paths of interest.

UITE-507

(Error) pin '%s' is not a D-pin of a transparency latch.

Feedback

Description

You receive this error message because the pin you specified with the does not correspond to the D-pin of a transparency latch.

What Next

Reexecute *set_latch_loop_breaker* and ensure that the D-pin entered corresponds to the D-pin of a transparency latch.

UITE-508

(Warning) User-defined latch-loop-breaker attrtibutes (avoid|set) on pin '%s' have not been defined. No user-defined latch-loop-breaker attribute for the pin is removed.

Description

This message is displayed when the user tries to remove the user-defined latch-loop-breaker attributes for the data pins of transparency latches which have not been previously defined.

UITE-509

(Warning) The command 'set_aocvm_parameters' is only supported in graph-based analysis (GBA) mode. Current, there is no support in path-based analysis (PBA) mode.

Description

You have received this message because *set_aocvm_parameters* has been specified by the user. This command is only supported in graph-based analysis (GBA) mode. Currently, there is no support in path-based analysis (PBA) mode.

See Also

- read_aocvm
- report_aocvm

UITE-510

(warning) Converting latch loop breaker pin '%s' to -to pin for timing report

Description

You are receiving this message because you have issued a report_timing command a through list (specified with -through) that includes a pin that has been defined as a latch loop breaker.

Feedback

This command should only be issued if timing_enable_through_paths is set to true.

In this case it is not possible to using such pins as through pins in a timing report and it will instead be converted to a -to pin.

What Next

It is recomended that the timing reports be reviewed to remove these -through pins and also to ensure that no timing paths are being missed. It is also possible to specify a latch loop breaker pin using the command set_latch_loop_breaker.

See Also

- timing_enable_through_paths
- set_latch_loop_breaker

UITE-511

(Error) No POCVM derate factors have been defined. PrimeTime cannot continue with POCVM analysis.

Description

You have received this message because you have attempted to perform an POCVM analysis, but no POCVM derate factors have been defined. A POCVM analysis requires POCVM derate factors.

POCVM derate factors are specified using the *read_aocvm* command.

What Next

Either define POCVM derate factors using the *read_aocvm* command.

See Also

- read_aocvm
- report_aocvm

UITE-512

(Error) No POCVM derate factors have been defined. PrimeTime cannot continue with POCVM analysis.

Feedback

Description

You have received this message because you have attempted to perform an POCVM analysis, but no POCVM derate factors have been defined. An POCVM analysis requires POCVM derate factors.

POCVM derate factors are specified using the *read_aocvm* command.

What Next

Define POCVM derate factors using the *read_aocvm* command.

See Also

- read_aocvm
- report_aocvm

UITE-513

(Error) Pins specified with this command must be transparent latch data pins.

Description

The get_latch_loop_groups and report_latch_loop_groups commands only accept transparent latch data pins with the *-of_objects* option.

What Next

Specify only latch data pins, or remove the *-of_objects* option.

See Also

- get_latch_loop_groups
- report_latch_loop_groups

UITE-514

(Warning) AOCVM and POCVM are concurrently enabled. Turning POCV analysis off.

Description

Parametric on-chip variation (POCV) analysis is incompatible with AOCV analysis. If AOCV is enabled concurrently with POCV, POCV analysis is not performed.

What Next

This is a warning message only. The analysis will proceed disabling POCV analysis internally. To ensure POCV is used, disable AOCVM.

Feedback

See Also

- timing_aocvm_enable_analysis
- timing_enable_cross_voltage_domain_analysis
- timing_pocvm_enable_analysis

UITE-515

(Warning) The setting of variable %s will have no effect. It requires %s to be set to %s

Description

This warning message indicates a dependency of one variable on another.
Some variables only take effect when a particular mode is enabled. For example, the variable timing_crpr_threshold_ps is only applicable if CRPR is enabled (timing_remove_clock_reconvergence_pessimism is set to true)

Similarily, timing_report_skip_early_paths_at_intermediate_latches is only applicable if timing_enable_through_paths is set to TRUE

What Next

Check your scripts to ensure that the correct variables are set and adjust as required

See Also

- timing_remove_clock_reconvergence_pessimism
- timing_crpr_threshold_ps
- timing_enable_through_paths

UITE-516

(Warning) Can not perform "%s" operation on pin %s. The new setting conflicts the previous operation set on the same pin: "%s"

Description

This warning message indicates that the new operation can not overwrite the previously set operation on an output pin. For example, auto-inferencing a MUX exclusivity on a pin that has been defined as "set_disable_auto_mux_clock_exclusivity" Another example would be to perform "set_disable_auto_mux_clock_exclusivity" on an output pin that has been previously set by "set_clock_exclusivity" command. Another example would be to perform "remove_clock_exclusivity" on an output pin that has been previously set by "set_disable_auto_mux_clock_exclusivity" command.

What Next

Check your scripts to ensure that the correct order of precedence has been used in regards to MUX exclusivity commands.

See Also

- timing_enable_auto_mux_clock_exclusivity

UITE-517

(Error) The exclusivity set with '%s' option on the output pin '%s' is dropped.

Description

This error message is issued when there is a MUX-exclusivity relationship defined on an output pin and the cell is not of a MUX type.

What Next

Make sure that MUX-exclusivity is only set on MUX cells.

UITE-518

(Error) There is no exclusivity defined on the output pin '%s'.

Description

This error message is issued when the user tries to remove the exclusivity relationship which has not been defined on the output pin.

What Next

Make sure that there is an exclusivity relationship defined on the output pin before trying to remove it.

UITE-519

(warning) 3D POCV table-lookup is not currently supported. (%s)

Description

This warning message is issued when the 2D POCV delay sigma lookup is used with a 3D POCV table.

Feedback

UITE-520

(Warning) It is not recommended to use full path recalculation for sign off analysis as a conservative path-based recalculation of the clock,data check reference or borrowing path can not be guaranteed.

Description

When the pba_recalculte_full_path variable is set to true, Primetime will recalculate all extra paths associated with the data path, namely the clock,data check reference and borrowing paths. When recalculating the extra paths, PrimeTime considers only the worst paths from graph based analysis. There is no guarantee that the worst paths from graph based analysis will be the worst paths following a path based analysis. So for example if there is reconvergence in the clock network, there is no guarantee that the recalculated clock path is the worst clock path. For further details see the pba_recalculate_full_path man page and solvenet article "What Are the Issues Involving Recalculating Reconverging Clock Paths" .

What Next

Set the variable pba_recalculate_full_path to false when doing signoff analysis.

UITE-521

(Warning) Path based analysis is not supported in fast analysis mode.

Description

Path based analysis is not supported in fast analysis mode. The report will proceed without performing path based analysis.

What Next

Do not use the -enable_fast_analysis option with the set_program_options command.

UITE-522

(Information) recalculated paths %d.

Description

Displays the number of paths recalculated in the current path group.

What Next

No action is required.

Feedback

UITE-523

(Information) finished endpoints %d, total endpoints %d, number of paths considered during analysis %lu.

Description

Displays the number of endpoints completed in the current path group. Also displays the number of paths considered during analysis. This number is derived by summing the number of paths in the critical violating region of each endpoint.

What Next

Nothing.

UITE-524

(Error) Size of a collection passed to report_timing in distibuted mode (%d) is larger than the limit (%d).

Description

Any collection passed to *report_timing* in the distributed hierarchical mode cannot exceed set limit.

What Next

This is a temporary limitation which will be removed in future releases of PrimeTime.

See Also

- report_timing

UITE-525

(Warning) No reporting data exists for block '%s'.

Description

The required reporting data were not found for a block. The reporting data are available at the top level of Hyperscale analysis, only if the reporting command has been issued at the block level.

What Next

Issue the reporting command with the same options at the block level so that the reporting data are available at the top level.

Feedback

UITE-526

(Warning) The skip early paths endpoint limit of %d has been exceeded at endpoint '%s'. For this endpoint %d paths were found and %d paths were skipped due to early arrival at intermediate latches.

Description

You have received this message because the skip early paths endpoint limit has been met for a skip early paths (*timing_report_skip_early_paths_at_intermediate_latches* = *true*) report to this endpoint.

This command can be very intensive in runtime, particularly when the majority of paths have early arrival at intermediate latches. The endpoint limit allows runtime to be kept in check.

What Next

Should the user wish to widen the search space then the slack_lesser_than switch could be used with the command to increase the search space (skip early paths defaults to a slack_lesser_than of 0)

See Also

- timing_enable_through_paths
- timing_report_skip_early_paths_at_intermediate_latches

UITE-527

(Warning) Automatically setting timing_report_use_worst_parallel_cell_arc to true because timing_reduce_parallel_cell_arcs is true

Description

When parallel cell arcs are collapsed during update_timing then we also need to collapse them during reporting. Otherwise we will return a large number of duplicate paths and/or the exhaustive path based algorithm will fail to converge.

What Next

If you are interested in seeing paths for all parallel cell arcs then set *timing_reduce_parallel_cell_arcs* to false and *timing_report_use_worst_parallel_cell_ars* to false

See Also

- timing_report_use_worst_parallel_cell_arc

Feedback

UITE-528

(warning) Cannot perform PBA on recalculated paths.

Description

Path-based analysis (PBA) can only recalculate a timing path once.

What Next

Only perform path-based analysis on paths which have not already been recalculated.

UITE-529

(warning) Interpolation/Extrapolation of %s sigma resulted in a negative sigma. Sigma will be clipped at zero. (%s)

Description

The process of interpolation or extrapolation resulted in a negative sigma. By definition, the sigma must be greater than or equal to zero.

What Next

Check the sigma tables.

See Also

- timing_pocvm_enable_analysis

UITE-530

(Warning) A very large delay (%g) has been detected between %s and %s.

Description

A large delay has been detected in a timing path between the 2 pins specified. This delay is large enough to affect the accuracy of other delays in the timing report.

It is recommended that the root cause of this large delay be identified and fixed.

See Also

- report_timing
- get_timing_paths

Feedback

UITE-531

(Warning) Setting slack_lesser_than to %g for this timing report.

Description

This warning message has been issued because the user is running report_timing with the variable *timing_report_skip_early_paths_at_intermediate_latches* to to *true* and no value has been specified for *l-slack_lesser_than*.

In this case the implied value for *-slack_lesser_than* will be overridden from infinity in order to minimize its impact on performance.

What Next

Should the user wish to increase the slack_lesser_than then they can repeat the command with the *-slack_lesser_than* switch specifying their desired slack value.

See Also

- timing_report_skip_early_paths_at_intermediate_latches

UITE-532

(Warning) Setting this variable to true could result in optimistic results, because dynamic CRP will always be removed from the slack.

Description

You are receiving this message because you have invoked a mode where the CRP removed will always be calculated from dynamic arrivals. This could lead to optimistic slacks.

UITE-533

(Error) create_dvfs_table -table option expects a list of {voltage_config value} pairs. Unexpectedly found %d objects in a %s: {%s}.

Description

The *-table opeion* of *create_dvfs_table* command expects a list of table rows. Each row of the table has the form {voltage_config value}. The "voltage_config" is itself a list of pairs of the form {supply_group_spec valid_labels}. The supply_group_spec identifies one supply group created with the *create_supply_group* command. The "valid_lables" identifies voltage level labels of the supply group which should be associated with the row.

Feedback

What Next

Check the syntax of the complex list taken by the table option. An example is shown below. In the example there are two domains, domain_A and domain_B. domain_A has three possible levels {x y z}, while domain_B has {A B C}.

```
pt_shell> set mytable [create_dvfs_table -type boolean -table \\
{
  { { {domain_A {x z}} {domain_B {A C}} }     true}
  { { {domain_A {x z}} {domain_B {A C}} }     true}
  { { {domain_A {y}} }                        true}
  { default                                   false}
}]
```

UITE-534

(Error) create_dvfs_table -table option expects a list of {voltage_config value} pairs. Syntax error found: {%s}.

Description

The *-table opeion* of *create_dvfs_table* command expects a list of table rows. Each row of the table has the form {voltage_config value}. The "voltage_config" is itself a list of pairs of the form {supply_group_spec valid_labels}. The supply_group_spec identifies one supply group created with the *create_supply_group* command. The "valid_lables" identifies voltage level labels of the supply group which should be associated with the row.

What Next

Check the syntax of the complex list taken by the table option. An example is shown below. In the example there are two domains, domain_A and domain_B. domain_A has three possible levels {x y z}, while domain_B has {A B C}.

```
pt_shell> set mytable [create_dvfs_table -type boolean -table \\
{
  { { {domain_A {x z}} {domain_B {A C}} }     true}
  { { {domain_A {x z}} {domain_B {A C}} }     true}
  { { {domain_A {y}} }                        true}
  { default                                   false}
}]
```

UITE-535

(Error) get_dvfs_scenarios option could not find a supply group matching %s, or more than one supply group matched.

Feedback

Description

The *-supply_group* option of the *get_dvfs_scenarios* command expects to match exactly one supply group in the design. The supply group reference names must have previously been specified using the *set_voltage_levels* command.

What Next

Check the spelling of the supply group name, and check that the *set_voltage_levels* command has already been run.

See Also

- set_voltage_levels

UITE-536

(Error) get_dvfs_scenarios option could not find voltage levels {%s} for supply group %s. %s

Description

The *-reference_names* option of *get_dvfs_scenarios* command expects a list of reference voltage names associated with the corresponding *-supply_group*.

What Next

Check the spelling for the level, and check that the supply group was created with that level.

See Also

- set_voltage_levels

UITE-537

(Error) Row %d of the table provided conflicts with a previous row.

Description

The table provided to *create_dvfs_table* is invalid because two rows specify similar voltage scenarios, but the row values are different. The scenarios for each distinct row should be distinct.

What Next

Rewrite the table in a way that does not introduce conflicts between rows.

Feedback

UITE-538

(Error) The table lacks a default, but the rows do not fully specify all possible scenarios.

Description

The table provided to *create_dvfs_table* is invalid because the rows do not identify the value for all possible scenarios. This can happen when no default row exists in the table. To add a default row, use the keyword "default" and append a row {devault value} to the table, where "value" is the default value to use for scenarios not specified by the other rows of the table.

What Next

Add more rows to completely specify the table, or add a default to the table.

UITE-539

(Error) Multiple default values were specified for the dvfs table.

Description

The table provided to *create_dvfs_table* is invalid because more than one row used the keyword "default" in place of a voltage configuration. Only one default row is allowed.

What Next

Specify only one default value for the table.

UITE-540

(Error) Must specify exactly one -reference_names option for each -supply_group option.

Description

The *get_dvfs_scenarios* option expects an equal number of *-supply_group* and *-reference_names* options. If there more than one reference voltage label should be part of the scenario, include all of them in the same -fl-reference_names *option corresponding to the -supply_group option.*

What Next

Specify exactly one *reference_names* option for each *-supply_group* option.

See Also

- set_voltage_levels

Feedback

UITE-541

(Error) get_dvfs_scenarios cannot reference supply group %s, which has not had reference names set by using set_voltage_levels.

Description

The supply group reference names must have previously been specified using the *set_voltage_levels* command.

What Next

Set the reference names for the supply group by using *set_voltage_levels*.

See Also

- set_voltage_levels

UITE-542

(error) The 'create_clock' command can only depend on one supply group (%d specified).

Description

The DVFS scenarios selected by the -dvfs_scenarios option of the create clock command reference more than one supply_group. Currently each clock can only depend on one supply_group

What Next

Select a scenario specification that depends only on one supply group and reissue the *create_clock* command.

UITE-543

(error) The -add option is required to add a DVFS scenario to an existing clock.

Description

When the -dvfs_scenarios option is used to add an additional scenario to an existing clock the -add option is required. If the intent is to overwrite the existing clock with a new clock please remove the -dvfs_scenarios option. In the later case a default clock for all scenarios gets created that can then be refined by adding additional clocks for specific scenarios using the -add option.

Feedback

What Next

Select add the -add option or remove the -dvfs_scenarios option and reissue the reissue the *create_clock* command.

UITE-544

(error) When adding a DVFS scenario to an existing clock the same source pins are required.

Description

When the -dvfs_scenarios and -add options are used to add an additional scenario to an existing clock it is required that the clock sources for the original clock scenario and the added clock scenario are the same.

What Next

Correct the -sources option to specify the same clock sources than were used for the original clock and reissue the *create_clock* command.

UITE-545

(error) Clock '%s' does not have a complete DVFS specification. Setting this clock inactive.

Description

When a clock has DVFS dependence the characteristics of the clock must be defined for all scenarios. If this is not the case the clock gets automatically disabled during update_timing.

What Next

Complete the clock specification by reissuing the *create_clock* command for the missing scenarios and rerun update_timing. Once the clock specification is complete the clock will be automatically re-enabled.

UITE-546

(error) When adding a DVFS scenario to an existing generated clock the same %s is required.

Description

When the -dvfs_scenarios and -add options are used to add an additional scenario to an existing generated clock it is required that the clock sources, master pin and master

clock (along with possibily other charactersitics) match the charactersitics of the original generated clock.

What Next

Correct the generated clock command to use the same characteristics as the original generated clock and reissue the *create_generated_clock* command.

UITE-548

(error) Cell instance %s has cross voltage check arc and SMVA guardband cell_check factor model too complex."

Description

This message is issued if there is a cross-voltage domain guardband cell_check derate on a cell that has at least one cross voltage domain constraint arc. This situation can not be guaranteed to be modeled correctly if the constraint arc belongs to a complex cell like an ETM.

What Next

Avoid cross-voltage domain guardband cell_check derate on complex macro cells that have cross voltage domain constraint arcs.

UITE-549

(error) set_max_delay constraint does not have a complete DVFS specification. Ignoring this constraint.

Description

When a set_max_delay constraint has DVFS dependence there must be a constraint value for all active scenarios. If this is not the case the constraint gets ignored during update_timing.

What Next

Complete the set_max_delay constraint specification by reissuing the \set_max_delay command for the missing scenarios and rerun update_timing. Once the clock specification is complete the set_max_delay constraint will be honored.

UITE-579

(Information) %.3f percent of pins in the design are being included in the critical region for graph-based refinement.

Feedback

Description

This message is issued during graph-based refinement. It indicates the percentage of pins in the design that are included in the critical region for graph-based refinement. The number of pins can be adjusted by changing the slack threshold for which a path is considered critical with the variables *timing_refinement_max_slack_threshold* and *timing_refinement_min_slack_threshold*.

See Also

- timing_enable_graph_based_refinement
- timing_refinement_max_slack_threshold
- timing_refinement_min_slack_threshold

UITE-580

(Warning) The exhaustive path-based all paths algorithm has failed to converge at pin '%s' and group '%s'. The worst PBA slack found at this pin was %g. It is known that no PBA paths exist with worse slack than %g endpoint for this group.

Description

You have received this message because the exhaustive path-based *all_paths* algorithm has failed to converge. This can happen when there are many paths with very similar slack in a region of design logic.

When the path-based analysis command completes, the following attributes store the UITE-580 information at the indicated endpoint pins:

- *pba_worst_endpoint_slack* - This is the worst PBA slack found at the endpoint. It represents a real recalculated path to the endpoint that could be reported.
- *pba_worst_path_pessimistic_bound* - This is the worst PBA slack that is possible at the endpoint. No specific path was found of this slack when the search exited, but the worst recalculated path to the endpoint cannot be worse than this.
- *pba_gap_to_convergence* - This is the difference between the previous two attributes.

These attributes are cleared at the start of the next path-based analysis command.

If you used the *-nworst N* option for the path search, the *pba_worst_endpoint_slack* attribute contains the PBA slack of the Nth worst path to the endpoint.

What Next

If there is a large gap between the currently worst known PBA slack and the worst potential slack, further explore the endpoint with *-from*/*-through* options.

Feedback

See Also

- report_timing
- get_timing_paths
- pba_exhaustive_endpoint_path_limit
- timing_aocvm_analysis_mode

UITE-581

(warning) Detected extrapolation of %s sigma beyond 10 percent of the library characterization range. (%s)

Description

During the POCV sigma lookup computation, extrapolation beyond 10 percent of the maximum index value was detected.

What Next

Check the sigma tables.

See Also

- timing_pocvm_enable_analysis

UITE-582

(Error) (%s) and (%s) are mutually exclusive; PrimeTime will ignore setting (%s).

Description

You have received this message because you have attempted to simultaneously set two variables that are mutually exclusive.

What Next

Please unset the undesired variable first.

UITE-583

(Error) Setting timing_cross_voltage_domain_analysis_mode to "legacy" is not compatible with get_dvfs_scenarios. Please try setting timing_cross_voltage_domain_analysis_mode to "full" for use with DVFS.

Feedback

Description

The *get_dvfs_scenarios* command cannot be used when *timing_cross_voltage_domain_analysis_mode* is set to "legacy".

If any get_dvfs_scenarios commands have been run in the current PrimeTime session, you cannot set the variable *timing_cross_voltage_domain_analysis_mode* to "legacy".

What Next

Please try setting the variable to "full" in order to use the command *get_dvfs_scenarios*.

UITE-584

(Warning) Setting timing_cross_voltage_domain_analysis_mode to "legacy" is not compatible with get_dvfs_scenarios. (Exception: at synopsys site, this is permitted for debug purposes only).

Description

The *get_dvfs_scenarios* command cannot be used when *timing_cross_voltage_domain_analysis_mode* is set to "legacy".

If any get_dvfs_scenarios commands have been run in the current PrimeTime session, you cannot set the variable *timing_cross_voltage_domain_analysis_mode* to "legacy".

What Next

Please try setting the variable to "full" in order to use the command *get_dvfs_scenarios*.

UITE-585

(Information) Beginning graph-based refinement for %s delay.

Description

This message is issued at the start of graph-based refinement. When *timing_enable_graph_based_refinement* is set to true, graph-based refinement is run prior to the first invocation of exhaustive PBA reporting in order to improve the performance of exhaustive PBA.

See Also

- timing_enable_graph_based_refinement

UITE-586

(Information) Graph-based refinement complete.

Feedback

Description

This message is issued when graph-based refinement has completed. When *timing_enable_graph_based_refinement* is set to true, graph-based refinement is run prior to the first invocation of exhaustive PBA reporting in order to improve the performance of exhaustive PBA.

See Also

- timing_enable_graph_based_refinement

UITE-587

(Warning) Graph-based refinement will not be performed as it is not supported with %s.

Description

When *timing_enable_graph_based_refinement* is set to true, graph-based refinement is run prior to the first invocation of exhaustive PBA reporting in order to improve the performance of exhaustive PBA. However, it is not supported with the current setting.

See Also

- timing_enable_graph_based_refinement

UITE-588

(Information) Graph-based refinement will not be used for delay_type %s, as the -slack_lesser_than value exceeds the refinement slack threshold.

Description

HyperTrace is a technology that that accelerates exhaustive path-based analysis (PBA) by computing refined graph-based timing data, then using it to drive the exhaustive PBA search.

Graph refinement (and thus HyperTrace acceleration) is restricted to the *slack-critical* region of the design, which is the set of pins whose slack is the same or less than the following min/max slack threshold variables:

```
timing_refinement_max_slack_threshold  (default: 0)
timing_refinement_min_slack_threshold  (default: 'disabled')
```

You receive this message when a command uses a *-slack_lesser_than* value that exceeds the corresponding refinement min/max slack threshold. Because the command scope exceeds the refinement region, HyperTrace acceleration will not be used.

Feedback

For example, the following commands will issue this message because the default max-default refinement threshold is *0*:

```
set_app_var timing_enable_graph_based_refinement true
report_timing -pba_mode exhaustive -slack_lesser_than 0.1
```

What Next

To use HyperTrace accelerated PBA for the command, set the corresponding refinement min/max slack threshold variable to the *-slack_lesser_than* value (or higher).

Note that changing a refinement threshold value will invalidate any refinement data already computed.

See Also

- eco_enable_graph_based_refinement
- timing_enable_graph_based_refinement
- timing_refinement_max_slack_threshold
- timing_refinement_min_slack_threshold

UITE-589

(Warning) The number of pins considered critical for graph-based refinement is large (%.3f percent of pins in the design). Graph-based refinement may incur significant runtime and memory impact.

Description

Graph-based refinement is triggered prior to the first exhaustive PBA report and improves the performance of exhaustive PBA reporting, but is confined to the portion of the circuit which is critical in terms of slack. A path is considered to be within the critical region if its slack is less than the value of the variable timing_refinement_max_slack_threshold (for a max path) or less than the value of the variable timing_refinement_min_slack_threshold (for a min path). The runtime and memory overhead of graph-based refinement depends on the values of these variables - the larger they are, the greater the overhead. Pins considered critical are those in data paths with slack less than the slack threshold, and all clock network pins relevant to those data paths. This warning is issued when at least 10 percent of pins in the design are critical.

What Next

In order to reduce the overhead of graph-based refinement, condsider setting the values of timing_refinement_max_slack_threshold and timing_refinement_min_slack_threshold. However they should not be lower than any slack_lesser_than arguments to be passed

Feedback

to exhaustive PBA reports, or else these reports will not benefit from the performance improvements delivered by graph-based refinement.

See Also

- timing_enable_graph_based_refinement
- timing_refinement_max_slack_threshold
- timing_refinement_min_slack_threshold
- timing_refinement_maximum_critical_pin_percentage

UITE-590

(Warning) Setting slack_lesser_than to %g for delay_type %s for this timing report.

Description

This warning message has been issued because the user is running exhaustive path-based reporting with the variable *timing_enable_graph_based_refinement* set to *true* and no value has been specified for *-slack_lesser_than*.

In this case the implied value for *-slack_lesser_than* will be overridden in order to minimize its impact on performance. The override value is from the relevant graph-refinement threshold i.e. *timing_refinement_max_slack_threshold* or *timing_refinement_min_slack_threshold* depending on the delay_type specifed for the exhaustive report.

What Next

Should the user wish to increase or decrease the slack_lesser_than then they can repeat the command with the *-slack_lesser_than* switch specifying their desired slack value. Alternatively they can set the appropriate refinement slack threshold to their desired slack value and rerun the report.

See Also

- timing_enable_graph_based_refinement
- timing_refinement_max_slack_threshold
- timing_refinement_min_slack_threshold

UITE-591

(Warning) POCV is not enabled so the -variation option will have no effect.

Description

The *-variation* switch to report_timing requires that POCV analysis be enabled. If POCV is not enabled then a regular non-variation report will be issued

What Next

Identify why POCV is not enabled in your run and rectify. If you do not intend to run POCV analysis then remove the *-variation* switch from your *report_timing* call

See Also

- report_timing
- timing_pocvm_enable_analysis

UITE-592

(Information) The exhaustive path-based recalculation limit of %d has been exceeded at at least one endpoint. The slack returned for each of these endpoints will be the %s slack at the point the endpoint limit is exceeded.

Description

This message is issued on completion of an exhaustive PBA analysis where at least one UITE-480 has been issued. In this case, depending on the value of *pba_path_recalculation_limit_compatibility* either the worst known path-based slack or the best known graph-based slack is returned for the endpoints that have UITE-480 warnings issued.

Depending on the design state the path-based and graph-based slacks may differ significantly to the user should be aware of the impact of this variable and the *pba_exhaustive_endpoint_path_limit*.

What Next

Consult the man pagess for *pba_path_recalculation_limit_compatibility* and *pba_exhaustive_endpoint_path_limit* and take the appropriate action.

See Also

- pba_path_recalculation_limit_compatibility
- pba_exhaustive_endpoint_path_limit

Feedback

UITE-593

(Warning) Enabling extended moments is not compatible with cross voltage domain analysis. No paths will be recalculated by PBA

Description

The extended moments POCV flow (enabled by setting *timing_pocvm_enable_extended_moments* to true) is not compatible with cross voltage domain PBA analysis (enabled by setting *timing_enable_cross_voltage_domain_analysis* to true). In this case no paths will be recalculated.

What Next

Disable extended moments and repeate the PBA command

See Also

- timing_pocvm_enable_extended_moments
- timing_enable_cross_voltage_domain_analysis

UITE-595

(Warning) A %s check is being %s for two asynchronous clocks. Check details: reference pin: %s clocked by %s; constrained pin: %s clocked by %s.

Description

This warning is issued when a max_skew or clock_separation constraint is defined for two clocks which have been specified as asynchronous. If two clocks are asynchronous they have no phase relationship at all and the skew/separation between clock edges cannot be computed correctly.

What Next

Verify that clock relationships are defined correctly and/or that it is valid to allow asynchronous clocks to reach these pins.

See Also

- set_clock_groups
- remove_clock_groups
- report_clock

Feedback

UITE-596

(Error) Failure in acquiring license for graph-based refinement.

Description

Graph-based refinement requires the *PT-ADVP* license. There was some error in attempting to check out this license.

What Next

Ensure *PT-ADVP* license can be acquired.

UITE-597

(Information) Graph-based refinement will not be used for delay_type %s, as the refinement slack threshold is set to 'disabled'.

Description

HyperTrace is a technology that that accelerates exhaustive path-based analysis (PBA) by computing refined graph-based timing data, then using it to drive the exhaustive PBA search.

Graph refinement (and thus HyperTrace acceleration) is restricted to the *slack-critical* region of the design, which is the set of pins whose slack is the same or less than the following min/max slack threshold variables:

```
timing_refinement_max_slack_threshold  (default: 0)
timing_refinement_min_slack_threshold  (default: 'disabled')
```

You receive this message when a command attempts to use HyperTrace accelerated PBA, but the corresponding refinement threshold is set to a value of *disabled*. Because HyperTrace acceleration is disabled for that delay type, it will not be used.

For example, the following commands will issue this message because the default min-default refinement threshold is *disabled*:

```
set_app_var timing_enable_graph_based_refinement true
report_timing -pba_mode exhaustive -delay min
```

By default, HyperTrace analysis is disabled for min-delay paths because they are typically short and not accelerated by refinement. If you have complex violating min-delay logic cones (such as I/O or memory interfaces) and the min-delay exhaustive PBA runtime recalculation is significant, setting a numeric threshold value might provide a benefit.

Feedback

What Next

To use HyperTrace accelerated PBA for the command, set the corresponding refinement min/max slack threshold variable to a numeric value that bounds the highest slack value you want to analyze.

Note that changing a refinement threshold value will invalidate any refinement data already computed.

See Also

- eco_enable_graph_based_refinement
- timing_enable_graph_based_refinement
- timing_refinement_max_slack_threshold
- timing_refinement_min_slack_threshold

UITE-598

(error) The tagged path set %s does not exist.

Description

The tagged path name shown by the error message does not correspond to any existing path tag sets.

Timing path signatures are created by *get_timng_paths* if the variable *enable_path_tagging* is set to *true*. These signatures can be associated with a named tag by passing a timing path collection to the *create_path_tag_set* command.

What Next

Run command *report_path_tag_set* without options to print out all currently defined path tag sets.

See Also

- create_path_tag_set
- enable_path_tagging

UITE-599

(Warning) Passing a wildcard pattern to the '%s' argument of this command can lead to unexpected behaviour. Object classes are checked for objects matching the pattern in the following precedence order: %s.

Feedback

Description

This command allows implicit matching of objects. This can lead to unexpected results as object classes are checked for objects matching the pattern in precedence order. If any of these object classes return a match, lower precedence classes will not be checked.

What Next

To narrow the search to a particular object class, it is recommended to pass a collection to the command using a "get_" command (e.g. get_pins).

UITE-600

(Error) get_dvfs_scenarios options %s and %s are incompatible.

Description

The specified command options are incompatible and cannot be specified simultaneously.

What Next

Specify only one of the options. If both results are desired, invoke two separate commands, each specifying one of the options.

UITE-601

(Warning) Option '%s' is not compatible with timing_enable_cross_voltage_domain_analysis set to "false".

Description

Cross-voltage domain analysis must be enabled for the specified option to be used.

What Next

Please try setting the variable *timing_enable_cross_voltage_domain_analysis* to "true" in order to use the option.

See Also

- timing_enable_cross_voltage_domain_analysis

UITE-602

(Error) Option -dvfs_scenarios of command set_timing_derate cannot be used on %s objects.

Feedback

Description

The command set_timing_derate can be used on cells, nets, designs, and library cells without the *-dvfs_scenarios* option. With the option, only leaf cell objects are permitted.

What Next

Please try the command again without the -dvfs_scenarios option

See Also

- timing_enable_cross_voltage_domain_analysis
- set_timing_derate

UITE-603

(Warning) DVFS scenarios are not applied as part of command set_timing_derate on objects of type %s when inside source -dvfs_scenarios.

Description

The command set_timing_derate can be sourced as part of source -dvfs_scenarios, but the scenarios are ignored if the object is a net, hierarchical cell, design, or library cell.

See Also

- timing_enable_cross_voltage_domain_analysis
- set_timing_derate

UITE-604

(Error) %s does not have needed supply group %s for use with set_timing_derate -dvfs_scenarios.

Description

The command set_timing_derate with the option -dvfs_scenarios can be used on cells/nets only when the dvfs scenarios depend only on the supply groups attached to the cell/net

What Next

Please try the command again without changing the argument to the -dvfs_scenarios option, so that the only dependence is on supply groups attached to the cell/net.

Feedback

See Also

- timing_enable_cross_voltage_domain_analysis
- set_timing_derate

UITE-605

(error) No topological specification for unconstrained reporting.

Description

The design is fully unconstrained such that no constrained path exists. Unconstrained reporting assumes the design is at least partially constrained, so requires a topology specification.

What Next

Add constraints to the design or restrict the topology covered by the report by specifying *-from*, *-to* etc.

UITE-606

(Information) Insufficient Endpoints to perform ML PBA analysis.

Description

The design does not have sufficient number of endpoints to complete training for ML PBA. So no ML model will be deployed for the rest of the PBA analysis.

UITE-607

(Information) Completed ML training on %d endpoints in %f seconds.

Description

The training phase of ML PBA analysis is complete.

What Next

ML PBA analysis will now move onto the validation phase.

UITE-608

(Information) Completed ML validation on %d endpoints in %f seconds.

Feedback

Description

The validation phase of ML PBA analysis is complete.

What Next

ML PBA analysis will now move onto the model deployment phase.

UITE-609

(Information) Deploying ML model on %d endpoints with %s setting.

Description

The ML model for PBA analysis has been trained and validated. The validation stage has configured the model to be in one of aggressive/medium/conservative/none setting.

What Next

ML PBA analysis will proceed to use the trained model in the mentioned setting for the rest of the analysis.

UITE-610

(Warning) Derates from %s family are ignored when variable timing_use_constraint_derates_for_pulse_checks is set.

Description

When variable timing_use_constraint_derates_for_pulse_checks is set and the design has min period or min pulse width family derates then, old behavior of timing_use_constraint_derates_for_pulse_checks variable is used.

What Next

Turn of variable timing_use_constraint_derates_for_pulse_checks.

UITE-615

(Warning) ML is not yet supported for PBA analysis with the *-cover_design* option.

Description

ML PBA analysis with cover_design is not yet supported. The analysis will proceed with ML disabled.

What Next

Remove either *-pba_mode ml_exhaustive* or *-cover_design* options to proceed.

Feedback

UITE-616

(Error) Failure in acquiring license for ML PBA analysis.

Description

Machine learning path-based analysis requires the *PT-ADVP* license. There was some error in attempting to check out this license.

What Next

Ensure *PT-ADVP* license can be acquired.

UITE-617

(Warning) The setting of variable %s will have no effect. Its behavior is incompatible with %s.

Description

This warning indicates that a particular variable setting is incompatible with a command, command option, or another variable.

For example, the behavior invoked by skip early arrival reporting (*timing_report_skip_early_paths_at_intermediate_latches* set to *true* is not compatible with the *-cover_design*, *-cover_through*, *start_end_pair* and *-pba_mode exhaustive* options to *report_timing* and *get_timing_paths*.

What Next

Check your scripts to ensure that the correct variables are set, review the intent of the script, and adjust as required.

See Also

- timing_report_skip_early_paths_at_intermediate_latches

UITE-618

(Information) Forcing pin '%s' to be a probe timing %s only for this probe-type timing exception. Existing timing paths are not affected.

Description

The specified pin is neither a valid timing startpoint nor endpoint. The *set_max_delay* and *set_min_delay* commands are point-to-point timing exception commands that can be specified with the *-probe* option, which creates a maximum or minimum delay constraint

Feedback

from any startpoint *-from from_list* or endpoint *-to to_list* specified, without affecting other timing constraints for paths through these pins.

What Next

PrimeTime assumes the behavior described above is intended. Without the *-probe* option, the specified pin becomes a timing startpoint *-from from_list* or endpoint *-to to_list* for all timing constraints. The pin is treated like a clock pin *-from from_list* or data input of a flip-flop *-to to_list*, effectively breaking all timing paths through these pins.

See Also

- set_max_delay
- set_min_delay

UITE-619

(Error) Failure in acquiring license required for %s '%s'.

Description

The specified %s '%s' requires the *PrimeTime-ADV-PLUS* license. There was an error in attempting to checkout this license.

What Next

Ensure *PrimeTime-ADV-PLUS* license can be acquired.

UITE-620

(Error) %s '%s' is currently not supported with Simultaneous Multi Voltage Analysis.

Description

The specified %s '%s' is currently not supported with Simultaneous Multi Voltage Analysis flows.

What Next

Disable Simultaneous Multi Voltage Analysis by setting 'timing_enable_cross_voltage_domain_analysis' to 'false'

UITE-621

(Error) Failure in acquiring sufficient licenses required for Multi Voltage Analysis. The specified number of voltage levels (%d) and DVFS scenarios necessary to analyze the design (%d) requires %d PT-ADVP licenses.

Feedback

Description

Insufficient number of *PT-ADVP* licenses necessary to analyze the specified number of voltage levels and the corresponding DVFS scenarios. There was an error in attempting to checkout these licenses.

What Next

Ensure sufficient *PT-ADVP* licenses can be acquired.

UITE-622

(Warning) All DVFS scenarios are currently disabled.

Description

All DVFS scenarios are disabled as a result of previously applied configure_dvfs_scenarios commands.

What Next

Please enable at least one DVFS scenario using the command configure_dvfs_scenarios command.

UITE-623

(Information) All DVFS scenarios are currently enabled.

Description

All DVFS scenarios are enabled. This is normal if your flow does not use configure_dvfs_scenarios commands. It can also happen as a result of the combined effect of previously applied configure_dvfs_scenarios commands.

UITE-624

(Warning) Pin %s%s included in more than one -from, -through, or -to set.

Description

When a pin is included in the object list of more than one -from, -through, or -to option, part or all of the exception may not be applied. In order for an exception to apply to a path, the path must pass through a pin or clock of each of the sets, in order. If the same pin is in two -through sets, it is not enough to pass through the pin once in order for the exception to apply.

Feedback

See Also

- set_multicycle_path
- set_false_path
- set_path_margin

UITE-625

(Error) Generated clock '%s' can not have the same master clock specified with option '-master_clock'

Description

This is error message is issued when the master clock specified in create_generated_clock command is the same as the generated clock itself.

What Next

Check for the generated clock definition to see if the master clock is correctly defined.

See Also

- create_generated_clock

UITE-626

(Error) All DVFS scenarios are currently disabled. Falling back to non-DVFS analysis.

Description

All DVFS scenarios are disabled as a result of previously applied configure_dvfs_scenarios commands. In this situation DVFS based analysis can not proceed and therefore the analysis falls back to regular (non-DVFS) Primetime analysis.

What Next

Please enable at least one DVFS scenario using the command configure_dvfs_scenarios command.

UITE-627

(Error) *update_noise* command must be explicitly entered with proper collection of DVFS scenarios prior to this command.

Feedback

Description

When Simultaneous Multi Voltage Analysis is turned on by setting 'timing_enable_cross_voltage_domain_analysis' to 'true', *update_noise* command must be explicitly entered with proper collection of DVFS scenarios.

What Next

Please try the command again after *update_noise* command with proper collection of DVFS scenarios.

See Also

- timing_enable_cross_voltage_domain_analysis
- update_noise

UITE-628

(Error) option '%s' of command '%s' requires Simultaneous Multi Voltage Analysis flow be enabled.

Description

The option is only supported with Simultaneous Multi Voltage Analysis flows.

What Next

Enable Simultaneous Multi Voltage Analysis flow by setting 'timing_enable_cross_voltage_domain_analysis' to 'true'.

See Also

- timing_enable_cross_voltage_domain_analysis
- update_noise

UITE-629

(Warning) %d invalid %s, %s, %s ignored.

Description

When *report_timing* or *get_timing_paths* is specified with "*" or a cell name, there is a possibility that many invalid startpoints or endpoints are included in the specification, such as *-from [get_pins FF/*]* which includes input, output and asynchronous pins. When *timing_report_always_use_valid_start_end_points* is set to true, these invalid start and endpoints are omitted from the search.

Feedback

What Next

You can use variable *timing_report_always_use_valid_start_end_points* to include invalid startpoints and endpoints, which will be treated as through points, though this can be much more time consuming.

See Also

- report_timing
- timing_report_always_use_valid_start_end_points

UITE-630

(Warning) Graph-based refinement is not being performed because the percentage of pins in critical region exceeds %.3f percent.

Description

This message indicates that the percentage of pins in the design included in the critical region for graph-based refinement exceeds the maximum critical pin percentage. The graph-based refinement analysis will not be performed to prevent large performance/ capacity overhead. Subsequent commands will proceed as if graph-based refinement were disabled.

What Next

The variable *timing_refinement_maximum_critical_pin_percentage* can be adjusted to enable graph based refinement to be performed even when the critical region is larger than recommended.

See Also

- timing_enable_graph_based_refinement
- timing_refinement_max_slack_threshold
- timing_refinement_min_slack_threshold
- timing_refinement_maximum_critical_pin_percentage

UITE-631

(Error) option '%s' of command '%s' must be provided with fully-specified voltage scenario. Please try a voltage scenario with all the supply groups specified.

Feedback

Description

When Simultaneous Multi Voltage Analysis is turned on by setting 'timing_enable_cross_voltage_domain_analysis' to 'true', the command requires a fully-specified voltage scenario. sA fully-specified voltage scenario requires for every supply voltage to have a specific voltage level.

What Next

Please make sure that the specified option is of the proper type.

See Also

- timing_enable_cross_voltage_domain_analysis
- update_noise

UITE-632

(Error) The input pin '%s' and the output pin '%s' do not belong to the same cell.

Description

the parameters specified in the command *set_clock_exclusivity* must belong to the same cell.

What Next

Check your scripts to ensure that the correct parameters are specified for the command *set_clock_exclusivity*.

UITE-633

(Warning) Path gathering has satisfied the max_paths criteria. There may be paths of interest with slack less than %s that were not considered when generating this report.

Description

This message indicates that the *report_timing* algorithm has succeeded in finding max_paths number of paths and that there may be further paths of interest.

This message only appears for *-cover_design*, *-cover_through* and *-start_end_pair* based reports.

What Next

To see more paths of interest, increase max_paths.

Feedback

See Also

- report_timing
- get_timing_paths

UITE-634

(Warning) You have specified more paths to be gathered than the recommended max_paths limit of %d.

Description

This message indicates that the *-max_paths* option is requesting more paths than recommended. Please note that additional path gathering will impact runtime and capacity.

See Also

- report_timing
- get_timing_paths

UITE-635

(Warning) Path gathering has encountered a path which can not be traced back further than %s.

Description

While tracing, PrimeTime has encountered an inconsistency which has caused the path gathering for the particular endpoint to be abandoned at the given pin.

NEXT STEPS

Run *update_timing -full* which may remove the inconsistency.

See Also

- update_timing
- report_timing
- get_timing_paths

UITE-636

(Warning) The -edges option of create_generated_clock for derived clock %s may result in impossible edge correspondance with the reference clock %s from which it is derived.

Feedback

Description

In some cases, use of the -edges option of create_generated_clock can results in edges after the first period that cannot correspond to any edge in the

Example:

create_clock -name clk -period 20 -waveform {0 12} [get_port clk] create_generated_clock -name gclk \ -master [get_clock clk] -source [get_port clk] -add \ -edges {1 2 4} [get_pin flop/Q]

In the above example, the edges of clock clk are

0 12 20 32 40 52 60 ...

While the edges of gclk are

0 20 32 52 64 84 96 ...

Beyond the first period, the edges of gclk don't correspond to any edges of clk.

This clock derivation is unlikely to be what the user intends. Please review the clocks and make appropriate changes to the clock derivation.

For instance, using -edges {1 2 5} results in a more reasonable set of edges, all of which correspond to edges of clk:

0 20 40 60 80 100 120 ...

See Also

- create_clock
- create_generated_clock

UITE-637

(Error) Must specify exactly one -corner_names option for each -corner_domains option.

Description

The *get_dvfs_scenarios* option expects an equal number of *-corner_domains* and *-corner_names* options. If there more than one corner label should be part of the scenario, include all of them in the same -fl-corner_names *option corresponding to the -corner_domains option.*

What Next

Specify exactly one *-corner_names* option for each *-corner_domainds* option.

Feedback

UITE-638

(Error) get_dvfs_scenarios option could not find corner {%s} for corner domain %s. %s

Description

The *-corner_names* option of *get_dvfs_scenarios* command expects a list of corner names associated with the corresponding *-corner_domain*.

What Next

Check the spelling for the corner, and check that the corner domain was created with that level.

UITE-639

(Error) get_dvfs_scenarios option could not find a corner domain matching %s, or more than one corner group matched.

Description

The *-corner_domain* option of the *get_dvfs_scenarios* command expects to match exactly one corner domain in the design. The corner domain corner names must have previously been specified using the *define_corner* command.

What Next

Check the spelling of the corner domain name, and check that the *define_corner* command has already been run.

UITE-640

(Error) get_dvfs_scenarios requires that the command define_corner be run before specifying the -corner option.

Description

The *-corner* option of the *get_dvfs_scenarios* command expects the *define_corner* command to have been run previously.

What Next

Check that the *define_corner* command has already been run.

UITE-641

(warning) Removing clock '%s'; all of its sources are now assigned to a new clock.%s

Feedback

Description

This message is printed when the *create_clock* command is issued on a source that already has a clock of a different name, and the *-add* option is not used. The existing clock(s) will be removed from these sources, and will be removed entirely if they have no remaining sources.

What Next

If existing clocks should be preserved, use *-add* in the later *create_clock* command.

If only the later clock is desired, change the constraint script to eliminate previous *create_clock* commands on those sources.

See Also

- create_clock

UITE-642

(Information) Restoring a session with current scenario defined as %s. %ld scenarios are on the stack to be popped with pop_dvfs_scenario.

Description

This message is printed when the *restore_session* command is used, and the session being restored has a current scenario set using the *push_dvfs_scenario* commmand. The user should be aware that the current scenario limits the tool to reporting on a subset of scenarios. The user can return to reporting all scenarios by using *pop_dvfs_scenario*.

UITE-643

(error) The corner '%s' does not belong to the corner domain of the input cells.

Description

This message is printed when the SMC related commands (e.g. *set_process* etc) are used. You can not call those SMC commands before the corners are defined correctly into its corner domains. Please define corners properly with *define_corner* command.

What Next

Check whether the corners that you defined in corner domains matches in this command.

UITE-644

(error) The corners of a corner domain can not be modified once specified.

Description

This message is printed when the user specifies a new define_corner for a corner domain that already has corner defined. *define_corners* can only set corner to a certain corner domain once.

UITE-645

(Error) Ignoring pin '%s'; object must be a port or hierarchical pin at the same hierarchical level as the *-instance* cell.

Description

This message occurs when the *report_logic_connectivity* command is called with a pin in the *object_list* that is not a hierarchical pin or port at the same level of hierarchy as the *-instance* cell. You cannot specify a leaf pin or a pin at a different level of hierarchy as the startpoint or endpoint for hierarchical connectivity analysis.

What Next

Specify only ports or hierarchical pins at the correct hierarchical level in the *object_list*.

UITE-646

(Error) DVFS scenarios count (%d) exceeds the maximum supported number of scenarios (%d).

Description

The size of the current design DVFS scenario space exceeds the maximum permissible number of DVFS scenarios that can be returned from the *get_dvfs_scenarios* command.

What Next

Modify the permissible DVFS scenario count limit specified with the *timing_max_get_dvfs_scenarios_count* variable. Please note this can result in large runtime overhead depending on the size of the current design DVFS scenario space and the new value specified for the DVFS scenario count limit.

UITE-647

(Warning) ML-PBA was used; additional unreported violating endpoints might exist, and worse violators might exist for the reported endpoints.

Feedback

Description

A machine learning model for PBA (ML-PBA) was used, and violators were returned by the current command. As a result, be aware of the following characteristics of ML-PBA violator reporting:

- Additional unreported violating endpoints could exist in the command scope.
- The reported endpoints might have worse violators than those returned or reported.

In other words, violations cannot be safely waived in an ML-PBA flow.

However, ML-PBA is safe for signoff if no violators are returned. The ML-PBA behavior can be summarized as follows:

- If ML-PBA reports no violations, regular exhaustive PBA will also report no violations.
- If ML-PBA reports a violation, regular exhaustive PBA will also report violations:
  - Regular exhaustive PBA might find worse paths to endpoints than ML-PBA.
  - Regular exhaustive PBA might find additional violating endpoints.

What Next

If signoff PBA accuracy is required for all violating endpoints in the design, then rerun the command with *-pba_mode exhaustive*.

UITE-648

(Error) The sequential library cell %s has no statetable or logic function associated with it; the *-through_sequential* option will not work with it.

Description

The *report_logic_connectivity* command can only reliably trace through sequential cells if they have a statetable or logic function defined.

What Next

Check whether the indicated library cells have statetable or logic functions associated with them.

UITE-649

(Error) A loop has been found on pin %s; the *report_logic_connectivity* command can not trace through loops when the *-through_sequential* option is used.

Feedback

Description

The *report_logic_connectivity -through_sequential* command can only reliably trace connections between pins if the connections do not contain loops.

What Next

Check for loops around the pins of interest, between the starting and ending pins.

UITE-650

(Error) Option '%s' is not supported when %s is enabled.

Description

The specified *report_timing* command option is not supported under the specified condition.

What Next

Refer to the manual page for this command for detailed information on valid option usage.

UITE-651

(error) Corner domain '%s' does not exsit.

Description

This message is printed when the SMC related commands *define_corners* are used. You can not define corners in a nonexistent corner domain. Please make sure that you create the right corner domain with *create_corner_domain* command first.

What Next

Check if the corner domain name is correct or not. If correct, create this corner domain before defining corners in it.

UITE-653

(error) Corners have already been defined.

Description

This message is printed when the SMC related command *define_corners* has been used for more than once, unless it is used for a different corner domain. Please make sure that you have all corner names added together in the same *define_corners* command.

Feedback

What Next

Check if the corner domain name is correct or not. If not, use the correct corner domain name instead. To re-define corners, you must remove the entire design.

UITE-655

(error) Thermal maps have already been defined.

Description

This message is printed when the SMC related command *define_thermal_maps* has been used for more than once. Please make sure that you have all thermal maps added together in the same *define_thermal_maps* command.

What Next

No further action.

UITE-657

(error) Global setup and hold analysis has already been defined.

Description

This message is printed when the command *configure_setup_hold_analysis* has been used for more than once. Please make sure that you have the correct sigma values added in the same *configure_setup_hold_analysis* command.

What Next

No further action.

UITE-658

(error) defined corner '%s' is missing a parasitic corner. Using parasitic corner '%s'.

Description

This message is printed when the command *set_corner_parasitics* has not been specificed for all corners listed in the *define_corners* command. Please make sure that all corners are covered. Another parasitic corner will be used, so miscorrelation may occur.

What Next

No further action.

Feedback

UITE-659

(error) Corner domain '%s' has already been created.

Description

This message is printed when the SMC related command *create_corner_domain* has been used to create the same corner domain. Please make sure that you have a different corner domain name used in the new *create_corner_domain* command.

What Next

Check if the corner domain name is correct or not. If not, use the correct corner domain name instead.

UITE-660

(Information) The value of the variable pba_exhaustive_any_slack_lesser_than exceeds the value of the -slack_lesser_than command option. This command will use %f from -slack_lesser_than as the pba_exhaustive_any_slack_lesser_than value.

Description

This message is printed when the value of the variable *pba_exhaustive_any_slack_lesser_than* exceeds the value of slack_lesser_than used by either *report_timing* or *get_timing_paths* in exhaustive PBA mode. The value of *pba_exhaustive_any_slack_lesser_than* used for the scope of the command is set to the salck lesser_than value used by *report_timing* or *get_timing_paths*.

See Also

- report_timing
- get_timing_paths
- pba_exhaustive_any_slack_lesser_than

UITE-661

(error) Missing thermal information for thermal map(s) %s.

Description

No thermal information for the specified thermal maps was annotated to the cells either because of missing thermal results or because of missing location information for the cells.

What Next

Check if all the thermal results for the defined thermal maps are loaded and the parasitics with location information is loaded.

See Also

- read_parasitics

UITE-663

(Error) The setting of variable %s is incompatible with %s.

Description

The PBA early termination modes *pba_exhaustive_slack_tolerance_percentage* and *pba_exhaustive_any_slack_lesser_than* are incompatible with the *-pba_mode ml_exhaustive* of reporting. The tool cannot enforce the slack bounding guarantees of the variables in ML exhaustive PBA mode.

What Next

Check your scripts to ensure that the correct variables are set, review the intent of the script, and adjust as required.

See Also

- pba_exhaustive_slack_tolerance_percentage
- pba_exhaustive_any_slack_lesser_than
- report_timing
- get_timing_paths

UITE-680

(Warning) The exhaustive path-based recalculation reached early convergence criteria %s at endpoint '%s' and group '%s'. The worst PBA slack found at this pin was %g. It is known that no PBA paths exist with worse slack than %g for this group.

Description

You have received this message because at least one user specified early convergence criteria has been reached during an exhaustive search for worst paths at this endpoint.

Feedback

When the path-based analysis command completes, the following attributes store the UITE-680 information at the indicated endpoint pins:

- *pba_worst_endpoint_slack* - This is the worst PBA slack found at the endpoint. It represents a real recalculated path to the endpoint that could be reported.
- *pba_worst_path_pessimistic_bound* - This is the worst PBA slack that is possible at the endpoint. No specific path was found of this slack when the search exited, but the worst recalculated path to the endpoint cannot be worse than this.
- *pba_gap_to_convergence* - This is the difference between the previous two attributes.
- *pba_convergence_status_min* - This is the convergence criteria that was reached during min analysis.
- *pba_convergence_status_max* - This is the convergence criteria that was reached during max analysis.

These attributes are cleared at the start of the next path-based analysis command.

If you used the *-nworst N* option for the path search, the *pba_worst_endpoint_slack* attribute contains the PBA slack of the Nth worst path to the endpoint.

What Next

If there is a large gap between the currently worst known PBA slack and the worst potential slack, further explore the endpoint with *-from*/*-through* options.

See Also

- report_timing
- get_timing_paths
- pba_exhaustive_endpoint_time_limit

UITE-681

(Warning) The derived clock %s with -edges of odd period, may result in all transitions with respect to master clock.

Description

In some cases, use of the -edges option of create_generated_clock with odd period may result in all transitions rise to rise, rise to fall, fall to rise, fall to fall, from the master clock.

Example:

create_clock -name clk -period 1 [get_port clk]

Feedback

create_generated_clock -source [get_port clk] -edges {1 4 6} -name gclk [get_pins F1/Q]

In the above example, the edges of clock clk are

0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5 5.5 6...

While the edges of gclk are

0 1.5 2.5 3 4.5 5.5 ...

Beyond the first period, the edges of gclk corresponds to further more transitions giving all possible transitions. So, in case of clock jitters, it's possible to have both clock cycle and duty clycle jitter. Worst jitter is applied in this case.

For instance, using -edges {1 2 5} with even period will not result in all transitions from master clock. It's possible to have only one clock jitter.

0 0.5 2 2.5 4 4.5 6 ...

See Also

- create_clock
- create_generated_clock

UITE-682

(Information) The default value for the -trace_arcs option of the %s command has been changed to all.

Description

In logical update reduction mode, the default value for the *all_fanin* and *all_fanout* command *-trace_arcs* option is changed from *timing* to *all*.

What Next

To return the default to normal, set the *timing_allow_logical_update_reduction* variable to false, or explicitly specify *-trace_arcs timing* to the all_fanin or all_fanout command.

Note that logical update reduction mode is not effective for any explicit *-trace_arcs* value apart from *all*.

See Also

- all_fanin
- all_fanout

Feedback

- report_transitive_fanin
- report_transitive_fanout

UPF

UPF-001

(error) Cell '%s' is already in the extent of power domain '%s'

Description

A cell cannot belong to multiple power domains.

What Next

Remove this cell from the list and re-run this command.

UPF-002

(warning) UPF version '%s' was requested but the tool supports '%s' Other constructs will be supported in future releases.

Description

The requested version of UPF syntax standard is different from the version supported by the tool.

What Next

Review which commands and options in your design scripts are not compliant with the version supported by the tool. Replace the commands and options by supported syntax if possible. Request the tool support team to add support for the other UPF version of the standard.

UPF-003

(error) Power domain '%s' already contains primary power and ground supply nets.

Description

The primary power and ground supply nets have already been specified earlier. A power domain can have only one set of primary and ground supply nets.

Feedback

What Next

The primary supply nets of a power domain cannot be changed once assigned. Do not attempt to set them again.

UPF-004

(error) The '%s' option of %s command must specify exactly one %s.

Description

This option of the command takes exactly one of the specified object type.

What Next

Check the command man page for more details and correct it accordingly.

UPF-005

(error) The -reuse option can only be used to reuse the supply net within another power domain in the same scope.

Description

The supply net object can only be resued in another power domain belonging to the same scope as the other power domains where the supply net object exists. Supply net objects cannot be reused across hierarchical scopes.

What Next

Create a new supply_net and connect it through supply ports if you would like to extend this net across another power domain in another scope.

UPF-006

(error) The %s object cannot be created because %s of name %s already exists.

Description

The given object already exists. Names are expected to be unique in a given scope.

What Next

Create a new object with a different name.

If you are using the create_supply_net command, please specify -reuse option to reuse a supply net.

Feedback

UPF-007

(error) The given supply net already exists in this domain.

Description

The given object already exists in the given domain. Names are expected to be unique in a given scope.

What Next

Create a new object with a different name.

If you are using the create_supply_net command, please specify -reuse option to reuse a supply net.

UPF-009

(Error) The value specified by % can not be greater than the value specified by %s.

Description

You are receiving this error message because a set_voltage command has been specified with dynamic component values that are greater than their associated voltages. The dynamic component values must be less than the voltages (-min_voltage, max_voltage) specified with the command.

What Next

Adjust the dynamic component values and re-issue the command.

UPF-010

(Error) Cannot open file '%s'.

Description

The file name provided to *load_upf* cannot be opened. Possible reasons for this are that the file does not exist in the search path specified or that it does not have read permissions.

What Next

Verify the location of the file to be read on and its permissions. Once the file has been verified re-run *load_upf*.

Feedback

UPF-011

(Error) Cannot set isolation on pin or port %s

Description

The pin or port must be in the same domain as the isolation strategy.

What Next

Compare relevant set_isolation and create_power_domain -elements commands and correct.

UPF-012

(error) The '%s' option of create_power_switch command must specify exactly one pair of %s.

Description

This option of create_power_switch command takes exactly one port on the switch and the net where the port connects.

What Next

Check the command man page for more details and correct it accordingly.

UPF-013

(error) Net '%s' specified for 'create_power_switch -control_port' can not be found in the design.

Description

Please check the signal net specified for option -control_port in command create_power_switch. Please Make sure that it exists in the current scope.

What Next

Check the command man page for more details and correct it accordingly.

UPF-014

(error) Supply net '%s' specified for '%s' can not be found.

Feedback

Description

Please check the supply net specified for the command. Make sure that the supply net exist in the current_scope.

What Next

Check the command man page for more details and correct it accordingly.

UPF-015

(Warning) Cannot set retention on cell %s which is not of retention type.

Description

Retention can only be set of hierarchical blocks or leaf cells with retention information in the Liberty model. The retention strategy is not applied for the above mentioned cell (is ignored).

What Next

Ensure that all retentions cells have necessary retention information in Liberty (.lib). Refer to the Liberty standard on *retention_cell* attribute. If you cannot correct the Liberty model for the above cell then you can explicitly connect power and ground retention pins by *connect_supply_net*.

See Also

- set_retention
- connect_supply_net

UPF-016

(error) The '%s' option of create_power_switch command is not specified.

Description

This option of create_power_switch command is a required option.

What Next

Check the command man page for more details and correct it accordingly.

UPF-017

(error) The '%s' option of create_power_switch command must specify exactly one set of %s.

Feedback

Description

This option of create_power_switch command takes exactly one set of a named state, the input_supply_port for which this is defined, and its corresponding Boolean function.

What Next

Check the command man page for more details and correct it accordingly.

UPF-018

(error) The input_supply_port '%s' specified in '%s' option does not match the port_name of the input_supply_port defined for the power switch.

Description

This option of create_power_switch command takes exactly one set of a named state, the input_supply_port for which this is defined, and its corresponding Boolean function. The input_supply_port must match the port_name specified for -input_supply_port option in the same command.

What Next

Check the command man page for more details and correct it accordingly.

UPF-019

(Information) The switch control port '%s' specified in boolean expression '%s' is not defined for the power switch.

Description

The control ports specified in the state boolean expression must be defined as the control ports of the power switch. Use option -control_port to create such control ports.

What Next

Fix the syntax and check the command man page for more details.

UPF-020

(error) Invalid specification in boolean expression '%s' for option '%s' in command create_power_switch.

Description

The specification for the named option is not a valid boolean expression.

Feedback

What Next

Check the boolean expression for the named option in command create_power_switch.

UPF-021

(error) The boolean expression is too long for option '%s' in command create_power_switch. The maximum acceptable number of characters is %d.

Description

The length limit for the boolean expression is currently set to be 2048 characters.

What Next

Check the boolean expression for the named option in command create_power_switch. Please contact Synopsys Customer Support Center if needed.

UPF-022

(error) Unknown function operator '%c' in boolean expression '%s' for option '%s' in command create_power_switch.

Description

The operator used in boolean expression for the named option is not support. The supported operator list is: (,), ~, &, |, ^, !.

What Next

Check the boolean expression for the named option in command create_power_switch.

UPF-023

(error) Missing close blacket in boolean expression '%s' for option '%s' in command create_power_switch.

Description

Missing close blacket in boolean expression for the named option in command create_power_switch.

What Next

Check the boolean expression for the named option in command create_power_switch.

Feedback

UPF-024

(warning) The state probability of net '%s' specified in the state boolean function for command create_power_switch is not set. Set to be 0.5.

Description

The state probability of nets should have been set at the beginning of power calculation in PrimePower.

What Next

Contact Synopsys Customer Support Center if needed.

UPF-025

(warning) The state probability of net '%s' specified in the state boolean function for command create_power_switch is %.3f. This is not acceptable. Set to be 1.0.

Description

An internal rare error has occurred. The state probability of a net cann't exceed 1.0.

What Next

Contact Synopsys Customer Support Center if needed.

UPF-026

(Information) Overwriting the voltage on nets

Description

The specified nets already have a voltage set on them. This new set_voltage command will overwrite the voltage values on all the specified nets.

This could happen, if you have already set a voltage explicitly on the given nets or internally, we propagate the set_voltage on all net segments.

What Next

If you think the voltages are propagated incorrectly in the tool, check the supply_net connections using report_power_network command.

UPF-027

(warning) Power domain '%s' instantiated cells from library '%s' that do not have PG pins.

Feedback

Description

The cells in the extent of the power domain do not have PG pins. Any set_voltage on UPF supply net is ignored and design operating conditions, and library default voltages are used instead.

What Next

It is recommended to use libraries with PG pins for low-power flow. Contact Synopsys Customer Support Center if needed.

UPF-028

(error) '%s' is not supported in UPF mode.

Description

The set_rail_voltage command and -object_list option of set_operating_conditions command are not supported in UPF mode.

What Next

Please use set_voltage to specify voltages and set_temperature to specify temperatures.

UPF-029

(warning) There are '%d' supply nets without set_voltage.

Description

Each supply net segment must have set_voltage defined. Supply net segment is a continuous metal connection through ports separated by switches.

The voltage needs to be set even on ground nets (typically 0.0) since UPF create_supply_net does not yet distinguish supply and ground nets.

If not specified, individual power and ground pins of cell instances connected to such nets are treated as unconnected during delay calculation (thus might default to library voltage map - see man set_voltage, effectively discarding any UPF power domains, isolation, retention, connectivity etc.).

What Next

Use check_timing -verbose -include supply_net_voltage to list the nets without set_voltage and set_voltage on each listed net.

See Also

- create_supply_net
- set_voltage

UPF-030

(Warning) There are '%d' unconnected power and ground pins.

Description

Power and ground pins of each cell instance should be connected to supply nets. If not connected, delay calculation thus might default to library voltage map - see man *set_voltage*, effectively discarding any UPF power domains, isolation, retention, connectivity etc.).

The connectivity of power supply nets is specified by UPF commands including *create_power_domain* (use *help upf* to list the commands).

What Next

Use *check_timing -verbose -include unconnected_pg_pins* to list the pg pins. Then use *report_power_pin_info*, *report_power_domain* and other UPF commands to find out why the pg pin is not connected.

See Also

- create_power_domain
- report_power_domain
- report_power_pin_info

UPF-031

(error) The specified %s is not available in the given power domain

Description

It is required that the supply nets should be available in the specified power domain for the command to succeed.

What Next

Check the supply nets and where they are created. Rerun the command with the nets that are available in this domain.

Feedback

See Also

- create_power_domain
- create_supply_net
- report_power_domain
- report_supply_net
- report_power_pin_info

UPF-032

(error) Inside/outside connection of supply port %s is already established/cannot be established to supply net %s.

Description

A supply port can only be connected by one supply net at each side (inside/outside).

Also, the top-level ports cannot have a connection to any net from a different scope.

What Next

Check the connections that have been already made.

See Also

- create_supply_net
- connect_supply_net

UPF-033

(warning) PG pin

Description

The PG pin of a cell should be connected to an appropriate supply net. Such connection can either be created through explicit connection or through auto-connection semantics. Missing PG connection can lead to incorrect power analysis results. This error could be caused by incorrect/incomplete UPF commands.

What Next

Check the UPF commands for the design.

See Also

- create_power_domain
- create_supply_net
- connect_supply_net
- report_power_domain
- report_supply_net
- report_power_pin_info

UPF-034

(error) The '%s' option must refer to signal and sense.

Description

This option must be specified in format {net high|low|posedge|negedge}.

What Next

Make sure the net exists in the current scope and that signal type is properly defined.

UPF-035

(error) Cannot override supply net %s by %s on retention %s.

Description

The UPF standard does not allow overriding of supply nets. Supply nets can only be layered (i.e., added to an existing retention that does not have the supply net defined).

What Next

Make sure that your previous set_retention command either does not have the supply nets or it is same as this command.

See Also

- set_retention

UPF-036

(error) Cannot override save/restore net or objects of retention %s.

Feedback

Description

The UPF standard does not allow overriding of save, restore signal or objects.

What Next

Make sure that this is the first set_retention command for the strategy in this domain.

See Also

- set_retention

UPF-037

(error) No retention strategy %s in domain %s.

Description

The set_retention_control can be only applied to existing retention strategy.

What Next

Create the retention strategy by set_retention.

See Also

- set_retention
- set_retention_control

UPF-038

(Error) % is not a valid voltage level reference_name for supply group %s.

Description

You are receiving this error message because a set_voltage command has been specified with a -reference_name argument that does not reference any of the valid voltage level labels for the supply group the command operated on. The voltage level labels must be setup using the set_voltage_levels command.

What Next

Use the report_supply_group command to check what levels have been defined. Use the set_voltage_levels command to adjust the levels as needed.

Feedback

UPF-040

(Error) Level reference_name '%c' contains illegal characters.

Description

You are receiving this error message because you specified a voltage level reference_name that contains special characters in it's name. Only '_', '.' and alphanumerical characters are allowed.

What Next

Re-issue the command using a compliant reference_name for the voltage level.

UPF-041

(Error) Voltage levels have already been assigned for supply_group '%s'.

Description

You are receiving this error message because you attempted to assign voltage level labels to a supply_group that had the labels already defined.

What Next

You can use set_voltage_levels -reset to remove the existing voltage level assignment if the supply_group has not been used in a get_dvfs_scenarion command yet. Afterwards reissue this comamnd.

UPF-042

(Error) Failed to reset voltage levels on supply_group '%s'.

Description

You are receiving this error message because you attempted to reset voltage level reference_names on a supply_group that was already used in one or more get_dvfs_scenarion commands.

What Next

Once you start using a supply group in one or more get_dvfs_scenarion commands you can no longer redefine the voltage levels on it unless you issue reset_design.

UPF-043

(Warning) Changing voltage levels invalidates pre-exisitng instance specific voltages.

Feedback

Description

When using voltage levels on supply_groups a command sequence must be followed where first all voltage levels are defined using the *set_voltage_levels* command and only then instance specific voltages using *set_voltage -cell -pg_pin_name -reference_name* are specified. If instance specific voltages exist when supply_group levels are changed they are discarded.

What Next

Reorder the commands in your script such that all *set_voltage_levels* commands are specified before using *set_voltage -cell -pg_pin_name -reference_name*

See Also

- set_voltage_levels
- set_voltage

UPF-044

(Error) Mismatched reference_name semantics for set_voltage.

Description

When setting instance specific voltages the syntax of the *set_voltage* command must match the supply_net associated with the pg_pin specified. I.e. if the supply_net has voltage_levels defined on it the *set_voltage* command must use the -reference_name option. If the supply_net does not have levels defined on it then the *set_voltage* command must not use the -reference_name option. This implies that you can not use the -reference_name option on a pg_pin that has no associated supply net.

What Next

Change the syntax of the set_voltage_command you are using such that it matches the state of the supply_net associated witht the pg_pin specified.

See Also

- set_voltage_levels
- set_voltage

UPF-045

(error) Cannot override supply net %s by %s on isolation %s.

Feedback

Description

The UPF standard does not allow overriding of supply nets. Supply nets can only be layered (i.e., added to an existing isolation that does not have the supply net defined).

What Next

Make sure that your previous set_isolation command either does not have the supply nets or it is same as this command.

See Also

- set_isolation

UPF-046

(error) Cannot override signal net or elements of isolation %s.

Description

The UPF standard does not allow overriding of isolation signal or elements.

What Next

Make sure that this is the first set_isolation command for the strategy in this domain.

See Also

- set_isolation

UPF-047

(error) No isolation strategy %s in domain %s.

Description

The set_isolation_control can be only applied to existing isolation strategy.

What Next

Create the isolation strategy by set_isolation.

See Also

- set_isolation
- set_isolation_control

Feedback

UPF-048

(Warning) Creating supply %s of name %s while logic %s of the same name already exists

Description

The IEEE 1801 UPF standard requires that UPF supply objects have different names than signal (or logic) netlist objects. There are two possible causes of this warning:

1. PrimeTime intepretation of PG (power or ground) supply nets, ports in Verilog as signal objects 2. Name space conflict between logic nets or ports and UPF supply objets.

What Next

Verify that the logic net or port are intended as supply objects. Then the warning can be ignored.

If the logic nets or ports are intended as part of signal paths (not PG) then correct the UPF file to use different object name to comply with IEEE 1801 (UPF) standard.

UPF-050

(Error) Variable %s can't be changed after library loading.

Description

The named variable impacts library loading. Once library is loaded, this variable has no impact on the tool. To show the consistency between the variable value and the library data loaded, it is not allowed to change the variable once the library is loaded.

What Next

If needed, you can remove the loaded libraries by issueing

remove_lib -all

and then set the variable.

UPF-051

(error) Explicit connection can not be made to the PG pins of cell '%s' (library cell '%s'). The PG pins of this library cell are added based on the default PG pin names by the tool.

Description

The library used is a non-PG pin library. The cell PG pins are added based on the default PG pin names by the tool. Since these PG pins are not defined in the library, explicit supply net connections can not be made to them.

Feedback

What Next

Create Liberty PG pin based .lib libraries.

See Also

- connect_supply_net

UPF-052

(Error) Explicit connection can not be made to PG pin '%s' as it is an internal PG pin of cell '%s' (library cell '%s').

Description

The PG pin is an internal PG pin of a fine-grain switch cell. Explicit supply net connection can only be made to non-internal PG pin of the cell.

See Also

- connect_supply_net

UPF-059

(error) UPF PG pin connection of cell %s cannot be established to supply net %s.

Description

Please check if the supply net is available in the power domain where the cell belongs to.

What Next

Check the connections that have been already made.

See Also

- create_supply_net
- connect_supply_net

UPF-060

(error) The '%s' option of create_supply_set command must specify exactly one pair of %s.

Feedback

Description

This option of create_supply_set command takes exactly one predefined supply function name and the corresponding supply net.

What Next

Check the command man page for more details and correct it accordingly.

UPF-061

(error) Unknow function name '%s' specified for create_supply_set

Description

Tool only supports 'power' and 'ground' predefined function names for create_supply_set.

What Next

Check the command man page for more details and correct it accordingly.

UPF-062

(warning) The voltage values of supply net handle '%s' do not match the voltage values of supply net '%s'.

Description

This warning message occurs when the supply net used for update has different voltage values than the specified supply set function. The voltage values set on the specific supply set function are overwritten by the values on the supply net used for update.

What Next

Make sure that the voltage set on the supply net used for update and the voltage set on the specified supply set function are equal.

See Also

- create_supply_set
- set_voltage

UPF-063

(error) '-function' option is not specified for supply set update.

Feedback

Description

When a supply set is updated with create_supply_set -update, -function option must be specified to provide the associated supply nets with supply set functions.

What Next

Check the command man page for more details and correct it accordingly.

UPF-065

(error) Hierarchical name %s cannot be directly specified for the object created by this command.

Description

This error message occurs when a hierarchical name is specified for the object created by this command.

Only simple names, without a slash (/), are permitted for the object created by this command. The created object automatically has its hierarchical name based on the scope instance in which it is created. For example, an object with the simple name of 'A' created in scope U1/U2/U3 (relative to the top) will have a hierarchical name of U1/U2/U3/A.

What Next

Use a simple name for the object and rerun the command.

UPF-066

(error) Cannot override supply set %s by %s on isolation %s.

Description

The UPF standard does not allow overriding of supply set. Supply set can only be layered (i.e., added to an existing isolation that does not have the supply set defined).

What Next

Make sure that your previous set_isolation command either does not have the supply sets or it is same as this command.

See Also

- set_isolation

Feedback

UPF-067

(error) Cannot override supply set %s by %s on retention %s.

Description

The UPF standard does not allow overriding of supply set. Supply set can only be layered (i.e., added to an existing retention that does not have the supply set defined).

What Next

Make sure that your previous set_retention command either does not have the supply set or it is same as this command.

See Also

- set_retention

UPF-068

(error) Hierarchical name '%s' cannot be directly specified for %s object in command %s.

Description

This error message occurs when a hierarchical name is specified for the object in the specific command.

Only simple names are permitted for the object in this specific command.

What Next

Use a simple name for the object and rerun the command.

UPF-069

(error) %s name '%s' in connect_supply_net cannot have a wild char '*'

Description

This error message occurs when a wild char '*' in connect_supply_net command's net or port name. The wild char is not allowed according to IEEE 1801.

What Next

Remove the wid char from connect_supply_net command.

Feedback

UPF-070

(error) Variable '%s' can not be changed after power domains are created.

Description

This variable must be set before creating the power domains. After creating the power domains, this variable is considered read-only.

What Next

Check the variable man page for more details and correct it accordingly.

UPF-071

(error) %s is not supported because supply handles are disabled.

Description

This error message occurs when you execute a command (with options) that is supported only when supply handles are enabled. To enable supply handles, use variable upf_create_implicit_supply_sets.

What Next

Please correct the command accordingly or enable supply handles.

See Also

- create_power_domain
- set_design_attributes
- upf_create_implicit_supply_sets

UPF-072

(error) PG pin database is missing.

Description

This error message occurs when you activate the Golden UPF mechanism after link. The Golden UPF feature needs to create a database of PG pins during link. To activate the Golden UPF feature, set variable enable_golden_upf before link.

What Next

Please set the variable enable_golden_upf before the link phase.

Feedback

See Also

- enable_golden_upf

UPF-073

(error) Mismatch between verilog PG and UPF commands.

Description

This error message occurs when you activate the Golden UPF mechanism and there is a mismatch between verilog PG nets and UPF supply nets.

What Next

Please check that the verilog contains PG connections and correct net names are used in UPF commands.

See Also

- enable_golden_upf

UPF-074

(information) UPF net '%s' does not exist in PG netlist of the current design.

Description

This error message occurs during the Golden UPF flow, when a UPF supply net is created but does not exist in the current design.

What Next

Please correct the UPF net name accordingly to your design.

See Also

- enable_golden_upf

UPF-075

(Information) Signal pin %s will be connected to constant net *Logic%d* as it was on a PG-net.

Description

If a signal pin is connected to a PG net, after PG-stripping in link, the pin is connected to either *Logic0* or *Logic1* net, depending on if the PG-net is a power or groung net.

Feedback

What Next

No action is necessary.

See Also

- enable_golden_upf

UPF-076

(error) Variable '%s' can not be changed after set_voltage_levels command has been issued.

Description

This variable must be set before assigning voltage_levels to supply_groups. After assigning the voltage levels, this variable is considered read-only.

What Next

Remove the voltage level assignments for all supply_groups using set_voltage_levels -reset. Or preferably reorder your UPF commands such that the pg network is compeltely specified including setting of this variable before specifying voltage_levels.

UPF-077

(error) The '%s' command can not be applied once voltage levels have been assigned.

Description

Once a supply net had voltage levels assigned by the set_voltage_levels command it can no longer be reconnected using the connect_supply_net or set_equivalent commands. If any of the supply_nets referenced by these commands already had voltage levels assigned the command fails and no reconnection is performed.

What Next

Remove the voltage level assignments for all supply_groups using set_voltage_levels -reset. Or preferably reorder your UPF commands such that the pg network is compeltely specified including connect_supply_net or set_equivalent commands before specifying voltage_levels.

UPF-078

(warning) There are '%d' supply groups missing set_voltage_levels.

Feedback

Description

Each supply group must have set_voltage_levels defined for each voltage level.

What Next

Use the report_supply_group command to report which voltage levels have not been defined for the supply group and use the set_voltage_levels command to assign voltage levels.

See Also

- report_supply_group
- set_voltage_levels

UPF-079

(error) Primary net in 'set_equivalent' command has to be one the nets mentioned in '-nets' option.

Description

When creating equivalent supply nets if '-primary_net' option is used then it should be specified from the list of nets for which equivalence is being created.

What Next

Use one of the nets from the list of nets of '-nets' option as primary net.

See Also

- report_supply_group
- set_voltage_levels

UPF-102

(error) The pin '%s' specified in '%s' as defined for userdefined attribute '%s' of pin '%s' is not defined for library cell '%s'. The '%s' cannot be interpreted thus ignored.

Description

The userdefined function attributes specifies the Boolean condition. special_function_clocked_logic, value as function of input pins post latency of trigger event. special_function_asynch_logic takes precedence over clocked function if applicable. Cell is asynchronously updated on all stages simultaneously(asynchronous reset). Supported only in time_based mode.

If the special_function_clocked_logic are not interpreted, propagation through synchronizer cell is not possible as functionality cannot be properly inferred from library view - marked as black boxes. It must refer to valid input pins of the cell.

What Next

Provide a correct specification for the userdefined function attributes in the .lib for output pin.

UPF-103

(error) Invalid specification '%s' for userdefined attribute '%s' of pin '%s' for library cell '%s'. The '%s' is ignored.

Description

The specification for the userdefined function is not a valid Boolean expression.

special_function_clocked_logic, value as function of input pins post latency of trigger event. special_function_asynch_logic takes precedence over clocked function if applicable. Cell is asynchronously updated on all stages simultaneously(asynchronous reset). Supported only in time_based mode.

If special_function_clocked_logic is ignored, propagation through synchronizer cell is not possible as functionality cannot be properly inferred from library view - marked as black boxes.

What Next

Check the Boolean expression for the userdefined attributes : special_function_clocked_logic and special_function_asynch_logic.

Provide a correct specification for the userdefined function attribute in the .lib for output pin.

UPF-104

(error) Boolean expression exceeds length limit for userdefined attribute '%s' of pin '%s' for library cell '%s'. The current length limit is 2048 characters. The '%s' is ignored.

Description

The current length limit for userdefined function Boolean expression is 2048 characters. special_function_clocked_logic, value as function of input pins post latency of trigger event. special_function_asynch_logic takes precedence over clocked function if applicable. Cell is asynchronously updated on all stages simultaneously(asynchronous reset). Supported only in time_based mode.

If special_function_clocked_logic is ignored, propagation through synchronizer cell is not possible as functionality cannot be properly inferred from library view - marked as black boxes.

What Next

Check the Boolean expression for the userdefined attributes : special_function_clocked_logic and special_function_asynch_logic.

If needed, contact Synopsys Customer Support Center.

Provide a correct specification for the userdefined function attribute in the .lib file for output pin.

UPF-105

(error) Unknown function operator '%c' in boolean expression '%s' for '%s' of pin '%s' for library cell '%s'. The '%s' function is ignored.

Description

The operator used in the Boolean expression for userdefined function is not supported. The following operators are allowed: (,), ~, &, |, ^, !. special_function_clocked_logic, value as function of input pins post latency of trigger event. special_function_asynch_logic takes precedence over clocked function if applicable. Cell is asynchronously updated on all stages simultaneously(asynchronous reset). Supported only in time_based mode.

If the special_function_clocked_logic are not interpreted, propagation through synchronizer cell is not possible as functionality cannot be properly inferred from library view - marked as black boxes.

What Next

Check the Boolean expression for the userdefined attributes : special_function_clocked_logic and special_function_asynch_logic.

Provide a correct specification for the userdefined function attribute in the .lib file.

UPF-106

(error) Missing close bracket in Boolean expression '%s' for '%s' of pin '%s' for library cell '%s'. The '%s' is ignored.

Description

The close bracket (]) in the Boolean expression is missing for userdefined function attribute. special_function_clocked_logic, value as function of input pins post latency of trigger event. special_function_asynch_logic takes precedence over clocked function if

Feedback

applicable. Cell is asynchronously updated on all stages simultaneously(asynchronous reset). Supported only in time_based mode.

If the special_function_clocked_logic are not interpreted, propagation through synchronizer cell is not possible as functionality cannot be properly inferred from library view - marked as black boxes.

What Next

Check the Boolean expression for the userdefined function attribute: special_function_clocked_logic and special_function_asynch_logic.

Provide a correct specification for the userdefined function attribute in the .lib file for the output pin.

UPF-121

(error) Supply port %s cannot be created at the logical instance %s.

Description

This error message occurs when a hierarchical name is specified as a supply port, but the logical instance path is invalid for the scope instance.

A scope instance must already exist and cannot be a leaf cell.

What Next

Use the *get_cells* command to verify that the scope instance exists. Make sure that the scope instance is not a leaf cell.

See Also

- get_cells

UPF-144

(information) Retention strategy '%s' specifies no elements with the -no_retention option.

Description

This warning message occurs because a *set_retention* command has no objects specified with the *-no_retention* option. None of the registers in the strategy's power domain will have retention unless other retention strategies specify objects for retention.

What Next

This is an information-only message. No action is required.

Feedback

However, you might want to check whether elements should be specified.

See Also

- set_retention

UPF-149

(warning) Retention strategy '%s' does not need a retention control command as it is -no_retention.

Description

This warning message occurs when a retention strategy is *-no_retention*. No *set_retention_control* command is needed for this strategy. It will be ignored.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, check the correctness of the *set_retention* and *set_retention_control* commands.

See Also

- set_retention
- set_retention_control

UPF-150

(warning) Retention strategy '%s' specifies power net(s) despite -no_retention option.

Description

This warning message occurs because a *set_retention* command was issued with the *-retention_power_net* and/or *-retention_ground_net* options while also using the *-no_retention* option. If no retention is desired, special power supply nets are not required. They will be ignored.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, check whether you really wanted no retention or actually planned to specify retention in this strategy, and adjust the command accordingly.

See Also

- set_retention

UPF-151

(Error) Supply independent upf_supply_net cannot be attached to a domain.

Description

UPF supply nets can be declared as domain dependent or domain independent. Once declared without a domain, the supply net cannot be attached to a particular domain, but instead are available for all domains in the scope in which the supply net was declared.

See Also

- create_supply_net

UPF-152

(Error) The supply set handle '%s' is invalid.

Description

The supply set handle is used to identify the role a supply set takes in the power domain. Valid supply set handles include 'primary', 'default_retention', 'default_isolation', and the unused role 'extra_supplies_#', where '#' is a number.

See Also

- create_power_domain

UPF-153

(Error) The supply set handle '%s' can be attached to only one supply set.

Description

The *-supply* option to *create_power_domain* attaches a single supply set to a supply set handle. Only one supply set can be attached to a given handle.

See Also

- create_power_domain

Feedback

UPF-162

(warning) The supply function %s of the supply set '%s' is already defined and cannot be changed.

Description

This warning message occurs when the supply set function has already been specified once. Another update on the same function is not allowed and is skipped by the tool.

What Next

This is only a warning message. No action is required.

See Also

- create_supply_set

UPF-171

(error) Supply set '%s' is not available in the scope where the power domain is being created.

Description

This error message occurs because the *create_power_domain* command with the *-supply* option specifies a supply set that is not available in the scope of the power domain.

What Next

Ensure that the command references a supply set that is available in the scope of the power domain.

See Also

- create_power_domain
- create_supply_set

UPF-175

(error) Supply set '%s' is not available in the scope of the power domain.

Description

This error message occurs when the supply set specified with either the *-isolation_supply_set* or the *-retention_supply_set* option is not available in the scope of the specified power domain.

What Next

Use a supply set that is available in the scope of the power domain specified with *set_isolation* or *set_retention* for the *-isolation_supply_set* or *-retention_supply_set* option.

See Also

- set_isolation
- set_retention
- create_supply_set

UPF-179

(error) Supply net '%s' in scope '%s' cannot be used for creating or updating the supply set.

Description

This error message occurs when a supply net from an incorrect scope is used to create or update the supply set. The scope of the supply net chosen for supply set functions must match with the scope of the supply set.

What Next

Make sure that the supply nets are created in the correct scope.

See Also

- create_supply_set

UPF-180

(error) Supply net '%s' is not domain independent.

Description

This error message occurs when a domain dependent supply net is used to update an explicitly created supply set. The domain dependent supply net is defined for a specific domain.

Only domain independent supply nets can be used to update explicitly created supply sets.

What Next

Use a domain independent supply net and run the command again.

Feedback

See Also

- create_supply_net
- create_supply_set

UPF-185

(warning) Found non top-level design element(s) '%s' specified for '-driver_supply/-receiver_supply' attribute. The attribute on invalid design element is ignored.

Description

This warning message occurs when non top-level design elements are specified for -elements option in command *set_port_attributes*. The non top-level design elements are filtered out from user specified list and ignored.

What Next

Check the command man page for more details and correct it accordingly.

UPF-200

(error) Symbol '%s' violates the UPF naming conventions.

Description

This error message occurs when an argument violates the identifier naming conventions of UPF.

What Next

The first character of an UPF identifier shall be alphabetic. All other characters of the identifier must be either an alphanumeric character, "A-Z a-z 0-9", or the underscore character, "_". UPF names are case sensitive.

UPF-201

(error) Power domain '%s' cannot be assigned a primary or ground supply net because it was created with a primary supply set.

Description

The primary power and ground supply nets are derived from the assigned primary supply set.

Feedback

What Next

The primary supply nets of a power domain cannot be changed once assigned. Do not attempt to set them.

UPF-270

(Error) Option '-%s' cannot be specified for %s '%s'.

Description

This error message occurs when the option specified is not compatible for the selected object.

UPF-271

(warning) Following objects do not reside in current scope: %s

Description

This warning message occurs when there are one or more objects to be reported by query commands, but they do not reside in the current scope. Such objects are filtered out and names of objects that reside in the current scope are returned.

What Next

Check the current scope and then reinvoke the command.

UPF-300

(error) lack arguments in set_single_upf_naming

Description

set_single_upf_naming command needs at least one arguments, either -hierarchical_separators, -bus_name_notations, -class, -reset, -show, or -verbose.

What Next

Check set_single_upf_naming command.

UPF-301

(error) %s option needs a list with at least 2 elements

Description

The option in set_single_upf_naming command needs a list with at least 2 elements.

Feedback

What Next

Check set_single_upf_naming command.

UPF-302

(error) -class option needs a list with at least 1 elements

Description

The -class option in set_single_upf_naming command needs a list with at least 1 elements.

What Next

Check set_single_upf_naming command.

UPF-303

(error) -reset option conflicts with -hierarchical_separators or -bus_name_notations

Description

The -reset option in set_single_upf_naming conflicts with -hierarchical_separators or -bus_name_notations. You can oly specify -reset wihtout -hierarchical_separators and -bus_name_notations.

What Next

Check set_single_upf_naming command.

UPF-304

(error) Bus notation %s doesn't have exact two characters

Description

Bus notation string elemenent in set_single_upf_naming -bus_name_notation must have exact two characters.

What Next

Check set_single_upf_naming command.

UPF-305

(error) Bus notation %s doesn't have exact same two characters

Feedback

Description

Beside paired characters such as "[]", "{}", "()" and "<>", bus notation string elemenent in set_single_upf_naming -bus_name_notation must have exact two same characters.

What Next

Check set_single_upf_naming command.

UPF-306

(error) Bus notation %s has an illegal character

Description

Bus notation string in set_single_upf_naming -bus_name_notation cannot have the following characters: A-Z, a-z, 0-9, '*', '?', '\\', '+', '^' and '/'.

What Next

Check set_single_upf_naming command.

UPF-307

(error) Hierarchical separator %s is an illegal character

Description

A hierarchical separator in set_single_upf_naming -hierarchical_separators cannot have the following characters: A-Z, a-z, 0-9, '*', '?', '\\', '+', '^', '(', ')', '<', '>', '{', '}', '[', ']'.

What Next

Check set_single_upf_naming command.

UPF-308

(error) Class name %s is illegal

Description

A class name in set_single_upf_naming -class can only be "cell", "net", "port" or "pin".

What Next

Check set_single_upf_naming command.

Feedback

UPF-309

(error) Miss a hierarchical separator which should be same as the variable hierarchy_separator

Description

In pt_shell there is a variable "hierarchy_separator". One of hierarchical separators in set_single_upf_naming -hierarchical_separators should be same as the one set by the "hierarchy_separator" variable.

What Next

Check set_single_upf_naming command.

UPF-310

(error) incorrect object type in set_isolation -element

Description

The object type of -element in set_isolation is either pin or port. This error indicates a wrong object type is used.

What Next

Check set_isolation -element in your script.

UPF-407

(error) Command %s requires one of the %s options to be used.

Description

This error message occurs when the specified command is used with less than the required number of options.

What Next

Look into the man page of the specified command and use the required options.

UPF-408

(warning) The voltage of driving cell '%s' (%.3f) does not match the related supply voltage at port '%s' (%.3f).

Feedback

Description

This error message occurs when the operating voltage of the driving cell of the port, does not match the voltage of the related supply of the port.

The driving cell is specified by command *set_driving_cell*. The voltage of the cell is derived from one of the following parameters:

```
PG signal level of the output pin
Related PG pin's voltage
Nominal voltage of the cell's library
```

The related supply of the port is specified by command *set_port_attributes* and its voltage are set by command *set_voltage*.

What Next

Make sure that the cell from the correct library matching the operating condition of the design is used in the *set_driving_cell* command.

See Also

- set_port_attributes
- set_voltage
- set_driving_cell

UPF-409

(warning) Port '%s' %s supply '%s' does not match the supply of the visible logic.

Description

This warning message occurs when the actual supply of the cell pin that connected to the port, does not match the corresponding supply attribute specified on the port through set_port_attributes command.

What Next

Make sure that set_port_attrubutes is set correctly on the port.

See Also

- set_port_attributes

UPF-420

(error) Cannot use -location fanout for isolation strategy %s

Feedback

Description

The -location fanout in set_isolation_control can only be used with the isolation strategy which has -source, -sink or -diff_supply_only true option. This error indicated that in the specified strategy there is neither -source, -sink, nor -diff_supply_only but in its set_isolation_control -location fanout is used.

What Next

Make sure that the isolation strategy has -source, -sink or -diff_supply_only true.

See Also

- set_isolation

UPF-421

(error) supply net/set for isolation strategy %s is missing

Description

Beside -location fanout in set_isolation_control, a power/ground net or supply set must be specified for an isolation strategy. This error indicated that in the specified strategy there is neither -isolation_power_net, -isolation_ground_net, nor -isolation_supply_set but in its set_isolation_control -location self or -location parent is used.

What Next

Make sure that the isolation strategy has supply net or supply set.

See Also

- set_isolation

UPF-422

(error) supply net/set for isolation strategy %s is not available

Description

The supply net/set in the specified isolation strategy is not available in the fanout load domain.

What Next

Make sure that the isolation strategy has correct supply net or supply set.

See Also

- set_isolation

UPF-426

(error) Only senses "high" and "low" are supported for option '%s'.

Description

This error message occurs when the sense specified with the '%s' option is neither "high" nor "low".

What Next

Check the command man page for more details and correct it accordingly.

UPF-531

(error) Cell %s was already assigned the isolation strategy %s before %s for %s pins.

Description

This error message occurs when using the *set_isolation* command and a cell is listed in the elements list of more than one isolation strategy referring the same pin direction. You may not explicitly include the same cell in multiple isolation strategies for the same pin direction.

What Next

Ensure that all cells are included in only one isolation strategy for each pin direction. For instance, if strategy iso_1 defines isolation on output pins of cell A, it is not allowed to define a new strategy iso_2 on cell A using the *-applies_to outputs* or *-applies_to both* option.

See Also

- set_isolation

UPF-532

(warning) The -applies_to option of isolation strategy %s has been ignored for at least 1 pin.

Feedback

Description

This warning message occurs when you define an isolation strategy that combines the *-applies_to* and *-elements* options, and at least 1 pin is listed in the *-elements* list whose direction does not match with the direction implied in the *-applies_to* option.

What Next

This is only a warning message. No action is required.

However, if the result is not what you intended, make sure that the isolation strategy is applied to all pins listed in the isolation strategy, particularly on those whose direction does not match the restriction implied by the *-applies_to* option. If only pins are listed in the strategy, consider removing the *-applies_to* option from the strategy. If pins and root cells are listed in the strategy, consider separating the original strategy into 2, with 1 listing only pins and the other listing cells and the additional *-applies_to* option.

See Also

- set_isolation

UPF-533

(error) Design element %s is not on boundary of domain %s.

Description

This error message occurs when attempting to specify a design element in the *-elements* option of the *set_isolation* command that is not a root cell of the power domain for which the isolation strategy is being defined.

What Next

Look at the design element in the error message, verify that it is not a root cell of the power domain, and change it to the root cell to which the isolation strategy applies.

See Also

- set_isolation

UPF-534

(warning) Pin %s is set by two isolation strategies %s and %s. %s is ignored.

Feedback

Description

A pin can only be set by one isolation strategy. If it's set by multiple ioslation strategies, the tool will decide to take which one according to the precedence and report which one is ignored.

What Next

Look at two isolation strategies mentioned in the warning message and make sure the ignored one is correct for the specified pin.

See Also

- set_isolation

UPF-535

(warning) UPF Commands are ignored outside load_upf when HyperScale is enabled.

Description

When PrimeTime hierarchical analysis is being used, limited UPF support is available. UPF commands outside load_upf are ignored.

What Next

Create upf files for blocks and for the top level design.

UPF-536

(Warning) The specified scope %s could not be found. The instance may have been removed from the design. UPF commands will be disabled until the next invocation of set_scope.

Description

When PrimeTime hierarchical analysis is being used, limited UPF support is available. The command *set_scope* may fail to find an instance if it is not included at the top level of the design. In this case, commands following *set_scope* will fail until the next successful *set_scope* commmand. The scope from the failing *set_scope* command will be remembered for later use if relative paths are used in the following *set_scope* command.

UPF-537

(error) Isolation strategy %s uses -source, -sink and -diff_supply_only true together

Feedback

Description

The three options -source, -sink and -diff_supply_only true in set_isolation command cannot be used together.

What Next

Look at the isolation strategies mentioned in the error message and remove one of options.

See Also

- set_isolation

UPF-538

(warning) Isolation strategy %s applies to nothing

Description

No any isolation cells can be found to associate with the specified isolation strategy.

What Next

Look at your design.

See Also

- set_isolation

UPF-539

(error) Isolation strategy %s uses -element pin/port with -source, -sink or -diff_supply_only true

Description

The three options -source, -sink and -diff_supply_only true in set_isolation command cannot be used with -element pin/port.

What Next

Look at the isolation strategies mentioned in the error message and remove one of options.

See Also

- set_isolation

Feedback

UPF-540

(warning) Attribute %s in %s is ignored

Description

PrimeTime Suite Tools only understand a limited number of UPF attributes. This message reports the specified attribute is not recongized by the tool and is ignored.

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

UPF-541

(warning) Attribute %s in %s is redefined

Description

The specified UPF attribute is redefined. The previous one wins and the later one is ignored.

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

UPF-542

(error) Attribute iso_source in set_port_attributes can only apply to input

Description

The attribute iso_source in set_port_attributes can only apply to input port.

What Next

Look at your UPF.

Feedback

See Also

- set_port_attributes

UPF-543

(error) Attribute iso_sink in set_port_attributes can only apply to output

Description

The attribute iso_sink in set_port_attributes can only apply to output port.

What Next

Look at your UPF.

See Also

- set_port_attributes

UPF-544

(error) attribute value %s has too many supply set

Description

The attribute iso_source/iso_sink in set_port_attributes can only have one supply set.

What Next

Look at your UPF.

See Also

- set_port_attributes

UPF-545

(error) attribute value %s doesn't have a pair of supply nets

Description

The attribute iso_source/iso_sink in set_port_attributes can only have one pair of supply nets.

What Next

Look at your UPF.

Feedback

See Also

- set_port_attributes

UPF-546

(error) Cannot find supply set %s in set_port_attributes

Description

The specified supply set in set_port_attributes is not found. The attribute value of iso_source/iso_sink in set_port_attributes must be either a pre-defined supply set or a pre-defined supply net pair (power net and ground net).

What Next

Look at your UPF.

See Also

- set_port_attributes

UPF-547

(error) UPF attribute in set_design_attributes cannot set on cell %s

Description

In UPF command set_design_attributes, attribute "merge_domain" and "external_supply_map" can only be set on cells that are hierarchical cells, macros, pads or black boxes.

What Next

Look at your UPF and make sure your cell is not a leaf cell.

See Also

- set_design_attributes

UPF-548

(warning) Attribute related_supply_default_primary with value false is not supported

Feedback

Description

For the related_supply_default_primary attribute in set_port_attribute PrimeTime Suite Tools only supports the value TRUE. This warning inddicates you set it to FALSE which the tool is not supported and it will be ignored.

What Next

Set the attribute value to TRUE.

See Also

- set_port_attributes

UPF-549

(error) Supply set '%s' is already associated or refined.

Description

A supply set cannot be associated with multiple sets.

What Next

Check the command for intended behavior

UPF-550

(error) Supply set '%s' can not be found.

Description

Please check the supply set specified for the command. Make sure that the supply set exists in the current_scope.

What Next

Check the command man page for more details and correct it accordingly.

UPF-551

(error) Supply set '%s' specified is not a set handle

Description

Only a supply set handle can be specified for the -handle option in associate_supply_set command.

Feedback

What Next

Check the command for intended behavior

UPF-552

(error) Association of a supply set '%s' can be done only if it is neither associated nor updated.

Description

Association of a supply set specified using the -handle attribute in associate_supply_set command can be done only if it is neither associated nor updated.

What Next

Check the command for intended behavior

UPF-553

(error) Supply set '%s' specified must be at or below the scope for supply set '%s'

Description

Supply set handle specified with the -handle option must be at or below the scope of the supply set it is being associated with.

What Next

Check the command for intended behavior

UPF-554

(error) Circular association - supply set '%s' is already associated with set '%s'

Description

Circular associations are not permitted between supply sets.

What Next

Check the command for intended behavior

UPF-555

(error) The name '%s' specified must correspond to exactly one power domain.

Feedback

Description

Please check the domain specified for the command

What Next

Check the command man page for more details and correct it accordingly.

UPF-556

(error) The -update attribute for command create_power_domain can only be specified with the -supply or -available_supplies attribute

Description

The -update attribute for create_power_domain command requires specification of a valid supply set using the -supply or -available_supplies attribute or a list of cells specified by the -elements option.

What Next

Check the command man page for more details and correct it accordingly.

UPF-557

(error) This command cannot be used to update Implicit Supply Sets without specifying the -update attribute

Description

It is an error to use create_supply_set command on Implicit Supply Sets without specifying the -update attribute

What Next

Check the command man page for more details and correct it accordingly.

UPF-558

(error) Supply set handle '%s' cannot be updated with a supply net handle

Description

When used on supply set handles, create_supply_set command can only be used to update to real supply nets, and not supply net handles.

What Next

Check the command for intended behavior

Feedback

UPF-559

(error) Supply net '%s' in scope '%s' cannot be used for creating or updating the supply set handle

Description

This error message occurs when a supply net from an incorrect scope is used to create or update a supply set handle. The scope of the supply net chosen for supply set functions must match with the highest scope for the supply sets in the group.

What Next

Make sure that the supply nets are created in the correct scope.

See Also

- create_supply_set

UPF-560

(error) attribute '%s' cannot be specified in power_domains_compatibility mode

Description

When power_domains_compatibility mode is set to TRUE, all UPF commands are disabled - power domain commands are enabled. To enable the attribute, set power_domains_compatibility to FALSE.

What Next

Set power_domains_compatibility to FALSE to allow use of this attribute in check_timing

UPF-562

(fatal) It is not allowed to use a domain dependent primary with an explicit supply set

Description

PrimeTime does not allow a domain dependent net and an explicit supply set to be specified together

What Next

Edit UPF script such that domain dependent nets and explicit supply sets are not specified together

Feedback

UPF-563

(Error) The domain %s specified has supply set handle creation disabled on it.

Description

The domain specified has supply set handle creation suppressed through the *suppress_iss* attribute of the *set_design_attributes* command

What Next

Check the command for correctness.

See Also

- set_design_attributes

UPF-564

(Error) The attribute suppress_iss cannot be set on power domain %s as it was previously created

Description

The given power domain already exists. The attribute *suppress_iss* must be set before the power domain is created.

UPF-565

(Error) The attribute suppress_iss cannot be specified more than once for a design

Description

The attribute *suppress_iss* has previously been specified. This attribute can only be specified once on a design.

UPF-567

(error) Connection of PG pin %s is already established/cannot be established to supply net %s.

Description

A PG pin can only be connected by one supply net. This connection cannot be overriden.

What Next

Check the connections that have been already made.

Feedback

See Also

- create_supply_net
- connect_supply_net

UPF-568

(Error) Explicit connection can not be made to bias pin '%s' of cell '%s' (library cell '%s') as its direction is '%s'

Description

The bias pin's direction is internal or output. Explicit supply net connection can only be made to input bias pin of the cell.

See Also

- connect_supply_net

UPF-569

(error) %s cell '%s' has the attribute value as '%s'. Cannot set the attribute value to '%s' on the %s cell.

Description

This error message occurs when an invalid configuration of the design attribute enable_state_propagation_in_add_power_state is detected. The valid attribute configurations are the following - 1. Attribute is set to FALSE for the entire design. 2. Attribute is set to TRUE for the entire design. 3. Attribute is set to TRUE for the block, and set to FALSE for the top design.

What Next

Look at your UPF.

See Also

- set_design_attributes
- add_pst_state
- create_supply_set

Feedback

UPF-570

(error) Use of %s is not allowed for the entire design or the block on which the attribute 'enable_state_propagation_in_add_power_state' of 'set_design_attributes' is enabled.

Description

Use of 'create_power_state_group' or '&&' in the 'supply_expr' of 'add_power_state' is not allowed for the entire design or the block on which the attribute 'enable_state_propagation_in_add_power_state' of 'set_design_attributes' is enabled.

What Next

Look at your UPF.

See Also

- set_design_attributes
- add_pst_state
- create_supply_set

UPF-571

(Warning) Ignoring logic_signal '%s==%s' in the -logic_expr '%s'.

Description

Logic signals in the '-logic_expr' of 'add_power_state' are read and ignored.

What Next

Review UPF setup.

See Also

- add_power_state

UPF-577

(Error) Parasitics corners cannot be set on non-hierarchical cell %s .

Description

This message is issued during a SMC run, when parasitic corners are set on leaf cells using *set_corner_parasitics*.

Feedback

What Next

Make sure there is no leaf cell in the cell list.

UPF-579

(Error) Parasitics corners must be set before reading parasitics.

Description

This message is issued during an SMC run, when parasitic corners are set after *read_parasitics*.

What Next

Make sure to set parasitics corners before reading parasitics. Or remove all parasitics and parasitics corners to set parasitics corners.

See Also

- remove_annotated_parasitics

UPF-600

(Error) The Golden UPF flow is not supported by HyperScale

Description

Golden UPF concept does not fit well in top down hierarchical flow because characterized UPF and the UPF from *propagate_constraints* are not the golden UPF user provides.

See Also

- enable_golden_upf

UPF-601

(Error) The -supplemental option of the load_upf command is only supported in Golden UPF flow

Description

The *-supplemental* option of the *load_upf* command is only supported in Golden UPF flow

See Also

- load_upf

Feedback

UPF-602

(Error) The -supplemental option is only supported when load_upf is executed in shell prompt.

Description

It is an error if the *-supplemental* option is used in embedded *load_upf* commands.

See Also

- load_upf

UPF-603

(Error) The Golden UPF flow does not support UPF commands executed in shell prompt.

Description

In Golden UPF flow non-query UPF commands can only be executed from *load_upf*.

See Also

- load_upf

UPF-604

(Error) The Golden UPF file can contain 1801 UPF commands only.

Description

Non 1801 UPF commands are not allowed in a Golden UPF file.

See Also

- load_upf

UPF-605

(error) Attribute %s in %s is ignored because the value does not match with the top most scope.

Description

The specified UPF attribute value does not match with the value on the top most scope. The attribute will be ignored. The default value of this attribute on top most scope is false.

Feedback

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

UPF-606

(warning) Resetting the value of attribute "%s" for "%s" to %s (new value).

Description

The specified UPF attribute was defined earlier. The attribute will be set to the new value.

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

UPF-607

(Warning) Attribute %s in %s is ignored. One or more power domains exist in the design.

Description

Attribute will be ignored because one or more power domainis exist in the design. Set the attribute for top level before defining any power domain. For any level, defining the attribute after defining power domain for that level will cause an error.

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

Feedback

UPF-608

(error) Attribute %s in %s is ignored. One or more level has the attribute set.

Description

Attribute will be ignored because it is set on the top level scope and one or more level has the attribute set already.

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

UPF-609

(error) Attribute %s in %s is ignored. Power domain is already defined for the cell.

Description

Attribute will be ignored because the cell already has power domain defined.

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

UPF-610

(warning) Isolation strategy %s for cell %s will be ignored because lower domain is missing.

Description

The isolation strategy is ignored because the cell is attached to lower domain boundary but the lower domain was not defined. When design attribute "lower_domain_boundary" is set to truei for a scope, lower domain boundary can be referenced from that scope

Feedback

even before creating the lower domain. However, the strategy will be ignored if the lower domain is not defined at all.

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

UPF-611

(error) Attribute %s in %s is ignored. %s cell %s has %s value.

Description

Attribute value false will be ignored because one of the descendent cell has true value. Attribute value true will be ignore because one of the ancestor cell has false value;

What Next

Look at your UPF.

See Also

- set_design_attributes
- set_port_attributes

UPF-612

(warning) Cell %s is set by two isolation strategies %s and %s. %s is ignored.

Description

If a cell is set by multiple isolation strategies, the tool will decide which one to take according to the precedence and report which one is ignored.

What Next

Look at two isolation strategies mentioned in the warning message and make sure the ignored one is correct for the specified pin.

See Also

- set_isolation

Feedback

UPF-613

(Warning) Rail mapping for port %s failed. Could not detect driver/reciever or pad pin for the port.

Description

UPF create pg pins for the ports. The pig pins primary power, ground, pwell and nwell. The rail mapping for these power pins are derived from the driver/receiver or pad pin connected to the port. If the port is dangling, the rail mapping could fail. This in turn could create SLG-216 warning.

What Next

Check if the ports are dangling. Remove dangling ports from design.

UPF-614

(information) Skipping explicit load_upf of HyperScale abstract for %s.

Description

In HyperScale flow, explicit load_upf for HS abstract will be ignored. Block UPF data will be automatically extracted during block run. If no UPF is present in block, nothing will be extracted. During top level run, the extracted block UPF will be automatically loaded in top level along with HS abstract. If top level has user specified load_upf for HS abstract, it will be ignored.

What Next

```
Please refer to documentation to understand guidelines and
 recommendations for
proper use of HyperScale analysis.
```

UPF-615

(Warning) Resolving type for net %s by name/voltage.

Description

PT issues this warning when it fails to detect the type of net using the UPF intent of the design. In such case, it will resolve the net type by using name first and if it fails then it will use the voltage. Any net with name containing VDD will be tagged as primary_power. Any net with name containging VSS will be tagged as primary_ground. This type will be used for detecting ETM pg_pin type as well. Any net containing voltage 0.0 will be tagged as primary_ground. Any net containing a valid voltage other then 0.0 will be tagged as primary_power.

What Next

Check the UPF commands for the design.

See Also

- set_domain_supply_net
- set_related_supply_net
- set_retention
- create_power_switch
- report_supply_net
- report_power_pin_info

UPF-616

(Warning) Ignoring variable %s. It is mutually exclusive with previously set variable %s.

Description

The variables *enable_golden_upf* and *link_keep_pg_connectivity* are mutually exclusive. Only one of these variables can be enabled at a time. The first one turns on the golden UPF flow and second one turns on the PG Verilog flow. In the PG Verilog flow, rail definitions and connectivity are derived from the PG netlist.

What Next

To set either variable to true, make sure the other one is set to false.

UPF-617

(Warning) Failed to detect clamp value of lib cell %s.

Description

The error occurs during auto detection of isolation strategy sense. Clamp value is needed to generate isolation_enable_condition during ETM generation. If this is missing ETM will not also tag the pin as "is_isolated". Timing analysis will not be effected by it.

What Next

Add proper clamp value in the specified isolation cell and rerun.

Feedback

UPF-618

(Warning) Found both clamp 0 and clamp 1 attribute in lib cell %s.

Description

The error occurs during auto detection of isolation strategy sense. Clamp value is needed to generate isolation_enable_condition during ETM generation. If this is missing ETM will not also tag the pin as "is_isolated". Timing analysis will not be effected by it.

What Next

Add proper clamp value in the specified isolation cell and rerun.

UPF-619

(Warning) Unable to set isolation control for cell %s.

Description

The error occurs during auto detection of isolation control. isolation control is needed for isolation_enable_condition during ETM creation. If this is missingi, ETM will not tag the port as "is_isolated". Timing analysis will not be effected by it.

What Next

Check lib cell clamp value. Check if isolation cell is properly connected to nets.

UPF-620

(Warning) Unable to find pg_net %s in internal database of pg_nets.

Description

The warning occurs during detection of pg_net and setting of primary supply of domain. All the instance connected to pg_net may get wrong supply net connections due to this issue.

What Next

Check pg verilog netlist to see if the pg net is connected with the pg pins.

UPF-621

(Warning) Unable to find upf supply net for pg_net %s.

Feedback

Description

The warning occurs during detection of pg_net and setting of primary supply of domain. All the instance connected to pg_net may get wrong supply net connectionsi due to this issue.

What Next

Check pg verilog netlist to see if the pg net is connected with the pg pins.

UPF-622

(Warning) Unable to find scope for hierarchical net %s.

Description

The warning occurs for hierarchical nets when net scope could not be found.

What Next

Check if net has correct hierarchy.

See Also

- create_supply_net

UPF-623

(Warning) Cannot create supply net for hierarchical net %s when it has domain defined.

Description

The warning occurs for hierarchical nets when it has domain defined. No nets will be created for this.

What Next

Remove the power domain associated with the command.

See Also

- create_supply_net

UPF-624

(Warning) Update option for set_retention cannot be specified with power and ground net.

Description

Update can only be used to merge the element list.

Feedback

What Next

Remove the power and ground net from *set_retention command*.

See Also

- create_supply_net

UPF-625

(Warning) -update option for set_isolation can be specified only with -elements, -exclude_elements, -domain and strategy_name. With -update at least one of these options must be specified: -elements and -exclude_elements.

Description

set_isolation -update is used for merging the existing element list in isolation strategy with new element list.

What Next

Fix the above error

See Also

- set_isolation

UPF-626

(Warning) -exclude_element option for set_isolation can be specified only with -update.

Description

-exclude_elements works with -update option to exclude elements from existing element lists of a given isolation strategy.

What Next

Fix the above error

See Also

- set_isolation

UPF-627

(Warning) Isolatation strategy %s has no elements in it. Cannot do the update.

Feedback

Description

-update option in set_isolation strategy cannot update element list for domain level strategy where elements are not present.

What Next

Fix the above error

See Also

- set_isolation

UPF-628

(Information) -exclude_elements in set_isolation will be ignored.

Description

PrimeTime ignores the -exclude_elements option in set_isolation. PrimeTime assumes that implementation tools are not going to insert any isolation cell in the excluded elements.

See Also

- set_isolation

UPF-629

(Warning) Invalid value for the argument

Description

The error occurs due to invalide arguement value.

What Next

Please check command man page for correct argument value.

See Also

- set_isolation

UPF-630

(Information) Maximum leaf level pg connection is limited to 10 per net.

Feedback

Description

Supply net might be explicitly connected to lots of instance level pg_pins. By explicit connection, it means connection using *connect_supply_net*. This is true for both UPF, UPF", golden UPF and PG verilog flow. In PG Verilog flow, the instance pg pins that are not connected to domain primary will have explicit connections too. *report_supply_net* will report 10 such explicit connections. Please use pg_pin_info attributes to derive leaf level pg pin connections per supply net.

See Also

- report_supply_net

UPF-631

(Warning) Net connect_supply_net will still be executed. Please check your UPF.

Description

The warning happens during *connect_supply_net* when net is not available under cell domain. For domain independent net, the scope of the net is lower than the scope of the cell domain. PT will still make the connection in this case.

What Next

Change the cell domain scope so it is same or lower than the net scope. Create domain dependent nets.

See Also

- connect_supply_net

UPF-632

(Error) Lib cell to store all of them. This could impact voltage value on logic pin.

Description

The error happens when libraray cell has more than 255 PG pin. PT currently cannot store more than 255 PG pins per cell. This could result in incorrect related_power/ground/pwell/nwell for logic pin. Eventually this will cause wrong voltage on logic pin.

What Next

Fix the library cell and rerun.

Feedback

UPF-701

(Error) Two options out of -supply, -group and -domain options cannot be specified at the same time.

Description

This error message occurs when two options out of *-supply*,*-group* and *-domain* options are specified at the same time in a single *add_power_state* command. A power state can be defined either on a supply set, group or on a domain. Multiple commands need to be used to specify power states on different objects.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-702

(Error) The '%s' option of add_power_state command must specify %s.

Description

This option of add_power_state command takes exactly one state name and the corresponding specifications.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-703

(Error) Power state format is not acceptable: %s.

Description

This error message occurs when the power state specified in the *-state* option of the *add_power_state* command does not comply with the UPF standard.

Feedback

What Next

Use the correct syntax for *add_power_state* and rerun the command.

See Also

- add_power_state

UPF-704

(Error) Unable to resolve supply_expr of state %s: %s.

Description

This error message occurs when an error is found in the definition of the supply_expr for the given state of the supply set.

If the following conditions are not met, the error is generated:

- The supply_expr may not include a Boolean operator other than &&.
- Each subexpression must have the syntax as: net == netstate.
- Only power and ground function nets may be used.
- Only FULL_ON and OFF states are allowed.
- Voltage must be defined for FULL_ON state.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-706

(Error) The power state %s already exists for supply set %s.

Description

This error message occurs when you try to define more than one power state with the same name for the supply set.

What Next

Define a unique name for the power state and run the command again.

Feedback

See Also

- add_power_state

UPF-707

(Error) The power state group %s already exists in the design.

Description

This error message occurs when you try to define more than one power state group with the same name in the design.

What Next

Define a unique name for the power state group and run the command again.

See Also

- create_power_state_group

UPF-708

(Error) Option -illegal is not supported for add_power_state. The command is ignored.

Description

This feature is not supported in the tool. The specification on the named power state is igored. Please adjust the usage accordingly.

What Next

Adjust the usage accordingly.

See Also

- add_power_state

UPF-709

(Warning) Voltage defined (%.2f) for power state %s does not match the operating voltage (%.2f) on the %s net of supply set %s.

Description

This warning message occurs when the voltage defined in the power state for the supply set does not match with the operating voltage value specified on the supply.

What Next

Use *set_voltage* command to assign an appropriate operating voltage to the function net of the supply set.

See Also

- add_power_state
- set_voltage

UPF-710

(Error) Power state group '%s' can not be found.

Description

Please check the power state group specified for the command. Make sure that the power state group exists in the current_scope.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- create_power_state_group

UPF-711

(Error) %s cannot be specified with -group in command add_power_state.

Description

This error message occurs when option *-supply_expr* is specified with the *-group* option in command *add_power_state*.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-712

(Error) The power state %s already exists for power state group %s.

Feedback

Description

This error message occurs when you try to define more than one power state with the same name for the power state group.

What Next

Define a unique name for the power state and run the command again.

See Also

- add_power_state

UPF-713

(Error) Unable to resolve logic_expr of state %s: %s.

Description

This error message occurs when an error is found in the definition of the logic_expr for the given state of the power state group.

If the following conditions are not met, the error is generated:

- The supply_expr may not include a Boolean operator other than &&.
- Each subexpression must have the syntax as: object == power_state.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-714

(Warning) Specifying group object in logic_expr is not yet supported.

Description

This feature is not currently supported in the tool. The specification on the named power state is ignored. Please adjust the usage accordingly.

What Next

Adjust the usage accordingly.

Feedback

See Also

- add_power_state

UPF-715

(Error) The named object '%s' in logic_expr for state '%s' can not be found.

Description

Please check the object name specified for the named state in add_power_state command. Make sure that the object exists in the current_scope.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-716

(Error) The power state '%s' specified in logic_expr is not defined for supply '%s'.

Description

Please check the power state specified in the logic_expr in add_power_state command. Make sure that the power state has been defined for the supply set object.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-717

(Error) Object '%s' appears more than once in logic_expr for state '%s'.

Description

Please check the power state specified in the logic_expr in add_power_state command.

What Next

Check the command man page for more details and correct it accordingly.

Feedback

See Also

- add_power_state

UPF-721

(Error) set_isolation_control is not allowed for strategy "%s" if any of -location/-isolation_sense/-isolation_signal is already defined for the strategy. Command is ignored.

Description

The error occurs if any of -location/-isolation_sense/-isolation_signal is already defined for the strategy. Please use set_isolation command to define these options.

What Next

Check set_isolation command for the strategy.

See Also

- set_isolation

UPF-722

(Error) set_retention_control is not allowed for strategy "%s" since one of the -save_signal/-restore_signal is already defined for the strategy using set_retention. Command is ignored.

Description

The error occurs if any of -save_signal/-restore_signal is already defined for the strategy using set_retention command. Please use set_retention command to define both of these signals.

What Next

Check set_retention command for the strategy.

See Also

- set_retention

UPF-730

(Error) The PST %s already exists in the design.

Feedback

Description

This error message occurs when you try to define more than one PST with the same name in the design.

What Next

Define a unique name for the PST and run the command again.

See Also

- create_pst

UPF-731

(Error) PST '%s' can not be found.

Description

Please check the pst name specified in the command. Make sure that the pst exists in the current_scope.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- create_pst

UPF-732

(Error) Incorrect specification for add_pst_state -state option.

Description

Please check option -state specified in the command. Make sure that the supply net states are specified correctly in the command.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_pst_state

Feedback

UPF-733

(Error) The state %s already exists for PST %s.

Description

This error message occurs when you try to define more than one state with the same name for the PST.

What Next

Define a unique name for the state and run the command again.

See Also

- add_pst_state

UPF-734

(Error) The power state '%s' specified in -state option is not defined for supply '%s'.

Description

Please check the power state specified for add_pst_state -state. Make sure that the power state has been defined for the supply net object.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_pst_state

UPF-735

(Error) Number of objects specified in add_pst_state -state do not match what were defined for pst '%s' by create_pst.

Description

This error message occurs when the number of objects specified in add_pst_state -state do not match the number of objects defined for the named pst by create_pst. Objects specified should be consistent across add_pst_state and create_pst for the same pst.

What Next

Make sure that the objects specified in add_pst_state -state match what were defined for the named pst in create_pst.

See Also

- add_pst_state
- create_pst

UPF-736

(Warning) Operating voltage (%.2f) on supply net %s does not match the voltage value (%.2f) defined in power state %s.

Description

This warning message occurs when the operating voltage value specified by set_voltage does not match the voltage value defined in the power state for the supply net.

What Next

Make necessary adjustment in either add_power_state or set_voltage.

See Also

- add_power_state
- set_voltage

UPF-737

(Warning) Operating voltage (%.2f) on supply net %s is not within the voltage range (%.2f - %.2f) defined in power state %s.

Description

This warning message occurs when the operating voltage value specified by set_voltage exceeds the voltage range defined in the power state for the supply net.

What Next

Make necessary adjustment in either add_power_state or set_voltage.

Feedback

See Also

- add_power_state
- set_voltage

UPF-738

(error) %s name '%s' in create_pst cannot have a wild char '*'.

Description

This error message occurs when a wild char '*' is used in create_pst -supplies for net name. The wild char is not allowed according to IEEE 1801.

What Next

Remove the wild char from create_pst.

See Also

- create_pst

UPF-739

(error) '%s' specified in create_pst -supplies is not a valid supply net name.

Description

This error message occurs when the name specified in create_pst -supplies does not match any UPF supply net in the design. UPF supply port object is not accepted in create_pst (a legacy feature).

What Next

Specify valid supply net names in create_pst.

See Also

- create_pst

UPF-740

(error) Each name specified in -supplies option of create_pst must refer to exactly one supply net object.

Feedback

Description

Each name specified in -supplies option of create_pst must refer to exactly one supply net object. It is an error upon ambiguity.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- create_pst

UPF-741

(Warning) Failed to create power switch for cell %s.

Description

This warning message occurs during pg verilog flow when auto power switch (upf_power_switch object) creation fails for certain cell.

What Next

Please check the net connection in PG verilog. The variable link_keep_unconnected_cells needs to be set to false.

UPF-742

(Warning) No power domain found for cell %s.

Description

This warning message occurs during pg verilog flow when user power domain is loaded.

What Next

Please check if the hierarchy is valid.

UPF-743

(Warning) No supply set found for domain %s.

Description

This warning message occurs during pg verilog flow when user defined power domain is loaded.

Feedback

What Next

Please check if correct element is listed in the element list.

UPF-744

(Warning) No all power domains have same supply set.

Description

This warning message occurs during pg verilog flow when user defined power domain is loaded.

What Next

Please check if correct element is listed in the element list.

UPF-745

(warning) Cell '%s' is already in the extent of power domain '%s'

Description

A cell cannot belong to multiple power domains.

What Next

Remove this cell from the list and re-run this command.

UPF-746

(Error) Supply net '%s' is not connected to top level port.

Description

This error message occurs when an given supply_net does not have any connection to top level port.

What Next

Please check your UPF.

UPF-747

(warning) There are '%d' supply nets without associated supply port.

Feedback

Description

It is a good practice to connect supply net to supply port. It gives a list of supply nets without associated supply port.

What Next

Use create_supply_port and connect_supply_net to fix the warning.

See Also

- create_supply_net
- connect_supply_net
- create_supply_port

UPF-748

(Error) Inconsistent syntax is not acceptable in add_power_state -state.

Description

This error message occurs when the power state specified in the *-state* option of the *add_power_state* command does not comply with the UPF standard.

What Next

Use the correct syntax for *add_power_state* and rerun the command.

See Also

- add_power_state

UPF-750

(Error) state can't be reassigned to functional net, earlier %s now %s.

Description

This error message occurs when you try to reassign state to functional net in a supply set's power state.

What Next

Give valid supply expression and run the command again.

Feedback

See Also

- add_power_state

UPF-751

(Error) voltage assigned to FULL_ON state can't be updated.

Description

This error message occurs when you try to change voltage of a funtional net's state in a supply set's power state.

What Next

Give valid supply expression and run the command again.

See Also

- add_power_state

UPF-753

(Error) power state can't be reassigned to the supply set in a group state of a pst group.

Description

This error message occurs when you try to reassign power state to the supply set in a group state of a pst group.

What Next

Give valid expression and run the command again.

See Also

- add_power_state

UPF-754

(Error) Extra group state can only be added with -update option of the command to the pst group %s.

Description

This error message occurs when you try to add extra group state to a pst group without add_power_state -update

Feedback

What Next

Use the update option and run the command again.

See Also

- add_power_state

UPF-755

(Information) Filename read from set_app_var upf_name_map '%s' overriding verilog pragma.

Description

The file name was read from set_app_var upf_name_map based on higher precedence.

What Next

Tcl global variable upf_name_map has a higher precedence than upf_name_map pragma in Verilog netlist.

UPF-756

(Error) Object %s is neither a port nor a hierarchical pin.

Description

The set_port_attributes command needs only ports or hierarchical pins.

What Next

Please specify only hierarchical pins or ports in set_port_attributes command.

UPF-757

(Information) Isolation sense for cell %s is determined to be %s.

Description

This gives sense information for isolation cell in PG verilog flow.

UPF-758

(Information) Skip overwriting the voltage on nets in block.

Feedback

Description

The specified nets already have a voltage set by block model.

What Next

Please check the block model.

UPF-759

(Warning) The %s of domain %s will be located in %s ,outside of its domain %s.

Description

It is an inconsistency,if the switch implementation is placed in a hierarchy that is not in the extent its domain.

UPF-760

(Error) The given switch %s is not found.

Description

The specified switch does not exist.

UPF-761

(Error) Incorrect number of arguments specified with '%s'.

Description

This error message occurs when an invalid number of arguments is speci- fied with the -function option of the create_supply_set command or with the -supply option of the create_power_domain command.

The -supply option in create_power_domain only accepts one argument, single or as a pair of supply_set_ref with handle.

To provide multiple supply_set_handle you can use -supply option multiple times.

What Next

Provide the correct number of arguments for the -function or the -sup- ply option in the following format:

-function {function_name supply_net_name}

-supply {supply_set_handle_name supply_set_name}

Feedback

See Also

- create_power_domain
- create_supply_set

UPF-762

(Error) -reset and -primary options are exclusive.

Description

This error message occurs when -primary option is used with -reset option in set_equivalent command.

What Next

Please remove -primary from the command and retry.

See Also

- create_power_domain
- create_supply_set

UPF-763

(Error) Please specify any one of -nets or -sets option.

Description

This error message occurs when set_equivalent command is issued without -nets -sets options.

What Next

Please specify either -nets or -sets options and retry.

See Also

- create_power_domain
- create_supply_set

UPF-764

(warning) '-function' option is not specified for supply set.

Feedback

Description

When a supply set is specified with enable_bias attribute, -function option must be specified to provide the associated supply nets with supply set functions.

What Next

Check the command man page for more details and correct it accordingly.

UPF-765

(Error) Element specified '%s' through set_isolation -element options is not valid.

Description

An isolation strategy cannot be defined by the set_isolation command for a cell if it is a black box.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- set_isolation

UPF-766

(Error) Create_supply_port command is disabled in PG Verilog flow.

Description

In PG verilog flow, supply ports are created using the netlist. Hence create_supply_port command is disabled. If you are loading the UPF, please set link_keep_pg_connectivity variable to FALSE.

What Next

If you are loading the UPF, please set link_keep_pg_connectivity variable to FALSE.

See Also

- load_upf

UPF-770

(error) Attribute 'enable_state_propagation_in_add_power_state' of 'set_design_attributes' command is enabled in the scope of domain %s.

Feedback

Description

Above attribute must be disabled in the scope of domains specified in add_power_state command.

What Next

Disable above attribute in the scope of domain %s.

See Also

- set_design_attributes
- add_power_state

UPF-773

(Error) Power state can't be reassigned to the supply set in a domain state of a power domain .

Description

This error message occurs when you try to reassign power state to the supply set in a domain state of a power domain.

What Next

Give valid expression and run the command again.

See Also

- add_power_state

UPF-774

(Error) Extra domain state can only be added with -update option of the command to the power domain %s.

Description

This error message occurs when you try to add extra domain state to a power domain without add_power_state -update.

What Next

Use the update option and run the command again.

See Also

- add_power_state

UPF-777

(Error) The power domain %s already exists in the design.

Description

This error message occurs when you try to define more than one power domain with the same name in the design.

What Next

Define a unique name for the power domain and run the command again.

See Also

- create_power_domain
- add_power_state

UPF-780

(Error) Power domain '%s' can not be found.

Description

Please check the power domain specified for the command. Make sure that the power domain exists in the current_scope.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- create_power_domain
- add_power_state

UPF-781

(Error) %s cannot be specified with -domain in command add_power_state.

Feedback

Description

This error message occurs when option *-supply_expr* is specified with the *-domain* option in command *add_power_state*.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-782

(Error) Domain state %s already exists for power domain %s.

Description

This error message occurs when you try to define more than one domain state with the same name for the power domain.

What Next

Define a unique name for the domain state and run the command again.

See Also

- add_power_state

UPF-783

(Error) Unable to resolve logic_expr of state %s: %s.

Description

This error message occurs when an error is found in the definition of the logic_expr for the given state of the power domain.

If the following conditions are not met, the error is generated:

- The supply_expr may not include a Boolean operator other than &&.
- Each subexpression must have the syntax as: object == power_state.

What Next

Check the command man page for more details and correct it accordingly.

See Also

- add_power_state

UPF-784

(Warning) Specifying domain object in logic_expr is not yet supported.

Description

This feature is not currently supported in the tool. The specification on the named power state is ignored. Please adjust the usage accordingly.

What Next

Adjust the usage accordingly.

See Also

- add_power_state

UPF-785

(Error) The value specified by %s is out of range.

Description

You are receiving this error message because a set_voltage command has been specified with a nominal value that is out of range (either smaller than the max_delay_voltage or greater than the min_delay_voltage). The specified nominal voltage value must be within the voltages (-min_voltage, max_voltage) specified with the command.

What Next

Adjust the nominal voltage values and re-issue the command.

UPF-786

(error) Power domain of '%s' is not specified.

Description

Excluded element from the element list does not have any power domain specified. Every instance must belong to a power domain after all create_power_domain commands are read.

Feedback

See Also

- create_power_domain

UPF-787

(Information) Supply set '%s' is already associated or refined.

Description

An handle would be associated with multiple supply sets. To understand how the association works, please read the following.

create_power_domain foo -handle {s1 s2} By default, it would create two implicit supply set s1 & s2 and associate with each other. Association group(g1) head would be s1 and its members would be s2.

create_power_domain bar -handle {s3 s2} By default, it would create an implicit supply set s3, s2 is already existing. After association, group(g1) head would be s3 and its members would be s2 and s1

create_power_domain foobar -handle {s2 s4} By default, it would create an implicit supply set s4, s2 is already existing. After association, group(g1) head would be s3 and its members would be s2, s1 & s4

create_power_domain foofoobar -handle {s5 s6} By default, it would create two implicit supply set s5 & s6 and associate with each other. Association group(g2) head would be s5 and its members would be s6.

create_power_domain foofoobarbar -handle {s3 s5} Since both of the supply sets already esiting, it would not create any implicit supply set. Association would happen between the groups of s3(g1) & s5(g2). After association, group(g1) head would be s3 and its members would be s2, s1, s4 & s5. Group g2 would be deleted.

What Next

Check the command for intended behavior

UPF-788

(Warning) Cannot open file '%s'.

Description

The file name provided to *load_upf* cannot be opened. Possible reasons for this are that the file does not exist in the search path specified or that it does not have read permissions.

Feedback

What Next

Verify the location of the file to be read on and its permissions. Once the file has been verified re-run *load_upf*.

UPF-789

(Warning) Cannot find the pg_pin %s in the specified cell/lib_cell.

Description

The pg_pin specified in the set_ignore_power_switches command doesn't exist on the cell or lib_cell object specified in the command.

What Next

Verify the names of pg_pin specified.

VAR

VAR-001

(Warning) Ignoring invalid token '%s' in gvar '%s' setting.

Description

You receive this message if an invalid string/toekn is passed to a gvar setting.

What Next

Check the valid token names for the gvar setting.

VAR-002

(Warning) Gvar '%s' is frozen and can no longer set token '%s'

Description

You receive this message if an gvar is set to be not modified by user.

VAR-003

(Warning) Invalid value '%s' for boolean token '%s'

Description

You receive this message if an invalid value is specified for a boolean value token

Feedback

VAR-004

(Warning) Cannot change value of variable '%s'

Description

Previous actions involving encrypted files are blocking changing this variable value for security reasons.

VAR-005

(Error) Cannot change value of variable '%s' to '%s'

Description

Changing the variable to the specified value is not allowed because it will affect parasitics background reading.

What Next

Set the variable to the specified value before any parasitics reading takes place.

WINSEL

WINSEL-001

(Warning) Invalid object class %s. Supported objects are : %s

Description

The specified object class does not exist.

What Next

Verify that the object class exists and the spelling is correct.

WINSEL-002

WINSEL-002 (ERROR) Bad syntax for rectangle: %s

Description

The syntax specified for the rectangle was not acceptable. Correct syntax is, a rectangle must be of the form

{ <lower_left_point> <upper_right_point> }

Feedback

and the point is

{ <x_dist > <y_dist> }

Note that distances are fixed point numbers, like 17.25 or 13000.1 or 2500.

What Next

Please fix the syntax and try again.

WINSEL-003

(error) Nothing matched for search constraints.

Description

No objects satisfied the constraints you specified.

What Next

Check the command arguments you gave, and see if the constraints can be changed or relaxed to make a match.

WSCR

WSCR-001

(error) Cannot open the output file %s

Description

The output file for write_script cannot be opened.

What Next

Verify that the path for the file name exists. If the path does exist, make sure you have access permission.

WSCR-002

(information) SDC supports a subset of the constraints supported by PrimeTime. Some constraints cannot be preserved by the write_sdc command.

Feedback

Description

The Synopsys Design Constraints (SDC) format is a subset of the constraints supported by PrimeTime. Some of the constraints that you applied to the design cannot be written to the SDC file. Others might only be partially written.

Constraints are written to the SDC file with the following limitations:

- For the *set_driving_cell* command, the *-min* and *-max* options are unsupported.
- For the *set_port_fanout_number* command, the *-min* and *-max* options are unsupported.

What Next

Ensure the constraints that you are using are accurate.

See Also

- set_driving_cell
- set_port_fanout_number
- write_sdc

WSCR-003

(Information) The design has rise/fall qualified exceptions which will not be written out.

Description

Rise/Fall qualified exceptions are only supported by Primetime. So *write_script* will not write out these exceptions for dcsh or dctcl mode. *write_sdc* also will not write these exceptions.

WSCR-004

(warning) Your SDC output may contain ambiguous names because you have set the variable sdc_write_unambiguous_names to FALSE.

Description

Beginning with version 1.2, the Synopsys Design Constraints (SDC) format has features ensuring that the cell, net, pin, lib_cell, and lib_pin names written to the file are unambiguous. Some third party applications do no understand these features.

You can set the *sdc_write_unambiguous_names* variable to *false* to suppress these features. This warning reminds you that the setting of this variable may cause your SDC output to be ambiguous.

Feedback

What Next

Verify that you really want to disable the writing of unambiguous names. Review the man pages for the *write_sdc* command and the *sdc_write_unambiguous_names* variable.

See Also

- write_sdc
- sdc_write_unambiguous_names

WSCR-005

(Warning) Clock '%s' created with -add option will not be written out.

Description

Multiple clock defination on same pin/port is only supported by PrimeTime. So *write_script* will not write out these clocks for dcsh or dctcl mode. *write_sdc* also will not write these clocks.

WSCR-006

(warning) Cannot disable %s objects from %s to %s.

Description

The write_script command has found multiple arcs between the pins noted in the message, such that a non-zero subset of the arcs is disabled and at least one arc is not disabled. Moreover, the write_script command is unable to generate a *filter expression* based on the attributes of the arc objects that can completely distinguish the subset of disabled arcs from the non-disabled ones. If it is the case that some, but not all, of the disabled arcs can be distinguished, then the write_script command will cause that subset only to be disabled.

What Next

To match the set of disable arcs between the pins, you need to replicate the methodology by which the arcs were disable in the first place and append the necessary commands to the script file generated by the write_script command.

WSCR-007

(error) %s option cannot be specified without %s option for write_sdc command.

Feedback

Description

The first option mentioned should only be specified with the second option for write_sdc command.

What Next

Add the second specified option along with the first specified option for write_sdc command.

WSCR-008

(error) %s global variable cannot be set to true if %s global variable is already set to true.

Description

The first global variable must not be set to true if the second global variable is already set to true. Only one of the global variables must be true at one time.

What Next

Set the first global variable to false and then set the second global variable to true.

XTALK

XTALK-001

(information) Starting crosstalk aware timing iteration %d.

Description

The timing update is being performed in the crosstalk aware mode. In this mode multiple crosstalk aware timing iterations might be performed.

What Next

For more information, see the PrimeTime user guides.

XTALK-002

(information) Setting timing_allow_short_path_borrowing to TRUE.

Description

You have received this informational message because in crosstalk aware timing mode, the *timing_allow_short_path_borrowing* variable must be set to *true* to perform accurate crosstalk analysis.

What Next

This is an informational message. No action is required on your part. For more information, see the *PrimeTime User Guide*.

See Also

- si_enable_analysis
- timing_allow_short_path_borrowing

XTALK-003

(information) Setting timing_save_pin_arrival_and_slack to TRUE.

Description

You have received this informational message because in crosstalk aware timing mode, the *timing_save_pin_arrival_and_slack* variable must be set to *true* to perform accurate crosstalk analysis.

What Next

This is an informational message. No action is required on your part. For more information, see the PrimeTime user guides.

See Also

- si_enable_analysis
- timing_save_pin_arrival_and_slack

XTALK-005

(information) Switching to on-chip-variation analysis type.

Description

Crosstalk analysis requires the on-chip-variation analysis type. The main reason is that minimum and maximum arrival times on aggressor nets are used to compute crosstalk effect on both minimum and maximum arrival times on the victim net. That means that the design can be in both minimum and maximum operating conditions at the same time.

What Next

After you are finished with crosstalk analysis use the *set_operating_conditions* command to return the design to the desired analysis type.

Feedback

See Also

- set_operating_conditions
- si_enable_analysis

XTALK-006

(information) Maximum number of crosstalk iterations %d was changed to %d.

Description

The *si_xtalk_exit_on_max_iteration_count* variable must be greater than or equal to 1.

What Next

Use only valid range of maximum iteration count.

See Also

- si_xtalk_exit_on_max_iteration_count

XTALK-007

(error) Command read_parasitics -keep_capacitive_coupling requires si_enable_analysis set to TRUE.

Description

You receive this message if you execute the *read_parasitics* command with the *-keep_capacitive_coupling* option, but you have not enable crosstalk analysis; that is, the *si_enable_analysis* variable is set to *false*. The *-keep_capacitive_coupling* variable is part of crosstalk analysis; and you must enable crosstalk analysis to use this option.

What Next

If you want to use the *-keep_capacitive_coupling* option, set the *set si_enable_analysis* variable to *true*. Next, reexecute the *read_parasitics -keep_capacitive_coupling* command. Otherwise, reexecute the *read_parasitics* command without setting the *-keep_capacitive_coupling* option.

See Also

- read_parasitics
- si_enable_analysis

Feedback

XTALK-008

(information) Crosstalk analysis was interrupted by user before iteration %d.

Description

You receive this message if PrimeTime receives an interrupt signal while inside the crosstalk iteration loop. The interrupt probably occurred because you pressed Control-C on the UNIX workstation. As with other crosstalk exit criteria, PrimeTime completes the current iteration, then exits. The message informs you of the iteration number that was completed. For more information about exit criteria, see the manual page for any of the *si_xtalk_exit_on_** variables.

What Next

This is an informational message only; no action is required on your part. Be aware that fewer iterations of crosstalk analysis were performed; therefore, reports are more pessimistic.

See Also

- si_xtalk_exit_on_max_iteration_count

XTALK-010

(information) Design has signal integrity data but signal integrity analysis is disabled.

Description

You received this error message because the *si_enable_analysis* variable has been set to *false* while the design still has signal integrity data, such as coupling capacitors. Signal integrity analysis is not performed. Thus the signal integrity data is redundant and only increases memory usage.

What Next

First, determine whether you want to perform signal integrity analysis. If you do, set the *si_enable_analysis* variable to *true*. If you do not and memory usage is not an issue, no action is required on your part. However, if memory usage is important, avoid using the *read_parasitics* command with the *-keep_capacitive_coupling* option to save memory.

See Also

- read_parasitics
- si_enable_analysis

Feedback

XTALK-011

(information) Signal integrity analysis is enabled but the design has no signal integrity data.

Description

You received this error message because the *si_enable_analysis* variable has been set to *true* while the design has no signal integrity data, such as coupling capacitors.

What Next

First determine whether you want to perform signal integrity analysis. If you do, use the *read_parasitics* command with the *-keep_capacitive_coupling* option, and analyze the output to verify that coupling parasitics data has been correctly read in. If you do not want to perform signal integrity analysis, set the *si_enable_analysis* variable to *false*.

See Also

- read_parasitics
- si_enable_analysis

XTALK-012

(information) Signal integrity analysis is disabled. All PrimeTime SI related global variables are no longer in use. Any coupling capacitors are reduced to ground by the reduction factor of one.

Description

You receive this message because the *si_enable_analysis* variable is set to its default of *false*.

What Next

First, determine whether you want to perform regular PrimeTime analysis. If you want to enable PrimeTime SI and the crosstalk-aware timing calculation mode, set the *si_enable_analysis* variable to *true*. If you want to reduce the coupling capacitors with another factor, the annotated parasitics has to be removed and a new one read in by using the *read_parasitics* command with the appropriate factor.

Feedback

See Also

- read_parasitics
- remove_annotated_parasitics
- si_enable_analysis

XTALK-014

(Warning) Crosstalk analysis with logically exclusive clocks could be conservative.

Description

You receive this warning message because you have enabled the *-logically_exclusive* of the *set_clock_groups* command, which is applied when the signal integrity analysis is enabled (the *si_enable_analysis* variable is set to *true*) or vice versa. This is to inform you that signal integrity analysis result could be pessimistic with exclusive clocks compared to analyzing each clock group separately. Even when the clocks are exclusive, they still might be active and physically coupled before the clock selection MUX. Crosstalk correctly analyzes this. The crosstalk affect after the clock selection MUX could be over estimated when the victim and aggressor arrival windows driven by clocks, which are exclusive to each other.

What Next

If this pessimism is not acceptable, one of the following approach could be adopted.

(1) If the clocks are physically exclusive to each other use the *-physically_exclusive* option.

(2) Only the clocks that could coexist in the chip at the same time should be created or derived for a single analysis.

(3) Only the clocks of one clock group are activated at any time using the *set_active_clock* command

(4) The proper set of clocks propagated by setting the *set_case_analysis* command on the clock selection MUXes.

When a proper set of clocks are analyzed together, it runs faster by analyzing only feasible crosstalk affect. The process of clock generation, activation, and selection should be carefully done in the static timing analysis environment, to match the tool with the behavior of the chip.

See Also

- remove_clock_groups
- set_clock_groups

Feedback

- set_case_analysis
- set_active_clocks
- si_enable_analysis
- pba_enable_path_based_physical_exclusivity

XTALK-015

(information) Setting rc_cache_min_max_rise_fall_ceff to TRUE.

Description

You receive this informational message because in crosstalk aware timing mode, the *rc_cache_min_max_rise_fall_ceff* variable must be set to *true* for accurate crosstalk analysis.

What Next

This is an informational message. No action is required on your part. For more information, see the PrimeTime user guides.

See Also

- si_enable_analysis
- rc_cache_min_max_rise_fall_ceff

XTALK-016

(information) Starting incremental signal integrity update.

Description

Update of timing and noise data is done incrementally (faster than full default update). The incremental updates are faster because only the affected parts of the design are updated. For example, after size_cell the nets connected to the cell, their aggressors are reselected and their fanout cone are reevaluated. Due to iterative nature of signal integrity updates the incremental update may not perfectly match the full update if number of iterations is small. The difference should be marginal in most case; however, if it is significant, perform a full update or increase the number of iterations.

What Next

This is an informational message. No action is required on your part. However, you can trade off accuracy for performance by forcing full update by using the *update_timing -full* command.

Feedback

See Also

- update_noise
- update_timing
- si_xtalk_exit_on_max_iteration_count

XTALK-017

(information) Setting timing_update_effort to low.

Description

You received this informational message because incremental update of timing and noise has been enabled. Where possible, PrimeTime SI automatically performs an incremental timing update when a change occurs that invalidates the timing of the design.

Incremental signal integrity analysis generally requires more timing information to be updated. For example, nets coupled with a changed net need to be updated. PrimeTime SI reverts to a full timing update depending on the number and severity of changes (see PTE-018).

The *timing_update_effort* variable must be set to *low* to ensure that the timing update is incremental.

What Next

This is an informational message. No action is required on your part. For more information, see the PrimeTime user guides.

See Also

- update_noise
- update_timing
- si_xtalk_exit_on_max_iteration_count
- timing_update_effort
- PTE-018
- XTALK-016

XTALK-018

(information) Command '%s' requires signal integrity analysis enabled.

Description

You received this error message because the *si_enable_analysis* variable has been set to *false* while the commend requires signal integrity analysis.

What Next

Determine whether you want to perform signal integrity analysis. If you do, set the *si_enable_analysis* variable to *true*. to save memory.

See Also

- report_si_bottleneck
- si_enable_analysis

XTALK-019

(information) report_si_bottleneck found zero net to report.

Description

You received this error message because the *report_si_bottleneck* command has filter out all the candidate nets.

What Next

Relax the filtering criteria of this command. For example, include clock nets, lower the number of active aggressors, include both min and max analysis, or increase the slack (by make it more positive.)

See Also

- report_si_bottleneck

XTALK-020

(information) Setting rc_driver_model_mode to basic.

Description

You receive this informational message because in crosstalk aware timing mode, the *rc_driver_model_mode* variable must be set to *basic*. The advanced driver model is not supported in crosstalk analysis.

What Next

This is an informational message. No action is required on your part. For more information, see the PrimeTime user guides.

Feedback

See Also

- si_enable_analysis
- rc_driver_model_mode

XTALK-021

(Warning) Usage of the -slack_lesser_than option in report_si_bottleneck requires that timing_save_pin_arrival_and_slack be set to true.

Description

You received this error message because the *timing_save_pin_arrival_and_slack* variable is set to *false*, while the command option requires that it is set to *true*. The default value of the *timing_save_pin_arrival_and_slack* variable is *false* to save memory.

What Next

No explicit action is required on your part - PrimeTime sets the value of the *timing_save_pin_arrival_and_slack* variable to *true* when a command that requires it is issued.

See Also

- report_si_bottleneck

XTALK-022

(Warning) For computing a common clock period for all clocks between victim and its effective aggressors PrimeTime limits the waveform expansion of the smallest period to be no more than %d times and the waveform expansion of the largest period to be no more than %d times. No common clock period is possible satisfying these limits, PrimeTime is doing the clock expansion based on these limits for window alignment.

Description

PrimeTime computes the common clock period of a set of related clocks on victim and effective aggressors. The commmon clock period is evenly divisible by every clock in the set. Since clock periods can be arbitrary floating-point numbers, PrimeTime limits the common clock period from becoming too large, PrimeTime must restrict clock waverform expansions by the limits mentioned in the warning message for xtalk, noise, and MIS window alignment.

If PrimeTime computed common clock period bounded by these limits, you can model all effective aggressors with *set_si_delay_analysis -ignore_arrival [get_nets <aggressor nets>]*.

Feedback

What Next

Use *set_si_delay_analysis -ignore_arrival* for infinite window alignment.

XTALK-101

(information) Crosstalk net reselection: Pin Slack Thresholds - Min-mode %.2f, Max-mode %.2f

Description

These are the crosstalk nets that are reselected for detailed crosstalk aware timing calculation in the next iteration of timing analysis.

What Next

For more information, see the user guide.

XTALK-102

(information) Net reselection criteria was : Critical Path Only.

Description

These are the crosstalk nets that are reselected for detailed crosstalk aware timing calculation in the next iteration of timing analysis.

What Next

For more information, see the user guide.

XTALK-104

(information) Removing crosstalk between nets %s and %s.

Description

You receive this informational message because the annotation on a net is being removed. Because of this, all coupling capacitances between the net being removed and aggressor nets are put to ground on the aggressor nets.

What Next

This is an informational message. No action is required on your part. For more information, see the user guide.

Feedback

See Also

- remove_annotated_parasitics

XTALK-105

(information) Number of nets evaluated in the previous iteration: %d.

Description

This message specifies the number of nets that were evaluated during each crosstalk-aware timing update iteration. This number includes the number of selected nets in that iteration plus any other net in its fanout cone of logic that needed a timing update.

What Next

For more information, see the PrimeTime user guides.

See Also

- remove_annotated_parasitics

XTALK-107

(Warning) Cannot remove %s that was not set on net(s) %s %s.

Description

You receive this warning message because the behavior that you are trying to reset was not set on the net. This can also be due to the following reasons.

1. You have set the net to be globally excluded or separated from all the nets and are trying to remove an individual pairwise behavior.
2. You have set the net to be pairwise excluded or separated from some nets and you are trying to remove the exclusion or separation globally.
3. The exclusive group that you specified was not set.

What Next

You can use the *report_si_delay_analysis*, *report_si_noise_analysis*, or *report_si_aggressor_exclusion* commands to view the exclusions, separations, or aggressor exclusive groups applied on the specified nets respectively.

For more information, see the PrimeTime user guides.

Feedback

See Also

- report_si_delay_analysis
- report_si_noise_analysis
- report_si_aggressor_exclusion
- remove_si_delay_analysis
- remove_si_noise_analysis
- remove_coupling_separation
- remove_si_aggressor_exclusion

XTALK-201

(Warning) For clock OCV pessimism reduction, timing_remove_clock_reconvergence_pessimism should be enabled. Without it, setting this variable has no effect on the analysis.

Description

You receive this error message because you can only set the *timing_remove_clock_reconvergence_pessimism* variable to *true* when the clock on-chip variation (OCV) pessimism reduction is enabled.

What Next

Set the *timing_remove_clock_reconvergence_pessimism* variable to *true*.

See Also

- pba_enable_xtalk_delay_ocv_pessimism_reduction

XTALK-302

(Information) The higher iteration is less likely to improve the result, so exiting from the iteration loop.

Description

You received this message because the adaptive reselection found that higher iteration recalculation has lower potential for quality of result (slack, path arrival) improvement. It is exiting from the iteration loop.

Feedback

What Next

If the timing violation shows even from the uncoupled analysis, the constraint and the design should be fixed.

See Also

- set_si_delay_analysis

XTALK-303

(Information) Crosstalk Composite aggressor mode is %s with threshold(s)-(%s).

Description

This message informs you about the composite aggressor settings.

In normal mode, PrimeTime SI combines the effect of some small aggressors (possibly including filtered ones) into a single composite aggressor, thereby accounting for their worst-case effects in an efficient manner.

In the statistical mode, all of the small aggressors below the threshold are still included as part of the composite aggressor. However, some statistical analysis is applied to adjust the composite bump height to a lower level. This analysis considers the finite probability that all the small aggressors will switch simultaneously to adversely affect the victim. This adjustment results in a more realistic, less pessimistic analysis than the normal composite aggressor mode.

An aggressor is treated as part of the composite aggressor if the bump height is below the threshold (Noise Peak Ratio). The *si_xtalk_composite_aggr_noise_peak_ratio* variable controls this threshold. In statistical mode, PrimeTime SI statistically combines the individual aggressors below the threshold. It determines the largest composite aggressor bump height having a probability of occurrence no greater than a certain value (percentile). The *si_xtalk_composite_aggr_quantile_high_pct* variable controls this percentile value.

What Next

This is an informational message. No action is required on your part. For more information, see the user guide.

See Also

- si_xtalk_composite_aggr_mode
- si_xtalk_composite_aggr_noise_peak_ratio
- si_xtalk_composite_aggr_quantile_high_pct

Feedback

XTALK-304

(information) Overriding net reselection with match mode file %s.

Description

This message informs you about overriding the net reselection algorithm using an external text based file.

What Next

This is an informational message. No action is required on your part.

XTALK-305

(error) Invalid match mode file %s. Aborting reselection override.

Description

This message informs about overriding the net reselection algorithm using an external text based file.

What Next

Make sure the file is valid. You might need to rerun the top-level analysis to generate a valid match mode file.

XTALK-307

(information) Setting 'max' for -triplet_type for multi-valued SPEF analysis.

Description

This message informs that the max triplet values are used for grounded capacitance and resistance if they are given in triplet format while multi-valued SPEF analysis.

What Next

This is an informational message. No action is required on your part.

XTALK-308

(information) Setting -keep_capacitive_coupling for multi-valued SPEF analysis.

Description

This message informs that the option -keep_capacitive_coupling is automatically used for multi-valued SPEF analysis.

Feedback

What Next

This is an informational message. No action is required on your part.

---

test